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EXC-1553PCMCIA

MIL-STD-1553
TEST AND SIMULATION BOARD
FOR PCMCIA COMPATIBLE COMPUTERS

User's Manual

EXCALIBUR SYSTEMS, INC.

311 Meacham Avenue ◆ Elmont ◆ NY 11003 ◆ Tel. (516) 327-0000 ◆ Fax (516) 327-4645

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What is in this manual?

This manual is divided into the following ten chapters:

Chapter 1, "**Introduction**" provides an overview of the EXC-1553PCMCIA card, and discusses card installation and 1553 bus connections.

Chapter 2, "**PCMCIA Bus Interface**" describes the EXC-1553PCMCIA attribute memory map, card information structure, configuration registers and the common memory map.

Chapter 3, "**Bus Controller Operation**" discusses bus controller message processing, control registers in BC mode, bus controller architecture, command block chaining, memory architecture, and MIL-STD-1553A operation in BC mode.

Chapter 4, "**Remote Terminal Operation**" discusses RT message processing, control registers in RT mode, the descriptor block, data structures, mode code and subaddress, encoder and decoder, RT-RT transfer compare, terminal address, reset, and MIL-STD-1553A operation in RT mode.

Chapter 5, "**Bus Monitor Operation**" discusses bus monitor message processing, control registers in BM mode, bus monitor architecture, bus monitor block chaining, memory architecture, RT/concurrent monitor operation and MIL-STD-1553A operation in BM mode.

Chapter 6, "**Interrupt Architecture**" provides an overview of the interrupt architecture of the EXC-1553PCMCIA and discusses the interrupt identification word and the interrupt address word.

Chapter 7, "**Switching Modes of Operation**" explains switching between the modes of EXC-1553PCMCIA operation.

Chapter 8, "**Mechanical and Electrical Specifications**" presents the EXC-1553PCMCIA connectors, mechanical outline and power requirements.

Chapter 9, "**Ordering Information**" presents the part number details required for ordering an EXC-1553PCMCIA card.

Chapter 10, "**Appendices**" provides information on the MIL-STD-1553B word and message formats.

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1 Introduction

Chapter 1 provides an overview of the EXC-1553PCMCIA avionics communication board. The following topics are covered:

- "Overview," page 1-1
- "Installation," page 1-3
- "1553 Bus Connections," page 1-13

1.1 Overview

The EXC-1553PCMCIA is an intelligent, memory-mapped MIL-STD-1553 interface card which complies with the Personal Computer Memory Card International Association (PCMCIA Release 2.1) standard, including Plug and Play. The EXC-1553PCMCIA card's small size and suitability for PCMCIA compatible notebook computers with Type II slots make it a total solution for developing and testing 1553 interfaces and for performing system simulation of the MIL-STD-1553 bus, both in the lab and in the field. The EXC-1553PCMCIA is designed around the UT69151 DX (UTMC's SUMMIT™ LX/DX 1553 controller).

The EXC-1553PCMCIA contains 64K words of dual-port static RAM and an additional 32 words of control registers, all mapped within the Common Memory space. The unit also contains an EEPROM-based Card Information Structure (CIS) within the Attribute Memory space. This card gives you direct access to the memory-mapped control registers in the SUMMIT chip and the control registers in the dual-port RAM. Operation of the card is controlled by accessing the control registers, which you can modify, along with data, in real time.

The EXC-1553PCMCIA comes complete with menu-driven software, a C-driver software library including source code, and a MIL-STD-1553 adapter cable.

The EXC-1553PCMCIA-R option comes with a ruggedized hardwired cable connection. For more details about the EXC-1553PCMCIA-R option, see "Mechanical and Electrical Specifications," page 8-1 and 8-3.

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EXC-1553PCMCIA Board Features:

- Operates as BC, RT, Bus Monitor, RT/Concurrent Monitor
- Multiple protocol capability:
  - MIL-STD-1553A
  - MIL-STD-1553B
- 64 K words memory mapped, dual-port RAM
- Message illegalization
- Real Time operation
- Polling or Interrupt driven
- Programmable broadcast mode
- Major and Minor frames
- Programmable Intermessage Gap
- Complies with PCMCIA standard release 2.1
- PCMCIA Type II PC card
- Plug and Play compatible
- 5 volt supply only
- Power down mode for low power consumption
- All logic self contained; no external module required
- EEPROM based Card Information Structure (CIS)
- 16-bit time tag
- Menu-driven software available
- C software library included

The board has four modes of operation:

- Bus Controller (BC) mode
- Remote Terminal (RT) mode
- Monitor mode
- RT with Concurrent Monitor operation

See "Ordering Information," page 9-1 for part number details.

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1.2 Installation

Inserting the EXC-1553PCMCIA card into your computer is a simple procedure, as described below. The EXC-1553PCMCIA card is delivered with software compatible with several operating systems. Card installation includes installing the card and the software for each system. For information about installing the accompanying drivers, see **ReadMe.txt** on the *EXC-1553PCMCIA Drivers* diskettes that came with your card.

Inserting the EXC-1553PCMCIA card:

NOTE The adapter cables may be connected to the card either before or after the card is inserted into the PCMCIA slot on the computer. In addition, the cables may be connected to and disconnected from the card while power to the computer is turned on, but not while the card is transmitting over the bus.

1. Open the expansion slot cover.
2. Insert the EXC-1553PCMCIA card with the label facing up (see Figure 1-1). When the card is almost all the way in the slot, push firmly, but gently, to ensure a firm connection with the computer. Do not force the card into position.

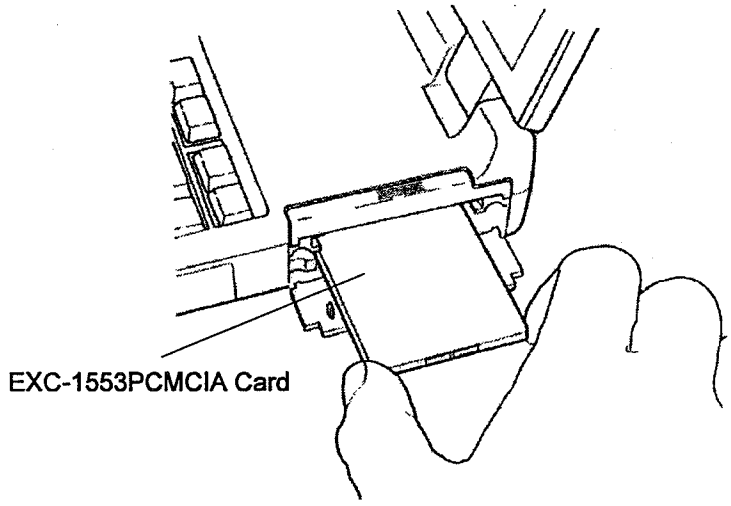


Figure 1-1. Inserting the EXC-1553PCMCIA Card

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1.3 1553 Bus Connections

The EXC-1553PCMCIA contains a 25-pin MIL-STD-1553 I/O bus connector. Each board is shipped with an adapter cable that converts the rear connector to a standard 1553 [miniature] female twinax type. The adapter cable comes wired and ready to connect to the 1553 channel (buses A and B). The 1553 connectors will mate, for example, with the Trompeter 'PL75' male twinax connector which is not supplied, but can be ordered from Excalibur Systems, Inc. (PN# PL75-29)

For short distances, direct coupling may be used to connect the EXC-1553PCMCIA directly to another 1553 device. Optional adapter cables for direct coupling may be ordered. You must make certain that the cable connecting the two devices is properly terminated with 78 Ohm resistors to insure data integrity (see Figure 1-2).

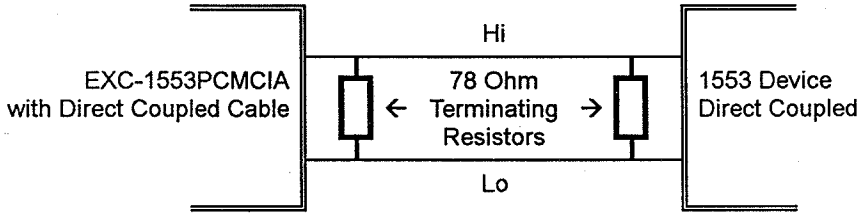


Figure 1-2. Direct Coupled Connection (One Bus Shown)

If you wish to operate in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems, Inc. We supply a three-stub coupler (PN# DB30010) and 78-ohm terminators (PN# RT500078). Two terminators are required for each coupler, which services a single bus, i.e. BUS A (see Figure 1-3).

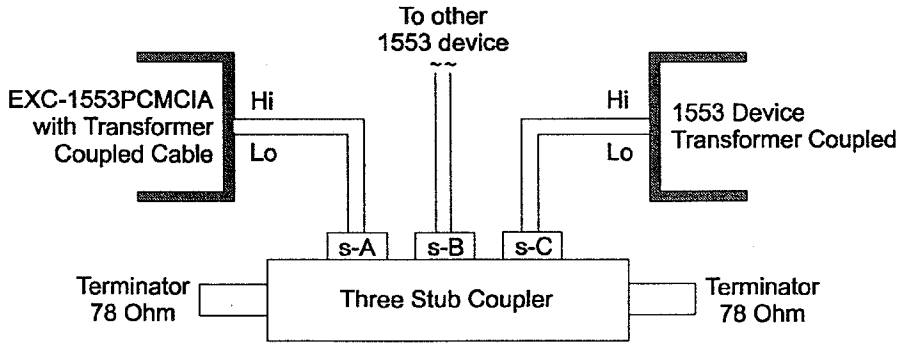


Figure 1-3. Transformer Coupled Connection (One Bus Shown)

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2 PCMCIA Bus Interface

Chapter 2 describes the PCMCIA bus interface. The following topics are covered:

- "Attribute Memory Map," page 2-2
- "Card Information Structure," page 2-3
- "Function Configuration Registers," page 2-8
- "Common Memory Map," page 2-9

The PCMCIA standard defines the electrical and physical interface between the PC Card and the host computer, including the 68-pin connector. Detailed specifications can be found in the PCMCIA PC Card Standard, Release 2.1, July 1993.

PCMCIA Standard Release 1.0 defined PC Memory cards. PCMCIA Standard Release 2.0 added a definition for I/O cards. Several signals are added or changed to support an I/O card. Upon powerup or after reset, the EXC-1553PCMCIA appears to the host as a Release 1.0 Memory Card, and afterwards the card is configured by the software to be an I/O card.

The EXC-1553PCMCIA supports two types of address spaces:

- Common Memory Address space, for regular memory accesses. The dual-port RAMs and the control registers are located in Common Memory.
- Attribute Memory Address space, for the Card Information Structure (CIS) and the Function Configuration Registers.

The Attribute Memory space is selected by driving the signal REG# low, and the Common Memory space is selected by driving the signal REG# high (see Tables 2-1 and 2-2 for details regarding memory access).

FUNCTION	REG#	CE2#	CE1#	A0	OE#	WE#	D15-D8	D7-D0
Standby	X	H	H	X	X	X	Hi-Z	Hi-Z
Lo Byte Read	H	H	L	L	L	H	Hi-Z	Even-Byte
Lo Byte Write	H	H	L	L	H	L	Hi-Z	Even-Byte
Hi Byte Read	H	L	H	X	L	H	Odd-Byte	Hi-Z
Hi Byte Write	H	L	H	X	H	L	Odd-Byte	Hi-Z
Word Read	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write	H	L	L	X	H	L	Odd-Byte	Even-Byte

Table 2-1. Common Memory Access for EXC-1553PCMCIA

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FUNCTION	REG#	CE2#	CE1#	A0	OE#	WE#	D15-D8	D7-D0
Standby	X	H	H	X	X	X	Hi-Z	Hi-Z
Lo Byte Read	L	H	L	L	L	H	Hi-Z	Even-Byte
Lo Byte Write	L	H	L	L	H	L	Hi-Z	Even-Byte
Hi Byte Read	L	L	H	X	L	H	Invalid	Hi-Z
Hi Byte Write	L	L	H	X	H	L	Invalid	Hi-Z
Word Read	L	L	L	X	L	H	Invalid	Even-Byte
Word Write	L	L	L	X	H	L	Invalid	Even-Byte

Table 2-2. Attribute Memory Access for EXC-1553PCMCIA

NOTE The EXC-429PCMCIA does not support odd byte accesses to data lines D7-D0.

Information concerning the format of the card is stored in the Card Information Structure (CIS). The CIS is a variable-length linked-list of data blocks, called tuples. The CIS resides in even bytes of the Attribute Memory, beginning at address 0. Two function configuration registers are also located in the Attribute Memory. These allow you to reset the EXC-1553PCMCIA card or to service interrupts.

2.1 Attribute Memory Map

The Attribute Memory is selected during an even byte or word access when the host drives the signal/REG low. The Attribute Memory contains the CIS and two Function Configuration Registers. The CIS is read-only. The CIS resides in the even bytes starting at address 0 and ending when the End_of_List tuple is encountered. The two Function Configuration Registers are located at addresses 40000 (H) and 40002 (H). The regions between the CIS and the Function Configuration Registers and above the Function Configuration Registers are reserved and shouldn't be accessed.

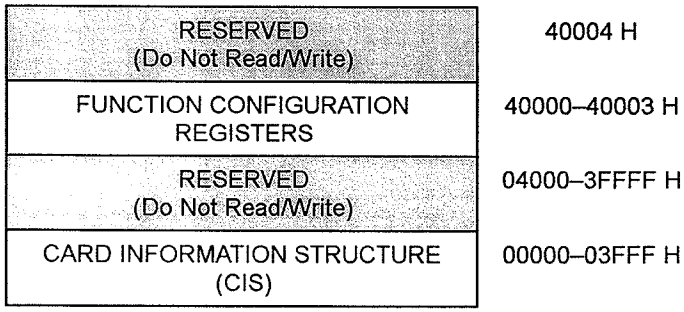


Figure 2-1. Attribute Memory Map

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2.2 Card Information Structure (CIS)

The Card Information Structure (CIS) contains information about the type of PC card (memory or I/O), the types and sizes of memory, and the interface to the host. Information is stored in a variable-length linked-list of data blocks, called **tuples**. The first byte of each tuple contains the tuple code, which defines what type of information the tuple provides. The next byte is the link byte, which indicates how many bytes remain in the current tuple.

2.2.1 Device Tuple For Common Memory

The first tuple identifies the card as a 5V PCMCIA card.

2.2.2 Level 1 Version/Product Information Tuple

This tuple contains Level-1-version compliance information as defined in PCMCIA Release 2.0, and information about the card manufacturer. Included are the major version number and the minor version number, [04 (H) and 01 (H) respectively, according to PCMCIA Release 2.0]. Also included are the manufacturer name and the product name.

2.2.3 Manufacturer Identification Tuple

This tuple contains Excalibur System's Manufacturer Code, which is 0145 (H). Also included is the current revision of the CIS table. The revisions of the CIS is read as hex numbers. For example, revision 1.0 would be read as 10 (H).

2.2.4 Configuration Tuple

This tuple establishes the number and address of the Function Configuration Registers, and indicates the index of the last Configuration Entry Tuple. The EXC-1553PCMCIA has two Configuration Registers at base address 40000 (H). The index of the last Configuration Entry Tuple is 2.

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2.2.5 Configuration Entry Tuple

This tuple describes the type of interface utilized by the EXC-1553PCMCIA, and establishes various configurable options. The CIS may contain several Configuration Entry tuples with different configurable options. Each of the Configuration Entry tuples contains a different Configuration Table Index. You can configure the PC Card according to either of the Configuration Entry tuples by writing the appropriate Configuration Table Index to bits 05-00 of the Configuration Option Register. This lets you set various options without using jumpers.

One Configuration Entry tuple is allowed for the EXC-1553PCMCIA. The entry, whose index is 2, configures the card to be a Memory card with no level interrupt request.

Under Windows95/NT, the Excalibur software drivers override this tuple. The card retrieves the required information from the following sources, according to the operating system you are using:

- Windows95 - from the **excpcmcia.inf** file in the tuple override section, included on the **Excalibur PCMCIA Hardware Installation** diskette.
- WindowsNT - automatically when you save your settings in **ExcConfigNT**.

For more information about the accompanying drivers, see the *Excalibur EP Family Galahad Software Tools User's Manual.*

2.2.6 No Link Tuple

This tuple indicates that the CIS doesn't continue in another linked list after the End of List tuple.

2.2.7 End Of List Tuple

This tuple indicates the end of the linked list.

2.2.8 CIS Table

Tuple Address	Tuple Value	Tuple Field Name	General Description
00 H	01 H	TPL_CODE	CISTPL_DEVICE
02 H	01 H	TPL_LNK	
04 H	FF H	End of Tuple	

The CIS Table continues on the next page.

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Tuple Address	Tuple Value	Tuple Field Name	General Description
06 H	15 H	TPL_CODE	CISTPL_VERS_1
08 H	2B H	TPL_LNK	
0A H	04 H	TPLLV1_MAJOR	Major version number (04 H)
0C H	01 H	TPLLV1_MINOR	Minor version number (01 H)
0E H	45 H	"E"	Name Of Manufacturer
10 H	78 H	"x"	
12 H	63 H	"c"	
14 H	61 H	"a"	
16 H	6C H	"l"	
18 H	69 H	"i"	
1A H	62 H	"b"	
1C H	75 H	"u"	
1E H	72 H	"r"	
20 H	20 H	"space"	
22 H	53 H	"S"	
24 H	79 H	"Y"	
26 H	73 H	"s"	
28 H	74 H	"t"	
2A H	65 H	"e"	
2C H	6D H	"m"	
2E H	73 H	"s"	
30 H	20 H	space	
32 H	49 H	"I"	
34 H	6E H	"n"	
36 H	63 H	"c"	
38 H	2E H	"."	
3A H	00 H	"terminator"	

The CIS Table continues on the next page.

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Tuple Address	Tuple Value	Tuple Field Name	General Description
3C H	45 H	"E"	Name of Product
3E H	58 H	"X"	
40 H	43 H	"C"	
42 H	2D H	"-"	
44 H	31 H	"1"	
46 H	35 H	"5"	
48 H	35 H	"5"	
4A H	33 H	"3"	
4C H	50 H	"P"	
4E H	43 H	"C"	
50 H	4D H	"M"	
52 H	43 H	"C"	
54 H	49 H	"I"	
56 H	41 H	"A"	
58 H	2F H	"/"	
5A H	42 H	"B"	
5C H	00 H	"terminator"	
5E H	FF H	end of tuple	
60 H	20 H	TPL_CODE	CISTPL_MANFID
62 H	04 H	TPL_LNK	
64 H	45 H	TPLMID_MANF	Manufacturer code for Excalibur Systems Lo
66 H	01 H	TPLMID_MANF	Manufacturer code for Excalibur Systems Hi
68 H	00 H	Reserved	
6A H	***	CIS Revision	*** Revision of CIS (Rev. 1.0 is read as 10 H)

The CIS Table continues on the next page.

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Tuple Address	Tuple Value	Tuple Field Name	General Description
6C H	1A H	TPL_CODE	CISTPL_CONFIG
6E H	06 H	TPL_LNK	
70 H	02 H	TPCC_SZ	3 address bytes for Configuration Registers
72 H	02 H	TPCC_LAST	Index number of last entry is 2
74 H	00 H	TPCC_RADR	Configuration Registers Base Address Lo
76 H	00 H	TPCC_RADR	Configuration Registers Base Address Mid
78 H	04 H	TPCC_RADR	Configuration Registers Base Address Hi
7A H	03 H	TPCC_RMSK	First two Configuration Registers
7C H	1B H	TPL_CODE	CISTPL_CFTABLE_ENTRY
7E H	0E H	TPL_LNK	
80 H	C2 H	TPCE_INDX	Interface follows, Set Default, Index is 2
82 H	80 H	TPCE_IF	WAIT, No Rdy/Bsy,WP,BVD,Memory Type Interface
84 H	62 H	TPCE_FS	Memory description follows,No IRQ,VCC and VPP power description
86 H	01 H	TPCE_PD	VCC: Nominal voltage
88 H	55 H	TPCE_PD	VCC: 5V
8A H	01 H	TPCE_PD	VPP: Nominal voltage
8C H	0E H	TPCE_PD	VPP: 12V
8E H	49 H	TPCE_MS	2 bytes address size, 1 byte length, 2 window description
90 H	80 H	TPCE_MS	Window 1 length size = 32K
92 H	00 H	TPCE_MS	Window 1 address = 000000 H
94 H	00 H	TPCE_MS	
96 H	01 H	TPCE_MS	Window 2 length size = 1/4K
98 H	00 H	TPCE_MS	Window 2 address = 040000 H
9A H	04 H	TPCE_MS	
9C H	14 H	TPL_CODE	CISTPL_NO_LINK
9E H	00 H	TPL_LNK	
A0 H	FF H	TPL_CODE	CISTPL_END

The CIS Table is continued from the previous page.

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2.3 Function Configuration Registers

The two function configuration registers are located in the Attribute Memory, at addresses 40000 (H) and 40002 (H). These allow you to reset the EXC-1553PCMCIA card or to service interrupts.

2.3.1 Configuration Option Register

Address: 40000 (H) READ/WRITE

Bit	Bit Name	Description
07	**Reset**	1 = Resets the EXC-1553PCMCIA. This bit remains high, and the card remains in reset mode, until a 0 is written to this bit. The default value of the reset bit is 0.
06	**Reserved**	Set to 1 on write. Ignore on read.
02-05	**Reserved**	Set to 0 on write. Ignore on read.
01	**RT Lock**	1 = Locks the board into RT mode. 0 = Allows you to select a mode via software.
00	**Reserved**	Set to 0 on write. Ignore on read.

2.3.2 Configuration & Status Register

Address: 40002 (H) READ/WRITE

Bit	Bit Name	Description
02-07	**Reserved**	Set to 0 on write. Ignore on read.
01	**Interrupt Pending**	1 = The EXC-1553PCMCIA has an interrupt waiting to be serviced. This bit remains high, and the card remains in interrupt pending mode, until a 0 is written to this bit. Writing a 1 to this bit has no effect on the value of the bit. The default value of the interrupt pending bit is 0.
00	**Reserved**	Set to 0 on write. Ignore on read.

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2.4 Common Memory Map

The PCMCIA standard defines two types of address spaces:

- Common Memory Address space, for regular memory accesses. The dual-port RAMs and the control registers are located in Common Memory.
- Attribute Memory Address space, for the Card Information Structure (CIS) and the Function Configuration Registers.

(See PCMCIA Standards, PC Card Standard 2.1 for more details on Attribute Memory).

The Common Memory contains 128Kb of dual-port RAM and 32 words of control registers. The RAM may be accessed in either byte or word mode, while the control registers must be accessed in word mode. The regions between the RAM and the control registers and above the control registers are reserved and should not be accessed.

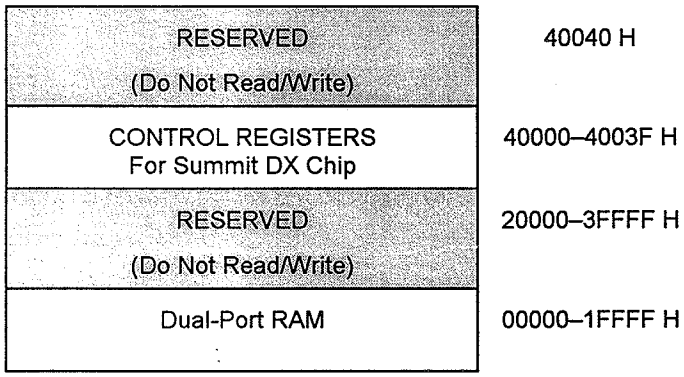


Figure 2-2. Common Memory Map

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3 Bus Controller Operation

Chapter 3 describes EXC-1553PCMCIA operation in Bus Controller (BC) mode. The following topics are covered:

- "Bus Controller Message Processing," page 3-1
- "Control Registers—BC Mode," page 3-2
- "Bus Controller Architecture," page 3-10
- "Command Block Chaining," page 3-16
- "Memory Architecture," page 3-17
- "MIL-STD-1553A Operation—BC Mode," page 3-18

3.1 Bus Controller Message Processing

To process 1553 messages, the EXC-1553PCMCIA uses data supplied in the control registers along with data stored in memory. The EXC-1553PCMCIA accesses eight 16-bit words stored in memory called a **command block**. The command block is accessed at the beginning and end of command processing. You can allocate memory spaces for the minor frame. The top of the command blocks can reside at any address location. You can define and enter the control registers into memory. The control registers are linked to the Command Block via the Command Block Pointer Register contents. Each command block contains a Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, Branch Address, and Timer Value. For a complete description of each location, see "Bus Controller Architecture," page 3-10.

NOTE In BC mode, the EXC-1553PCMCIA does not need to re-read the Command Block on a retry situation.

Control word information allows the EXC-1553PCMCIA to control the commands transmitted over the 1553 bus. The Control word allows the EXC-1553PCMCIA to transmit commands on a specific channel, perform retries, initiate RT-RT transfers, and interrupt on certain conditions. The host defines each command word associated with each command block. For normal 1553 commands, only the first command word location will contain valid data. For RT-RT commands, as specified in the Control word, the host must define the first command word as a receive and the second command word as a transmit.

For a receive command the Data Pointer is read to determine where data words are retrieved. The EXC-1553PCMCIA retrieves data words sequentially from the address specified by the Data Pointer. For a transmit command the Data Pointer is read to determine the top

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memory location. The EXC-1553PCMCIA stores data words sequentially from this top memory location.

The EXC-1553PCMCIA reads the command block during minor frame processing. The EXC-1553PCMCIA then begins the acquisition of data words for either transmission or storage.

After transmission or reception, the EXC-1553PCMCIA begins post-processing, and the command block is updated. The EXC-1553PCMCIA modifies the Control word as required. An optional interrupt log entry is performed after the command block update.

3.2 Control Registers—BC Mode

The control registers are read/write unless otherwise stated. All control registers must be accessed in word mode. All control register bits are active high and are reset to 0 unless otherwise stated.

Figure 3-1 below illustrates the control registers for Bus Controller mode.

Reserved	40012-4003F H
Command Block Pointer Register	40010 H
Minor Frame Register	4000E H
BIT Word Register	4000C H
Interrupt Log List Pointer Register	4000A H
Pending Interrupt Register	40008 H
Interrupt Mask Register	40006 H
Current Command Block Register	40004 H
Operational Status Register	40002 H
Setup Register	40000 H

Figure 3-1. Control Registers—BC Mode

3.2.1 Setup Register — Address: 40000 (H)

The Setup Register's function is to configure the EXC-1553PCMCIA for operation. To make changes to the BC and this register, the STEX bit (Bit 15) must be logic zero. To operate the EXC-1553PCMCIA as a bus controller, use the bits described below.

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Bit	Bit Name	Description
15	STEX	Start Execution. 1 = Starts operation of the EXC-1553PCMCIA. 0 = Inhibits operation of the EXC-1553PCMCIA. After execution begins, a write of logic zero will halt the EXC-1553PCMCIA after completing the current 1553 message.
14	SBIT	Start BIT. 1 = Places the card into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. The host must halt the card in order to place it into the Built-In Test mode (STEX = 0). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13	SRST	Software Reset. 1 = Performs a software reset. The configuration registers are not affected when this bit is asserted. The software reset takes 6 usec. to execute.
05-12	Reserved	Set to 0
04	BCEN	Broadcast Enable. 1 = Enables the broadcast option for BC Mode. 0 = Enables the remote terminal address 31 as a unique RT address. When enabled, the EXC-1553PCMCIA does not expect a status word response from the remote terminal.
03	Reserved	Set to 0
02	PPEN	Ping-Pong Enable. This bit controls the method by which the EXC-1553PCMCIA will retry messages. 1 = Allows the EXC-1553PCMCIA to ping-pong between buses during retries. 0 = Dictates that all retries will be performed on the programmed bus as defined in the Retry Number field of the Command Block control word.
01	INTEN	Interrupt Log List Enable. 1 = Enables the Interrupt Log List. 0 = Prevents the logging of interrupts as they occur.
00	Reserved	Set to 0

Setup Register

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3.2.2 Operational Status Register — Address: 40002 (H)

The Operational Status register provides pertinent status information for BC Mode and is reset to ED82 (H).

To make changes to the BC and to this register, the STEX bit (Setup Register, bit 15) must be logic zero.

Bit	Bit Name	Description
10-15	Reserved	Set to 0
09	MSEL1	Mode Select 1. In conjunction with Mode Select 0, this bit determines the mode of operation of the EXC-1553PCMCIA.
08	MSEL0	Mode Select 0. In conjunction with Mode Select 1, this bit determines the mode of operation of the EXC-1553PCMCIA.

MSEL1	MSEL0	Mode of Operation
0	0	BC Mode
0	1	RT Mode
1	0	Monitor Mode
1	1	RT/ Concurrent Monitor Mode

07	A/B STD	Military Standard 1553A or 1553B. This bit determines whether the EXC-1553PCMCIA will operate under MIL-STD-1553A or 1553B protocol. 1 = Forces the EXC-1553PCMCIA to look for all responses in 11 usec. or generate time-out errors. 0 = Automatically allows the EXC-1553PCMCIA to operate under the MIL-STD-1553B protocol. See "MIL-STD-1553A Operation—BC Mode," page 3-18, for further information.
04-06	Reserved	These read-only bits are 0.
03	EX	EXC-1553PCMCIA Executing. This read-only bit indicates whether the card is presently executing or is idle. 1 = The EXC-1553PCMCIA is executing. 0 = The EXC-1553PCMCIA is idle.
02	Reserved	Ignore this read-only bit.
01	READY	Ready. This read-only bit indicates that the EXC-1553PCMCIA has completed initialization or that it has completed the BIT. This bit is cleared on reset.
00	TERACT	Teract. Read-only. 1 = The EXC-1553PCMCIA is presently processing a message. Note: When STEX transitions from 1 to 0, EX and TERACT stay active until command processing is complete.

Operational Status Register

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3.2.3 Current Command Register — Address: 40004 (H) READ ONLY

The Current Command register contains the last 1553 command that was transmitted by the EXC-1553PCMCIA. Upon the execution of each Command Block, this register will automatically be updated. The register is updated when transmission of the Command Word begins. In an RT-RT transfer, this register will reflect the latest Command Word as it is transmitted.

Bit	Bit Name	Description
00-15	CC[15-0]	Current Command. These bits contain the latest 1553 command that was transmitted by the bus controller.

Current Command Register

3.2.4 Interrupt Mask Register — Address: 40006 (H)

The EXC-1553PCMCIA interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked if the corresponding bit of the Interrupt Mask register is set to a logic zero.

Bit	Bit Name	Description
15	DMAF	DMA Fail Interrupt
14	WRAPF	Wrap Fail Interrupt
13	Reserved	Set to 0
12	BITF	BIT Fail Interrupt
11	MERR	Message Error Interrupt
06-10	Reserved	Set to 0
05	EOL	End Of List Interrupt
04	ILLCMD	Illogical Command Interrupt
03	ILLOP	Illogical Opcode Interrupt
02	RTF	Retry Fail Interrupt
01	CBA	Command Block Accessed Interrupt
00	Reserved	Set to 0

Interrupt Mask Register

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3.2.5 Pending Interrupt Register — Address: 40008 (H) READ ONLY

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. A 125 nsec. interrupt is generated when any bit in this register is set by the card.

NOTE All register bits are cleared on a host read.

Bit	Bit Name	Description
15	DMAF	DMA Fail Interrupt. Indicates that a memory access failed.
14	WRAPF	Wrap Fail Interrupt. The EXC-1553PCMCIA automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set and an interrupt is generated. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	Reserved	Ignore on read.
12	BITF	BIT Fail Interrupt. 1 = A BIT failure. Interrogate Bit Word Register bits 11 and 10 to determine the specific channel that failed. In BC mode, an interrupt is generated and command processing stops if initiated by opcode.
11	MERR	Message Error Interrupt. 1 = A message error occurred. The EXC-1553PCMCIA can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.
06-10	Reserved	Ignore on read.
05	EOL	End Of List Interrupt. 1 = The EXC-1553PCMCIA is at the end of the command block. An interrupt is generated.
04	ILLCMD	Illogical Command Interrupt. 1 = An illogical command (i.e., Transmit Broadcast or improperly formatted RT-RT message) was written into the Command Block. The EXC-1553PCMCIA checks for RT-RT Terminal address field match, RT-RT transmit/receive bit mismatch and correct order, and broadcast transmit commands. If illogical commands occur, the EXC-1553PCMCIA will halt execution. An interrupt is generated.

Pending Interrupt Register (continues on next page)

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Bit	Bit Name	Description
03	ILLOP	Illogical Opcode Interrupt. 1 = An illogical opcode (i.e., any reserved opcode) was used in the command block. The EXC-1553PCMCIA halts operation if this condition occurs. An interrupt is generated.
02	RTF	Retry Fail Interrupt. 1 = All programmed retries failed. An interrupt is generated.
01	CBA	Command Block Accessed Interrupt. 1 = A command block was accessed (Opcode 1010), if enabled. An interrupt is generated.
00	Reserved	Ignore on read.

Pending Interrupt Register (continued from previous page)

3.2.6 Interrupt Log List Pointer Register

Address: 4000A (H)

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts. The EXC-1553PCMCIA architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List in a 64K word memory space. Initialize the lower five-bits of this register to a logic zero. The EXC-1553PCMCIA controls the lower five-bits to implement the ring-buffer architecture. This register is read to determine the location and number of interrupts in the Interrupt Log List (least significant five-bits).

Bit	Bit Name	Description
00-15	INT[15-0]	Interrupt Log List Pointer Bits. These bits indicate the starting location of the Interrupt Log List.

Interrupt Log List Pointer Register

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3.2.7 BIT Word Register — Address: 4000C (H)

The BIT Word register contains information on the current status of the EXC-1553PCMCIA.

Bit	Bit Name	Description
15	DMAF	DMA Fail. 1 = A memory access failed.
14	WRAPF	Wrap Fail. The EXC-1553PCMCIA automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	Reserved	Ignore on read.
12	BITF	BIT Fail. 1 = A BIT failure. Interrogate bit 11 and 10 to determine the specific channel that failed.
11	CHAF	Channel A Fail. 1 = A BIT test failure in Channel A.
10	CHBF	Channel B Fail. 1 = A BIT test failure in Channel B.
00-09	Reserved	Ignore on read.

BIT Word Register

3.2.8 Minor Frame Timer Register — Address: 4000E (H) READ ONLY

The Minor Frame Timer register is loaded via the Minor Frame Timer (MFT) opcode (Opcode 1110).

Bit	Bit Name	Description
00-15	MFT[15-0]	Minor Frame Timer. These bits indicate the value of the timer.

Minor Frame Timer Register

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3.2.9 Command Block Pointer Register — Address: 40010 (H)

The Command Block Pointer register contains the location to start the Command Blocks. After execution begins, this register is automatically updated with the address of the next block.

Bit	Bit Name	Description
00-15	CBA[15-0]	Command Block Address. These bits indicate the starting location of the Command Block.

Command Block Pointer Register

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3.3 Bus Controller Architecture

As defined in MIL-STD-1553, the bus controller initiates all communications on the bus. To comply with MIL-STD-1553 bus controller requirements, the EXC-1553PCMCIA uses a Command Block architecture that takes advantage of both control registers and SRAM. Each command word transmitted over the bus must be associated with a Command Block. The Command Block requires eight contiguous 16-bit memory locations for each message.

These eight locations include:

- A control word
- Two command word locations
- A data pointer
- Two status word locations
- A branch address location
- A timer value

The host must initialize each of the locations associated with each Command Block. The exception is for the two status locations which will be updated as command words are transmitted and corresponding status words are received.

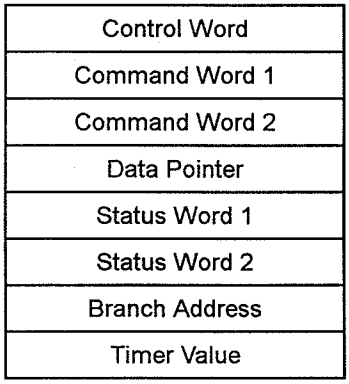


Figure 3-2. BC Mode Command Block

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3.3.1 Control Word

The first memory location of each BC Mode Command Block contains the control word. Each control word contains the opcode, retry number, bus definition, RT-RT instruction, condition codes, and the block access message error. The control word is defined below:

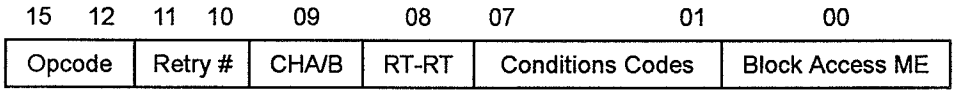


Figure 3-3. Control Word Definition

Bit	Bit Name	Description
12-15	Opcode	These bits define the opcode to be used by the EXC-1553PCMCIA for that particular Command Block. If the opcode does not perform any 1553 function, all other bits are ignored. Each of the available opcodes is defined in "Opcode Definition," page 3-12.
10-11	Retry Number	These bits define the number of retries for each individual Command Block and if retry opcode is used. If the Ping-Pong Enable Bit (bit 02 of the Setup Register) is not enabled, all retries will occur on the programmed bus. However, if bit 02 is enabled, the first retry will always occur on the alternate bus, the second retry will occur on the primary bus, the third retry will occur on the alternate bus, and the fourth retry will occur on the primary bus.
09	Bus A/B	This bit defines on which of the two buses the command will be transmitted (i.e., primary bus). (Logic 1 = Bus A, Logic 0 = Bus B).
08	RT-RT Transfer	This bit defines whether or not the present Command Block is an RT-RT transfer and if the EXC-1553PCMCIA should transmit the second command word. Data associated with an RT-RT is always stored by the EXC-1553PCMCIA.
01-07	Condition Codes	These bits define the condition code the EXC-1553PCMCIA uses for that particular Command Block. Each of the available condition codes are defined in "Condition Codes," page 3-14.
00	Block Access Message Error	The card sets this bit to 1, indicating a protocol message error occurred in the RT's response. For this occurrence, the EXC-1553PCMCIA will overwrite this bit prior to storing the Control Word into memory. An example of this type of error would be noise on the 1553 bus.

BIT 11	BIT 10	No. of Retries
0	1	1
1	0	2
1	1	3
0	0	4

Control Word Description

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3.3.2 Opcode Definition

Opcode	Field Name	Definition
0000	End Of List	This opcode instructs the EXC-1553PCMCIA that the end of the command block has been encountered. Command processing stops and the interrupt is generated if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0001	Skip	This opcode instructs the EXC-1553PCMCIA to load the message-to-message timer with the value stored in timer value location. The EXC-1553PCMCIA will then wait the specific time before proceeding to the next command block. This opcode allows for scheduling of specific time between message execution. No command processing takes place (i.e., no 1553).
0010	Go To	This opcode instructs the EXC-1553PCMCIA to "go to" the command block as specified in the branch address location. No command process takes place (i.e., no 1553).
0011	Built-in Test	This opcode instructs the SUMMIT chip to perform an internal built-in test. If the device passes the built-in test, then processing of the next command block will continue. However, if the device fails the built-in test, then processing stops and an interrupt is generated, if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0100	Execute Block; Continue	This opcode instructs the EXC-1553PCMCIA to execute the current command block and proceed to the next command block. This opcode allows for continuous operations.
0101	Execute Block; Branch	This opcode instructs the EXC-1553PCMCIA to execute the current command block and unconditionally branch to the location as specified in the branch address location.
0110	Execute Block; Branch on Condition	This opcode instructs the EXC-1553PCMCIA to execute the current command block and branch only if the condition is met. If no conditions are met, the opcode appears as an execute and continue.
0111	Retry on Condition	This opcode instructs the EXC-1553PCMCIA to perform automatic retries, as specified in the control word, if particular conditions occur. If no conditions are met, the opcode appears as an execute and continue.
1000	Retry on Condition; Branch	This opcode instructs the EXC-1553PCMCIA to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met, the EXC-1553PCMCIA retries. Once all retries have executed, the EXC-1553PCMCIA branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and branch.

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Opcode	Field Name	Definition
1001	**Retry on Condition; Branch if all Retries Fail**	This opcode instructs the EXC-1553PCMCIA to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met and all the retries fail, the EXC-1553PCMCIA branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and continue.
1010	**Interrupt; Continue**	This opcode instructs the EXC-1553PCMCIA to interrupt and continue processing on the next command block. When using this opcode, no 1553 processing occurs.
1011	**Call**	This opcode instructs the EXC-1553PCMCIA to "go to" the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the EXC-1553PCMCIA may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1100	**Return to Call**	This opcode instructs the EXC-1553PCMCIA to return to the command block address saved during the Call opcode. No command processing takes place (i.e., no 1553).
1101	**Reserved**	The EXC-1553PCMCIA will generate an illegal opcode interrupt (if interrupt enabled) and automatically stop execution if a reserved opcode is used.
1110	**Load Minor Frame Timer**	This opcode instructs the EXC-1553PCMCIA to load the minor frame timer (MFT) with the value stored in the eighth location of the current command block. The timer will be loaded after the previous MFT has decremented to zero. After the MFT timer is loaded with the new value, the EXC-1553PCMCIA will proceed to the next command block. No command processing takes place (i.e., no 1553).
1111	**Return to Branch**	This opcode instructs the EXC-1553PCMCIA to return to the command block address saved during a Branch opcode. No command processing takes place (i.e., no 1553).

Opcode Definition

NOTE For retries with interrupts enabled, all interrupts are logged after message processing is complete.

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3.3.3 Condition Codes

Condition codes have been provided as a means for the EXC-1553PCMCIA to perform certain functions based on the RT's status word. In an RT-RT transfer, the conditions apply to both of the status words. Each bit of the condition codes is defined below.

Bit Number	Description
07	Message Error. This condition will be met if the EXC-1553PCMCIA detects an error in the RT's response, or if it detects no response. (The EXC-1553PCMCIA will wait 15 usec. in 1553B mode and 11 usec. in 1553A mode before declaring an RT no response).
06	Status Word Response with the Message Error bit set (Bit time 09 in 1553A mode). This condition is met if the EXC-1553PCMCIA detects that the RT's status word has the Message Error bit set.
05	Status Word Response with the Busy bit set (Bit time 16 in 1553A mode). This condition is met if the EXC-1553PCMCIA detects that the RT's status word has the Busy bit set.
04	Status Word Response with the Terminal Flag bit set (Bit time 19 in 1553A mode). This condition is met if the EXC-1553PCMCIA detects that the RT's status word has the Terminal Flag bit set.
03	Status Word Response with the Subsystem Fail bit set (Bit time 17 in 1553A mode). This condition is met if the EXC-1553PCMCIA detects that the RT's status word has the Subsystem Fail bit set.
02	Status Word Response with the Instrumentation bit set (Bit time 10 in 1553A mode). This condition is met if the EXC-1553PCMCIA detects that the RT's status word has the Instrumentation bit set.
01	Status Word Response with the Service Request bit set (Bit time 11 in 1553A mode). This condition is met if the EXC-1553PCMCIA detects that the RT's status word has the Service Request bit set.

Condition Codes

3.3.4 Command Words

The next two locations of the BC Mode Command Block are for 1553 command words. In most 1553 messages, only the first command word needs to be initialized. However, in an RT-RT transfer, the first command word is the Receive Command and the second command word is the Transmit Command.

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3.3.5 Data Pointer

The fourth location of the BC Mode Command Block is the data pointer that points to the first memory location to store or retrieve the data words associated with the message for that command block. This data structure allows the EXC-1553PCMCIA to store or retrieve the exact specified number of data words, thus saving memory space and providing efficient space allocation.

NOTE In an RT-RT transfer, the EXC-1553PCMCIA uses the data pointer as the location in memory to store the transmitted data in the transfer.

One common application for data pointer occurs when the EXC-1553PCMCIA needs to send the same data words to several RTs. Here, each Command Block associated with those messages would contain the same data pointer value, and, therefore, retrieve and transmit the same data. Note that the Data Pointer is never updated (i.e., the EXC-1553PCMCIA reads and writes the pointer but never changes its value).

3.3.6 Status Words

The next two locations in the BC Mode Command Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. In an RT-RT transfer, the first status word will be the status of the Transmitting RT while the second status word will be the status of the Receiving RT.

3.3.7 Branch Address

The seventh location in the BC Mode Command Block contains the starting location of the branch. This location simply allows the EXC-1553PCMCIA to branch to another location in memory when certain opcodes are used.

3.3.8 Timer Value

The last location in the BC Mode Command Block is the Timer Value. This timer is used for one of two purposes. First, the value may be used to set up minor frame schedules when using the Load Minor Frame Timer opcode (1110). The MFT counter is clocked by a 64 usec. internal clock. The MFT counter runs continuously during message processing and must decrement to zero prior to loading the next Minor Frame time value. Second, the value may be used as a message-to-message timer (MMT) when using the Skip opcode (0001). The MMT timer is clocked at a 24 MHz rate and allows for scheduling of specific time between message execution.

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3.4 Command Block Chaining

To determine the first Command Block, set the initial start address in the Command Block Pointer Register [Address 40010 (H)]. The Command Blocks will execute in a contiguous fashion as long as no "go to", "branch", "call", or "return" opcodes are used. With the use of these opcodes, almost any memory configuration is possible. Figures 3-4 and 3-5 show how several Command Blocks may be linked together to form a command frame and how branch opcodes may be used to link minor frames. The minimum BC intermessage gap is 28.0 usec.

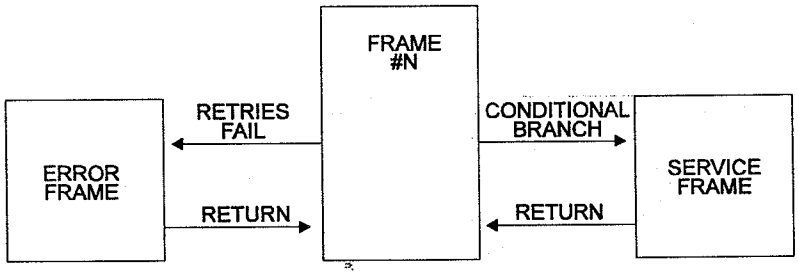


Figure 3-4. Message Control Options

The example in Figure 3-5 shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 msec. long, Message A is sent every 10 msec., Message B is sent every 20 msec., and Message C is sent every 40 msec.

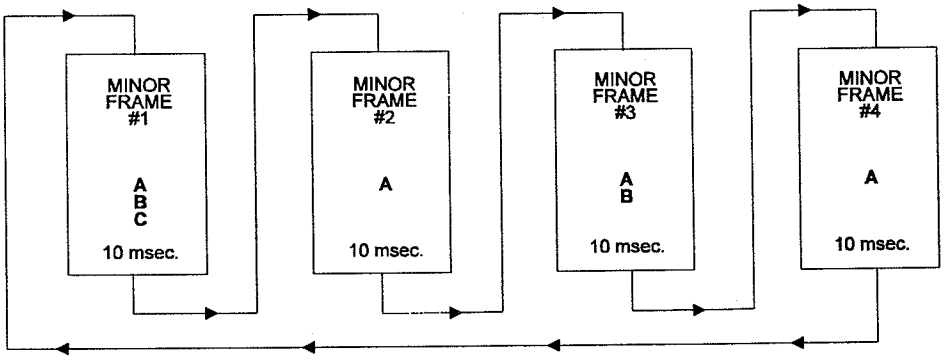


Figure 3-5. Minor Frame Sequencing

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3.5 Memory Architecture

After reviewing the control registers, it may be advantageous to look at how you can set up memory to configure the EXC-1553PCMCIA as a bus controller. This section shows one method for defining the memory configuration.

The configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities. Figure 3-6 shows that the first block of memory is allocated for the Command Blocks. Notice that the Command Block Pointer Register initially points to the control word of the first Command Block. After completing execution for that first Command Block, the Command Block Pointer Register will automatically be updated to show the address of the next Command Block.

Following the Command Block locations is the memory required for all the data words. In BC applications, the number of data words for each Command Block is known. In Figure 3-6, for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. Since the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List (see "Interrupt Log List Pointer Register," page 3-7). Notice that the Interrupt Log List Pointer Register points to the top of the initial Log List. After execution of that first BC Command Block, the Interrupt Log List Pointer Register will automatically be updated.

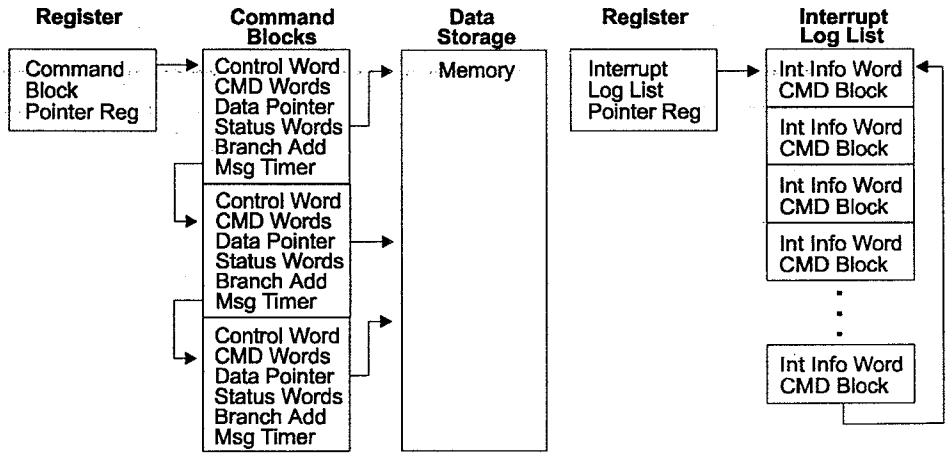


Figure 3-6. Memory Architecture for BC Mode

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3.6 MIL-STD-1553A Operation—BC Mode

The EXC-1553PCMCIA may be configured to meet the MIL-STD-1553A protocol. When configured as a MIL-STD-1553A bus controller, the EXC-1553PCMCIA will operate as follows:

- Looks for the RT response within 11 usec.
- Defines all mode codes without data
- Defines subaddress 00000 as a mode code

A/B STD	RESULT
0	1553B response, 1553B standard
1	1553A response, 1553A standard

Table 3-1. MIL-STD-1553A Operation—BC Mode

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4 Remote Terminal Operation

Chapter 4 describes EXC-1553PCMCIA operation in Remote Terminal (RT) mode. The following topics are covered:

- "RT Message Processing," page 4-1
- "Control Registers—RT Mode," page 4-2
- "Descriptor Block," page 4-14
- "Data Structures," page 4-23
- "Mode Code and Subaddress," page 4-29
- "Encoder and Decoder," page 4-31
- "RT-RT Transfer Compare," page 4-32
- "Terminal Address," page 4-32
- "Reset," page 4-33
- "MIL-STD-1553A Operation—RT Mode," page 4-33

The EXC-1553PCMCIA can be configured as both a remote terminal and monitor. For more information about this feature, see "RT/Concurrent Monitor Operation" on page 5-13.

4.1 RT Message Processing

To process messages, the EXC-1553PCMCIA uses data from the control registers with data stored in the static RAM. The EXC-1553PCMCIA accesses a four 16-bit word descriptor block stored in RAM. The descriptor block is accessed at the beginning and end of command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table.

The EXC-1553PCMCIA allocates 512 consecutive memory spaces for the subaddress and mode code descriptor table. The control registers are linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit commands (T/R bit equal zero or one).

Control word information allows the EXC-1553PCMCIA to generate interrupts, buffer messages, and control message processing. For a receive command, the Data List Pointer is read to determine the top of the data buffer. The EXC-1553PCMCIA stores data sequentially from the top of the data buffer plus two 16-bit locations (e.g., 0100, 0101, 0102, 0103, etc.). When processing a transmit command, the Data List

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Pointer is read to determine where data words are retrieved. The EXC-1553PCMCIA retrieves data words sequentially from the address Data List Pointer designates plus two 16-bit address locations.

The Broadcast Data Pointer allows for separate storage of non-broadcast data from broadcast data per MIL-STD-1553B Notice II. You can enable or disable this feature via the Control Word's least significant bit. When disabled, the non-broadcast and broadcast data are stored via Data List Pointer A or B. For transmit commands, the Broadcast Data Pointer is not used. The EXC-1553PCMCIA does not transmit any information on the receipt of a broadcast transmit command.

The EXC-1553PCMCIA reads the descriptor block during command processing (i.e., TERACT = 1. See the TERACT bit in the Operational Status Register, page 4-5). The EXC-1553PCMCIA then begins acquiring data words for either transmission or storage.

After transmission or reception, the EXC-1553PCMCIA begins post-processing. The Descriptor Block is updated. An optional interrupt log entry is performed after a descriptor update.

4.2 Control Registers—RT Mode

The control registers are read/write unless otherwise stated. All control registers must be accessed in word mode. All control register bits are active high and are reset to 0 unless otherwise stated.

Figure 4-1 below illustrates the control registers for Remote Terminal mode.

Illegalization Registers	40020-4003F H
Reserved	40014-4001E H
1553 Status Word Bits Register	40012 H
RT Descriptor Pointer Register	40010 H
Time Tag Register	4000E H
BIT Word Register	4000C H
Interrupt Log List Pointer Register	4000A H
Pending Interrupt Register	40008 H
Interrupt Mask Register	40006 H
Current Command Block Register	40004 H
Operational Status Register	40002 H
Setup Register	40000 H

Figure 4-1. Control Registers—RT Mode

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4.2.1 Setup Register

Address: 40000 (H)

The Setup Register controls RT Mode configuration. To make changes to the RT Mode and this register, the STEX bit (Bit 15) must be logic zero.

Bit	Bit Name	Description
15	STEX	Start Execution. 1 = Initiates RT Mode operation. 0 = Inhibits EXC-1553PCMCIA operation. A remote terminal address parity error prevents RT Mode operation regardless of the logical state of this bit. If an RT address parity error exists, bit 03 of the Operational Status Register will be set low and bit 02 of the Operational Status Register will be set high.
14	SBIT	Start BIT. 1 = Places the card into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. The host must halt the card in order to place it into the Built-In Test mode (STEX = 0). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13	SRST	Software Reset. 1 = Performs a software reset. The configuration registers are not affected when this bit is asserted. The software reset takes 6 usec. to execute.
12	CHAEN	Channel A Enable. 1 = Enables Channel A operation. 0 = The EXC-1553PCMCIA does not recognize commands received over Channel A.
11	CHBEN	Channel B Enable. 1 = Enables Channel B operation. 0 = The EXC-1553PCMCIA does not recognize commands received over Channel B.
05-10	Reserved	Set to 0
04	BCEN	Broadcast Enable. 1 = Enables the broadcast option for RT Mode. 0 = Enables remote terminal address 31 as a unique remote terminal address.

Setup Register (continues on next page)

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Bit	Bit Name	Description
03	DYNBC	Dynamic Bus Control Acceptance. This bit controls the EXC-1553PCMCIA's ability to accept the dynamic bus control mode code. 1 = Allows the EXC-1553PCMCIA to respond to a dynamic bus control mode code with status word bit 18 set to a logic one. 0 = Prevents the card from setting bit 18 of the status word upon reception of the dynamic mode code.
02	PPEN	Ping-Pong Enable. 1 = Enables the ping-pong buffer feature of the EXC-1553PCMCIA and disables the message indexing feature. 0 = Disables the ping-pong feature and enables the message indexing feature.
01	INTEN	Interrupt Log Enable. 1 = Enables the interrupt logging feature. 0 = Prevents the logging of interrupts.
00	XMTSW	Transmit Last Status Word. 1 = Allows the EXC-1553PCMCIA to automatically execute the TRANSMIT LAST STATUS WORD mode code when configured for MIL-STD-1553A mode operation.

Setup Register (continued from previous page)

4.2.2 Operational Status Register

Address: 40002 (H)

The Operational Status register reflects pertinent status information for RT Mode and defaults to ED82 (H) on reset.

NOTE To make changes to the RT Mode and this register, the STEX bit (Bit 15 in the Setup Register) must be logic zero.

Bit	Bit Name	Description
11-15	RTA[4-0]	Remote Terminal Address. These five bits contain the remote terminal address. This field defaults to 1F (H) on the falling (last) edge of a reset.
10	RTAPTY	Terminal Address Parity Bit. This bit is appended to the remote terminal address bus (RTA[4-0]) to supply odd parity. The EXC-1553PCMCIA requires odd parity for proper operation. This bit defaults to 1 on the falling (last) edge of a reset.
09	MSEL1	Mode Select 1. In conjunction with Mode Select 0, this bit determines the mode of operation of the EXC-1553PCMCIA.

Operational Status Register (continues on next page)

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Bit	Bit Name	Description
08	MSEL0	Mode Select 0. In conjunction with Mode Select 1, this bit determines the mode of operation of the EXC-1553PCMCIA.

MSEL1	MSEL0	Mode of Operation
0	0	BC Mode
0	1	RT Mode
1	0	Monitor Mode
1	1	RT/ Concurrent Monitor Mode

Bit	Bit Name	Description
07	A/B STD	Military Standard 1553A or 1553B. This bit determines whether the EXC-1553PCMCIA will operate under MIL-STD-1553A or 1553B protocol. 1 = Enables the XMTSW bit (Bit 00 of the Setup Register) (1553A). 0 = Automatically allows the EXC-1553PCMCIA to operate under the MIL-STD-1553B protocol.
06	LOCK	Lock Mode. This read-only bit indicates whether the card is currently in lock mode or not. 1 = The EXC-1553PCMCIA is in lock mode. In this mode, you cannot operate the EXC-1553PCMCIA in BC mode.
04-05	Reserved	These read-only bits are 0.
03	EX	EXC-1553PCMCIA Executing. This read-only bit indicates whether the card is presently executing or is idle. 1 = The EXC-1553PCMCIA is executing. 0 = The EXC-1553PCMCIA is idle.
02	TPARF	Terminal Parity Fail. Read only. This bit indicates the observance of a terminal address parity error. The EXC-1553PCMCIA checks for odd parity. This bit reflects the parity of Operational Status Register bits 15-10, and defaults to 1 on the falling (final) edge of a reset.
01	READY	Ready. Read-only. 1 = The EXC-1553PCMCIA has completed initialization or that the SUMMIT chip has completed BIT, and is cleared on reset.
00	TERACT	Teract. Read-only. 1 = The EXC-1553PCMCIA is presently processing a message.

Operational Status Register (continued from previous page)

NOTE Remote Terminal Address and Parity are checked on start of execution.

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4.2.3 Current Command Register — Address: 40004 (H) - READ ONLY

This 16-bit register contains the last valid command processed by the EXC-1553PCMCIA.

Bit	Bit Name	Description
00-15	CC[15-0]	Current Command. These bits contain the latest 1553 command that was received by the EXC-1553PCMCIA. This register is valid 13 usec. after the TERACT bit (Bit 00 of the Operational Status Register) is set to 0. (Bit 15 MSB - Bit 00 LSB).

Current Command Register

4.2.4 Interrupt Mask Register — Address: 40006 (H)

The EXC-1553PCMCIA interrupt architecture allows for the masking of all interrupts. An interrupt is masked if the corresponding bit of this register is set to logic zero. This feature allows the host to temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event.

Bit	Bit Name	Description
15	DMAF	DMA Fail Interrupt
14	WRAPF	Wrap Fail Interrupt
13	TAPF	Terminal Address Parity Fail Interrupt
12	BITF	BIT Fail Interrupt
11	MERR	Message Error Interrupt
10	SUBAD	Subaddress Accessed Interrupt
09	BDRCV	Broadcast Command Received Interrupt
08	IXEQ0	Index Equal Zero Interrupt
07	ILLCMD	Illegal Command Interrupt
00-06	Reserved	Set to 0

Interrupt Mask Register

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4.2.5 Pending Interrupt Register — Address: 40008 (H) - READ ONLY

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. A 125 nsec. interrupt is generated when any bit in this register is set by the card. A register read of the Pending Interrupt Register will clear all bits.

Bit	Bit Name	Description
15	DMAF	DMA Fail Interrupt. Indicates that a memory access failed.
14	WRAPF	Wrap Fail Interrupt. The EXC-1553PCMCIA automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set and an interrupt is generated. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	TAPF	Terminal Address Parity Fail Interrupt. This bit reflects the outcome of the remote terminal address parity check. 1 = A parity failure. When a parity error occurs, the EXC-1553PCMCIA does not begin operation (STEX bit forced to logic zero), channel A and B do not enable, the EXC-1553PCMCIA sets the TAPF bit here and in the BIT Word Register, and an interrupt is generated (if not masked).
12	BITF	BIT Fail Interrupt. 1 = A BIT failure. Interrogate Bit Word Register bits 11 and 10 to determine the specific channel that failed. In BC mode, an interrupt is generated and command processing stops if initiated by opcode.
11	MERR	Message Error Interrupt. 1 = A message error occurred. The EXC-1553PCMCIA can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.

Pending Interrupt Register (continues on next page)

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Bit	Bit Name	Description
10	SUBAD	Subaddress Accessed Interrupt. 1 = The board has processed a message for which the IWA bit in the associated descriptor block is set (see "Receive Control Word," page 4-15). To determine the exact subaddress, the host checks the interrupt log IAW. An interrupt is generated.
09	BDRCV	Broadcast Command Received Interrupt. 1 = The EXC-1553PCMCIA's receipt of a valid broadcast command. The EXC-1553PCMCIA suppresses status word transmission. An interrupt is generated.
08	IXEQ0	Index Equal Zero Interrupt. The EXC-1553PCMCIA sets this bit to 1 to indicate the completion of a pre-defined number of commands by the RT. Upon assertion of this interrupt, the host updates the subaddress descriptor to prevent the potential loss of data. An interrupt is generated.
07	ILCMD	Illegal Command Interrupt. 1 = The EXC-1553PCMCIA received an illegal command. Upon receipt of this command, the EXC-1553PCMCIA responds with a status word only; Bit 09 of the status word is set to a logic one. An interrupt is generated.
00-06	Reserved	These read-only bits are 0.

Pending Interrupt Register (continued from previous page)

4.2.6 Interrupt Log List Pointer Register

Address: 4000A (H)

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32 word ring-buffer that contains information pertinent to the service of interrupts. The EXC-1553PCMCIA architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K word memory space. The lower 5 bits of this register should be initialized to a logic zero by the host. The EXC-1553PCMCIA controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	INT[15-0]	Interrupt Log List Pointer Bits. (Bit 15 MSB - Bit 00 LSB)

Interrupt Log List Pointer Register

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4.2.7 BIT Word Register

Address: 4000C (H)

The BIT Word register contains information on the current status of the EXC-1553PCMCIA. The EXC-1553PCMCIA transmits the contents of this register upon reception of a Transmit BIT Word Mode Code.

Bit	Bit Name	Description
15	DMAF	DMA Fail. 1 = A memory access failed.
14	WRAPF	Wrap Fail. The EXC-1553PCMCIA automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set. The loop-back path is via the MIL-STD-1553 bus transceiver.
13	TAPF	Terminal Address Parity Fail. This bit reflects the outcome of the remote terminal address parity check. 1 = A parity failure. When a parity error occurs the EXC-1553PCMCIA does not begin operation (STEX bit forced to a logic zero), channel A and B do not enable, and an interrupt is generated (if not masked).
12	BITF	BIT Fail. 1 = A BIT failure. Interrogate bit 11 and 10 to determine the specific channel that failed.
11	CHAF	Channel A Fail. 1 = A BIT test failure in Channel A.
10	CHBF	Channel B Fail. 1 = A BIT test failure in Channel B.
00-09	Reserved	Ignore on read.

BIT Word Register

4.2.8 Time-Tag Register

Address: 4000E (H)

The Time-Tag register reflects the state of a 16-bit free running counter. The resolution of this counter is 64 usec./bit. The Time-Tag counter is automatically reset when the EXC-1553PCMCIA receives a valid synchronize without data mode code. The EXC-1553PCMCIA automatically loads the Time-Tag counter with the data associated with reception of a valid synchronize with data mode code.

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The Time-Tag counter begins operation in either of two cases:

- within 64 usec. of the rising (final) edge of a reset
- after the receipt of one of the following valid mode codes:
  - reset of the remote terminal
  - sync with/without data

When the EXC-1553PCMCIA is halted (STEX = 0), the Time-Tag continues to run.

Bit	Bit Name	Description
00-15	TT[15-0]	Time-Tag Counter Bits. (Bit 15 MSB - Bit 00 LSB)

Time-Tag Register

4.2.9 Remote Terminal Descriptor Pointer Register

Address: 40010 (H)

Each subaddress and mode code has a reserved block of memory containing information about how to process a valid command to that subaddress or mode code. Located contiguously in memory, these reserved memory locations are called a descriptor space. The Remote Terminal Descriptor Pointer Register contains an address that points to the top of this memory space. The EXC-1553PCMCIA uses the T/R bit, subaddress/mode code field, and mode code to select one block within the descriptor table for message processing. The Remote Terminal Descriptor Pointer Register is static during message processing.

Bit	Bit Name	Description
00-15	RTA[15-0]	Remote Terminal Descriptor Address Bits. (Bit 15 MSB - Bit 00 LSB)

Remote Terminal Descriptor Pointer Register

4.2.10 1553 Status Word Bits Register

Address: 40012 (H)

The 1553 Status Word Bits register controls the outgoing MIL-STD-1553 status word. The host controls the Instrumentation, Busy, Terminal Flag, Service Request, and Subsystem Flag by writing to bits 09 through 00 of this register. The EXC-1553PCMCIA's status word response reflects assertion of these bit(s) until negated by the host unless the Immediate Clear Function is enabled. The Immediate Clear Function automatically clears these bits after being transmitted in a status word.

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The Immediate Clear Function does not affect the operation of the Transmit Last Status word and Transmit Last Command word Mode Codes. Transaction of a legal valid command with the INS bit set to a logic one and the Immediate Clear Function enabled, results in the transmission of a status word with Bit 10 set. If the ensuing command is a Transmit Last Status word or Last Command mode code, Bit 10 of the outgoing status word remains a logic one.

For MIL-STD-1553B applications, the 1553 Status Word Bits register is as follows:

Bit	Bit Name	Description
15	IMCLR	Immediate Clear Function. 1 = Enables the Immediate Clear Function (IMF) of the EXC-1553PCMCIA. Enabling the IMF results in the clearing of the INS, BUSY, TF, SRQ, and/or SUBF bit immediately after a message is completed. To enable this function, set this bit to 1 when setting bit(s) INS, BUSY, TF, SRQ, and/or SSYSF to 1. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
10-14	Reserved	Set to 0
09	INS	Instrumentation Bit. This bit sets the Instrumentation bit of the MIL-STD-1553B status word. (Bit 10 of the Status Word).
08	SRQ	Service Request Bit. This bit sets the Service Request bit of the MIL-STD-1553B status word. (Bit 11 of the Status Word).
04-07	Reserved	Set to 0
03	BUSY	Busy Bit. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. 1 = Prevents memory accesses. (Bit 16 of the Status Word).
02	SSYF	Subsystem Flag Bit. This bit sets the Subsystem Flag bit of the MIL-STD-1553B status word. (Bit 17 of the Status Word).
01	Reserved	Set to 0
00	TF	Terminal Flag. Assertion of this bit is reflected in the outgoing MIL-STD-1553B status word. The EXC-1553PCMCIA automatically sets this bit if a BIT failure occurs. Inhibit Terminal Flag mode code prevents the assertion by the host. Override Inhibit Terminal Flag Mode Code re-establishes the Terminal Flag option. (Bit 19 of the Status Word).

1553 Status Word Bits Register—MIL-STD-1553B

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For MIL-STD-1553A applications, the 1553 Status Word Bits register is as follows:

Bit	Bit Name	Description
15	IMCLR	Immediate Clear Function. 1 = Enables the Immediate Clear Function (IMF) of the EXC-1553PCMCIA. Enabling the IMF results in the clearing of the bits 10-19 immediately after a status word is transmitted. To enable this function, set this bit when writing to bits 10-19. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
10-14	Reserved	Set to 0
09	SB10	Status bit time 10
08	SB11	Status bit time 11
07	SB12	Status bit time 12
06	SB13	Status bit time 13
05	SB14	Status bit time 14
04	SB15	Status bit time 15
03	SB16	Status bit time 16
02	SB17	Status bit time 17
01	SB18	Status bit time 18
00	SB19	Status bit time 19

1553 Status Word Bits Register—MIL-STD-1553A

4.2.11 Illegalization Registers

Address: 40020 - 4003F (H)

The 16 registers are divided into 8 blocks, 2 registers per block, as shown in Table 4-1 below:

Block Name	Address (H)
Receive	40020 and 40022
Transmit	44024 and 40026
Broadcast Receive	40028 and 4002A
Broadcast Transmit (Automatically Illegalized)	4002C and 4002E
Mode Code Receive	40030 and 40032
Mode Code Transmit	40034 and 40036
Broadcast Mode Code Receive	40038 and 4003A
Broadcast Mode Code Transmit	4003C and 4003E

Table 4-1. Illegalization Register Blocks

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The blocks correspond to the following types of commands. Register address 40020 (H) and 40022 (H) illegalize receive commands to 32 subaddresses. The most significant bit of register 40020 (H) controls the illegalization of subaddress 01111. The least significant bit controls subaddress 00000. Register 40022 (H) controls illegalization of subaddresses 10000 through 11111. The least significant bit relates to subaddress 10000; the most significant bit relates to subaddress 11111. Transmit commands and broadcast commands (both receive and transmit) use the same encoding scheme as receive subaddress illegalization.

Register 40030 (H) through 4003E (H) controls the illegalization of mode codes. Register 40030 (H) governs the illegalization of receive mode codes (T/R bit = 0) 00000 through 01111 and register 40032 (H) mode codes 10000 through 11111. Register blocks Transmit Mode Code (T/R bit = 1), Broadcast Receive Mode Codes, and Broadcast Transmit Mode Codes use the same decode scheme as receive mode codes.

Table 4-2 shows the illegalization register map. For Receive, Transmit, Broadcast Receive, and Broadcast Transmit blocks, the numbers shown in the column under each bit number identify the specific subaddress or mode code (in hex) that the register bit illegalizes (Logical 0 = legal, Logical 1 = illegal).

Name	Register Address (H) (40000 +)															
Bit Number		15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Receive	20	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	22	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Transmit	24	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	26	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Board Receive	28	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	2A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Board Transmit	2C	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
	2E	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
Mode Receive	30	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	32	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Transmit	34	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	36	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Board Receive	38	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	3A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Board Transmit	3C	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	3E	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY

Table 4-2. Illegalization Register Map

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Notes:

1. Brd = Broadcast
2. Mode = Mode code
3. XX = Automatically illegalized by EXC-1553PCMCIA.
4. YY = Automatically illegalized by EXC-1553PCMCIA in 1553B only.
5. ZZ = Automatically illegalized by EXC-1553PCMCIA in 1553B and 1553A if XMTSW is enabled.
6. WW = Automatically illegalized in 1553A.
7. UU = Automatically illegalized in 1553A if XMTSW enabled.

4.3 Descriptor Block

The EXC-1553PCMCIA accesses a four 16-bit word descriptor block stored in RAM. The descriptor block is accessed at the beginning and end of command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The EXC-1553PCMCIA allocates 512 consecutive memory spaces for the subaddress and mode code descriptor table (see Figure 4-2). The top of the descriptor table can reside at any address location. The control registers are linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit commands (T/R bit equals zero or one).

The EXC-1553PCMCIA reads the descriptor block during command processing (i.e., after setting the TERACT bit). The EXC-1553PCMCIA then begins acquiring data words for either transmission or storage.

After transmission or reception, the EXC-1553PCMCIA begins post-processing. The Descriptor Block is updated. During the descriptor update, the EXC-1553PCMCIA modifies the Control Word index field and bits 4, 2, and 1, if required. The EXC-1553PCMCIA updates Data Pointer A and B if no message errors occurred during the message transaction. Neither Data Pointer A or B is updated if the EXC-1553PCMCIA has the ping-pong mode of operation enabled. When a broadcast command is received, with no message errors, the Broadcast Data Pointer is updated. The card performs an optional interrupt log entry after a descriptor update.

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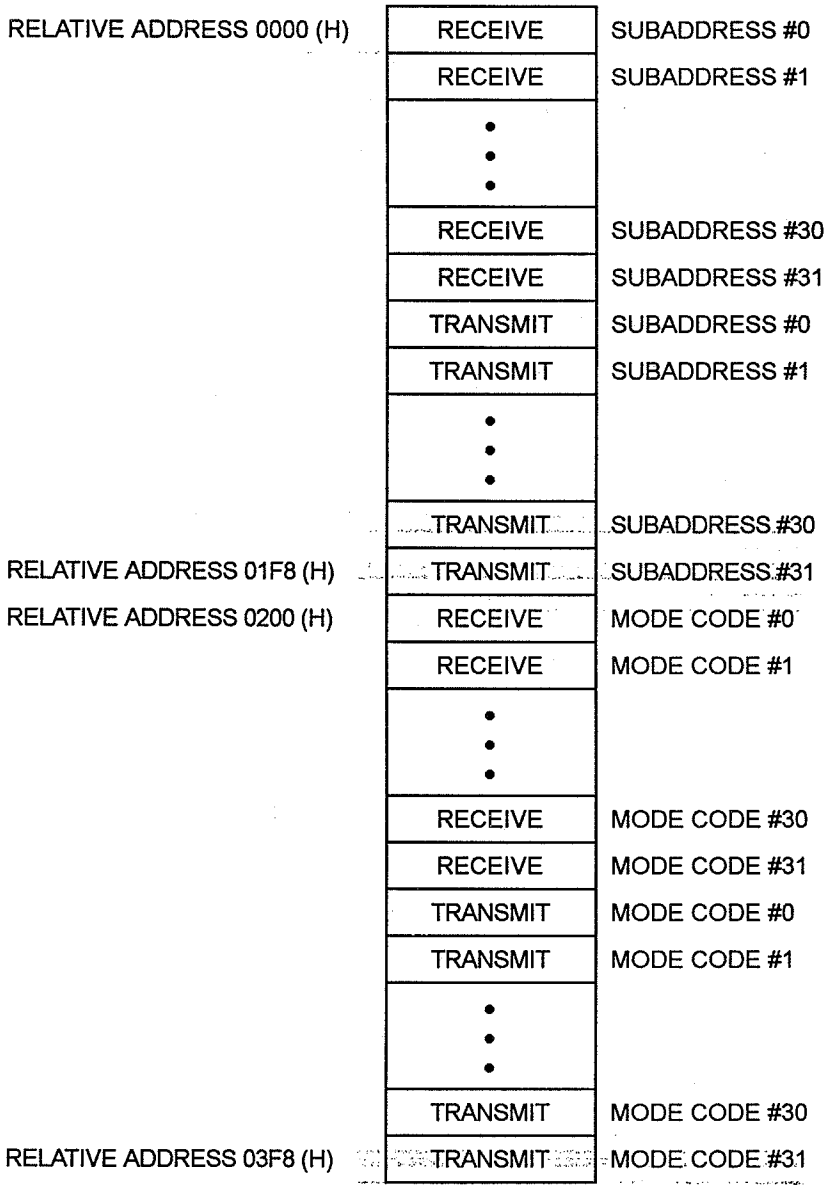


Figure 4-2. Descriptor Table

4.3.1 Receive Control Word

Information contained in the Receive Control word assists the EXC-1553PCMCIA in message processing. The following bits describe the receive subaddress descriptor Control word. The descriptor control word is initialized by the host and updated by the EXC-1553PCMCIA during command post-processing.

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Bit	Bit Name	Description
08-15	INDX	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the EXC-1553PCMCIA to buffer "N" messages. "N" can range from 0 (00 H) to 256 (FF H). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). During ping-pong mode operation, you should initialize the index field to 00 (H). The RT does not perform multiple message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the subaddress is illegalized. The EXC-1553PCMCIA can generate an interrupt when the index field transitions from one to zero (see bit 07).
07	INTX	Interrupt Index Equals Zero. 1 = Enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
06	IWA	Interrupt When Accessed. 1 = Enables the generation of an interrupt when the subaddress receives a valid command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	IBRD	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when the subaddress receives a valid broadcast command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	BAC	Block Accessed. The host initializes this bit to zero; the EXC-1553PCMCIA overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	Reserved	Set to 0
02	A/B	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a "don't care" if buffer ping-ponging is not enabled.
01	BRD	Broadcast Received. 1 = Reception of a valid broadcast command.
00	NII	Notice II. 1 = Enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. 0 = Broadcast information is stored in the same buffer as non-broadcast information.

Receive Control Word

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4.3.2 Transmit Control Word

Information contained in the Transmit Control word assists the EXC-1553PCMCIA in message processing. The following bits describe the transmit subaddress descriptor Control word. The descriptor control word is initialized by the host and updated by the EXC-1553PCMCIA during command post-processing.

Bit	Bit Name	Description
07-15	Reserved	Set to 0
06	IWA	Interrupt When Accessed. 1 = Enables the generation of an interrupt when the subaddress receives a valid command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	Reserved	Set to 0
04	BAC	Block Accessed. The host initializes this bit to zero; the EXC-1553PCMCIA overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	Reserved	Set to 0
02	A/B	Buffer A/B. Indicates the data pointer to access when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a "don't care" if buffer ping-ponging is not enabled.
01	BRD	Broadcast Received. 1 = Reception of a broadcast command.
00	Reserved	Set to 0

Transmit Control Word

4.3.3 Mode Code Receive Control Word

Information contained in the Mode Code Receive Control word assists the EXC-1553PCMCIA in message processing. The following bits describe the receive mode code descriptor Control word. The descriptor control word is initialized by the host and updated by the EXC-1553PCMCIA during command post-processing.

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NOTE In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Bit Name	Description
08-15	INDX	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the EXC-1553PCMCIA to buffer "N" messages. "N" can range from 0 (00 H) to 256 (FF H). If buffer ping-ponging is enabled, the INDX field is "don't care" (i.e., does not contain applicable information). The EXC-1553PCMCIA does not perform message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the mode code is illegalized. The EXC-1553PCMCIA can generate an interrupt when the index field transitions from one to zero (see bit 07).
07	INTX	Interrupt Index Equals Zero. 1 = Enables the generation of an interrupt when the index field transitions from one to zero. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
06	IWA	Interrupt When Accessed. 1 = Enables the generation of an interrupt when mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	IBRD	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when a valid broadcast mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	BAC	Block Accessed. The host initializes this bit to zero; the EXC-1553PCMCIA overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	Reserved	Set to 0
02	A/B	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, you designate the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a "don't care" if buffer ping-ponging is not enabled.
01	BRD	Broadcast Received. 1 = Reception of a valid broadcast command.
00	NII	Notice II. 1 = Enables the use of the Broadcast Data Pointer as a buffer for broadcast command information. 0 = Broadcast information is stored in the same buffer as non-broadcast information.

Mode Code Receive Control Word

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4.3.4 Mode Code Transmit Control Word

Information contained in the Mode Code Transmit Control word assists the EXC-1553PCMCIA in message processing. The following bits describe the transmit mode code descriptor Control word. You initialize the descriptor control word and the EXC-1553PCMCIA updates it during command post-processing.

NOTE In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Bit Name	Description
07-15	Reserved	Set to 0
06	IWA	Interrupt When Accessed. 1 = Enables the generation of an interrupt when mode code command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	IBRD	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when a broadcast mode code is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	BAC	Block Accessed. The host initializes this bit to zero; the EXC-1553PCMCIA overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	Reserved	Set to 0
02	A/B	Buffer A/B. This bit indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, you designate the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a "don't care" if buffer ping-ponging is not enabled.
01	BRD	Broadcast Received. 1 = Reception of a broadcast command.
00	Reserved	Set to 0

Mode Code Transmit Control Word

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4.3.5 Data Pointer A and B

Data List Pointer A and B contains address information for the retrieval and storage of message data words. In the index mode of operation, the EXC-1553PCMCIA reads Data Pointer A to determine the location of data for retrieval or storage. The EXC-1553PCMCIA uses the Data Pointer to initialize an internal counter, which increments after each data word. For a receive command, the EXC-1553PCMCIA stores the incoming data word sequentially into memory. As part of command post-processing, the EXC-1553PCMCIA writes a new data pointer into the descriptor block. The EXC-1553PCMCIA continues to update the data pointer until the Control Word index field decrements to zero. An example is shown in Figure 4-3.

NOTE The index feature is not applicable for transmit commands (i.e., T/R bit = 1).

Bit	Bit Name	Description
00-15	DP[15-0]	Data Pointer Bits. The second and third words of the descriptor block contain the data buffer location. The EXC-1553PCMCIA accesses either Data Pointer A or Data Pointer B depending on the state of Control Word Bit 02 during ping-pong operation. For index operation, the EXC-1553PCMCIA accesses only Data Pointer A. The EXC-1553PCMCIA updates data pointer A after message processing is complete and the index field is not equal to zero and ping-pong operation disabled. Bit 15 is the most significant bit; bit 00 is the least significant bit.

Data Pointer A and B

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Receive Subaddress #1 Descriptor Block	CONTROL WORD	Index field contents: 03XX (H)	
	DATA POINTER A	Data Pointer A: 0100 (H)	
	DATA POINTER B	Data Pointer B: XXXX (H)	
	BROADCAST DATA POINTER	Broadcast Data Pointer: XXXX (H)	
Command #1 Receive three words	Message Info Word	0100 (H)	Index equals three
	Time-Tag	0102 (H)	
	Data Word #1	0104 (H)	
	Data Word #2	0106 (H)	
	Data Word #3	0108 (H)	Index decrements to two
Command #2 Receive two words	Message Info Word	010A (H)	Index equals two
	Time-Tag	010C (H)	
	Data Word #1	010E (H)	
	Data Word #2	0110 (H)	Index decrements to one
Command #3 Receive three words	Message Info Word	0112 (H)	Index equals one
	Time-Tag	0114 (H)	
	Data Word #1	0116 (H)	
	Data Word #2	0118 (H)	
	Data Word #3	011A (H)	Index decrements to zero [Data Pointer A updated to 011C (H), interrupt generated enabled]

Note: X = "don't care"

Figure 4-3. Non-Broadcast Receive Message Indexing

For ping-pong buffer operation, the host uses either Data Pointer A or Data Pointer B. The EXC-1553PCMCIA determines which pointer to access via the state of Control Word bit 02. The EXC-1553PCMCIA retrieves or stores data words from the address contained in the data pointer, automatically incrementing the data pointer as data words are received. The data pointer is never updated as part of command post-processing in the ping-pong mode of operation. See Figures 4-4 and 4-5.

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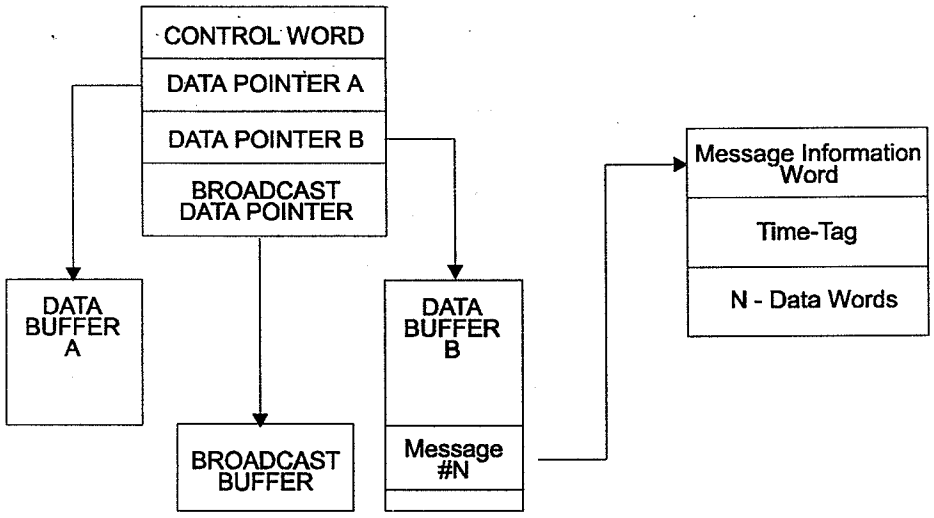


Figure 4-4. EXC-1553PCMCIA Descriptor Block (Receive)

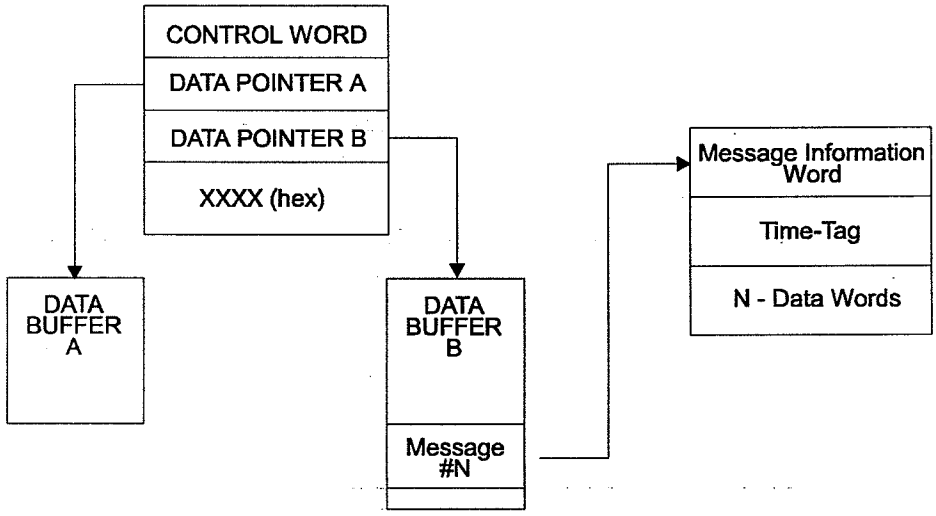


Figure 4-5. EXC-1553PCMCIA Descriptor Block (Transmit)

4.3.6 Broadcast Data Pointer

The Broadcast Data Pointer contains the address for the Message Information word, Time-Tag word, and data words associated with a broadcast command. The following bits describe the receive subaddress/mode code descriptor Broadcast Data Pointer. The EXC-1553PCMCIA automatically increments this data pointer during command post-processing, if ping-pong operation disabled.

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Bit	Bit Name	Description
00-15	BP[15-0]	Broadcast Data Pointer. The fourth word of the descriptor block contains the broadcast data buffer location. This pointer can reside anywhere in memory space. The EXC-1553PCMCIA accesses this pointer when Control Word bit 00 is a logic one and broadcast is enabled. Bit 15 is the most significant bit, bit 00 is the least significant bit. Note: If ping-pong is enabled, this pointer does not update. Note: When the broadcast command is followed by a Transmit Last Command or Last Status Word mode code, the EXC-1553PCMCIA transmits a status word with bit 15 of the status word set to a logic one. The broadcast bit is cleared when the next valid non-broadcast command is received.

Broadcast Data Pointer

4.4 Data Structures

The following sections discuss the data structures that result from command processing. For each complete message processed, the EXC-1553PCMCIA generates a Message Information word and Time-Tag word. These words aid the host in further message processing. The Message Information word contains word count, message type, and message error information. The Time-Tag word is a 16-bit word containing the command validity time. The Time-Tag word data comes from the EXC-1553PCMCIA's internal Time-Tag counter.

4.4.1 Subaddress Receive Data

For receive commands, the EXC-1553PCMCIA stores data words plus two additional words. The EXC-1553PCMCIA adds a Receive Information word and Time-Tag word to each receive command data packet. The EXC-1553PCMCIA places the Receive Information word and Time-Tag word ahead of the data words associated with a receive command (see Figures 4-3, 4-4 and 4-5 above). When message errors occur, the EXC-1553PCMCIA stores the Receive Information word and Time-Tag word. Once a message error condition is observed, all data words are considered invalid.

Data storage occurs at the memory location pointed to by the data pointer plus two 16-bit locations.

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RECEIVE INFORMATION WORD

The following bits describe the Receive Information Word contents:

Bit	Bit Name	Description
11-15	WC[4-0]	Word Count Bits. These five bits contain word count information extracted from the receive command word bits 15 to 19.
10	Reserved	Ignore on read.
09	CHA/B	Channel A/B. 1 = The message was received on channel A. 0 = The message was received on channel B.
08	RTRT	Remote Terminal to Remote Terminal Transfer. The command processed was an RT-to-RT transfer.
07	ME	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	Reserved	Ignore on read.
04	ILL	Illegal Command Received. 1 = The command received was an illegal command.
03	TO	Time-Out Error. 1 = The EXC-1553PCMCIA did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
02	OVR	Overrun Error. 1 = The EXC-1553PCMCIA received a word when none was expected or the number of data words received was greater then expected.
01	PRTY	Parity Error. 1 = The EXC-1553PCMCIA observed a parity error in the incoming data words.
00	MAN	Manchester Error. 1 = The EXC-1553PCMCIA observed a Manchester error in the incoming data words.

Receive Information Word

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4.4.2 Subaddress Transmit Data

You are responsible for organizing the data packet (i.e., N data words) into memory and establishing the applicable data pointer. You can allocate two 16-bit memory locations at the top of the data packet for the storage of the Transmit Information word and the Time-Tag word. An example transmit data structure for three words is shown below:

Data Pointer A ⟶	0100 (H)	XXXX	Reserved for Transmit Info word
equals 0100 (H)	0102 (H)	XXXX	Reserved for Time-Tag word
	0104 (H)	FFFF	Data word
	0106 (H)	FFFF	Data word
	0108 (H)	FFFF	Data word

NOTE Data Pointer A points to the top of the data structure, not to the top of the data words.

TRANSMIT INFORMATION WORD

The following bits describe the Transmit Information word contents:

Bit	Bit Name	Description
11-15	WC[4-0]	Word Count Bits. These five bits contain word count information extracted from the receive command word bits 15 to 19.
10	Reserved	Ignore on read.
09	CHA/B	Channel A/B. 1 = The message was received on the A bus. 0 = The message was received on the B bus.
08	Reserved	Ignore on read.
07	ME	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for more detail.
05-06	Reserved	Ignore on read.
04	ILL	Illegal Command Received. 1 = The command received was an illegal command.
03	Reserved	Ignore on read.
02	OVR	Overrun Error. 1 = The EXC-1553PCMCIA received a data word with a Transmit Command.
00-01	Reserved	Ignore on read.

Transmit Information Word

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4.4.3 Mode Code Data

The transmit and receive data structures for mode codes are similar to those for a subaddress. The receive data structure contains an Information word, Time-Tag word, and message data word. All receive mode codes with data have one associated data word. Data storage occurs at the memory location pointed to by the data pointer plus two 16-bit locations. Reception of the synchronize with data mode code automatically loads the Time-Tag counter and stores the data word at the address defined by the data pointer plus two 16-bit locations.

The transmit mode code data structure contains an Information word, Time-Tag word, and associated data word. The host is responsible for linking the EXC-1553PCMCIA Data Pointer to the data (e.g., Transmit Vector word). For mode codes with internally generated data words (e.g., Transmit BIT word, Transmit Last Command), the transmitted data word is added to the data structure.

For MIL-STD-1553A mode of operation, all mode codes are defined without data words. For mode codes without data, the data structure contains the Message Information word and Time-Tag word only.

NOTE In MIL-STD-1553A, all mode codes are without data and the T/R bit is ignored.

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MODE CODE RECEIVE INFORMATION WORD

The following bits describe the Mode Code Receive Information word contents:

Bit	Bit Name	Description
11-15	MC[4-0]	Mode Code. These five bits contain the mode code information extracted from the receive command word bits 15 to 19.
10	Reserved	Ignore on read.
09	CHA/B	Channel A/B. 1 = The message was received on the A bus. 0 = The message was received on the B bus.
08	RTRT	Remote Terminal to Remote Terminal Transfer. 1 = The command processed was an RT-to-RT transfer.
07	ME	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	Reserved	Ignore on read.
04	ILL	Illegal Command Received. 1 = The command received was an illegal command.
03	TO	Time-out Error. 1 = The EXC-1553PCMCIA did not receive the proper number of data words, i.e., the number of data words received was less than the word count specified in the command word.
02	OVR	Overrun Error. 1 = The EXC-1553PCMCIA received a word when none was expected, or the number of data words received was greater than expected.
01	PRTY	Parity Error. 1 = The EXC-1553PCMCIA observed a parity error in the incoming data words.
00	MAN	Manchester Error. 1 = The EXC-1553PCMCIA observed a Manchester error in the incoming data words.

Mode Code Receive Information Word

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MODE CODE TRANSMIT INFORMATION WORD

The following bits describe the Mode Code Transmit Information word contents:

Bit	Bit Name	Description
11-15	MC[4-0]	Mode Code. These five bits contain the mode code information extracted from the command word bits 15 to 19.
10	Reserved	Ignore on read.
09	CHA/B	Channel A/B. 1 = The message was received on the A bus. 0 = The message was received on the B bus.
08	Reserved	Ignore on read.
07	ME	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	Reserved	Ignore on read.
04	ILL	Illegal Command Received. 1 = The command received was an illegal command.
03	Reserved	Ignore on read.
02	OVR	Overrun Error. 1 = The EXC-1553PCMCIA received a data word with a Transmit Command.
00-01	Reserved	Ignore on read.

Mode Code Transmit Information Word

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4.5 Mode Code and Subaddress

The EXC-1553PCMCIA provides subaddress and mode code decoding that meets MIL-STD-1553B requirements. In addition, the card has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. Table 4-3 shows the EXC-1553PCMCIA's response to all possible mode code combinations.

T/R	Mode Code	Function	Operation
0	00000-01111	Undefined (w/o data)	1. Command word stored 2. Status word transmitted
0	10000	Undefined (with data)	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10001	Synchronize (with data)	1. Command Word stored 2. Data word stored 3. Time-Tag counter loaded with data word value 4. Status word transmitted
0	10010	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10011	Undefined	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10100	Selected Transmitter Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10101	Override Selected Transmitted Shutdown	1. Command word stored 2. Data word stored 3. Status word transmitted
0	10110-11111	Reserved	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control	1. Command word stored 2. Dynamic Bus Acceptance bit set in outgoing status word if enabled in the Setup Register 3. Status word transmitted
1	00001	Synchronize	1. Command word stored 2. Time-Tag counter reset to 0000 (H) 3. Status word transmitted

Table 4-3. Mode Code Description

(The Mode Code Description table continues on the next page.)

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T/R	Mode Code	Function	Operation
1	00010	Transmit Status Word	1. Command word stored 2. Last status word transmitted 3. Status word cleared after reset Note: EXC-1553PCMCIA updates status word if illegalized
1	00011	Initiate Self-Test	1. Command word stored 2. Status word transmitted 3. BIT initiated 4. TF bit set if BITF bit asserted
1	00100	Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus disabled
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Status word transmitted 3. Alternate bus enabled Note: Reception of the override transmitter shut-down mode code does not enable a channel not previously enabled in the Setup Register. Reset remote terminal mode code clears the transmitter shutdown function.
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal flag bit set to zero and assertion disabled 3. Status word transmitted
1	001111	Override Inhibit Terminal Flag	1. Command Word stored 2. Terminal flag bit enabled for assertion 3. Status word transmitted
1	01000	Reset Remote Terminal	1. Command word stored 2. Status word transmitted 3. Software reset
1	01001-01111	Reserved	1. Command word stored 2. Status word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Service request bit set to a logic zero in out going status 3. Status word transmitted 4. Data word transmitted 5. Clears the SRQ bit in the 1553 Status Word Bits Register
1	10001	Reserved	1. Command word stored 2. Status word transmitted 3. Data word stored

Table 4-3. Mode Code Description (continues on next page)

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T/R	Mode Code	Function	Operation
1	10010	Transmit Last Command	1. Command word stored 2. Last status word transmitted 3. Last command word transmitted 4. Data word stored (Transmit Last Command) 5. Transmitted data word is all zero reset Note: EXC-1553PCMCIA stores the Transmit Last Command mode code if illegalized and updates status word
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. BIT word transmitted from BIT Word Register 4. Data word stored (Transmit BIT Word)
1	10100-10101	Undefined (with data)	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10110-11111	Reserved	1. Command word stored 2. Status word transmitted 3. Data word transmitted

Table 4-3. Mode Code Description (continued from previous page)

4.6 Encoder and Decoder

The EXC-1553PCMCIA receives the command word from the MIL-STD-1553 bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the EXC-1553PCMCIA processes each incoming data word for correct format, word count, and contiguous data. If a message error is detected, the EXC-1553PCMCIA stops processing the remainder (if any) of the message, suppresses status word transmission, and asserts bit 09 (ME bit) of the status word.

The EXC-1553PCMCIA automatically compares the transmitted word (encoder word) with the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is asserted in the BIT Word Register and an interrupt will be generated, if enabled. In addition to the loop-back compare test, a timer precludes a transmission greater than 800 usec. by the assertion of Fail-Safe Timer. This timer is reset upon receipt of another command.

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Remote Terminal Response-Time:

MIL-STD-1553A = 7 usec.

MIL-STD-1553B = 10 usec.

Data Contiguity Time-Out = 1.0 usec.

4.7 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic ensures that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the message-error bit and suppressing transmission of the status word. (RT-to-RT transfer time-out = 55 to 59 usec.). EXC-1553PCMCIA does not check ME or SSYSF of the transmitting remote terminal when receiving.

4.8 Terminal Address

The EXC-1553PCMCIA Terminal Address is programmed via the most significant six bits in the Operational Status Register: RTA[4-0] and RTPTY. The Terminal Address parity is odd; RTPTY is set to a logic state to satisfy this requirement. When the Operational Status Register bit 02 (TAPF) is set, this indicates incorrect Terminal Address parity. The Operational Status Register bit 02 is valid after the rising (final) edge of a reset.

For example:

RTA[4-0] = 05(H) = 00101

RTPTY = 1(H) = 1 Sum of 1s = 3 (odd), Operational Status Register Bit 02 = 0

RTA[4-0] = 04 (H) = 00100

RTPTY = 0 (H) = 0 Sum of 1s = 1 (odd), Operational Status Register Bit 02 = 0

RTA[4-0] = 04 (H) = 00100

RTPTY = 1 (H) = 0 Sum of 1s = 2 (even), Operational Status Register Bit 02 = 0

NOTE The EXC-1553PCMCIA checks the Terminal Address and parity after RT mode operation has been started. With Broadcast disabled, RTA(4:0) = 11111 operates as a normal RT address.

The BIT Word Register parity fail bit is valid after RT mode has been started.

The Terminal Address is also programmed via a write to the Operational Status Register. The EXC-1553PCMCIA loads the Terminal Address upon completion of the Setup Register write which activates RT mode.

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4.9 Reset

The EXC-1553PCMCIA provides for several different reset mechanisms. The configuration register reset bit (Configuration Register 1 Bit 07) is equivalent to a hardware reset. Set this bit to 1 immediately to reset the EXC-1553PCMCIA and terminate command processing. You are responsible for resetting the reset bit and re-initializing the EXC-1553PCMCIA for operation.

The software reset bit (Setup Register Bit 13) is also equivalent to a hardware reset and takes 6 usec. to complete. Set this bit to 1 immediately to reset the EXC-1553PCMCIA and terminate command processing. You are responsible for re-initializing the EXC-1553PCMCIA for operation.

A Reset Remote Terminal mode code (Mode Code 01000, T/R = 1) clears the encoder/decoders, resets the time-tag, enables the channels to the programmed host state, and re-enables the Terminal Flag for assertion. This reset is performed after the 1553 Status word is transmitted.

4.10 MIL-STD-1553A Operation—RT Mode

To maximize flexibility, the EXC-1553PCMCIA can operate in many different systems which use various protocols. Specifically, two of the protocols that the EXC-1553PCMCIA may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, you can configure the EXC-1553PCMCIA through the control register. Table 4-4 defines the three ways to program the EXC-1553PCMCIA.

A/B STD	XMIT SW	RESULT (protocol selected)
0	X	1553B response, 1553B Standard
1	0	1553A response, 1553A Standard
1	1	1553A response, Auto execute the TRANSMIT LAST STATUS WORD mode code.

Table 4-4. MIL-STD-1553A Operation—RT Mode

When configured as a remote terminal to meet MIL-STD-1553A, the EXC-1553PCMCIA will operate as follows:

- Responds with a status word within 7 usec.
- Ignores the T/R bit for all mode codes.
- All mode codes are defined without data.
- All mode codes use mode code transmit control and information words.

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- Mode code 00000 is defined as dynamic bus control (DBC).
- Subaddress 00000 defines a mode code.
- ME and TF bits are defined in the 1553 status word.
- All other status word bits are programmable (i.e., NO BUSY mode, etc.)
- Broadcast of all mode codes, except Mode Code 00000 (DBC) and mode code 00010 (transmit status word if enabled), is allowed.
- To illegalize a Mode Code, you need to illegalize both the receive and transmit version.
- Illegalization of row 1F (H) is not automatic.

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5 Bus Monitor Operation

Chapter 5 describes EXC-1553PCMCIA operation in Bus Monitor mode. The following topics are covered:

- "Bus Monitor Message Processing," page 5-1
- "Control Registers—BM Mode," page 5-2
- "Bus Monitor Architecture," page 5-9
- "Bus Monitor Block Chaining," page 5-12
- "Memory Architecture," page 5-13
- "RT/Concurrent Monitor Operation," page 5-13
- "MIL-STD-1553A Operation—BM Mode," page 5-15

5.1 Bus Monitor Message Processing

To process messages, the EXC-1553PCMCIA uses data supplied in the control registers along with SRAM. The EXC-1553PCMCIA uses seven 16-bit memory locations for each message called a monitor block. The monitor block is updated at the end of command processing. The following paragraphs discuss the command block in detail.

You can allocate memory spaces for each monitor block. The top of the monitor blocks can reside at any address location. The control registers are initialized by the host and linked to the Monitor Block via the Initial Monitor Block Pointer Register and the Monitor Block Counter Register contents. Each monitor block contains a Message Information Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, and Time-Tag.

The Message Information word allows the EXC-1553PCMCIA to inform you on which bus the command was received, whether the message was an RT-RT transfer, and conditions associated with the message. The EXC-1553PCMCIA also stores each command word associated with the message in the appropriate location. For normal 1553 commands, only the first command word location will contain data. For RT-RT commands, the second command word location will contain data, and bit 08 in the Message Information word will be set.

For each command, the Data Pointer is read to determine where to store data words. The EXC-1553PCMCIA stores data sequentially from the top memory location. The EXC-1553PCMCIA also stores each status word associated with the message in the appropriate location. For normal 1553 commands, only the first status word location will contain data. For RT-RT commands, the second status word location will contain data.

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The EXC-1553PCMCIA begins monitoring after Setup Register bit 15 = 1 (i.e., assertion of TERACT and STEX). After reception, the EXC-1553PCMCIA begins post-processing. Command post-processing involves storing data to memory. An optional interrupt log entry is performed after a monitor is entered. Monitor Time-Out:

- MIL-STD-1553A = 11 usec.
- MIL-STD-1553B = 15 usec.

5.2 Control Registers—BM Mode

The control registers are read/write unless otherwise stated. All control registers **must** be accessed in word mode. All control register bits are active high and are reset to 0 unless otherwise stated.

Figure 5-1 below illustrates the control registers for Bus Monitor mode.

Reserved	40020-4003F H
Monitor Filter Register Lo	4001E H
Monitor Filter Register Hi	4001C H
Monitor Block Counter Register	4001A H
Initial Monitor Data Pointer Register	40018 H
Initial Monitor Command Block Pointer Register	40016 H
Reserved	40010-40014 H
Time Tag Register	4000E H
BIT Word Register	4000C H
Interrupt Log List Pointer Register	4000A H
Pending Interrupt Register	40008 H
Interrupt Mask Register	40006 H
Current Command Block Register	40004 H
Operational Status Register	40002 H
Setup Register	40000 H

Figure 5-1. Control Registers—BM Mode

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5.2.1 Setup Register

Address: 40000 (H)

To operate the EXC-1553PCMCIA as a bus monitor, use the following bits. To make changes to the Monitor and to this register, the STEX bit (Bit 15) must be logic zero.

Bit	Bit Name	Description
15	STEX	Start Execution. 1 = Initiates RT Mode operation. 0 = Inhibits EXC-1553PCMCIA operation. After execution has begun, a write of a logic zero will halt the EXC-1553PCMCIA after completing the current 1553 message.
14	SBIT	Start BIT. 1 = Places the card into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. The host must halt the card in order to place it into the Built-In Test mode (STEX = 0). Note: If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
13	SRST	Software Reset. 1 = Performs a software reset. The configuration registers are not affected when this bit is asserted. The software reset takes 6 usec. to execute. The software reset clears all internal logic, just as an external reset does. SRST will only function after READYB is asserted.
06-12	Reserved	Set to 0
05	MTC	Monitor Control. This bit determines whether the EXC-1553PCMCIA will monitor all RTs or selected RTs. 1 = The EXC-1553PCMCIA will monitor only the RTs as specified in the Monitor Filter Registers. 0 = The EXC-1553PCMCIA will monitor all RTs.
04	BCEN	Broadcast Enable. 1 = Enables the broadcast option for RT Mode. 0 = Enables remote terminal address 31 as a unique remote terminal address.
02-03	Reserved	Set to 0
01	INTEN	Interrupt Log Enable. 1 = Enables the interrupt logging feature. 0 = Prevents the logging of interrupts.
00	Reserved	Set to 0

Setup Register

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5.2.2 Operational Status Register — Address: 40002 (H)

The Operational Status register reflects pertinent status information for the EXC-1553PCMCIA and is reset to ED82 (H) on reset.

NOTE To make changes to the Monitor and to this register, the STEX bit (Setup Register, bit 15) must be logic zero.

Bit	Bit Name	Description
10-15	Reserved	Set to 0
09	MSEL1	Mode Select 1. In conjunction with Mode Select 0, this bit determines the EXC-1553PCMCIA mode of operation.
08	MSEL0	Mode Select 0. In conjunction with Mode Select 1, this bit determines the EXC-1553PCMCIA mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC Mode
0	1	RT Mode
1	0	Bus Monitor Mode
1	1	RT/ Concurrent Monitor Mode

07	A/B STD	Military Standard 1553A or 1553B Standard. This bit determines whether the EXC-1553PCMCIA will look for the RT's response in 7 usec. (MIL-STD-1553A) or in 12 usec. (MIL-STD-1553B). 1 = Forces the EXC-1553PCMCIA to declare a time-out error condition if the RT has not responded in 7 usec. 0 = Allows the EXC-1553PCMCIA to declare a time-out error condition if the RT has not responded in 12 usec.
04-06	Reserved	These read-only bits are 0.
03	EX	EXC-1553PCMCIA Executing. This read-only bit indicates whether the EXC-1553PCMCIA is presently executing or whether it is idle. 1 = The EXC-1553PCMCIA is executing. 0 = The EXC-1553PCMCIA is idle.
02	Reserved	Set to 0
01	READY	Ready. This read-only bit indicates that the EXC-1553PCMCIA has completed initialization or that the SUMMIT chip has completed BIT, and is cleared on reset.
00	TERACT	Teract. Read-only. 1 = The EXC-1553PCMCIA is presently processing a message.

Operational Status Register

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5.2.3 Current Command Register — Address: 40004 (H) READ ONLY

The Current Command register contains the last valid command that was transmitted over the 1553 bus. In an RT-RT transfer, this register will update as each of the two commands are received by the Bus Monitor.

Bit	Bit Name	Description
00-15	CC[15-0]	Current Command. These bits contain the latest 1553 word that was received by the EXC-1553PCMCIA.

Current Command Register

5.2.4 Interrupt Mask Register — Address: 40006 (H)

The EXC-1553PCMCIA interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked if the corresponding bit of this register is set to logic zero.

Bit	Bit Name	Description
15	DMAF	DMA Fail Interrupt
13-14	Reserved	Set to 0
12	BITF	BIT Fail Interrupt
11	MERR	Message Error Interrupt
01-10	Reserved	Set to 0
00	MBC	Monitor Block Counter Interrupt

Interrupt Mask Register

5.2.5 Pending Interrupt Register — Address: 40008 (H) READ ONLY

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. Note that all register bits are cleared on a host read.

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Bit	Bit Name	Description
15	DMAF	DMA Fail Interrupt. Indicates that a memory access failed. Once the SUMMIT chip has initiated a memory access, an internal timer is started. If the memory access has not been completed by the time the timer decrements to zero, an interrupt is generated (if not masked), current command processing will end, and the EXC-1553PCMCIA will remain on-line.
13-14	Reserved	Ignore on read.
12	BITF	BIT Fail Interrupt. 1 = A BIT failure. Interrogate Bit Word Register bits 11 and 10 to determine the specific channel that failed. An interrupt is generated, operation continues.
11	MERR	Message Error Interrupt. 1 = A message error occurred. The Monitor can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated after message processing is complete.
01-10	Reserved	Ignore on read.
00	MBC	Monitor Block Counter Interrupt. This bit is set if the EXC-1553PCMCIA's monitor block counter reaches zero (transition from 1 to 0). Note: The Monitor does not discriminate between error-free messages and those messages with errors. An interrupt is generated.

Pending Interrupt Register

5.2.6 Interrupt Log List Pointer Register — Address: 4000A (H)

The Interrupt Log List Pointer register indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts. The EXC-1553PCMCIA architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K word memory space. Initialize the lower five-bits of this register to a logic zero. The SUMMIT chip controls the lower five-bits to implement the ring-buffer architecture. This register is read to determine the location and number of interrupts within the Interrupt Log List (least significant five-bits).

Bit	Bit Name	Description
00-15	INT[15-0]	Interrupt Log List Pointer Bits. These bits indicate the starting location of the Interrupt Log List.

Interrupt Log List Pointer Register

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5.2.7 BIT Word Register — Address: 4000C (H)

The BIT Word register contains information on the current status of the EXC-1553PCMCIA.

Bit	Bit Name	Description
15	DMAF	DMA Fail. This bit is set if a memory access has not been completed within 7 usec.
13-14	Reserved	Ignore on read.
12	BITF	BIT Fail. 1 = A BIT failure. Interrogate bits 11 and 10 to determine the specific channel that failed.
11	CHAF	Channel A Fail. 1 = A BIT test failure in Channel A.
10	CHBF	Channel B Fail. 1 = A BIT test failure in Channel B.
00-09	Reserved	Ignore on read.

BIT Word Register

5.2.8 Time-Tag Register — Address: 4000E (H)

The Time-Tag register reflects the state of a 16-bit free running ring counter in the RT and Bus Monitor modes. This counter will remain a free running counter as long as the device is not in a reset or software reset mode. The resolution of this counter is 64 usec./bit. The Time-Tag counter begins operation on the falling (final) edge of the reset pulse.

Bit	Bit Name	Description
00-15	TT[15-0]	Time-Tag Counter Bits. These bits indicate the state of the 16-bit internal counter.

Time-Tag Register

5.2.9 Initial Monitor Block Pointer Register — Address: 40016 (H)

The Initial Monitor Block Pointer register contains the starting location of the Monitor Blocks.

NOTE It is recommended that this register not be changed while the EXC-1553PCMCIA is active (i.e., Operational Status Register, bit 03 = 1).

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Bit	Bit Name	Description
00-15	MBA[15-0]	Initial Monitor Block Address. These bits indicate the starting location of the Monitor Block.

Initial Monitor Block Pointer Register

5.2.10 Initial Monitor Data Pointer Register — Address: 40018 (H)

The Initial Monitor Data Pointer register contains the starting location of the Monitor Data.

NOTE It is recommended that this register not be changed while the EXC-1553PCMCIA is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	MDA[15-0]	Initial Monitor Data Address. These bits indicate the starting location of the Monitor Data.

Initial Monitor Data Pointer Register

5.2.11 Monitor Block Counter Register — Address: 4001A (H)

The Monitor Block Counter register contains the number of Monitor Blocks you want to log. After execution begins, this register automatically decrements as commands are logged. When this register is decremented from one to zero, an interrupt will be generated, if enabled. The EXC-1553PCMCIA will start over at the initial pointers as identified in the Initial Monitor Block Pointer Register and the Initial Monitor Data Pointer Register.

NOTE It is recommended that this register not be changed while the EXC-1553PCMCIA is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	MBC[15-0]	Monitor Block Count. These bits indicate the number of Monitor Blocks to log.

Monitor Block Counter Register

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5.2.12 Monitor Filter Register Hi — Address: 4001C (H)

The Monitor Filter register determines which RTs (RT 31 through RT 16) the EXC-1553PCMCIA will monitor.

Bit	Bit Name	Description
00-15	MF[31-16]	Monitor Filter. These bits determine which RT to monitor.

Monitor Filter Register Hi

5.2.13 Monitor Filter Register Lo — Address: 4001E (H)

The Monitor Filter register determines which RTs (RT 15 through RT 0) the EXC-1553PCMCIA will monitor.

Bit	Bit Name	Description
00-15	MF[15-0]	Monitor Filter. These bits determine which RT to monitor.

Monitor Filter Register Lo

5.3 Bus Monitor Architecture

To meet the MIL-STD-1553 monitor requirements, the EXC-1553PCMCIA uses a Monitor Block architecture similar to the BC Command Block architecture, which takes advantage of both control registers and RAM. The Monitor Block, which is located in contiguous memory, requires eight 16-bit locations for each message.

These eight locations include:

- A message information word
- Two command word locations
- A data pointer
- Two status word locations
- A time-tag location
- An unused location

You must initialize the starting locations of the Monitor Block, the Data Pointer, the Block Counter, and the Interrupt Log Pointer. From then on, the EXC-1553PCMCIA will build a Monitor Block for each message it receives over the 1553 bus. Figure 5-2 shows a diagram of the Monitor Block followed by a description of each location associated with the Monitor Block.

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Message Info Word
Command Word 1
Command Word 2
Data Pointer
Status Word 1
Status Word 2
Time Tag
Unused

Figure 5-2. Monitor Block Diagram

The first memory location of each Monitor Block contains the message information word. Each information word contains the opcode, retry number, bus definition, RT-RT messages, and the message information.

15 12	11 10	09	08	07 00
0 1 0 0	0 0	CHA/B	RT-RT	Message Information

Figure 5-3. Message Information Word

Bit Number	Description
12-15	Default. With the Monitor Block architecture resembling the BC Command Block architecture, these bits default to a "0100" state (which is the Execute and Continue opcode) in case the monitor must switch to the BC mode of operation.
10-11	Default. With the Monitor Block architecture resembling the BC, these bits default to a "00" state. If the monitor must switch to the BC, the retries will be set at four per message.
09	Channel A/B. This bit defines on which of the two buses the command was received. (Logic 1 = Bus A, Logic 0 = Bus B).
08	RT-RT Transfer. This bit defines whether or not the message associated with this Monitor Block was an RT-RT transfer and whether the EXC-1553PCMCIA saved the second command word. This bit will be set only if the EXC-1553PCMCIA is instructed to monitor the Receive RT.
00-07	Message Information Bits. These bits define the conditions of the message received by the EXC-1553PCMCIA for that particular Monitor Block. Each of the message information bits is defined in the following section.

Message Information Word

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MESSAGE INFORMATION BITS

Message information bits are provided as a means to supply more data on the message. In an RT-RT transfer, the information applies to both of the status words. Each message information bit is defined below.

Bit Number	Description
07	Message Error. This bit will be set if the monitor detects an error in either the command word, data words, or the RT's status.
06	Mode Code without Data. This bit will be set if the monitor detects that the command being processed is a mode code without data words.
05	Broadcast. This bit will be set if the monitor detects that the command being processed is a broadcast message.
04	Reserved
03	Time-Out Error. This bit will be set if the RT did not receive the proper number of data words, e.g., the number of data words received was less than the word count specified in the command word.
02	Overrun Error. This bit will be set if the RT received a word when none were expected or the number of data words received was greater than expected.
01	Parity Error. This bit will be set if a parity error has occurred on the data words or the RT's status word.
00	Manchester Error. This bit will be set if a Manchester error has occurred on either the data words or the RT's status word.

Message Information Bits

5.3.1 Command Words

The next two locations in the EXC-1553PCMCIA Monitor Block are for command words. In non-RT-RT 1553 messages, only the first command word will be stored. However, in an RT-RT transfer, the first command word is the Receive Command and the second command word is the Transmit Command.

5.3.2 Data Pointer

The fourth location in the Monitor Block is the data pointer. This pointer points to the first memory location to store the data words associated with the message for this block. Note that the data associated with each individual message will be stored contiguously. This data structure allows the EXC-1553PCMCIA to store the specified number of data words.

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NOTE In an RT-RT transfer, the EXC-1553PCMCIA uses the data pointer as the location in memory to store the transmitting data in the transfer.

5.3.3 Status Words

The next two locations in the Monitor Block are for status words. As the RT responds to the BC's command, the corresponding status word will be stored in Status Word 1. However, in an RT-RT transfer, the first status word will be the status of the Transmitting RT while the second status word will be the status of the Receiving RT.

5.3.4 Time-Tag

The seventh location in the Monitor Block is the time-tag associated with the message. The time-tag is stored into this location at the end of message processing (i.e., captured after the command is validated).

5.3.5 Reserved

The last location in the EXC-1553PCMCIA Monitor Block is reserved.

5.4 Bus Monitor Block Chaining

The host determines the first Monitor Block by setting the start address in the Initial Monitor Block Pointer Register. Figure 5-4 shows the Monitor Block as the blocks execute in a contiguous fashion.

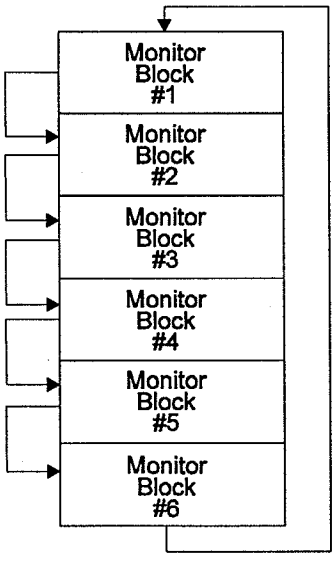


Figure 5-4. Bus Monitor Block Structuring

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5.5 Memory Architecture

The configuration shows the Monitor Blocks, data locations, and the Interrupt Log List as separate entities. Figure 5-5 shows that the first block of memory is allocated for the Monitor Blocks. Notice that the Initial Monitor Block Pointer Register points to the initial Monitor Block location, the Initial Monitor Data Pointer Register points to the initial Data location, Interrupt Log List Pointer Register points to the Interrupt Log, and the Monitor Block Counter Register contains the Monitor Block count. After execution begins, the EXC-1553PCMCIA will build command blocks and store data words until the count reaches zero. When the count reaches zero, the EXC-1553PCMCIA will simply wrap back to the initial values and start again.

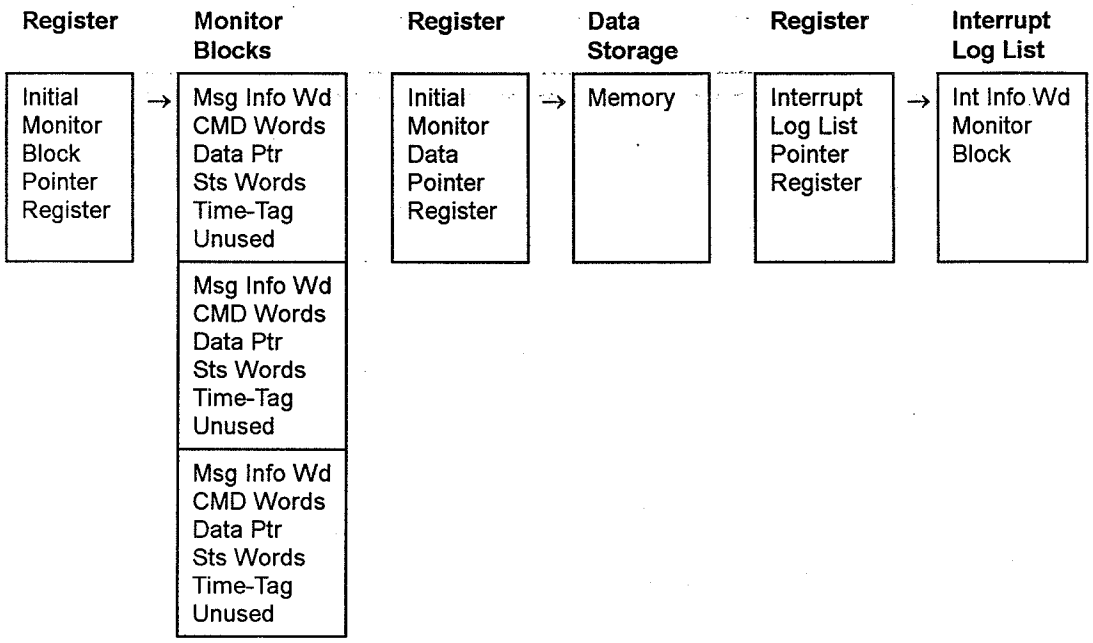


Figure 5-5. Memory Architecture for Bus Monitor Mode

5.6 RT/Concurrent Monitor Operation

For applications that require simultaneous Remote Terminal and Bus Monitor operation, the EXC-1553PCMCIA should be configured as both a remote terminal and bus monitor. This feature allows the EXC-1553PCMCIA to communicate on the bus for one specific address and to monitor the bus for other specific addresses. Configuration as both Bus Monitor and RT precludes the EXC-1553PCMCIA from monitoring its own remote terminal address.

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When the EXC-1553PCMCIA is configured as both RT and Bus Monitor, the RT has priority over the Bus Monitor. For example, commands to the RT will always take priority over commands for the Bus Monitor. The examples below describe what happens if the RT is defined for terminal address 1 and the Bus Monitor is to monitor terminal address 12.

Example 1:

Bus A	CMD/TA = 12
Bus B	CMD/TA = 1

In this example, the Bus Monitor will decode the first command on bus A, realize the message is for terminal address 12, and start monitoring the message. However, as soon as the EXC-1553PCMCIA realizes the second command on bus B is to terminal address 1, the RT will take priority and begin RT message processing.

Example 2:

Bus A	CMD/TA = 1
Bus B	CMD/TA = 12

In Example 2, the RT will decode the first command on bus A, realize the message is for terminal address 1, and start message processing. As the message on bus B is received, the EXC-1553PCMCIA will realize it is to terminal address 12, but since the RT has priority the Bus Monitor will not switch to the bus monitor mode.

The above examples also apply to an RT-RT message. For example, if the first command in an RT-RT transfer matches the terminal address of the EXC-1553PCMCIA, the entire message will be stored (Message 1). However, if the first command in an RT-RT transfer matches the terminal address of the Bus Monitor and the second command matches the terminal address of the RT, the RT will take priority and only the RT message is stored (Message 2). Below is an RT-RT message example.

Message 1	CMD/TA = 1	CMD/TA = 12
Message 2	CMD/TA = 12	CMD/TA = 1

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5.7 MIL-STD-1553A Operation—BM Mode

The EXC-1553PCMCIA be configured to meet the MIL-STD-1553A protocol.

A/B STD	RESULT
0	1553B response, 1553B Standard
1	1553A response, 1553A Standard

Table 5-1. MIL-STD-1553A Operation—BM Mode

When configured as a MIL-STD-1553A bus monitor, the EXC-1553PCMCIA will operate as follows:

- Looks for the RT response within 11 usec.
- Ignores the T/R bit for all mode codes.
- Defines all mode codes without data.
- Defines subaddress 00000 as a mode code.

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6 Interrupt Architecture

Chapter 6 describes the interrupt architecture of the EXC-1553PCMCIA. The following topics are discussed:

- "Overview," page 6-1
- "Interrupt Identification Word," page 6-1
- "Interrupt Address Word," page 6-2

6.1 Overview

The EXC-1553PCMCIA interrupt architecture involves two control registers, an Interrupt Log List, and the interrupt output. The two control registers are the Interrupt Mask Register and the Pending Interrupt Register. The Interrupt Log List is started at the location specified by the Interrupt Log List Pointer Register and is enabled by bit 01 of the Setup Register.

The upper four interrupt bits of the Pending Interrupt Registers and the BIT Word Register must be handled as they occur and are not stored in the Interrupt Log List. If the pending interrupt register is not cleared after the first interrupt, the setting of other interrupt bits will not result in an interrupt pulse.

The lower twelve interrupt bits of the Pending Interrupt Register are entered into the Interrupt Log List, if the Interrupt Log List is enabled.

The EXC-1553PCMCIA interrupt architecture also allows the entry of 16 interrupts into a 32-word (64 byte) ring buffer. The EXC-1553PCMCIA automatically handles the interrupt logging overhead. Each interrupt generates two words of information to help the host perform interrupt processing. The Interrupt Identification Word (IIW) identifies the type(s) of interrupt(s) that occurred. The Interrupt Address Word (IAW) identifies the interrupt source via a 16-bit address. The EXC-1553PCMCIA asserts an interrupt to signal you that an interrupt event occurred.

6.1.1 Interrupt Identification Word (IIW)

The Interrupt Identification Word (IIW) is a 16-bit word identifying the interrupt type. The format is similar to the Pending Interrupt Register. The host reads the IIW to determine which interrupt event occurred. The bit description for the IIW is provided below.

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Bit	Bit Name	Description
12-15	Reserved	Ignore on read
11	MERR	Message Error Interrupt (All modes)
10	SUBAD	Subaddress Accessed Interrupt (RT Mode)
09	BDRCV	Broadcast Command Received Interrupt (RT Mode)
08	IXEQ0	Index Equal Zero Interrupt (RT Mode)
07	ILCMD	Illegal Command Interrupt (RT Mode)
06	Reserved	Set to 0
05	EOL	End Of List (BC Mode)
04	ILLCMD	Illogical Command (BC Mode)
03	ILLOP	Illogical Opcode (BC Mode)
02	RTF	Retry Fail (BC Mode)
01	CBA	Command Block Accessed (BC Mode)
00	MBC	Monitor Block Count Equal Zero (Monitor Mode)

Interrupt Identification Word (IIW)

6.1.2 Interrupt Address Word (IAW)

The Interrupt Address Word (IAW) is a 16-bit word that identifies the interrupt source. Depending on the mode of operation (i.e., RT, BC, or Monitor), the IAW has different meanings. In the RT mode operation, the IAW identifies the subaddress or mode code descriptor that generated the interrupt. For the BC mode of operation, the IAW points to the command block addressed when the interrupt occurred. In the Monitor mode of operation, the IAW marks the monitor counter count when the interrupt occurred. You use the IAW with the Initial Monitor Command Block Pointer Register to determine the monitor command block that generates the interrupt.

When in RT/Concurrent Monitor mode, you must determine if the IAW contains information for the RT or the Monitor. The determination is made by comparing the contents of the IAW base address with the descriptor base address. If a match occurs, then the IAW contains a subaddress or mode code identifier. If no match occurs, the IAW contains monitor counter information.

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6.1.3 Interrupt Log List Address

The interrupt log list resides in a 32-word (64-byte) ring buffer. The host defines the location buffer, within the memory space, via the Interrupt Log List Register. Restrict the ring buffer address to a 32-word boundary.

During initialization you will write a value to the Interrupt Log List Pointer Register. Initialize the least significant five-bits to a logic zero. The most significant 11 bits determine the base address of the buffer. The EXC-1553PCMCIA increments the ring buffer pointer on the occurrence of the first interrupt, storing the IIW and IAW at locations 00000 and 00001 respectively. The EXC-1553PCMCIA logs ensuing interrupts sequentially into the ring buffer until interrupt number 16 occurs. The EXC-1553PCMCIA enters interrupt 16's IIW in buffer location 11110 and the IAW at location 11111.

The EXC-1553PCMCIA increments the ring buffer pointer as interrupts occur. The least significant five-bits of the Interrupt Log List Pointer Register reflect the ring buffer pointer value. Figure 6-1 shows the ring buffer architecture.

You can read the ring buffer pointer value to determine the number of interrupts that have occurred. By extracting the least significant five bits from the Interrupt Log List Register and logical shifting the data once to the right, you can determine the number of interrupt events.

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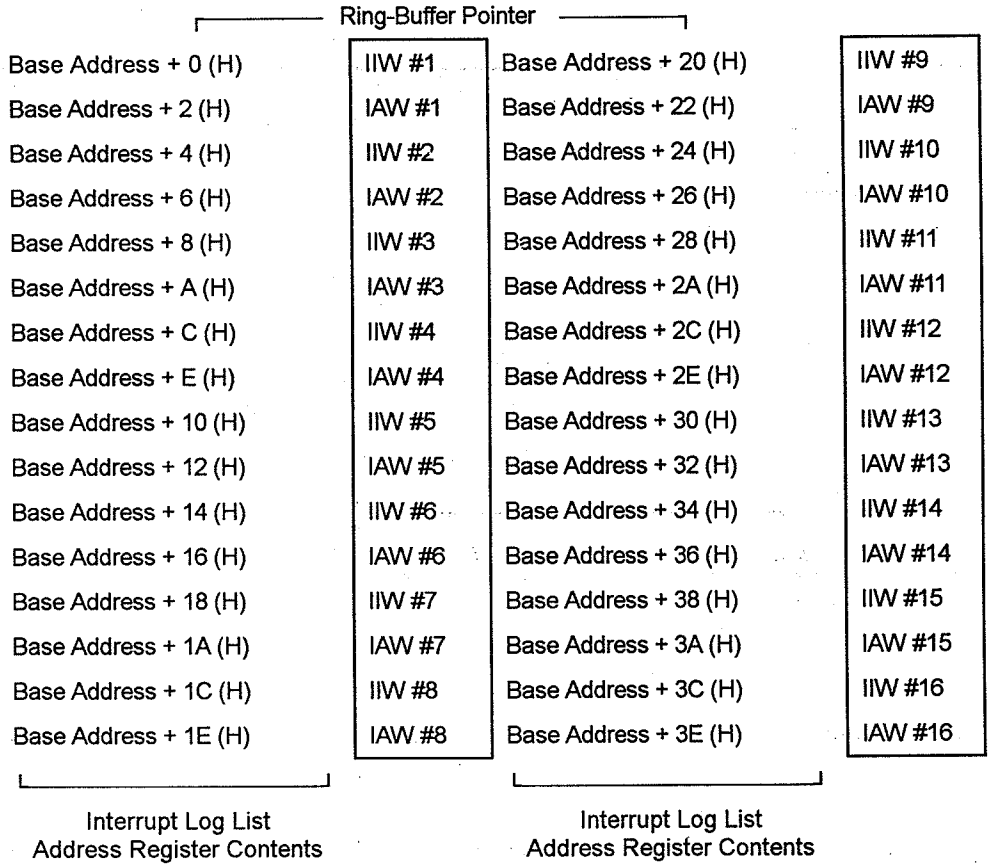


Table 6-1. Interrupt Ring Buffer

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7 Switching Modes of Operation

Many test applications utilizing the EXC-1553PCMCIA simulate only one operation mode, i.e., Bus Controller. For these applications, the information in this chapter is not relevant.

If your application requires simulation of more than one mode, you can switch from one mode of operation to another, i.e., between the Bus Controller and Remote Terminal modes.

To switch between modes of operation:

1. Halt the operation of the board (via the STEX bit in the Setup register).
2. Modify the control registers to the desired mode.
3. Set up the memory as required.
4. Set the STEX bit in the Setup register.

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8 Mechanical and Electrical Specifications

Chapter 8 describes the mechanical and electrical specifications of the EXC-1553PCMCIA board. The following topics are discussed:

- "Connectors," page 8-1
- "Mechanical Outline," page 8-3
- "Power Requirements," page 8-4

8.1 Connectors

The EXC-1553PCMCIA contains two connectors:

- 25-Pin MIL-STD-1553 I/O Bus Connector
- 68-Pin PCMCIA Bus Connector

NOTE Each card is shipped with one twinax adapter cable. For custom cable/coupling requirements, Excalibur Systems, Inc. carries a complete line of data bus products. Contact us for detailed ordering information.

The EXC-1553PCMCIA-R option has Bus A and B twinax cables soldered directly on to the PCMCIA PCB, exiting the card in the same location as the original 25-pin connector. The cables are "strain relieved" so that no force can be applied to the cable/PCB solder connections. In addition, the cable connections are hermetically sealed with epoxy potting compound, making the card and cable one inseparable entity.

8.1.1 25-Pin MIL-STD-1553 I/O Bus Connector Pinout

Pin	Signal
1	GROUND
2	NC
3	Reserved
4	NC
5	BUS B HI (DIRECT MODE)
6	BUS B LO (DIRECT MODE)
7	NC
8	NC
9	BUS B HI (TXFRMR MODE)
10	BUS B LO (TXFRMR MODE)
11	NC
12	NC
13	NC

Pin	Signal
14	NC
15	NC
16	BUS A HI (DIRECT MODE)
17	BUS A LO (DIRECT MODE)
18	NC
19	NC
20	BUS A HI (TXFRMR MODE)
21	BUS A LO (TXFRMR MODE)
22	NC
23	Reserved
24	NC
25	GROUND

NOTE: NC = Not Connected and reserved for future use

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8.1.2 68-Pin PCMCIA Bus Connector Pinout

Pin	Signal	Pin	Signal
1	GND	35	GND
2	D3	36	GND
3	D4	37	D11
4	D5	38	D12
5	D6	39	D13
6	D7	40	D14
7	CE1#	41	D15
8	A10	42	CE2#
9	OE#	43	NC
10	A11	44	NC
11	A9	45	NC
12	A8	46	NC
13	A13	47	NC
14	A14	48	NC
15	WE#	49	NC
16	IREQ#	50	NC
17	VCC	51	VCC
18	NC	52	NC
19	A16	53	NC
20	A15	54	NC
21	A12	55	NC
22	A7	56	NC
23	A6	57	NC
24	A5	58	RESET
25	A4	59	WAIT#
26	A3	60	NC
27	A2	61	REG#
28	A1	62	BVD2
29	A0	63	NC
30	D0	64	D8
31	D1	65	D9
32	D2	66	D10
33	GND	67	GND
34	GND	68	GND

NOTE: NC = Not Connected

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8.2 Mechanical Outline

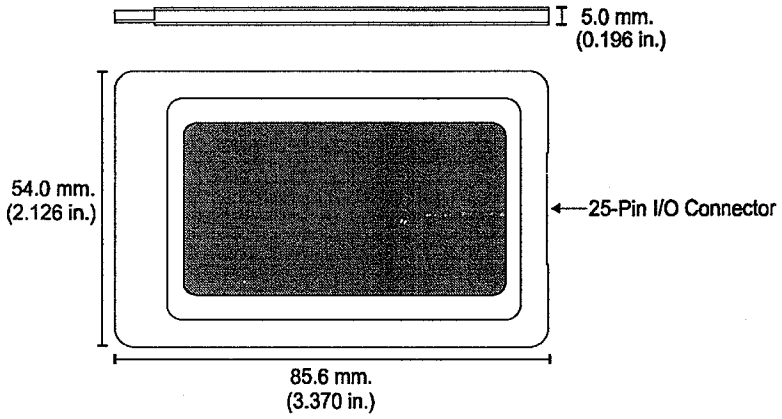


Figure 8-1. Mechanical Outline—EXC-1553PCMCIA Card

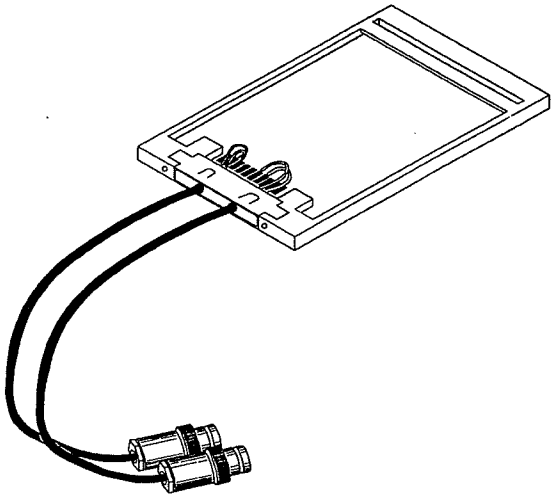


Figure 8-2. EXC-1553PCMCIA-R Card

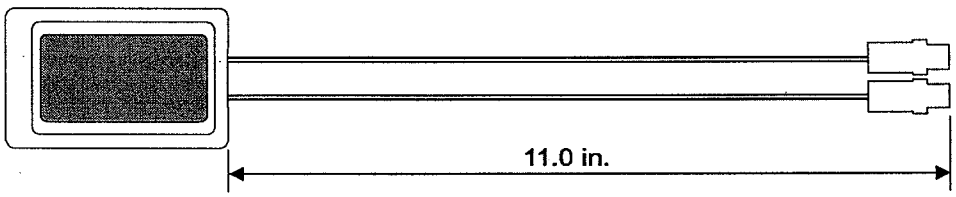


Figure 8-3. Mechanical Outline—EXC-1553PCMCIA-R Card

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8.3 Power Requirements

Power requirements for the EXC-1553PCMCIA card are listed in the following table. All values are typical.

	75% Duty Cycle	0% Duty Cycle (Standby)	Power Down Mode (Software)
EXC-1553PCMCIA	560 mA	165 mA	0 mA

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9 Ordering Information

Chapter 9 describes the part numbers you must indicate when ordering an EXC-1553PCMCIA or EXC-1553PCMCIA-R card.

PART NUMBER	DESCRIPTION
EXC-1553PCMCIA/B	PCMCIA Type II MIL-STD-1553 interface card for PCMCIA-compatible notebook computers. Supports BC, RT, BM and RT/Concurrent Monitor modes. Plug and Play compatible.
EXC-1553PCMCIA/B-R	As above, with ruggedized hardwired cable connection.
EXC-1553PCMCIA/B-E	As above, with extended temperature (–40° to +85° C) operation.
EXC-1553PCMCIA/B-R-E	As above, with ruggedized hardwired cable connection and extended temperature (–40° to +85° C) operation.
C2002	Adapter cable assembly for transformer coupled mode (standard mode). Supplied with the EXC-1553PCMCIA card.
C2004	Cable for direct coupled mode. Optional.

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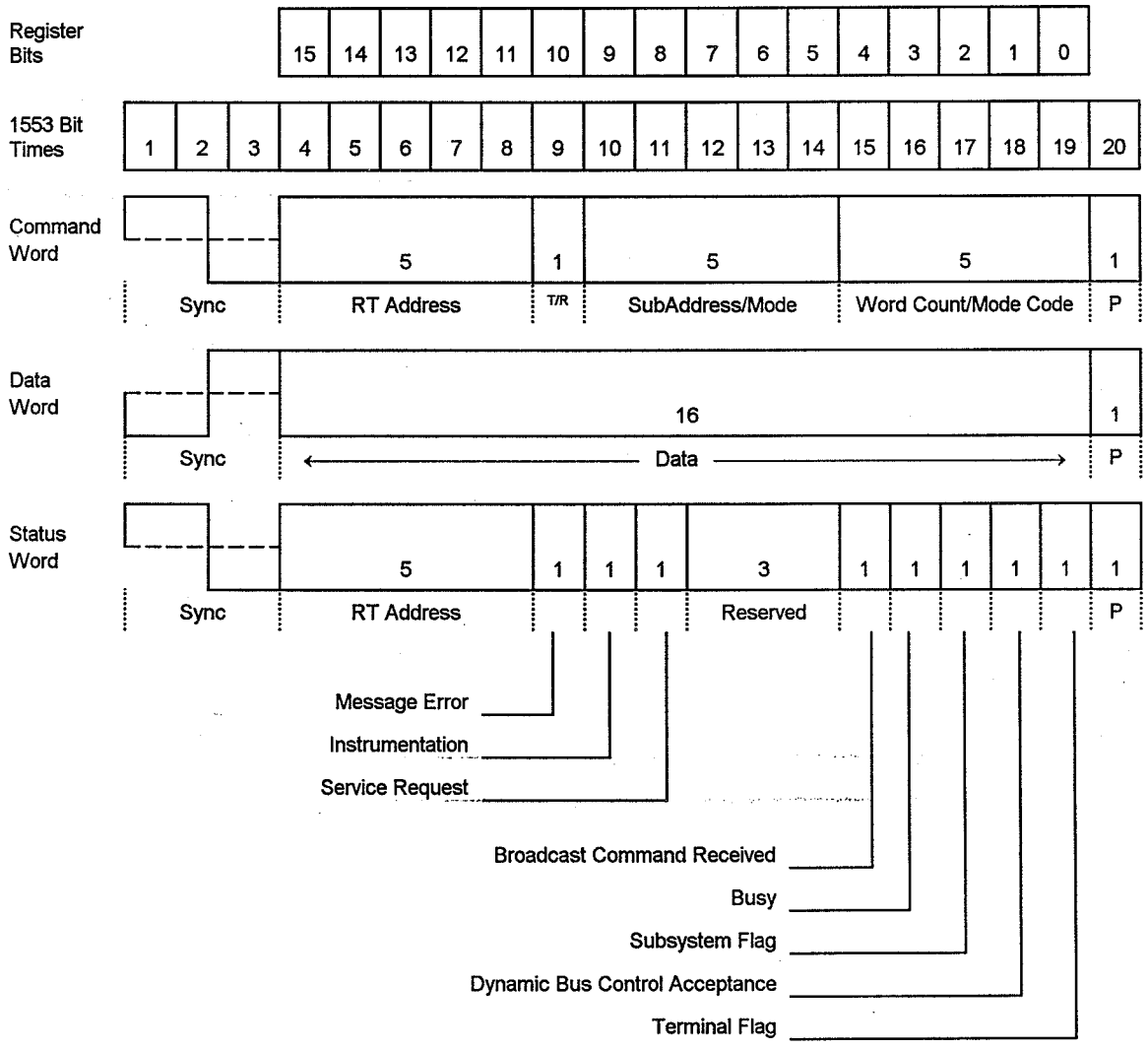
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10 Appendices

Chapter 10 contains appendices describing the Military Standard 1553B word and message formats. The following topics are included:

- "MIL-STD-1553B Word Formats," page 10-1
- "MIL-STD-1553B Message Formats," page 10-2

Appendix A MIL-STD-1553B Word Formats

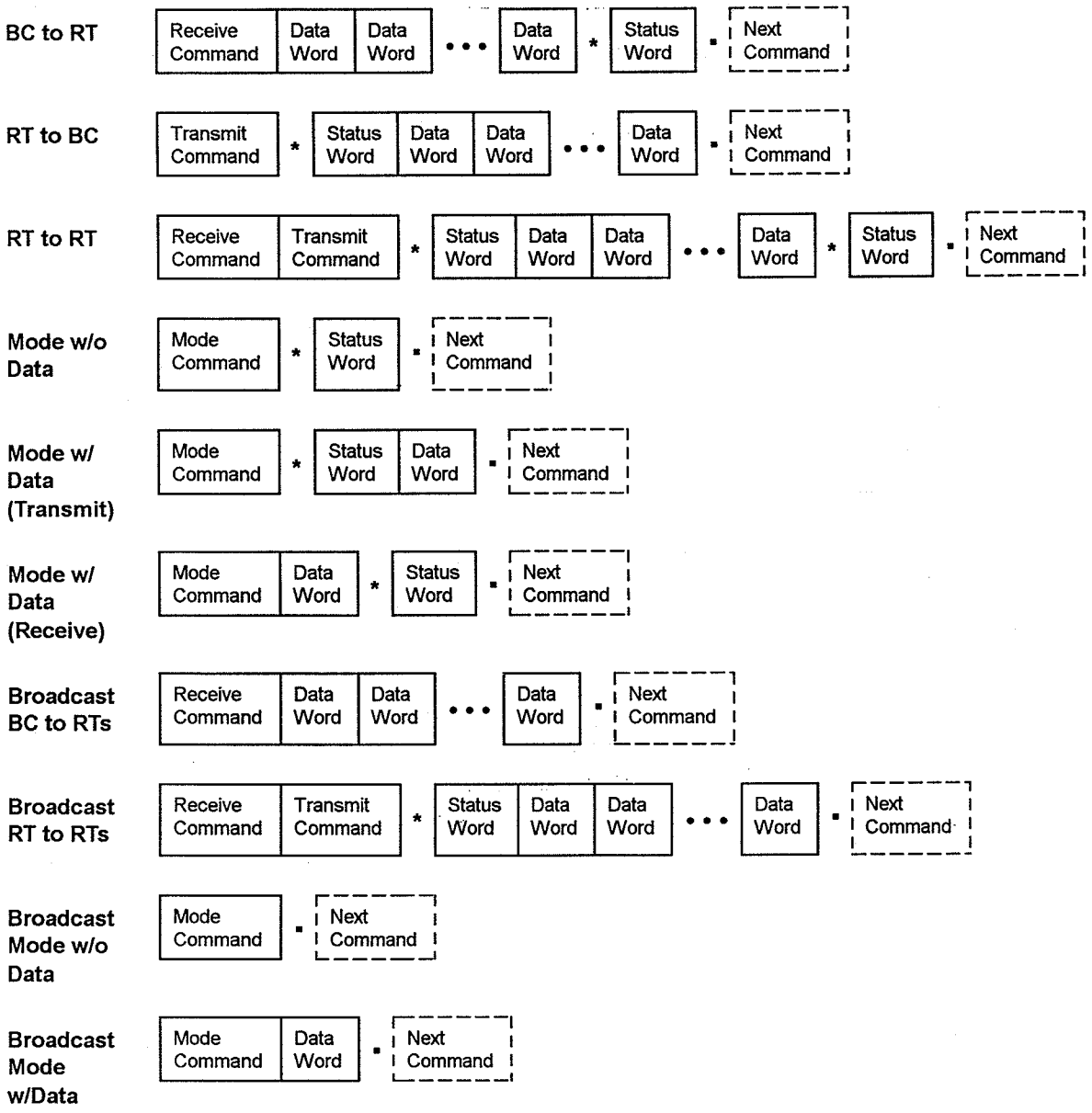


NOTE: T/R = Transmit/Receive
P = Parity

Figure 10-1. MIL-STD-1553B Word Formats

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Appendix B MIL-STD-1553B Message Formats



NOTE: * = Response time
▪ = Intermessage gap

Figure 10-2. MIL-STD-1553B Message Formats

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