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EXC-1553PCI/EP

MIL-STD-1553
Test and Simulation Board
for PC Compatible Computers

User's Manual

EXCALIBUR SYSTEMS

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What is in this manual?

This manual is divided into the following nine chapters:

Chapter 1, "**Introduction**" provides an overview of the EXC-1553PCI/EP card, and discusses card installation, 1553 bus connections, memory structure, the PCI configuration space header, PCI header space registers and PCI global interrupt control registers.

Chapter 2, "**Bus Controller Operation**" describes the Bus Controller memory map, instruction stack, message block formats, and continuous or one-shot message transfers. It also includes a program example from Bus Controller mode and the control register definitions.

Chapter 3, "**Remote Terminal Operation**" describes the Remote Terminal memory map, data block look-up table, active RT table, 1553 RT status words, message stack, RT last command words, 1553 RT BIT words, 1553 RT vector words, alter table, mode codes, broadcast mode, and error injection features. It also includes a program example from Remote Terminal mode and the control register definitions.

Chapter 4, "**BC/Concurrent-RT Operation**" describes the Bus Controller/Concurrent-RT memory map, instruction stack, remote terminal simulation, message block formats, and continuous or one-shot message transfers. It also includes a program example from BC/Concurrent-RT mode and the control register definitions.

Chapter 5, "**Bus Monitor Operation**" describes the Bus Monitor sequential mode, which includes fixed-block and link-list operation, and look-up table mode. This chapter also discusses the message status word, time tag value, trigger operation, program examples in Bus Monitor mode, and the control register definitions. There is also an explanation of the Concurrent Monitor option, and the differences between Concurrent and Non-Concurrent Monitor operation.

Chapter 6, "**Switching Modes of Operation**" explains switching between the modes of EXC-1553PCI/EP operation.

Chapter 7, "**Mechanical and Electrical Specifications**" presents the EXC-1553PCI/EP board layout, LED indicators, DIP switch settings, connectors and power requirements.

Chapter 8, "**Ordering Information**" presents the part number details required for ordering an EXC-1553PCI/EP card.

Chapter 9, "**Appendices**" provides information on the MIL-STD-1553B word, Military Standard message formats, internal and external loop back tests and customer support.

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1 Introduction

Chapter 1 provides an overview of the EXC-1553PCI/EP avionics communication board. The following topics are covered:

- "Overview," page 1-1
- "Installation," page 1-3
- "1553 Bus Connections," page 1-5
- "Memory Structure," page 1-6
- "PCI Configuration Space Header," page 1-7
- "PCI Header Space Registers," page 1-8
- "PCI Global Interrupt Control Registers," page 1-19

1.1 Overview

The EXC-1553PCI/EP is an intelligent, memory-mapped MIL-STD-1553 interface card which operates within host computers equipped with the PCI Local Bus. This card provides a total solution for developing and testing 1553 interfaces and for performing system simulation of the MIL-STD-1553 bus. The EXC-1553PCI/EP card contains an 18k × 8 (true dual-ported) RAM for data blocks, control registers, and look-up tables. This card gives you direct access to all control registers and data blocks; you can modify various parameters and data in real time. Operation of the card is controlled by accessing the memory-mapped control registers.

The concurrent 1553 Monitor has an additional 18k × 8 true dual-port RAM dedicated to the Monitor function. The EXC-1553PCI/EP comes complete with menu-driven software, a C-driver software library including source code, and 1553 adapter cables.

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EXC-1553PCI/EP Board Features:

- Operates as BC, RT, BC/Concurrent-RT or Monitor
- Compatible with PCI local bus
- Handles 4µsec. intermessage gap times in all modes
- Loopback Mode facilitates 1553 cable testing
- Real-time operation
- Multiple protocol capability (i.e. 1553A, B, F-16, McAir)
- Multiple-RT simulation (up to 32 remote terminals)
- Programmable broadcast mode
- Multi-mode triggerable monitor
- Variable amplitude (McAir/1553-compatible) transceiver (standard feature)
- Hardware Time Tag circuit for use in RT and monitor modes
  - RT mode has 16-bit time tag
  - Monitor mode has a 16-bit or 32-bit (user-selectable) time tag value
- Time tag counter can be read by the host in real time
- Concurrent Bus Monitor
- Optional Independent Concurrent Bus Monitor: allows concurrent monitoring of an independent, dual-redundant, 1553 channel
- Error injection capability:
  - Bit count
  - Word count
  - Incorrect sync.
  - Parity
  - Incorrect RT address
  - Non-contiguous data
- Data Integrity value
- Minor Frame operation
- Asynchronous Frame operation

The EXC-1553PCI/EP offers a wide range of options that can be used for various 1553 applications. Although the EXC-1553PCI/EP is very flexible, its memory-mapped board and easy-to-use features eliminate the need for complicated software and shorten development time. The EXC-1553PCI/EP options are activated and programmed via control registers described in this manual.

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Examples of user selectable parameters are as follows:

- You can select whether an RT will return a status word in the event a message containing a data word error is received by the RT.
- Selectable broadcast mode
- Variable response time
- Variable transmit amplitude
- Select mode code subaddress (00000, 11111, or both)
- 1553A RT timing
- You can define each bit in the 1553 Status word

The board has four modes of operation:

- Bus Controller (BC) mode
- Multiple Remote Terminal (RT) mode (up to 32 RTs)
- BC with Concurrent RT operation (up to 32 RTs)
- Triggerable Monitor mode

The EXC-1553PCI/EP board can be ordered in three basic variations:

- Half-size card without a concurrent bus monitor
- Three-quarter size card with a concurrent bus monitor
- Three-quarter size card with an independent, concurrent bus monitor

See “Ordering Information,” page 8-1 for the exact part numbers.

1.2 Installation

EXC-1553PCI/EP installation includes installing the software for each system and installing the board.

1.2.1 Software Installation

The EXC-1553PCI/EP is delivered with software compatible with several operating systems. For information about installing the accompanying software drivers, see **ReadMe.txt** on the *Galahad Software Tools* diskettes that came with your board.

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1.2.2 Board Installation

The EXC-1553PCI/EP operates as a slave on the PCI bus. Installation of the EXC-1553PCI/EP card is similar to that of all PCI "Local Bus" cards. The EXC-1553PCI/EP complies with the "Plug and Play" specification of the PCI standard, and as such its absolute address is set under software control. A detailed description of the software (drivers and BIOS calls) required for determining the card base address is provided in the EXC-1553PCI/EP(M) Software Drivers Manual.

WARNING *You should wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board.*

To install the EXC-1553PCI/EP, follow the instructions below, in the order given.

1. 1553 devices may be connected to the 1553 bus either directly (direct-coupled) or via a bus-coupling stub (transformer coupled). Use DIP switches SW1, SW2, SW3, and SW4 to set the coupling mode to the 1553 bus(es) (see "DIP Switches," page 7-4).
2. **Make certain the computer power source is disconnected.** Insert the EXC-1553PCI/EP card into any PCI compatible slot (see Figure 1-1).

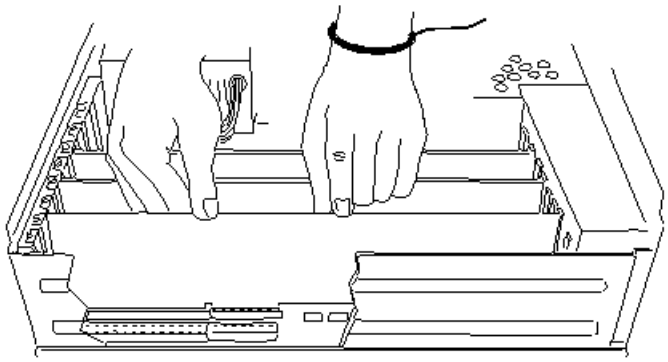


Figure 1-1. Inserting the Excalibur PCI Board

3. Attach the 1553 adapter cables to the board's DB9 connectors and to the bus. The cables may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting over the bus.

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1.3 1553 Bus Connections

For short distances, the EXC-1553PCI/EP may be coupled directly to another 1553 device. To ensure data integrity, you must make certain that the cable connecting the two devices is properly terminated with 78-ohm resistors (see Figure 1-2).

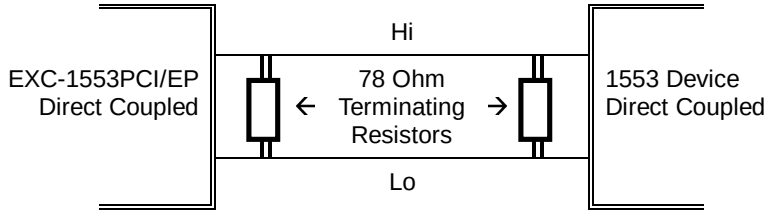


Figure 1-2. Direct Coupled Connection (One Bus Shown)

If you wish to operate in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems, Inc. We supply a three-stub coupler (PN# ESI310) and 78-ohm terminators (PN# ESIT5078). Two terminators are required for each coupler, which services a single bus [e.g. BUS A] (see Figure 1-3).

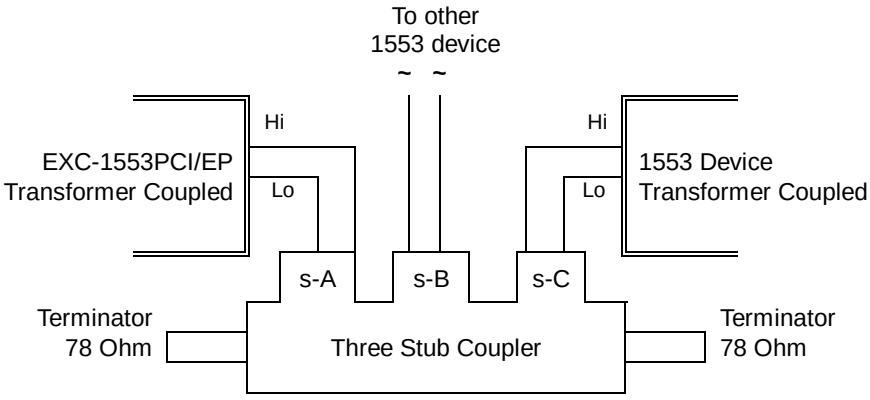


Figure 1-3. Transformer Coupled Connection (One Bus Shown)

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1.4 Memory Structure

There are two distinct areas of memory in the EXC-1553PCI/EP. The first area, the PCI Configuration Space Header Region, is located in a fixed location in host memory and contains all information necessary for the Plug-and-Play operation of the card. The address of this region is fixed in the hardware.

The second area, the Control/Data Region, which contains dual-port RAM and the Control Registers used in setting up the card as a MIL-STD-1553 interface, is divided into three memory Pages (Pages0-2). A Page is a block of memory which has been assigned a unique base address by the Plug-and-Play BIOS. The base address of each Page is determined by the BIOS following power-up and is written into the Base Address Registers 0-2 located in the PCI Configuration Space Header. The memory structure is shown below in Figure 1-4.

PCI Configuration Space Header Region	256 bytes	PCI Bus Plug-and-Play Parameters
Control/Data Region	64 bytes - Page 0	PCI Global Interrupt Control Registers
	16K x 16 - Page 1	BC Mode RT Mode BC/Concurrent RT Mode Monitor Mode
	16K x 16 - Page 2	Concurrent Monitor Mode

Figure 1-4. EXC-1553PCI/EP Memory Structure

NOTE Throughout this manual the terms Page 1 and Channel 1, and Page 2 and Channel 2 will be used interchangeably. Page1/Channel 1 refers to the BC/RT/BC-RT/Monitor channel and Page 2/Channel 2 refers to the optional Concurrent Monitor channel. References to Page 2 should be disregarded for cards supplied without the /EPM(I) option.

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1.5 PCI Configuration Space Header

The EXC-1553PCI/EP includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to setup the Plug-and-Play operation of the card, and set aside system resources.

The PCI Configuration Space Header contents are backed up in on-board non-volatile memory (nvRAM), at the factory. You should not alter the contents of the nvRAM. When you power up, this 'Boot-Load' nvRAM is automatically loaded into the PCI Configuration Space Header.

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0's				38 H
Reserved = 0's				34 H
Expansion ROM Base Address (not used)				30 H
Reserved = 0's				2C H
Reserved = 0's				28 H
Base Address Register #5 (not used)				24 H
Base Address Register #4 (not used)				20 H
Base Address Register #3 (not used)				1C H
Base Address Register #2(Control/Data Region Page 2)				18 H
Base Address Register #1(Control/Data Region Page 1)				14 H
Base Address Register #0 (Control/Data Region Page 0)				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status		Command		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 1-5. PCI Configuration Space Header

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1.6 PCI Header Space Registers

This section describes the registers contained in the PCI Header Space.

1.6.1 Vendor Identification Register (VID) **Address: 00 — 01 (H)**

Power-up value: 10E8 H
Boot-load: External nvRAM offset 040 - 41 H
Attribute: Read Only (RO)
Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group assigned vendor identification number.

Bit	Description
00-15	10E8H

Vendor Identification Register

1.6.2 Device Identification Register (DID) **Address: 02 — 03 (H)**

Power-up value: 0001 H
Boot-load: External nvRAM offset 042 - 43 H
Attribute: Read Only
Size: 16 bits

The Device Identification register contains the vendor-assigned device identification number.

Bit	Description
00-15	0001H

Device Identification Register

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1.6.3 PCI Command Register (PCICMD) Address: 04 — 05 (H)

Power-up value: 0000 H

Boot-load: Not Used

Attribute: Read/Write (R/W on 6 bits, Read Only for all others)

Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s.
09	**Fast Back-to Back Enable**	Always set to 0.
08	**System Error Enable**	When set to 1, this bit permits the PCI Controller to drive the open drain output pin, SERR#. This bit is cleared to 0 upon RESET#. The SERR# pin driven active normally signifies a parity error on the address/control bus.
07	**Wait Cycle Enable**	Always set to 0.
06	**Parity Error Enable**	When set to 1, this bit allows this controller to check for parity errors. When a parity error is detected, the PCI bus signal PERR# is asserted. This bit is cleared (parity testing disabled) upon the assertion of RESET#.
05	**Palette Snoop Enable**	Always set to 0.
04	**Memory Write and Invalidate Enable**	Always set to 0.
03	**Special Cycle Enable**	Always set to 0.
02	**Bus Master Enable**	Always set to 0.
01	**Memory Space Enable**	This bit allows the PCI Controller to decode and respond as a target for memory regions that may be defined in one of the three base address registers. This bit is initialized to 0 upon the assertion of signal pin RESET#.
00	**I/O Space Enable**	This bit allows the PCI Controller to decode and respond as a target to I/O cycles which are to regions defined by any one of the three base address registers. This bit is initialized to 0 upon the assertion of signal pin RESET#.

PCI Command Register

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1.6.4 PCI Status Register (PCISTS) **Address: 06 — 07 (H)**

Power-up value: 0080 H

Boot-load: Not Used

Attribute: Read Only (RO), Read/Write Clear (R/WC)

Size: 16 bits

The PCI Status register contains the PCI status information. Most status bits in this register are designated as "write clear," meaning that in order to clear a given bit, the bit must be written as a 1. All bits written with a 0 are left unchanged. These bits are identified below as (R/WC), while those which are Read Only are shown as (RO).

Bit	Bit Name	Description
15	**Detected Parity Error (R/WC)**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error (R/WC)**	This bit is set whenever the device asserts the signal SERR#. This bit can be reset by writing a 1 to this location.
13	**Received Master Abort (R/WC)**	This bit is set whenever a bus master abort occurs. This bit can be reset by writing a 1 to this location.
12	**Received Target Abort (R/WC)**	This bit is set whenever this device has one of its own initiated cycles terminated by the currently addressed target. This bit can be reset by writing a 1 to this location.
11	**Signaled Target Abort (R/WC)**	This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location.
09-10	**Device Select (DEVSEL#) Timing Status (RO)**	These bits are read-only and define the signal behavior of DEVSEL# from this device when accessed as a target.

Bit 09	Bit 10	Description
0	0	Fast (PCI Controller)
0	1	Medium
1	0	Slow
1	1	Reserved

08	**Data Parity Reported (R/WC)**	This bit is set upon the detection of a data parity error for a transfer involving the PCI Controller as the master. The Parity Error Enable bit (D6 of the Command Register) must be set in order for this bit to be set. Once set, it can only be cleared by either writing a 1 to this location or by the assertion of the signal RESET#.
07	**Fast Back-to-Back Capable (RO)**	When equal to 1, this indicates that the device can accept fast back-to-back cycles as a target.
00-06	**Reserved (RO)**	Always returns 0s.

PCI Status Register

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1.6.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 00 H

Boot-load: External nvRAM/EPROM offset 048 H

Attribute: Read Only

Size: 8 bits

The Revision Identification register contains the revision identification number of the EXC-1553PCI/EP.

Bit	Description
00-07	Revision identification number

Revision Identification Register

1.6.6 Class Code Register (CLCD) Address: 09 — 0B (H)

Power-up value: FF0000 H

Boot-load: External nvRAM offset 049 - 4B H

Attribute: Read Only

Size: 24 bits

The Class Code register is divided into three one-byte fields, residing in the following locations:

- Base class - 0B H
- Sub-class - 0A H
- Programming interface - 09 H

The Class Codes of the EXC-1553PCI/EP are set as indicated below:

Bit	Address	Fields	Value	Description
00-07	0B H	Base Class	07H	Simple communication controller
00-07	0A H	Sub-Class	80H	Other communications device
00-07	09 H	Prog I/F	00H	Register Level Programming Interface

Class Code Register

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1.6.7 Cache Line Size Register (CALN) Address: 0C (H)

Power-up value: 00 H, hardwired
Boot-load: Not Used
Attribute: Read Only
Size: 8 bits

The Cache Line Size register is hardwired to 0.

Bit	Description
00-07	Cache Line Size (RO)

Cache Line Size Register

1.6.8 Latency Timer Register (LAT) Address: 0D (H)

Power-up value: 00 H
Boot-load: External nvRAM offset 04D H
Attribute: Read/Write: bits 03 - 07; Read Only: bits 00 - 02
Size: 8 bits

The Latency Timer register has meaning only for bus masters and thus is not used with the EXC-1553PCI/EP.

Bit	Bit Name	Description
03-07	**Latency Timer Value (R/W)**	Always set to 0
02		Always returns 0
01		Always returns 0
00		Always returns 0

Latency Timer Register

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1.6.9 Header Type Register (HDR)

Address: 0E (H)

Power-up value: 00 H

Boot-load: External nvRAM offset 04E H

Attribute: Read Only

Size: 8 bits

The Header Type register consists of two fields:

- Bits 00 - 06 define the format for bytes 10 H through 3F H of the device configuration header.
- Bit 07 establishes whether this device represents a single function (bit 07 = 0) or a multi-function (bit 07 = 1) PCI bus agent. The PCI Controller is a single function PCI device.

Bit	Description
07	Always returns 0
06-00	Always returns 0s

Header Type Register

1.6.10 Built-In Self-Test Register (BIST)

Address: 0F (H)

Power-up value: 00 H

Boot-load: External nvRAM/EPROM offset 04F H

Attribute: Read Only: D7, D5 - 0; Write Only: D6 as PCI bus

Size: 8 bits

The Built-In Self-Test register is not implemented in the EXC-1553PCI/EP.

Bit	Bit Name	Description
07	**BIST Capable (RO)**	Always returns 0
06	**Start BIST (WO)**	Always set to 0
04-05	**Reserved (RO)**	Always returns 0
03-00	**User-Defined Completion Code (RO)**	Always returns 0

Built-In Self-Test Register

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1.6.11 Base Address Registers (BADR) Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: FFFFFFC1 H for offset 10 H; 00000000 H for all others

Boot-load: External nvRAM offset 050 H, 54 H, 58 H, 5C H, 60 H (BADR0-4)

Attribute: Read/Write: High bits; Read Only: Low bits

Size: 32 bits

The Base Address registers provide a mechanism for assigning memory or I/O space for the card. To determine the actual location(s) the card must respond to: first the board interrogates these registers to ascertain the size or space desired, and then writes the high-order field of each register to place it physically in the system's address space. Bit zero of each field is used to select whether the space required is to be decoded as memory (bit 00 = 0) or I/O (bit 00 = 1). The EXC-1553PCI/EP uses three of the six available base address registers in the on-board PCI controller, as shown below:

Register	Offset	Size	Function
Base Address Register 0 (PAGE 0)	10H	64Byte	PCI Global Interrupt Control Registers
Base Address Register 1 (PAGE 1)	14H	32Kb	1553 Full Channel
Base Address Register 2 (PAGE 2)	18H	32Kb	1553 Concurrent Monitor

Base Address Registers Definition

NOTE The contents of Base Address Register 0 are not loadable from nvRAM.

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DETERMINING BASE ADDRESS SIZE

The address space defined by a given base address register is determined by writing all 1s to a given base address register from the PCI bus and then reading that register back. The number of 0s returned starting from D4 for memory space and D2 for I/O space toward the high-order bits reveals the amount of address space desired. The following table indicates the required nvRAM/EPROM boot values corresponding to PAGES 1-2.

PAGE	nvRAM Offset	nvRAM Contents
PAGE 1	50H	FFFF8000H
PAGE 2	54H	FFFF8000H

Base Address nvRAM/EPROM Boot Values

Bit	Bit Name	Description
31-04	**Base Address Location (RW)**	These bits are used to position the decoded region in memory space. Only bits which return a 1 after being written as 1 are usable for this purpose. Except for Base Address Register 0, these bits are individually enabled by the contents sourced from the external boot memory.
03	**Prefetchable (RO)**	When set as a 1, this bit signifies that this region of memory can be cached. Cachable regions can only be located in the region altered through PCI bus memory writes. This bit, when set, also implies that all read operations will return the data associated for all bytes regardless of the Byte Enables. Memory space which cannot support this behavior should leave this bit in the zero state. For Base Addresses 1 through 4, this bit is set by the Reset pin and later initialized by the external boot memory (if present). Base Address Register 0 always has this bit set to 0. This bit is read only from the PCI interface.
02-01	**Memory Type (RO)**	These two bits identify whether the memory space is 32 or 64 bits wide and if the space location is restricted to be in the first megabyte of memory space. The encoding is as follows:

Bits	02	01	Description
	0	0	Region is 32 bits wide and can be located anywhere in 32 bit memory space.
	0	1	Region is 32 bits wide and must be mapped below the first MByte of memory space.
	1	0	Not Supported.
	1	1	Not Supported.

00	**Memory Space Indicator (RO)**	When set to 0, this bit identifies a base address region as a memory space.

Base Address Register - Memory (Bit 0 = 0)

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Bit	Bit Name	Description
02-31	Base Address Location (RW)	These bits are used to position the decoded region in I/O space. Only bits which return a 1 after being written as 1 are usable for this purpose. Except for Base Address 0, these bits are individually enabled by the contents sourced from the external boot memory (EPROM or nvRAM).
01	Reserved (RO)	This bit should be zero. (Note: Disabled Base Address Registers will return all zeros for the entire register location, bits 31 through 00).
00	I/O Space Indicator (RO)	When set to 1, this bit identifies a base address region as an I/O space.

Base Address Register - I/O (Bit 0 = 1)

1.6.12 Expansion ROM Base Address Register (XROM) Address: 30 (H)

Power-up value: 00000000 H

Boot-load: External nvRAM offset 70 H

Attribute: Read/Write: bits 11 - 31, bit 00; Read Only: bits 01 - 10

Size: 32 bits

The Expansion ROM Space is not implemented on the EXC-1553PCI/EP.

Bit	Bit Name	Description
11-31	Expansion ROM Base Address Location (R/W)	Don't Care
01-10	Reserved (RO)	Always returns 0
00	Address Decode Enable (RW)	Always set to 0

Expansion ROM Base Address Register

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1.6.13 Interrupt Line Register (INTLN) Address: 3C (H)

Power-up value: FF H

Boot-load: External nvRAM offset 7C H

Attribute: Read/Write

Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The ultimate value for this register is system-architecture specific. For x86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines. In x86-based PC systems, the values of 0 to 15 correspond with the IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (the controller's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. This register is boot-loaded from the external boot memory, if present, and may be written by the PCI interface.

Bit	Description
00-07	Desired IRQ #

Interrupt Line Register

1.6.14 Interrupt Pin Register (INTPIN) Address: 3D (H)

Power-up value: 01 H

Boot-load: External nvRAM offset 7D H

Attribute: Read Only

Size: 8 bits

The Interrupt Pin register identifies which PCI interrupt, if any, is connected to the controller's PCI interrupt pins. The allowable values are 0 (no interrupts) or 1 (INTA#). The default power-up value assumes INTA#.

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Bit	Bit Name	Description			
03-07	Reserved	All zeros (RO)			
02-00	Pin Number	Bit 02	Bit 01	Bit 00	Description
		0	0	0	None
		0	0	1	INTA#

Interrupt PIN Register

1.6.15 Minimum Grant Register (MINGNT)

Address: 3E (H)

Power-up value: 00 H

Boot-load: External nvRAM offset 7E H

Attribute: Read Only

Size: 8 bits

The Minimum Grant register is not implemented on the EXC-1553PCI/EP.

Bit	Description
07-00	Don't Care

Minimum Grant Register

1.6.16 Maximum Latency Register (MAXLAT)

Address: 3F (H)

Power-up value: 00 H

Boot-load: External nvRAM offset 7F H

Attribute: Read Only

Size: 8 bits

The Maximum Latency register is not implemented on the EXC-1553PCI/EP.

Bit	Description
07-00	Don't Care

Maximum Latency Register

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1.7 PCI Global Interrupt Control Registers

The PCI Global Interrupt Control Registers are used to enable /disable and check the status of interrupts generated on the PCI bus. These registers are located in PAGE 0 of the EXC-1553PCI/EP.

Note that to generate interrupts on the PCI bus, the interrupt condition registers in Channel 1 and Channel 2 must be programmed according to the interrupt conditions desired.

1.7.1 PCI Interrupt Status Register

Register Name PCI Interrupt Status Register
Address 1CH
Attribute: Read/Write
Size: 32 bits

The PCI Interrupt Status Register is used to determine the source of the card generated PCI bus interrupt, Channel 0 or 1.

Bit	Bit Name	Description
26-31	**Not Used**	Don't Care
25	**IFLAG1**	When set, indicates that Channel 1 generated interrupt
24	**IFLAG0**	When set, indicates that Channel 0 generated interrupt
00-23	**Not Used**	Don't Care

PCI Interrupt Status Register

1.7.2 PCI Interrupt Control Register

Register Name PCI Interrupt Control Register
Address 38H
Attribute: Read/Write
Size: 32 bits

The PCI Interrupt Control Register provides a global enable/disable of card generated PCI interrupts.

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Bit	Bit Name	Description
13-31	**Not Used**	Don't Care
17	**GINT**	When set, indicates that an interrupt occurred. This bit must be reset, to enable further interrupts. To reset, write a 1 to this bit location.
13-16	**Not Used**	Always set to 00H
12	**GINTEN**	To enable PCI interrupts, write a 1 to this bit.
00-11	**INTSEL**	Always set to F00H

PCI Interrupt Control Register

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2 Bus Controller Operation

Chapter 2 describes EXC-1553PCI/EP operation in Bus Controller (BC) mode. The following topics are covered:

- "BC Memory Map," page 2-2
- "Instruction Stack," page 2-3
- "Message Block Formats," page 2-9
- "Continuous or One-Shot Message Transfers," page 2-11
- "Program Example—BC Mode," page 2-13
- "Control Register Definitions," page 2-14

In BC mode, the EXC-1553PCI/EP can be programmed to transmit multiple messages in One-Shot, n-Times, or Loop mode. Simulated errors can be injected into individual messages on a message-by-message basis. You can also preprogram the Intermessage Gap Time of each message.

To program message transfers, load a (relocatable) stack with instructions. Each instruction block contains four words. Many instruction stacks can be created; they reside simultaneously in the dual-port memory. Point to the active instruction stack by programming the Instruction Stack Pointer.

Perform the following procedure after a power-up or a software reset.

To determine whether the board is installed and ready to operate:

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE 1. Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

2. Excalibur Systems recommends that new users use BC/Concurrent-RT mode rather than BC mode. BC/Concurrent-RT mode includes all the functionality of BC mode, and more. In addition, future product development will focus on BC/Concurrent-RT mode.

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2.1 BC Memory Map

Figure 2-1 below illustrates the Bus Controller memory usage.

Concurrent Start Register	7005 H
Reserved	7004 H
Global Software Reset Register	7002 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Reserved	4000–6FFF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF7–3FF9 H
Loop Count Register	3FF6 H
Bit Count Register	3FF5 H
Word Count Register	3FF4 H
BC Response Time Register	3FF3 H
Variable Amplitude Register	3FF2 H
Stack Pointer (16 Bits)	3FF0 H

Frame Time Register (16 Bits)	3FEE H
Frame Time Res. Reg. (16 Bits)	3FEC H
Instruction Counter	3FEB H
Reserved	3E81–3FEA H
Firmware Revision Register	3E80 H
Reserved	3400–3E7F H
Stack(s) and Message Block Area	0000–33FF H

(continued in next column ↗)

Figure 2-1. BC Memory Map

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2.2 Instruction Stack

You use the Instruction stack to program the board. The stack is divided into instruction blocks, each containing four words. The block contains control information (that you write) and status information (that the board writes). Figure 2-2 illustrates one instruction block.

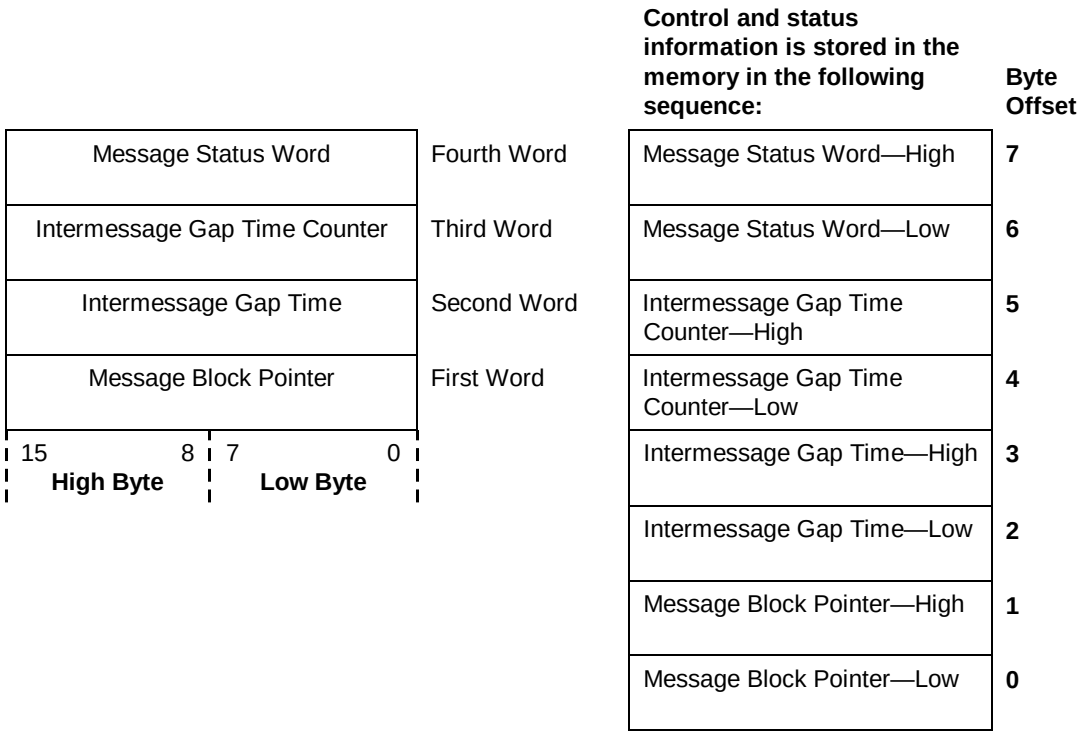


Figure 2-2. Instruction Block Structure—BC Mode

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2.2.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see “1553 RT Status Words,” page 3-7). The contents of the Message status word are described below.

NOTE A logic 1 indicates occurrence of status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed.
14	**Reserved**	Set to 0
13	**Incorrect 1553 Bus**	Remote Terminal response was not received on the active 1553 bus.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit was set in the RT Status word (other than the Message Error bit). The error bit is not set in conjunction with this bit.
10	**Invalid Message Error**	A 1553 message-level error occurred (e.g. Word count, incorrect sync); details in the bits described below.
09	**Response Time Failure**	RT responded late (see “BC Response Time Register,” page 2-20).
08	**Reserved**	Set to 0
07	**Invalid Word Received**	At least one invalid 1553 word received (e.g., bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	1553 Status word received did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the status or data word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word

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NOTE To ensure data integrity, the board sets a special status value of 7F00 (H) to indicate that the message is currently being transmitted. This alerts you *not* to alter this message now. You must check this value *before* attempting to change the data words of the message. Otherwise, the results are indeterminate.

2.2.2 Intermessage Gap Time

The Intermessage Gap Time value is a 16-bit word that you write that allows you to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 4 μsec. measured as dead time on the bus. The value in the word is added to this minimum time. The resolution of this word is 155 nsec. per bit.

2.2.3 Intermessage Gap Time Counter

The Intermessage Gap Time counter (IGT_counter) is a 16-bit word that you write that allows you to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used. For example, if the counter is set to 0, then the gap time is not repeated and depends on the contents of the Intermessage Gap Time location. If the gap time counter is 1 then the gap time is repeated once and equals the Intermessage Gap Time value × 2, etc.

NOTE To ensure maximum Intermessage Gap Time accuracy when using the IGT_counter, use the largest possible value for the Intermessage Gap Time word and the smallest value for the IGT_counter, for a given desired intermessage gap time.

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2.2.4 Message Block Pointer

The Message Block pointer is a 16-bit word that you write that points to the beginning of a 1553 message block.

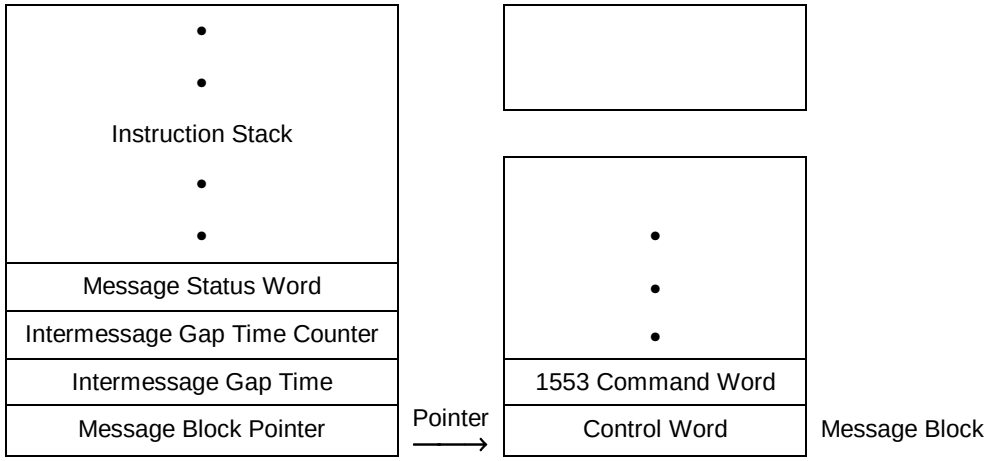


Figure 2-3. Message Block Pointer—BC Mode

2.2.5 Message Block

You can load the message block anywhere in the Instruction Stack/Message Block area (see “BC Memory Map,” page 2-2). Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers “point” to the message blocks in sequence.

Each block contains a 1553 message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the board which type of message to transmit (i.e., RT to RT, Mode code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats (i.e., BC to RT, RT to BC and RT to RT) are illustrated in “Message Block Formats,” page 2-9.

The description of each bit in the Control word follows.

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2.2.6 Control Word

NOTE Logic 1 enables the function; 0 disables the function.

Bit	Bit Name	Description
15	**Stop On Error**	Message error stops BC operation. You can restart by writing to the Instruction Count register and issuing a Start command.
14	**Parity Error**	Selects Even parity in 1553 word.
13	**Halt/Continue**	1 = Halt; stops BC transfer operation. This bit must be reset to 0 to Run or Continue.
12	**Word Count Error**	Transmits fewer or more words than are indicated by the Word Count field (see "Word Count Register," page 2-20). This function is valid for BC to RT messages only.
11	**Bit Count Error**	Transmits invalid number of bits in 1553 words (see "Bit Count Register," page 2-19).
10	**Incorrect Sync**	Transmits incorrect sync. Data type Sync is transmitted in the Command word.
09	**Non-Contiguous Data**	Transmits the first 1553 Data word with invalid Gap Time (between Command and Data word).
08	**Error Placement/ Error Injection Enable**	For BC-to-RT, Broadcast Receive, and Mode Code with Data messages, bit 08 selects the Parity, Sync, and Bit Count error injection placements: 0 in Command word 1 in Data words For other error injection types or other message types, this bit must be set (=1) to enable error injection.
07	**Bus A/B**	Selects active 1553 bus: logic 1 selects bus A; logic 0 selects bus B.
06	**Auto Bus Switch**	On error, the BC will retry message transfer on alternate bus. (Note: Auto-retry must be selected.)
04-05	**Auto Retry Code**	On error, selects the number of retries before transferring the next message:

Bit 05	Bit 04	Description
0	0	No Retry
0	1	1 Retry
1	0	2 Retries
1	1	3 Retries

00-03 **Command Code**	03	02	01	00	Description
	0	0	0	0	Transmit command (RT to BC)
	0	0	0	1	Receive command (BC to RT)
	0	0	1	0	RT-to-RT command
	0	0	1	1	Mode code
	0	1	0	0	Broadcast Receive command
	0	1	0	1	Broadcast RT-to-RT command
	0	1	1	0	Broadcast Mode code
	0	1	1	1	Skip Message (see "Skip Message Operation," page 2-8)
	1	0	0	0	Jump command (see "Jump Command Operation," page 2-8)

BC Control Word

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2.2.7 Halt Operation

You normally set the Halt Operation bit to logic 0 before writing to the Start register. In real-time (during BC execution), you can set this bit to logic 1. When operating on that particular message block's Control word, the board will halt transfer operations until the bit is reset to logic 0.

When the board detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status register (see "Control Register Definitions," page 2-14). You can use the Wait For Continue bit to find out when the board has arrived at the halted instruction block. When the board detects that you have reset the Halt bit (Continue Mode), the board will reset the Wait For Continue bit in the Message Status Register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* (as yet) been executed by the board.

NOTE The Halt operation can be used in conjunction with the Jump command described below (see "Jump Command Operation," below).

2.2.8 Skip Message Operation

The Skip Message command allows you to skip a message defined in a certain message block. You do this by modifying the Command field in the Control word. This lets you selectively send a message in the current frame. The "skip" takes place immediately and does not wait until the Intermessage Gap Time expires.

2.2.9 Jump Command Operation

You can modify the board's BC transfer cycle by setting the Jump command in the BC Control word. The Jump command instructs the board to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 command word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the board has tested the Halt/Continue bit in the Control word. The "jump" takes place immediately and does not wait until the Intermessage Gap Time expires.

The memory structure of the jump command is illustrated in Figure 2-4 below.

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Don't Care	Instruction Count	Third Word
Stack Pointer		Second Word
Control Word		First Word
15 8 **High Byte**	7 0 **Low Byte**	

Figure 2-4. Jump Command Memory Structure

2.3 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire 1553 message as it appears on the 1553 bus, including Command word(s), Data word(s), and Status word(s).

Examples of Message block formats follow.

Example No. 1: Transmit Command

Block *before* execution

1553 Transmit Command	
Control Word	First Location In Block

Block *after* execution

1553 Data Word	From Transmitting Remote Terminal
•	•
•	•
1553 Data Word	•
RT Status Word	From Transmitting Remote Terminal
1553 Transmit Command	
Control Word	First Location In Block

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Example No. 2: Receive Command

Block *before* execution

•
•
1553 Data Word
1553 Data Word
1553 Receive Command
Control Word

First Location In Block

Block *after* execution

RT Status Word
•
•
1553 Data Word
1553 Data Word
1553 Receive Command
Control Word

From Remote Terminal

First Location In Block

Example No. 3: RT-to-RT Command

Block *before* execution

1553 Transmit Command
1553 Receive Command
Control Word

First Location In Block

Block *after* execution

(Receive) RT Status Word	From Receiving Remote Terminal
1553 Data Word	From Transmitting Remote Terminal
•	•
•	•
1553 Data Word	•
(Transmit) RT Status Word	From Transmitting Remote Terminal
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location In Block

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2.4 Continuous or One-Shot Message Transfers

The board can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

In One-Shot mode, (after receiving a Start command) the board transfers all messages, sets the Message Complete bit in the Message Status register, issues an interrupt (if programmed), and waits for a new Start command. Use the Start register (see "Start Register," page 2-17) to select One-Shot mode.

In *n*-Times mode, you load the Loop Count register with the number of times to transmit the messages (frame) and set the Loop and Start bits in the Start register. You can transmit 1–255 times (see "Start Register," page 2-17 and "Loop Count Register," page 2-19). The time between frames is determined by Frame Time register (see "Frame Time Register," page 2-22).

In Continuous Loop mode, the board will retransmit the message frame at a predetermined, user-programmable rate. Use the Start register and the Loop Count register (see "Start Register," page 2-17 and "Loop Count Register," page 2-19) to select Continuous Loop mode. In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the board's operation (see "Start Register," page 2-17).

The Loop time or Frame time is a function of two control registers: the Frame Time register and the Frame Time Resolution register. The internal Frame Time counter is loaded when a Start command with the 16-bit value found in the Frame Time register is received. The Frame Time Counter is decremented every $n \times 155$ nsec., where *n* is the value of the Frame Time Resolution register. After all instructions are executed (1 frame), the board waits until the internal Frame Time counter reaches 0 before transmitting the next frame.

NOTE If the Frame time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 20 µsec, measured as dead time on the bus.

You can implement the desired Frame time by programming the appropriate combinations of the two registers. An example using one method is described below.

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Example Calculating Frame Time

Given: Frame time of 500 msec is required.

Method:

Select Frame Time Resolution of 3225 (Dec) → 0C99 (H)

Frame Time Resolution = 3225 x 155 nsec = 500 µsec (.5 msec)

Subsequently, the Frame Time register value must be equal to:

$$\frac{[500 \text{ msec (desired time)} / .5 \text{ msec} = 1000 \text{ (Dec)}] - 1}{\text{Count} - 1} \rightarrow 03E7 \text{ (H)}$$

Before issuing the Start command, set:

- Frame Time register = 03E7 (H)
- Frame Time Resolution register = 0C99 (H)

2.4.1 Mode Codes

The board handles all dual-redundant 1553B Mode codes; the Word Count field is decoded according to MIL-STD-1553B. The two Quad-Redundant Mode codes, Selected Transmitter Shutdown and Override Selected Transmitter Shutdown are not implemented by the board.

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2.5 Program Example—BC Mode

NOTE All values are in HEX unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,01`	Set Configuration register to BC mode.
`20 POKE &H3FF0,00`	Set Stack Pointer registers to 0000.
`30 POKE &H3FF1,00`	(Stack now begins at address: 0000)
`40 POKE &H3FF2,xx`	Set Variable Amplitude register.
`50 POKE &H3FF3,xx`	Set BC Response Time-Out register.
`60 POKE &H00,00`	Pointer to first message:
`70 POKE &H01,01`	[Location of message is 0100 (H)]
`80 POKE &H02,xx`	Set Intermessage Gap Time location.
`90 POKE &H03,xx`	
`100 POKE &H08,&H40`	Pointer to second message:
`110 POKE &H09,01`	[Location of message is 0140 (H)]
`120 POKE &H0A,xx`	Set Intermessage Gap Time location.
`130 POKE &H0B,xx`	
`140 POKE &H100,&H80`	Set Control word to Transmit command,
`150 POKE &H101,00`	Bus A, and no errors injected.
`160 POKE &H102,&H23`	Set command word to 0C23.
`170 POKE &H103,&H0C`	
`180 POKE &H140,02`	Set Control word to RT to RT command, Bus B,
`190 POKE &H141,00`	and no errors injected.
`200 POKE &H142,&H23`	Set first (receive) command word to 0823.
`210 POKE &H143,08`	
`220 POKE &H144,&H43`	Set second (transmit) command word to 1C43.
`230 POKE &H145,&H1C`	

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BASIC Instruction	Remarks
`240 POKE &H3FEB,2`	Set Instruction counter to 2 (2 messages).
`250 POKE &H3FEE,xx`	Set Frame Time registers.
`260 POKE &H3FEF,xx`	
`270 POKE &H3FEC,xx`	Set Frame Time Resolution registers.
`280 POKE &H3FED,xx`	
`290 POKE &H3FF6,4`	Set Loop Count register to 4 (Transmit these two messages 4 times and stop).
`300 POKE &H3FFC,5`	Set Start register to 5. Starts message transfers in Loop mode.
`310 STOP`	

2.6 Control Register Definitions

2.6.1 Concurrent Start Register — Address: 7005 (H) WRITE

Set the Concurrent Start register to start the operation of Channel 1 and Channel 2 (if present), simultaneously. Starting both channels simultaneously assures that they will be synchronized.

When using the Concurrent Start Register, the standard Start registers of the dual-port RAM must be set to logic 0.

To stop the selected operation(s), follow the normal procedure described under the respective Start register.

NOTE A concurrent start can also be achieved by sending a low TTL pulse of 100 nsec. minimum to the EXSTART$ pin (see “Connectors,” page 7-6).

Bit	Description
00-07	X (Don’t Care)

Concurrent Start Register

2.6.2 Global Software Reset Register — Address: 7002 (H)

Set the Global Software Reset register) to reset both Channel 1 and Channel 2 (if EXC-1553PCI/EPM(I) option present), simultaneously (data field = don’t care).

NOTE Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation is completed.

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2.6.3 Interrupt Reset Register

Address: 7001 (H)

To reset the Interrupt signal generated by Channel 1 write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

2.6.4 Software Reset Register

Address: 7000 (H)

Write to the Software Reset register to reset the current bank (data field = don't care). The bank will act as if power had been switched OFF, then ON. The Board status, the Board ID, Firmware revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

WARNING *Reset erases all memory locations in the dual-port RAM.*

2.6.5 Board Configuration Register

Address: 3FFF (H)

Use the Board configuration register to set the operating mode of the board.

You must set the Board Configuration register before issuing a Start command to the board. To modify the Board Configuration register, issue a Stop command, write one of the hex values to the register (see the table below), then issue a Start command (see "Start Register," page 2-17).

Hex Value	Operating Mode
01	**BC Mode**
02	RT Mode
04	BC/Concurrent-RT Mode
08	BM Sequential Block Mode
10	BM Sequential Link List
20	BM Look-Up Table Mode
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix C, "Internal Loop Back Test," page 9-4).
FF	External Loop Test (see Appendix D, "External Loop Back Test," page 9-5).

Board Configuration Register Values—BC Mode

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2.6.6 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value “E”.

2.6.7 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Board Type is EXC-1553PCI/EP
06	X (Don’t Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

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2.6.8 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the board. Writing the appropriate bit (bit 0) to the Start register starts the Bus Controller transfer operation. When operating in Continuous Loop or *n*-Times mode, you must set the Start and Loop bits in the Start register. The Loop and *n*-Times number are selected via the Loop Count register. In the One-Shot and *n*-Times modes, the board resets the Start bit in the register after *all* messages have been transferred. The board does not reset any bit while in Continuous Loop mode. To halt the Loop operation between messages, set bit 00 to 0. In order to halt the operation at the end of the entire frame, set bit 02 to 0 (bit 02 is not tested between message transfers). Related data bit 04 in the Board Status register indicates when the board has been halted (see "Board Status Register").

Bit	Description
03-07	0
02	1 = Loop Mode 0 = One-Shot Mode
01	0
00	1 = Start Operation 0 = Stop Operation

Start Register

2.6.9 Interrupt Condition Register

Address: 3FFB (H)

The Interrupt Condition register allows you to set interrupt triggers. When a condition occurs that is enabled in this register, an interrupt is generated. To determine which condition caused the interrupt, check the Message Status register.

You must set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 2-17).

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NOTE The interrupt will be sent at the end of the message for all interrupt conditions.

Bit	Description
04-07	0
03	1 = Message Error
02	1 = End Of Frame
01	1 = Message Complete
00	0

Interrupt Condition Register

2.6.10 Message Status Register

Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. The definition of each status bit is described below.

Bit	Bit Name	Description
04-07	**0**	
03	**Message Error**	1 = The message has been sent. As a result, the Error bit has been set in the Message Status word.
02	**End Of Frame**	1 = The last word of the last message in the frame has been sent.
01	**Message Complete**	1 = The last word of the message has been sent.
00	**Wait For Continue**	1 = A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue.

Message Status Register

NOTE Status bits are *not* reset by the board. After reading them, you must reset them.

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2.6.11 Loop Count Register

Address: 3FF6 (H)

The Loop Count register is used in conjunction with the Loop bit in the Start register. If the Loop bit in the Start register is set, then set the Loop Count register to specify the number of times the Message frame will be transmitted. A value of zero is interpreted as a request for continuous looping. You must set the Loop Counter register before issuing a Start command to the board. To modify the Loop Counter register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 2-17).

Bit	Value	Description
00-07	**0**	Transmits in Continuous Loop
	1–255	Sends Message Frame *n*-times (1–255) as defined

Loop Count Register Values

2.6.12 Bit Count Register

Address: 3FF5 (H)

The Bit Count register sets the total number of bits in the 1553 word, including Sync(3) and Parity(1). This register is used by the board only for messages for which the Bit Count Error bit is set in the Control Word of the Message Block (see "Control Word," page 2-7). If the Bit Count Error bit is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

You must set the Bit Count register before issuing a Start command to the board. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 2-17).

Bit	Description			
03–07	0			
00–02	**Bit 02**	**Bit 01**	**Bit 00**	**No. of 1553 bits sent per word**
	0	0	0	17 (-3)
	0	0	1	18 (-2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	22 (+2)
	1	1	0	23 (+3)

Bit Count Register

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2.6.13 Word Count Register

Address: 3FF4 (H)

The Word Count register controls the number of 1553 data words (± 3) in the message and allows you to inject a Word Count error. The error is an offset relative to the 1553 command word Word Count field. This register is used by the board only for messages for which the Word Count Error bit is set in the Control word register (see "Control Word," page 2-7). If the Word Count Error bit is not set, a correct number of words is transmitted regardless of the contents of the Word Count register.

You must set the Word Count register before issuing a Start command to the board. To modify the Word Count register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 2-17).

Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Register Values

2.6.14 BC Response Time Register

Address: 3FF3 (H)

The BC Response Time register sets the BC's Response Time window, whose value determines the maximum (wait) time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 2 µsec.

You must set the BC Response Time register before issuing a Start command to the board. To modify the BC Response Time register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 2-17).

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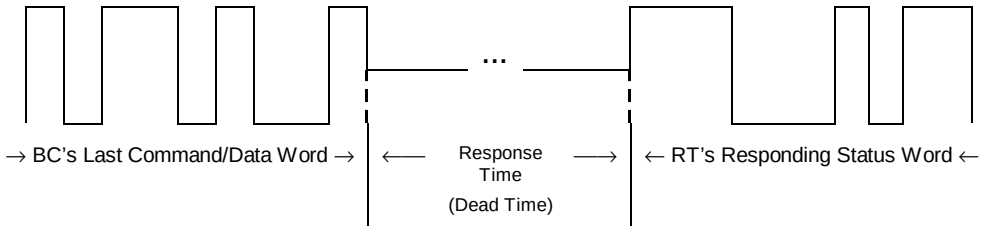


Figure 2-5. BC Response Time Definition

Example Setting the BC Response Time Register

To set up a BC response time of 14 µsec:

Write 90 to the BC Response Time register.

90 x 0.155 ≅ 14 µsec

2.6.15 Variable Amplitude Register

Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.5 volts (peak-to-peak) when measured on the 1553 bus using 1553 direct coupling and 35-ohm load (that is, two 70-ohm termination resistors). If 78-ohm termination resistors are used, a higher transmit (output) amplitude will appear on the 1553 bus. The Variable Amplitude register has a resolution of 30 mV/bit (p-p) on the bus.

You must set the Variable Amplitude register before issuing a Start command to the board. To modify the Variable Amplitude register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 2-17). After a reset, the Variable Amplitude register defaults to FFH, providing maximum amplitude.

2.6.16 Stack Pointer

Address: 3FF0 (H)

The 16-bit Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 (H) and 33FF (H). You must set the Stack Pointer register before issuing a Start command to the board. To modify the Stack Pointer register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 2-17).

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2.6.17 Frame Time Register

Address: 3FEE (H)

The Frame Time register contains the 16-bit Frame Time value for Continuous and *n*-Times modes operation. The value written to the Frame Time register is multiplied by the value set in the Frame Time Resolution register pair described below. The value set must equal the desired multiplication factor – 1 (see "Calculating Frame Time," page 2-12).

You must set the Frame Time register before issuing a Start command to the board. To modify the Frame Time register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 2-17).

2.6.18 Frame Time Resolution Register

Address: 3FEC (H)

The 16-bit Frame Time Resolution value represents the resolution of the Frame Time counter in increments of 155 nsec. (see also "Continuous or One-Shot Message Transfers," page 2-11).

You must set the Frame Time Resolution register before issuing a Start command to the board. For an example of how to calculate Frame Time and Frame Time Resolution, see "Calculating Frame Time," page 2-12. To modify the Frame Time Resolution register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 2-17).

2.6.19 Instruction Counter

Address: 3FEB (H)

The Instruction Counter must be loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than 0 before you write to the Start register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The board updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

You must set the Instruction Counter register before issuing a Start command to the board. To modify the Instruction Counter register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 2-17). When in the Continuous Loop mode, the Instruction Counter register cycles from the initial value down to 1.

2.6.20 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.

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3 Remote Terminal Operation

Chapter 3 describes EXC-1553PCI/EP operation in Remote Terminal (RT) mode. The following topics are covered:

- "RT Memory Map," page 3-3
- "Data Block Look-Up Table," page 3-4
- "Active RT Table," page 3-5
- "1553 RT Status Words," page 3-7
- "Message Stack," page 3-8
- "RT Last Command Words," page 3-11
- "1553 RT BIT Words," page 3-11
- "1553 RT Vector Words," page 3-11
- "Alter Table," page 3-12
- "Mode Codes," page 3-12
- "Broadcast Mode," page 3-12
- "Error Injection Features," page 3-13
- "Program Example—RT Mode," page 3-14
- "Control Register Definitions," page 3-15

The EXC-1553PCI/EP can be configured to simulate up to 32 remote terminals. You can select which terminal(s) are operating (active). In addition, you can inject errors into message responses.

After receiving the Start command, the board handles the transfer of all messages (see "Control Register Definitions," page 3-15). Data associated with a particular RT subaddress combination is transferred via a 2K x 8 look-up table, which points to one of 200 data blocks. Load data blocks associated with transmit commands with 1553 data to transmit, and read received 1553 data from data blocks associated with receive commands.

The board will respond properly to messages received at the maximum rate permitted by the 1553 specification, i.e., with an intermessage gap of 2.0 µsec. measured as dead time on the bus.

You can choose whether the remote terminal should transmit its 1553 status word at the end of a message, even if the message contains *invalid* data words (invalid as specified by MIL-STD-1553). Use the Status Response register to activate or disable this feature (see "Control Register Definitions," page 3-15).

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The remote terminal transmits its 1553 status word in approximately 4 µsec. (measured as dead time on the bus). Use the RT Response Time register to increase the time it takes the remote terminal to transmit the 1553 status word.

The board provides a data integrity value, which indicates that a message is currently being transmitted, and you should not alter it at this time. You must check this value *before* attempting to change the data words of the message (see "Alter Table," page 3-12).

Since most 1553 parameters, such as response time, status word content, etc. are user-programmable, the board can operate in various 1553 environments. The board also allows you to enable or disable the 1553 Broadcast function. If broadcasting is enabled, RT address 31 (11111) is reserved; if broadcasting is disabled, all 32 RT addresses are available (see "DIP Switches," page 7-4).

You can program the 1553 Mode Code subaddress identifier (see "Mode Code Control Register," page 3-23) so that either 31, 0, or both are used to indicate that the 1553 command word is a Mode code.

Perform the following procedure after a power-up or a software reset.

To determine whether the board is installed and ready to operate:

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

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3.1 RT Memory Map

Figure 3-1 illustrates the RT memory usage.

Time Tag Counter Byte 3	700E H
Time Tag Counter Byte 2	700C H
Time Tag Counter Byte 1	700A H
Time Tag Counter Byte 0	7008 H
Time Tag Reset Register	7007 H
Time Tag Options Register	7006 H
Concurrent Start Register	7005 H
Reserved	7004 H
Global Software Reset Register	7002 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Data Block Look-Up Table	4000–47FF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Message Status Register	3FFB H
Reserved	3FF8 H
Time Tag Resolution Register	3FF7 H
Bit Count Register	3FF6 H
Reserved	3FF5 H
RT Response Time Register	3FF4 H
Error Injection Register	3FF3 H
Variable Amplitude Register	3FF2 H
Message Stack Pointer (16 Bits)	3FF0 H
Status Response Register	3FEF H

Reserved	3E86–3FEE H
Board Options Register (16 bits)	3E84 H
Reserved	3E81–3E83 H
Firmware Revision Register	3E80 H
Reserved	3650–3E7F H
Alter Table	34C0–364F H
1553 RT Vector Words (64 Bytes)	3480–34BF H
1553 RT Bit Words (64 Bytes)	3440–347F H
RT Last Command Words (64 Bytes)	3400–343F H
Reserved	33FD–33FF H
Interrupt Condition Register	33FC H
Message Stack (42 Blocks)	3300–33FB H
Word Count Error Table (32 Bytes)	32E0–32FF H
Reserved	3267–32DF H
Mode Code Control	3266 H
Reserved	3260–3265 H
1553 RT Status Words (64 Bytes)	3220–325F H
Active RT Table (32 Bytes)	3200–321F H
1553 Data Blocks (200 Blocks)	0000–31FF H

(continued in next column ↗)

Figure 3-1. RT Memory Map

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3.2 Data Block Look-Up Table

Address: 4000–47FF (H)

The received command word's RT Address, T/R Bit, and Subaddress fields are used to index the entries in the (user-programmed) look-up table. Each entry in the table represents a data block number (from 0 to 199 decimal). Each block can contain up to 32 1553 data words (64 bytes). Data Block 0 begins at address 0000, Data Block 1 begins at address 0040 (H), etc.

	(11 most significant bits of the 1553 command word)					
Base Address	(5 bits) **RT address**	(1 bit) **T/R**	(5 bits) **Sub-address**	**Look-up table (2K x 8)**	**Data block**	**Hex address of data block**
4000+	11111	1	11111	Block #	Data Block 199	31C0
	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
4000+	00000	0	00001	Block #	Data Block 1	0040
4000+	00000	0	00000	Block #	Data Block 0	0000

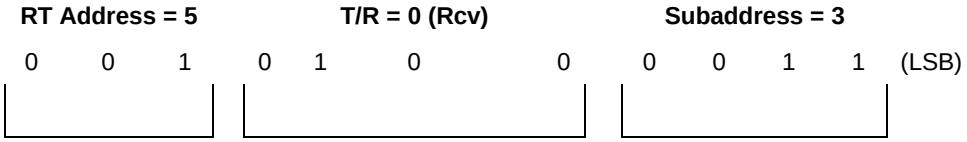
Figure 3-2. Data Block Look-Up Table

NOTE **For RT-to-RT messages:**
When the board is simulating both RTs in an RT-to-RT message transfer, the simulated receiving RT's data block is not updated with the transmit data. (The data is transmitted over the 1553 bus.)

To create the address to the table

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example To allocate a data block for a 1553 receive message to RT#5, Subaddress 3.



Hex representation = 143 (H)

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2. Add the hex value of this part of the command word to the base address of the look-up table (4000H).

```
  4000   (H)
+ 143    (H)
-------
  4143   (H)
```

3. Write the data block number to this location.

Example `POKE &H4143,01` allocates block #1 for the data of this message. Read the 1553 data out by reading block #1, which starts at address 0040 (H). Each data block, beginning at address 0000 is 64 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its block number by 64 (40 H).

3.2.1 Data Storage

The data words must be stored and/or read in the following format in the data block:

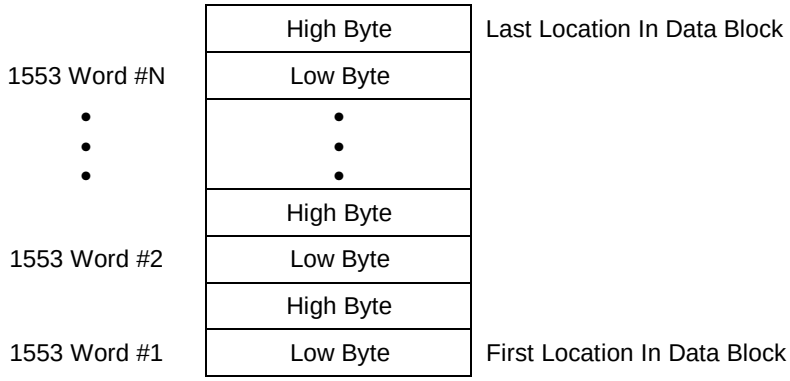


Figure 3-3. Data Storage Sequence

3.3 Active RT Table

Address: 3200–321F (H)

The 32 locations (bytes) of the Active RT table contain the list of active remote terminals. To select an RT to be simulated, set bit 00 in the Active Remote Terminal byte to logic 1. The first active RT byte relates to RT #0, the next to RT #1, and the last location relates to RT #31.

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RT #31 Active RT byte	32nd byte	321F H
• • •	• • •	• • •
RT #0 Active RT byte	1st byte	3200 H

Figure 3-4. Active RT Table—RT Mode

Bit	Bit Name	Description
04-07	**0**	
03	**Inactive Bus B**	1 = Bus B Inactive 0 = Bus B Active If bit 00 is set to 1 and bit 03 is set to 0, the board will respond to all messages received over bus B for this RT; and the board will generate interrupts, if requested to do so. If bit 03 is set to 1, all messages over bus B for this RT will be ignored, regardless of the settings of other bits in this register.
02	**Inactive Bus A**	1 = Bus A Inactive 0 = Bus A Active If bit 00 is set to 1 and bit 02 is set to 0, the board will respond to all messages received over bus A for this RT; and the board will generate interrupts, if requested to do so. If bit 02 is set to 1, all messages over bus A for this RT will be ignored, regardless of the settings of other bits in this register.
01	**Interrupt**	1 = Interrupt 0 = No Interrupt If bit 01 is set to 1, the RT is active and the Interrupt Condition register is enabled, this RT will generate an interrupt.
00	**Active**	1 = Active 0 = Inactive If bit 00 is set to 0, the RT is not active. If it is set to 1, bits 01, 02, and 03 are checked.

Table 3-1. Active RT Byte Definition—RT Mode

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3.4 1553 RT Status Words

Address: 3220–325F (H)

These locations are reserved for the 32 1553 RT status words. Load the desired status words into their respective locations in the block. The first two bytes (word) relate to RT #0, the next two bytes (word) to RT #1, while the last two bytes (word) relate to RT #31. Load low byte, then high byte.

For each RT that is to be simulated, all 16 bits of that RT must be defined in its status word.

In a non-1553B environment (see "Status Response Register," page 3-22) the user-defined status word is sent whenever the RT has to respond with a status word.

In a 1553B environment (see "Status Response Register," page 3-22), the same status word is sent with the following conditions:

Message Error (Bit 10)
In case an error occurred in the previous message, the Status Word will be sent with the Message Error bit set to 1 if the current message is of type Send Status or Send Last Command. This will occur even if you set the Message Error bit to 0.

If you set the Message Error bit to 1, it will always be sent set to 1.

Busy (Bit 03)
The Busy bit is always sent as you defined it. In the case of Transmit commands, when Busy is set to 1, no data words will be transmitted by the RT following the transmission of the status word.

The MIL-STD-1553B Format for the status word is as follows:

Bit	Bit Name
11–15	RT Address
10	Message Error
09	Instrumentation
08	Service Request
05–07	Reserved
04	Broadcast
03	Busy
02	Subsystem Flag
01	Dynamic Bus
00	Terminal Flag

1553B Status Word

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3.5 Message Stack

The board generates a message stack in the dual-port memory. This stack contains information you can use for post-processing of RT messages. The stack is divided into 42 blocks, each containing three words. The stack operates as a circular buffer. The Message Stack Pointer points to the beginning of the (next) unused block. Only active RT messages are stored. Figure 3-5 illustrates one block.

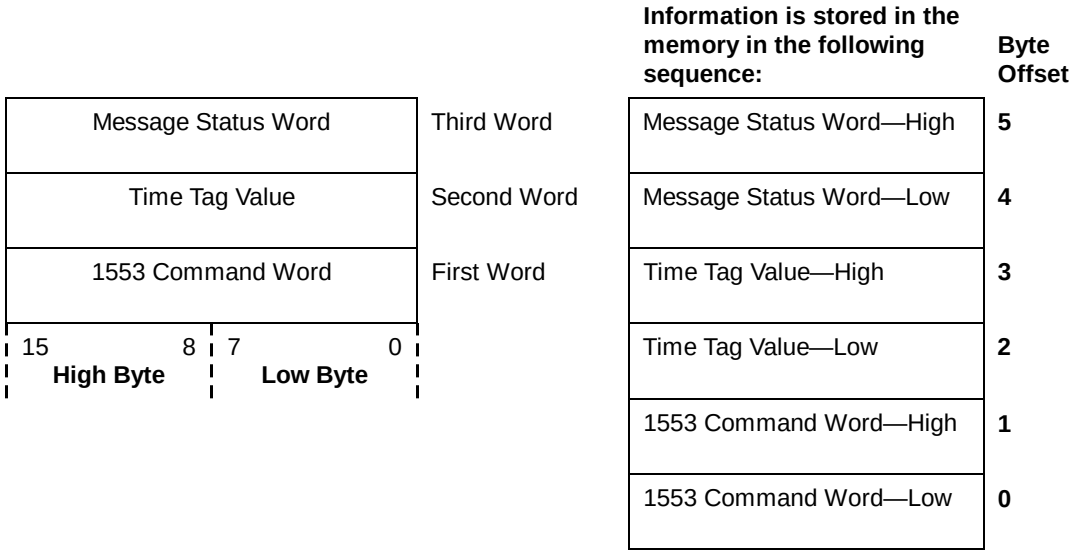


Figure 3-5. Message Stack Block Structure

How the board updates an RT-to-RT message

When an RT-to-RT message is received—where the board is functioning as both RTs—the Message stack is updated as follows:

Two message stack blocks are utilized.

1. The 1553 Receive command word is written into the *first* message stack block.
2. The RT-RT bits in *both* message status words are set to 1.
3. The board updates the Time Tag word in the *second* stack block and the *second* Message Status word. The board updates only the RT-to-RT bit in the *first* Message Status word to Active status.
4. The 1553 Transmit command word is written into the *second* stack block.

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3.5.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see "1553 RT Status Words," page 3-7). The contents of the Message status word are described below.

NOTE A logic 1 indicates the occurrence of a status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed
14	**Bus A/B**	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
13	**Reserved**	Set to 0
12	**Reserved**	Set to 0
11	**Reserved**	Set to 0
10	**Tx Time Out**	Board, acting as receiver in RT-to-RT message, did not sense a transmitter status word (in 14 µsec.)
09	**Reserved**	Set to 0
08	**Reserved**	Set to 0
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity)
06	**Reserved**	Set to 0
05	**Word Count Error (Receive Message)**	Incorrect number of words received in the message
04	**Broadcast Message**	Broadcast command word received
03	**Incorrect Sync Received**	Sync of either the command or the data word(s) is incorrect
02	**Non - Contiguous Data (Receive Message)**	Invalid gap between received 1553 words
01	**RT-RT Message**	RT-to-RT message received where board was simulating both RTs
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word Definitions

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3.5.2 Time Tag Value

Read by User

The Time Tag value is a 16-bit word which can be used to determine the time elapsed since the Start command was issued or the time between 1553 messages. The Time Tag implementation uses a 32-bit, free-running counter whose resolution is set by the Time Tag Resolution register. This register has a resolution of 4 µsec. per bit. The equation to determine the Time Tag resolution = (register value + 1) x 4 µsec.

Example

Register value = 0 → Counter's resolution = 4 µsec

Register value = 4 → Counter's resolution = 20 µsec

To reset the Time Tag counter (to 0) any time, write to the Time Tag Reset Register (see "Control Register Definitions," page 3-15).

When the first command of each message is received, the value of the 16 lower bits of the Time Tag Counter register are written to dual-port RAM.

NOTE 1. You can read the counter's value any time by reading the Time Tag Counter addresses (see "Control Register Definitions," page 3-15).

2. The counter can also be clocked and/or reset from an external source (see EXTTCLKx and EXTTRSTx$ pins in "Connectors," page 7-7).

Example How To Calculate Elapsed Time

Time Tag Resolution register = 03 (initialized before Start command)

Time Tag values (read during or after message transfers):

Low = 40 (H)
High = 10 (H)

Time elapsed since Start command
= (Time Tag register value) x (Time Tag Resolution value + 1) x (4 µsec)
= 1040 (H) x (03 + 1) x 4 µsec
= 4160 (Dec) x (4 x 4 µsec) = 66560 µsec (66.56 msec.)

3.5.3 1553 Command Word

The command word location contains the 1553 command word associated with the message.

Only active RT 1553 command words are stored.

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3.5.4 RT-To-RT Messages

When the board is operating as both RTs in an RT-to-RT transfer:

- The board transmits both 1553 Status and Data words onto the bus.
- The board does *not* copy the Transmit data block into the Receiver data block area (pointed to by the look-up table pointer).

3.6 RT Last Command Words

Address: 3400–343F (H)

The Last command word locations are reserved for the (32) 1553 Last command words. The board writes to these locations at the end of each message transfer (for active RTs only). The first two bytes (word) are for RT #0, the next two bytes (word) are for RT #1, and the last two bytes (word) are for RT #31. Read low byte, then high byte. These words are used for the implementation of the Transmit Last Command Word Mode code.

NOTE Only command words of valid messages containing no errors are recorded in this table.

3.7 1553 RT BIT Words

Address: 3440–347F (H)

The RT BIT word locations are reserved for the 32 1553 BIT words. Load the desired BIT words into the corresponding locations in the block. The first two bytes (word) are for RT #0, the next two bytes (word) are for RT #1, and the last two bytes (word) are for RT #31. Set low byte, then high byte. These words are used to implement the Transmit BIT Word Mode code.

3.8 1553 RT Vector Words

Address: 3480–34BF (H)

The RT Vector Word locations are reserved for the 32 1553 Vector words. Load the desired Vector words into the corresponding locations in the block. The first two bytes (word) are for RT #0, the next two bytes (word) are for RT #1, and the last two bytes (word) are for RT #31. Read low byte, then high byte. These words are used to implement the Transmit Vector word Mode code.

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3.9 Alter Table

Address: 34C0–364F (H)

To ensure data integrity, the board sets a special status value of 7F00 (H) to indicate that the message is currently being transmitted. This alerts you *not* to alter this message now.

This special status value is stored in a 200-word table in the dual-port RAM, one element for each data block that can be associated with an RT or with multiple RTs. When you start sending out data over the bus (from a specific data block), the board sets the Alter Table entry for this block to the special status value, 7F00 (H), indicating to you to *not* alter the data associated with this block at this time. When the card has completed sending the data out over the bus, the board resets the Alter Table entry to 0, indicating that you may now alter the data.

You must check this value *before* attempting to change the data words of the message. Otherwise, the results are indeterminate.

3.10 Mode Codes

You can program the Subaddress code to indicate that a Mode command has been received. Either or both of the following codes can be used: 11111 and 00000. You must program the Mode Code Control register as described in “Control Register Definitions,” page 3-15.

The board handles all dual-redundant 1553B Mode codes. The Word Count field is decoded according to MIL-STD-1553B. One of the Mode codes (Synchronize with Data word) is operated upon as a standard message transfer, using the Data Block look-up table. When the board encounters the Synchronize with Data word Mode code, the command word’s RT Address, T/R bit, and Subaddress fields are used as a pointer to the look-up table. The table entries that are addressed when the T/R bit = 0 and Subaddress = 00000 or 11111 should contain a Data Block number (0–199) indicating where the Synchronize with Data Word’s data word should be stored.

The data associated with mode codes (Transmit Last Command, Transmit Bit word, and Transmit Vector word) is set using the dedicated blocks in the on-board memory (described in “RT Last Command Words,” page 3-11, “1553 RT BIT Words,” page 3-11, and “1553 RT Vector Words,” page 3-11).

3.11 Broadcast Mode

To operate the board in the broadcast environment, select the appropriate DIP switch setting as defined in “DIP Switches,” page 7-4.

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When operating in Broadcast mode, you must set the active RT look-up table entry for RT #31 as Not Active. The board tests the Broadcast DIP switch to determine whether the board is operating in Broadcast mode.

In Broadcast mode, the board stores the received message in a 1553 data block area in the same way as standard message formats. RT address, T/R bit, and Subaddress are used as a pointer to the Data Block look-up table memory.

NOTE When operating in Broadcast mode, the Broadcast bits in the 1553 Status words are *not* updated by the board's processor.

3.12 Error Injection Features

The board allows two types of error injection:

- Global (for all RTs)
- Per RT

The global errors such as Parity, Sync, Non-Contiguous data and Bit count are described in "Error Injection Register," page 3-21. These errors are either ON or OFF for all RTs. The ability to inject a 1553 Word Count error, however, can be set per RT.

3.12.1 Word Count Error Table **Address: 32E0–32FF (H)**

The Word Count Error is selected by writing to the Word Count Error table, which contains 32 bytes (one per remote terminal). The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31. The contents of each location controls the number of 1553 words (±3 words) in the message. The variation is an offset, relative to the 1553 command word's Word Count field. The resulting message (if an error is programmed) must contain at least one data word.

Upon power-up and software reset, the board sets the Word Count Error Table to the default value, 00.

You must set the Word Count Error register before issuing a Start command to the board. To modify the Word Count Error register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 3-18).

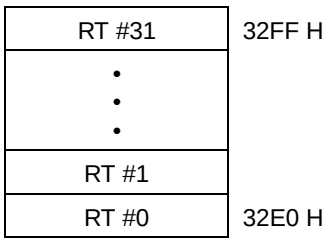


Figure 3-6. Word Count Error Table Addresses

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Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Error Byte Values

3.13 Program Example—RT Mode

NOTE All values are in HEX unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,02`	Set Configuration register to RT mode.
`20 POKE &H3FF2,xx`	Set Variable Amplitude register.
`30 POKE &H3201,1`	Enable RT #1.
`40 POKE &H3204,1`	Enable RT #4.
`50 POKE &H3222,00`	Set Status word of RT #1 to 0800.
`60 POKE &H3223,08`	
`70 POKE &H3228,00`	Set Status word of RT #4 to 2000.
`80 POKE &H3229,&H20`	
`90 POKE &H3FF7,xx`	Set Time Tag Resolution register.
`100 POKE &H3266,00`	Set Mode Code Control register to Subaddress 0 & 31.
`110 POKE &H3FF3,00`	Set No global error injection.
`120 POKE &H4xxx,1`	Load block number 1 for data storage into look-up table xxx.
`130 POKE &H4yyy,2`	Load block number 2 for data storage into look-up table yyy.
`140 POKE &H3FFC,1`	Set Start register to 1 to start RT mode.
`150 STOP`	

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3.14 Control Register Definitions

3.14.1 Time Tag Counter — Address: 7008—700E (H) READ ONLY

Read the four bytes of the Time Tag Counter to determine the current bank's free-running, 32-bit Time Tag counter value. You may read the counter at any time.

The counter must be read in the following sequence:

1. 7008 (H)
2. 700A (H)
3. 700C (H)
4. 700E (H)

7008 (H) contains the LSB; 700E (H) contains the MSB. The Time Tag Resolution register sets the resolution of the counter ("Time Tag Resolution Register," page 3-19).

The counter is reset upon power-up or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFFFFFF (H), the counter wraps around to 0 and continues counting.

3.14.2 Time Tag Reset Register — Address: 7007 (H) WRITE ONLY

Write to the Time Tag Reset register to reset the Channel 1 Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

NOTE The counter can also be reset from an external source (see EXTTRSTx$ pin in "Connectors," page 7-7).

3.14.3 Time Tag Options Register — Address: 7006 (H) WRITE ONLY

Set the Time Tag Options register's 00 bit to select the Channel 1 Time Tag Counter Clock Source. After power-up or software reset, the Time Tag Options register's 00 bit is set to 0.

Bit	Description
01–07	Reserved
00	0 = Internal Time Tag Clock 1 = External Time Tag Clock (see EXTTCLKx pin in Connectors, page 7-7).

Time Tag Options Register

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3.14.4 Concurrent Start Register

Address: 7005 (H) WRITE

Set the Concurrent Start register to start the operation of Channel 1 and Channel 2 (if present), simultaneously. Starting both channels simultaneously assures that they will be synchronized.

When using the Concurrent Start register, the standard Start registers of the dual-port RAM must be set to logic 0.

To stop the selected operation(s), follow the normal procedure described under the respective Start register.

NOTE A concurrent start can also be achieved by sending a low TTL pulse of 100 nsec. minimum to the EXSTART$ pin (see "Connectors," page 7-7).

Bit	Description
00-07	X (Don't Care)

Concurrent Start Register

3.14.5 Global Software Reset Register

Address: 7002 (H)

Set the Global Software Reset register to reset both Channel 1 and Channel 2 (if EXC-1553PCI/EPM(I) option present), simultaneously (data field = don't care).

NOTE Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation is completed.

3.14.6 Interrupt Reset Register

Address: 7001 (H)

To reset the Interrupt signal generated by Channel 1, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

3.14.7 Software Reset Register

Address: 7000 (H)

Set the Software Reset register to reset Channel 1 (data field = don't care). The bank will act as if the power had been switched OFF then ON. After the reset operation is completed, the board writes to the Board status, the Board ID, Firmware revision, and Variable Amplitude registers.

WARNING *Reset erases all memory locations in the dual-port RAM.*

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3.14.8 Board Configuration Register

Address: 3FFF (H)

Use the Board configuration register to set the operating mode of the board.

You must set the Board Configuration register before issuing a Start command to the board. To modify the Board Configuration register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 3-18).

Hex Value	Operating Mode
01	BC Mode
02	**RT Mode**
04	BC/Concurrent RT
08	BM Sequential Block Mode
10	BM Sequential Link List
20	BM Look-Up Table Mode
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix C, "Internal Loop Back Test," page 9-4).
FF	External Loop Test (see Appendix D, "External Loop Back Test," page 9-5).

Board Configuration Register Values-RT Mode

3.14.9 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value "E".

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3.14.10 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Board Type is EXC-1553PCI/EP
06	X (Don't Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

3.14.11 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the board. You can Start, then Stop the RT operation, modify RT parameters (example: the Error Injection register or Response Time), and then issue a new Start command in real time.

For more information about Bit 04 (Board Halted/Running) in the Board Status Register, see the note in "Board Status Register."

Bit	Description
01–07	0
00	1 = Start Operation 0 = Stop Operation

Start Register

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3.14.12 Message Status Register

Address: 3FFB (H)

The Message Status register indicates that a 1553 message has been received. This bit is also set for messages with errors.

Bit	Description
01–07	0
00	1 = Message Complete

Message Status Register

NOTE After reading, reset the Message Complete bit; the board does not reset this bit.

3.14.13 Time Tag Resolution Register

Address: 3FF7 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 µsec.

To determine the Time Tag Counter's Resolution, use the following equation:

= (Time Tag Resolution register value + 1) x 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

You must set the Time Tag Resolution register before issuing a Start command to the board. To modify the Time Tag Resolution register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 3-18).

3.14.14 Bit Count Register

Address: 3FF6 (H)

The Bit Count register sets the total number of bits within the 1553 word, including Sync(3) and Parity(1). This register is used by the board only if the Bit Count Error bit is set in the Error Injection register. If the Bit Error Count is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

You must set the Bit Count register before issuing a Start command to the board. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 3-18).

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Bit	Description			
03–07	0			
00–02	Bit 02	Bit 01	Bit 00	No. of 1553 bits sent per word
	0	0	0	18 (-2)
	0	0	1	22 (+2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	17 (-3)
	1	1	0	23 (+3)

Bit Count Register

3.14.15 RT Response Time Register

Address: 3FF4 (H)

The RT Response Time register sets the Response Time of the Remote Terminal. The resolution of the Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 4 µsec., which is achieved by writing a 0 to this register. Any value above zero will result in a Response Time equal to 4 µsec. plus the contents of the register x 155 nsec. The actual response time has a tolerance of ± 1 µsec.

You must set the Response Time register before issuing a Start command to the board. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command (see “Start Register,” page 3-18).

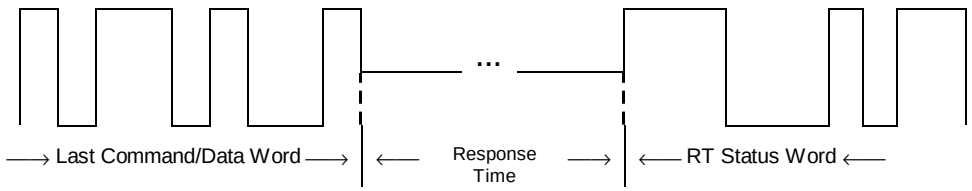


Figure 3-7. RT Response Time Definition

Example Setting RT Response Time Register

To request a response time of 9 µsec:

Write 32 to the RT Response Time register.

32 x 0.155 ≅ 5 µsec + 4 µsec = 9 µsec

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3.14.16 Error Injection Register

Address: 3FF3 (H)

The Error Injection register is a global register that allows you to select the type of error to be injected in a transmitted message. When the board receives a Start command (issued by writing to the Start register), the board reads this register.

To modify the Error Injection register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 3-18).

Bit	Description
07	Data Word Sync Error (Data Words Sent With Command Sync)
06	Data Word Parity Error (Data Words Sent With Even Parity)
05	Status Word Synchronization Error (Status Word Sent With Data Sync)
04	Status Word Parity Error (Status Word Sent With Even Parity)
03	Reserved (Set to 0)
02	Non-Contiguous Data (Between First and Second Data Word)
01	Bit Count Error (see "Bit Count Register," page 3-19)
00	Reserved (Set to 0)

Error Injection Register

3.14.17 Variable Amplitude Register

Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.5 volts (peak-to-peak), when measured on the 1553 bus using 1553 coupling and 35-ohm load (that is, two 70-ohm termination resistors) as specified. If 78-ohm termination resistors are used, a higher Transmit (output) amplitude will appear on the 1553 bus. The Variable Amplitude register has a resolution of 30 mV/bit (p-p) on the Bus.

You must set the Variable Amplitude register before issuing a Start command to the board. To modify the Variable Amplitude register, issue a Stop command, modify, and then issue a Start command (see "Start Register," page 3-18). After a reset, the Variable Amplitude register defaults to FFH, providing maximum amplitude.

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3.14.18 Message Stack Pointer

Address: 3FF0 (H)

The 16-bit Message Stack pointer indicates the Message Stack position. After the entire message is received, the Message Stack pointer is updated (incremented by 6). This word is initialized to 3300 (H) and circulates in the Message Stack between 3300 (H) to 33F6 (H).

3.14.19 Status Response Register

Address: 3FEF (H)

The Status Response register allows you to control the Status Response mode of operation.

After a Receive message, you can respond with a 1553 Status word even if an invalid 1553 Data word was received. You can also select a 1553 environment, which will affect some 1553 RT Status word bits (see "1553 RT Status Words," page 3-7).

You must set the Status Response register before issuing a Start command to the board. To modify the Status Response register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 3-18).

Bit	Description
02–07	0
01	Environment: 0 = 1553B 1 = Non-1553B
00	On Error: 0 = Suppress Status 1 = Send Status

Status Response Register

3.14.20 Board Options Register

Address: 3E84 (H) READ ONLY

The Board Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

Bit	Description
10–15	Reserved
09	1 = 1760
08	1 = 1553
00–07	Reserved

Board Options Register

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3.14.21 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level = 1.2.

3.14.22 Interrupt Condition Register

Address: 33FC (H)

The Interrupt Condition register allows you to enable an interrupt trigger. The Message Complete bit works in conjunction with the Interrupt bit in the Active RT table. When a message is received by an RT for which the Active RT interrupt bit is set, the board will check the Message Complete bit. If this bit is also set, an interrupt will be generated.

You must set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see “Start Register,” page 3-18).

Bit	Description
02–07	0
01	1 = Message Complete
00	0

Interrupt Condition Register

3.14.23 Mode Code Control Register

Address: 3266 (H)

The Mode Code Control register allows you to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

You must set the Mode Code Control register before issuing a Start command. To modify the Mode Code Control register, issue a Stop command, modify the register, then issue a Start command (see “Start Register,” page 3-18).

Bit	Description		
02–07	0		
00–01	**Bit 01**	**Bit 00**	**Subaddresses Recognized as Mode Code**
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

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4 BC/Concurrent-RT Operation

Chapter 4 describes EXC-1553PCI/EP operation in Bus Controller/Concurrent-Remote Terminal mode. The following topics are covered:

- "BC/Concurrent-RT Memory Map," page 4-3
- "Instruction Stack," page 4-4
- "Remote Terminal Simulation," page 4-12
- "Message Block Formats," page 4-13
- "Continuous or One-Shot Message Transfers," page 4-15
- "Program Example—BC/Concurrent-RT Mode," page 4-17
- "Control Register Definitions," page 4-18

The EXC-1553PCI/EP can simultaneously operate as the bus controller and up to 32 Remote Terminals. The messages and the instruction stack are loaded as for BC operation.

In BC/Concurrent-RT mode, load message blocks with the RT's 1553 Status and Data words for those Remote Terminals that you are actively simulating. These words must be loaded into the appropriate locations in the message blocks in the sequence that the 1553 words appear on the 1553 bus.

NOTE The requirement for loading the message blocks only applies to RTs that you are actively simulating. For RTs that are not active (not simulated by the board in a single message), you can leave the corresponding locations blank in the associated 1553 message blocks.

The Remote Terminals simulated in BC/Concurrent-RT mode have a minimum response time of approximately 4 µsec., measured as dead time on the bus.

In BC/Concurrent-RT mode, the board supports Minor Frame operation, a message type which functions as a "delay time" message, between groups of messages. You can use the minor frame to produce a list of messages which will be sent out over the bus at different frequencies. You can also send Asynchronous Frames, so that in the middle of the transmission of the messages of a frame, you can transmit another frame and then return to continue transmitting the messages of the previous frame.

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Perform the following procedure after a power-up or a software reset.

To determine whether the board is installed and ready to operate:

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

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4.1 BC/Concurrent-RT Memory Map

Figure 4-1 below illustrates the BC/Concurrent-RT memory usage.

Concurrent Start Register	7005 H
Reserved	7004 H
Global Software Reset Register	7002 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Reserved	4000–6FFF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
RT Response Time Register	3FF9 H
Reserved	3FF7–3FF8 H
Loop Count Register	3FF6 H
Bit Count Register	3FF5 H
Word Count Register	3FF4 H
BC Response Time Register	3FF3 H
Variable Amplitude Register	3FF2 H
Stack Pointer	3FF0 H
Frame Time Register	3FEE H
Frame Time Resolution Reg.	3FEC H
Instruction Counter	3FEB H

Reserved	3FEA H
Minor Frame Time Register	3FE8 H
Minor Frame Resolution Register	3FE6 H
Reserved	3E86–3FE5 H
Board Options Register (16 bits)	3E84 H
Reserved	3E81–3E83 H
Firmware Revision Register	3E80 H
Reserved	3425–3E7F H
Asynchronous Start Flag Register	3424 H
Asynchronous Frame Pointer Reg.	3422 H
Asynchronous Message Count Reg.	3420 H
Active RT Table (32 Bytes)	3400–341F H
Instruction and Message Block Area	0000–33FF H

(continued in next column ↗)

Figure 4-1. BC/Concurrent-RT Memory Map

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4.2 Instruction Stack

You use the Instruction stack to program the board. The stack is divided into instruction blocks, each containing four words. The block contains control information (that you write) and status information (that the board writes). Figure 4-2 illustrates one instruction block.

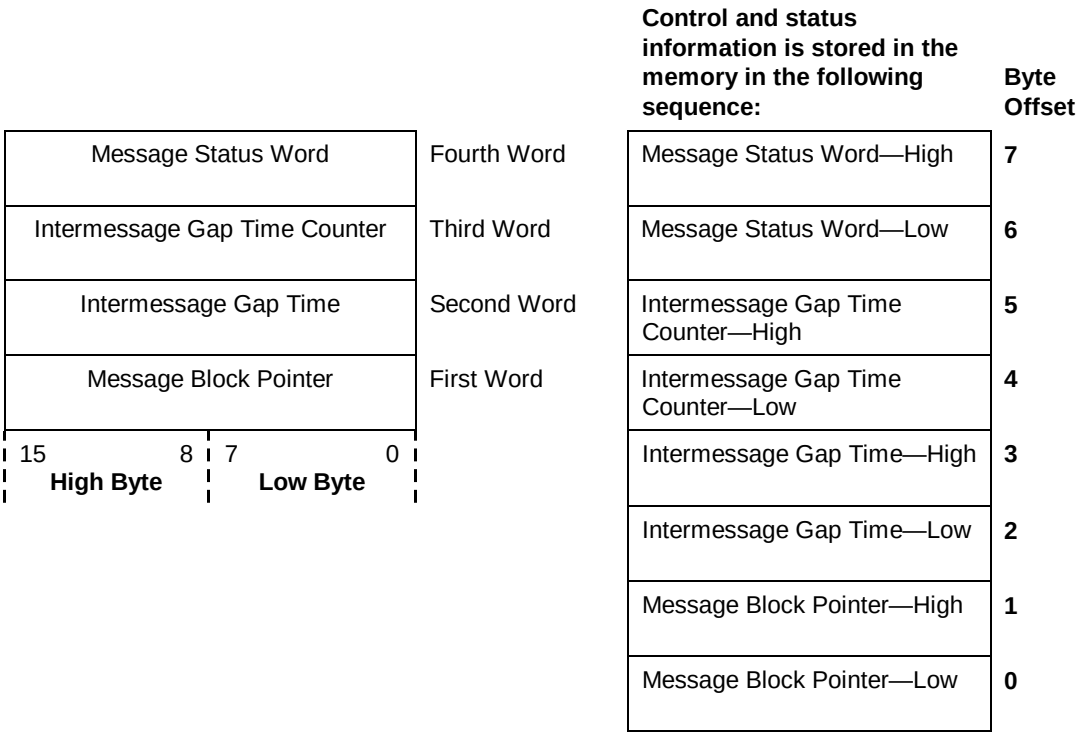


Figure 4-2. Instruction Block Structure—BC/Concurrent-RT Mode

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4.2.1 Message Status Word

The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse this word with the 1553 Status word (see "1553 RT Status Words," page 3-7). The contents of the Message status word are described below.

NOTE A logic 1 indicates occurrence of status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed.
14	**Reserved**	Set to 0
13	**Incorrect 1553 Bus**	Remote Terminal response was not received on the active 1553 bus.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit was set in the RT Status word (other than the Message Error bit). The error bit is not set in conjunction with this bit.
10	**Invalid Message Error**	A 1553 message-level error occurred (e.g. Word count, incorrect sync); details in the bits described below.
09	**Response Time Failure**	RT responded late (see "BC Response Time Register," page 4-26).
08	**Reserved**	Set to 0
07	**Invalid Word Received**	At least one invalid 1553 word received (e.g., bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	1553 Status word received did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the status or data word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word

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NOTE To ensure data integrity, the board sets a special status value of 7F00 (H) to indicate that the message is currently being transmitted. This alerts you *not* to alter this message now. You must check this value *before* attempting to change the data words of the message. Otherwise, the results are indeterminate.

4.2.2 Intermessage Gap Time

The Intermessage Gap Time value is a 16-bit word that you write that allows you to insert a unique intermessage delay time between the current message and the next message. The minimum Intermessage Gap Time is approximately 4 µsec. measured as dead time on the bus. The maximum Intermessage Gap Time is approximately 10 µsec., which can be extended up to approximately 80 sec. using the IGT Counter value (see below). The value in the word is added to this minimum time. The resolution of this word is 155 nsec. per bit.

4.2.3 Intermessage Gap Time Counter

The Intermessage Gap Time counter (IGT_counter) is a 16-bit word that you write that allows you to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used (bits 00–12). Use bit 13 in this register to instruct the board to generate an interrupt when this specific message completed.

Bit	Bit Name	Description
14–15	**Reserved**	Set to 0
13	**Int_On_Select_Msg**	1 = Generate an interrupt when this specific message is completed. To set general interrupt conditions, see “Interrupt Condition Register,” page 4-22.
00–12	**IGT_counter**	Write a value to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used. For example, if the counter is set to 0, then the gap time is not repeated; and depends on the contents of the Intermessage Gap Time location. If the gap time counter is 1 then the gap time is repeated once and equals the Intermessage Gap Time value × 2, etc. Note: To ensure maximum Intermessage Gap Time accuracy when using the IGT_counter, use the largest possible value for the Intermessage Gap Time word and the smallest value for the IGT_counter, for a given desired intermessage gap time.

Intermessage Gap Time Counter

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4.2.4 Message Block Pointer

The Message Block pointer is a 16-bit word that you write that points to the beginning of a 1553 message block.

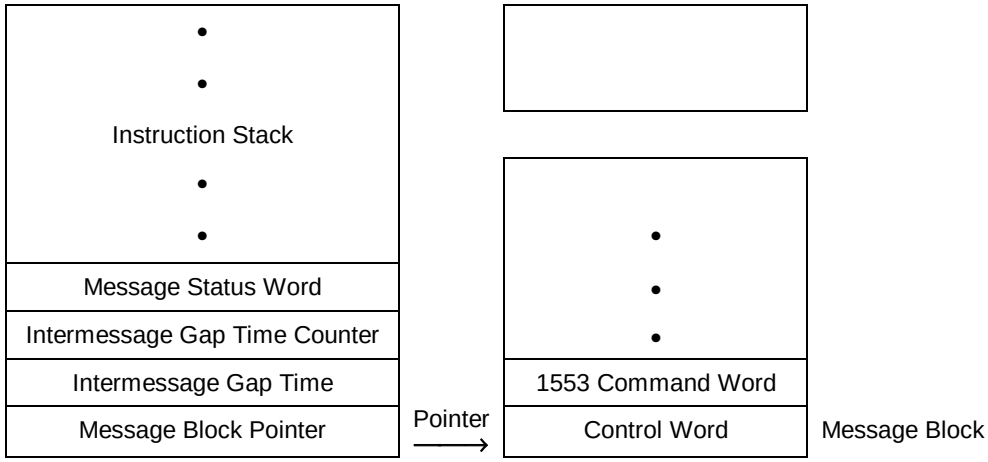


Figure 4-3. Message Block Pointer—BC/Concurrent-RT Mode

4.2.5 Message Block

You can load the message block anywhere in the Instruction Stack/Message Block area (see "BC/Concurrent-RT Memory Map," page 4-3). Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers "point" to the message blocks in sequence.

Each block contains a 1553 message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the board which type of message to transmit (i.e., RT to RT, Mode code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats (i.e., BC to RT, RT to BC and RT to RT) are illustrated in Message Block Formats, page 4-13.

The description of each bit in the Control word follows.

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4.2.6 Control Word

NOTE Logic 1 enables the function; 0 disables the function.

Bit	Bit Name	Description
15	**Stop On Error**	Message error stops BC operation. You can restart by writing to the Instruction Count register and issuing a Start command.
14	**Parity Error**	Selects Even parity in 1553 word.
13	**Halt/Continue**	1 = Halt; stops BC transfer operation. This bit must be reset to 0 to Run or Continue.
12	**Word Count Error**	Transmits fewer or more words than are indicated by the Word Count field (see "Word Count Register," page 4-25). This function is valid for BC to RT messages only.
11	**Bit Count Error**	Transmits invalid number of bits in 1553 words (see "Bit Count Register," page 4-24).
10	**Incorrect Sync**	Transmits incorrect sync. Data type Sync is transmitted in the Command word.
09	**Non-Contiguous Data**	Transmits the first 1553 Data word with invalid Gap Time (between Command and Data word).
08	**Error Placement/ Error Injection Enable**	For BC-to-RT, Broadcast Receive, and Mode Code with Data messages, bit 08 selects the Parity, Sync, and Bit Count error injection placements: 0 in Command word 1 in Data words For other error injection types or other message types, this bit must be set (=1) to enable error injection.
07	**Bus A/B**	Selects active 1553 bus: logic 1 selects bus A; logic 0 selects bus B.
06	**Auto Bus Switch**	On error, the BC will retry message transfer on alternate bus. (Note: Auto-retry must be selected.)
04-05	**Auto Retry Code**	On error, selects the number of retries before transferring the next message:

Bit 05	Bit 04	Description
0	0	No Retry
0	1	1 Retry
1	0	2 Retries
1	1	3 Retries

00-03 **Command Code**	03	02	01	00	Description
	0	0	0	0	Transmit command (RT to BC)
	0	0	0	1	Receive command (BC to RT)
	0	0	1	0	RT-to-RT command
	0	0	1	1	Mode code
	0	1	0	0	Broadcast Receive command
	0	1	0	1	Broadcast RT-to-RT command
	0	1	1	0	Broadcast Mode code
	0	1	1	1	Skip Message (see "Skip Message Operation," page 4-9)
	1	0	0	0	Jump command (see "Jump Command Operation," page 4-9)
	1	1	1	1	Minor Frame command (see "Minor Frame Operation," page 4-10)

BC/RT Control Word

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4.2.7 Halt Operation

You normally set the Halt Operation bit to logic 0 before writing to the Start register. In real-time (during BC execution), you can set this bit to logic 1. When operating on that particular message block's Control word, the board will halt transfer operations until the bit is reset to logic 0.

When the board detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status register (see "Control Register Definitions," page 4-18). You can use the Wait For Continue bit to find out when the board has arrived at the halted instruction block. When the board detects that you have reset the Halt bit (Continue Mode), the board will reset the Wait For Continue bit in the Message Status Register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* (as yet) been executed by the board.

NOTE The Halt operation can be used in conjunction with the Jump command described below (see "Jump Command Operation," below).

4.2.8 Skip Message Operation

The Skip Message command allows you to skip a message defined in a certain message block. To use Skip Message operation, modify the Command field in the Control word. This lets you selectively send a message in the current frame. The "skip" takes place immediately and does not wait until the Intermessage Gap Time expires.

4.2.9 Jump Command Operation

You can modify the board's BC transfer cycle by setting the Jump command in the BC Control word. The Jump command instructs the board to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 command word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the board has tested the Halt/Continue bit in the Control word. The "jump" takes place immediately and does not wait until the Intermessage Gap Time expires.

The memory structure of the jump command is illustrated in Figure 4-4 below.

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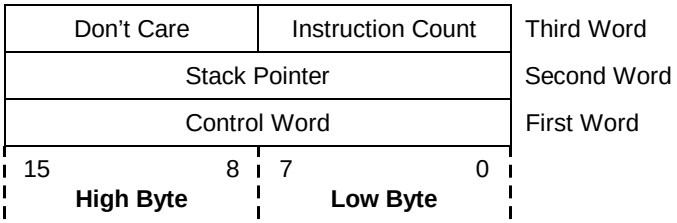


Figure 4-4. Jump Command Memory Structure

4.2.10 Minor Frame Operation

You can use the Minor Frame type of message in the following ways:

- To function as a "delay time" message between groups of messages.
- To produce a list of messages which will be sent out over the bus at different frequencies.

Minor frame time is defined as the time elapsed from the beginning of a minor frame to beginning of the next minor frame. To set up minor frame operation, you must begin each minor frame with a minor frame command (see "Minor Frame Time Register," and "Minor Frame Resolution Register," page 4-28). The maximum value possible for the Minor Frame Time is 16 sec.

The example in Figure 4-5 shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 msec. long, Message A is sent every 10 msec., Message B is sent every 20 msec., and Message C is sent every 40 msec.

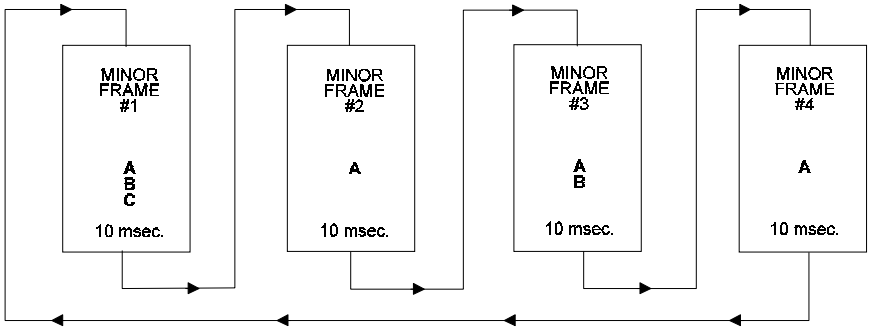


Figure 4-5. Minor Frame Sequencing

NOTE 1. The MINOR_FRAME message does not appear as a real message on the data bus.

2. Frame Time should not exceed the total time of all the minor frames in the minor frame sequence (see "Frame Time Register," page 4-27).

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4.2.11 Asynchronous Frame Operation

During standard operation the board sets up a frame of messages and then sends them out synchronously over the bus. You can set up multiple frames of messages, and select which one to send out.

Asynchronous Frame operation allows you to transmit a frame asynchronously, meaning that in the middle of the transmission of the messages of a frame (frame 1), you can transmit another frame (frame 2), and then return to continue transmitting the messages of the previous frame (frame 1).

To transmit an asynchronous frame, you must write the number of messages in the asynchronous frame into the Asynchronous Message Count register, place a pointer to the beginning of the asynchronous frame in the Asynchronous Frame Pointer register, and then set the Asynchronous Start Flag register to a non-zero value. This will send out the asynchronous frame over the bus (see “Asynchronous Start Flag Register,” “Asynchronous Frame Pointer Register,” “Asynchronous Message Count Register,” page 4-29).

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4.3 Remote Terminal Simulation

When the board is simulating both the Bus Controller and one or more Remote Terminals, you must write the simulated Remote Terminal 1553 Status word and Data word(s) into the message block in the sequence in which they are to be transmitted over the 1553 bus (see "Message Block Formats," page 4-13).

To indicate to the board which Remote Terminals are to be simulated, write to the 32- byte Active Remote Terminal table. Each entry in the 32-byte table corresponds to a specific Remote Terminal.

The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31 (for a total of 32 locations). A table entry value of 1 enables the Remote Terminal simulation by the board; a value of 0 disables the simulation by the board.

RT #31 Active RT byte	341F H
RT #30 Active RT byte	
• • •	
RT #0 Active RT byte	3400 H

Figure 4-6. Active RT Table—BC/Concurrent-RT Mode

Bit	Description
01-07	0
00	1 = Enabled; 0 = Disabled

Active RT Byte Definition—BC/Concurrent-RT Mode

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4.4 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire 1553 message as it appears on the 1553 bus, including Command word(s), Data word(s), and Status word(s).

Examples of Message block formats follow.

Example No. 1: Transmit Command Operating as BC Only

Block *before* execution

1553 Transmit Command	
Control Word	First Location In Block

Block *after* execution

1553 Data Word	From Transmitting Remote Terminal (Not Simulated)
•	•
•	•
1553 Data Word	•
RT Status Word	From Transmitting Remote Terminal (Not Simulated)
1553 Transmit Command	
Control Word	First Location In Block

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Example No. 2: Receive Command Operating as Both BC and Receiving RT

Block *before* execution

RT Status Word	Simulated By EXC-1553PCI/EP (Loaded by User)
1553 Data Word	•
•	•
•	•
1553 Data Word	Simulated By EXC-1553PCI/EP (Loaded by User)
1553 Receive Command	
Control Word	First Location In Block

Block *after* execution

RT Status Word
1553 Data Word
•
•
1553 Data Word
1553 Receive Command
Control Word

First Location In Block

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Example No. 3: RT-to-RT Command Operating as BC and Receiving RT

Block *before* execution

(Receive) RT Status Word	Simulated By EXC-1553PCI/EP (Loaded By User)
Leave Empty For Data +N	
•	
•	
Leave Empty For Data #1	
Leave Empty For (Transmit) RT Status Word	
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location In Block

Block *after* execution

(Receive) RT Status Word	
1553 Data Word	From Transmitting Remote Terminal (Not Simulated)
•	•
•	•
1553 Data Word	•
(Transmit) RT Status Word	From Transmitting Remote Terminal (Not Simulated)
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location In Block

4.5 Continuous or One-Shot Message Transfers

The board can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

In One-Shot mode, (after receiving a Start command) the board transfers all messages, sets the Message Complete bit in the Message Status register, issues an interrupt (if programmed), and waits for a new Start command. Use the Start register (see "Start Register," page 4-21) to select One-Shot mode.

In n-Times mode, load the Loop Count register with the number of times to transmit the messages (frame) and set the Loop and Start bits in the Start register. You can transmit 1–255 times (see "Start Register," page 4-21 and "Loop Count Register," page 4-24). The time between frames is determined by the Frame Time register (see "Frame Time Register," page 4-27).

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In Continuous Loop mode, the board will retransmit the message frame at a predetermined, user-programmable rate. Use the Start register and the Loop Count register (see "Start Register," page 4-21 and "Loop Count Register," page 4-24) to select Continuous Loop mode. In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the board's operation (see "Start Register," page 4-21).

The Loop time or Frame time is a function of two control registers: the Frame Time register and the Frame Time Resolution register. The internal Frame Time counter is loaded when a Start command with the 16-bit value found in the Frame Time register is received. The Frame Time Counter is decremented every *n* x 155 nsec., where *n* is the value of Frame Time Resolution register. After all instructions are executed (1 frame), the board waits until the internal Frame Time counter reaches 0 before transmitting the next frame.

NOTE If the Frame time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 20 µsec, measured as dead time on the bus.

You can implement the desired Frame time by programming the appropriate combinations of the two registers. An example using one method is described below.

Example Calculating Frame Time

Given: Frame time of 500 msec. is required.

Method:

Select Frame Time Resolution of 3225 (Dec) → 0C99 (H)

Frame Time Resolution = 3225 x 155 nsec = 500 µsec (.5 msec)

Subsequently, the Frame Time register value must be equal to:

$$\frac{[500\ \text{msec (desired time)} \ /\ .5\ \text{msec} = 1000\ \text{(Dec)}] - 1}{\text{Count} - 1} \rightarrow 03E7\ \text{(H)}$$

Before issuing the Start command, set:

- Frame Time register = 03E7 (H)
- Frame Time Resolution register = 0C99 (H)

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4.5.1 Mode Codes

The board handles all dual-redundant 1553B Mode codes; the Word Count field is decoded according to MIL-STD-1553B. The two Quad-Redundant Mode codes, Selected Transmitter Shutdown and Override Selected Transmitter Shutdown, are not implemented by the board.

4.6 Program Example—BC/Concurrent-RT Mode

NOTE All values are in HEX unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,04`	Set Configuration register to BC/RT mode.
`20 POKE &H3FF0,00`	Set Stack Pointer registers to 0000.
`30 POKE &H3FF1,00`	(stack now begins at address: 0000)
`40 POKE &H3FF2,&HFF`	Set Variable Amplitude register.
`50 POKE &H00,00`	Pointer to first message:
`60 POKE &H01,01`	[Location of message is 0100 (H)]
`70 POKE &H02,xx`	Set Intermessage Gap Time location.
`80 POKE &H03,xx`	
`90 POKE &H08,&H40`	Pointer to second message:
`100 POKE &H09,01`	[Location of message is 0140 (H)]
`110 POKE &H0A,xx`	Set Intermessage Gap Time location.
`120 POKE &H0B,xx`	
`130 POKE &H100,&H80`	Set Control word to Transmit command,
`140 POKE &H101,00`	Bus A, and no errors injected.
`150 POKE &H102,&H23`	Set Command word to 0C23.
`160 POKE &H103,&H0C`	
`170 POKE &H104,&H00`	Set Status word to 0800.
`180 POKE &H105,&H08`	
`190 POKE &H106,&Hxx`	Set Data word to xxxx.
`200 POKE &H107,&Hxx`	
`210 POKE &H108,&Hyy`	Set Data word to yyyy.
`220 POKE &H109,&Hyy`	
`230 POKE &H10a,&Hzz`	Set Data word to zzzz.
`240 POKE &H10b,&Hzz`	

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BASIC Instruction	Remarks
`250 POKE &H140,02`	Set Control word to RT-to-RT command,
`260 POKE &H141,00`	Bus B, and no errors injected.
`270 POKE &H142,&H23`	Set first (Receive) command word to 3823H.
`280 POKE &H143,&H38`	
`290 POKE &H144,&H43`	Set second (Transmit) command word to 1C43H.
`300 POKE &H145,&H1C`	
`310 POKE &H3FEB,2`	Set Instruction Counter to 2 (i.e., 2 messages)
`320 POKE &H3FEC,xx`	Set Frame Time Resolution registers.
`330 POKE &H3FED,xx`	
`340 POKE &H3FEE,xx`	Set Frame Time registers
`350 POKE &H3FEF,XX`	
`360 POKE &H3401,1`	Enable RT #1. Use the Active RT's look-up table to enable RTs. Board will simulate enabled RTs.
`370 POKE &H3FFC,1`	Set Start register to 1. Starts message transfers in One-Shot mode.
`380 STOP`	

4.7 Control Register Definitions

4.7.1 Concurrent Start Register

Address: 7005 (H) WRITE

Set the Concurrent Start register to start the operation of Channel 1 and Channel 2 (if present), simultaneously. Starting both channels simultaneously assures that they will be synchronized.

When using the Concurrent Start Register, the standard Start registers of the dual-port RAM must be set to logic 0.

To stop the selected operation(s), follow the normal procedure described under the respective Start register.

NOTE A concurrent start can also be achieved by sending a low TTL pulse of 100 nsec. minimum to the EXSTART$ pin (see "Connectors," page 7-7).

Bit	Description
00-07	X (Don't Care)

Concurrent Start Register

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4.7.2 Global Software Reset Register **Address: 7002 (H)**

Set the Global Software Reset register to reset both Channel 1 and Channel 2 (if EXC-1553PCI/EPM(I) option present), simultaneously (data field = don't care).

NOTE Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation is completed.

4.7.3 Interrupt Reset Register **Address: 7001 (H)**

To reset the Interrupt signal generated by Channel 1, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

4.7.4 Software Reset Register **Address: 7000 (H)**

Write to the Software Reset register to reset Channel 1 (data field = don't care). The bank will act as if power had been switched OFF, then ON. The Board status, the Board ID, Firmware revision and Variable Amplitude registers are written by the board after the reset operation has been completed.

WARNING *Reset erases all memory locations in the dual-port RAM.*

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4.7.5 Board Configuration Register

Address: 3FFF (H)

Before issuing a Start command to the board, set the operating mode of the board via the Board Configuration register. To modify the Board Configuration register, issue a Stop command, write one of the hex values to the register (see the table below), then issue a Start command (see "Start Register," page 4-21).

Hex Value	Operating Mode
01	BC Mode
02	RT Mode
04	**BC/Concurrent-RT Mode**
08	BM Sequential Block Mode
10	BM Sequential Link List
20	BM Look-Up Table Mode
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix C, "Internal Loop Back Test," page 9-4).
FF	External Loop Test (see Appendix D, "External Loop Back Test," page 9-5).

Board Configuration Register Values—BC/RT Mode

4.7.6 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value "E".

4.7.7 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

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Bit	Description
07	1 = Board Type is EXC-1553PCI/EP
06	X (Don't Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

4.7.8 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the board. Writing the appropriate bit (bit 00) to the Start register starts the Bus Controller transfer operation. When operating in Continuous Loop or *n*-Times mode, you must set the Start and Loop bits in the Start register. The Loop and *n*-Times number are selected via the Loop Count register. In the One-Shot and *n*-Times modes, the board resets the Start bit in the register after *all* messages have been transferred. The board does not reset any bit while in Continuous Loop mode. To halt the Loop operation between messages, set bit 00 to 0. In order to halt the operation at the end of the entire frame, set bit 02 to 0 (bit 02 is not tested between message transfers). Related data bit 04 in the Board Status register indicates when the board has been halted (see "Board Status Register").

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Bit	Description
03-07	0
02	1 = Loop Mode 0 = One-Shot Mode
01	0
00	1 = Start Operation 0 = Stop Operation

Start Register

4.7.9 Interrupt Condition Register

Address: 3FFB (H)

The Interrupt Condition register allows you to set interrupt triggers. When a condition that is enabled in this register occurs, an interrupt is generated. To determine which condition caused the interrupt, check the Message Status register.

You must set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command (see “Start Register,” page 4-21).

NOTE The interrupt will be sent at the end of the message for all interrupt conditions.

Bit	Description
04-07	0
03	1 = Message Error
02	1 = End Of Frame
01	1 = Message Complete
00	0

Interrupt Condition Register

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4.7.10 Message Status Register

Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. The definition of each status bit is given below.

Bit	Bit Name	Description
04-07	**0**	
03	**Message Error**	1 = The message has been sent. As a result, the Error bit has been set in the Message Status word.
02	**End Of Frame**	1 = The last word of the last message in the frame has been sent.
01	**Message Complete**	1 = The last word of the message has been sent.
00	**Wait For Continue**	1 = A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue.

Message Status Register

NOTE Status bits are *not* reset by the board. After reading them, you must reset them.

4.7.11 RT Response Time Register

Address: 3FF9 (H)

The RT Response Time register sets the Remote Terminal's Response Time. The resolution of the Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 4 µsec. The value in the register is added to the minimum time. The actual Response Time has a tolerance of ±1 µsec.

You must set the Response Time register before issuing a Start command to the board. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 4-21).

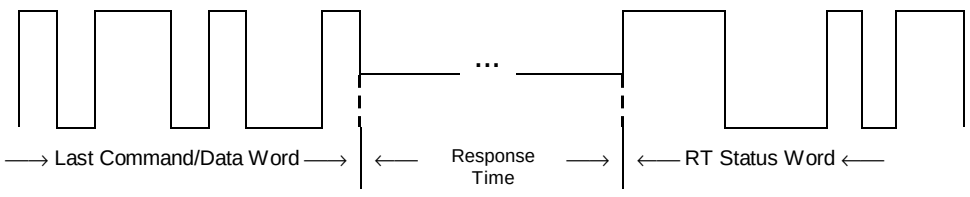


Figure 4-7. RT Response Time Definition

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Example Setting the RT Response Time Register

To request a response time of 9 µsec:

Write 32 to the RT Response Time register.

32 x 0.155 ≅ 5 µsec + 4 µsec = 9 µsec.

4.7.12 Loop Count Register

Address: 3FF6 (H)

The Loop Count register is used in conjunction with the Loop bit in the Start register. If the Loop bit in the Start register is set, then set the Loop Count register to specify the number of times the Message frame will be transmitted. A value of zero is interpreted as a request for continuous looping. You must set the Loop Counter register before issuing a Start command to the board. To modify the Loop Counter register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 4-21).

Bit	Value	Description
00-07	**0**	Transmits in Continuous Loop.
	1–255	Sends Message Frame *n*-times (1–255) as defined.

Loop Count Register

4.7.13 Bit Count Register

Address: 3FF5 (H)

The Bit Count register sets the total number of bits in the 1553 word, including Sync(3) and Parity(1). This register is used by the board only for messages for which the Bit Count Error bit is set in the Control Word of the Message Block (see "Control Word," page 4-8). If the Bit Count Error bit is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

You must set the Bit Count register before issuing a Start command to the board. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 4-21).

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Bit	Description			
03–07	0			
00–02	Bit 02	Bit 01	Bit 00	No. of 1553 bits sent per word
	0	0	0	17 (-3)
	0	0	1	18 (-2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	22 (+2)
	1	1	0	23 (+3)

Bit Count Register

4.7.14 Word Count Register

Address: 3FF4 (H)

The Word Count register controls the number of 1553 data words (± 3) in the message and allows you to inject a Word Count error. The error is an offset relative to the 1553 command word Word Count field. This register is used by the board only for messages for which the Word Count Error bit is set in the Control word register (see “Control Word,” page 4-8). If the Word Count Error bit is not set, a correct number of words is transmitted regardless of the contents of the Word Count register.

You must set the Word Count register before issuing a Start command to the board. To modify the Word Count register, issue a Stop command, modify the register, and then issue a Start command (see “Start Register,” page 4-21).

Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Register Values

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4.7.15 BC Response Time Register

Address: 3FF3 (H)

The BC Response Time register sets the BC's Response Time window, whose value determines the maximum (wait) time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time register is 155 nsec. per bit, measured as the dead time on the 1553 bus. The minimum time is approximately 2 µsec.

You must set the BC Response Time register before issuing a Start command to the board. To modify the BC Response Time register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 4-21).

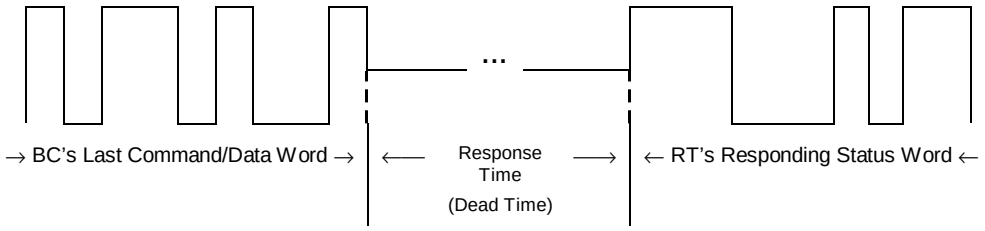


Figure 4-8. BC Response Time Definition

Example Setting the BC Response Time Register

To set up a BC response time of 14 µsec:

Write 90 to the BC Response Time register.

90 x 0.155 ≅ 14 µsec

4.7.16 Variable Amplitude Register

Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.5 volts (peak-to-peak) when measured on the 1553 bus using 1553 direct coupling and 35-ohm load (that is, two 70-ohm termination resistors). If 78-ohm termination resistors are used, a higher transmit (output) amplitude will appear on the 1553 bus. The Variable Amplitude register has a resolution of 30 mV/bit (p-p) on the bus.

You must set the Variable Amplitude register before issuing a Start command to the board. To modify the Variable Amplitude register, issue a Stop command, modify the register, and then issue a Start command (see "Start Register," page 4-21). After a reset, the Variable Amplitude register defaults to FFH, providing maximum amplitude.

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4.7.17 Stack Pointer

Address: 3FF0 (H)

The Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 (H) and 33FF (H). You must set the Stack Pointer register before issuing a Start command to the board. To modify the Stack Pointer register, issue a Stop command, modify the register, then issue a Start command (see “Start Register,” page 4-21).

4.7.18 Frame Time Register

Address: 3FEE (H)

The Frame Time register contains the 16-bit Frame Time value for Continuous and *n*-Times modes operation. The value written to the Frame Time register is multiplied by the value set in the Frame Time Resolution register described below. The value set must equal the desired multiplication factor – 1 (see “Calculating Frame Time,” page 4-16).

You must set the Frame Time register before issuing a Start command to the board. To modify the Frame Time register, issue a Stop command, modify the register, then issue a Start command (see “Start Register,” page 4-21).

4.7.19 Frame Time Resolution Register

Address: 3FEC (H)

The 16-bit Frame Time Resolution value represents the resolution of the Frame Time counter in increments of 155 nsec. (see also “Continuous or One-Shot Message Transfers,” page 4-15).

You must set the Frame Time Resolution register before issuing a Start command to the board. For an example of how to calculate Frame Time and Frame Time Resolution, see “Calculating Frame Time,” page 4-16. To modify the Frame Time Resolution register, issue a Stop command, modify the register, then issue a Start command (see “Start Register,” page 4-21).

4.7.20 Instruction Counter

Address: 3FEB (H)

The Instruction Counter must be loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than 0 before you write to the Start register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The board updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

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You must set the Instruction Counter register before issuing a Start command to the board. To modify the Instruction Counter register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 4-21). When in the Continuous Loop mode, the Instruction Counter register cycles from the initial value down to 1.

4.7.21 Minor Frame Time Register

Address: 3FE8 (H) WRITE

The 16-bit Minor Frame Time register is used to set the length of a single minor frame (see "Minor Frame Operation," page 4-10). The resolution of the Minor Frame Time register is 1 µsec. per bit. The maximum value is approximately 65 msec., which can be extended by the multiplier set in the Minor Frame Time Resolution register described below.

You must set the Minor Frame Time register before issuing a Start command to the board. To modify the Minor Frame Time register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 4-21).

4.7.22 Minor Frame Resolution Register

Address: 3FE6 (H) WRITE

The 8-bit Minor Frame Resolution is a multiplier of the Minor Frame Time described above. The value you write to the Minor Frame Resolution register allows you to extend the Minor Frame Time beyond the 65 msec. maximum in the Minor Frame Time register. The maximum Minor Frame Resolution is 255. The maximum Minor Frame Time possible using both registers is approximately 16 sec.

Example To generate a Minor Frame Time of 1 sec., set the Minor Frame Time register to F424 (H) (62,500 Dec.), and set the Minor Frame Resolution register to 10 (H) (16 Dec.).

You must set the Minor Frame Time Resolution register before issuing a Start command to the board. To modify the Minor Frame Time Resolution register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 4-21).

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4.7.23 Board Options Register

Address: 3E84 (H) READ ONLY

The Board Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

Bit	Description
10–15	Reserved
09	1 = 1760
08	1 = 1553
00–07	Reserved

Board Options Register

4.7.24 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.

4.7.25 Asynchronous Start Flag Register

Address: 3424 (H) WRITE

Write a 1 to the Asynchronous Start Flag register to indicate that it is now time to send a selected frame asynchronously. The card will automatically reset this value to 0 when it sends the frame.

4.7.26 Asynchronous Frame Pointer Register

Address: 3422 (H) WRITE

The Asynchronous Frame Pointer register points to the beginning of the selected frame that you scheduled to send asynchronously.

4.7.27 Asynchronous Message Count Register

Address: 3420 (H) WRITE

Write to the Asynchronous Message Count register to set how many messages to send, when sending the asynchronous frame over the data bus. The maximum number of messages allowed in a frame is determined by the amount of available space in the message stack area of the card and the size of the individual messages.

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5 Bus Monitor Operation

Chapter 5 describes EXC-1553PCI/EP operation in Bus Monitor mode. The following topics are covered:

- "Sequential Fixed-Block Memory Map," page 5-3
- "Sequential Link-List Memory Map," page 5-4
- "Sequential Mode Message Block Area," page 5-5
- "Look-Up Table Mode Memory Map," page 5-8
- "Look-Up Table," page 5-9
- "Look-Up Table Mode Message Block Area," page 5-11
- "Message Status Word," page 5-12
- "Time Tag Value," page 5-13
- "Trigger Operation," page 5-14
- "Program Examples—BM Mode," page 5-18
- "Control Register Definitions," page 5-19

The Bus Monitor can operate in one of two modes:

Sequential mode—1553 Message blocks are stored in sequential locations in memory. Sequential mode supports two types of operations:

Fixed-Block operation—1553 messages are stored at fixed sequential blocks in the memory. Sequential Fixed-Block mode supports Trigger capability.

Link-List operation—1553 messages are packed one after another in the memory, separated by a header.

Look-Up Table mode—Each 1553 message is stored in a unique Message block. In Look-Up Table mode, the board addresses the user-programmable look-up table when it receives a 1553 Command word. The Command word's RT address, T/R bit, and Subaddress fields make up the 11-bit pointer to a Look-Up table with 2048 (2K x 8) locations.

Use the Board Configuration register ("Board Configuration Register," page 5-22) to program the desired mode of operation.

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NOTE The operation of the non-concurrent bus monitor and the concurrent-monitor found on the board are identical and both provide a user selectable 16- or 32-bit time tag (selected via a unique DIP switch on the board). The memory for each monitor, however, resides in its own memory page (see "Concurrent Monitor Option," page 5-29).

Perform the following procedure after a power-up or a software reset.

To determine whether the board is installed and ready to operate:

1. Check the Board ID register (test for value = 45 H).
2. Check the Board Status register (test for Board Ready bit = 1).

The board is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the (software) Board Reset register.

NOTE Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

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5.1 Sequential Fixed-Block Memory Map

Time Tag Counter Byte 3	700E H
Time Tag Counter Byte 2	700C H
Time Tag Counter Byte 1	700A H
Time Tag Counter Byte 0	7008 H
Time Tag Reset Register	7007 H
Time Tag Options Register	7006 H
Concurrent Start Register	7005 H
Monitor Options Register	7004 H
Global Software Reset Register	7002 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Reserved	4000–6FFF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF7–3FF9 H
Time Tag Resolution Register	3FF6 H
Message Counter	3FF5 H
Counter Trigger Register	3FF4 H

Trigger Word #1 Register	3FF2 H
Trigger Mask #1 Register	3FF0 H
Trigger Word #2 Register	3FEE H
Trigger Mask #2 Register	3FEC H
Trigger Control Register	3FEB H
Mode Code Control Register	3FEA H
Broadcast Control Register	3FE8 H
Reserved	3E86–3FE7 H
Board Options Register (16 bits)	3E84 H
Reserved	3E81–3E83 H
Firmware Revision Register	3E80 H
Message Block Area (200 Blocks)	0000–3EF7 H

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Figure 5-1. BM—Sequential Fixed-Block Memory Map

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5.2 Sequential Link-List Memory Map

Time Tag Counter Byte 3	700E H
Time Tag Counter Byte 2	700C H
Time Tag Counter Byte 1	700A H
Time Tag Counter Byte 0	7008 H
Time Tag Reset Register	7007 H
Time Tag Options Register	7006 H
Concurrent Start Register	7005 H
Monitor Options Register	7004 H
Global Software Reset Register	7002 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Reserved	4000–6FFF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF7–3FF9 H
Time Tag Resolution Register	3FF6 H
End Buffer Pointer	3FF4 H

Next Message Pointer	3FF2 H
Reserved	3FEB–3FF1 H
Mode Code Control Register	3FEA H
Broadcast Control Register	3FE8 H
Reserved	3E86–3FE7 H
Board Options Register (16 bits)	3E84 H
Reserved	3E81–3E83 H
Firmware Revision Register	3E80 H
Message Block Spill Area	3E00–3E7F H
Message Block Area	0000–3DFF H

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Figure 5-2. BM—Sequential Link-List Memory Map

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5.3 Sequential Mode Message Block Area

The Sequential Mode Message Block area is partitioned into either blocks of fixed length or into a link list of blocks of varying lengths. The type of partitioning is determined by the Board Configuration register (see “Board Configuration Register,” page 5-22).

For a description of the 16 and 32-bit Time Tag function, see “Time Tag,” page 5-13, and “Board Configuration DIP Switch (SW1),” page 7-4.

5.3.1 Message Block Fixed-Block Operation

In Fixed-Block operation, the Message Block area is divided into 200 blocks of 80 bytes each. The first block starts at address 0000 (H), the second at 0050 (H), the third at 00A0 (H), etc. The Trigger option can be used only in Sequential mode with Fixed-Block operation (see “Trigger Operation,” page 5-14).

BUS MONITOR MESSAGE BLOCK—FIXED-BLOCK OPERATION

16-Bit Time Tag Mode

	Information is stored in the memory in the following sequence:	**Byte Offset**
1553 Data Word	•	•
•	•	•
•	•	•
1553 Data Word	1553 Data Words	•
1553 Command Word	1553 Command Word—High	**5**
Time Tag Word	1553 Command Word—Low	**4**
Message Status Word	Time Tag Word—High	**3**
	Time Tag Word—Low	**2**
	Message Status Word—High	**1**
	Message Status Word—Low	**0**

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BUS MONITOR MESSAGE BLOCK—FIXED-BLOCK OPERATION

32-Bit Time Tag Mode

	Information is stored in the memory in the following sequence:	Byte Offset
1553 Data Word	•	•
•	•	•
•	•	•
1553 Data Word	1553 Data Words	•
1553 Command Word	1553 Command Word—High	7
Time Tag Word #2 (MSB)	1553 Command Word—Low	6
Time Tag Word #1 (LSB)	Time Tag Word #2—High	5
Message Status Word	Time Tag Word #2—Low	4
	Time Tag Word #1—High	3
	Time Tag Word #1—Low	2
	Message Status Word—High	1
	Message Status Word—Low	0

5.3.2 Message Block Link-List Operation

In Link-List operation, the Message Block area is divided into a linked list of message blocks. The length of each message block varies according to message size. The first two locations in each message comprise the message header. This header contains the address of the next Message Block header. The header of the last 1553 block received contains XXFF (End of File), indicating that there are no more messages stored. After a message is processed and stored in memory, the header of the preceding message block is updated from XXFF to the address (of the header in the block) of the newly stored message.

The Link-List method can store more data than Fixed-Block operation.

Take special care with the last message in the Message Block area. Since the buffer never wraps around in the middle of a message and a message may start at any address up to 3DFE (H), the final message in the buffer may extend past the end of the standard Message Block area into the Message Block Spill area. The End Buffer pointer (“End Buffer Pointer,” page 5-27) exists for this special case. The End Buffer pointer points to the address after the last location of the message, indicating the length of the message. The next message will start at the first location of the Message Block area (0000 H).

The following figures illustrate the contents of the Message block. For a description of the 16 and 32-bit Time Tag function, see “Time Tag,” page 5-13, and “Board Configuration DIP Switch (SW1),” page 7-4.

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BUS MONITOR MESSAGE BLOCK—LINK-LIST OPERATION

16-Bit Time Tag Mode

	Information is stored in the memory in the following sequence:	**Byte Offset**
End Of File: XXFF	End Of File—High: XX	**n+1**
1553 Data Word	End Of File—Low: FF	**n**
•	1553 Data Words	
•	•	•
1553 Data Word	•	•
1553 Command Word	•	•
Time Tag Word	1553 Data Words	•
Message Status Word	Time Tag Word—High	**5**
Message Header - Address of Next Block	Time Tag Word—Low	**4**
	Message Status Word—High	**3**
	Message Status Word—Low	**2**
	Message Header—High	**1**
	Message Header—Low	**0**

32-Bit Time Tag Mode

	Information is stored in the memory in the following sequence:	**Byte Offset**
End Of File: XXFF	End Of File—High: XX	**n+1**
1553 Data Word	End Of File—Low: FF	**n**
•	1553 Data Words	
•	•	•
1553 Data Word	•	•
1553 Command Word	•	•
Time Tag Word #2 (MSB)	1553 Data Words	•
Time Tag Word #1 (LSB)	Time Tag Word #2—High	**7**
Message Status Word	Time Tag Word #2—Low	**6**
Message Header - Address of Next Block	Time Tag Word #1—High	**5**
	Time Tag Word #1—Low	**4**
	Message Status Word—High	**3**
	Message Status Word—Low	**2**
	Message Header—High	**1**
	Message Header—Low	**0**

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5.4 Look-Up Table Mode Memory Map

Time Tag Counter Byte 3	700E H
Time Tag Counter Byte 2	700C H
Time Tag Counter Byte 1	700A H
Time Tag Counter Byte 0	7008 H
Time Tag Reset Register	7007 H
Time Tag Options Register	7006 H
Concurrent Start Register	7005 H
Monitor Options Register	7004 H
Global Software Reset Register	7002 H
Interrupt Reset Register	7001 H
Software Reset Register	7000 H
Data Block Look-Up Table (2K x 8)	4000–47FF H
Board Configuration Register	3FFF H
Board ID Register	3FFE H
Board Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
Reserved	3FF7–3FF9 H
Time Tag Resolution Register	3FF6 H

(continued in next column ↗)

Reserved	3FF3–3FF5 H
Last Block Register	3FF2 H
Reserved	3FEB–3FF1 H
Mode Code Control Register	3FEA H
Broadcast Control Register	3FE8 H
Reserved	3E86–3FE7 H
Board Options Register (16 bits)	3E84 H
Reserved	3E81–3E83 H
Firmware Revision Register	3E80 H
Reserved	2800–3E7F H
Message Block Area (128 Blocks)	0000–27FF H

Figure 5-3. BM—Look-Up Table Mode Memory Map

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5.5 Look-Up Table Mode

In Look-Up Table mode, the board can store 128 unique messages by using a 2K × 8 look-up table in on-board memory. Each (table) byte is divided into a 7-bit block number and an Interrupt Select bit, as described below. Data Block numbers (0-127 decimal) each consisting of 80 bytes are loaded into the table. The first block starts at address 0, the second at 50 (H), etc. Set the Interrupt Select bit to specify which messages will set the interrupt flag. The Interrupt Condition register must also be programmed.

Bit	Description
07	1 = Interrupt Select Bit is Enabled
00-06	Block Numbers (0-127)

Look-Up Table Byte Structure

When a 1553 message is received, the Command word's RT address, T/R Bit, and Subaddress fields are used as an 11-bit index to the look-up table. This index is used to extract the Data block number from the look-up table.

	(11 most significant bits of the 1553 command word)					
Base Address	(5 bits) **RT address**	(1 bit) **T/R**	(5 bits) **Sub-address**	**Look-up table (2K x 8)**	**Data block**	**Hex address of data block**
4000+	11111	1	11111	Block #	Data Block 127	27B0
	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
4000+	00000	0	00001	Block #	Data Block 3	00F0
4000+	00000	0	00001	Block #	Data Block 2	00A0
4000+	00000	0	00001	Block #	Data Block 1	0050
4000+	00000	0	00000	Block #	Data Block 0	0000

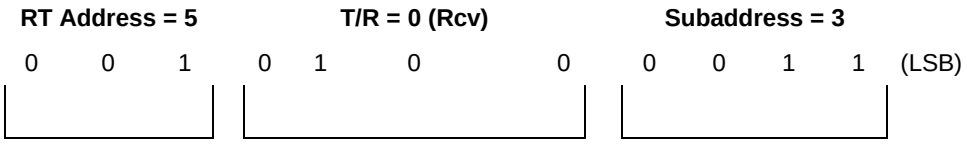
Figure 5-4. Look-Up Table

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To create the address to the table:

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example To allocate a data block for a 1553 receive message to RT#5, Subaddress #3.



Hex representation = 143

2. Add the hex value of this part of the command word to the base address of the look-up table (4000 H).

```
  4000  (H)
+ 143   (H)
------------
  4143  (H)
```

3. Write the Data Block number to this location.

Example `POKE &H4143,XX` writes an 8-bit Block Number value to the look-up table address &H4143. Each data block, beginning at address 0000 is 128 bytes long (for up to 32 1553 data words). The address of a block is obtained by multiplying its block number by 50 (H).

The block addresses are calculated as follows:

- Block 0 is located at location 0000 (H).
- Block 1 is located at location 0050 (H).
- The location of the block is obtained by multiplying the block number by 50 (H).

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5.6 Look-Up Table Mode Message Block Area

BUS MONITOR MESSAGE BLOCK—LOOK-UP TABLE MODE

16-Bit Time Tag Mode

	Information is stored in the memory in the following sequence:	**Byte Offset**
1553 Data Word	•	•
•	•	•
•	•	•
1553 Data Word	1553 Data Words	•
1553 Command Word	1553 Command Word—High	**5**
Time Tag Word	1553 Command Word—Low	**4**
Message Status Word	Time Tag Word—High	**3**
	Time Tag Word—Low	**2**
	Message Status Word—High	**1**
	Message Status Word—Low	**0**

32-Bit Time Tag Mode

	Information is stored in the memory in the following sequence:	**Byte Offset**
1553 Data Word	•	•
•	•	•
•	•	•
1553 Data Word	1553 Data Words	•
1553 Command Word	1553 Command Word—High	**7**
Time Tag Word #2 (MSB)	1553 Command Word—Low	**6**
Time Tag Word #1 (LSB)	Time Tag Word #2—High	**5**
Message Status Word	Time Tag Word #2—Low	**4**
	Time Tag Word #1—High	**3**
	Time Tag Word #1—Low	**2**
	Message Status Word—High	**1**
	Message Status Word—Low	**0**

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5.7 Message Status Word

The Message Status word is identical for all Bus Monitor modes. The Message Status word indicates the status of the message transfer. This word is created by the board. Do not confuse it with the 1553 Status word (see "1553 RT Status Words," page 3-7). The contents of the Message Status word are described below.

NOTE A logic 1 indicates the occurrence of a status flag.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed.
14	**Trigger Found**	Trigger message was received and stored. This status is valid for Sequential Fixed-Block mode with the following modes: **Store After** mode—the Trigger Found bit will be set only in the *first* Trigger message. **Store Only** mode—the Trigger Found bit will be set in *every* Trigger message. (see "Trigger Operation," page 5-14)
13	**RT-RT**	RT-to-RT message was received.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit other than the Message Error bit in the RT Status word was set. The Error Bit is *not* set in conjunction with this bit.
10	**Invalid Message**	1553 message-level error occurred (Word Count, Incorrect Sync, etc.). Examine the other bits in this table to determine which error occurred.
09	**Reserved**	Set to 0
08	**Bus A/B**	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	Received 1553 Status word did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the command or the data word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Response Time Error**	Response Time error occurred in the message.
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word

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5.8 Time Tag Value

In all Bus Monitor modes, each incoming message has a Time Tag value. The Time Tag value is a 16- or 32-bit word used to determine the time elapsed since the Start command was issued or the time between 1553 messages. To select 16- or 32-bit Time Tag mode, use the dedicated DIP Switch (see “DIP Switches,” page 7-4). The Time Tag implementation uses a 32-bit, free-running counter whose resolution is fixed at 4 µsec. per bit in 16-bit mode, and is programmable in 32-bit mode (see “Time Tag Resolution Register,” page 5-26). You can reset the Time Tag counter (to 0) any time by writing to the Time Tag Reset register (see “Control Register Definitions,” page 5-19).

The Time Tag counter's value is written to the dual-port RAM during the reception of the (first) command of each message. In 16-bit mode, only the counter's 16 lower bits are written to the dual-port RAM.

NOTE 1. You can also read the counter's value any time at the Time Tag Counter addresses.

2. The counter can also be clocked and/or reset from external source (see EXTTCLKx and EXTTRSTx$ pins in “Connectors,” page 7-7).

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5.9 Trigger Operation

Only Sequential Fixed-Block mode supports triggers.

A trigger is a filter you can set to tell the board when and how to store 1553 messages. The board can be programmed to store messages in the following ways:

Store All—stores all 1553 messages, without regard to triggers; no triggers are active

Store Only—stores only messages which meet the trigger condition

Store After—stores only the trigger message and messages that come after the trigger message

You can define up to two triggers. Each trigger is defined using two registers:

- Trigger Word register
- Trigger Mask register

Use the **Trigger Word register** to define a particular 1553 Command word or a Message Status word as a trigger. For example, you can use the Message Status word as the trigger source to store all messages on bus A, only messages with errors, or messages with errors received over bus B, etc. (see “Trigger Word Registers,” page 5-15).

The **Trigger Mask register** defines which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored (“don’t care”). The Trigger Mask registers must be defined when using the trigger function (see “Trigger Mask Registers,” page 5-16.)

Set the **Trigger Control register** to specify the following trigger conditions (see “Trigger Control Register,” page 5-17):

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

You must set these registers—Trigger Word, Trigger Mask and Trigger Control—before issuing a Start command to the board. To modify these registers, set the Initialize bit in the Start register to 10 (H), modify the Trigger Word, Trigger Mask and Trigger Control registers, then issue a Start command (81 H).

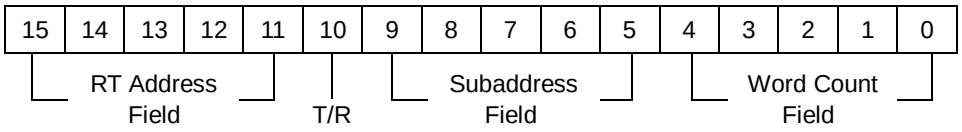
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5.9.1 Trigger Word Registers (1 and 2) **Address: 3FF2, 3FFE (H)**

Use the Trigger Word register to define a particular 1553 Command word or a Message Status word as a trigger. Load these locations (illustrated below) with the desired 1553 Command word or Message Status word, which will be used as the trigger source. You must also define the Trigger Mask Registers when using the trigger function (see "Trigger Mask Registers," page 5-16). You can define which trigger is active (Trigger #1, Trigger #2, or both) via the Trigger Control Register (see "Trigger Control Register," page 5-17).

Using the 1553 Command Word—Trigger Word Registers

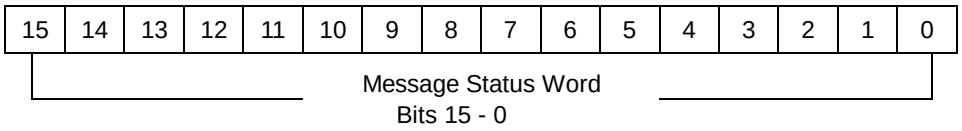
Use a 1553 Command word as a trigger when you want to filter messages based on information found in the Command word. For example, if you want to filter messages from a particular RT, or with a particular word count, set the Trigger Word register with those parameters defined in the 1553 Command word.



Using the Message Status Word—Trigger Word Registers

Use a Message Status word as a trigger when you want to filter messages based on information found in the Message Status word. Do not confuse the Message Status word with the 1553 Status word (see "1553 RT Status Words," page 3-7). For example, if you want to filter messages transferred over bus A (vs. bus B), or error messages, set the Trigger Word register with those parameters defined in the Message Status word.

For an explanation of the Message Status word, see page 5-12.



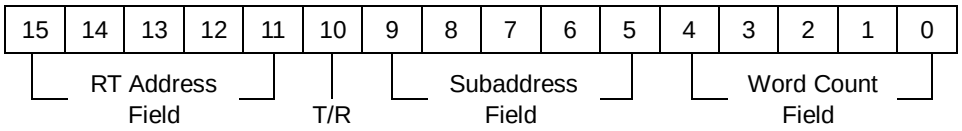
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5.9.2 Trigger Mask Registers (1 and 2) **Address: 3FF0, 3FEC (H)**

Set the Trigger Mask register to define which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored ("don't care"). You must define the Trigger Mask registers when using the trigger function. All bits in this register should be set to 1, except for those bits you want to be "don't care" in the incoming Command word or Message Status word.

Using the 1553 Command Word—Trigger Mask Registers

After setting the Trigger Word register with a 1553 Command word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the 1553 Command word trigger.



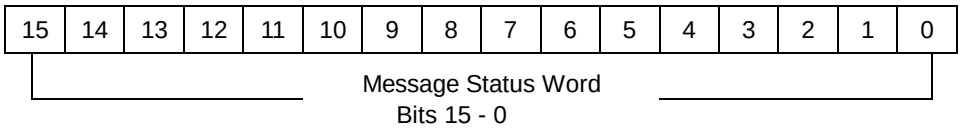
1 = Trigger on corresponding bit value in Trigger Word Register

0 = Corresponding bit value in Trigger Word Register is "Don't Care"

Using the Message Status Word—Trigger Mask Registers

After setting the Trigger Word register with a Message Status word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the Message Status word trigger.

For an explanation of the Message Status word, see page 5-12.



1 = Trigger on corresponding bit value in Trigger Word Register

0 = Corresponding bit value in Trigger Word Register is "Don't Care"

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5.9.3 Trigger Control Register

Address: 3FEB (H)

The Trigger Control register is relevant only in Sequential Fixed-Block mode. Set the Trigger Control register to specify the following trigger conditions:

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

NOTE Logic 1 enables the function.

Bit	Description
07	Trigger Source: 0 = 1553 Command Word 1 = Message Status Word
05-06	Reserved
04	1 = Store After
03	1 = Store Only
02	1 = Store All
01	1 = Enable Trigger Word #2
00	1 = Enable Trigger Word #1

Trigger Control Register

5.9.4 Defining a Trigger - Example

Conditions:

- Define the Command word 0825 (H) as Trigger word #1 (Receive Command for RT#1, Subaddress #1, and 5 words).
- Ignore the Word Count field.
- Use Trigger word #1 (Disable Trigger word #2).

Procedure:

1. Set Trigger Word #1 register = 0825 (H)
2. Set Trigger Mask #1 register = FFE0 (H)
3. Set Trigger Control register = 09 (H)

NOTE If you wish to use trigger(s), at least one of the bits Store All, Store Only, or Store After, must be set.

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5.10 Program Examples—BM Mode

Bus Monitor Sequential Fixed-Block Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,08`	Set the Board Configuration register for Bus Monitor Sequential Fixed-Block mode.
`20 POKE &H3FF0,xx`	Set trigger mask #1—low to xx.
`30 POKE &H3FF1,xx`	Set trigger mask #1—high to xx.
`40 POKE &H3FF2,xx`	Set trigger word #1—low to xx.
`50 POKE &H3FF3,xx`	Set trigger word #1—high to xx.
`60 POKE &H3FEB,xx`	Set the Trigger Control register (see "Trigger Control Register," page 5-17).
`70 POKE &H3FEA,00`	Set the Mode Code Control Register to 1s and 0s (see "Mode Code Control Register," page 5-28).
`80 POKE &H3FE8,00`	Set the Broadcast Control register to RT31 = regular (see "Broadcast Control Register," page 5-29).
`90 POKE &H3FFC,01`	Start command.

NOTE Messages are read from memory starting from address 0000.

Bus Monitor Sequential Link-List Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H10`	Set the Board Configuration register to Bus Monitor Link-List mode (see "Board Configuration Register," page 5-22).
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (see "Mode Code Control Register," page 5-28).
`30 POKE &H3FE8,01`	Set the Broadcast Control Register to RT31 = Broadcast (see "Broadcast Control Register," page 5-29).
`40 POKE &H3FFC,01`	Start command.

NOTE Messages are read from memory starting from address 0000.

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Bus Monitor Look-Up Table Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H20`	Set the Board Configuration register to Bus Monitor Look-Up Table mode.
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (see "Mode Code Control Register," page 5-28).
`30 POKE &H3FE8,00`	Set the Broadcast Control register to RT31 = Regular.
`40 POKE &H4143,00`	Set the Look-Up Table so that Command words with Remote Terminal 5, Receive mode, and Subaddress 3 point to Data Block #0 (see "Look-Up Table," page 5-9).
`50 POKE &H4144,01`	Set the Look-Up Table so that Command words with Remote Terminal 5, Receive mode, and Subaddress 4 point to Data Block #1 (see "Look-Up Table," page 5-9).
`60 POKE &H3FFC,01`	Start Command.

NOTE Messages are read from memory according to the address pointer derived from Command word (see "Look-Up Table," page 5-9).

5.11 Control Register Definitions

5.11.1 Time Tag Counter

Address: 7008–700B (H) READ

Read the four bytes of the Time Tag Counter to determine the current bank's free-running, 32-bit Time Tag counter value. You may read the counter at any time.

The counter must be read in the following sequence:

1. 7008 (H)
2. 700A (H)
3. 700C (H)
4. 700E (H)

7008 (H) contains the LSB; 700E (H) contains the MSB. The Time Tag Resolution register sets the resolution of the counter ("Time Tag Resolution Register," page 5-26).

The counter is reset upon power-up or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFFFFFF (H), the counter wraps around to 0 and continues counting.

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5.11.2 Time Tag Reset Register — Address: 7007 (H) WRITE ONLY

Write to the Time Tag Reset register to reset the Channel 1 Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

NOTE The counter can also be reset from an external source (see EXTTRSTx$ pin in "Connectors," page 7-7).

5.11.3 Time Tag Options Register — Address: 700C (H) WRITE

Set bit 00 of the Time Tag Options register to select the clock source for the Channel 1 Time Tag counter. The Time Tag Options register will be set to 0 after power-up or software reset.

Bit	Description
01-07	x
00	External Clock Source: 0 = Internal Time Tag Clock 1 = External Time Tag Clock (see EXTTCLKx pin in "Connectors," page 7-7).

Time Tag Options Register

5.11.4 Concurrent Start Register — Address: 7005 (H) WRITE

Set the Concurrent Start register to start the operation of Channel 1 and Channel 2 (if present), simultaneously. Starting both channels simultaneously assures that they will be synchronized.

When using the Concurrent Start register, the standard Start registers of the dual-port RAM must be set to logic 0.

To stop the selected operation(s), follow the normal procedure described under the respective Start register.

Bit	Description
00-07	X (Don't Care)

Concurrent Start Register

NOTE 1. A concurrent start can also be achieved by sending a low TTL pulse of 100 nsec. minimum to the EXSTART$ pin (see "Connectors," page 7-7).

2. The Concurrent Start register is not supported in Channel 2 (see "Concurrent/Non-Concurrent Monitor Differences," page 5-30).

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5.11.5 Monitor Options Register

Address: 7004 (H)

The Monitor Options register is used to check for the presence of a Concurrent Monitor [EMP(I) option].

Bit	Description
06-07	Reserved
05	Concurrent Monitor Installed Bit. Read Only 0 = Not Installed (card is an EXC-1553PCI/EP) 1 = Installed [card is an EXC-1553PCI/EPM(I)]
00-04	Reserved

Monitor Options Register

NOTE The Monitor Options register is not supported in Channel 2 (see "Concurrent/Non-Concurrent Monitor Differences," page 5-30).

5.11.6 Global Software Reset Register

Address: 7002 (H)

Set the Global Software Reset register to reset both Channel 1 and Channel 2 (if EPM(I) option present), simultaneously (data field = don't dare).

NOTE 1. Global Software Reset erases all locations in dual-port RAM. Board status, Board ID, Firmware Revision and Variable Amplitude registers are written by the board after the reset operation is completed.

2. The Global Software Reset register is not supported in Channel 2 (see "Concurrent/Non-Concurrent Monitor Differences," page 5-30).

5.11.7 Interrupt Reset Register

Address: 7001 (H)

To reset the Interrupt signal generated by Channel 1, write to the Interrupt Reset register at the beginning of a user-written interrupt service routine (data field = don't care).

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5.11.8 Software Reset Register **Address: 7000 (H)**

Write to the Software Reset register to reset Channel 1 (data field = don't care). The bank will act as if power had been switched OFF then ON. After the reset operation is completed, the board writes to the Board status, the Board ID, Firmware Revision and Variable Amplitude registers.

WARNING *Software Reset erases all memory locations in the dual-port RAM.*

5.11.9 Board Configuration Register **Address: 3FFF (H)**

Before issuing a Start command to the board, you must set the operating mode of the board via the Board Configuration register. To modify the Board Configuration register, issue a Stop command, write one of the hex values to the register (see the table below), and then issue a Start command (see "Start Register," page 5-24).

Hex Value	Operating Mode
01	BC Mode
02	RT Mode
04	BC/Concurrent-RT
08	**BM Sequential Block Mode**
10	**BM Sequential Link List**
20	**BM Look-Up Table Mode**
40	Reserved
80	Reserved
ED	Internal Loop Test (see Appendix C, "Internal Loop Back Test," page 9-4).
FF	External Loop Test (see Appendix D, "External Loop Back Test," page 9-5).

Board Configuration Register Values—Monitor Mode

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5.11.10 Board ID Register

Address: 3FFE (H)

The Board ID register contains a fixed value that can be read by your initialization routine to detect the presence of the board. The one-byte value of this register is: 45 (Hex), ASCII value “E”.

5.11.11 Board Status Register

Address: 3FFD (H)

The Board Status register indicates the status of the board. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Board Type is EXC-1553PCI/EP
06	X (Don’t Care)
05	BM Time Tag Mode: 1 = 16-Bit Mode 0 = 32-Bit Mode
04	1 = Board Halted 0 = Board Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Board Ready

Board Status Register

NOTE Board operation stops after you clear the Start bit in the Start Register. Following this, the board sets bit 04 (Board Halted). Certain registers may be modified only after the Board Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the board resets the Board Halted bit. The condition of this bit after power-up or software reset is logic 1.

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5.11.12 Start Register

Address: 3FFC (H)

The Start register controls the Start/Halt operation of the board. For more information about Bit 04 (Board Halted/Running) in the Board Status Register, see the note in "Board Status Register."

Write to the Start register with the appropriate bit set to execute one of the functions described below.

Bit	Bit Name	Description
06-07	**Reserved**	Set to 0
05	**Stop on Trigger/ Continue**	This bit is used in Sequential Fixed-Block mode only. 1 = Stop On Trigger. Stop storing 1553 messages when the Message Counter equals the Message Counter Trigger. 0 = Continue After Stop. Continue monitoring operations. You must first set this bit to 1 before Halting the board (setting bit 00 = 0).
04	**Initialize Board**	You must set this bit to re-initialize the board, in order to change the board's mode of operation (via the Board Configuration register). To switch Monitor modes, you must stop and start the board (Start/Halt bit (bit 00)) and set this bit (bit 04). After the specific function is completed, the board clears this bit and the Start/Halt bit to 0. Board Halted bit (04) of the Board Status register is set when both of the following are true: • A Halt command is issued (bit 00 of this register is set to 0) • An Initialize Board command is issued (this bit is set to 1) 1 = Initialize Board 0 = Stay in Monitor Mode
03	**Clear Memory**	This bit clears the 1553 message blocks and all readable control registers. 1 = Clear Memory 0 = Don't Clear Memory
01-02	**Reserved**	Set to 0
00	**Start/Halt**	1 = Start Operation 0 = Halt Operation

Start Register

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NOTE 1. The board tests Clear Memory (bit 03) and Initialize Board (bit 04) only when the Start/Halt bit (bit 00) = 0.

Clear Memory clears the 1553 message blocks and all readable control registers. The Initialize Board bit enables you to re-initialize the board, change the board's mode of operation (modify the Board Configuration register) and restart.

To switch Monitor modes, you must stop and start the board (Start/Halt bit (bit 00)) and set the Initialize Board bit (bit 04). After the specific function is completed, the board sets the Initialize Board bit and the Start/Halt bit to 0.

2. The Stop On Trigger/Continue bit (bit 05) is used in Sequential Fixed-Block mode only. The Stop On Trigger/Continue bit is tested when the Message counter equals the Message Counter Trigger. If Stop On Trigger/Continue bit = 1, the board will stop storing 1553 messages. Setting Stop On Trigger/Continue bit = 0 allows the board to continue monitoring operations. You must first Continue (set bit 05 = 1) before Halting the board (setting bit 00 = 0).

3. Bit 04 of the Board Status register is set if one of the following is true:

- A Halt command is issued (bit 00 is set to 0)
- An Initialize Board command is issued (bit 04 is set to 1)

5.11.13 Interrupt Condition Register **Address: 3FFB (H)**

Set the Interrupt Condition register to enable interrupt triggers. When a condition that is enabled in this register occurs, an interrupt is generated. Check the Message Status register to determine which condition caused the interrupt.

You must set the Interrupt Condition register before issuing a Start command to the board. To modify the Interrupt Condition register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 5-24).

NOTE For all interrupt conditions, the interrupt will be sent at the end of the message.

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Bit	Description
03-07	0
02	1 = Counter Trigger Match (Valid Only in Sequential Fixed-Block Mode)
01	1 = Message Reception in Progress (Valid in All Modes)
00	1 = Trigger Word Received (Valid Only in Sequential Fixed-Block Mode)

Interrupt Condition Register

5.11.14 Message Status Register — Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. Each status bit is described in the table below.

Bit	Description
03-07	0
02	1 = Counter Trigger Match
01	1= Message Reception In Progress
00	1 = Trigger Word Received / Busy Trigger word received is valid only in Sequential Fixed-Block mode. Busy is valid in Linked-List and Look-Up Table mode. The busy bit is set when the board is processing a message. It is set together with message reception in progress, but is reset approximately 5 µsec. after the end of each message. For consecutive messages with short intermessage gap times, the busy bit may not be reset between messages.

Message Status Register

NOTE Status bits are *not* reset by the board. Reset them after you have read them.

5.11.15 Time Tag Resolution Register — Address: 3FF6 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 µsec.

To determine the Time Tag Counter's Resolution, use the following equation:

= (Time Tag Resolution register value + 1) x 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

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You must set the Time Tag Resolution register before issuing a Start command to the board. To modify the Time Tag Resolution register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 5-24).

NOTE In Bus Monitor mode, the Time Tag Resolution register is applicable only in 32-bit time tag mode.

5.11.16 Message Counter Register — Address: 3FF5 (H)

Sequential Fixed-Block mode only.

Read the Message Counter register to determine the current Message Block number (0–199). The value is incremented by the board as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* 1553 message transfer operation. To determine the arrival of the first 1553 message, check the Message Status word of the *first* Message block. The End of Message bit (bit 15) in the Message Status word will be set.

5.11.17 Counter Trigger Register — Address: 3FF4 (H)

Sequential Fixed-Block mode only.

Read the Counter Trigger register to determine when a specific message block number has been updated by the board. Set the Counter Trigger register to a value that when equal to the Message counter will set a bit in the Message status register and set an interrupt (if programmed in the Interrupt Condition register).

Set the Counter Trigger register before issuing a Start command to the board. To modify the Counter Trigger register, issue a Stop command, modify the register, then issue a Start command (see "Start Register," page 5-24).

You can also program the board to stop monitoring when the Counter Trigger value is equal to the Message Counter (see the Stop/Continue bit in the "Start Register," page 5-24).

5.11.18 End Buffer Pointer — Address: 3FF4 (H)

Link-List mode only.

The End Buffer pointer is a 16-bit pointer that indicates the address following the last word in the final message in the Message Block area. The End Buffer pointer is updated each time a final message is written into the buffer. Final messages that are longer than the remaining

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available space in the Message Block area do not wrap around to the start of the buffer. They are spilled into the Message Block Spill area, which is contiguous to the Message Block area. The value of this register varies from 3400 (H) (end of Message Block area) to 347E (H) (end of Message Block Spill area). Until the first buffer wrap around occurs, this register contains 0000 (H).

5.11.19 Next Message Pointer

Address: 3FF2 (H)

Link-List mode only.

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 0 (H) to 33FE (H).

5.11.20 Last Block Register

Address: 3FF2 (H)

Look-Up Table mode only.

Read the Last Block register to determine the (Look-Up Table) block number of the current 1553 message. This register is used to identify the location of the current 1553 message. The Last Block register is updated at the end of each message reception.

5.11.21 Mode Code Control Register

Address: 3FEA (H)

Set the Mode Code Control register to determine which 1553 Subaddress value indicates the reception of a 1553 Mode command.

You must set the Mode Code Control register before issuing a Start command to the board. To modify the Mode Code Control register, issue a Stop command, modify the register, then issue a Start command (see “Start Register,” page 5-24).

Bit	Description		
02–07	0		
00–01	Bit 01	Bit 00	Subaddresses Recognized as Mode Code
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

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5.11.22 Broadcast Control Register

Address: 3FE8 (H)

Write to the Broadcast Control register to select whether RT address 11111 (RT 31) is interpreted as a valid RT number or as a Broadcast address.

Bit	Description
01-07	0
00	1 = Broadcast option is active. RT #31 is Broadcast Address. 0 = Broadcast option is inactive. RT #31 is Regular RT.

Broadcast Control Register

5.11.23 Board Options Register

Address: 3E84 (H) READ ONLY

The Board Options register is a 16-bit register in which the low 8 bits are reserved. This register identifies the type of on-board firmware.

Bit	Description
10–15	Reserved
09	1 = 1760
08	1 = 1553
00–07	Reserved

Board Options Register

5.11.24 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-board firmware. The value 0001 0010 would be read as revision level: 1.2.

5.12 Concurrent Monitor Option

With the exception of the operation of the **Monitor Options Register**, the operation of the Concurrent Monitor in Channel 2 is identical to that of the Non-Concurrent Monitor in Channel 1. You can use both monitors simultaneously, since they operate independently of one another.

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You can choose to (concurrently) operate as a monitor on the same 1553 bus on which you are utilizing the board's BC, RT, or non-concurrent monitor functions. The EXC-1553PCI/EPM option allows you to monitor an "alternate," independent dual-redundant, 1553 bus. The EXC-1553PCI/EPMI option allows you to concurrently monitor two different dual-redundant buses.

See "Ordering Information," page 8-1, EXC-1553PCI/EPM and EXC-1553PCI/EPMI.

5.13 Concurrent/Non-Concurrent Monitor Differences

This section discusses the differences between concurrent and non-concurrent monitor operation. Several registers are not supported in Channel 2, and the Monitor Options register in the Concurrent Monitor operates differently than the Monitor Options register in the Non-Concurrent Monitor.

5.13.1 Concurrent Start Register

Address: 7005 (H)

The Concurrent Start register is not supported in Channel 2.

5.13.2 Monitor Options Register

Address: 7004 (H)

The Monitor Options register is used to check for the presence of the Independent Concurrent Monitor (EPMI option), and if present, to select Independent or Non-Independent operation. You can modify this register at any time, without having to start and stop board operation.

Bit	Description
06-07	Reserved
05	Independent Monitor Option Installed Bit. Read Only 0 = Independent Option Not Installed (card is an EXC-1553PCI/EPM) 1 = Independent Option Installed (card is an EXC-1553PCI/EPMI)
04	Independent/Non-Independent Select Bit (for EXC-1553PCI/EPMI option only). Read/Write. 0 = Non-Independent Monitor Channel Selected 1 = Independent Monitor Channel Selected
00-03	Reserved

Monitor Options Register

5.13.3 Global Software Reset Register

Address: 7002 (H)

The Global Software Reset register is not supported in Channel 2.

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6 Switching Modes of Operation

Many test applications utilizing the EXC-1553PCI/EP simulate only one operation mode, i.e., Bus Controller. For these applications, the information in this chapter is not relevant.

If your application requires simulation of more than one mode, you can switch from one mode of operation to another, i.e., between the Bus Controller and Remote Terminal modes.

To switch between modes of operation:

1. Halt the operation of the board (via the Start register).
2. Modify the Configuration register to the desired mode.
3. Set up the memory as required.
4. Set the Start bit in the Start register.

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7 Mechanical and Electrical Specifications

Chapter 7 describes the mechanical and electrical specifications of the EXC-1553PCI/EP board. The following topics are discussed:

- "Board Layout," page 7-1
- "LED Indicators," page 7-3
- "DIP Switches," page 7-4
- "Connectors," page 7-6
- "Power Requirements," page 7-8

NOTE Throughout this manual, writing a 1 to the Start register is referred to as "issuing a Start command."

7.1 Board Layout

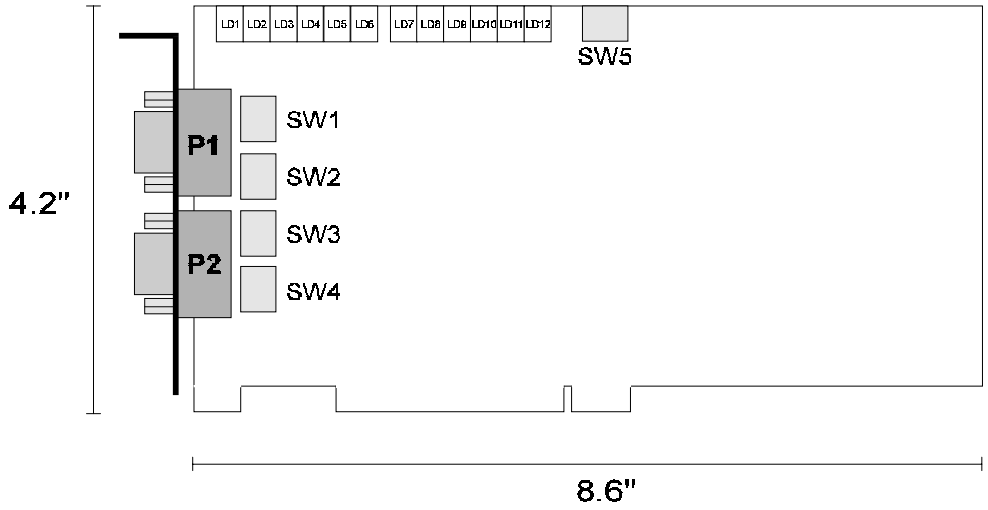


Figure 7-1. Board Layout—EXC-1553PCI/EPM(I) (Three-Quarter Size)

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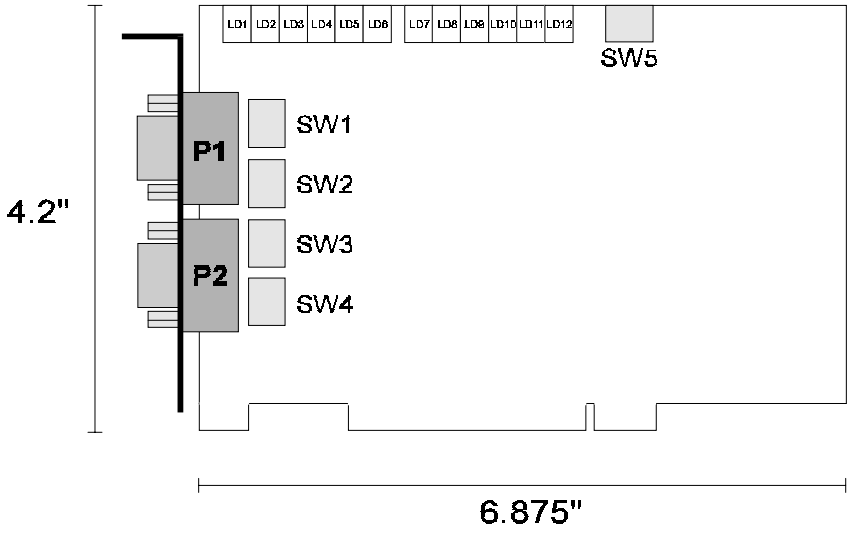


Figure 7-2. Board Layout EXC-1553PCI/EP (Half Size)

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7.2 LED Indicators

The EXC-1553PCI/EP board contains twelve LEDs. The LEDs indicate the bank's operational mode and bus activity. The function of each LED is described below.

7.2.1 Channel 1 - BC, RT, and Non Concurrent Monitor

LED	Indication
LD1	1553 Bus B Active
LD2	1553 Bus A Active
LD3	Monitor Mode Active
LD4	RT Mode Active
LD5	BC or BC/RT Mode Active
LD6	Channel 1 Ready

7.2.2 Channel 2 - Concurrent Bus Monitor

LED	Indication
LD7	1553 Bus B Active (BUS B', if Independent Monitor Activated)
LD8	1553 Bus A Active (BUS A', if Independent Monitor Activated)
LD9	Monitor Active
LD10	Reserved
LD11	Reserved
LD12	Channel 2 Ready

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7.3 DIP Switches

There are five DIP Switches on the EXC-1553PCI/EP board which control the following functions:

- Board Configuration
- 1553 Coupling selectors

Each DIP switch is described below.

7.3.1 Board Configuration DIP Switch (SW1)

The Board Configuration DIP switch selects the various system modes of the EXC-1553PCI/EP board.

Switch	Description
1	**Concurrent BM Time Tag Mode (Channel 2):** ON (Closed) = 32-bit time tag mode OFF(Open) = 16-bit time tag mode (see “Message Block Fixed-Block Operation,” page 5-5)
2	**Broadcast Mode (RT Mode Only):** ON (Closed) = Broadcast option is **not** in use. This switch indicates to the board that the Remote Terminal Address 11111 is a valid RT address. The board will respond to it with a 1553 Status word. OFF (Open) = Broadcast option is **in use**. This switch indicates to the board that Remote Terminal Address 11111 is a 1553 Broadcast command. **No** RT Status word will be transmitted.
3	**Non-Concurrent BM Time Tag Mode (Bank 0):** ON (Closed) = 32-bit time tag mode OFF (Open) = 16-bit time tag mode (see “Message Block Fixed-Block Operation,” page 5-5)
4	**Power-On Delay / LED Test Mode:** ON (Closed) = Delay is **not active**. After completing the internal self-test, the board will wait for a user-issued Start command (after approximately 2 seconds). OFF (Open) = Delay is **active**. After completing the internal self-test, the board will test the LEDs (LD3 - LD6) and then insert a time delay of approximately 5 seconds before responding to PC instructions. This option exists to assure that the board’s processor ignores any PC accesses (writes) until the PC self-test is complete. Since the board is memory-mapped, the PC BIOS’s power-on self-test might inadvertently write in the board’s memory, starting the 1553 operation.

Board Configuration DIP Switch (SW1)

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7.3.2 1553 Coupling Mode Select DIP Switches (SW3, SW4, SW5, SW6)

There are four DIP switches on the EXC-1553PCI/EP board which select the 1553 coupling mode of the board to the 1553 bus. The board can be either direct- or transformer-coupled.

Each DIP switch corresponds to a bus as follows:

DIP Switch	Channel, Bus
SW1	BUS A of the BC, RT and Non-Independent Monitor
SW2	BUS B of the BC, RT and Non-Independent Monitor
SW3	BUS A' of the Independent Concurrent Monitor (EPMI only)
SW4	BUS B' of the Independent Concurrent Monitor (EPMI only)

Each DIP switch contains four switch contacts, which are used to set the coupling mode, as described below:

Switch Contact	Direct-Coupled Setting	Transformer-Coupled Setting
1	ON (Closed)	OFF (Open)
2	ON (Closed)	OFF (Open)
3	OFF (Open)	ON (Closed)
4	OFF (Open)	ON (Closed)

7.3.3 Factory Default DIP Switch Settings

Following are the factory preset default settings:

SW1-4 Transformer-Coupled

SW5 All Closed

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7.4 Connectors

The board contains two DB-9 connectors, labeled P1 and P2. Each board is shipped with two adapter cables that convert the DB-9 to a standard 1553 (miniature) female twinax type, which will mate with a Trompeter PL75-type male connector (not supplied). The EPMI option has double type adapter cables. The adapter cables are wired and ready to connect to the 1553 bus. Excalibur Systems, Inc. carries a complete line of data bus products. Contact us for detailed ordering information.

7.4.1 Connectors P1 and P2 Pinout

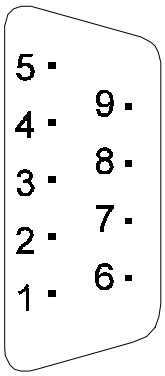


Figure 7-3. Connectors P1 and P2 Layout (Front View)

7.4.2 Connectors P1 and P2 Pin Assignments

Connector P1		Connector P2	
1	BUS_A'_HI	**1**	BUS_B'_HI
2	BUS_A'_LO	**2**	BUS_B'_LO
3	GND	**3**	GND
4	BUS_A_LO	**4**	BUS_B_LO
5	BUS_A_HI	**5**	BUS_B_HI
6	SHIELD	**6**	SHIELD
7	EXTTRST0$	**7**	EXTTRST1$
8	EXTTCLK0	**8**	EXTTCLK1
9	EXSTART$	**9**	

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7.4.3 Connectors P1 and P2 Signals Description

Signal	Description
BUS_A_HI, BUS_A_LO	Channel #1, Bus A, connection.
BUS_B_HI, BUS_B_LO	Channel #1, Bus B, connection.
BUS_A'_HI, BUS_A'_LO	Channel #2 (EPMI only), Bus A, connection.
BUS_B'_HI, BUS_B'_LO	Channel #2 (EPMI only), Bus B, connection.
SHIELD (case)	Provided for 1553 cables shield connection. This signal is connected to the case of the computer.
EXSTART$	External Start Low Active TTL input (see Concurrent Start register in all modes).
EXTTCLKx	Bank #x External Time Tag Clock TTL input. Provides an option to drive the Time Tag Counter clock from an external source for synchronizing in a multiple-board application. Connect a 250KHz or less clock with respect to the GND pin. Note: The external clock takes affect only after the EXTTCLK bit in the Time Tag Options register is activated by the user.
EXTTRSTx$	Bank #x External Time Tag Reset low active TTL input. Provides an option to reset the Time Tag counter from an external source, to achieve common initialization in a multiple boards application. Apply a low TTL pulse of 100 nsec/min. with respect to the GND pin. Note: The reset takes affect only after the board is started in RT or BM mode.
GND	Provides ground reference for the digital signal connections.

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7.5 Power Requirements

The power required by the EXC-1553PCI/EP depends on the options ordered. Power requirements are listed in the following tables.

	+5v	+12v	-12v
EXC-1553PCI/EP	1.2 A	190 mA	155 mA

	+5v	+12v	-12v
EXC-1553PCI/EPM	1.45 A	190 mA	155 mA

	+5v	+12v	-12v
EXC-1553PCI/EPMI	1.6 A	190 mA	155 mA

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8 Ordering Information

Chapter 8 explains how to indicate which options you want when ordering a EXC-1553PCI/EP card.

The following suffixes can be added to the name of the card (EXC-1553PCI/EP) to indicate specific options. The suffixes are added to "EXC-1553PCI/EP" in the order in which they appear in the table.

SUFFIX	DESCRIPTION
M	Concurrent monitor option
I	Independent concurrent monitor channel option

Ordering examples:

PART NUMBER	DESCRIPTION
EXC-1553PCI/EP	MIL-STD-1553 interface card, half size, for PC computers. Supports BC, RT, BC/RT and BM modes.
EXC-1553PCI/EPM	MIL-STD-1553 interface card, three-quarter size, for PC computers. Supports BC, RT, BC/RT and BM modes. With concurrent monitor.
EXC-1553PCI/EPMI	MIL-STD-1553 interface card, three-quarter size, for PC computers. Supports BC, RT, BC/RT and BM modes. With independent concurrent monitor channel.

NOTE The Independent Monitor option is only available in conjunction with the Concurrent Monitor option.

The Half-Size Card option is not available with the Concurrent Monitor option.

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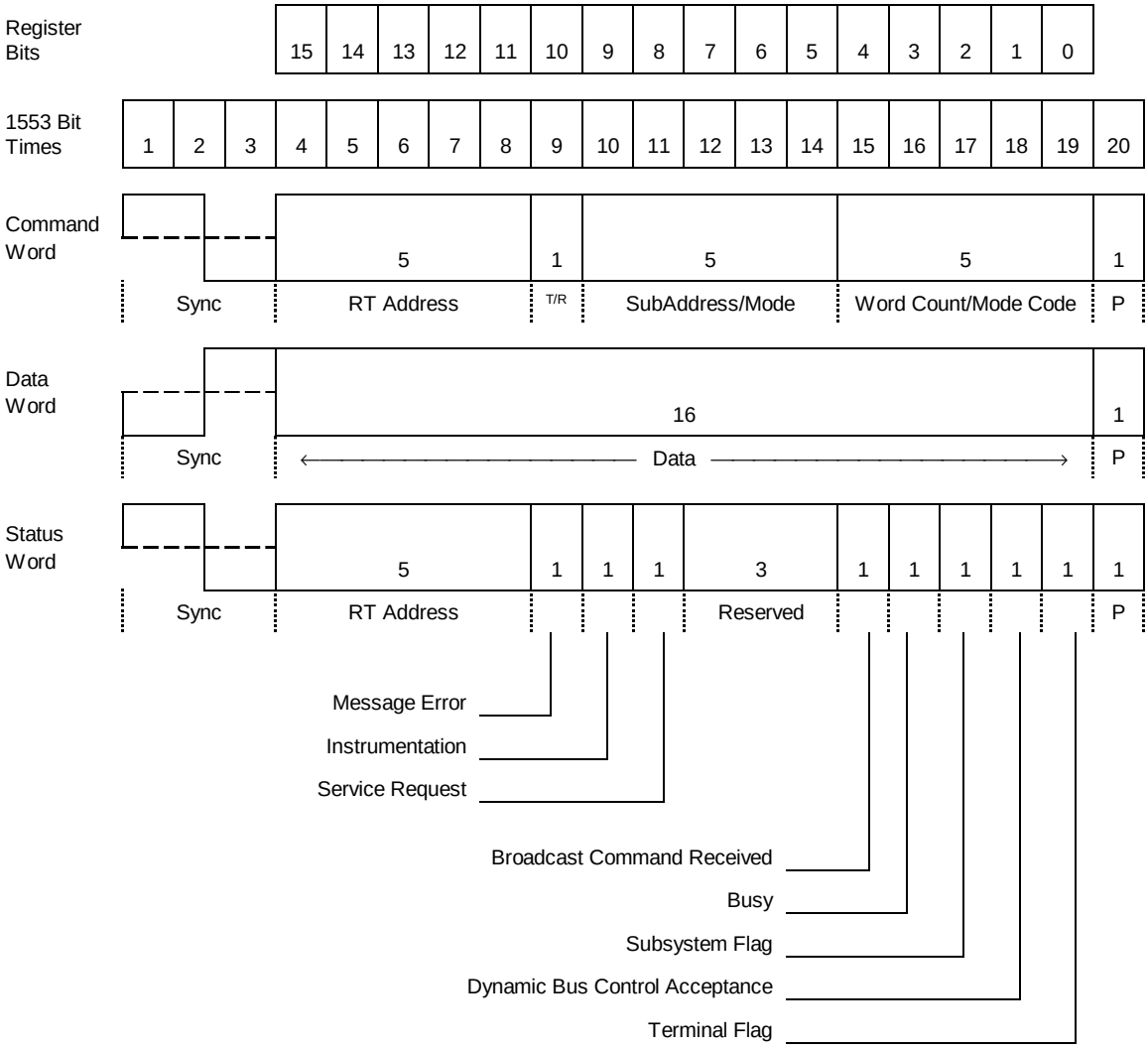
9 Appendices

Chapter 9 contains appendices describing the Military Standard 1553B word, Military Standard message formats, internal and external loop back tests and customer support. These topics are discussed on the following pages:

- "MIL-STD-1553B Word Formats," page 9-2
- "MIL-STD-1553B Message Formats," page 9-3
- "Internal Loop Back Test," page 9-4
- "External Loop Back Test," page 9-5
- "Customer Support," page 9-6

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Appendix A MIL-STD-1553B Word Formats

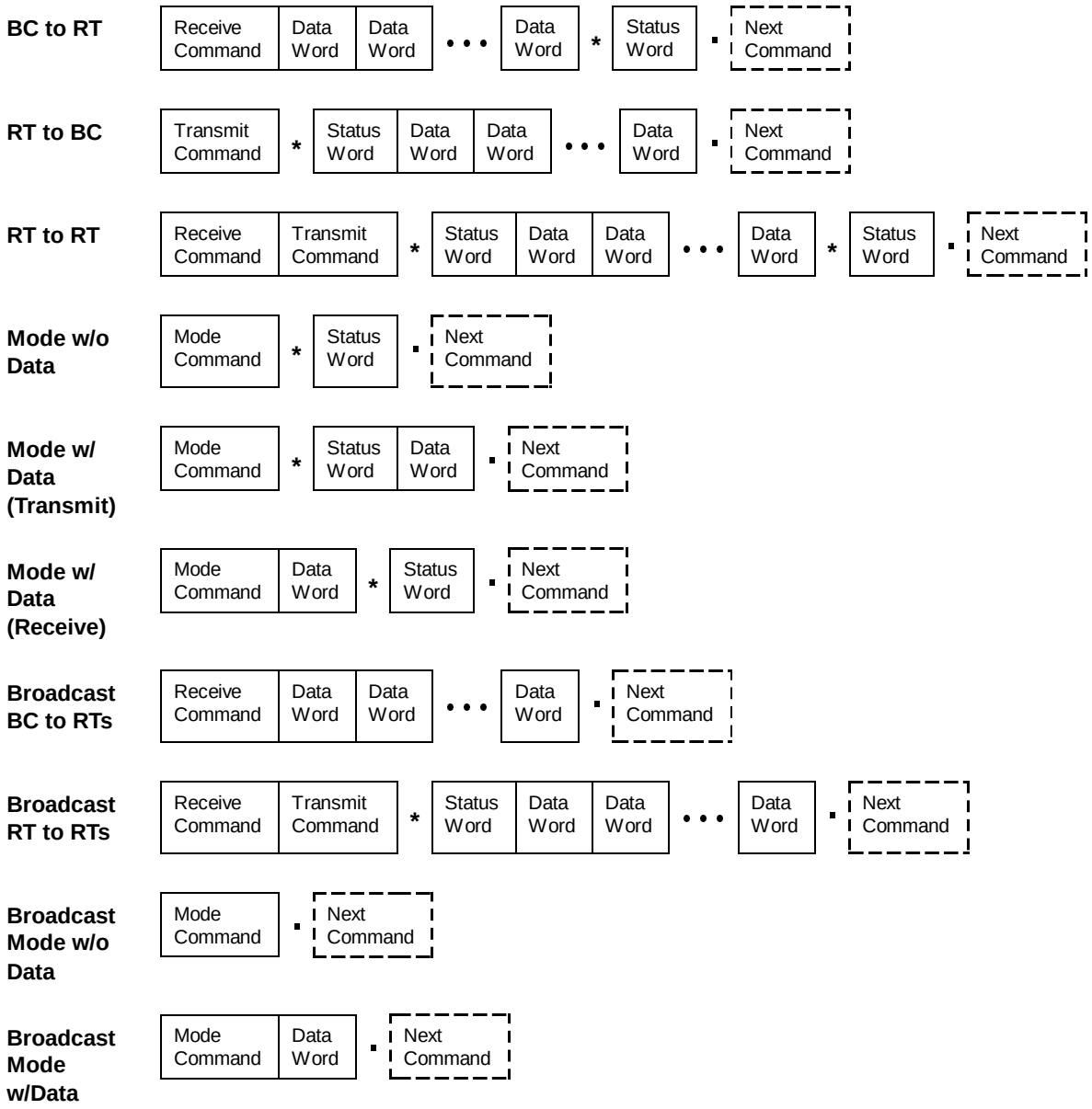


NOTE: T/R = Transmit/Receive
P = Parity

Figure 9-1. MIL-STD-1553B Word Formats

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Appendix B MIL-STD-1553B Message Formats



NOTE: * = Response time
▪ = Intermessage gap

Figure 9-2. MIL-STD-1553B Message Formats

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Appendix C Internal Loop Back Test

The Internal Loop Back Test is used to check the 1553 front-end logic, excluding transceivers and coupling transformers.

To initiate the internal loop back test:

1. Write ED (H) into the Board Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

struct I_LOOPBACK

{

	Address in Dual-Port RAM	Status Value
usint frame_val;	0	X (not for user)
usint frame_status;	2	8000H passed, 8001H failed
usint resp_status;	4	8000H passed, 8001H failed
usint early_val;	6	6 LSB must be 15H
usint receive_data1;	8	5555H
usint status_1;	10	8000H passed, else failed
usint receive_data2;	12	AAAAH
usint status_2;	14	8000H passed, else failed
usint mc_status;	16	8000H passed, else failed
usint ttag_val_lo;	18	30D4H ± 2
usint ttag_val_hi;	20	0
usint ttag_status;	22	8000H passed, 8001H failed
usint prl;	24	8 LSB contain the CPU version

} *I_loopback;

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Appendix D External Loop Back Test

The External Loop Back Test is used to check the 1553 transceivers, transformers and associated bus cables.

NOTE The External Loop Back Test requires a loopback cable to connect bus A to bus B.

To initiate the external loop back test:

1. Write FF (H) into the Board Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

struct E_LOOPBACK

{

	Address in Dual-Port RAM	Status Value
usint frame_val;	0	X (not for user)
usint frame_status;	2	8000H passed, 8001H failed
usint cmd_send[8];	4	cmd_send[0]: 5555H
		cmd_send[1]:8000H passed, else failed
		cmd_send[2]: 1234H
		cmd_send[3]:8000H passed, else failed
		cmd_send[4]: 5555H
		cmd_send[5]:8000H passed, else failed
		cmd_send[6]: 1234H
		cmd_send[7]:8000H passed, else failed
usint ttag_val_lo	20	30D4H ± 2
usint ttag_val_hi	22	0
usint ttag_status;	24	8000H passed, 8001H failed

} *E_loopback;

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Appendix E Customer Support

Excalibur Systems, Inc. is interested in the applications you develop with our products, and we are ready to answer any technical questions you may have.

When you want to talk to us, call the representative nearest you, or contact our corporate headquarters or website as follows:

EXCALIBUR WEBSITE	www.mil-1553.com
EXCALIBUR CORPORATE HEADQUARTERS	Tel.: 1-800-MIL-1553 (Toll Free) Fax.: 516-327-4645 Email: excalibur@mil-1553.com

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