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M4K429RTx

ARINC 429
Test and Simulation Module for the EXC-4000 Family of Carrier Boards

User's Manual

EXCALIBUR SYSTEMS

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Table of Contents

1 Introduction

1.1 Overview 1-1
1.1.1 *M4K429RTx* Module Features 1-2
1.2 Installation 1-3
1.2.1 Module Installation 1-3
1.3 Getting Started 1-3
1.4 *M4K429RTx* General Memory Map 1-5
1.5 Technical Support 1-6

2 Module Control Registers (Advanced)

2.1 Global Registers Memory Map 2-3
2.2 ARINC 429 Module Global Register Definitions 2-4
2.2.1 Module Options Register 2-4
2.2.2 Interrupt Status Busy Register 2-4
2.2.3 Receive Merge Status Register 2-5
2.2.4 Receive Merge Interrupt/Trigger Condition Register 2-6
2.2.5 Receive Merge Configuration Register 2-6
2.2.6 Receive Merge Label Trigger Register 2-7
2.2.7 Receive Merge Error Count Register 2-7
2.2.8 Receive Merge Interval Count Trigger Register 2-7
2.2.9 Receive Merge Buffer Wraparound Register 2-7
2.2.10 Receive Merge Word Count Trigger Register 2-8
2.2.11 Receive Merge Word Counter 2-8
2.2.12 Receive Merge Filter Table Start Address 2-8
2.2.13 Receive Merge Current Pointer 2-8
2.2.14 Receive Merge End Pointer 2-8
2.2.15 Receive Merge Start Pointer 2-8
2.2.16 Receive Data Storage Mode Register 2-9
2.2.17 Channel *x* Configuration Status Register 2-10
2.2.18 Programmable Bit Rate Register 2-10
2.2.19 Interrupt Status Register 2-11
2.2.20 Firmware Revision Register 2-11
2.2.21 Board Status Register 2-12
2.2.22 Board ID Register 2-13
2.2.23 Start/Stop Register 2-13
2.2.24 Time Tag Reset Register 2-13
2.2.25 Software Reset Register 2-14
2.2.26 Time Tag Counter 2-14
2.2.27 Hardware Revision Register 2-14
2.2.28 Channel Enable Register 2-15
2.2.29 Channel Type Select Register 2-16
2.3 Transmit Channel Operation 2-17
2.3.1 Interblock Time Mode and Data Rate Mode 2-17
2.3.2 FIFO Mode 2-22
2.4 Receive Channel Operation 2-26
2.4.1 Sequential and Merge Modes 2-26
2.4.2 Look-up Table Mode Operation 2-33
2.5 Translation (Dual Channel) Operation 2-35
2.5.1 Allocating a Translation Table in a Channel 2-35
2.5.2 Allocating a Translation Table Entry 2-35
2.5.3 Using Translation Functions 2-35

2.6 Channel Control Registers Maps 2-38
2.6.1 Channel 0 Control Register Block Memory Map 2-38
2.6.2 Channel 1 Control Register Block Memory Map 2-39
2.6.3 Channel 2 Control Register Block Memory Map 2-40
2.6.4 Channel 3 Control Register Block Memory Map 2-41
2.6.5 Channel 4 Control Register Block Memory Map 2-42
2.6.6 Channel 5 Control Register Block Memory Map 2-43
2.6.7 Channel 6 Control Register Block Memory Map 2-44
2.6.8 Channel 7 Control Register Block Memory Map 2-45
2.6.9 Channel 8 Control Register Block Memory Map 2-46
2.6.10 Channel 9 Control Register Block Memory Map 2-47
2.7 Channel Control Register Definitions 2-48
2.7.1 Channel *x* Scratch Buffer End Register 2-48
2.7.2 Channel *x* Scratch Buffer Start Register 2-48
2.7.3 Channel *x* Status Register 2-48
2.7.4 Channel *x* Interrupt/Trigger Condition Register 2-49
2.7.5 Channel x Transmit Loop Counter 2-49
2.7.6 Channel *x* Transmit Instruction Counter 2-50
2.7.7 Channel *x* Transmit Instruction Stack Pointer 2-50
2.7.8 Channel *x* Receive Label Trigger Register 2-50
2.7.9 Channel x Receive Error Count Register 2-50
2.7.10 Channel x Receive Interval Counter Trigger Register 2-50
2.7.11 Channel x Receive Data Word Counter Trigger Registers 2-51
2.7.12 Channel *x* Receive Buffer Wraparound Register 2-51
2.7.13 Channel *x* Receive/Transmit Data Word Count Register 2-51
2.7.14 Channel *x* Receive Filter Table Start Address 2-51
2.7.15 Channel *x* Receive Look-up Table Start Address 2-52
2.7.16 Channel *x* Receive Data Current Pointer 2-52
2.7.17 Channel *x* Receive Data End Pointer 2-52
2.7.18 Channel *x* Receive Data Start Pointer 2-52
2.7.19 Channel *x* Configuration Register 2-53

3 Mechanical and Electrical Specifications

3.1 Module Layout 3-2
3.2 LED Indicators 3-2
3.3 Connectors 3-3
3.3.1 EXC-4000 Carrier Board 96-pin Connector 3-3
3.3.2 *M4K429RTx* Module Adapter Cable 3-5
3.4 Power Supply Requirements 3-6

4 Ordering Information

Appendix A ARINC 429 Basic Word Formats

Appendix B ARINC 429 Connection Precautions

Figures

Figure 1-1 *M4K429RTx* Module Block Diagram 1-2
Figure 1-2 Module Operation Flowchart 1-4
Figure 1-3 General Memory Map 1-5
Figure 2-1 Interblock Time Mode 2-17
Figure 2-2 Data Rate Mode 2-17
Figure 2-3 Transmit Instruction Stack Structure 2-19
Figure 2-4 Transmit Data Block 2-21
Figure 2-5 32-Bit Transmit Data Words Format 2-21
Figure 2-6 32-Bit Word Transmit Order Bit 2-22
Figure 2-7 Buffer Structure 2-23
Figure 2-8 Receive Sequential Mode Buffer Structure with Standard Time Tags 2-28
Figure 2-9 Receive Sequential Mode Buffer Structure with IRIG B Time Tags 2-28
Figure 2-10 32-Bit Receive Data Word Format 2-29
Figure 2-11 32-Bit ARINC Word Order Bit 2-29
Figure 2-12 Time Tag Word Format in Standard (Non-IRIG B) Mode 2-30
Figure 2-13 Time Tag Word Format in IRIG B Mode 2-30
Figure 2-14 Receive Sequential Mode Filter Table Diagram 2-32
Figure 2-15 Receive Look-up Table Structure 2-33
Figure 2-16 Translation Table Entry 2-36
Figure 2-17 Channel 0 Control Register Block Map 2-38
Figure 2-18 Channel 1 Control Register Block Map 2-39
Figure 2-19 Channel 2 Control Register Block Map 2-40
Figure 2-20 Channel 3 Control Register Block Map 2-41
Figure 2-21 Channel 4 Control Register Block Map 2-42
Figure 2-22 Channel 5 Control Register Block Map 2-43
Figure 2-23 Channel 6 Control Register Block Map 2-44
Figure 2-24 Channel 7 Control Register Block Map 2-45
Figure 2-25 Channel 8 Control Register Block Map 2-46
Figure 2-26 Channel 9 Control Register Block Map 2-47
Figure 3-1 *M4K429RTx* Module Layout 3-2
Figure 3-2 EXC-4000 Carrier Board 96-pin Female I/O Connector – Front View 3-3
Figure 3-3 EXC-4000 Carrier Board 96-pin Male I/O Mating Cable Connector – Front View 3-3
Figure 3-4 Adapter Cable 26-pin Connector – Front View 3-5
Figure A-1 ARINC 429 Basic Word Formats A-1

Tables

Table 2-1 Look-up Table: Received Status/Control Word 2-34
Table 3-1 Module Terminal Stick: Pin Assignments and Description 3-4
Table 3-2 *M4K429RTx* Adapter Cable Connections 3-5

1 Introduction

Chapter 1 provides an overview of the *M4K429RTx* avionics communication module. The following topics are covered:

1.1 Overview 1-1
1.1.1 *M4K429RTx* Module Features 1-2
1.2 Installation 1-3
1.2.1 Module Installation 1-3
1.3 Getting Started 1-3
1.4 *M4K429RTx* General Memory Map 1-5
1.5 Technical Support 1-6

1.1 Overview

The *M4K429RTx* is an ARINC 429 multi-channel test and simulation module to be used on the Excalibur 4000 family of carrier boards. The module supports up to ten ARINC 429 channels in any combination of transmitters and receivers. Each of these channels feature error injection and detection capabilities.

The receive channels allow for the storage of all selected Labels with status and Time Tag information appended to each word. The receivers allow for filtering and multi-storage modes of Data Words.

The transmit channels operate via a transmit 'instruction stack' which allows scheduling of data transmissions and reduces the need for host computer intervention.

The *M4K429RTx* comes complete with GUI software, a C-driver software library including the source code.

For exact part numbers, see **Chapter 4 Ordering Information**.

Note: The *M4K429RTx* module can be mounted on the following Excalibur carrier boards:

- *EXC-4000PCI[e]*
- *EXC-4000cPCI*
- *EXC-2000PCI[e]*
- *EXC-4000VME*
- *EXC-4000VXI*
- *EXC-4000P104plus*

1.1.1 *M4K429RTx* Module Features

Global

10 ARINC 429 Channels each programmable as receive or transmit
Two module types: RT5, RT10
Memory Mapped, 64K x 8 dual-port RAM
Programmable Hardware Trigger Output
Interrupt and Polling Modes of Operation
5V operation only

Programmable (per channel)
Buffer size
Bit rates (Hi, Lo, Programmable)
Parity (Odd, Even, On, Off)

Transmit Channel

Transmit Modes
Interblock Time
Data Rate
FIFO Data

Transmit Features
Transmit Sync Time (between Words)
One-shot, *N*-times or Loop transmission

Transmit Error Injection per Block
Bit Count Hi/Lo
Sync Time
Stretch Bit
Bit Rate (frequency)
Parity

Receive Channel

Receive Modes
Look-up Table
Sequential per channel
Sequential Merge Mode
(stores data from all Receive channels in one buffer)

Receive Features
Word Status Tagging
Word Time Tagging (32-bit) or
IRIG B Time Tagging (64-bit)
Label/Data Filtering
Start Triggers
Receive Error Count per channel
Receive Count Interval Trigger

Receive Error Detection per Word
Bit Count
Sync Time
Parity
Bit Coding Error

Figure 1-1 illustrates the *M4K429RTx* module.

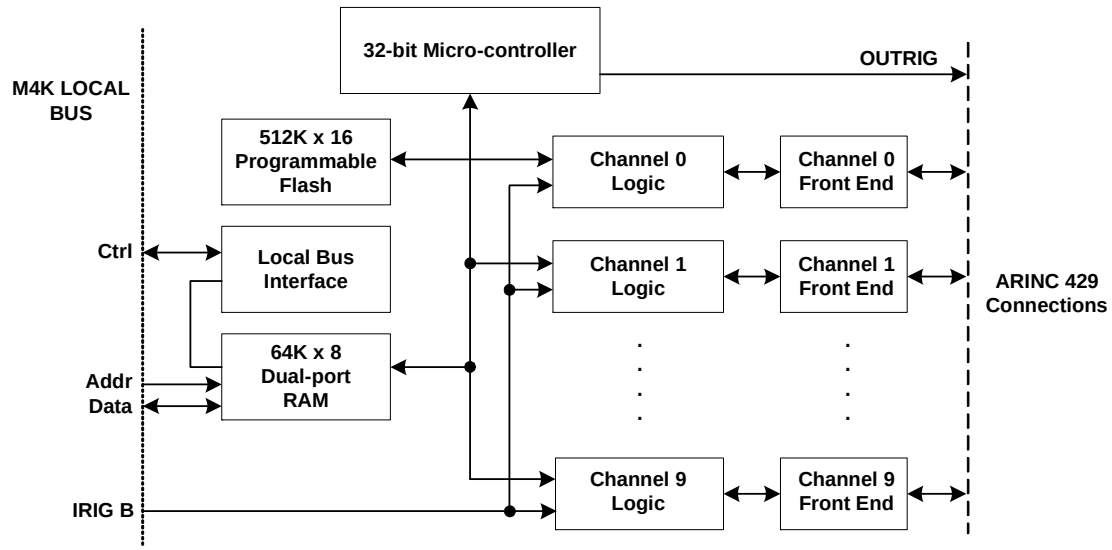


Figure 1-1 *M4K429RTx* Module Block Diagram

1.2 Installation

For hardware and software installation instructions, see the **readme.pdf** file on the root folder of the installation CD. When downloading new software from the Excalibur website, the **readme.pdf** file is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see the **readme.pdf** file. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.2.1 Module Installation

Warning: Make sure that you are grounded for electrostatic discharge when handling the Excalibur device, and use all antistatic precautionary measures.

1. If the module is supplied separately from the carrier board, *very carefully*, insert the module into the desired module location. The pin #1 marker (marked with a white rectangle) on the module must be aligned with the white rectangles on the carrier board.
2. With the computer power source switched **off**, insert the carrier board with the *M4K429RTx* module into a slot in the computer.
3. Attach the ARINC adapter cable to the carrier board I/O connector and to the bus. See **Appendix B ARINC 429 Connection Precautions**.

For mechanical and electrical specifications, see **Chapter 3 Mechanical and Electrical Specifications**.

1.3 Getting Started

The module operation makes extensive use of pointers for setting up the size and location on both the receiver and data blocks, transmitter instruction stacks and receiver Look-up Tables. Each channel has its own pointer registers so that the unique memory areas may be allocated for each channel. It is also possible to share memory areas. For example, more than one receiver channel may point to and use the same Label Look-up Table that controls which labels will be stored by the module.

The flowchart Figure 1-2 **Module Operation Flowchart** on page 1-4, describes the necessary steps to set up transmit and receive channels. For details how to operate each specific protocol, see the sections: **Transmit Channel Operation,** page 2-17 and **Receive Channel Operation,** page 2-26.

After power-up, perform the following steps:

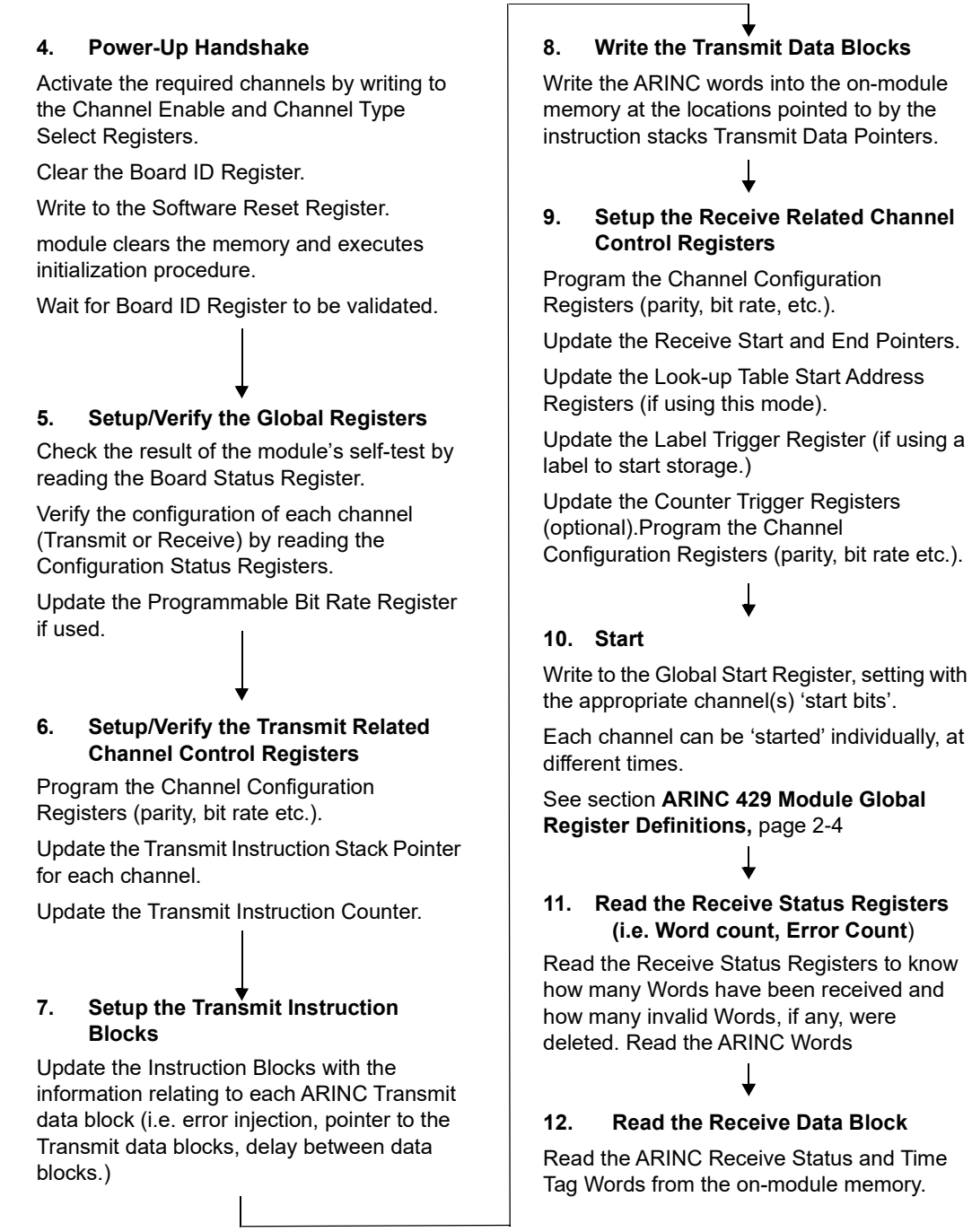


Figure 1-2 Module Operation Flowchart

1.4 *M4K429RTx* General Memory Map

The *M4K429RTx* occupies 64K x 8 of the module's 128K memory space. The 64K are divided into Control registers that reside at the upper end and the main memory block, which stores all the Stacks, Receive and Transmit Data Blocks and Look-up Tables.

Transmit Instruction Stack Transmit Data Blocks Receive Data Blocks Receive Look-Up Tables	00000 – 0F9FF H
Reserved	0FA00 – 0FD1F H
Channel Control Register Block 0	0FD20 – 0FD4E H
Channel Control Register Block 1	0FD50 – 0FD0FE H
Channel Control Register Block 2	0FD80 – 0FDAE H
Channel Control Register Block 3	0FDB0 – 0FDDE H
Channel Control Register Block 4	0FDE0 – 0FE0E H
Channel Control Register Block 5	0FE10 – 0FE3E H
Channel Control Register Block 6	0FE40 – 0FE6E H
Channel Control Register Block 7	0FE70 – 0FE9E H
Channel Control Register Block 8	0FEA0 – 0FECE H
Channel Control Register Block 9	0FED0 – 0FEFE H
Global Control Registers	0FF00 – 0FFFF H
Reserved Memory Space	10000 – 1FFFF H

Figure 1-3 General Memory Map

1.5 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, visit the Technical Support page of our website (www.mil-1553.com). You can also contact us by phone. To find the location nearest you, visit to the Contact Us page of our website. Before contacting Technical Support, please see Information Required for Technical Support.

2 Module Control Registers (Advanced)

Chapter 2 describes how to run the *M4K429RTx* module via the memory registers, which enables you to develop your own software tools. When using Excalibur's software tools, this chapter is not required.

The following topics are covered:

2.1 Global Registers Memory Map 2-3

2.2 ARINC 429 Module Global Register Definitions 2-4

2.2.1 Module Options Register 2-4
2.2.2 Interrupt Status Busy Register 2-4
2.2.3 Receive Merge Status Register 2-5
2.2.4 Receive Merge Interrupt/Trigger Condition Register 2-6
2.2.5 Receive Merge Configuration Register 2-6
2.2.6 Receive Merge Label Trigger Register 2-7
2.2.7 Receive Merge Error Count Register 2-7
2.2.8 Receive Merge Interval Count Trigger Register 2-7
2.2.9 Receive Merge Buffer Wraparound Register 2-7
2.2.10 Receive Merge Word Count Trigger Register 2-8
2.2.11 Receive Merge Word Counter 2-8
2.2.12 Receive Merge Filter Table Start Address 2-8
2.2.13 Receive Merge Current Pointer 2-8
2.2.14 Receive Merge End Pointer 2-8
2.2.15 Receive Merge Start Pointer 2-8
2.2.16 Receive Data Storage Mode Register 2-9
2.2.17 Channel *x* Configuration Status Register 2-10
2.2.18 Programmable Bit Rate Register 2-10
2.2.19 Interrupt Status Register 2-11
2.2.20 Firmware Revision Register 2-11
2.2.21 Board Status Register 2-12
2.2.22 Board ID Register 2-13
2.2.23 Start/Stop Register 2-13
2.2.24 Time Tag Reset Register 2-13
2.2.25 Software Reset Register 2-14
2.2.26 Time Tag Counter 2-14
2.2.27 Hardware Revision Register 2-14
2.2.28 Channel Enable Register 2-15
2.2.29 Channel Type Select Register 2-16
2.2.30 IRIG B Time Tag Counter 0, 1, 2 and 3 2-17
2.2.31 IRIG B Preload Seconds 2-18
2.2.32 IRIG B Preload Minutes/Hours 2-18
2.2.33 IRIG B Preload Days 2-18
2.2.34 IRIG B Load Counter 2-18

2.3 Transmit Channel Operation 2-19

2.3.1 Interblock Time Mode and Data Rate Mode 2-19
2.3.2 FIFO Mode 2-24

2.4 Receive Channel Operation 2-28

2.4.1 Sequential and Merge Modes 2-28
2.4.2 Look-up Table Mode Operation 2-35

2.5 Translation (Dual Channel) Operation 2-37
2.5.1 Allocating a Translation Table in a Channel 2-37
2.5.2 Allocating a Translation Table Entry 2-37
2.5.3 Using Translation Functions 2-37
2.6 Channel Control Registers Maps 2-40
2.6.1 Channel 0 Control Register Block Memory Map 2-40
2.6.2 Channel 1 Control Register Block Memory Map 2-41
2.6.3 Channel 2 Control Register Block Memory Map 2-42
2.6.4 Channel 3 Control Register Block Memory Map 2-43
2.6.5 Channel 4 Control Register Block Memory Map 2-44
2.6.6 Channel 5 Control Register Block Memory Map 2-45
2.6.7 Channel 6 Control Register Block Memory Map 2-46
2.6.8 Channel 7 Control Register Block Memory Map 2-47
2.6.9 Channel 8 Control Register Block Memory Map 2-48
2.6.10 Channel 9 Control Register Block Memory Map 2-49
2.7 Channel Control Register Definitions 2-50
2.7.1 Channel *x* Scratch Buffer End Register 2-50
2.7.2 Channel *x* Scratch Buffer Start Register 2-50
2.7.3 Channel *x* Status Register 2-50
2.7.4 Channel *x* Interrupt/Trigger Condition Register 2-51
2.7.5 Channel x Transmit Loop Counter 2-51
2.7.6 Channel *x* Transmit Instruction Counter 2-52
2.7.7 Channel *x* Transmit Instruction Stack Pointer 2-52
2.7.8 Channel *x* Receive Label Trigger Register 2-52
2.7.9 Channel x Receive Error Count Register 2-52
2.7.10 Channel x Receive Interval Counter Trigger Register 2-52
2.7.11 Channel x Receive Data Word Counter Trigger Registers . . .2-53
2.7.12 Channel *x* Receive Buffer Wraparound Register 2-53
2.7.13 Channel *x* Receive/Transmit Data Word Count Register 2-53
2.7.14 Channel *x* Receive Filter Table Start Address 2-53
2.7.15 Channel *x* Receive Look-up Table Start Address 2-54
2.7.16 Channel *x* Receive Data Current Pointer 2-54
2.7.17 Channel *x* Receive Data End Pointer 2-54
2.7.18 Channel *x* Receive Data Start Pointer 2-54
2.7.19 Channel *x* Configuration Register 2-55

2.1 Global Registers Memory Map

The ARINC 429 Module Global Registers are registers that affect all *M4K429RTx* channels.

Reserved	0FF00–0FF37 H	Channel 8 Configuration Status	0FF6A H
Module Options	0FF38	Channel 9 Configuration Status	0FF6C H
Reserved	0FF3A	Programmable Bit Rate	0FF6E H
Interrupt Status Busy	0FF3C H	Interrupt Status	0FF70 H
Receive Merge Status	0FF3E H	Firmware Revision	0FF72 H
Receive Merge Interrupt/Trigger Condition	0FF40 H	Board Status	0FF74 H
Receive Merge Configuration	0FF42 H	Board ID	0FF76 H
Receive Merge Label Trigger	0FF44 H	Reserved	0FF78 H
Receive Merge Error Count	0FF46 H	Start / Stop	0FF7A H
Receive Merge Interval Count Trigger	0FF48 H	Time Tag Reset	0FF7C H
Receive Merge Buffer Wraparound	0FF4A H	Reserved	0FF7E – 0FF82 H
Receive Merge Word Count Trigger	0FF4C H	Software Reset	0FF84 H
Receive Merge Word Count	0FF4E H	Reserved	0FF86 – 0FF8E H
Receive Merge Filter Table Start Address	0FF50 H	Time Tag Counter	0FF90 – 0FF92 H
Receive Merge Current Pointer	0FF52 H	Hardware Revision Register	0FF94 H
Receive Merge End Pointer	0FF54 H	Reserved	0FF96 H
Receive Merge Start Pointer	0FF56 H	Channel Enable	0FF98 H
Receive Data Storage Mode	0FF58 H	Channel Type Select	0FF9A H
Channel 0 Configuration Status	0FF5A H	Reserved	0FF9C – 0FFBE
Channel 1 Configuration Status	0FF5C H	IRIG B Time Tag Counter	0FFC0 – 0FFC6
Channel 2 Configuration Status	0FF5E H	Reserved	0FFC8 – 0FFD0
Channel 3 Configuration Status	0FF60 H	IRIG B Preload Seconds	0FFD2
Channel 4 Configuration Status	0FF62 H	IRIG B Preload Minutes/Hours	0FFD4
Channel 5 Configuration Status	0FF64 H	IRIG B Preload Days	0FFD6
Channel 6 Configuration Status	0FF66 H	IRIG B Load Counter	0FFD8
Channel 7 Configuration Status	0FF68 H	Reserved	0FFDA – 0FFFF H

Figure 2-1ARINC 429 Module Global Registers Memory Map

2.2 ARINC 429 Module Global Register Definitions

2.2.1 Module Options Register

Address: 0FF38 (H)

The Module Options Register shows whether the module is Nios-based. There are several features that are only available on Nios-based modules, use this register to determine if those features are available.

Bit	Bit Name	Description
03-15	Reserved – set to 0	
02	Nios II Processor	1 = This is a newer Nios-based module. 0 = This is an older Motorolla-based module.
00-01	Reserved – set to 0	

Module Options Register

2.2.2 Interrupt Status Busy Register

Address: 0FF3C (H)

The Interrupt Status Busy Register indicates if the Channel *x* Status Register, the Receive Merge Status Register and the Interrupts Status Register may be accessed by the user.

Bit	Bit Name	Description
11-15		Reserved
10	**MRGBSY**	1 = Receive Merge Status Register is busy – do not access the register 0 = The contents of the register is valid and may be accessed
09	**CH9BSY**	1 = Channel 9 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 9 Status Register may be accessed
08	**CH8BSY**	1 = Channel 8 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 8 Status Register may be accessed
07	**CH7BSY**	1 = Channel 7 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 7 Status Register may be accessed
06	**CH6BSY**	1 = Channel 6 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 6 Status Register may be accessed
05	**CH5BSY**	1 = Channel 5 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 5 Status Register may be accessed
04	**CH4BSY**	1 = Channel 4 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 4 Status Register may be accessed
03	**CH3BSY**	1 = Channel 3 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 3 Status Register may be accessed
02	**CH2BSY**	1 = Channel 2 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 2 Status Register may be accessed

Interrupt Status Busy Register

Bit	Bit Name	Description
01	CH1BSY	1 = Channel 1 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 1 Status Register may be accessed
00	CH0BSY	1 = Channel 0 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 0 Status Register may be accessed

Interrupt Status Busy Register (Continued)

Note: Before accessing the Global Interrupt Register, the user should wait until the Interrupt Status Busy Register = 0. The user then has at least 15 msec. to safely access the status registers.

2.2.3 Receive Merge Status Register

Address: 0FF3E (H)

The Receive Merge Status Register indicates the operational status of the Merge Mode receive buffer. This register can be used to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. Writing a 0 to this register resets the status bits.

Bit	Bit Name — Interrupt Causes
07-15	Reserved
06	Stopped on Buffer Full
05	Error Word Received
04	Word Count Trigger
03	Interval Count Trigger
02	Label Received
00-01	Reserved

Receive Merge Status Register

Note: The Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the Filter Table.

2.2.4 Receive Merge Interrupt/Trigger Condition Register

Address: 0FF40 (H)

The Receive Merge Interrupt/Trigger Condition Register sets the Interrupt and Trigger condition or conditions for receive channels in Merge Mode. The Trigger Conditions set a pulse on the External Trigger Output.

Trigger Condition Bits 08 – 15		Interrupt Condition Bits 00 – 07	
Bit	**Bit Name**	**Bit**	**Bit Name**
15	Reserved	**07**	Reserved
14	Stopped on buffer full	**06**	Stopped on buffer full
13	Error Word received	**05**	Error Word received
12	Data Word Count Trigger	**04**	Data Word Count Trigger
11	Interval Count Trigger	**03**	Interval Count Trigger
10	Label Received	**02**	Label Received
08–09	Reserved	**00–01**	Reserved

Receive Merge Interval/Trigger Condition Register

Note:
1. The Label Received interrupt or trigger only occurs upon reception of a label that has been marked for interrupt in the Filter Table.
2. To activate the Interval Count Trigger interrupt or trigger, the Receive Merge Interval Count Trigger Register must also be set. (see **Receive Merge Interval Count Trigger Register** on page 2-7).
3. To activate Data Word Count Trigger interrupt or trigger, the Receive Merge Word Count Trigger Register must also be set. (see **Receive Merge Word Count Trigger Register** on page 2-8).

2.2.5 Receive Merge Configuration Register

Address: 0FF42 (H)

The Receive Merge Configuration Register sets up run parameters for Merge Mode.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**Enable Receive Filter Table**	1 = Enable Filter table. Stores labels per table 0 = Disables table. Stores all labels.
08	**Reserved**	Set to 0
07	**Receive Label Trigger**	1 = Start data storage upon receipt of label *xx*. (see **Receive Merge Label Trigger Register**) 0 = Receive stores data without Start Label Trigger.
06	**Receive Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receive wraps around the data in the block.
00-05	**Reserved**	Set to 0

Receive Merge Configuration Register

2.2.6 Receive Merge Label Trigger Register Address: 0FF44 (H)

The Receive Merge Label Trigger Register is used in conjunction with the Receive Label Trigger bit in the Receive Merge Configuration Register to begin the reception and storage of data upon receipt of a unique ARINC label.

The module will not store any ARINC words received prior to the first instance of this label.

Bit	Description
08–15	Set to 0
00–07	Trigger Label

Receive Merge Label Trigger Register

2.2.7 Receive Merge Error Count Register Address: 0FF46 (H)

The Receive Merge Error Count Register is a 16-bit counter. The register indicates the number of error words received on the channel. This counter Register wraps around and is reset only by the user.

2.2.8 Receive Merge Interval Count Trigger Register Address: 0FF48 (H)

The Receive Merge Interval Count Trigger Register (a 16-bit value) allows the user to generate an interrupt (or pollable bit) every *N* number of words, where *N* is the value written to this register. For example, to request an interrupt after every five ARINC words, write 05 to this register.

To generate an interrupt or trigger, the appropriate bit must also be set in the Receive Merge Interrupt Condition Register (see **Receive Merge Interrupt/Trigger Condition Register** on page 2-6).

2.2.9 Receive Merge Buffer Wraparound Register Address: 0FF4A (H)

The Receive Merge Buffer Wraparound Register contains 2 bits for synchronization with the host.

Bit	Description
15	Multiple Wraparound - data lost
14	Single Wraparound - the receive buffer has wrapped around once since the last data read
00–13	Reserved

Receive Merge Buffer Wraparound Register

2.2.10 Receive Merge Word Count Trigger Register Address: 0FF4C (H)

The Receive Merge Word Count Trigger Register sets a trigger (used for polling or interrupts) and a flag that indicates when a specific number of words have been received (1 - 65535).

To generate a trigger or interrupt, the appropriate bit in the Receive Merge Interrupt/ Trigger Condition Register must also be set. (see **Receive Merge Interrupt/ Trigger Condition Register** on page 2-6).

Note: This trigger is set when the value in the Receive Merge Word Counter matches the value set in this register.

2.2.11 Receive Merge Word Counter Address: 0FF4E (H)

The Receive Merge Word Counter indicates the number of ARINC words received (0 - 65535). This register wraps around to 0 after it reaches 65535. The user can reset the register only when the channel is stopped.

2.2.12 Receive Merge Filter Table Start Address Address: 0FF50 (H)

The Receive Merge Filter Table Start Address sets the start address of the (256×16) Label Filter Table as described in the Sequential Storage Mode (see section **Receive Buffer Storage Sequence** on page 2-29.) The address must be on a word boundary.

2.2.13 Receive Merge Current Pointer Address: 0FF52 (H)

The Receive Merge Current Pointer indicates the current address where the next ARINC receive word is to be placed in the Receive buffer. This pointer value is incremented after the entire receive block (ARINC word, Time Tag, and Status) is written into memory.

2.2.14 Receive Merge End Pointer Address: 0FF54 (H)

The Receive Merge End Pointer sets the End Address of the Receive Data buffer. The data will wrap around or stop when the buffer is full, (when the End Address is reached), depending upon the contents of the Receive Merge Configuration Register Wraparound bit. (See **Receive Merge Configuration Register** on page 2-6).

2.2.15 Receive Merge Start Pointer Address: 0FF56 (H)

The Receive Merge Start Pointer sets the Start Address of the Receive Data buffer. The address must be on a word boundary within the Receive Data Blocks area.

Example: To cause the Merge buffer to begin at byte offset 001A0 (H), write a 01A0 (H) to this register.

2.2.16 Receive Data Storage Mode Register Address: 0FF58 (H)

The Receive Data Storage Mode register is used to select the Receive Data Storage Mode and the Merge Mode option. ARINC Data Words can be stored with, or without, Time Tag and Status words appended to the data block. The Merge Mode Control Registers are used only when the Merge Mode option is selected.

Bit	Bit Name	Description
05-15	Reserved – set to 0	
04	IRIG B Time Tag	0 = Use a 32-bit, 10 microsecond precision, Time Tag. 1 = Use a 64-bit IRIG B Time Tag. In order to use an IRIG B Time Tag, the module must be mounted on a carrier board that has IRIG B wired to the module, and the carrier board must be receiving an IRIG B signal. The IRIG B input must be using the standard IRIG B120 serial time code.
02-03	Reserved – set to 0	
01	Merge Mode option	0 = Sequential Mode – stores data sequentially per channel, utilizing different receive buffer areas for each channel. 1 = Merge Mode – utilizes a single receive buffer for all channels. Each Receive Status Word is tagged with Channel Code information.
00	Receive Data Storage Mode option	0 = Standard Mode – appends both Time Tag and Status Words to each ARINC word stored in memory 1 = Store Only Data

Receive Data Storage Mode Register

Note: 1. If Data Only Storage Mode is selected (bit 00 set to 1), storage will be per independent channel regardless of the state of bit 01.

2. Data Only Storage Mode is not available in Look-up Table Mode.

3. The Receive Data Storage Mode Register can only be changed when all the channels are turned off for at least 1 msec. (Stop/Start register = 0).

2.2.17 Channel *x* Configuration Status Register

Address: 0FF5A – 0FF6C (H)

These Registers indicate to the host the type of channel configured in each channel socket on the module.

Bit	Description				
04-15	Reserved – set to 0				
00-03	Configuration Status Code				
	Bit 3	Bit 2	Bit 1	Bit 0	Configuration Status Code
	0	0	0	0	Undefined Channel
	0	0	0	1	ARINC-429 Receive Channel
	0	0	1	0	ARINC-429 Transmit Channel

Channel *x* Configuration Status Register

2.2.18 Programmable Bit Rate Register

Address: 0FF6E (H)

The Programmable Bit Rate Register selects the programmable bit rate value for the ARINC channels. This register is only read by the firmware when the Start/ Stop Register contains a value of 0, i.e. all channels are inactive for at least 1 msec.

Bit	Description
15	Set to 1
11-14	Reserved – set to 0
00-10	Bit Rate value

Programmable Bit Rate Register

To calculate the Bit Rate Value (BRV)

$$BRV = \frac{5000}{\text{freq (KHz)}} - 1$$

Example: Desired programmable bit rate 12.5 KHz:

$$BRV = \frac{5000}{12.5\text{KHz}} - 1 = 399\text{Dec (018F H)}$$

Write the value 818F (H) to this register.

2.2.19 Interrupt Status Register

Address: 0FF70 (H)

The Interrupt Status Register indicates which channel issued the interrupt: 1 = Active. The status bit or bits are only reset by the user.

Bit	Bit Name
10-15	Reserved – set to 0
09	Channel 9 Interrupt Status Bit
08	Channel 8 Interrupt Status Bit
07	Channel 7 Interrupt Status Bit
06	Channel 6 Interrupt Status Bit
05	Channel 5 Interrupt Status Bit
04	Channel 4 Interrupt Status Bit
03	Channel 3 Interrupt Status Bit
02	Channel 2 Interrupt Status Bit
01	Channel 1 Interrupt Status Bit
00	Channel 0 Interrupt Status Bit

Interrupt Status Register

2.2.20 Firmware Revision Register

Address: 0FF72 (H)

The Firmware Revision Register indicates the revision level of the firmware. For example: 0114 (H) = Rev 1.14.

2.2.21 Board Status Register

Address: 0FF74 (H)

The Board Status Register indicates the result of the module's self-test. The self-test is performed on module power-up and after a software reset. However, on power-up the Channel Status bits (bits 00 – 09) are all set to 0. To test the channels, you must enable the desired channels, select whether the channels should be transmit or receive, then perform a software reset. (See **Channel Enable Register** on page 2-15, **Channel Type Select Register** on page 2-16 and **Software Reset Register** on page 2-14.) After a software reset, the Channel Status bit is set to 1 for each channel that tested OK.

Bit	Bit Name	
14–15	Reserved	Set to 0
13	Extended Time Support	1 = Extended Interblock Time/Data Rate Mode supported 0 = Not supported (See **Interblock Time/Data Rate Word** on page 2-22.)
12	Baud Rate Generator	1 = 40 MHz
11	Host Ready Timeout	
10	Memory Status Bit	1 = Memory OK 0 = Memory failed
09	Channel 9 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
08	Channel 8 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
07	Channel 7 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
06	Channel 6 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
05	Channel 5 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
04	Channel 4 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
03	Channel 3 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
02	Channel 2 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
01	Channel 1 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed
00	Channel 0 Status bit	1 = Channel present and self-test OK 0 = Channel not present or self-test failed

Board Status Register

Note:

- The module continues to operate on condition of channel self-test failure, but will not operate on condition of memory failure.
- To check whether a channel is configured as receive or transmit, read the Channel *x* Configuration Register. See **Channel x Configuration Register** on page 2-55.

2.2.22 Board ID Register — Address: 0FF76 (H)

The Board ID register indicates that the module has completed its initialization sequence and that the module is ready to be accessed by the host. The module writes the value A429 (H) into this register when ready.

2.2.23 Start/Stop Register — Address: 0FF7A (H)

The user can start one or more channels at the same time — wait a minimum of 500 μsec. between writes to this register.

Bit	Description	
10-15	Reserved – set to 0	
09	Channel 9 Start Bit	1 = Start 0 = Stop
08	Channel 8 Start Bit	1 = Start 0 = Stop
07	Channel 7 Start Bit	1 = Start 0 = Stop
06	Channel 6 Start Bit	1 = Start 0 = Stop
05	Channel 5 Start Bit	1 = Start 0 = Stop
04	Channel 4 Start Bit	1 = Start 0 = Stop
03	Channel 3 Start Bit	1 = Start 0 = Stop
02	Channel 2 Start Bit	1 = Start 0 = Stop
01	Channel 1 Start Bit	1 = Start 0 = Stop
00	Channel 0 Start Bit	1 = Start 0 = Stop

Start/Stop Register

Note: Only after the Start/Stop Register contains a 0 for at least 1 msec. do any changes in a channel's Configuration, Programmable Bit Rate, or Receive Data Storage Mode Registers take effect on the module.

2.2.24 Time Tag Reset Register — Address: 0FF7C (H)

Write Writing any value to the Time Tag Reset Register causes the Time Tag to be reset to 0.

2.2.25 Software Reset Register — Address: 0FF84 (H)

Write Writing a 0 to the Software Reset Register resets the module. Following a reset, the module executes a self-test, both memory and channels, clears all the dual-port RAM, resets the module's interrupts and updates the Board Status Register. The module then indicates that it is ready by writing a value of A429 (H) to the Board ID Register.

2.2.26 Time Tag Counter — Address: 0FF90–0FF92 (H)

The two Time Tag Counter Words represent the current value of the free-running 32-bit Time Tag counter. The counter can be read at any time. The following sequence must be kept:

First: 0FF90 H (Lo word – LSB)
Last: 0FF92 H (Hi word – MSB)

The resolution of the counter is 10 μsec. The counter is reset to 0 upon power-up or software reset or through the Time Tag Reset register. After the reset operation, the counter starts counting. When the counter reaches the value FFFF FFFF (H), it wraps around to 0 and continues counting.

2.2.27 Hardware Revision Register — Address: 0FF94 (H)

Read The Hardware Revision register indicates the module type and the revision level of the hardware.

Bit	Description	
12-15	Module type	5 = RT5 A = RT10
00-11	Hardware revision	021 H = Rev 2.1 022 H = Rev 2.2 023 H = Rev 2.3 ... ...

Hardware Revision Register

2.2.28 Channel Enable Register

Address: 0FF98 (H)

Write

The Channel Enable register is used to enable/activate the required channels. This register, in conjunction with the Channel Type Select register, must be set first, before any other operations are carried out on the module. This register is reset to 0000 after module reset.

Note: In order for the on-module micro controller to recognize the channel's definitions, a software reset has to be applied. (See **Software Reset Register** on page 2-14.)

Bit	Description	
10-15	Reserved – set to 0	
09	Channel 9 enable bit	1 = enabled 0 = disabled
08	Channel 8 enable bit	1 = enabled 0 = disabled
07	Channel 7 enable bit	1 = enabled 0 = disabled
06	Channel 6 enable bit	1 = enabled 0 = disabled
05	Channel 5 enable bit	1 = enabled 0 = disabled
04	Channel 4 enable bit	1 = enabled 0 = disabled
03	Channel 3 enable bit	1 = enabled 0 = disabled
02	Channel 2 enable bit	1 = enabled 0 = disabled
01	Channel 1 enable bit	1 = enabled 0 = disabled
00	Channel 0 enable bit	1 = enabled 0 = disabled

Channel Enable Register

2.2.29 Channel Type Select Register

Address: 0FF9A (H)

Write

The Channel Type Select Register sets each channel's type, either transmit or receive. This register, in conjunction with the Channel Enable Register, must be set prior to any other operations are carried out on the module. This register is reset to 0000 after module reset. See the Module Operation Flowchart on page 1-4.

Note: In order for the on-module micro-controller to recognize the channel's definitions, a software reset has to be applied. (See **Software Reset Register** on page 2-14.)

Bit	Description	
10-15	Reserved – set to 0	
09	Channel 9 type select bit	1 = transmit 0 = receive
08	Channel 8 type select bit	1 = transmit 0 = receive
07	Channel 7 type select bit	1 = transmit 0 = receive
06	Channel 6 type select bit	1 = transmit 0 = receive
05	Channel 5 type select bit	1 = transmit 0 = receive
04	Channel 4 type select bit	1 = transmit 0 = receive
03	Channel 3 type select bit	1 = transmit 0 = receive
02	Channel 2 type select bit	1 = transmit 0 = receive
01	Channel 1 type select bit	1 = transmit 0 = receive
00	Channel 0 type select bit	1 = transmit 0 = receive

Channel Type Select Register

2.2.30 IRIG B Time Tag Counter 0, 1, 2 and 3

Address: 0FFC0, 0FFC2, 0FFC4, 0FFC6 (H)

Read

This 64-bit counter is read from four locations starting at FFC0 (H) and ending at FFC6 (H). Reading FFC0 (H) freezes the current counter values until the last location (FFC6 (H)) is read. Its value represents the IRIG B time received in addition to a six BCD digit 1 µsec counter. When no IRIG B signal is received from an external source, the counter continues counting based on an internal source. When running based on the internal source, the counter can be loaded with "preload" values, which are starting values that the counter will use.

Bit	Description
00–15	1 µsec counter (4 Lo BCD digits)

IRIG B Time Tag Counter 0 – Address FFC0 (H)

Bit	Description
08–15	IRIG B Seconds (2 BCD digits)
00–07	1 µsec counter (2 Hi BCD digits)

IRIG B Time Tag Counter 1 – Address FFC2 (H)

Bit	Description
08–15	IRIG B Hours (2 BCD digits)
00–07	IRIG B Minutes (2 BCD digits)

IRIG B Time Tag Counter 2 – Address FFC4 (H)

Bit	Description
15	0 = Time Tag updating from an external source 1 = No IRIG B signal; updating Time Tag from internal source
12–14	Reserved – set to 0
00–11	IRIG B Days (3 BCD digits)

IRIG B Time Tag Counter 3 – Address FFC6 (H)

2.2.31 IRIG B Preload Seconds

Address: 0FFD2 (H)

Read/Write This register loads the IRIG B seconds to the IRIG B Time Tag Counter. Its value is loaded when any value is written to the IRIG B Load Counter (at FFD8 (H)) and the IRIG B counter is updating from an internal source. (See Bit 15 of the IRIG B Time Tag Counter.) All bits of this register are set to 0 at power-up.

Bit	Bit Name	Description
12–15	SecDig1	Seconds Digit_1 Preload Value (0-5)
08–11	SecDig0	Seconds Digit_0 Preload Value (0-9)
00–07	Reserved	Set to 0 (reserved for upper 2 microsecond digits)

IRIG B Preload Seconds Register

2.2.32 IRIG B Preload Minutes/Hours

Address: 0FFD4 (H)

Read/Write This register loads the IRIG B minutes and hours to the IRIG B Time Tag Counter. Its value is loaded when any value is written to the IRIG B Load Counter (at 70D8 (H)) and the IRIG B counter is updating from an internal source. (See Bit 15 of the IRIG B Time Tag Counter.) All bits of this register are set to 0 at power-up.

Bit	Bit Name	Description
12–15	HrsDig1	Hours Digit_1 Preload Value (0-2)
08–11	HrsDig0	Hours Digit_0 Preload Value (0-9)
04–07	MinDig1	Minutes Digit_1 Preload Value (0-5)
00–03	MinDig0	Minutes Digit_0 Preload Value (0-9)

IRIG B Preload Minutes/Hours Register

2.2.33 IRIG B Preload Days

Address: 0FFD6 (H)

Read/Write This register loads the IRIG B days to the IRIG B Time Tag Counter. Its value is loaded when any value is written to the IRIG B Load Counter (at FFD8 (H)) and the IRIG B counter is updating from an internal source. (See Bit 15 of the IRIG B Time Tag Counter.) Bits 01 – 15 of this register are set to 0 at power-up. Bit 00 is set to 1 at power-up.

Bit	Bit Name	Description
12–15	Reserved	Set to 0
08–11	DayDig2	Days Digit_2 Preload Value (1-3)
04–07	DayDig1	Days Digit_1 Preload Value (0-9)
00–03	DayDig0	Days Digit_0 Preload Value (0-9)

IRIG B Preload Days Register

2.2.34 IRIG B Load Counter

Address: 0FFD8 (H)

Write Writing any value to this register loads the values in registers FFD2 (H) – FFD6 (H) to the IRIG B Time Tag Counter when the IRIG B counter is updating from an internal source. (See Bit 15 of the IRIG B Time Tag Counter 3.)

2.3 Transmit Channel Operation

Each transmit channel has three basic modes of operation: Interblock Time Mode, Data Rate Mode and FIFO Mode.

Interblock Time Mode and Data Rate Mode are described in the following sections. FIFO Mode is described in **2.3.2 FIFO Mode** on page 2-24.

Note: In addition to the above modes, there is also a Translation Mode, which uses one channel to receive and one channel to transmit. For more information, see **2.5 Translation (Dual Channel) Operation** on page 2-37.

2.3.1 Interblock Time Mode and Data Rate Mode

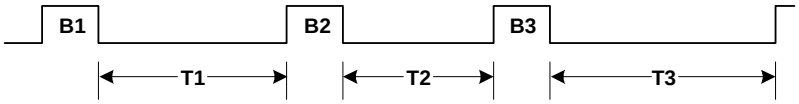
The transmit mode is selected via the Channel *x* Configuration register. See **Channel x Configuration Register** on page 2-55.

In Interblock Time and Data Rate modes, Words are sent out in blocks (groups of Words). Each block is sent with dedicated parameters including word count, interblock time (or data rate) and error injection. The blocks reside sequentially in stack structure, each pointing to its Data Buffer. In Interblock Time Mode, the blocks can be sent either continuously or *N* times. In Data Rate Mode, blocks are always sent continuously.

Interblock Time Mode and Data Rate Mode are recommended for use when transmitting the same data repeatedly or when the data to transmit needs to be updated in real-time. For transmitting a large amount of known data, such as a file, it recommended to use FIFO Mode. (See **2.3.2 FIFO Mode** on page 2-24.)

Note: When using Data Rate Mode, the value of the Channel *x* Transmit Loop Counter register is ignored and the data is transmitted continuously. See **Channel x Transmit Loop Counter** on page 2-51.

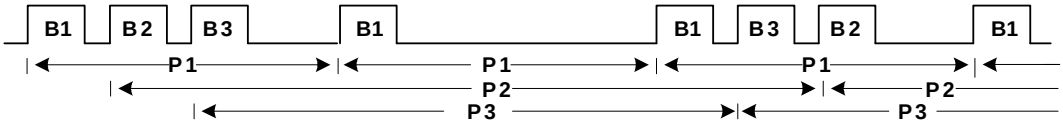
Interblock Time Mode sends out blocks of Words sequentially; each block has its own Interblock delay time.



B - Block
T - Interblock time

Figure 2-2 Interblock Time Mode

Data Rate Mode sends out blocks of Words periodically; each block is sent according to it's own data rate.



B - Block
T - Interblock time
P - Block period time

Figure 2-3 Data Rate Mode

To use Interblock Time Mode or Data Rate Mode, set bits 11 and 12 of the Channel x Configuration Register to 0, and select either Interblock Time Mode or Data Rate Mode by setting Bit 08 of this register to 0 or 1.

In these modes, the user:

- Sets up the transmitting channel's parameters by writing to the various Channel *x* Control Registers.
- Creates an Instruction Stack for the transmitting channel.
- Writes the data into the dual-port RAM.
- Starts transmission by writing to the Start/Stop Register found within the ARINC 429 Module Global Control Register area.

The sequence of writes to memory is not important, except for the write to Start Register operation, which is performed last.

Transmit Instruction Block

The Transmit Instruction Stack is divided into Instruction Blocks, each containing four Words. Each Instruction Block relates to a Data Buffer. A Data Buffer contains one or more ARINC Words which the user desires to transmit with the same amount of delay time between each Word. The stack is sequential, so that the first Instruction Block follows the second Data Block, and so on.

The Instruction Block consists of:

1st Word: The Control Word, which contains error injection parameters.

2nd Word: Contains 2 bytes:

- An 8-bit Word Count which instructs the module as to the number of ARINC Words to transmit within a particular block, and
- An 8-bit, inter-word delay value which programs the time between Words within the same buffer.

3rd Word: Contains a 16-bit, user-supplied data pointer. This is a 16-bit address (must be a Word boundary) that points to the beginning of the Data Words within the memory.

4th Word: Is the Interblock Time/Data Rate value and is used to program the time between Data Block transfers or the transmission period for the specific data block.

Figure 2-4 illustrates the Transmit Instruction Stack structure.

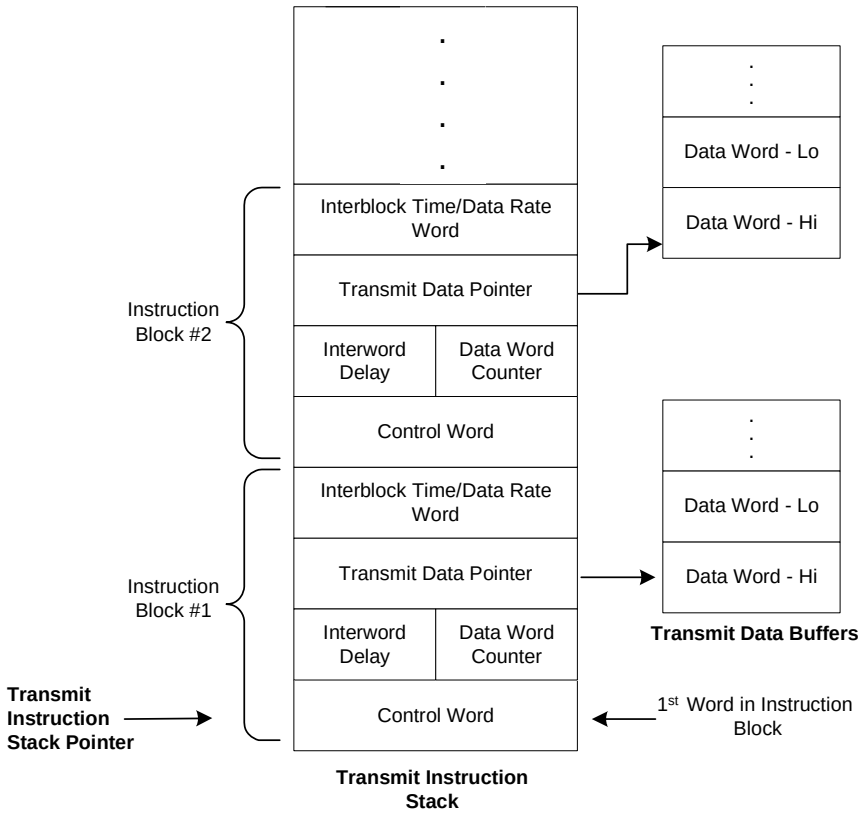


Figure 2-4 Transmit Instruction Stack Structure

Control Word Definition

This is the 1st Word in the ARINC Transmit Instruction Block.

Bit	Bit Name	Description
06-15	**Reserved**	Set to 0
05	**Suppress Parity [1]**	1 = Forces a no-parity condition within the Word even though 'parity-on' has been selected in the Channel *x* Configuration Register 0 = Regular parity as set up in the Channel *x* Configuration Register
04	**Bit Count Lo Error**	1 = Thirty-one ARINC bits are transmitted within each Word within the block 0 = No error
03	**Bit Count Hi Error**	1 = Thirty-three ARINC bits are transmitted within each Word within the block 0 = No error
02	**Stretch Bit Error**	1 = The 2nd ARINC bit within each Word within the block is 'stretched' causing a Manchester coding error. 0 = No error
01	**Null Bit Error**	1 = A Null Bit Error is inserted within the second bit of each Word within the block (ARINC Bit 02). 0 = No error
00	**Parity Error**	1 = A Parity Error is inserted within all ARINC Words within the block. 0 = No error

Control Word Definition

1. The **Suppress Parity** is useful when most of the Data Buffers contain standard data with parity and a few buffers contain data type without parity. In such a case, the parity can be set ON for all Words within the Channel x Configuration Register while exceptional cases, can be forced to NO PARITY, using this bit.

Interword Delay/Data Word Counter Word

This Word is divided into two bytes, the Interword Delay (high byte) and the Data Word Counter (low byte).

The Interword Delay byte specifies the time between Words within this data block. The resolution is in the form of 'bit times' according to the transmission bit rate.

Bit Rate	Resolution
Lo-Speed	80μsec/bit
Hi-Speed	10μsec/bit
Programmable	$\frac{1}{\text{Programmable Bit Rate (MHz)}}$

Interword Delay Resolution

Note: The ARINC specification defines the minimum Interword time as 4 bit times, so values less that 4 may be interpreted on the receiving side as Sync error.

The Word Counter byte specifies the number of data Words within this Data block (1-255).

Transmit Data Pointer

The Transmit Data Pointer is used to set the start address of the block's Transmit Data Buffer. The address must be a Word boundary. The size of the buffer is determined by the Data Word Count value.

Interblock Time/Data Rate Word

The Interblock Time/Data Rate Word has two functions:

- In **Interblock Time Mode,** the Instruction Blocks are accessed sequentially and their associated Data Words transmitted according to this sequential order. The Interblock Time allows the user to specify the time between Data Blocks. It is inserted after the block transmission.
- In **Data Rate Mode**, the user can specify the transmission period of the particular Data Block. If the number *N* is written to this location, then the message is transmitted every *N* bit times.

The resolution of this 16-bit Word is according to the bit rate selected in the Channel *x* Configuration register, which is the same as in the Interword Delay byte. (For a detailed explanation of the resolution, see **Interword Delay/Data Word Counter Word** on page 2-22).

The maximum value for the Interblock Time/Data Rate is 65,535 bit times, which is 655 msec. in Hi-speed and 5,243 msec. in Lo-speed. When a longer Interblock Time/Data Rate is required, the user can enable Extended Time Mode. In Extended Time Mode, the actual Interblock Time/Data Rate implemented on the

bus will be twice the specified value. (See **Channel x Configuration Register** on page 2-55.)

Note: In Data Rate Mode, a scratch buffer for the firmware must be allocated via the **Channel x Scratch Buffer Start Register** and **Channel x Scratch Buffer End Register,** see page 2-50. This buffer must be at least eight bytes long for each block defined.

Transmit Data Block Format

Figure 2-5 illustrates the format of the Transmit Data Words within the memory.

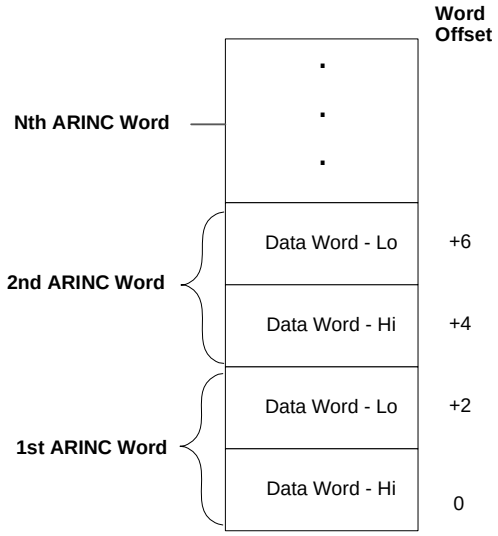


Figure 2-5 Transmit Data Block

Figure 2-6 defines the locations and bit definitions of the data bytes within the memory. The numbers shown in the two Words represent the ARINC Word bit numbers.

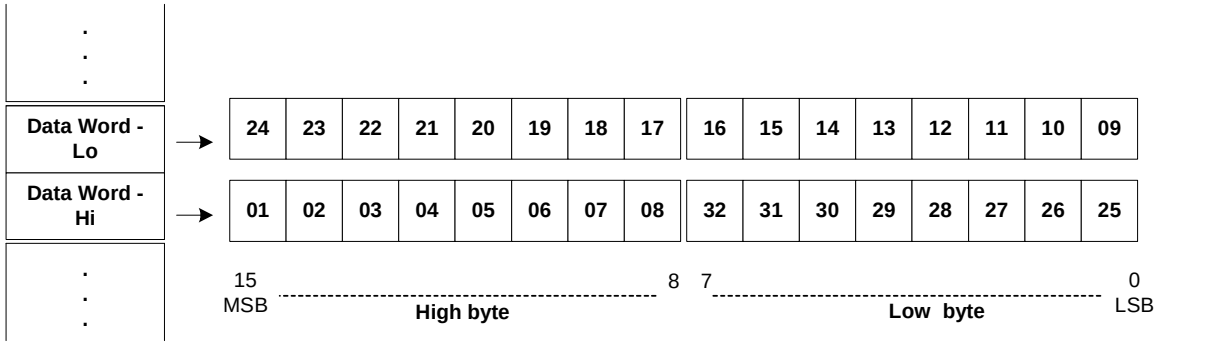


Figure 2-6 32-Bit Transmit Data Words Format

1. The numbers contained within the Words in Figure 2-6 represent the ARINC bit locations within the 32-bit Word.
2. The ARINC Word bits are transmitted in the following order:

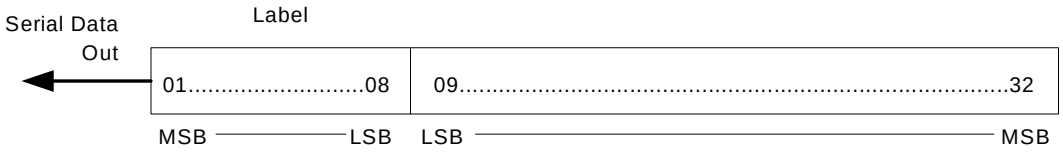


Figure 2-7 32-Bit Word Transmit Order Bit

3. Bits 09 through 32 are ordered from LSB to MSB (as opposed to the Label field that is organized from MSB to LSB). For this reason, in the Data Block, the Hi-Word is first, followed by the Lo-Word, with the label and the ARINC field 32 through 25 in the Hi-Word and bits 24 through 09, in the Lo-Word.

2.3.2 FIFO Mode

FIFO Mode is selected via the Channel *x* Configuration register. See **Channel x Configuration Register** on page 2-55.

In this mode, the user may define multiple buffers for each channel. Each buffer is used to transmit labels at a selected frequency. If a buffer is defined to transmit at a frequency of 50 milliseconds, the labels in that buffer will be transmitted at a rate of one 32-bit word every 50 milliseconds. If the length of the buffer is set to ten words, the first word will be sent at time 0,the second 50 milliseconds later and so on, until the final word is sent 450 milliseconds after the first. While these words are being transmitted, the user may refill the buffer, thereby creating a situation in which data is being transmitted at a constant rate. The user only needs to update the buffer every 500 milliseconds.

FIFO Mode is recommended for use when transmitting a large amount of known data, such as a file. When transmitting the same data repeatedly or when the transmitted data changes in real-time, it is recommended to use Interblock Time Mode or Data Rate Mode. (See **2.3.1 Interblock Time Mode and Data Rate Mode** on page 2-19.)

Note: When using FIFO Mode, the value of the Channel *x* Transmit Loop Counter register is ignored and the data is transmitted continuously. See **Channel x Transmit Loop Counter** on page 2-51.

In this mode, the user:

- Sets up the transmitting channel's parameters by writing to the various Channel *x* Control Registers.
- Allocates the number of buffers desired for each channel.
- Creates the buffers.
- Writes the data into the buffers.
- Starts transmission by writing to the Start/Stop Register found within the ARINC 429 Module Global Control Register area.

The sequence of writes to memory is not important, except for the write to Start Register operation, which is performed last.

Allocating Space for Buffer Pointers

Set the Transmit Instruction Stack Pointer to point to an array of 16-bit words, which will be used as pointers to the buffers. This array is called the array of buffer pointers.

Set the Transmit Instruction Counter to the number of buffers that will be created.

Allocating Buffers

Set an entry within the array of buffers to point to the buffer to be allocated. Allocate space for a 10 word header plus 3 words for each message in the buffer, with each word containing 16 bits. For example, for a 15 message buffer, allocate 55 16-bit words.

Figure 2-8 illustrates the structure of one buffer.

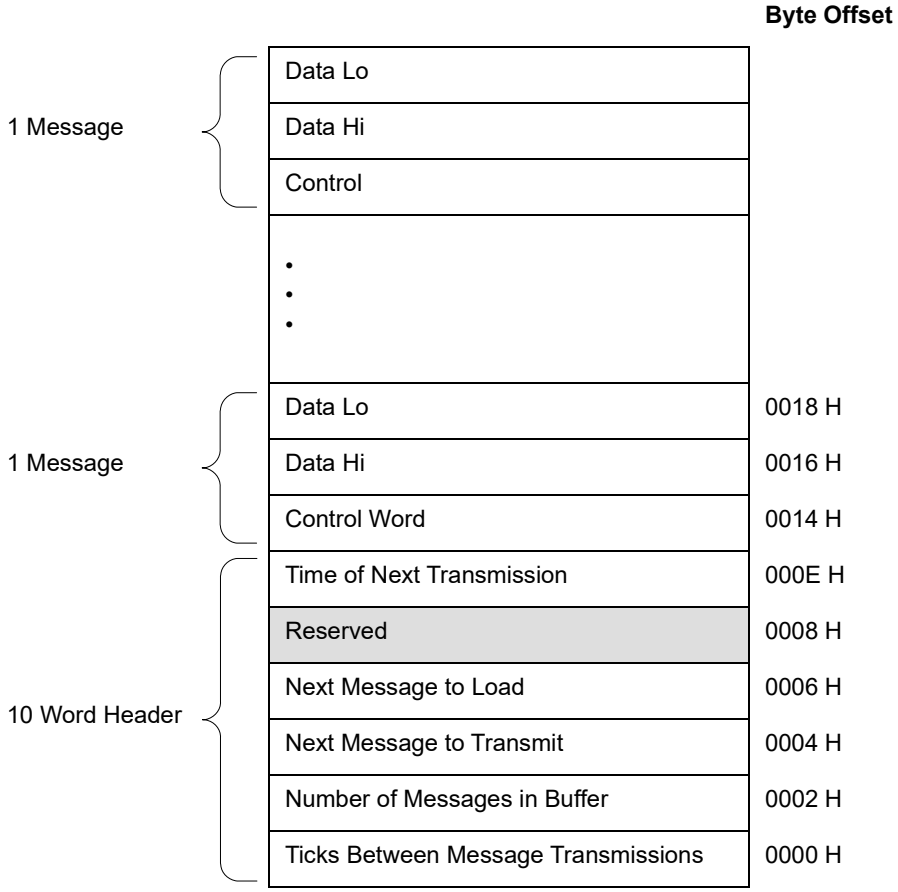


Figure 2-8 Buffer Structure

Ticks Between Message Transmissions **Byte Offset: 0000 (H)**

The number of ticks between the transmission of each message in the buffer. Each tick is 100 microseconds. This allows up to six seconds between message transmission.

Number of Messages in Buffer **Byte Offset: 0002 (H)**

How many messages are in the buffer. When this number is reached, the module wraps around to the start of the message area.

Next Message to Transmit **Byte Offset: 0004 (H)**

The index of next word to transmit. This must be initialized to 0. It is updated by the firmware.

Next Message to Load **Byte Offset: 0006 (H)**

Index of the next message that **Load_Transmit_FIFO_RTx** will load. This is not used by the firmware but is here for the use by the host software.

Time of Next Transmission **Byte Offset: 000E (H)**

Time Tag of the next transmission. This must be initialized to 0. It is updated by the firmware.

Control Word **Byte Offset: 0014 (H)**

Bit	Bit Name	Description
06-15	**Reserved**	Set to 0
05	**Suppress Parity** [1]	1 = Forces a no-parity condition within the Word even though 'parity-on' has been selected in the Channel *x* Configuration Register 0 = Regular parity as set up in the Channel *x* Configuration Register
04	**Bit Count Lo Error**	1 = Thirty-one ARINC bits are transmitted within each Word within the block 0 = No error
03	**Bit Count Hi Error**	1 = Thirty-three ARINC bits are transmitted within each Word within the block 0 = No error
02	**Stretch Bit Error**	1 = The 2nd ARINC bit within each Word within the block is 'stretched' causing a Manchester coding error. 0 = No error
01	**Null Bit Error**	1 = A Null Bit Error is inserted within the second bit of each Word within the block (ARINC Bit 02). 0 = No error
00	**Parity Error**	1 = A Parity Error is inserted within all ARINC Words within the block. 0 = No error

Control Word Definition

1. The **Suppress Parity** is useful when most of the Data Buffers contain standard data with parity and a few buffers contain data type without parity. In such a case, the parity can be set ON for all Words within the Channel x Configuration Register while exceptional cases, can be forced to NO PARITY, using this bit.

Data Hi **Byte Offset: 0016 (H)**

The high 16 bits of the transmit data.

Data Lo **Byte Offset: 0018 (H)**

The low 16 bits of the transmit data.

2.4 Receive Channel Operation

The user sets up each receive channel's mode of operation by writing to various Control Registers (global and channel specific). Each receive channel has three basic modes of operation:

Sequential Mode:	Stores data sequentially per channel, utilizing different receive buffer areas for each channel
Merge Mode:	Stores all receive channel data sequentially into one receive buffer area
Look-Up Table Mode:	Allows the user to store Words in specific locations of memory according to the label

In all these modes, the Data Words are stored with a 16-bit Receive Status Word and a Time Tag value. In Data Only option the Status and Time Tag are not stored. In Merge Mode, the channel ID information (indicates on which channel the data was received) is contained within the Receive Status Word.

The format of the Time Tag depends on the value of the IRIG Time Tag bit in the Receive Data Storage Mode register. See **Receive Data Storage Mode Register** on page 2-9. The two Time Tag formats are described in **Time Tag Word Format** on page 2-31.

In Receive Channel Operation the module is initialized in a wait loop, looking for a START command from the computer. This command is issued by writing to the Global Start Register. (See the **Global Start/Stop Register** on page 2-13). The command instructs the module to begin operation on the selected channels.

Sequential and Merge modes are described in detail in the following sections. Look-Up Table Mode is described in **2.4.2 Look-up Table Mode Operation** on page 2-35.

Note: In addition to the above modes, there is also a Translation Mode, which uses one channel to receive and one channel to transmit. For more information, see **2.5 Translation (Dual Channel) Operation** on page 2-37.

2.4.1 Sequential and Merge Modes

Sequential Mode

The Sequential Mode has a software-selectable feature that filters the storage of the specific, user-defined labels or stores all labels within one buffer. (See Figure 2-9 **Receive Sequential Mode Buffer Structure with Standard Time Tags** on page 2-30.) The data buffer's size and location within the memory is programmed via a Start and End pointer. (See **Channel x Receive Data Start Pointer** and **Channel x Receive Data End Pointer**, on page 2-54). Each received ARINC Data Word is tagged with a status Word, indicating the status of the receive Word and a 32-bit Time Tag value.

These five, 16-bit Words make up a single receive data block. Alternatively, the Sequential Mode offers the user the capability of storing only the ARINC data without the Time Tag and Status Words. This global selection affects all receive channels. (See **Receive Data Storage Mode Register** on page 2-9.) A 16-bit register indicates the number of invalid Words received. Interrupts and pollable status registers allow for numerous event recognition and are described in the Channel

Control Register section of this manual. (See **Channel x Configuration Register** on page 2-55).

To use Sequential Mode, set Bit 01 of the Receive Data Storage Mode Register to 0 and set Bit 05 of the Channel x Configuration Register to 1.

Merge Mode

The Merge Mode operates in the same manner as the Sequential Mode except that all the receive channels are merged into one Data Buffer area. If data from different channels is to be processed similarly, using Merge Mode is more efficient than reading data from each channel separately.

The Control registers for the Merge Mode are located on the **ARINC 429 Module Global Registers Map** on page 2-3 and defined in section **2.2 ARINC 429 Module Global Register Definitions**.

In this mode the Receive Data Blocks are stored in sequential order and each receive Status Word is tagged with a channel ID, indicating the channel on which the data was received. Each data block contains a Time Tag word as in the standard Sequential Mode of operation.

To use Merge Mode, set Bit 01 of the Receive Data Storage Mode Register to 1. When this bit is set to 1, Bit 05 of the Channel x Configuration Register is ignored.

Receive Buffer Storage Sequence

Figures 2-9 and 2-10 illustrate how Receive Data Blocks are stored within the dual-port RAM, while in the Sequential Mode of operation.

The Channel *x* Receive Error Count Register (see page 2-52) is updated with every invalid Word which is stored. The Start and End pointers set up the buffer size. The Receive Data Storage will stop when the end pointer is reached or will wrap around to the beginning of the buffer, depending upon the condition of the Receive Wrap Around bit in the Channel *x* Configuration Register (see page 2-55). The format of the Time Tag depends on the value of the IRIG Time Tag bit in the Receive Data Storage Mode register. (See **Receive Data Storage Mode Register** on page 2-9.)

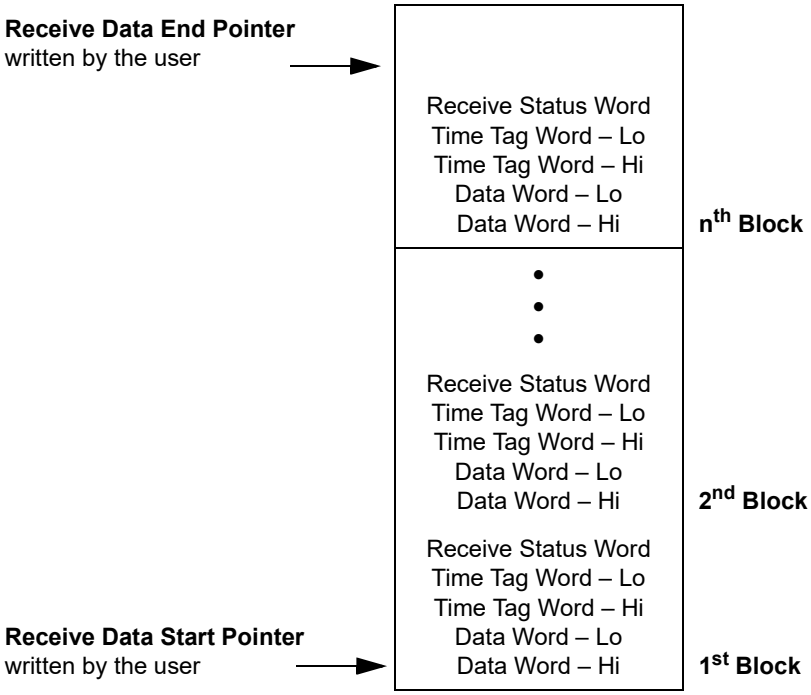


Figure 2-9 Receive Sequential Mode Buffer Structure with Standard Time Tags

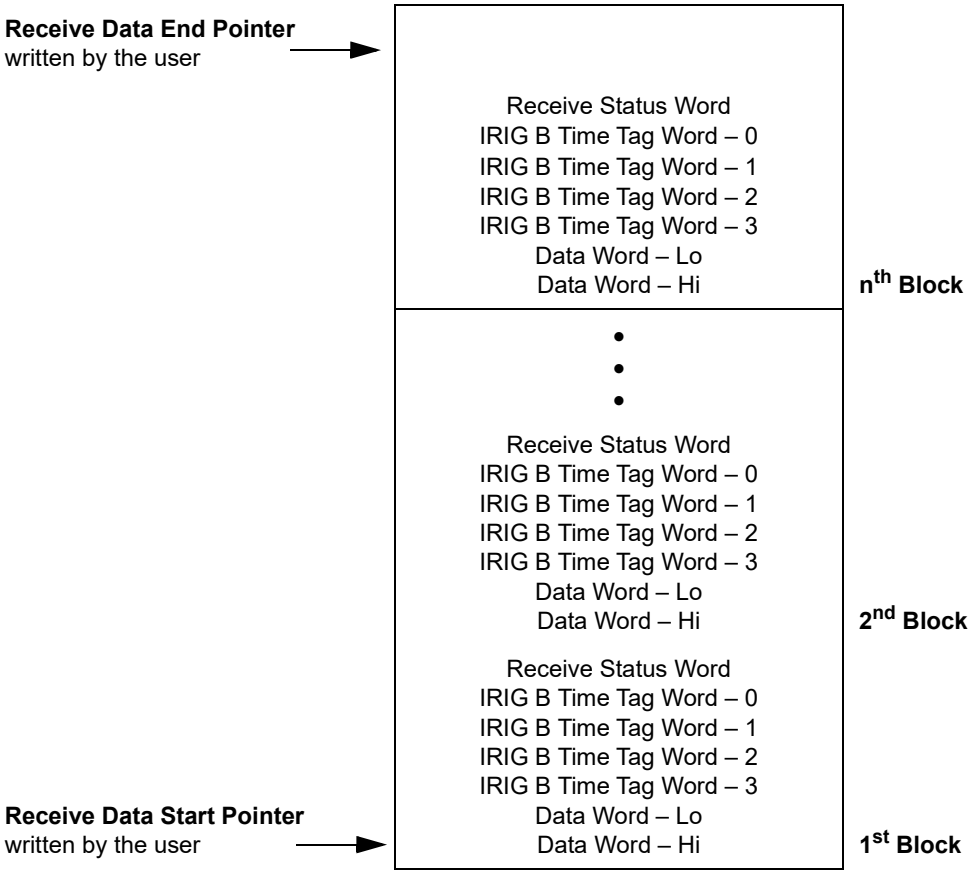


Figure 2-10 Receive Sequential Mode Buffer Structure with IRIG B Time Tags

Receive Data Word Format

The received ARINC Word is stored as two 16-bit Words within the memory (Hi-word followed by a Lo-word).

The numbers shown within the two Words represent the ARINC bit numbers.

32-Bit ARINC Word Receive Format

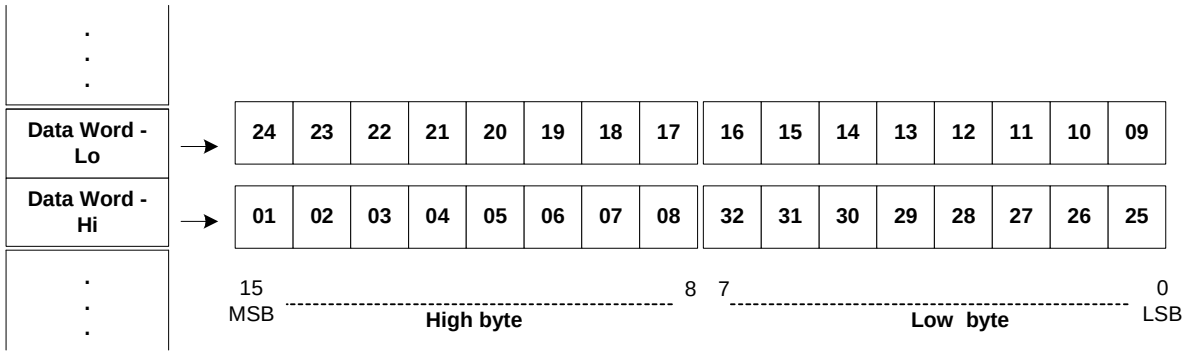


Figure 2-11 32-Bit Receive Data Word Format

Note: 1. The ARINC Word bits are received in the following order:

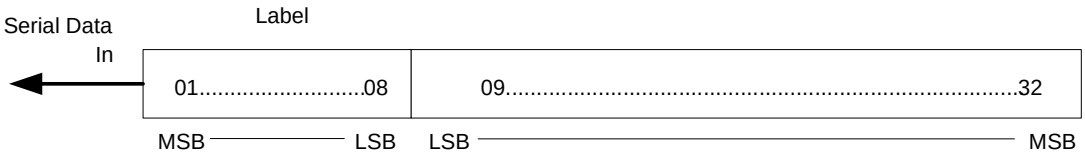


Figure 2-12 32-Bit ARINC Word Order Bit

2. Bits 09 through 32 are ordered from LSB to MSB (as opposed to the Label field which is organized from MSB to LSB). For this reason, in the Data Block the Hi-word is first, followed by the Lo-word, with the Label and the ARINC field 32 through 25 in the Hi-word, and bits 24 through 09, in the Lo-word.

Time Tag Word Format

The format of the Time Tag depends on the value of the IRIG Time Tag bit in the Receive Data Storage Mode register. (See **Receive Data Storage Mode Register** on page 2-9.)

Standard (Non-IRIG B) Time Tag Format

When using the standard (non-IRIG B) Time Tag, the Time Tag is a 32-bit Word made up of two 16-bit Words: Time Tag-Hi and Time Tag-Lo. The Time Tag resolution is 10 microseconds.

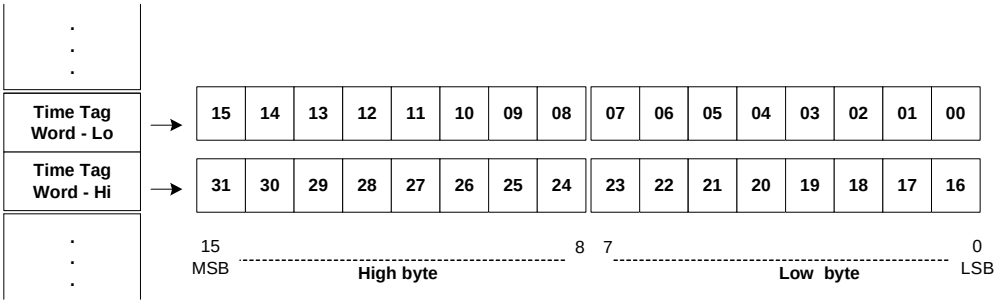


Figure 2-13 Time Tag Word Format in Standard (Non-IRIG B) Mode

IRIG B Time Tag Format

When using the IRIG B Time Tag, the Time Tag is made up of four 16-bit Words.

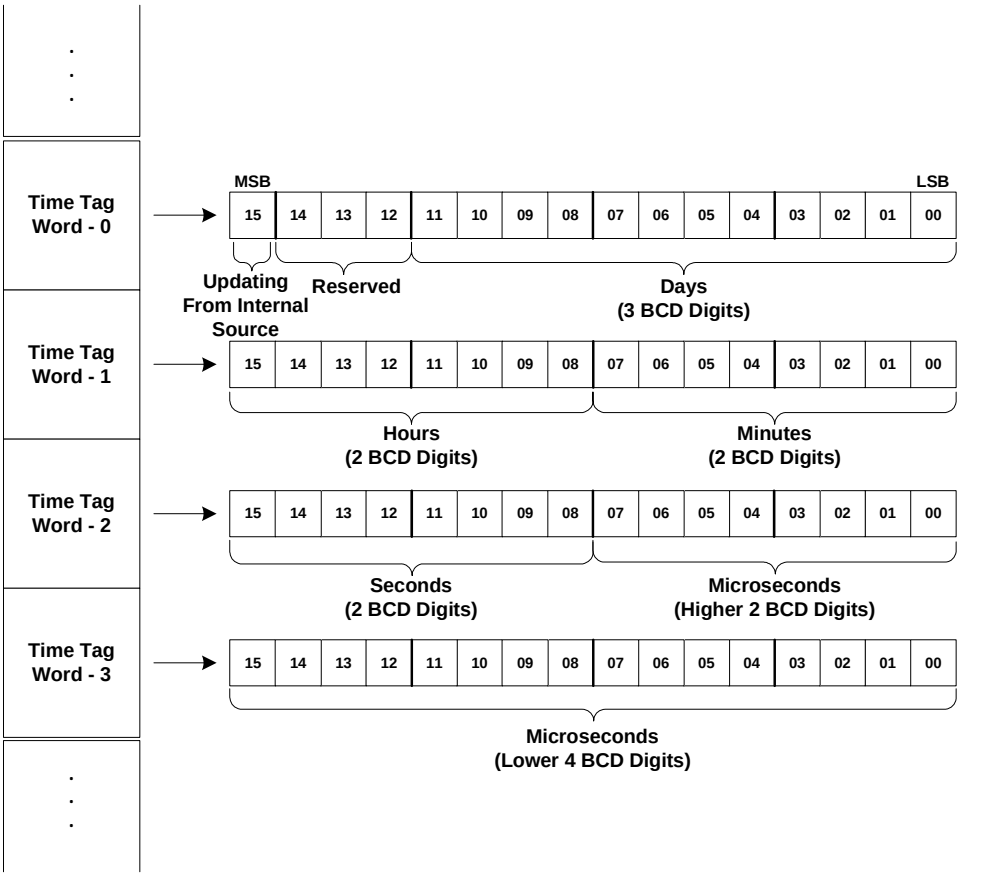


Figure 2-14 Time Tag Word Format in IRIG B Mode

The Updating from Internal Source bit indicates whether a valid IRIG B signal is being received by the module. When this bit is set to 1, the module is not receiving an IRIG B signal, and the module is updating the Time Tag based on its internal clock.

Receive Sequential Mode Status Word

Bit	Bit Name	Description
12-15	**Reserved**	
08-11	**Merge Channel ID Code** ***(Merge Mode only)***	0000 – Data received over Channel 0 0001 – Data received over Channel 1 0010 – Data received over Channel 2 0011 – Data received over Channel 3 0100 – Data received over Channel 4 0101 – Data received over Channel 5 0110 – Data received over Channel 6 0111 – Data received over Channel 7 1000 – Data received over Channel 8 1001 – Data received over Channel 9 **Note**: Channel ID Code: bit 8 = LSB Channel ID Code: bit 11 = MSB
07	**Valid Word**	1 = The Received ARINC word was valid in all respects (Global bit). 0 = Not a valid Word
06	**Reserved**	
05	**Gap [Sync] Time Error**	1 = Gap [Sync] Time Error occurred between Words (less than a 4 bit times between Words. 0 = No error
04	**Invalid Coding Error**	1 = Bit level coding error was detected in the ARINC Word 0 = No error
03	**Parity Error**	1 = A parity error was detected in the ARINC Word. 0 = No error
02	**Lo Bit Count / Invalid Word Error**	1 = A Lo Bit Count or a Null bit Error was detected in the ARINC Word. 0 = No error
01	**Hi Bit Count Error**	1 = A Hi Bit Count or a Null bit Error was detected in the ARINC Word. 0 = No error
00	**Word Received**	1 = Data is in memory. This bit is cleared while data is in the process of being updated. 0 = No received Word

Receive Sequential Mode Status Word

Receive Sequential Mode Filter Table Diagram

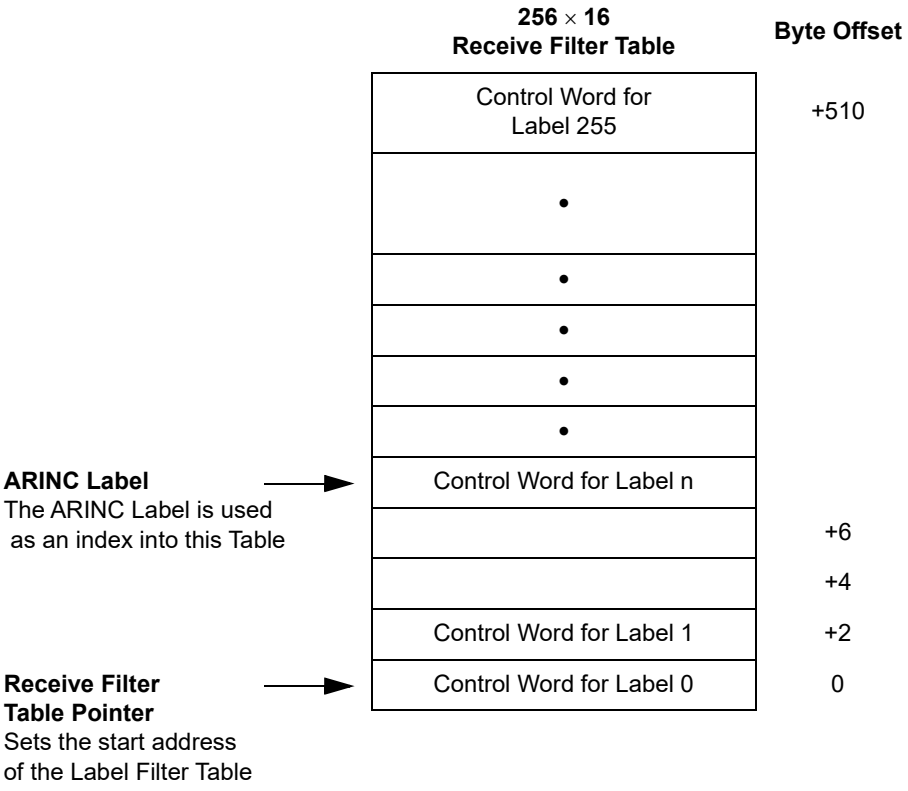


Figure 2-15 Receive Sequential Mode Filter Table Diagram

Bit	Description
02-15	Reserved
01	1 = Interrupt 0 = Don't Interrupt
00	1 = Store Word 0 = Don't Store

Label Control Word Structure (Write)

2.4.2 Look-up Table Mode Operation

In Look-up Table Mode, the Word's label is used by the module as an offset to a 256-word Look-up Table. The Table is programmed by the user with address pointers as to where to write the Receive Data Block. Each block contains a:

- 32-bit ARINC Word,
- 32-bit Time Tag
- Error Count Word
- Status Word

The 256-word Table can be placed anywhere within the memory via a user-programmable Receive Look-up Table Start Address Register.

The user has the ability to monitor the operational status of each channel and to be interrupted on various events. In addition, there exist pollable registers that can be used with or instead of interrupt processing.

To use Look-up Table Mode, set Bit 05 of the Channel x Configuration Register to 0 and set Bit 01 of the Receive Data Storage Mode Register to 0.

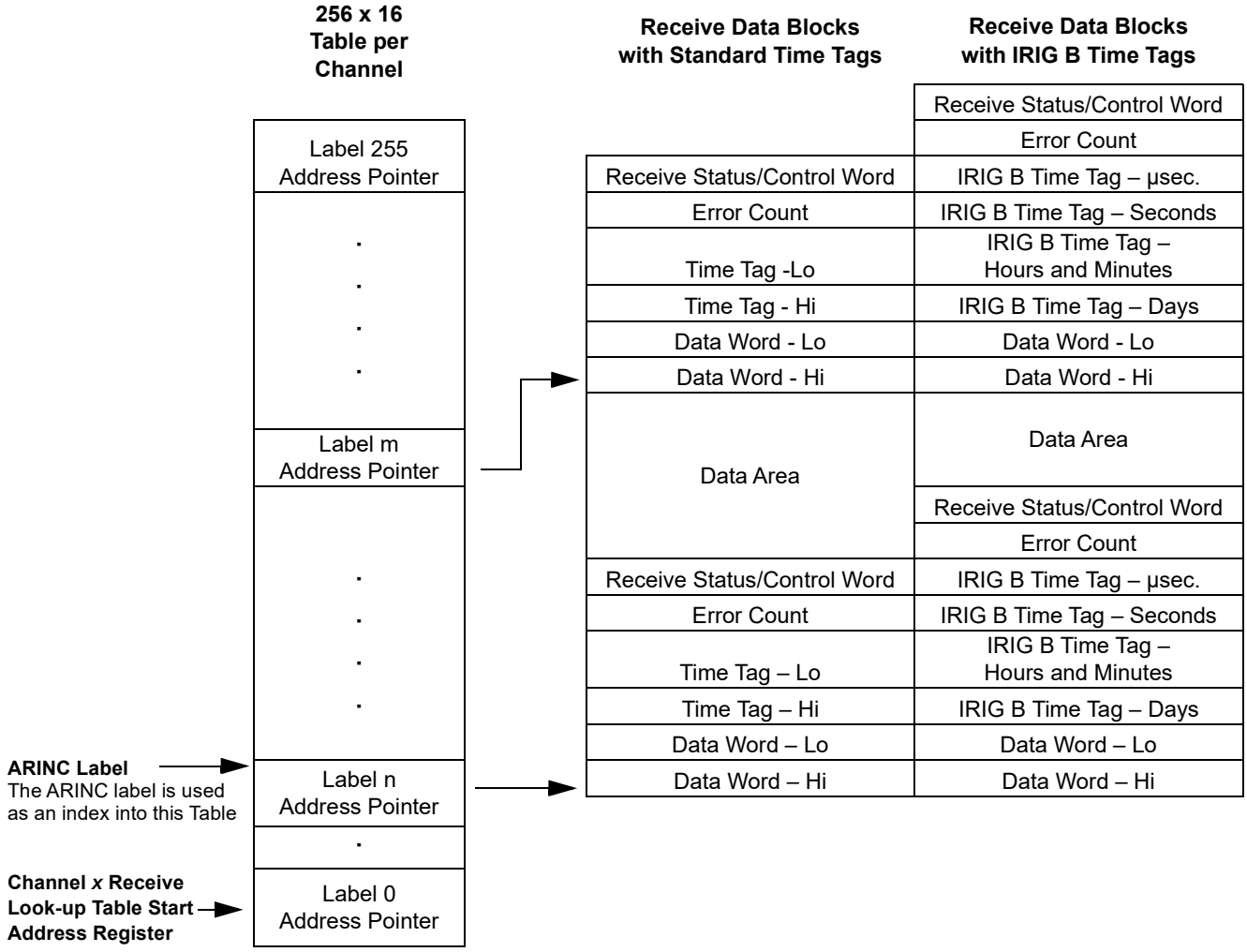


Figure 2-16 Receive Look-up Table Structure

Receive Data Block Description

The Receive Data Block components are:

Data Word The ARINC Data Word is stored as two 16-bit Words with the same format as Sequential Mode. See **Receive Data Word Format** on page 2-31.

Time Tag Word The standard (non-IRIG B) Time Tag Word is stored in two 16-bit Words with the same format as Sequential Mode.

The IRIG Time Tag is stored in four 16-bit Words with the same format as Sequential Mode.

See **Time Tag Word Format** on page 2-31.

Error Count Word The Error Count Word indicates the number of error Words received on a particular label.

Receive Status/ Control Word See **Table 2-1 Look-up Table: Received Status/Control Word**.

	Bit	Bit Name	Description
Control Byte	**15**	Enable Label Interrupt	Enables the 'interrupt on label received' capability. This bit is used in conjunctions with the Channel *x* Interrupt/ Trigger Condition Register
	08–14	Reserved	Set to 0
Status Byte	**07**	Valid Word	1 = The Received ARINC Word was valid in all respects (Global bit) 0 = Not a valid Word
	06	Reserved	Set to 0
	05	Gap[Sync] Time Error	1 = Gap[Sync] Time Error occurred between Words (less than 4 bit times between Words.) 0 = No error
	04	Invalid Coding Error	1 = Bit level coding error was detected in the ARINC Word 0 = No error
	03	Parity Error	1 = A parity error was detected in the ARINC Word 0 = No error
	02	Lo Bit Count/ In Valid Word Error	1 = A Lo Bit Count or a Null bit error was detected in the ARINC Word 0 = No error
	01	Hi Bit Count Error	1 = A Lo Bit Count or a Null bit error was detected in the ARINC Word 0 = No error
	00	Word Received	1 = Data is in memory. This bit is cleared while data is in the process of being updated 0 = No Word received

Table 2-1 Look-up Table: Received Status/Control Word

2.5 Translation (Dual Channel) Operation

Translation Mode is selected by setting the Translation Mode bit in the Channel *x* Configuration Register of two contiguous channels. The first of the two channels must be a receive channel, the second must be a transmit channel. In this mode, labels received by the receive channel are retransmitted over the transmit channel after undergoing a translation function. A different translation function may be assigned for each label to be received.

To use Translation Mode, set Bit 11 of the Channel x Configuration Register in the receive channel to 1 and set Bit 12 to 0.

In Data Translation operation the user:

- Sets up the receive and transmit channel's parameters by writing to the various Channel *x* Control Registers. In Translation Mode, only bits 00 – 04 of the transmit channel should be set.
- Allocates a translation table for the receive channel.
- Assigns translation functions.
- Writes the data into the FIFOs.
- Starts operation by writing to the Start/Stop Register found within the ARINC 429 Module Global Control Register area. Only the bits associated with the receive channel must be set.

2.5.1 Allocating a Translation Table in a Channel

Set the Filter Table Start Address to point to an array of 256 16-bit words which will be used as pointers to the translation entries. This array is called the array of translation entries.

2.5.2 Allocating a Translation Table Entry

Set an entry within the array of translation entries to point to the Translation Table entry to be allocated. Space must be allocated for a 12 16-bit words per entry. The index into the array of translation entries corresponds to the label of the word to be translated.

2.5.3 Using Translation Functions

To use translation functions, specify which translation functions you want to use in the highest two words of the Translation Table entry, by setting specific bits to 1, and specify the data to be used for the translation functions in the remaining words of the Translation Table entry. You can use up to five translation functions per Translation Table entry. See Figure 2-17 and the following sections.

The structure of a Translation Table entry is as follows:

	Byte Offset
Translation Functions	0000 H
Data for Function 1	0004 H
Data for Function 2	0008 H
Data for Function 3	000C H
Data for Function 4	0010 H
Data for Function 5	0014 H

Figure 2-17 Translation Table Entry

Data for Function 5 **Byte Offset: 0000 H**

The data to be used for the fifth function. The fifth function is the function represented by the highest bit that is set to 1 within the highest two words of the Translation Table entry (byte offsets 0014 H – 0017 H). See **Translation Functions** on page 2-39.

Data for Function 4 **Byte Offset: 0004 H**

The data to be used for the fourth function selected.

Data for Function 3 **Byte Offset: 0008 H**

The data to be used for the third function selected.

Data for Function 2 **Byte Offset: 000C H**

The data to be used for the second function selected.

Data for Function 1 **Byte Offset: 0010 H**

The data in this location will be used for the first function selected. For example, if Bit 0 of byte offset 0014 H is set to 1, this data will be AND with the 24 bits of data of the incoming label. If Bit 0 of byte offset 0014 H is set to 0 and Bit 1 is set to 1, this data will be ORed with the 24 bits of data of the incoming label, and so fourth.

Translation Functions **Byte Offset: 0014 H**

The bits at byte offset 0014 H specify which translation functions to apply. You can use up to five functions for each Translation Table entry. For example, you can AND the value in the incoming label with a specified value, then OR the result with another value.

Bit	Bit Name	Description
09	**SKIP Function**	1 = Do not retransmit the incoming message 0 = Retransmit the incoming message
08	**REPLACE LABEL Function**	1 = Replace the incoming 8-bit label value with the supplied value; the data will be retransmitted as is 0 = Do not use this function
07	**REPLACE ALL Function**	1 = Replace the incoming label and data with the supplied value; all 32 bits will be replaced 0 = Do not use this function
06	**SUBTRACT Function**	1 = Subtract the supplied value from the incoming message data; this will not affect the label but may alter the SDI bits 0 = Do not use this function
05	**ADD Function**	1 = Add the supplied value to the incoming message data; this will not affect the label but may alter the SSM bits 0 = Do not use this function
04	**NOR Function**	1 = NOR the supplied value with the incoming message data; 1 NOR 1 = 0, 1 NOR 0 = 0, 0 NOR 1 = 0, 0 NOR 0 = 1 0 = Do not use this function
03	**XOR Function**	1 = XOR the supplied value with the incoming message data; 1 XOR 1 = 0, 1 XOR 0 = 1, 0 XOR 1 = 1, 0 XOR 0 = 0 0 = Do not use this function
02	**NAND Function**	1 = NAND the supplied value with the incoming message data; 1 NAND 1 = 0, 1 NAND 0 = 1, 0 NAND 1 = 1, 0 NAND 0 = 1 0 = Do not use this function
01	**OR Function**	1 = OR the supplied value with the incoming message data; 1 OR 1 = 1, 1 OR 0 = 1, 0 OR 1 = 1, 0 OR 0 = 0 0 = Do not use this function
00	**AND Function**	1 = AND the supplied value with the incoming message data; 1 AND 1 = 1, 1 AND 0 = 0, 0 AND 1 = 0, 0 AND 0 = 0 0 = Do not use this function

Receive Sequential Mode Status Word

2.6 Channel Control Registers Maps

2.6.1 Channel 0 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FD20-0FD22 H
Channel 0 Scratch Buffer End (W)	0FD24 H
Channel 0 Scratch Buffer Start (W)	0FD26 H
Channel 0 Status Register (R)	0FD28 H
Channel 0 Interrupt / Trigger Conditions (W)	0FD2A H
Reserved	0FD2C H
Channel 0 Transmit Loop Counter (W)	0FD2E H
Channel 0 Transmit Instruction Counter (W)	0FD30 H
Channel 0 Transmit Instruction Stack Pointer (W)	0FD32 H
Channel 0 Receive Label Trigger (W)	0FD34 H
Channel 0 Receive Error Count (R/W)	0FD36 H
Channel 0 Receive Interval Counter Trigger (W)	0FD38 H
Reserved	0FD3A H
Channel 0 Receive Data Word Counter Trigger (W)	0FD3C H
Channel 0 Receive Buffer Wraparound (W)	0FD3E H
Channel 0 Receive/Transmit Data Word Count (R)	0FD40 H
Channel 0 Receive Filter Table Start Address (W)	0FD42 H
Channel 0 Receive Look-up Table Start Address (W)	0FD44 H
Channel 0 Receive Data Current Pointer (R)	0FD46 H
Channel 0 Receive Data End Pointer (W)	0FD48 H
Channel 0 Receive Data Start Pointer (W)	0FD4A H
Reserved	0FD4C H
Channel 0 Configuration (W)	0FD4E H

Figure 2-18 Channel 0 Control Register Block Map

2.6.2 Channel 1 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FD50-0FD52 H
Channel 1 Scratch Buffer End (W)	0FD54 H
Channel 1 Scratch Buffer Start (W)	0FD56 H
Channel 1 Status Register (R)	0FD58 H
Channel 1 Interrupt / Trigger Conditions (W)	0FD5A H
Reserved	0FD5C H
Channel 1 Transmit Loop Counter (W)	0FD5E H
Channel 1 Transmit Instruction Counter (W)	0FD60 H
Channel 1 Transmit Instruction Stack Pointer (W)	0FD62 H
Channel 1 Receive Label Trigger (W)	0FD64 H
Channel 1 Receive Error Count (R/W)	0FD66 H
Channel 1 Receive Interval Counter Trigger (W)	0FD68 H
Reserved	0FD6A H
Channel 1 Receive Data Word Counter Trigger (W)	0FD6C H
Channel 1 Receive Buffer Wraparound (W)	0FD6E H
Channel 1 Receive/Transmit Data Word Count (R)	0FD70 H
Channel 1 Receive Filter Table Start Address (W)	0FD72 H
Channel 1 Receive Look-up Table Start Address (W)	0FD74 H
Channel 1 Receive Data Current Pointer (R)	0FD76 H
Channel 1 Receive Data End Pointer (W)	0FD78 H
Channel 1 Receive Data Start Pointer (W)	0FD7A H
Reserved	0FD7C H
Channel 1 Configuration (W)	0FD7E H

Figure 2-19 Channel 1 Control Register Block Map

2.6.3 Channel 2 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FD80-0FD82 H
Channel 2 Scratch Buffer End (W)	0FD84 H
Channel 2 Scratch Buffer Start (W)	0FD86 H
Channel 2 Status Register (R)	0FD88 H
Channel 2 Interrupt / Trigger Conditions (W)	0FD8A H
Reserved	0FD8C H
Channel 2 Transmit Loop Counter (W)	0FD8E H
Channel 2 Transmit Instruction Counter (W)	0FD90 H
Channel 2 Transmit Instruction Stack Pointer (W)	0FD92 H
Channel 2 Receive Label Trigger (W)	0FD94 H
Channel 2 Receive Error Count (R/W)	0FD96 H
Channel 2 Receive Interval Counter Trigger (W)	0FD98 H
Reserved	0FD9A H
Channel 2 Receive Data Word Counter Trigger (W)	0FD9C H
Channel 2 Receive Buffer Wraparound (W)	0FD9E H
Channel 2 Receive/Transmit Data Word Count (R)	0FDA0 H
Channel 2 Receive Filter Table Start Address (W)	0FDA2 H
Channel 2 Receive Look-up Table Start Address (W)	0FDA4 H
Channel 2 Receive Data Current Pointer (R)	0FDA6 H
Channel 2 Receive Data End Pointer (W)	0FDA8 H
Channel 2 Receive Data Start Pointer (W)	0FDAA H
Reserved	0FDAC H
Channel 2 Configuration (W)	0FDAE H

Figure 2-20 Channel 2 Control Register Block Map

2.6.4 Channel 3 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FDB0-0FDB2 H
Channel 3 Scratch Buffer End (W)	0FDB4 H
Channel 3 Scratch Buffer Start (W)	0FDB6 H
Channel 3 Status Register (R)	0FDB8 H
Channel 3 Interrupt / Trigger Conditions (W)	0FDBA H
Reserved	0FDBC H
Channel 3 Transmit Loop Counter (W)	0FDBE H
Channel 3 Transmit Instruction Counter (W)	0FDC0 H
Channel 3 Transmit Instruction Stack Pointer (W)	0FDC2 H
Channel 3 Receive Label Trigger (W)	0FDC4 H
Channel 3 Receive Error Count (R/W)	0FDC6 H
Channel 3 Receive Interval Counter Trigger (W)	0FDC8 H
Reserved	0FDCA H
Channel 3 Receive Data Word Counter Trigger (W)	0FDCC H
Channel 3 Receive Buffer Wraparound (W)	0FDCE H
Channel 3 Receive/Transmit Data Word Count (R)	0FDD0 H
Channel 3 Receive Filter Table Start Address (W)	0FDD2 H
Channel 3 Receive Look-up Table Start Address (W)	0FDD4 H
Channel 3 Receive Data Current Pointer (R)	0FDD6 H
Channel 3 Receive Data End Pointer (W)	0FDD8 H
Channel 3 Receive Data Start Pointer (W)	0FDDA H
Reserved	0FDDC H
Channel 3 Configuration (W)	0FDDE H

Figure 2-21 Channel 3 Control Register Block Map

2.6.5 Channel 4 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FDE0-0FDE2 H
Channel 4 Scratch Buffer End (W)	0FDE4 H
Channel 4 Scratch Buffer Start (W)	0FDE6 H
Channel 4 Status Register (R)	0FDE8 H
Channel 4 Interrupt / Trigger Conditions (W)	0FDEA H
Reserved	0FDEC H
Channel 4 Transmit Loop Counter (W)	0FDEE H
Channel 4 Transmit Instruction Counter (W)	0FDF0 H
Channel 4 Transmit Instruction Stack Pointer (W)	0FDF2 H
Channel 4 Receive Label Trigger (W)	0FDF4 H
Channel 4 Receive Error Count (R/W)	0FDF6 H
Channel 4 Receive Interval Counter Trigger (W)	0FDF8 H
Reserved	0FDFA H
Channel 4 Receive Data Word Counter Trigger (W)	0FDFC H
Channel 4 Receive Buffer Wraparound (W)	0FDFE H
Channel 4 Receive/Transmit Data Word Count (R)	0FE00 H
Channel 4 Receive Filter Table Start Address (W)	0FE02 H
Channel 4 Receive Look-up Table Start Address (W)	0FE04 H
Channel 4 Receive Data Current Pointer (R)	0FE06 H
Channel 4 Receive Data End Pointer (W)	0FE08 H
Channel 4 Receive Data Start Pointer (W)	0FE0A H
Reserved	0FE0C H
Channel 4 Configuration (W)	0FE0E H

Figure 2-22 Channel 4 Control Register Block Map

2.6.6 Channel 5 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FE10-0FE12 H
Channel 5 Scratch Buffer End (W)	0FE14 H
Channel 5 Scratch Buffer Start (W)	0FE16 H
Channel 5 Status Register (R)	0FE18 H
Channel 5 Interrupt / Trigger Conditions (W)	0FE1A H
Reserved	0FE1C H
Channel 5 Transmit Loop Counter (W)	0FE1E H
Channel 5 Transmit Instruction Counter (W)	0FE20 H
Channel 5 Transmit Instruction Stack Pointer (W)	0FE22 H
Channel 5 Receive Label Trigger (W)	0FE24 H
Channel 5 Receive Error Count (R/W)	0FE26 H
Channel 5 Receive Interval Counter Trigger (W)	0FE28 H
Reserved	0FE2A H
Channel 5 Receive Data Word Counter Trigger (W)	0FE2C H
Channel 5 Receive Buffer Wraparound (W)	0FE2E H
Channel 5 Receive/Transmit Data Word Count (R)	0FE30 H
Channel 5 Receive Filter Table Start Address (W)	0FE32 H
Channel 5 Receive Look-up Table Start Address (W)	0FE34 H
Channel 5 Receive Data Current Pointer (R)	0FE36 H
Channel 5 Receive Data End Pointer (W)	0FE38 H
Channel 5 Receive Data Start Pointer (W)	0FE3A H
Reserved	0FE3C H
Channel 5 Configuration (W)	0FE3E H

Figure 2-23 Channel 5 Control Register Block Map

2.6.7 Channel 6 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FE40-0FE42 H
Channel 6 Scratch Buffer End (W)	0FE44 H
Channel 6 Scratch Buffer Start (W)	0FE46 H
Channel 6 Status Register (R)	0FE48 H
Channel 6 Interrupt / Trigger Conditions (W)	0FE4A H
Reserved	0FE4C H
Channel 6 Transmit Loop Counter (W)	0FE4E H
Channel 6 Transmit Instruction Counter (W)	0FE50 H
Channel 6 Transmit Instruction Stack Pointer (W)	0FE52 H
Channel 6 Receive Label Trigger (W)	0FE54 H
Channel 6 Receive Error Count (R/W)	0FE56 H
Channel 6 Receive Interval Counter Trigger (W)	0FE58 H
Reserved	0FE5A H
Channel 6 Receive Data Word Counter Trigger (W)	0FE5C H
Channel 6 Receive Buffer Wraparound (W)	0FE5E H
Channel 6 Receive/Transmit Data Word Count (R)	0FE60 H
Channel 6 Receive Filter Table Start Address (W)	0FE62 H
Channel 6 Receive Look-up Table Start Address (W)	0FE64 H
Channel 6 Receive Data Current Pointer (R)	0FE66 H
Channel 6 Receive Data End Pointer (W)	0FE68 H
Channel 6 Receive Data Start Pointer (W)	0FE6A H
Reserved	0FE6C H
Channel 6 Configuration (W)	0FE6E H

Figure 2-24 Channel 6 Control Register Block Map

2.6.8 Channel 7 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FE70-0FE72 H
Channel 7 Scratch Buffer End (W)	0FE74 H
Channel 7 Scratch Buffer Start (W)	0FE76 H
Channel 7 Status Register (R)	0FE78 H
Channel 7 Interrupt / Trigger Conditions (W)	0FE7A H
Reserved	0FE7C H
Channel 7 Transmit Loop Counter (W)	0FE7E H
Channel 7 Transmit Instruction Counter (W)	0FE80 H
Channel 7 Transmit Instruction Stack Pointer (W)	0FE82 H
Channel 7 Receive Label Trigger (W)	0FE84 H
Channel 7 Receive Error Count (R/W)	0FE86 H
Channel 7 Receive Interval Counter Trigger (W)	0FE88 H
Reserved	0FE8A H
Channel 7 Receive Data Word Counter Trigger (W)	0FE8C H
Channel 7 Receive Buffer Wraparound (W)	0FE8E H
Channel 7 Receive/Transmit Data Word Count (R)	0FE90 H
Channel 7 Receive Filter Table Start Address (W)	0FE92 H
Channel 7 Receive Look-up Table Start Address (W)	0FE94 H
Channel 7 Receive Data Current Pointer (R)	0FE96 H
Channel 7 Receive Data End Pointer (W)	0FE98 H
Channel 7 Receive Data Start Pointer (W)	0FE9A H
Reserved	0FE9C H
Channel 7 Configuration (W)	0FE9E H

Figure 2-25 Channel 7 Control Register Block Map

2.6.9 Channel 8 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FEA0-0FEA2 H
Channel 8 Scratch Buffer End (W)	0FEA4 H
Channel 8 Scratch Buffer Start (W)	0FEA6 H
Channel 8 Status Register (R)	0FEA8 H
Channel 8 Interrupt / Trigger Conditions (W)	0FEAA H
Reserved	0FEAC H
Channel 8 Transmit Loop Counter (W)	0FEAE H
Channel 8 Transmit Instruction Counter (W)	0FEE0 H
Channel 8 Transmit Instruction Stack Pointer (W)	0FEB2 H
Channel 8 Receive Label Trigger (W)	0FEB4 H
Channel 8 Receive Error Count (R/W)	0FEB6 H
Channel 8 Receive Interval Counter Trigger (W)	0FEB8 H
Reserved	0FEBA H
Channel 8 Receive Data Word Counter Trigger (W)	0FEBC H
Channel 8 Receive Buffer Wraparound (W)	0FEBE H
Channel 8 Receive/Transmit Data Word Count (R)	0FEC0 H
Channel 8 Receive Filter Table Start Address (W)	0FEC2 H
Channel 8 Receive Look-up Table Start Address (W)	0FEC4 H
Channel 8 Receive Data Current Pointer (R)	0FEC6 H
Channel 8 Receive Data End Pointer (W)	0FEC8 H
Channel 8 Receive Data Start Pointer (W)	0FECA H
Reserved	0FECC H
Channel 8 Configuration (W)	0FECE H

Figure 2-26 Channel 8 Control Register Block Map

2.6.10 Channel 9 Control Register Block Memory Map

The registers are marked read only (R) or write only (W) — only the Receive Error Count Register is both read and write.

Reserved	0FED0-0FED2 H
Channel 9 Scratch Buffer End (W)	0FED4 H
Channel 9 Scratch Buffer Start (W)	0FED6 H
Channel 9 Status Register (R)	0FED8 H
Channel 9 Interrupt / Trigger Conditions (W)	0FEDA H
Reserved	0FEDC H
Channel 9 Transmit Loop Counter (W)	0FEDE H
Channel 9 Transmit Instruction Counter (W)	0FEE0 H
Channel 9 Transmit Instruction Stack Pointer (W)	0FEE2 H
Channel 9 Receive Label Trigger (W)	0FEE4 H
Channel 9 Receive Error Count (R/W)	0FEE6 H
Channel 9 Receive Interval Counter Trigger (W)	0FEE8 H
Reserved	0FEEA H
Channel 9 Receive Data Word Counter Trigger (W)	0FEEC H
Channel 9 Receive Buffer Wraparound (W)	0FEEE H
Channel 9 Receive/Transmit Data Word Count (R)	0FEF0 H
Channel 9 Receive Filter Table Start Address (W)	0FEF2 H
Channel 9 Receive Look-up Table Start Address (W)	0FEF4 H
Channel 9 Receive Data Current Pointer (R)	0FEF6 H
Channel 9 Receive Data End Pointer (W)	0FEF8 H
Channel 9 Receive Data Start Pointer (W)	0FEFA H
Reserved	0FEFC H
Channel 9 Configuration (W)	0FEFE H

Figure 2-27 Channel 9 Control Register Block Map

2.7 Channel Control Register Definitions

2.7.1 Channel *x* Scratch Buffer End Register — Write

Data Rate Mode

For transmission in Data Rate Mode, the Channel *x* Scratch Buffer End Register contains the end address of the scratch buffer that must be assigned by the user. See **Channel x Scratch Buffer Start Register** on page 2-50.

2.7.2 Channel *x* Scratch Buffer Start Register — Write

Data Rate Mode

For transmission in Data Rate Mode, the user must allocate a scratch buffer for use by the firmware. Its length must be at least (Transmit Instruction Counter × 10 + 4) bytes. If the buffer is not long enough, the channel will turn itself off without transmitting.

The Channel *x* Scratch Buffer Start Register contains the start address of this buffer. The address must be a word boundary.

2.7.3 Channel *x* Status Register — Read

The Channel *x* Status Register indicates the operational status of the channel. This register can be used to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts, the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. The user must reset status bits, by writing a 0 to this register.

Bit	Bit Name – Interrupt Cause
07-15	Reserved
06	Receive - Stopped on Buffer Full
05	Receive - Error Word Received
04	Receive - Data Word Count Trigger
03	Receive - Interval Count Trigger
02	Receive - Label Received
01	Transmit - End of Frame
00	Transmit - End of Block

Channel *x* Status Register

Look-up Mode

In Look-Up Mode, the Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the label's Control byte.

Sequential Mode

In Sequential Mode, the Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the Filter Table.

2.7.4 Channel *x* Interrupt/Trigger Condition Register — Write

The Channel *x* Interrupt/Trigger Condition Register sets the Interrupt and Trigger condition or conditions of the channel. The Trigger Conditions set a pulse on the External Trigger Output.

Trigger Condition Bits 08 – 15		Interrupt Condition Bits 00 – 07	
Bit	**Bit Name**	**Bit**	**Bit Name**
15	Reserved	**07**	Reserved
14	Receive – Stopped on buffer full	**06**	Receive – Stopped on buffer full
13	Receive – Error Word received	**05**	Receive – Error Word received
12	Receive – Data Word Count Trigger [1]	**04**	Receive – Data Word Count Trigger [1]
11	Receive – Interval Count Trigger [2]	**03**	Receive – Interval Count Trigger [2]
10	Receive – Label Received [3]	**02**	Receive – Label Received [3]
09	Transmit – End of Frame	**01**	Transmit – End of Frame
08	Transmit – End of Block	**00**	Transmit – End of Block

Receive Merge Interval/Trigger Condition Register

1. To activate the Receive – Data Word Count Trigger interrupt or trigger, the Channel x Receive Data Word Counter Trigger register must also be set.
2. To activate the Receive – Interval Count Trigger interrupt or trigger, the Channel x Receive Interval Counter Trigger register must also be set.
3. The Receive – Label Received interrupt or trigger only occurs upon reception of a label, which has been marked for interrupt in a Filter Table (in Sequential Mode) or in a Control Byte (in Look-up Table Mode.

2.7.5 Channel x Transmit Loop Counter — Write

The Channel *x* Transmit Loop counter sets the number of times to execute the transmit instruction blocks (the frame): *N* Times or Continuous Loop. If the continuous value is selected, setting the related channel bit in the Global Start/ Stop Register to a 0 can terminate the channel's operation.

Bit	Value	
00–15	0000	= Continuous
	0001	= One time
	0002	= Two times
		•
		•
		•
	FFFF	= 65535 times

Channel *x* Transmit Loop Counter

Note: When using Data Rate Mode or FIFO Mode, the value of this register is ignored and the data is transmitted continuously. See **Channel x**

Configuration Register on page 2-55. For an explanation of all transmit modes, see **2.3 Transmit Channel Operation** on page 2-19.

2.7.6 Channel *x* Transmit Instruction Counter — Write

The Channel *x* Transmit Instruction Counter sets the number of Transmit Instruction blocks to process. These instruction blocks taken together comprise a frame.

2.7.7 Channel *x* Transmit Instruction Stack Pointer — Write

The Channel *x* Transmit Instruction Stack Pointer sets the starting address of the Transmit Instruction Stack**.** The address must be a word boundary within the Transmit Instruction Stack area. For example, to place the Transmit Instruction stack starting at location 0300 (H), write 0300 (H) to this register.

2.7.8 Channel *x* Receive Label Trigger Register — Write

Sequential Mode

The Channel *x* Receive Label Trigger Register is used in conjunction with the Receive Label Trigger bit in the Channel *x* Configuration Register (see **Channel x Configuration Register** on page 2-55). This register enables the reception and storage of data upon receipt of a unique ARINC label. The module will not store any ARINC words received prior to the first instance of this label.

Bit	Description
08–15	Set to 0
00–07	Trigger Label

Channel *x* Receive Label Trigger Register

2.7.9 Channel x Receive Error Count Register — Read/Write

Sequential Mode

The 16-bit Channel *x* Receive Error Count Register indicates the number of errors received on a particular channel. To reset the register, write 0000 to it.

2.7.10 Channel x Receive Interval Counter Trigger Register — Write

Sequential Mode

The Channel *x* Receive Interval Counter Trigger Register allows the user to generate an interrupt and set a flag upon reception of every *N* number of words, where *N* is the value written to this register. For example, to request an interrupt after every five ARINC words, write 0005 (H) to this register.

To generate an interrupt or a trigger, the appropriate bit must also be set in the Channel *x* Interrupt / Trigger Condition Register (see **Channel x Interrupt/Trigger Condition Register** on page 2-51).

2.7.11 Channel x Receive Data Word Counter Trigger Registers — Write

The Channel *x* Receive Data Word Counter Trigger Register lets the user generate an interrupt and set a flag, which indicates when a specific number of words have been received (1-65535). To generate an interrupt, the appropriate bit must also be set in the Channel *x* Interrupt/Trigger Condition Register (see **Channel x Interrupt/Trigger Condition Register** on page 2-51).

Note: This trigger is set when the value in the Receive Data Word Counter matches the value set in this register.

2.7.12 Channel *x* Receive Buffer Wraparound Register — Write

The Channel *x* Receive Buffer Wraparound Register contains 2 bits for synchronization with the host.

Bit	Description
15	1 = Multiple Wraparound - Data Lost
14	1 = Single Wraparound since last data read
00-13	0

Channel *x* Receive Buffer Wraparound Register

Note: Excalibur software drivers handle these bits. If these drivers, are used, they do not need to be modified.

The user should clear bit 14 each time the first word of the buffer is read. When the buffer wraps around bit 14 is checked. If bit 14 is '0', the module sets the bit to indicate a Single Wraparound ('1'). If bit 14 is '1', the module sets bit 15 to indicate a Multiple Wraparound ('1') has occurred.

2.7.13 Channel *x* Receive/Transmit Data Word Count Register — Read

Sequential Mode

The Channel *x* Receive/Transmit Data Word Count Register indicates the number of ARINC words received (0-65535). This register wraps around to 0 after it reaches 65535. The user may reset the register to 0, only when the channel is stopped.

2.7.14 Channel *x* Receive Filter Table Start Address — Write

Sequential Mode

The Channel *x* Receive Filter Table Start Address sets the Start Address of the 256 × 16 Label Filter Table as described in section **2.4.1 Sequential and Merge Modes** on page 2-28. The address must be a word boundary. It is valid for several channels to use the same Filter Table.

This table is valid only if the Channel *x* Configuration Register Enable Receive Filter Table bit is set. (See bit 09 in the **Channel x Configuration Register** on page 2-55.)

2.7.15 Channel *x* Receive Look-up Table Start Address — Write

Look-up Table Mode

The Channel *x* Receive Look-Up Table Start Address sets the start address of the 256 × 16 Receive Look-Up Table (see bit 05 in the **Channel x Configuration Register** on page 2-55). The address must be a word boundary.

This address points to the *first* location of the Look-Up Table. The module stores one ARINC data block for each label received. The data block contains: 32-bit ARINC word, 32-bit Time Tag, and the 16-bit Receive Status Word. The subsequent reception and storage of another ARINC word will overwrite the Data Block with the same ARINC label.

2.7.16 Channel *x* Receive Data Current Pointer — Read

Sequential Mode

In Sequential Mode the Channel *x* Receive Data Current Pointer indicates the address where the next ARINC receive word is to be placed in the buffer. This pointer value is incremented after the entire receive block (ARINC word, Time Tag, and Status word) is written into memory.

Look-up Table Mode

In Look-Up Table Mode this register contains the address of the last ARINC receive word written to the receive area.

2.7.17 Channel *x* Receive Data End Pointer — Write

Sequential Mode

The Channel *x* Receive Data End Pointer sets the end address of the Receive Data buffer. The address must be a word boundary. The data will wrap around or stop when the buffer is full, (when the End Address is reached), depending upon the contents of the Receive Wrap Around control bit in the Channel *x* Configuration Register.

2.7.18 Channel *x* Receive Data Start Pointer — Write

Sequential Mode

The Channel *x* Receive Data Start Pointer Register sets the start address of the Receive Data buffer. The address must be a word boundary within the Receive Data Blocks area.

Example: To cause the Channel *x* Receive Data Buffer to begin at address 001A0 (H), write 01A0 (H) to this register.

2.7.19 Channel *x* Configuration Register — Write

The Channel *x* Configuration Register sets up various channel parameters. Bits that are not used (for example, receive-related bits while operating as a transmitter) are ignored by the module.

Bit	Bit Name	Description
13-15	Reserved	Set to 0
12	Transmit Mode Select 0	This bit works in conjunction with Bit 08. See the table in Bit 08. 1 = FIFO Mode selected as the transmit mode. (See **2.3.2 FIFO Mode** on page 2-24.) 0 = Interblock Time Mode selected as the transmit mode. (See **2.3.1 Interblock Time Mode and Data Rate Mode** on page 2-19.) **Note:** When using Data Rate Mode or FIFO Mode, the value of the Channel *x* Transmit Loop Counter register is ignored and the data is transmitted continuously. See **Channel x Transmit Loop Counter on page 2-51**.
11	Translation Mode	1 = Translation Mode selected. Translation Mode works in pairs of channels. Labels received by the first channel are retransmitted over the next channel after a translation function is performed. See **2.5 Translation (Dual Channel) Operation** on page 2-37. 0 = Translation Mode not selected.
10	Extended Time Mode	1 = Extended Time Mode selected 0 = Standard Time Mode selected When Extended Time Mode is selected, the Interblock Time/Data Rate is doubled on the bus. See **Interblock Time/Data Rate Word** on page 2-22. This bit is only relevant if Extended Time Mode is supported by the firmware. See **Board Status Register** on page 2-12.
09	Enable Receive Filter Table	1 = Enable Filter Table (Stores labels per table) 0 = Disables table. Stores all labels.
08	Transmit Mode Select 1	This bit works in conjunction with Bit 12. See the table below. 1 = Data Rate Mode (per data block) – Data blocks sent on a scheduled data rate basis. For example: Data Block 1 every 50 msec. Data Block 2 every 25 msec. In this mode a scratch buffer must be allocated via the Channel *x* Scratch Buffer Start/End registers. For more information, see **2.3.1 Interblock Time Mode and Data Rate Mode** on page 2-19. 0 = Interblock Time Mode or FIFO Mode (depending on the value of Bit 12) **Note:** When using Data Rate Mode or FIFO Mode, the value of the Channel *x* Transmit Loop Counter register is ignored and the data is transmitted continuously. See **Channel x Transmit Loop Counter** on page 2-51.

Bit 08	Bit 12	Transmit Mode
0	0	Interblock Time Mode selected
0	1	FIFO Mode selected
1	0	Data Rate Mode selected
1	1	

07	Receive Label Trigger	1 = Start data storage upon receipt of label xx. See **Channel x Receive Label Trigger Register** on page 2-52. 0 = Receive stores data without Start Label Trigger

Channel *x* Configuration Register

Bit	Bit Name	Description
06	**Receive Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receive wraps around the data within the block. (This bit is used in Sequential Storage Mode only.)
05	**Receive Storage Mode**	1 = Sequential Storage Mode 0 = Look-up Table Mode (see **Channel x Receive Look-up Table Start Address** on page 2-54). This bit is ignored if Bit 01 of the Receive Data Storage Mode Register is set to 1 (Merge Mode).
04	**Parity: Even/Odd**	1 = Even 0 = Odd - Standard ARINC Mode
03	**Parity: On/Off**	1 = Off 0 = On
02	**Transmit Rise/ Fall Time**	1 = Lo Speed (10 +/- 5μsec.) 0 = Hi Speed (1.5 +/- 0.5μsec.)
00-01	**Bit Rate**	If the Programmable Bit Rate is selected then the bit rate is defined by the global **Programmable Bit Rate Register** (see page 2-10).

Bit 01	Bit 00	Channel Bit rate
0	0	12.5 KHz – Lo Speed
0	1	100 KHz – Hi Speed
1	0	Programmable
1	1	Undefined

Channel *x* Configuration Register (Continued)

The Channel *x* Configuration Register can only be written to when *all* the channels are turned off (via the Start/Stop Register).

The module should be started (via the Start/Stop Register) only after a minimum of 1msec. from the time that the contents of the register have been modified.

All active Channel *x* Configuration Registers should be set up immediately following the Board ID validation, before programming other parameters.

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specification of the *M4K429RTx* module.

3.1 Module Layout 3-2

3.2 LED Indicators 3-2

3.3 Connectors. 3-3

3.3.1 EXC-4000 Carrier Board 96-pin Connector 3-3

3.3.2 *M4K429RTx* Module Adapter Cable 3-5

3.4 Power Supply Requirements 3-6

3.1 Module Layout

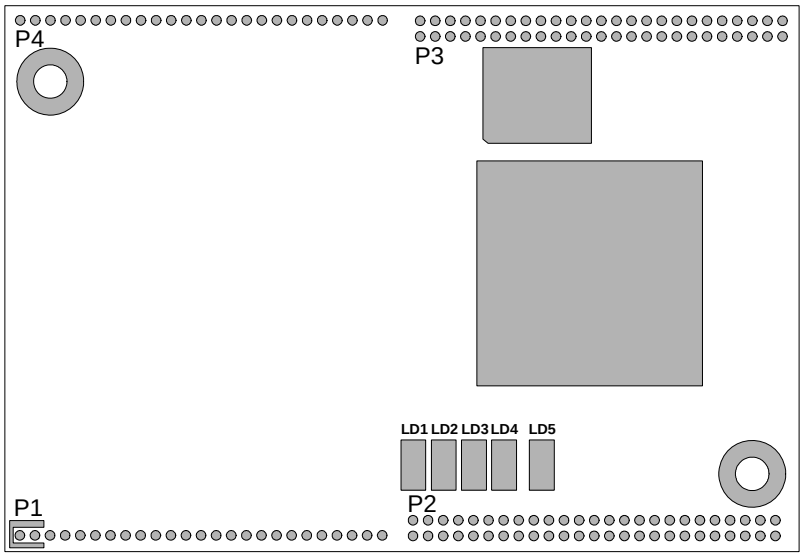


Figure 3-1 *M4K429RTx* Module Layout

3.2 LED Indicators

The *M4K429RTx* contains four LEDS:

LED	Indications
LD1	Receive activity on channels 0–4
LD2	Transmit activity on channels 0–4
LD3	Receive activity on channels 5–9
LD4	Transmit activity on channels 5–9
LD5	Module ready

LED Indicators

3.3 Connectors

The *M4K429RTx* contains four 25-pin, 0.05" spacing strips (P1 – P4), which comprise a total of 100 pins for all module connections. These pins mate with the carrier board socket strips. Out of these 100 pins, 24 pins are assigned for the communication I/O signals.

On most carrier boards, all the module's 24 I/O signals are wired to a 96-pin female connector (Molex® LFH75 51-26-000). This connector is divided into four rows of 24 pins each. Each row is for one module location on the carrier board. The mating connector (Molex® LFH75 51-26-0012) contains four Terminal Sticks; one for each module. See Figure 3-2 and Figure 3-3.

For the *EXC-4000P104plus* carrier board connectors, refer to the *EXC-4000P104plus Carrier Board User's Manual*.

For the *EXC-2000PCIe* carrier board connectors, refer to the *EXC-2000PCI & EXC-2000PCIe User's Manual*.

3.3.1 EXC-4000 Carrier Board 96-pin Connector

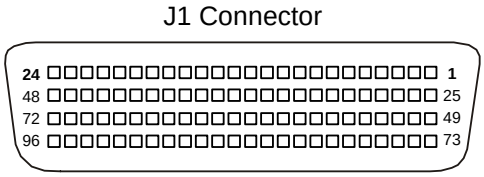


Figure 3-2 EXC-4000 Carrier Board 96-pin Female I/O Connector – Front View

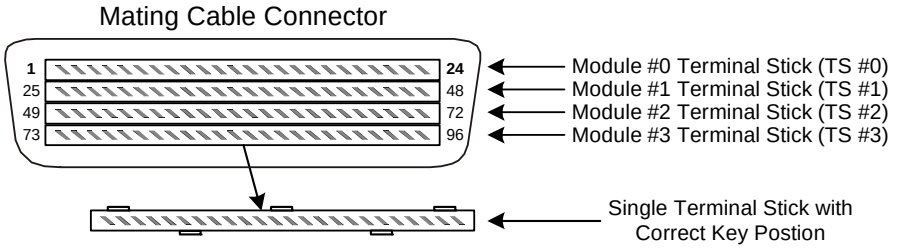


Figure 3-3 EXC-4000 Carrier Board 96-pin Male I/O Mating Cable Connector – Front View

3.3.1.1 Module Terminal Stick Pin Assignments and Description

Pin #	Signal Name	Description
1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	CH0L	Channel 0 ARINC low line connection
3	CH0H	Channel 0 ARINC high line connection
4	CH1L	Channel 1 ARINC low line connection
5	CH1H	Channel 1 ARINC high line connection
6	CH2L	Channel 2 ARINC low line connection
7	CH2H	Channel 2 ARINC high line connection
8	CH3L	Channel 3 ARINC low line connection
9	CH3H	Channel 3 ARINC high line connection
10	CH4L	Channel 4 ARINC low line connection
11	CH4H	Channel 4 ARINC high line connection
12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	CH5L	Channel 5 ARINC low line connection
14	CH5H	Channel 5 ARINC high line connection
15	CH6L	Channel 6 ARINC low line connection
16	CH6H	Channel 6 ARINC high line connection
17	CH7L	Channel 7 ARINC low line connection
18	CH7H	Channel 7 ARINC high line connection
19	CH8L	Channel 8 ARINC low line connection
20	CH8H	Channel 8 ARINC high line connection
21	CH9L	Channel 9 ARINC low line connection
22	CH9H	Channel 9 ARINC high line connection
23	OUTRIGn	This low active output provides trigger pulses of approximately 400 nsec. width and is activated under software control upon the same conditions as interrupts. See Interrupt/ Trigger Conditions Registers. This output is an open-collector with 330-ohm pull-up resistor
24	GND	Provides ground reference for the OUTRIGn output.

Table 3-1 Module Terminal Stick: Pin Assignments and Description

3.3.2 *M4K429RTx* Module Adapter Cable

Excalibur's standard *M4K429RTx* adapter cable converts the Molex® terminal stick to a standard 26-pin high density D-type female connector with jack screws. The cable is 0.5 meter in length and a mating connector with hoods is provided. The 26-pin connector pinout is the same as the module's terminal stick pins 1 to 24, while pins 25, 26 are not connected. See Figure 3-4.

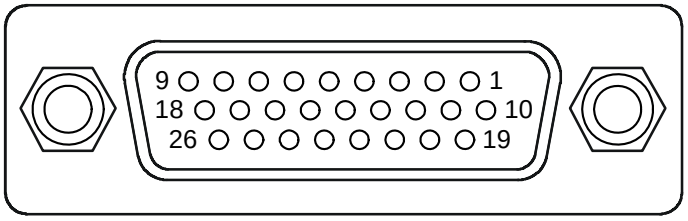


Figure 3-4 Adapter Cable 26-pin Connector – Front View

3.3.2.1 *M4K429RTx* Adapter Cable Connections

24 Pin Terminal Stick Pin no.	Signal Name	High density D-type Female 26-pin connector pin no.
1	SHIELD	1
2	CH0L	2
3	CH0H	3
4	CH1L	4
5	CH1H	5
6	CH2L	6
7	CH2H	7
8	CH3L	8
9	CH3H	9
10	CH4L	10
11	CH4H	11
12	SHIELD	12
13	CH5L	13
14	CH5H	14
15	CH6L	15
16	CH6H	16
17	CH7L	17
18	CH7H	18
19	CH8L	19
20	CH8H	20
21	CH9L	21
22	CH9H	22
23	OUTRIGn	23
24	GND	24
N/C		25,26

Table 3-2 *M4K429RTx* Adapter Cable Connections

3.4 Power Supply Requirements

The modules' maximum power supply requirements are:

M4KRT5	*M4KRT10*	**Conditions**
+5V @ 550mA	+5V @ 550mA	All channels set to receive (default on power-up)
+5V @ 50mA	+5V @ 50mA	Add this amount for each channel set to transmit at high speed, maximum load and 100% duty cycle
+5V @ 800mA	+5V @ 1050mA	Total amount for all channels set to transmit at high speed, maximum load and 100% duty cycle

4 Ordering Information

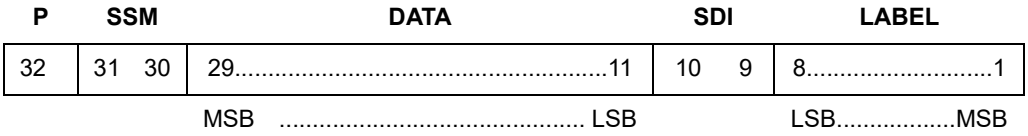
Chapter 4 explains which options to indicate when ordering a *M4K429RTx* module:

Basic Part #	Option	Description
M4K429RT*x*		ARINC 429 Interface module for the *Excalibur 4000* family of carrier boards. Supports up to 10 channels, each programmable as receive or transmit. **Note:** Replace the "***x***" in the part number with 5 or 10 to indicate the desired number of ARINC 429 channels.
	-E	Add this suffix for ruggedized, extended temperature option (-40°C – +85°C)
	-001	Add this suffix for conformal coating
Optional adapter cable:		
X4KBx		M4K429RTx adapter cable, 0.5 meter length with high density D-type 26-pin female connector. See **M4K429RTx Module Adapter Cable,** page 3-5.

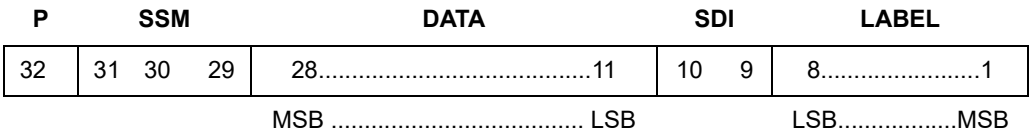
Appendix A ARINC 429 Basic Word Formats

All data sent over the ARINC bus is composed of 32-bit words. A number of different formats can be used, as the following diagrams show:

Format 1



Format 2



Format 3

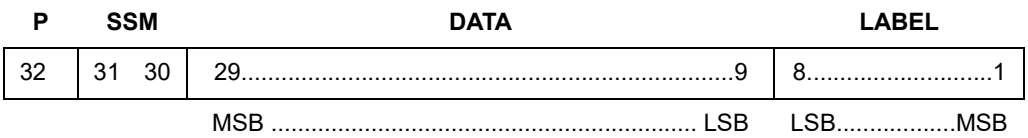


Figure A-1 ARINC 429 Basic Word Formats

Key:

Field	Description
LABEL	Information identifier
SDI	Source/Destination Identifier bits
DATA	Information data: may be presented in one of the following formats
	BNR (Binary)
	BCD (Binary Coded Decimal)
	Discrete
	Maintenance and Acknowledgment
	Alpha Numeric (ISO Alphabet no.5)
SSM	Sign/Status Matrix bits
P	Parity bit (Odd parity)
LSB	Least Significant bit
MSB	Most Significant bit

Bits are transmitted starting with bit 1, the final bit transmitted is the parity bit, bit 32. The label is transmitted with the most significant bit first while the data is transmitted least significant bit first.

The **LABEL** is an octal value from 1 to 377 representing a particular type of data. Most labels are defined in the specification though some are reserved for future needs. Many labels are multiply defined in the specification based on the type of equipment being used.

The **SDI** field is used when a transmitter is connected to multiple receivers but not all data is meant to be used by all the receivers. In this case each receiver will be assigned an SDI value and will look only at labels that match its SDI value. While the specification calls for SDI 00 to be universally accepted, a good deal of equipment appears to disregard this requirement.

The **DATA** field contains the actual data to be sent. A number of data formats are defined in the specification. Binary Coded Decimal (BCD) format uses each four bits to contain a single decimal digit. BNR data is a binary coding. For both data types the specification calls out the units, the resolution, the range, the number of bits used and how frequently the label should be sent. A discrete type has multiple single bit fields defined within a single label. A number of other formats are described in the specification.

SSM, which is sometime 3 bits long, is used for information which helps interpret the numeric value in the data field. Examples of SSM values might be Plus, North, East, Right, To or Above.

P is the parity bit. ARINC 429 calls for odd parity. The parity bit is the last bit sent over the bus.

Appendix B ARINC 429 Connection Precautions

Appendix B describes connection precautions for ARINC 429 cards and modules:

1. Verify the ARINC-429 line is not overloaded beyond the spec:

   Rload > 400 ohm

   Cload < 30,000 pF
2. Use shielded twisted pair wires with typical impedance of 60 to 80 Ohms.
3. Ensure that there is common ground between the connected systems in order to avoid potential differences.
4. Connect/Disconnect cables while the card is powered OFF or *not* transmitting at least.
5. Special care needs to be taken while applying probes of measuring instruments to avoid shorting out signals.

Index

Numerics

32-Bit ARINC Word Order Bit 2-29
32-Bit Receive Data Word Format 2-29
32-Bit Transmit Data Words Format 2-21
32-Bit Word Transmit Order Bit 2-22

A

Adapter Cable 3-5
ARINC 429 Word Formats A-1

B

Block Diagram, Module 1-2
Board ID Register 2-13
Board Status Register 2-12

C

Cable 3-5
Channel Control Register
- Definitions 2-48
- Maps 2-38

Channel Enable Register 2-15
Channel Type Select Register 2-16
Channel x Configuration Register 2-53
Channel x Configuration Status Register 2-10
Channel x Interrupt/Trigger Condition Register 2-49
Channel x Receive Buffer Wraparound Register 2-51
Channel x Receive Data Current Pointer 2-52
Channel x Receive Data End Pointer 2-52
Channel x Receive Data Start Pointer 2-52
Channel x Receive Data Word Counter Trigger Registers 2-51
Channel x Receive Error Count Register 2-50
Channel x Receive Filter Table Start Address 2-51
Channel x Receive Interval Counter Trigger Register 2-50
Channel x Receive Label Trigger Register 2-50
Channel x Receive Look-up Table Start Address 2-52
Channel x Receive/Transmit Data Word Count Register 2-51
Channel x Scratch Buffer End Register 2-48
Channel x Scratch Buffer Start Register 2-48
Channel x Status Register 2-48
Channel x Transmit Instruction Counter 2-50
Channel x Transmit Instruction Stack Pointer 2-50
Channel x Transmit Loop Counter 2-49
Connection Precautions B-1
Connectors 3-3, 3-5
Control Byte 2-34
Control Word Definition 2-19
Counter
- Channel x Transmit Instruction Counter 2-50
- Channel x Transmit Loop Counter 2-49
- Interword Delay/Data Word Counter Word 2-20
- Receive Merge Word Counter 2-8
- Time Tag Counter 2-14

D

Data Block
- Receive Data Block Description 2-34

Data Rate Mode 2-17, 2-53
Data Word 2-20, 2-34
- 32-Bit Transmit Data Words Format 2-21
- Channel x Receive Data Word Counter Trigger Registers 2-51
- Channel x Receive/Transmit Data Word Count Register 2-51
- Interword Delay/Data Word Counter Word 2-20
- Receive Data Word Format 2-29

E

Error Count 2-34
Error Detection 1-2
Error Injection 1-1, 1-2, 1-4, 2-17, 2-18
Extended Time Mode 2-53

F

Features 1-2
FIFO Mode 2-22, 2-53
Filter Table 2-53
Firmware Revision Register 2-11

G

Getting Started 1-3

H

Hardware Revision Register 2-14

I

Installation 1-3, B-1
Instruction Block 2-18
Interblock Time Mode 2-17, 2-53
Interblock Time/Data Rate Word 2-20
Interrupt Status Busy Register 2-4
Interrupt Status Register 2-11
Interword Delay/Data Word Counter Word 2-20
Introduction 1-1
IRIG B 2-9, 2-28, 2-30, 2-33, 2-34, R-1

L

LEDs 3-2

Look-up Table Mode 2-26
- Operation 2-33
- Receive Look-up Table Structure 2-33

Look-up Table Received Status/Control Word 2-34

M

Memory Map
- Channel 0 Control Register Block 2-38
- Channel 1 Control Register Block 2-39
- Channel 2 Control Register Block 2-40
- Channel 3 Control Register Block 2-41
- Channel 4 Control Register Block 2-42
- Channel 5 Control Register Block 2-43
- Channel 6 Control Register Block 2-44
- Channel 7 Control Register Block 2-45
- Channel 8 Control Register Block 2-46
- Channel 9 Control Register Block 2-47
- Channel Control Registers Maps 2-38
- General 1-5

Merge Mode 2-26

Module
- Block Diagram 1-2
- Layout 3-2
- Pinouts 3-4
- Power Supply Requirements 3-6

Module Operation 2-1

Module Options Register 2-4

O

Operation 2-1

Ordering Information 4-1

Overview 1-1

P

Pinouts 3-4, 3-5

Pointer
- Channel x Receive Data Current Pointer 2-52
- Channel x Receive Data End Pointer 2-52
- Channel x Receive Data Start Pointer 2-52
- Channel x Transmit Instruction Stack Pointer 2-50
- Receive Data End Pointer 2-28
- Receive Data Start Pointer 2-28
- Receive Merge Current Pointer 2-8
- Receive Merge End Pointer 2-8
- Receive Merge Start Pointer 2-8
- Transmit Data Pointer 2-20

Power Supply Requirements 3-6

Programmable Bit Rate Register 2-10

R

Receive Buffer Storage Sequence 2-27

Receive Channel 1-2

Receive Channel Operation 2-26

Receive Data Block Description 2-34

Receive Data End Pointer 2-28

Receive Data Start Pointer 2-28

Receive Data Storage Mode Register 2-9

Receive Data Word Format 2-29

Receive Look-up Table Structure 2-33

Receive Merge Buffer Wraparound Register 2-7

Receive Merge Configuration Register 2-6

Receive Merge Current Pointer 2-8

Receive Merge End Pointer 2-8

Receive Merge Error Count Register 2-7

Receive Merge Filter Table Start Address 2-8

Receive Merge interrupt/Trigger Condition Register 2-6

Receive Merge Interval Count Trigger Register 2-7

Receive Merge Label Trigger Register 2-7

Receive Merge Start Pointer 2-8

Receive Merge Status Register 2-5

Receive Merge Word Count Trigger Register 2-8

Receive Merge Word Counter 2-8

Receive Mode 2-54

Receive Modes 1-2

Receive Sequential Mode Buffer Structure 2-28

Receive Sequential Mode Filter Table Diagram 2-32

Receive Sequential Mode Status Word 2-31

Receive Status/ Control Word 2-34

Register
- Board ID Register 2-13
- Board Status Register 2-12
- Channel Enable Register 2-15
- Channel Type Select Register 2-16
- Channel x Configuration Register 2-53
- Channel x Configuration Status Register 2-10
- Channel x Interrupt/Trigger Condition Register 2-49
- Channel x Receive Buffer Wraparound Register 2-51
- Channel x Receive Data Word Counter Trigger Registers 2-51
- Channel x Receive Error Count Register 2-50
- Channel x Receive Interval Counter Trigger Register 2-50
- Channel x Receive Label Trigger Register 2-50
- Channel x Receive/Transmit Data Word Count Register 2-51
- Channel x Scratch Buffer End Register 2-48
- Channel x Scratch Buffer Start Register 2-48
- Channel x Status Register 2-48
- Firmware Revision Register 2-11
- Hardware Revision Register 2-14
- Interrupt Status Busy Register 2-4
- Interrupt Status Register 2-11
- Module Options Register 2-4
- Programmable Bit Rate Register 2-10
- Receive Data Storage Mode Register 2-9
- Receive Merge Buffer Wraparound Register 2-7

Receive Merge Configuration Register 2-6
Receive Merge Error Count Register 2-7
Receive Merge interrupt/Trigger Condition Register 2-6
Receive Merge Interval Count Trigger Register 2-7
Receive Merge Label Trigger Register 2-7
Receive Merge Status Register 2-5
Receive Merge Word Count Trigger Register 2-8
Software Reset Register 2-14
Start/Stop Register 2-13
Time Tag Reset Register 2-13

S

Sequential Mode 2-26, 2-54
Receive Sequential Mode Buffer Structure 2-28
Receive Sequential Mode Filter Table Diagram 2-32
Receive Sequential Mode Status Word 2-31
Software Reset Register 2-14
Specifications, Mechanical and Electrical 3-1
Start/Stop Register 2-13
Status Byte 2-34

T

Technical Specifications 3-1
Time Tag 2-34
IRIG B 2-9, 2-28, 2-30, 2-33, 2-34, R-1
Time Tag Counter 2-14
Time Tag Reset Register 2-13
Word Format 2-29
Translation Mode 2-35, 2-53
Transmit Channel 1-2
Transmit Data Block Format 2-21
Transmit Data Pointer 2-20
Transmit Instruction Block 2-18
Transmit Mode Select 2-53
Transmit Modes 2-17
Trigger
Channel x Receive Data Word Counter Trigger Registers 2-51
Output Trigger 3-4
Receive Merge Interrupt/Trigger Condition Register 2-6
Receive Merge Interval Count Trigger Register 2-7
Receive Merge Word Count Trigger Register 2-8

Release Notes

M4K429RTx Module Rev D

1. The *M4K429RTx* Rev D module implements 5V only front end and does not require the +/-12V supplies anymore.
2. The *M4K429RTx* Rev D module has an additional IRIG B input for the new optional IRIG B Time Tag mode. (To utilize this feature, a carrier board that has IRIG B wired to the module is required.)
3. The *M4K429RTx* Rev D implements an additional LED LD5.
4. Connectors P2 and P3 have been extended to the dual row type for future 32-bit operation.

The information contained in this document is believed to be accurate. However, no responsibility is assumed by Excalibur Systems, Inc. for its use and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

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