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EXC-3000PC
EXC-3000PCH
MAGICard

Test and Simulation Board for PC Compatible Computers

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

Chapter 1 provides an overview of the EXC-3000PC MAGICard avionics communication boards. The following topics are covered:

1.1 Overview page 1-1
EXC-3000PC MAGICard board features page 1-2
1.2 Installation page 1-3
Installing the Board page 1-3
Adding *MAGICard Drivers* page 1-4
1.3 Getting Started page 1-4
1.4 General Memory Map page 1-6
1.5 Timing Considerations page 1-7

1.1 Overview

The EXC-3000PC MAGICard is a multi-protocol test and simulation board for PC compatible computers. The board supports up to 10 ARINC 429/561/568/575/582 and RS-232/422/423/485 channels in any combination of transmitters and receivers on board with the addition of two protocol channels on plug-in adapter boards. Additional protocol channels, such as MIL-STD-1553, may be added using plug-in piggyback adapter boards. In addition, unique, customer interfaces can usually be implemented either on-board or in the form of a plug-in adapter.

The transmitters for all standard protocols operate via a transmitter 'instruction' stack that allows the user to schedule data transmission and reduce the need for host computer (PC) intervention. The receivers allow for filtering and multi-storage modes of Data Words.

NOTE The EXC-3000PCH MAGICard half-size PC board supports up to 4 channels. The EXC-3000PCH half-size board is 100% software compatible with the EXC-3000PC MAGICard full-size board.

This manual supports both the full-size and half-size boards. Users of the half-size board should ignore all references to channels 4-9.

See Ordering Information, page 5-1 for the exact part numbers.

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1.1.1 EXC-3000PC MAGICard Features

Multi-Protocol Advanced Gateway Interface Card for PC Systems

General

- Communication Channels
  10 for EXC-3000PC
  4 for EXC-3000PCH
- Channel Types Include
  ARINC-429/419 (561/568/575/582)
  ARINC- 575 24-bit
  RS-232/422/423/485
- Memory Mapped, 32K x 8 dual-port RAM
- Programmable (per channel)
  Buffer size
  Transmit Inter-block time (per block)
- Receive Features
  Word Status Tagging
  Word Time Tagging (32-bit)
  Label/Data Filtering
  Start Triggers
  Receive Error Count per channel
  Receive Count Interval Trigger
- Transmit Features
  3 Modes (one-shot, loop, *N* times)
- Programmable Hardware Trigger
- Interrupt and Polling Modes of Operation

ARINC Channels

- Programmable Features
  Transmit Sync Time (between words)
  Transmit Variable Amplitude
  Bit Rates (Hi, Lo, Variable)
  Parity (Odd, Even, On, Off)
- Error Injection per Block
  Bit Count Hi/Lo
  Sync Time
  Stretch Bit
  Bit Rate (frequency)
  Parity
- Error Injection per Word
  Bit Count
  Sync Time
  Parity
  Bit Coding Error
- Receive/Monitor Modes
  Look-up Table
  Sequential per channel
  Sequential Merge Mode
  (stores data from all Receive channels in one buffer)

RS Channels

Per channel baud to 256K
From 5 to 8 Data Bits
Even/Odd/No/Stick Parity
Selectable CTS/DTR (RS-232)
Selectable Loopback (RS-485)

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Figure 1-1 illustrates the EXC-3000PC MAGICard

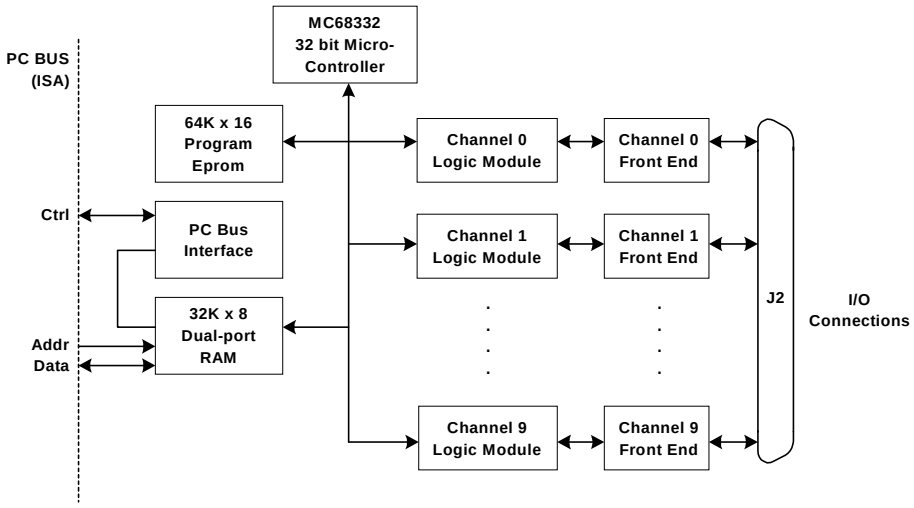


Figure 1-1 EXC-3000PC MAGICard Block Diagram

1.2 Installation

To operate the EXC-3000PC MAGICard board:

1. Install the board in the computer
2. Add MAGICard Drivers to the hard disk

1.2.1 Installing the Board

WARNING *Wear a suitably grounded electrostatic discharge wrist strap whenever handling the MAGICard board.*

1. Before installing the board, it is very important to determine which area of the memory is available. This board requires a 32K (8000 H) area of memory.

2. If interrupts are to be used, find an unused interrupt line. If a segment and /or an interrupt line is already in use and is also used for the MAGICard, the board will exhibit unpredictable behavior. It may work in some modes but not in others; it may seem to work yet exhibit intermittent errors; or it may not function at all.

3. After determining the board base address, set the DIP switch SW2 - see DIP Switches, page 4-3.

4. Check that the power source of the computer is disconnected. Insert the board into an available slot.

5. Turn on the computer. On the Windows taskbar click **Start > Settings > Control Panel > Add New Hardware**. The **Add New Hardware Wizard** is displayed. Click, **Next**.

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6. The Wizard asks **Do you want Windows to search for your new hardware?** Click, **No > Next.**

7. From **Hardware Types**, select **Other Devices > Next**. Click, **Have disk..**

8. Insert the Hardware installation diskette that came with the EXC-3000PC MAGICard board into drive A. When the **Install from Disk** dialog box is displayed, type **a** in **Copy files from.** Click, **OK.**

9. On the Wizard screen, click **Excalibur Card > Next > Finish**.

10. When prompted to **Insert Disk**, click **OK**, as the diskette is already in drive A.

For more information about installing the board, see Chapter 5, Mechanical and Electrical Specifications.

1.2.2 Adding MAGICard Drivers to a Computer

The standard software included with the EXC-3000PC MAGICard board is for Windows 95. Software for other operating systems can be downloaded from our site: www.mil-1553.com.

For information about adding MAGICard drivers, see the **`ReadMe.txt`** file on the software diskette that came with the board.

1.3 Getting Started

The MAGICard operation makes extensive use of pointers for setting up the size and location on both the receiver and data blocks, transmitter instruction stacks and receiver Look-up Tables. Each channel has its own pointer registers so that the unique memory areas may be allocated for each channel. It is also possible to share memory areas. For example, more than one receiver channel may point to and use the same Label Look-up Table that controls which labels will be stored by the board.

The flowchart on page 1-5, Figure 1-2 describes the necessary steps to set up the transmit and receive channels. For details how to operate each specific protocol, see the appropriate chapters:

	Channel Operation	
	Transmit	**Receive**
ARINC 429/561/568/575/582	page 2-35	page 2-43
RS-232/422/423/485	page 3-29	page 3-32

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After power-up, perform the following steps:

1. Power-Up Handshake

User indicates HOST READY by writing to the HOST READY Register.

Board clears the memory and executes initialization procedure.

User waits for BOARD READY Register to be valid.

User designates channels as transmit or receive channel.

2. Setup/Verify the Global Registers

User can check the result of the power – up Self-test by reading the Board Status Register.

User can verify the configuration of each channel (Transmit or Receive) by reading the Configuration Status Registers.

Update the ARINC Programmable Bit Rate Register (if used).

Update the Interrupt Request Level Register (if interrupts are used).

3. Setup the Transmit Related Channel Control Registers

Program the channel Configuration Registers (parity, bit rate, etc.).

Update the Transit Instruction Stack Pointer for each channel.

Update the Transmit Instruction Counter.

Update the Transmit Amplitude Register for each channel.

For RS channels, set the Channel Start Transmit Register to 1.

4. Setup the Transmit Instruction Blocks

Update the Instruction Blocks with information relating to each ARINC or RS Transmit data block (i.e. error injection, pointer to the Transmit data blocks, delay between data blocks).

2. Write the Transmit Data Blocks

Write the ARINC words (or bytes for RS channels) into the on-board memory at locations pointed to by the instruction stacks Transmit Data Pointers.

6. Setup the Receive Related Channel Control Registers

Program the channel Configuration Registers (parity, bit rate, etc.).

Update the Receive Start and End Pointers.

Update the Look-up Table Start Address Register (If using this mode).

Update the Label Trigger Register (if using a label to start storage).

Update the Counter Trigger Registers (optional).

For RS channels, set the Channel Start Receive Register to 1.

7. Start

Write to the Global Start Register, setting the appropriate channel (s) 'start' bits. Each channel can be 'started' individually, at different times.

See Global Registers and definitions, (ARINC) page 2-2 and (RS) page 3-3.

8. Read the Receive Status Registers (i.e. Word Count, Error Count)

Read the Receive Status Registers to know how many words have been received and how many invalid words, if any, were detected.

9. Read the Receive Data Block

Read the ARINC words or RS bytes (and Receive Status and Time Tag Words) from the on-board memory.

Figure 1-2 Board Operation Flowchart

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1.4 General Memory Map

The EXC-3000PC MAGICard occupies 32K x 8 of the PC's memory. The board is memory-mapped to any half-segment boundary (e.g. D000, D800 etc.) of the PC's memory space via DIP switch SW2.

For more details about DIP switch settings see DIP Switches, page 4-3.

Transmit Instruction Stacks Transmit Data blocks Receive Data Blocks Receive Look-Up Tables	0000-79FF H
Reserved	7A00-7D1F H
Channel Control Register Block 0	7D20-7D4E H
Channel Control Register Block 1	7D50-7D7E H
Channel Control Register Block 2	7D80-7DAE H
Channel Control Register Block 3	7DB0-7DDE H
Channel Control Register Block 4	7DE0-7E0E H
Channel Control Register Block 5	7E10-7E3E H
Channel Control Register Block 6	7E40-7E6E H
Channel Control Register Block 7	7E70-7E9E H
Channel Control Register Block 8	7EA0-7ECE H
Channel Control Register Block 9	7ED0-7EFE H
Global Control Registers	7F00-7FFF H

Figure 1-4 General Memory Map

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1.5 Timing Considerations

The EXC-3000PC MAGICard has a processing overhead time of approximately 50 microseconds per channel during actual reception or transmission. This permits:

- 10 channels to run at Hi-Speed with an inter-word delay of 18 bit times;
- Gives an effective throughput of 1 Word per channel every 500 microseconds.

If fewer channels are used, a smaller interword delay can be realized.

If the Duty Cycle is exceeded in the Transmit Mode, all data will be sent but the inter-word times may be elongated. In the Receive Mode, exceeding the maximum Duty Cycle, will result in occasional loss of data.

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2 ARINC 429/561/568/575/582 Channels

Chapter 2 describes EXC-3000PC MAGICard operation for the ARINC-429/561/568/575/582. The topics covered in this chapter are:

2.1 ARINC Global Control Registers
- Map page 2-2
- Definitions page 2-3

2.2 ARINC Channel Control Registers
- Maps page 2-17
- Definitions page 2-27

2.3 Transmit Channel Operation page 2-35
- ARINC Transmit Instruction Stack page 2-36
- Transmit Data Block Format page 2-40

2.4 Receive Channel Operation page 2-43
- Sequential and Merge Modes page 2-44
- Look-Up Table Mode Operation page 2-51

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2.1 ARINC Global Control Registers

Global Control Registers can be set at any time.

Reserved	7F00-7F3A H	Channel 4 Configuration Status	7F62 H
		Channel 5 Configuration Status	7F64 H
Interrupt Status Busy	7F3C H	Channel 6 Configuration Status	7F66 H
Receive Merge Status	7F3E H	Channel 7 Configuration Status	7F68 H
Receive Merge Interrupt/Trigger Condition	7F40 H	Channel 8 Configuration Status	7F6A H
Receive Merge Configuration	7F42 H	Channel 9 Configuration Status	7F6C H
Receive Merge Label Trigger	7F44 H	ARINC Programmable Bit Rate	7F6E H
Receive Merge Error Count	7F46 H	Interrupt Status	7F70 H
Receive Merge Interval Count Trigger	7F48 H	Firmware Revision	7F72 H
Receive Merge Buffer Wraparound	7F4A H	Board Status	7F74 H
Receive Merge Word Count Trigger	7F4C H	Board ID (Handshake)	7F76 H
Receive Merge Word Count	7F4E H	Host Ready (Handshake)	7F78 H
Receive Merge Filter Table Start Address	7F50 H	Start / Stop	7F7A H
Receive Merge Current Pointer	7F52 H	Reset Time Tag	7F7C H
Receive Merge End Pointer	7F54 H	Reserved	7F7E H
Receive Merge Start Pointer	7F56 H	Interrupt Request Level Select	7F80 H
Receive Data Storage Mode	7F58 H	Reset Interrupt	7F82 H
Channel 0 Configuration Status	7F5A H	Software Reset	7F84 H
Channel 1 Configuration Status	7F5C H	Reserved	7F86-7FFF H
Channel 2 Configuration Status	7F5E H		
Channel 3 Configuration Status	7F60 H		

Figure 2-1 ARINC Global Control Registers Map

The registers are described in the order they appear on the map.

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Global Control Register Definitions

2.1.1 Interrupt Status Busy Register

Address: 7F3C (H)

The Interrupt Status Busy Register indicates whether the Channel *x* Status Register, the Receive Merge Status Register and the Interrupt Status Register may be accessed by the user.

Bit	Bit Name	Description
11-15		Reserved
10	**MRGBSY**	1 = Receive Merge Status Register is busy – do not access the register 0 = The contents of the register is valid and may be accessed
09	**CH9BSY**	1 = Channel 9 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 9 Status Register may be accessed
08	**CH8BSY**	1 = Channel 8 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 8 Status Register may be accessed
07	**CH7BSY**	1 = Channel 7 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 7 Status Register may be accessed
06	**CH6BSY**	1 = Channel 6 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 6 Status Register may be accessed
05	**CH5BSY**	1 = Channel 5 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 5 Status Register may be accessed
04	**CH4BSY**	1 = Channel 4 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 4 Status Register may be accessed
03	**CH3BSY**	1 = Channel 3 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 3 Status Register may be accessed
02	**CH2BSY**	1 = Channel 2 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 2 Status Register may be accessed
01	**CH1BSY**	1 = Channel 1 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 1 Status Register may be accessed
00	**CH0BSY**	1 = Channel 0 Status Register and the Global Interrupt Status Register are busy – do not access 0 = Channel 0 Status Register may be accessed

Interrupt Status Busy Register

NOTE Before accessing the global Interrupt Status Register, the user should wait until the Interrupt Status Busy Register = 0. The user then has at least 15 microseconds to safely access the status registers.

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2.1.2 Receive Merge Status Register

Address: 7F3E (H)

The Receive Merge Status Register indicates the operational status of the Merge Mode receive buffer. This register can be used to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. Writing a 0 to this register resets the status bits.

Bit	Bit Name – Interrupt Cause
07-15	Reserved
06	Stopped on Buffer Full
05	Error Word Received
04	Word Count Trigger
03	Interval Count Trigger
02	Label Received
00-01	Reserved

Receive Merge Status Register

NOTE The Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the Filter Table.

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2.1.3 Receive Merge Interrupt /Trigger Condition Register

Address: 7F40 (H)

The Receive Merge Interrupt/Trigger Condition Register sets the Interrupt and Trigger condition or conditions for ARINC receive channels in Merge Mode. The Trigger Conditions set a pulse on the External Trigger Connector, J1.

Trigger Condition Bits 08-15

Bit	Bit Name
15	Reserved
14	Stopped on Buffer Full
13	Error Word Received
12	Data Word Count Trigger
11	Interval Count Trigger
10	Label Received
08-09	Reserved

Interrupt Condition Bits 00-07

Bit	Bit Name
07	Reserved
06	Stopped On Buffer Full
05	Error Word Received
04	Data Word Count Trigger
03	Interval Count Trigger
02	Label Received
00-01	Reserved

Receive Merge Interval/Trigger Condition Register

NOTE 1. The Label Received interrupt or trigger only occurs upon reception of a label that has been marked for interrupt in the Filter Table.

2. To activate the Interval Count Trigger interrupt or trigger, the Receive Merge Interval Count Trigger Register must also be set. (see Receive Merge Interval Count Trigger Register, page 2-7).

3. To activate Data Word Count Trigger interrupt or trigger, the Receive Merge Word Count Trigger Register must also be set. (see Receive Merge Word Count Trigger Register, page 2-7).

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2.1.4 Receive Merge Configuration Register

Address: 7F42 (H)

The Receive Merge Configuration Register sets up run parameters for Merge Mode.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**Enable Receive Filter Table**	1 = Enable filter table. (Stores Labels per table) 0 = Disables table. Stores all Labels.
08	**Reserved**	Set to 0
07	**Receive Label Trigger**	1 = Start data storage upon receipt of Label *xx*. (see Receive Merge Label Trigger Register) 0 = Receive stores data without Start Label Trigger.
06	**Receive Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receive wraps around the data in the block.
00-05	**Reserved**	Set to 0

Receive Merge Configuration Register

2.1.5 Receive Merge Label Trigger Register

Address: 7F44 (H)

The Receive Merge Label Trigger Register is used in conjunction with the Receive Label Trigger bit in the Receive Merge Configuration Register to begin the reception and storage of data upon receipt of a unique ARINC label.

The board will not store any ARINC words received prior to the first instance of this label.

Bit	Description
08-15	Set to 0
00-07	Trigger Label

Receive Merge Label Trigger Register

2.1.6 Receive Merge Error Count Register

Address: 7F46 (H)

The Receive Merge Error Count Register is a 16-bit counter. The register indicates the number of error words received on the channel. This counter Register wraps around and is reset only by the user.

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2.1.7 Receive Merge Interval Count Trigger Register

Address: 7F48 (H)

The Receive Merge Interval Count Trigger Register (a 16-bit value) allows the user to generate an interrupt (or pollable bit) every *N* number of words, where *N* is the value written to this register. For example, to request an interrupt after every 5 ARINC words, write 05 to this register.

To generate an interrupt or trigger, the appropriate bit must also be set in the Receive Merge Interrupt Condition Register (see Receive Merge Interrupt /Trigger Condition Register, page 2-5).

2.1.8 Receive Merge Buffer Wraparound Register

Address: 7F4A (H)

The Receive Merge Buffer Wraparound Register contains 2 bits for synchronization with the host.

Bit	Description
15	Multiple Wraparound - data lost
14	Single Wraparound - the receive buffer has wrapped around once since the last data read
00-13	Reserved

Receive Merge Buffer Wraparound Register

2.1.9 Receive Merge Word Count Trigger Register

Address: 7F4C (H)

The Receive Merge Word Count Trigger Register sets a trigger (used for polling or interrupts) and a flag that indicates when a specific number of words have been received (1- 65535).

To generate a trigger or interrupt, the appropriate bit in the Receive Merge Interrupt/ Trigger Condition Register must also be set. (see Receive Merge Interrupt /Trigger Condition Register, page 2-5).

NOTE This trigger is set when the value in the Receive Merge Word Counter matches the value set in this register.

2.1.10 Receive Merge Word Counter

Address: 7F4E (H)

The Receive Merge Word Counter indicates the number of ARINC words received (0-65535). This register wraps around to 0 after it reaches 65535. The user can reset the register only when the channel is stopped.

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2.1.11 Receive Merge Filter Table Start Address

Address: 7F50 (H)

The Receive Merge Filter Table Start Address sets the start address of the (256 x 8) Label Filter Table as described in the Sequential storage mode (see Receive Buffer Storage Sequence, page 2-45). The address must be on a word boundary.

2.1.12 Receive Merge Current Pointer

Address: 7F52 (H)

The Receive Merge Current Pointer indicates the current address where the next ARINC receive word is to be placed in the Receive buffer. This pointer value is incremented after the entire receive block (ARINC word, Time Tag, and Status) is written into memory.

2.1.13 Receive Merge End Pointer

Address: 7F54 (H)

The Receive Merge End Pointer sets the End Address of the Receive Data buffer. The data will wrap around or stop when the buffer is full, (when the End Address is reached), depending upon the contents of the Receive Merge Configuration Register Wraparound bit. (See Receive Merge Configuration Register, page 2-6).

2.1.14 Receive Merge Start Pointer

Address: 7F56 (H)

The Receive Merge Start Pointer sets the Start Address of the Receive Data buffer. The address must be on a word boundary within the Receive Data Block areas.

Example To cause the Merge buffer to begin at byte offset 1A0 (H), write a 1A0 (H) to this register.

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2.1.15 Receive Data Storage Mode Register

Address: 7F58 (H)

The Receive Data Storage Mode register is used to select the Receive Data Storage Mode and the Merge Mode option. ARINC Data Words can be stored with Time Tag and Status words appended to the data block or they can be stored without these additional words. Set bit 00 to a logic 0, to select the standard mode which appends both Time Tag and Status Words to each ARINC word stored in memory.

Set register bit 00 to logic 1 to select **Data Only mode**.

Bit 01 controls the Receive Merge Mode selection. Logic 0 selects the standard independent mode that utilizes different receive buffer areas for each receive channel. Logic 1 selects the **Merge Mode** that utilizes a single receive buffer for all channels. Each Receive Status Word, in this case, is tagged with Channel Code information.

The Merge Mode Control Registers are used only when the Merge Mode option is selected.

Bit	Description
02-15	0
01	Merge Mode Option 0 = Independent Mode 1 = Merge Mode
00	Receive Data Storage Mode 0 = Standard Mode 1 = Store Only Data

Receive Data Storage Mode Register

NOTE 1. If Data Only Storage Mode is selected (bit 00 set to 1), storage will be per independent channel regardless of the state of bit 01.

2. Data Only Storage Mode is not available in Look-up Table Mode.

3. The Receive Data Storage Mode Register can only be changed when all the channels are turned off for at least 1 msec. (Stop/Start register = 0).

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2.1.16 Channel *x* Configuration Status Register

Address: 7F5A-7F6C (H)

These Registers indicate to the host the type of channel configured in each channel socket on the board.

Bit	Description
05-15	Reserved – set to 0
00-04	Configuration Status Code

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Configuration Status Code
0	0	0	0	0	Undefined Channel
0	0	0	0	1	ARINC-429 Receive Channel
0	0	0	1	0	ARINC-429 Transmit Channel
0	0	0	1	1	ARINC-561 Receive Channel
0	0	1	0	0	ARINC-561 Transmit Channel
0	0	1	0	1	ARINC-568 Receive Channel
0	0	1	1	0	ARINC-568 Transmit Channel
0	0	1	1	1	ARINC-575 Receive Channel
0	1	0	0	0	ARINC-575 Transmit Channel
0	1	0	0	1	ARINC-582 2-Wire Receive Channel
0	1	0	1	0	ARINC-582 2-Wire Transmit Channel
0	1	0	1	1	ARINC-582 6-Wire Receive Channel
0	1	1	0	0	ARINC-582 6-Wire Transmit Channel
0	1	1	0	1	ARINC-575 24-Bit Receive Channel
0	1	1	1	0	ARINC-575 24-Bit Transmit Channel
0	1	1	1	1	Free code for future channels
1	0	0	0	0	RS-232 Channel
1	0	0	0	1	RS-422 Channel
1	0	0	1	0	RS-485 Channel
1	0	0	1	1	RS-423 Channel
1	0	1	0	0	Free code for future channels
1	0	1	0	1	Free code for future channels
1	0	1	1	0	Free code for future channels
1	0	1	1	1	Free code for future channels
1	1	0	0	0	Free code for future channels
1	1	0	0	1	Free code for future channels
1	1	0	1	0	Free code for future channels
1	1	0	1	1	Free code for future channels
1	1	1	0	0	Free code for future channels
1	1	1	0	1	reserved
1	1	1	1	0	reserved
1	1	1	1	1	reserved

Channel *x* Configuration Status Register

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2.1.17 ARINC Programmable Bit Rate Register

Address: 7F6E (H)

The ARINC Programmable Bit Rate Register selects the programmable bit rate value for the ARINC channels. This register is only read by the firmware when the Start/Stop Register contains a value of 0, i.e. all channels are inactive for at least 1 msec.

Bit	Description
15	0 = 33 MHz 1 = 40 MHz Should be the same as the Baud Rate Generator Oscillator Frequency bit in the Board Status Register, see page 2-13
11-14	Reserved – set to 0
00-10	Bit Rate value

ARINC Programmable Bit Rate Register

1. To calculate the Bit Rate Value (BRV) when the Baud Rate Generator Oscillator Frequency = **33 MHz**:

$$BRV = \frac{4125}{\text{freq (KHz)}} - 1$$

Example Desired programmable bit rate is 100 KHz:

$$BRV = \frac{4125}{100\ KHz} - 1 = 41 - 1 = 40\ \text{Dec or (0028 H)}$$

Note: The number has been rounded off to 41 (not 41.25)

Write the value 0028 (H) to this register.

2. To calculate the Bit Rate Value (BRV) when the Baud Rate Generator Oscillator Frequency = **40 MHz**:

$$BRV = \frac{5000}{\text{freq (KHz)}} - 1$$

Example Desired programmable bit rate is 12.5 KHz:

$$BRV = \frac{5000}{12.5\ KHz} - 1 = 399\ \text{Dec or (018F H)}$$

Write the value 818F (H) to this register.

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2.1.18 Interrupt Status Register

Address: 7F70 (H)

The Interrupt Status Register indicates which channel issued the interrupt: 1 = Active. The status bit or bits are only reset by the user.

Bit	Bit Name
10-15	Reserved – set to 0
09	Channel 9 Interrupt Status Bit
08	Channel 8 Interrupt Status Bit
07	Channel 7 Interrupt Status Bit
06	Channel 6 Interrupt Status Bit
05	Channel 5 Interrupt Status Bit
04	Channel 4 Interrupt Status Bit
03	Channel 3 Interrupt Status Bit
02	Channel 2 Interrupt Status Bit
01	Channel 1 Interrupt Status Bit
00	Channel 0 Interrupt Status Bit

Interrupt Status Register

2.1.19 Firmware Revision Register

Address: 7F72 (H)

The Firmware Revision Register indicates the revision level of the firmware. For example: 0114 (H) = Rev 1.14.

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2.1.20 Board Status Register

Address: 7F74 (H)

The Board Status Register indicates the result of the power-up, Self-test of the board.

Bit	Bit Name	Description
13-15	Reserved.	set to 0
12	Baud Rate Generator Oscillator Frequency	1 = 40 MHz 0 = 33 MHz
11	Host Ready Timeout	
10	Memory Status Bit	1 = Memory OK 0 = Memory failed
09	Channel 9 Status Bit	1 = Self-test OK 0 = Self-test fail
08	Channel 8 Status Bit	1 = Self-test OK 0 = Self-test fail
07	Channel 7 Status Bit	1 = Self-test OK 0 = Self-test fail
06	Channel 6 Status Bit	1 = Self-test OK 0 = Self-test fail
05	Channel 5 Status Bit	1 = Self-test OK 0 = Self-test fail
04	Channel 4 Status Bit	1 = Self-test OK 0 = Self-test fail
03	Channel 3 Status Bit	1 = Self-test OK 0 = Self-test fail
02	Channel 2 Status Bit	1 = Self-test OK 0 = Self-test fail
01	Channel 1 Status Bit	1 = Self-test OK 0 = Self-test fail
00	Channel 0 Status Bit	1 = Self-test OK 0 = Self-test fail

Board Status Register

NOTE

1. The 'Self-test Fail' is set when the channel Self-test fails or when the channel is not present on the board.
2. The board continues to operate (wait for a Host Ready), on condition of channel Self-test failures *but* will not continue to operate on condition of a memory failure.

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2.1.21 Board ID (Handshake) Register

Address: 7F76 (H)

Handshake from the board indicating that the board has completed its initialization sequence and that the board is ready to be accessed by the host. The board writes the value 3000 (H) into this register when ready. (See Host Ready Register, page 2-14).

2.1.22 Host Ready (Handshake) Register

Address: 7F78 (H)

After power-up or a software reset, the user must write a 0 to the Board Ready Register. Then wait for the contents of the Host Ready Register to be 0, and write the value 1234 (H) to it. This indicates to the board that the host system has finished its power-up sequence (BIOS memory tests, etc.) and is ready to communicate with the board. The board then executes its initialization procedure. When the procedures are completed, a value of 3000 (H) is written to the Board Ready Register.

If, after a timeout period (approximately 45 seconds after power-up) the host does not write this value to the register, the board sets the Host Ready Timeout bit in the Board Status Register. (See Board Status Register, page 2-13).

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2.1.23 Start / Stop Register

Address: 7F7A (H)

The user can start one or more channels at the same time - wait a minimum of 500 µsec. between writes to this register.

Bit	Description	
10-15	Reserved – set to 0	
09	Channel 9 Start Bit	1 = Start 0 = Stop
08	Channel 8 Start Bit	1 = Start 0 = Stop
07	Channel 7 Start Bit	1 = Start 0 = Stop
06	Channel 6 Start Bit	1 = Start 0 = Stop
05	Channel 5 Start Bit	1 = Start 0 = Stop
04	Channel 4 Start Bit	1 = Start 0 = Stop
03	Channel 3 Start Bit	1 = Start 0 = Stop
02	Channel 2 Start Bit	1 = Start 0 = Stop
01	Channel 1 Start Bit	1 = Start 0 = Stop
00	Channel 0 Start Bit	1 = Start 0 = Stop

Start/Stop Register

NOTE Only after the Start/Stop Register contains a 0 for at least 1 msec. do any changes in a channel's Transmit Amplitude Register, or Configuration Register, or the ARINC Programmable Bit Rate Register, or Receive Data Storage Mode Register, take effect on the board.

2.1.24 Reset Time Tag Register

Address: 7F7C (H)

Writing any non-0 value to the Reset Time Tag Register causes the Time Tag to be reset to 0. Upon completion of the Time Tag reset operation, the board clears the register.

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2.1.25 Interrupt Request Level Select Register

Address: 7F80 (H) WRITE ONLY

The Interrupt Request Level Select Register is used to select the interrupt request level to be used by the board within the PC/AT computer. The board ignores the high byte. The content of the low byte is shown below.

Bit	Description				
04-07	Piggyback adapter board interrupt request level				
00-03	Bit 3	Bit 2	Bit 1	Bit 0	
	0	0	0	0	No interrupt selected
	0	0	0	1	No interrupt selected
	0	0	1	0	Interrupt level 2
	0	0	1	1	Interrupt level 3
	0	1	0	0	Interrupt level 4
	0	1	0	1	Interrupt level 5
	0	1	1	0	Interrupt level 6
	0	1	1	1	Interrupt level 7
	1	0	0	0	No interrupt selected
	1	0	0	1	No interrupt selected
	1	0	1	0	Interrupt level 10
	1	0	1	1	Interrupt level 11
	1	1	0	0	Interrupt level 12
	1	1	0	1	No interrupt selected
	1	1	1	0	Interrupt level 14
	1	1	1	1	Interrupt level 15

Interrupt Level Select Request Register

An interrupt may be caused either by an on-board interrupt condition or by the transfer from a piggyback adapter on the board.

2.1.26 Reset Interrupt Register

Address: 7F82 (H) WRITE ONLY

Writing to the Reset Interrupt Register resets the board's interrupt. The least significant bit within the Data Word (bit 00) must be a logic 0. This register should be written to, immediately following the entry into the host interrupt service routine.

2.1.27 Software Reset Register

Address: 7F84 (H) WRITE ONLY

Writing a 0 to the Software Reset Register resets the board. Following a reset, the user must wait for a value of 0 to appear in the Host Ready Register (see Host Ready (Handshake) Register, page 2-14), then write 1234(H) to the register. The board then executes a Self-test, both memory and channels, clears all the dual-port RAM, resets the board's interrupts and updates the Board Status Register. The board then indicates that it is ready by writing a value of 3000 (H) to the Board Ready Register.

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2.2 ARINC Channel Control Registers

2.2.1 Channel 0 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7D20-7D22 H
Channel 0 Scratch Buffer End (W)	7D24 H
Channel 0 Scratch Buffer Start (W)	7D26 H
Channel 0 Status Register (R)	7D28 H
Channel 0 Interrupt / Trigger Conditions (W)	7D2A H
Channel 0 Transmit Amplitude (W)	7D2C H
Channel 0 Transmit Loop Counter (W)	7D2E H
Channel 0 Transmit Instruction Counter (W)	7D30 H
Channel 0 Transmit Instruction Stack Pointer (W)	7D32 H
Channel 0 Receive Label Trigger (W)	7D34 H
Channel 0 Receive Error Count (R/W)	7D36 H
Channel 0 Receive Interval Counter Trigger (W)	7D38 H
Reserved	7D3A H
Channel 0 Receive Data Word Counter Trigger (W)	7D3C H
Channel 0 Receive Buffer Wraparound (W)	7D3E H
Channel 0 Receive Data Word Count (R)	7D40 H
Channel 0 Receive Filter Table Start Address (W)	7D42 H
Channel 0 Receive Look-Up Table Start Address (W)	7D44 H
Channel 0 Receive Data Current Pointer (R)	7D46 H
Channel 0 Receive Data End Pointer (W)	7D48 H
Channel 0 Receive Data Start Pointer (W)	7D4A H
Reserved	7D4C H
Channel 0 Configuration (W)	7D4E H

Figure 2-2 Channel 0 Control Register Block Map

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2.2.2 Channel 1 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7D50-7D52 H
Channel 1 Scratch Buffer End (W)	7D54 H
Channel 1 Scratch Buffer Start (W)	7D56 H
Channel 1 Status Register (R)	7D58 H
Channel 1 Interrupt / Trigger Conditions (W)	7D5A H
Channel 1 Transmit Amplitude (W)	7D5C H
Channel 1 Transmit Loop Counter (W)	7D5E H
Channel 1 Transmit Instruction Counter (W)	7D60 H
Channel 1 Transmit Instruction Stack Pointer (W)	7D62 H
Channel 1 Receive Label Trigger (W)	7D64 H
Channel 1 Receive Error Count (R/W)	7D66 H
Channel 1 Receive Interval Counter Trigger (W)	7D68 H
Reserved	7D6A H
Channel 1 Receive Data Word Counter Trigger (W)	7D6C H
Channel 1 Receive Buffer Wraparound (W)	7D6E H
Channel 1 Receive Data Word Count (R)	7D70 H
Channel 1 Receive Filter Table Start Address (W)	7D72 H
Channel 1 Receive Look-Up Table Start Address (W)	7D74 H
Channel 1 Receive Data Current Pointer (R)	7D76 H
Channel 1 Receive Data End Pointer (W)	7D78 H
Channel 1 Receive Data Start Pointer (W)	7D7A H
Reserved	7D7C H
Channel 1 Configuration (W)	7D7E H

Figure 2-3 Channel 1 Control Register Block Map

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2.2.3 Channel 2 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7D80-7D82 H
Channel 2 Scratch Buffer End (W)	7D84 H
Channel 2 Scratch Buffer Start (W)	7D86 H
Channel 2 Status Register (R)	7D88 H
Channel 2 Interrupt / Trigger Conditions (W)	7D8A H
Channel 2 Transmit Amplitude (W)	7D8C H
Channel 2 Transmit Loop Counter (W)	7D8E H
Channel 2 Transmit Instruction Counter (W)	7D90 H
Channel 2 Transmit Instruction Stack Pointer (W)	7D92 H
Channel 2 Receive Label Trigger (W)	7D94 H
Channel 2 Receive Error Count (R/W)	7D96 H
Channel 2 Receive Interval Counter Trigger (W)	7D98 H
Reserved	7D9A H
Channel 2 Receive Data Word Counter Trigger (W)	7D9C H
Channel 2 Receive Buffer Wraparound (W)	7D9E H
Channel 2 Receive Data Word Count (R)	7DA0 H
Channel 2 Receive Filter Table Start Address (W)	7DA2 H
Channel 2 Receive Look-Up Table Start Address (W)	7DA4 H
Channel 2 Receive Data Current Pointer (R)	7DA6 H
Channel 2 Receive Data End Pointer (W)	7DA8 H
Channel 2 Receive Data Start Pointer (W)	7DAA H
Reserved	7DAC H
Channel 2 Configuration (W)	7DAE H

Figure 2-4 Channel 2 Control Register Block Map

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2.2.4 Channel 3 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7DB0-7DB2 H
Channel 3 Scratch Buffer End (W)	7DB4 H
Channel 3 Scratch Buffer Start (W)	7DB6 H
Channel 3 Status Register (R)	7DB8 H
Channel 3 Interrupt / Trigger Conditions (W)	7DBA H
Channel 3 Transmit Amplitude (W)	7DBC H
Channel 3 Transmit Loop Counter (W)	7DBE H
Channel 3 Transmit Instruction Counter (W)	7DC0 H
Channel 3 Transmit Instruction Stack Pointer (W)	7DC2 H
Channel 3 Receive Label Trigger (W)	7DC4 H
Channel 3 Receive Error Count (R/W)	7DC6 H
Channel 3 Receive Interval Counter Trigger (W)	7DC8 H
Reserved	7DCA H
Channel 3 Receive Data Word Counter Trigger (W)	7DCC H
Channel 3 Receive Buffer Wraparound (W)	7DCE H
Channel 3 Receive Data Word Count (R)	7DD0 H
Channel 3 Receive Filter Table Start Address (W)	7DD2 H
Channel 3 Receive Look-Up Table Start Address (W)	7DD4 H
Channel 3 Receive Data Current Pointer (R)	7DD6 H
Channel 3 Receive Data End Pointer (W)	7DD8 H
Channel 3 Receive Data Start Pointer (W)	7DDA H
Reserved	7DDC H
Channel 3 Configuration (W)	7DDE H

Figure 2-5 Channel 3 Control Register Block Map

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2.2.5 Channel 4 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7DE0-7DE2 H
Channel 4 Scratch Buffer End (W)	7DE4 H
Channel 4 Scratch Buffer Start (W)	7DE6 H
Channel 4 Status Register (R)	7DE8 H
Channel 4 Interrupt / Trigger Conditions (W)	7DEA H
Channel 4 Transmit Amplitude (W)	7DEC H
Channel 4 Transmit Loop Counter (W)	7DEE H
Channel 4 Transmit Instruction Counter (W)	7DF0 H
Channel 4 Transmit Instruction Stack Pointer (W)	7DF2 H
Channel 4 Receive Label Trigger (W)	7DF4 H
Channel 4 Receive Error Count (R/W)	7DF6 H
Channel 4 Receive Interval Counter Trigger (W)	7DF8 H
Reserved	7DFA H
Channel 4 Receive Data Word Counter Trigger (W)	7DFC H
Channel 4 Receive Buffer Wraparound (W)	7DFE H
Channel 4 Receive Data Word Count (R)	7E00 H
Channel 4 Receive Filter Table Start Address (W)	7E02 H
Channel 4 Receive Look-Up Table Start Address (W)	7E04 H
Channel 4 Receive Data Current Pointer (R)	7E06 H
Channel 4 Receive Data End Pointer (W)	7E08 H
Channel 4 Receive Data Start Pointer (W)	7E0A H
Reserved	7E0C H
Channel 4 Configuration (W)	7E0E H

Figure 2-6 Channel 4 Control Register Block Map

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2.2.6 Channel 5 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7E10-7E12 H
Channel 5 Scratch Buffer End (W)	7E14 H
Channel 5 Scratch Buffer Start (W)	7E16 H
Channel 5 Status Register (R)	7E18 H
Channel 5 Interrupt / Trigger Conditions (W)	7E1A H
Channel 5 Transmit Amplitude (W)	7E1C H
Channel 5 Transmit Loop Counter (W)	7E1E H
Channel 5 Transmit Instruction Counter (W)	7E20 H
Channel 5 Transmit Instruction Stack Pointer (W)	7E22 H
Channel 5 Receive Label Trigger (W)	7E24 H
Channel 5 Receive Error Count (R/W)	7E26 H
Channel 5 Receive Interval Counter Trigger (W)	7E28 H
Reserved	7E2A H
Channel 5 Receive Data Word Counter Trigger (W)	7E2C H
Channel 5 Receive Buffer Wraparound (W)	7E2E H
Channel 5 Receive Data Word Count (R)	7E30 H
Channel 5 Receive Filter Table Start Address (W)	7E32 H
Channel 5 Receive Look-Up Table Start Address (W)	7E34 H
Channel 5 Receive Data Current Pointer (R)	7E36 H
Channel 5 Receive Data End Pointer (W)	7E38 H
Channel 5 Receive Data Start Pointer (W)	7E3A H
Reserved	7E3C H
Channel 5 Configuration (W)	7E3E H

Figure 2-7 Channel 5 Control Register Block Map

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2.2.7 Channel 6 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7E40-7E42 H
Channel 6 Scratch Buffer End (W)	7E44 H
Channel 6 Scratch Buffer Start (W)	7E46 H
Channel 6 Status Register (R)	7E48 H
Channel 6 Interrupt / Trigger Conditions (W)	7E4A H
Channel 6 Transmit Amplitude (W)	7E4C H
Channel 6 Transmit Loop Counter (W)	7E4E H
Channel 6 Transmit Instruction Counter (W)	7E50 H
Channel 6 Transmit Instruction Stack Pointer (W)	7E52 H
Channel 6 Receive Label Trigger (W)	7E54 H
Channel 6 Receive Error Count (R/W)	7E56 H
Channel 6 Receive Interval Counter Trigger (W)	7E58 H
Reserved	7E5A H
Channel 6 Receive Data Word Counter Trigger (W)	7E5C H
Channel 6 Receive Buffer Wraparound (W)	7E5E H
Channel 6 Receive Data Word Count (R)	7E60 H
Channel 6 Receive Filter Table Start Address (W)	7E62 H
Channel 6 Receive Look-Up Table Start Address (W)	7E64 H
Channel 6 Receive Data Current Pointer (R)	7E66 H
Channel 6 Receive Data End Pointer (W)	7E68 H
Channel 6 Receive Data Start Pointer (W)	7E6A H
Reserved	7E6C H
Channel 6 Configuration (W)	7E6E H

Figure 2-8 Channel 6 Control Register Block Map

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2.2.8 Channel 7 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7E70-7E72 H
Channel 7 Scratch Buffer End (W)	7E74 H
Channel 7 Scratch Buffer Start (W)	7E76 H
Channel 7 Status Register (R)	7E78 H
Channel 7 Interrupt / Trigger Conditions (W)	7E7A H
Channel 7 Transmit Amplitude (W)	7E7C H
Channel 7 Transmit Loop Counter (W)	7E7E H
Channel 7 Transmit Instruction Counter (W)	7E80 H
Channel 7 Transmit Instruction Stack Pointer (W)	7E82 H
Channel 7 Receive Label Trigger (W)	7E84 H
Channel 7 Receive Error Count (R/W)	7E86 H
Channel 7 Receive Interval Counter Trigger (W)	7E88 H
Reserved	7E8A H
Channel 7 Receive Data Word Counter Trigger (W)	7E8C H
Channel 7 Receive Buffer Wraparound (W)	7E8E H
Channel 7 Receive Data Word Count (R)	7E90 H
Channel 7 Receive Filter Table Start Address (W)	7E92 H
Channel 7 Receive Look-Up Table Start Address (W)	7E94 H
Channel 7 Receive Data Current Pointer (R)	7E96 H
Channel 7 Receive Data End Pointer (W)	7E98 H
Channel 7 Receive Data Start Pointer (W)	7E9A H
Reserved	7E9C H
Channel 7 Configuration (W)	7E9E H

Figure 2-9 Channel 7 Control Register Block Map

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2.2.9 Channel 8 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7EA0-7EA2 H
Channel 8 Scratch Buffer End (W)	7EA4 H
Channel 8 Scratch Buffer Start (W)	7EA6 H
Channel 8 Status Register (R)	7EA8 H
Channel 8 Interrupt / Trigger Conditions (W)	7EAA H
Channel 8 Transmit Amplitude (W)	7EAC H
Channel 8 Transmit Loop Counter (W)	7EAE H
Channel 8 Transmit Instruction Counter (W)	7EB0 H
Channel 8 Transmit Instruction Stack Pointer (W)	7EB2 H
Channel 8 Receive Label Trigger (W)	7EB4 H
Channel 8 Receive Error Count (R/W)	7EB6 H
Channel 8 Receive Interval Counter Trigger (W)	7EB8 H
Reserved	7EBA H
Channel 8 Receive Data Word Counter Trigger (W)	7EBC H
Channel 8 Receive Buffer Wraparound (W)	7EBE H
Channel 8 Receive Data Word Count (R)	7EC0 H
Channel 8 Receive Filter Table Start Address (W)	7EC2 H
Channel 8 Receive Look-Up Table Start Address (W)	7EC4 H
Channel 8 Receive Data Current Pointer (R)	7EC6 H
Channel 8 Receive Data End Pointer (W)	7EC8 H
Channel 8 Receive Data Start Pointer (W)	7ECA H
Reserved	7ECC H
Channel 8 Configuration (W)	7ECE H

Figure 2-10 Channel 8 Control Register Block Map

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2.2.10 Channel 9 Control Register Block Map

The registers are marked read only (R) or write only (W) – only the Receive Error Count Register is both (R) and (W).

Reserved	7ED0-7ED2 H
Channel 9 Scratch Buffer End (W)	7ED4 H
Channel 9 Scratch Buffer Start (W)	7ED6 H
Channel 9 Status Register (R)	7ED8 H
Channel 9 Interrupt / Trigger Conditions (W)	7EDA H
Channel 9 Transmit Amplitude (W)	7EDC H
Channel 9 Transmit Loop Counter (W)	7EDE H
Channel 9 Transmit Instruction Counter (W)	7EE0 H
Channel 9 Transmit Instruction Stack Pointer (W)	7EE2 H
Channel 9 Receive Label Trigger (W)	7EE4 H
Channel 9 Receive Error Count (R/W)	7EE6 H
Channel 9 Receive Interval Counter Trigger (W)	7EE8 H
Reserved	7EEA H
Channel 9 Receive Data Word Counter Trigger (W)	7EEC H
Channel 9 Receive Buffer Wraparound (W)	7EEE H
Channel 9 Receive Data Word Count (R)	7EF0 H
Channel 9 Receive Filter Table Start Address (W)	7EF2 H
Channel 9 Receive Look-Up Table Start Address (W)	7EF4 H
Channel 9 Receive Data Current Pointer (R)	7EF6 H
Channel 9 Receive Data End Pointer (W)	7EF8 H
Channel 9 Receive Data Start Pointer (W)	7EFA H
Reserved	7EFC H
Channel 9 Configuration (W)	7EFE H

Figure 2-11 Channel 9 Control Register Block Map

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Channel Control Register Definitions

2.2.11 Channel *x* Scratch Buffer End Register — WRITE

Data Rate Mode

For transmission in Data Rate Mode, the Channel *x* Buffer End Register contains the end address of the scratch buffer that must be assigned by the user. See Channel *x* Scratch Buffer Start Register, page 2-27.

2.2.12 Channel *x* Scratch Buffer Start Register — WRITE

Data Rate Mode

For transmission in Data Rate Mode, the user must allocate a scratch buffer for use by the firmware. Its length must be at least (Transmit Instruction Counter x 10 + 4) bytes. If the buffer is not long enough, the channel will turn itself off without transmitting.

The Channel *x* Scratch Buffer Start Register contains the start address of this buffer. The address must be a word boundary.

2.2.13 Channel *x* Status Register — READ

The Channel *x* Status Register indicates the operational status of the channel. This register can be used to poll the status of the channel or it can be used with interrupts. When used in conjunction with interrupts, the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. The user must reset status bits, by writing a 0 to this register.

Bit	Bit Name – Interrupt Cause
07-15	Reserved
06	Receive - Stopped on Buffer Full
05	Receive - Error Word Received
04	Receive - Data Word Count Trigger
03	Receive - Interval Count Trigger
02	Receive - Label Received
01	Transmit - End of Frame
00	Transmit - End of Block

Channel *x* Status Register

Look-Up Mode

In Look-Up Mode, the Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the label's Control byte.

Sequential Mode

In Sequential Mode, the Label Received status bit is set upon receipt of any label for which an interrupt has been requested via the Filter Table.

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2.2.14 Channel *x* Interrupt/Trigger Condition Register **WRITE**

The Channel *x* Interrupt /Trigger Condition Register sets the Interrupt and Trigger condition or conditions of the channel. The trigger conditions set a pulse on the External Trigger Connector, J1.

Trigger Condition Bits 08-15

Bit	Bit Name
15	Reserved
14	Receive – Stopped on Buffer Full
13	Receive – Error Word Received
12	Receive – Data Word Count Trigger (3)
11	Receive – Interval Count Trigger (2)
10	Receive – Label Received (1)
09	Transmit – End of Frame
08	Transmit – End of Block

Interrupt Condition Bits 00-07

Bit	Bit Name
07	Reserved
06	Receive – Stopped on Buffer Full
05	Receive – Error Word Received
04	Receive – Data Word Count Trigger (3)
03	Receive – Interval Count Trigger (2)
02	Receive – Label Received (1)
01	Transmit – End of Frame
00	Transmit – End of Block

Channel *x* InterruptTrigger Condition Register

NOTE 1. The Receive – Label Received interrupt or trigger only occurs upon reception of a label, which has been marked for interrupt in a Filter Table (in Sequential Mode) or in a Control Byte (in Look-up Table Mode).
This condition is *not* applicable for ARINC 575 24-bit channels.

2. To activate the Receive – Interval Count Trigger interrupt or trigger, the Channel *x* Receive Interval Counter Trigger Register must also be set.

3. To activate the Receive – Data Word Count Trigger interrupt or trigger, the Channel *x* Receive Data Word Counter Trigger register must also be set.

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2.2.15 Channel *x* Transmit Amplitude Register

WRITE

The Channel *x* Transmit Amplitude Register sets the Transmit amplitude level of the transmit channel. This register has a resolution of 39mv/bit. The maximum register value gives a voltage of 10V (peak) measured across the ARINC bus differentially. At startup and after a software reset, this register is initialized to 00FF (H), which is the maximum value.

Bit	Description
08-15	Set to 0
00-07	Amplitude Value

Channel *x* Transmit Amplitude Register

NOTE This register is not applicable to ARINC 561/568/582 6-wire channels.

2.2.16 Channel *x* Transmit Loop Counter

WRITE

The Channel *x* Transmit Loop counter sets the number of times to execute the transmit instruction blocks (the frame): *N*' Times or Continuous Loop. If the continuous value is selected, setting the related channel bit in the Global Start/Stop Register to a 0 can terminate the channel's operation.

Bit	Value	
00-15	**0000**	= Continuous
	0001	= One Time
	0002	= Two Times
		•
		•
		•
	FFFF	= 65535 Times

Channel *x* Transmit Loop Counter

2.2.17 Channel *x* Transmit Instruction Counter

WRITE

The Channel *x* Transmit Instruction Counter sets the number of Transmit Instruction blocks to process. These instruction blocks taken together comprise a frame.

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2.2.18 Channel *x* Transmit Instruction Stack Pointer

WRITE

The Channel *x* Transmit Instruction Stack Pointer sets the starting address of the Transmit Instruction Stack**.** The address must be a word boundary within the Transmit Instruction Stack area. For example, to place the Transmit Instruction stack starting at location 0300(H), write 0300(H) to this register.

2.2.19 Channel *x* Receive Label Trigger Register

WRITE

Sequential Mode

The Channel *x* Receive Label Trigger Register is used in conjunction with the Receive Label Trigger bit in the Channel *x* Configuration Register (see Channel *x* Configuration Register, page 2-33). This register enables the reception and storage of data upon receipt of a unique ARINC label. The board will not store any ARINC words received prior to the first instance of this label.

Bit	Description
08-15	Set to 0
00-07	Trigger Label

Channel *x* Receive Label Trigger Register

2.2.20 Channel *x* Receive Error Count Register

READ/WRITE

Sequential Mode

The 16-bit Channel *x* Receive Error Count Register indicates the number of errors received on a particular channel. To reset the register, write 0000 to it.

2.2.21 Channel *x* Receive Interval Counter Trigger Register

WRITE

Sequential Mode

The Channel *x* Receive Interval Counter Trigger Register allows the user to generate an interrupt and set a flag upon reception of every *N* number of words, where *N* is the value written to this register. For example, to request an interrupt after every five ARINC words, write 0005(H) to this register.

To generate an interrupt or a trigger, the appropriate bit must also be set in the Channel *x* Interrupt / Trigger Condition Register (see Channel *x* Interrupt/Trigger Condition Register, page 2-28).

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2.2.22 Channel *x* Receive Data Word Counter Trigger Register **WRITE**

Sequential Mode

The Channel *x* Receive Data Word Counter Trigger Register lets the user generate an interrupt and set a flag, which indicates when a specific number of words have been received (1-65535). To generate an interrupt, the appropriate bit must also be set in the Channel *x* Interrupt/Trigger Condition Register (see Channel *x* Interrupt/Trigger Condition Register, page 2-28).

NOTE This trigger is set when the value in the Receive Data Word Counter matches the value set in this register.

2.2.23 Channel *x* Receive Buffer Wraparound Register **WRITE**

The Channel *x* Receive Buffer Wraparound Register contains 2 bits for synchronization with the host.

Bit	Description
15	1 = Multiple Wraparound - Data Lost
14	1 = Single Wraparound since last data read
00-13	0

Receive Buffer Wraparound Register

NOTE Excalibur software drivers handle these bits. If these drivers, are used, they do not need to be modified.

The user should clear bit 14 each time the first word of the buffer is read. When the buffer wraps around it checks bit 14. If bit 14 is not set, the module sets it; otherwise the module sets bit 15.

2.2.24 Channel *x* Receive Data Word Count Register **READ**

Sequential Mode

The Channel *x* Receive Data Word Count Register indicates the number of ARINC words received (0-65535). This register wraps around to 0 after it reaches 65535. The user may reset the register to 0, only when the channel is stopped.

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2.2.25 Channel *x* Receive Filter Table Start Address

WRITE

Sequential Mode

The Channel *x* Receive Filter Table Start Address sets the Start Address of the 256 x 8 Label Filter Table as described in Sequential/Merge Mode, page 2-44. The address must be a word boundary. It is valid for several channels to use the same Filter Table.

This table is valid only if the Channel *x* Configuration Register Enable Receive Filter Table bit is set (see bit 09 in the Channel *x* Configuration Register, page 2-33.)

2.2.26 Channel *x* Receive Look-Up Table Start Address

WRITE

Look-Up Table Mode

The Channel *x* Receive Look-Up Table Start Address sets the start address of the 256 x 16 Receive Look-Up Table (see bit 05 in the Channel *x* Configuration Register, page 2-33.) The address must be a word boundary.

This address points to the *first* location of the Look-Up Table. The board stores one ARINC data block for each Label received. The data block contains: 32-bit ARINC word, 32-bit Time Tag, and the 16-bit Receive Status Word. The subsequent reception and storage of another ARINC word will overwrite the Data Block with the same ARINC Label.

2.2.27 Channel *x* Receive Data Current Pointer

READ

Sequential Mode

In Sequential Mode the Channel *x* Receive Data Current Pointer indicates the address where the next ARINC receive word is to be placed in the buffer. This pointer value is incremented after the entire receive block (ARINC word, Time Tag, and Status) is written into memory.

Look-Up Table

In Look-Up Table Mode this register contains the address of the last Bit ARINC receive word written to the receive area.

2.2.28 Channel *x* Receive Data End Pointer

WRITE

Sequential Mode

The Channel *x* Receive Data End Pointer sets the end address of the Receive Data buffer. The address must be a word boundary. The data will wrap around or stop when the buffer is full, (when the End Address is reached), depending upon the contents of the Receive Wrap Around control bit in the Channel *x* Configuration Register.

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2.2.29 Channel *x* Receive Data Start Pointer

WRITE

Sequential Mode

The Channel *x* Receive Data Start Pointer Register sets the start address of the Receive Data buffer. The address must be a word boundary within the Receive Data Blocks area.

Example To cause the Channel *x* Receive Data buffer to begin at address 01A0(H), write 01A0(H) to this register.

2.2.30 Channel *x* Configuration Register

WRITE

The Channel *x* Configuration Register sets up various run parameters for each channel. Bits that are not used (for example, receive-related bits while operating as a transmitter) are ignored by the board.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**Enable Receive Filter Table**	1 = Enable Filter Table (Stores labels per table) 0 = Disables table. Stores all labels. **Note:** This is not applicable for ARINC 575 24-bit channels.
08	**Transmit Mode Select** (6)	1 = Data Rate mode (per data block) 0 = Interblock Gap Time mode
07	**Receive Label Trigger**	1 = Start data storage upon receipt of Label xx. See Channel *x* Receive Label Trigger Register, page 2-31. 0 = Receive stores data without Start Label Trigger **Note:** This is not applicable for ARINC 575 24-bit channels.
06	**Receive Wrap Around**	1 = Data storage is halted when the buffer is full. 0 = Receive wraps around the data within the block. (This bit is used in Sequential Storage Mode only.)
05	**Receive Storage Mode**	1 = Sequential Storage Mode 0 = Look-up Table Mode (see Channel x Receive Look-Up Table Start Address, page 2-32). **Note:** This is not applicable for ARINC 575 24-bit channels.
04	**Parity: Even/Odd**	1 = Even 0 = Odd - Standard ARINC Mode
03	**Parity: On/Off**	1 = Off 0 = On
02	**Transmit Rise/Fall Time** (5)	1 = Lo Speed (10 +/- 5 µsec.) 0 = Hi Speed (1.5 +/- 0.5 µsec.)
00-01	**Bit Rate** (4)	If the Programmable Bit Rate is selected then the bit rate is defined by the Global ARINC Programmable Bit Rate Register.

Bit 01	Bit 00	Channel Bit rate
0	0	12.5 KHz – Lo Speed
0	1	100 KHz – Hi Speed
1	0	Programmable
1	1	Undefined

Channel *x* Configuration Register

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NOTE

1. The Channel *x* Configuration Register can only be written to when *all* the channels are turned off (via the Start/Stop Register).

2. The board should be started (via the Start/Stop Register) only after a minimum of 1 msec. from the time that the contents of the register have been modified.

3. All active Channel *x* Configuration Registers should be set up immediately following the Board Handshake procedure before programming other parameters.

4. ARINC-561/568/575/582 specify Lo Speed (Bit Rate) operation only.

5. Transmit Rise/Fall Time bit not applicable to ARINC 561/568/582 6-wire channels.

6. The Transmit Mode Select bit allows the user to select the transmission mode.

   A logic 1 instructs the transmitter to use the Inter-block Time/Data Rate Word as a Data Rate value and to send data blocks on a scheduled data rate basis – e.g., Data Block 1, every 50 msec. and Data Block 2, every 25 msec. In this mode, a scratch buffer must be allocated via the Channel *x* Scratch Buffer Start and Channel *x* Scratch Buffer End Registers.

   A logic 0 instructs the transmitter to use the Interblock Time/Data Rate Word as an Interblock Gap Time.

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2.3 Transmit Channel Operation

In transmit channel operation words are sent out in Blocks (groups of words). Each Block is sent with dedicated parameters: for example word count, interblock time, and error injection. The Blocks reside sequentially in stack structure, each pointing to its Data Buffer. The Blocks can be sent either Continuously or *N* times.

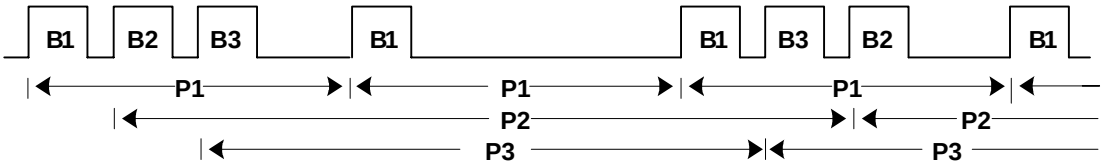
Each transmit channel has two basic modes of operation:

Interblock Time Mode Sends out sequential Blocks of words, each followed with its Interblock delay time.

B – Block
T – Interblock time



Data Rate Mode Sends out periodically Blocks of words, each with its period (data rate) time.



B – Block
P – Block period time

In transmit operation the user:

- Sets up the transmitting channel's parameters by writing to the various Channel *x* Control Registers;
- Creates an Instruction Stack for the transmitting channel;
- Writes the data into the dual-port RAM;
- Start transmission by writing to the Start/Stop Register found within the Global Control Register area.

The sequence of writes to memory is not important, except for the write to Start Register operation, which is performed last.

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2.3.1 ARINC Transmit Instruction Stack

The Transmit Instruction Stack is divided into Instruction Blocks, each containing four words. Each Instruction Block relates to a Data Buffer. A Data Buffer contains one or more ARINC words which the user desires to transmit with the same amount of delay time between each word. The stack is sequential, so that the first Instruction Block follows the second Data Block, and so on.

The Instruction Block consists of:

1st Word: The Control Word, which contains error injection parameters.

2nd Word: Contains 2 bytes:

1. An 8-bit Word Count which instructs the board as to the number of ARINC words to transmit within a particular block, and
2. An 8-bit, inter-word delay value which programs the time between words within the same buffer.

3rd Word: Contains a 16-bit, user-supplied data pointer. This is a 16-bit address (must be a word boundary) that points to the beginning of the Data Words within the memory.

4th Word: Is the Interblock Time/Data Rate value and is used to program the time between Data Block transfers or the transmission period for the specific data block.

For details see Figure 2-12, ARINC Transmit Instruction Stack, page 2-37.

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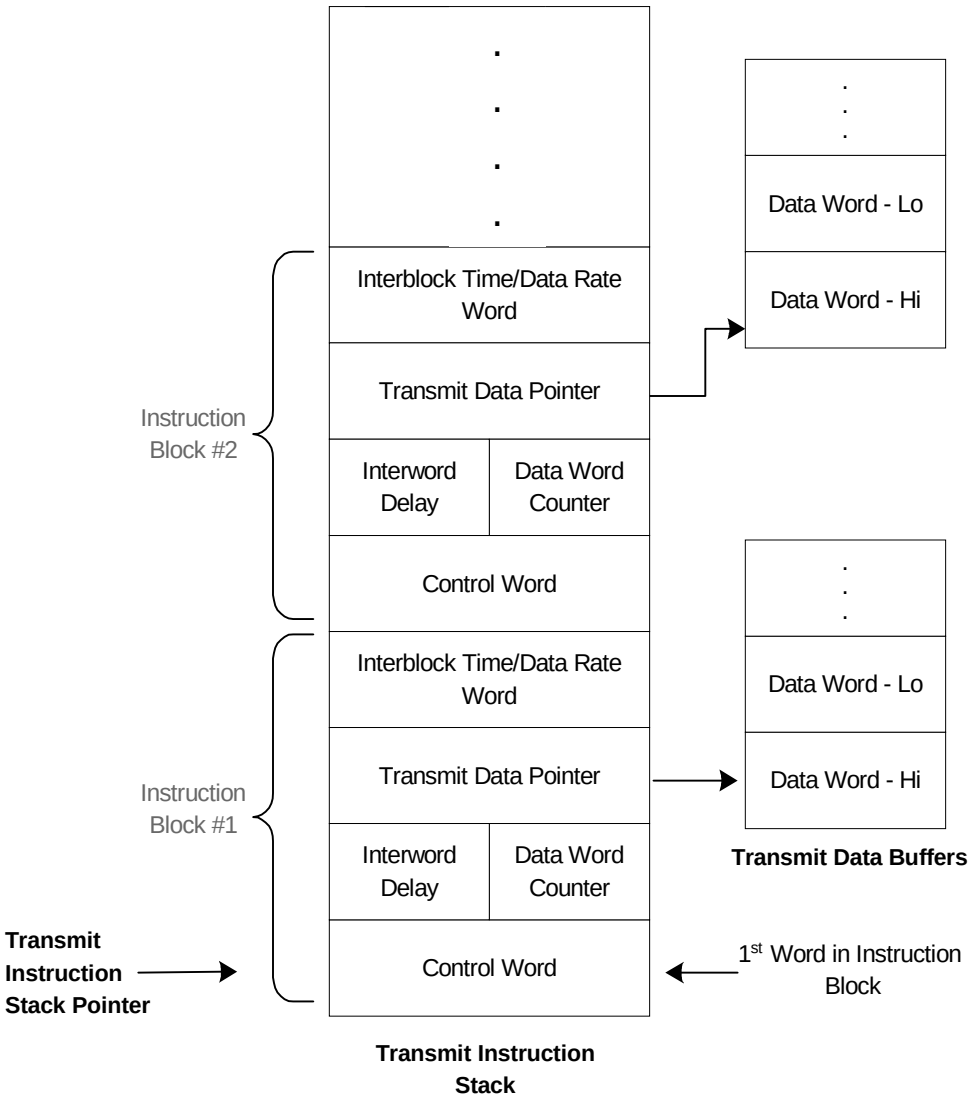


Figure 2-12 ARINC Transmit Instruction Stack Structure

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2.3.1.1 Control Word Definition

This is the 1st word in the ARINC Transmit Instruction Block.

Bit	Bit Name	Description
06-15	**Reserved**	Set to 0
05	**Suppress Parity (see Note)**	1 = Forces a no-parity condition within the word even though 'parity-on' has been selected in the Channel *x* Configuration Register 0 = Regular parity as set up in the Channel *x* Configuration Register
04	**Bit Count Lo Error**	1 = Thirty-one ARINC bits are transmitted within each word within the block 0 = No error
03	**Bit Count Hi Error**	1 = Thirty-three ARINC bits are transmitted within each word within the block 0 = No error
02	**Stretch Bit Error**	1 = The 2nd ARINC bit within each word within the block is 'stretched' causing a Manchester coding error. 0 = No error **Note**: This bit is valid for ARINC-429/575/582 2-wire only.
01	**Null Bit Error**	1 = A Null Bit Error is inserted within the second bit of each word within the Block (ARINC Bit 02). 0 = No error **Note**: This bit is valid for ARINC-429/575/582 2-wire only.
00	**Parity Error**	1 = A Parity Error is inserted within all ARINC words within the block. 0 = No error

Control Word Definition

NOTE The **Suppress Parity** is useful when most of the Data Buffers contain standard data with parity and a few buffers contain data type without parity. In such a case, the parity can be set ON for all words within the Channel *x* Configuration Register while exceptional cases, can be forced to NO PARITY, using this bit.

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2.3.1.2 Interword Delay/ Data Word Counter Word

This word is divided into two bytes, the Interword Delay (high byte) and the Data Word Counter (low byte).

The Interword Delay byte specifies the time between words within this data block. The resolution is in the form of 'bit times' according to the transmission bit rate.

Bit Rate	Resolution
Lo-Speed	80 µsec/bit
Hi-Speed	10 µsec/bit
Programmable	$\frac{1}{\text{Programmable Bit Rate (MHz)}}$

Interword Delay Resolution

NOTE The ARINC specification defines the minimum Interword time as 4 bit times, so values less that 4 may be interpreted on the receiving side as sync error

The Word Counter byte specifies the number of data words within this Data block (1-255).

2.3.1.3 Transmit Data Pointer

The Transmit Data Pointer is used to set the start address of the block's Transmit Data Buffer. The address must be a word boundary. The size of the buffer is determined by the Data Word Count value.

2.3.1.4 Interblock Time/Data Rate Word

The Interblock Time/Data Rate Word has two functions:

1. In **Standard Transmit Mode,** the Instruction Blocks are accessed sequentially and their associated Data Words transmitted according to this sequential order. The Interblock Time allows the user to specify the time between Data Blocks. It is inserted after the block transmission.

2. In **Data Rate Mode**, the user can specify the transmission period of the particular Data Block. If the number *N* is written to this location, then the message is transmitted every *N* bit times.

The resolution of this 16-bit word is according to the transmission bit rate which is the same as in the Interword Delay byte, see Interword Delay/ Data Word Counter Word.

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The Transmit Mode Select bit within the Channel x Configuration Register (see Channel *x* Configuration Register, page 2-33) determines mode selection.

NOTE In Data Rate Mode, a scratch buffer for the firmware must be allocated via the Channel *x* Scratch Buffer Start Register and Channel *x* Scratch Buffer End Register, see page 2-27.

2.3.2. Transmit Data Block Format

Figure 2-13 below illustrates the format of the Transmit Data Words within the memory.

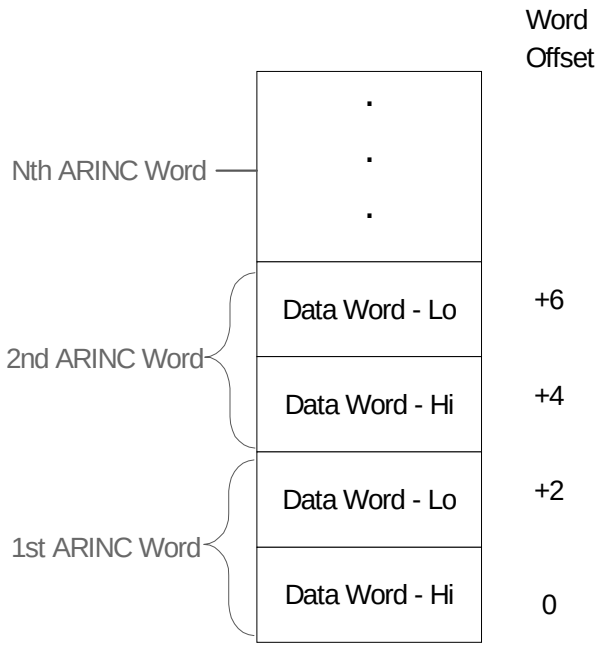


Figure 2-13 Transmit Data Block

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Figure 2-14 defines the locations and bit definitions of the data bytes within the memory. The numbers shown in the two words represent the ARINC word bit numbers.

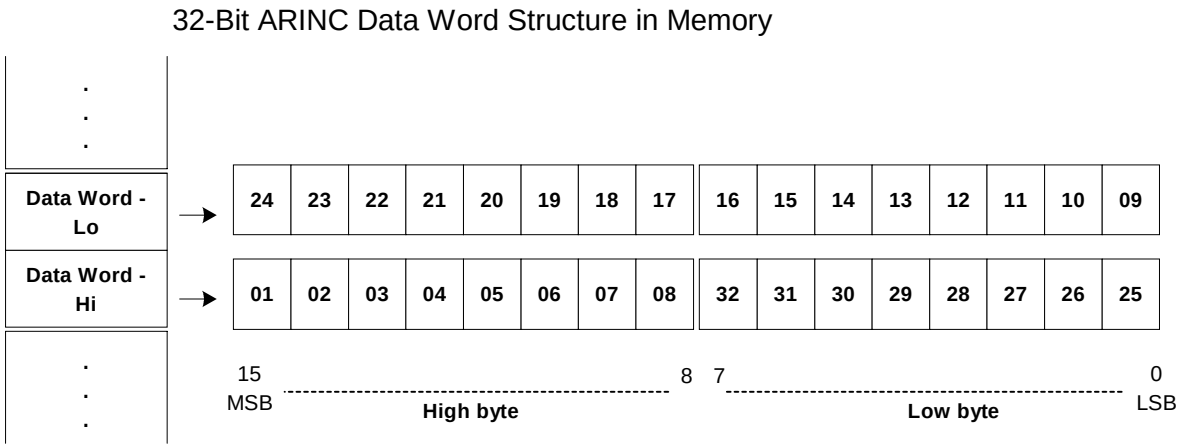


Figure 2-14 32-Bit Transmit Data Words Format

NOTE 1. The numbers contained within the words in Figure 2-14, represent the ARINC bit locations within the 32-bit word.

2. The ARINC word bits are transmitted in the following order:

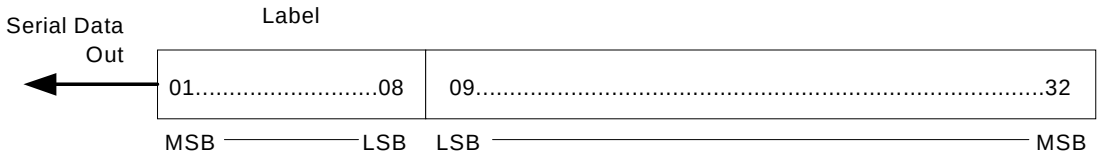


Figure 2-15 32-bit Word Transmit Order Bit

3. Bits 09 through 32 are ordered from LSB to MSB (as opposed to the Label field that is organized from MSB to LSB). For this reason, in the Data Block, the Hi-Word is first, followed by the Lo-Word, with the Label and the ARINC field 32 through 25 in the Hi-Word and bits 24 through 09, in the Lo-Word.

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24-Bit ARINC Data Word Structure in the Memory

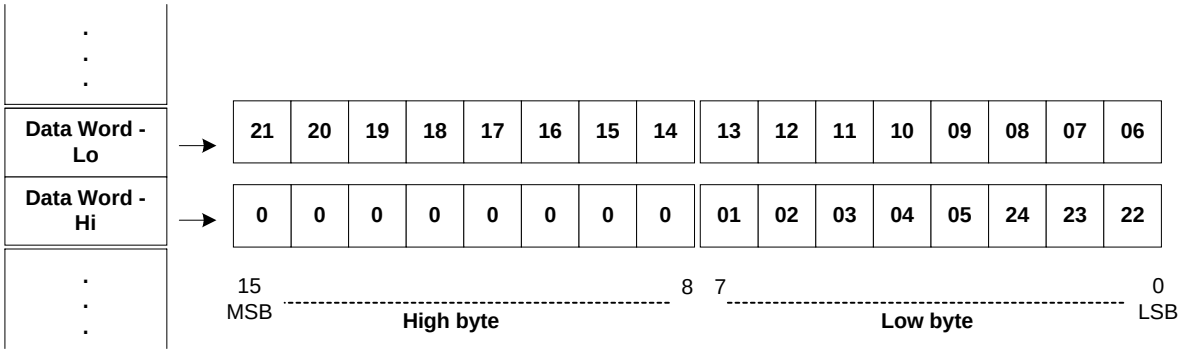


Figure 2-16 24-Bit Transmit Data Word Structure

NOTE 1. The numbers contained within the data word structure in Figure 2-15, represent the ARINC bit location within the 24-bit word.

2. The 24-bit ARINC word is transmitted the following order:

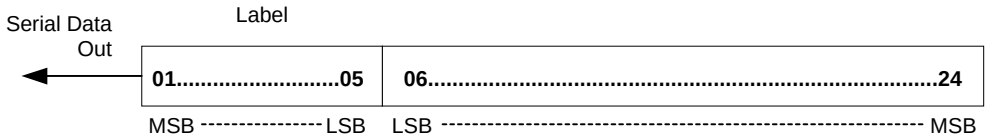


Figure 2-17 24-Bit Word Transmit Order Bit

3. Bits 06 through 24 are ordered from LSB to MSB. For this reason the Data Block is built the way it is.

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2.4 Receive Channel Operation

The user sets up each receive channel's mode of operation by writing to various Control Registers (Global and channel specific). Each receive channel has three basic modes of operation:

Sequential Mode: Stores data in sequential locations within the receive data area

Merge Mode: Siphons all ARINC receive channels data into *one* receive buffer area

Look-Up Table Mode: Allows the user to store words in specific locations of memory according to the Label

In all these modes, the Data Words are stored with a 16-bit Receive Status Word and a 32-bit Time Tag value. In Data Only option the Status and Time Tag are not stored. In Merge Mode, the channel ID information (indicates on which channel the data was received) is contained within the Receive Status Word.

In Receive Channel Operation the board is initialized in a wait loop, looking for a START command from the computer. This command is issued by writing to the Global Start Register (see Global Start Register, page 2-15). The command instructs the board to begin operation on the selected channels.

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2.4.1 Sequential and Merge Modes

Sequential Mode

The Sequential Mode has a software-selectable feature that filters the storage of the specific, user-defined Labels or stores all Labels within a buffer. (See page 2-50) The data buffer's size and location within the memory is programmed via a Start and End pointer. (See Receive Data Start Pointer Register and Receive Data End Pointer Register, page 2-32). Each received ARINC Data Word is tagged with a status Word, indicating the status of the receive Word and a 32-bit Time Tag value.

These five, 16-bit words, make up a single receive data block. Alternatively, the Sequential Mode offers the user the capability of storing only the ARINC data without the Time Tag and Status Words. This global selection affects all receive channels. (See Receive Data Storage Mode Register, page 2-9.) A 16-bit register indicates the number of invalid words received. Interrupts and pollable status registers allow for numerous event recognition and are described in the Channel Control Register section of this manual. (See Channel *x* Control Registers, page 2-17).

Merge Mode

The Merge Mode operates in the same manner as the Sequential Mode except that all the receive channels are merged into one Data Buffer area. The Control registers for the Merge Mode are located and defined in the Global Register Sections, see page 2-2. In this mode the Receive Data Blocks are stored in sequential order and each receive Status Word is tagged with a channel ID, indicating the channel on which the data was received. Each data block contains a Time Tag word as in the standard Sequential Mode of operation.

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2.4.1.1 Receive Buffer Storage Sequence

Figure 2-15 illustrates how Receive Data Blocks are stored within the dual-port RAM, while in the Sequential Mode of operation.

The Channel *x* Receive Error Count Register (see page 2-30) is updated with every invalid word, which is stored. The Start and End pointers set up the buffer size. The Receive Data Storage will stop when the end pointer is reached or will wrap around to the beginning of the buffer, depending upon the condition of the Receive Wrap Around bit in the Channel *x* Configuration Register (see page 2-33). The Time Tag resolution is 10 µsec/bit.

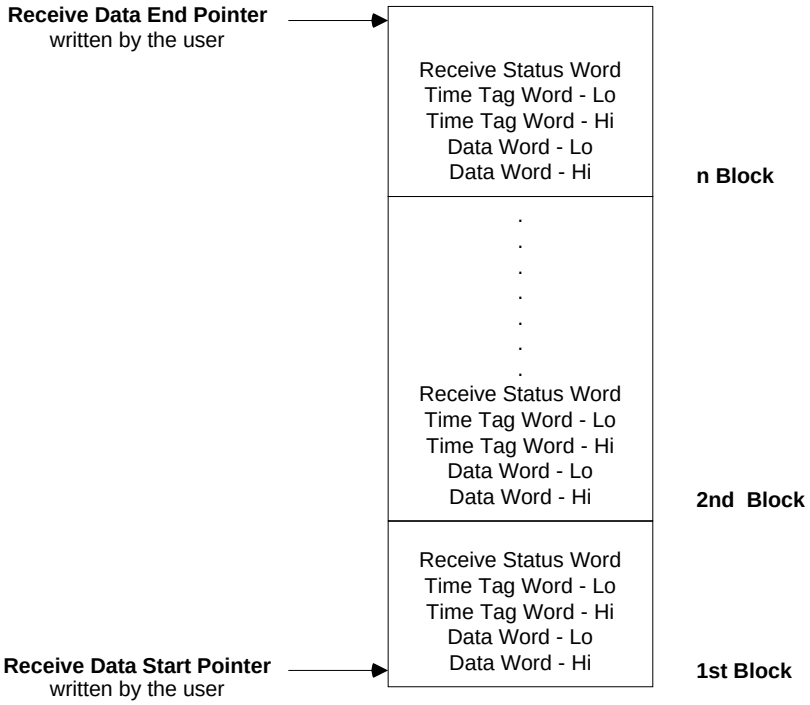


Figure 2-18 Receive Sequential Mode Buffer Structure

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2.4.1.2 Receive Data Word Format

The received ARINC word is stored as two, 16-bit words within the memory (Hi-Word followed by a Lo-Word).

The numbers shown within the two words represent the ARINC bit numbers.

32-Bit ARINC Word Receive Format

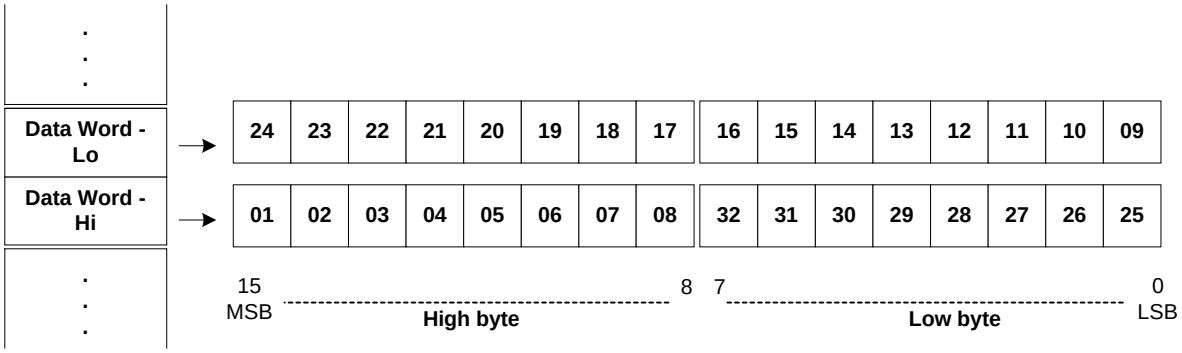


Figure 2-19 32-Bit Receive Data Word Format

NOTE 1. The ARINC word bits are received in the following order:

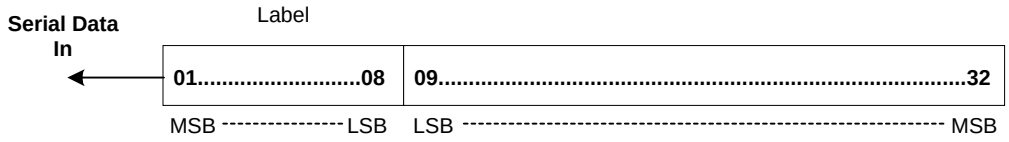


Figure 2-20 32-Bit ARINC Word Order Bit

2. Bits 09 through 32 are ordered from LSB to MSB (as opposed to the Label field which is organized from MSB to LSB). For this reason, in the Data Block the Hi-word is first, followed by the Lo-word, with the Label and the ARINC field 32 through 25 in the Hi-word, and bits 24 through 09, in the Lo-word.

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24-Bit ARINC Word Receive Format

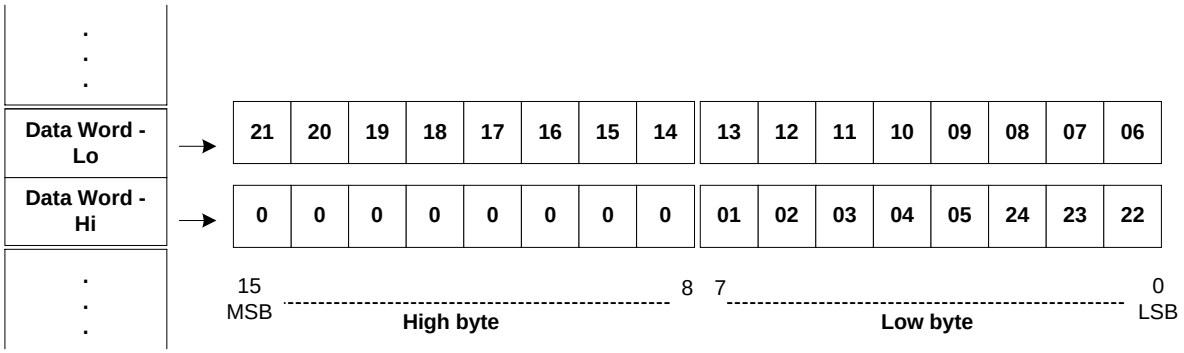


Figure 2-21 32-Bit Receive Data Words Format

NOTE 1. The ARINC word bits are received in the following order:

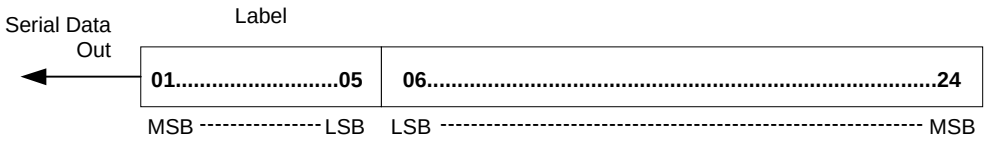


Figure 2-22 24-Bit ARINC Word Order Bit

2. Bits 06 through 24 are order from LSB to MSB. For this reason the Data Block is built the way it is.

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2.4.1.3 Time Tag Word Format

The Time Tag is a 32-bit word made up of two 16-bit words Time Tag-Hi and Time Tag-Lo.

The resolution of the Time Tag is 10 µsec/bit.

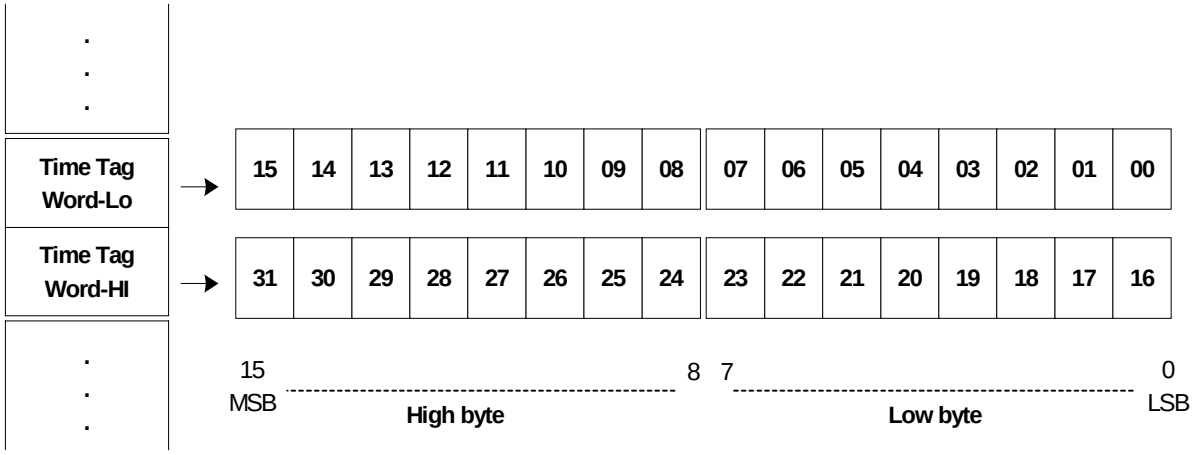


Figure 2-23 ARINC Time Tag Word Format

NOTE There is latency between the time a word is received on the bus and the time that word is recorded in dual-port RAM. The number of channels and data rate of these channels affects this latency. The Time Tag reflects the time the word is written to dual-port RAM rather than the time the word is received over the bus. In no event will this latency exceed a single Hi-speed Word time of 360 microseconds.

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2.4.1.4 Receive Sequential Mode Status Word

Bit	Bit Name	Description
12-15	Reserved	
08-11	Merge Channel ID Code ***(Merge Mode Only)***	0000 – Data received over Channel 0 0001 – Data received over Channel 1 0010 – Data received over Channel 2 0011 – Data received over Channel 3 0100 – Data received over Channel 4 0101 – Data received over Channel 5 0110 – Data received over Channel 6 0111 – Data received over Channel 7 1000 – Data received over Channel 8 1001 – Data received over Channel 9 **Note**: Channel ID Code: bit 8 = LSB Channel ID Code: bit 11 = MSB
07	Valid Word	1 = The Received ARINC word was valid in all respects (Global bit). 0 = Not a valid word
06	Reserved	
05	Gap [Sync] Time Error	1 = Gap [Sync] Time Error occurred between words (less than a 4 bit times between words for ARINC 429/575/582 2-wire channels and less than 1 bit time between words for ARINC 561/568/582 6-wire channels.) 0 = No error
04	Invalid Coding Error	1 = Bit level coding error was detected in the ARINC word 0 = No error
03	Parity Error	1 = A parity error was detected in the ARINC word. 0 = No error
02	Lo Bit Count / Invalid Word Error	1 = A Lo Bit Count or a Null bit Error was detected in the ARINC word. 0 = No error
01	Hi Bit Count Error	1 = A Hi Bit Count or a Null bit Error was detected in the ARINC word. 0 = No error
00	Word Received	1 = Data is in memory. This bit is cleared while data is in the process of being updated. 0 = No received word

Receive Sequential Mode Status Word

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2.4.1.5 Receive Sequential Mode Filter Table Diagram

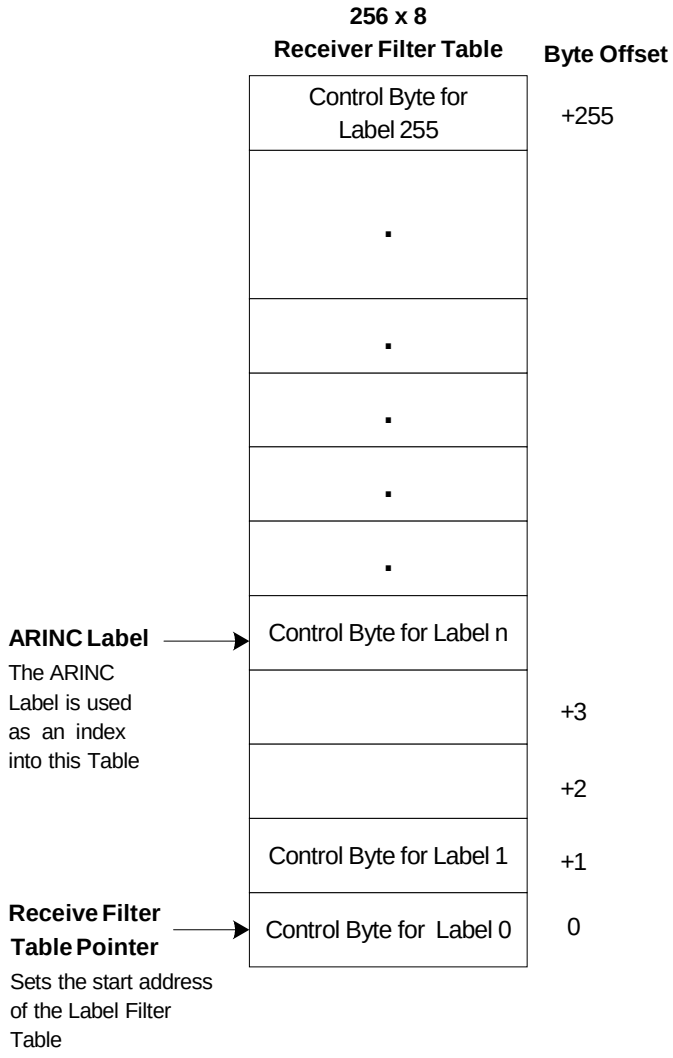


Figure 2-24 Receive Sequential Mode Filter Table Diagram

Bit	Description
02-07	Reserved
01	1 = Interrupt 0 = Don't Interrupt
00	1 = Store Word 0 = Don't Store

Label Control Byte Structure (WRITE)

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2.4.2 Look-Up Table Mode Operation

In Look-up Table mode, the word's LABEL is used by the board as an offset to a 256-word Look-up Table. The Table is programmed by the user with address pointers as to where to write the Receive Data Block. Each Block contains a:

- 32-bit ARINC word,
- 32-bit Time Tag
- Error Count Word
- Status Word

The 256-word Table can be placed anywhere within the memory via a user-programmable Receive Look-up Table Start Address Register.

The user has the ability to monitor the operational status of each channel and to be interrupted on various events. In addition, there exist pollable registers that can be used with or instead of interrupt processing.

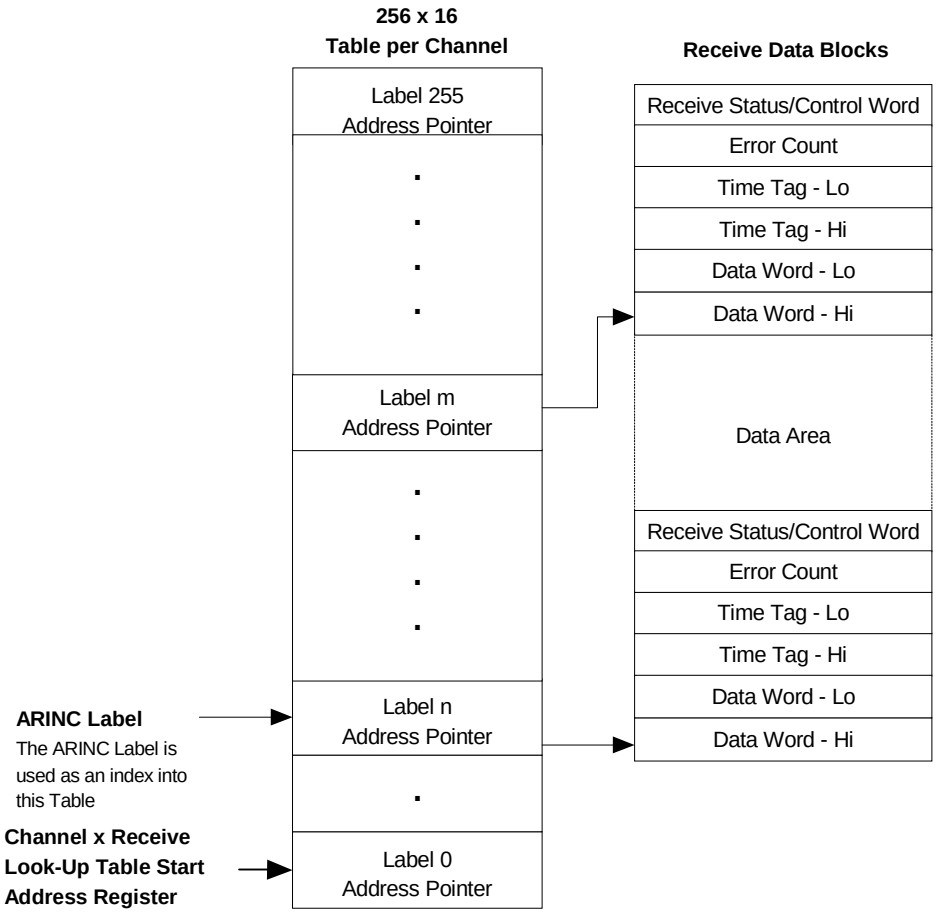


Figure 2-25 Receive Look-Up Table Structure

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2.4.2.1 Receive Data Block Description

The Receive Data Block components are:

2.4.2.1.1 Data Word

The ARINC Data Word is stored as two 16-bit with the same format as described in section 2.4.1.2.

2.4.2.1.2 Time Tag Word

The Time Tag Word is stored a two 16-bit with the format described in section 2.4.1.3.

2.4.2.1.3 Error Count Word

The Error Count Word indicates the number of error words received on the particular label.

2.4.2.1.4 Look-Up Table – Receive Status / Control Word

Control Byte

Bit	Bit Name	Description
15	Enable Label Interrupt	Enables the 'interrupt on Label received' capability. This bit is used in conjunction with the Channel *x* Interrupt / Trigger Condition Register
08-14	Reserved	Set to 0

Status Byte

07	Valid Word	1 = The Received ARINC word was valid in all respects (Global bit). 0 = Not a valid word
06	Reserved	
05	Gap [Sync] Time Error	1 = Gap [Sync] Time Error occurred between words (less than a 4 bit times between words for ARINC 429/575/582 2-wire channels and less than 1 bit time between words for ARINC 561/568/582 6-wire channels). 0 = No error
04	Invalid Coding Error	1 = Bit level coding error was detected in the ARINC word 0 = No error
03	Parity Error	1 = A parity error was detected in the ARINC word. 0 = No error
02	Lo Bit Count / Invalid Word Error	1 = A Lo Bit Count or a Null bit Error was detected in the ARINC word. 0 = No error
01	Hi Bit Count Error	1 = A Hi Bit Count or a Null bit Error was detected in the ARINC word. 0 = No error
00	Word Received	1 = Data is in memory. This bit is cleared while data is in the process of being updated. 0 = No received word

Look-Up Table: Receive Status / Control Word

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3 RS-232/422/423/485 Channels

Chapter 3 describes EXC-3000PC MAGICard operation for RS-232/422/423/485 channels. The topics covered in this chapter are:

3.1 RS Global Control Registers
- Map page 3-2
- Definitions page 3-3

3.2 RS Channel Control Registers
- Maps page 3-10
- Definitions page 3-20

3.3 Baud Rate Limitations page 3-28

3.4 RS Transmit Channel Operation page 3-29
- Transmit Instruction Stack page 3-29
- Transmit Data Block Format page 3-31

3.5 RS Receive Channel Operation page 3-32
- Receive Buffer Structure page 3-33

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3.1. RS Global Control Registers

Global registers can be set at any time.

Reserved	7F00-7F38 H		
RS-232/422/423/485 Operating Mode	7F3A H		
Reserved	7F3C-7F56 H		
Receive Data Storage Mode	7F58 H		
Channel 0 Configuration Status	7F5A H		
Channel 1 Configuration Status	7F5C H		
Channel 2 Configuration Status	7F5E H		
Channel 3 Configuration Status	7F60 H	Board ID (Handshake)	7F76 H
Channel 4 Configuration Status	7F62 H	Host Ready (Handshake)	7F78 H
Channel 5 Configuration Status	7F64 H	Start/Stop	7F7A H
Channel 6 Configuration Status	7F66 H	Reset Time Tag	7F7C H
Channel 7 Configuration Status	7F68 H	Reserved	7F7E H
Channel 8 Configuration Status	7F6A H	Interrupt Request Level Select	7F80 H
Channel 9 Configuration Status	7F6C H	Reset Interrupt	7F82 H
Reserved	7F6E H	Software Reset	7F84 H
Interrupt Status	7F70 H	Reserved	7F86-7FFF H
Firmware Revision	7F72 H		
Board Status	7F74 H		

Figure 3-1 RS Global Control Registers Map

The registers are described in the order they appear on the map.

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Global Control Registers Definitions

3.1.1 RS-232/422/423/485 Operating Mode Register

Address: 7F3A (H)

This register is used to select the operation mode for all RS-232/422/423/485 channels.

Bit	Description
01-15	Reserved - set to 0
00	0 = Regular Mode: Supports operation with Hi-speed ARINC channels BUT at high baud rates, data is lost. 1 = Fast Mode: • Supports operation at high baud rates BUT high speed ARINC receives modules may loose data. • Received bytes are stored without Status and Time Tag.

RS-232/422/423/485 Operating Mode Register

For more information about these modes, see Baud Rate Limitations, see page 3-28.

3.1.2 Receive Data Storage Mode Register

Address: 7F58 (H)

The Receive Data Storage Mode register is used to select the Receive Data Storage Mode for all RS-232/422/423/485 channels. Data bytes can be stored with Time Tag and Status Byte appended to the Data block or without these additional bytes.

Bit	Description
01-15	0
00	0 = Standard Mode: appends both time Tag and Status byte to each Data byte stored in memory 1 = Store Only Data

Receive Data Storage Mode Register

NOTE 1. There is no Merge Mode for RS type channels.

2. A change in this register is noted by the firmware only after the Start/Stop register contains a value of 0 for at least 1 msec.

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3.1.3 Channel *x* Configuration Status Register

Address: 7F5A-7F6C (H)

This register indicates to the host the type of channel configured in each channel socket on the board.

Bit	Description					
05-15	Reserved – set to 0					
00-04	Configuration Status Code					
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Configuration Status Code
	0	0	0	0	0	Undefined Channel
	0	0	0	0	1	ARINC-429 Receive Channel
	0	0	0	1	0	ARINC-429 Transmit Channel
	0	0	0	1	1	ARINC-561 Receive Channel
	0	0	1	0	0	ARINC-561 Transmit Channel
	0	0	1	0	1	ARINC-568 Receive Channel
	0	0	1	1	0	ARINC-568 Transmit Channel
	0	0	1	1	1	ARINC-575 Receive Channel
	0	1	0	0	0	ARINC-575 Transmit Channel
	0	1	0	0	1	ARINC-582 2-Wire Receive Channel
	0	1	0	1	0	ARINC-582 2-Wire Transmit Channel
	0	1	0	1	1	ARINC-582 6-Wire Receive Channel
	0	1	1	0	0	ARINC-582 6-Wire Transmit Channel
	0	1	1	0	1	ARINC-575 24-Bit Receive Channel
	0	1	1	1	0	ARINC-575 24-Bit Transmit Channel
	0	1	1	1	1	Free code for future channels
	1	0	0	0	0	RS-232 Channel
	1	0	0	0	1	RS-422 Channel
	1	0	0	1	0	RS-485 Channel
	1	0	0	1	1	RS-423 Channel
	1	0	1	0	0	Free code for future channels
	1	0	1	0	1	Free code for future channels
	1	0	1	1	0	Free code for future channels
	1	0	1	1	1	Free code for future channels
	1	1	0	0	0	Free code for future channels
	1	1	0	0	1	Free code for future channels
	1	1	0	1	0	Free code for future channels
	1	1	0	1	1	Free code for future channels
	1	1	1	0	0	Free code for future channels
	1	1	1	0	1	reserved
	1	1	1	1	0	reserved
	1	1	1	1	1	reserved

Channel *x* Configuration Status Register

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3.1.4 Interrupt Status Register

Address: 7F70 (H)

The Interrupt Status Register indicates which channel issued the interrupt: 1 = Active. The user, only, resets the status bit or bits.

Bit	Bit Name
10-15	Reserved – set to 0
09	Channel 9 Interrupt Status Bit
08	Channel 8 Interrupt Status Bit
07	Channel 7 Interrupt Status Bit
06	Channel 6 Interrupt Status Bit
05	Channel 5 Interrupt Status Bit
04	Channel 4 Interrupt Status Bit
03	Channel 3 Interrupt Status Bit
02	Channel 2 Interrupt Status Bit
01	Channel 1 Interrupt Status Bit
00	Channel 0 Interrupt Status Bit

Interrupt Status Register

3.1.5 Firmware Revision Register

Address: 7F72 (H)

The Firmware Revision Register indicates the revision level of the firmware. For example: 0114 (H) = Rev 1.14.

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3.1.6 Board Status Register

Address: 7F74 (H)

The Board Status Register indicates the result of the power on, Self-test of the board.

Bit	Bit Name	Description
13-15	Reserved	Set to 0
12	Reserved	
11	Host Ready Timeout	
10	Memory Status Bit	1 = Memory OK 0 = Memory failed
09	Channel 9 Status bit	1 = Self-test OK 0 = Self-test failed
08	Channel 8 Status bit	1 = Self-test OK 0 = Self-test failed
07	Channel 7 Status bit	1 = Self-test OK 0 = Self-test failed
06	Channel 6 Status bit	1 = Self-test OK 0 = Self-test failed
05	Channel 5 Status bit	1 = Self-test OK 0 = Self-test failed
04	Channel 4 Status bit	1 = Self-test OK 0 = Self-test failed
03	Channel 3 Status bit	1 = Self-test OK 0 = Self-test failed
02	Channel 2 Status bit	1 = Self-test OK 0 = Self-test failed
01	Channel 1 Status bit	1 = Self-test OK 0 = Self-test failed
00	Channel 0 Status bit	1 = Self-test OK 0 = Self-test failed

Board Status Register

NOTE

1. The 'Self-test Fail' is set when the channel Self-test fails or when the channel is not present on the board.
2. The board continues to operate (wait for a Host Ready, etc.) on condition of channel Self-test failures *but* will not continue to operate on condition of a memory failure.

3.1.7 Board ID (Handshake) Register

Address: 7F76 (H)

Handshake from the board indicating that the board has completed its initialization sequence and that the board is ready to be accessed by the host. The board writes the value 3000 (H) into this register when ready. (See Host Ready (Handshake) Register, page 3-7.)

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3.1.8 Host Ready (Handshake) Register

Address: 7F78 (H)

After power-up or a software reset, the user must write a 0 to the Board Ready Register. Then wait for the contents of the Host Ready Register to be 0, and then write the value 1234 (H) to it. This indicates to the board that the host system has finished its power-up sequence (BIOS memory tests, etc.) and is ready to communicate with the board. The board then executes its initialization procedure. When the procedures are completed, a value of 3000 (H) is written to the Board Ready Register.

If after a timeout period (approximately 45 seconds after power-up) the host does not write this value to the register, the board sets the Host Ready Timeout bit within the Board Status Register. (See Board Status Register, page 3-6.)

3.1.9 Start / Stop Register

Address: 7F7A (H)

The user can start one or more channels at the same time - wait a minimum of 500 µsec. between writes to this register.

Bit	Bit Name	Description
10-15	Reserved	Set to 0
09	Channel 9 Start Bit	1 = Start 0 = Stop
08	Channel 8 Start Bit	1 = Start 0 = Stop
07	Channel 7 Start Bit	1 = Start 0 = Stop
06	Channel 6 Start Bit	1 = Start 0 = Stop
05	Channel 5 Start Bit	1 = Start 0 = Stop
04	Channel 4 Start Bit	1 = Start 0 = Stop
03	Channel 3 Start Bit	1 = Start 0 = Stop
02	Channel 2 Start Bit	1 = Start 0 = Stop
01	Channel 1 Start Bit	1 = Start 0 = Stop
00	Channel 0 Start Bit	1 = Start 0 = Stop

NOTE A change in a channel's Configuration Register or in the Receive Data Storage Mode Register is acted upon by the firmware, only after the Start/Stop Register contains a value of 0 for at least 1 msec.

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3.1.10 Reset Time Tag Register

Address: 7F7C (H)

Writing any non-0 value to the Reset Time Tag Register causes the Time Tag to be reset to 0. Upon completion of the Time Tag reset operation, this register is cleared by the board.

3.1.11 Interrupt Request Level Select Register

Address: 7F80 (H) WRITE ONLY

The Interrupt Request Level Select Register is used to select the interrupt request level to be used by the board within the PC/AT computer. The high byte is ignored by the board. The content of the low byte is shown below.

Bit	Description				
04-07	Piggyback adapter board interrupt request level				
00-03	Bit 3	Bit 2	Bit 1	Bit 0	
	0	0	0	0	No interrupt selected
	0	0	0	1	No interrupt selected
	0	0	1	0	Interrupt level 2
	0	0	1	1	Interrupt level 3
	0	1	0	0	Interrupt level 4
	0	1	0	1	Interrupt level 5
	0	1	1	0	Interrupt level 6
	0	1	1	1	Interrupt level 7
	1	0	0	0	No interrupt selected
	1	0	0	1	No interrupt selected
	1	0	1	0	Interrupt level 10
	1	0	1	1	Interrupt level 11
	1	1	0	0	Interrupt level 12
	1	1	0	1	No interrupt selected
	1	1	1	0	Interrupt level 14
	1	1	1	1	Interrupt level 15

Interrupt Level Select Request Register

3.1.12 Reset Interrupt Register

Address: 7F82 (H) WRITE ONLY

Writing to the Reset Interrupt Register resets the board's interrupt. The least significant bit within the Data Word (bit 00) must be a logic 0. Write to this register immediately following the entry into the host interrupt service function.

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3.1.13 Software Reset Register

Address: 7F84 (H) WRITE ONLY

Writing a 0 to the Software Reset Register resets the board. Following a reset, the user must wait for a value of 0 to appear in the Host Ready Register, then write 1234 (H) to the register. The board then executes a Self-test, both memory and channels, clears all the dual-port RAM, resets the board's interrupts and updates the Board Status Register. The board then indicates that it is ready by writing a value of 3000 (H) to the Board Ready Register.

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3.2 RS Channel Control Registers

3.2.1 Channel 0 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 0 Start Receive (W)	7D20 H
Channel 0 Start Transmit (W)	7D22 H
Reserved	7D24-7D26 H
Channel 0 Status Register (R)	7D28 H
Channel 0 Interrupt / Trigger Conditions (W)	7D2A H
Reserved	7D2C H
Channel 0 Transmit Loop Counter (W)	7D2E H
Channel 0 Transmit Instruction Counter (W)	7D30 H
Channel 0 Transmit Instruction Stack Pointer (W)	7D32 H
Channel 0 Start Receive Byte Trigger (W)	7D34 H
Channel 0 Receive Error Count (R/W)	7D36 H
Channel 0 Receive Interval Counter Trigger (W)	7D38 H
Reserved	7D3A H
Channel 0 Receive Data Byte Counter Trigger (W)	7D3C H
Channel 0 Receive Buffer Wraparound (W)	7D3E H
Channel 0 Receive Data Byte Count (R)	7D40 H
Reserved	7D42-7D44 H
Channel 0 Receive Data Current Pointer (R)	7D46 H
Channel 0 Receive Data End Pointer (W)	7D48 H
Channel 0 Receive Data Start Pointer (W)	7D4A H
Channel 0 Baud Rate Generator (W)	7D4C H
Channel 0 Configuration (W)	7D4E H

Figure 3-2 Channel 0 Control Register Block Map

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3.2.2 Channel 1 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 1 Start Receive (W)	7D50 H
Channel 1 Start Transmit (W)	7D52 H
Reserved	7D54-7D56 H
Channel 1 Status Register (R)	7D58 H
Channel 1 Interrupt / Trigger Conditions (W)	7D5A H
Reserved	7D5C H
Channel 1 Transmit Loop Counter (W)	7D5E H
Channel 1 Transmit Instruction Counter (W)	7D60 H
Channel 1 Transmit Instruction Stack Pointer (W)	7D62 H
Channel 1 Start Receive Byte Trigger (W)	7D64 H
Channel 1 Receive Error Count (R/W)	7D66 H
Channel 1 Receive Interval Counter Trigger (W)	7D68 H
Reserved	7D6A H
Channel 1 Receive Data Byte Counter Trigger (W)	7D6C H
Channel 1 Receive Buffer Wraparound (W)	7D6E H
Channel 1 Receive Data Byte Count (R)	7D70 H
Reserved	7D72-7D74 H
Channel 1 Receive Data Current Pointer (R)	7D76 H
Channel 1 Receive Data End Pointer (W)	7D78 H
Channel 1 Receive Data Start Pointer (W)	7D7A H
Channel 1 Baud Rate Generator (W)	7D7C H
Channel 1 Configuration (W)	7D7E H

Figure 3-3 Channel 1 Control Register Block Map

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3.2.3 Channel 2 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 2 Start Receive (W)	7D80 H
Channel 2 Start Transmit (W)	7D82 H
Reserved	7D84-7D86 H
Channel 2 Status Register (R)	7D88 H
Channel 2 Interrupt / Trigger Conditions (W)	7D8A H
Reserved	7D8C H
Channel 2 Transmit Loop Counter (W)	7D8E H
Channel 2 Transmit Instruction Counter (W)	7D90 H
Channel 2 Transmit Instruction Stack Pointer (W)	7D92 H
Channel 2 Start Receive Byte Trigger (W)	7D94 H
Channel 2 Receive Error Count (R/W)	7D96 H
Channel 2 Receive Interval Counter Trigger (W)	7D98 H
Reserved	7D9A H
Channel 2 Receive Data Byte Counter Trigger (W)	7D9C H
Channel 2 Receive Buffer Wraparound (W)	7D9E H
Channel 2 Receive Data Byte Count (R)	7DA0 H
Reserved	7DA2-7DA4 H
Channel 2 Receive Data Current Pointer (R)	7DA6 H
Channel 2 Receive Data End Pointer (W)	7DA8 H
Channel 2 Receive Data Start Pointer (W)	7DAA H
Channel 2 Baud Rate Generator (W)	7DAC H
Channel 2 Configuration (W)	7DAE H

Figure 3-4 Channel 2 Control Register Block Map

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3.2.4 Channel 3 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 3 Start Receive (W)	7DB0 H
Channel 3 Start Transmit (W)	7DB2 H
Reserved	7DB4-7DB6 H
Channel 3 Status Register (R)	7DB8 H
Channel 3 Interrupt / Trigger Conditions (W)	7DBA H
Reserved	7DBC H
Channel 3 Transmit Loop Counter (W)	7DBE H
Channel 3 Transmit Instruction Counter (W)	7DC0 H
Channel 3 Transmit Instruction Stack Pointer (W)	7DC2 H
Channel 3 Start Receive Byte Trigger (W)	7DC4 H
Channel 3 Receive Error Count (R/W)	7DC6 H
Channel 3 Receive Interval Count Trigger (W)	7DC8 H
Reserved	7DCA H
Channel 3 Receive Data Byte Counter Trigger (W)	7DCC H
Channel 3 Receive Buffer Wraparound (W)	7DCE H
Channel 3 Receive Data Byte Counter (R)	7DD0 H
Reserved	7DD2-7DD4 H
Channel 3 Receive Data Current Pointer (R)	7DD6 H
Channel 3 Receive Data End Pointer (W)	7DD8 H
Channel 3 Receive Data Start Pointer (W)	7DDA H
Channel 3 Baud Rate Generator (W)	7DDC H
Channel 3 Configuration (W)	7DDE H

Figure 3-5 Channel 3 Control Register Block Map

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3.2.5 Channel 4 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 4 Start Receive (W)	7DE0 H
Channel 4 Start Transmit (W)	7DE2 H
Reserved	7DE4-7DE6 H
Channel 4 Status Register (R)	7DE8 H
Channel 4 Interrupt /Trigger Conditions (W)	7DEA H
Reserved	7DEC H
Channel 4 Transmit Loop Counter (W)	7DEE H
Channel 4 Transmit Instruction Counter (W)	7DF0 H
Channel 4 Transmit Instruction Stack Pointer (W)	7DF2 H
Channel 4 Start Receive Byte Trigger (W)	7DF4 H
Channel 4 Receive Error Count (R/W)	7DF6 H
Channel 4 Receive Interval Count Trigger (W)	7DF8 H
Reserved	7DFA H
Channel 4 Receive Data Byte Counter Trigger (W)	7DFC H
Channel 4 Receive Buffer Wraparound (W)	7DFE H
Channel 4 Receive Data Byte Counter (R)	7E00 H
Reserved	7E02-7E04 H
Channel 4 Receive Data Current Pointer (R)	7E06 H
Channel 4 Receive Data End Pointer (W)	7E08 H
Channel 4 Receive Data Start Pointer (W)	7E0A H
Channel 4 Baud Rate Generator (W)	7E0C H
Channel 4 Configuration (W)	7E0E H

Figure 3-6 Channel 4 Control Register Block Map

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3.2.6 Channel 5 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 5 Start Receive (W)	7E10 H
Channel 5 Start Transmit (W)	7E12H
Reserved	7E14-7E16 H
Channel 5 Status Register (R)	7E18 H
Channel 5 Interrupt / Trigger Conditions (W)	7E1A H
Reserved	7E1C H
Channel 5 Transmit Loop Counter (W)	7E1E H
Channel 5 Transmit Instruction Counter (W)	7E20 H
Channel 5 Transmit Instruction Stack Pointer (W)	7E22 H
Channel 5 Start Receive Byte Trigger (W)	7E24 H
Channel 5 Receive Error Count (R/W)	7E26 H
Channel 5 Receive Interval Counter Trigger (W)	7E28 H
Reserved	7E2A H
Channel 5 Receive Data Byte Counter Trigger (W)	7E2C H
Channel 5 Receive Buffer Wraparound (W)	7E2E H
Channel 5 Receive Data Byte Count (R)	7E30 H
Reserved	7E32-7E34 H
Channel 5 Receive Data Current Pointer (R)	7E36 H
Channel 5 Receive Data End Pointer (W)	7E38 H
Channel 5 Receive Data Start Pointer (W)	7E3A H
Channel 5 Baud Rate Generator (W)	7E3C H
Channel 5 Configuration (W)	7E3E H

Figure 3-7 Channel 5 Control Register Block Map

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3.2.7 Channel 6 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 6 Start Receive (W)	7E40 H
Channel 6 Start Transmit (W)	7E42 H
Reserved	7E44-7E46 H
Channel 6 Status Register (R)	7E48 H
Channel 6 Interrupt / Trigger Conditions (W)	7E4A H
Reserved	7E4C H
Channel 6 Transmit Loop Counter (W)	7E4E H
Channel 6 Transmit Instruction Counter (W)	7E50 H
Channel 6 Transmit Instruction Stack Pointer (W)	7E52 H
Channel 6 Start Receive Byte Trigger (W)	7E54 H
Channel 6 Receive Error Count (R/W)	7E56 H
Channel 6 Receive Interval Counter Trigger (W)	7E58 H
Reserved	7E5A H
Channel 6 Receive Data Byte Counter Trigger (W)	7E5C H
Channel 6 Receive Buffer Wraparound (W)	7E5E H
Channel 6 Receive Data Byte Count (R)	7E60 H
Reserved	7E62-7E64 H
Channel 6 Receive Data Current Pointer (R)	7E66 H
Channel 6 Receive Data End Pointer (W)	7E68 H
Channel 6 Receive Data Start Pointer (W)	7E6A H
Channel 6 Baud Rate Generator (W)	7E6C H
Channel 6 Configuration (W)	7E6E H

Figure 3-8 Channel 6 Control Register Block Map

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3.2.8 Channel 7 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 7 Start Receive (W)	7E70 H
Channel 7 Start Transmit (W)	7E72 H
Reserved	7E74-7E46 H
Channel 7 Status Register (R)	7E78 H
Channel 7 Interrupt / Trigger Conditions (W)	7E7A H
Reserved	7E7C H
Channel 7 Transmit Loop Counter (W)	7E7E H
Channel 7 Transmit Instruction Counter (W)	7E80 H
Channel 7 Transmit Instruction Stack Pointer (W)	7E82 H
Channel 7 Start Receive Byte Trigger (W)	7E84 H
Channel 7 Receive Error Count (R) / (W)	7E86 H
Channel 7 Receive Interval Counter Trigger (W)	7E88 H
Reserved	7E8A H
Channel 7 Receive Data Byte Counter Trigger (W)	7E8C H
Channel 7 Receive Buffer Wraparound (W)	7E8E H
Channel 7 Receive Data Byte Count (R)	7E90 H
Reserved	7E92-7E94 H
Channel 7 Receive Data Current Pointer (R)	7E96 H
Channel 7 Receive Data End Pointer (W)	7E98 H
Channel 7 Receive Data Start Pointer (W)	7E9A H
Channel 7 Baud Rate Generator (W)	7E9C H
Channel 7 Configuration (W)	7E9E H

Figure 3-9 Channel 7 Control Register Block Map

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3.2.9 Channel 8 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 8 Start Receive (W)	7EA0 H
Channel 8 Start Transmit (W)	7EA2 H
Reserved	7EA4-7EA6 H
Channel 8 Status Register (R)	7EA8 H
Channel 8 Interrupt / Trigger Conditions (W)	7EAA H
Reserved	7EAC H
Channel 8 Transmit Loop Counter (W)	7EAE H
Channel 8 Transmit Instruction Counter (W)	7EB0 H
Channel 8 Transmit Instruction Stack Pointer (W)	7EB2 H
Channel 8 Start Receive Byte Trigger (W)	7EB4 H
Channel 8 Receive Error Count (R/W)	7EB6 H
Channel 8 Receive Interval Counter Trigger (W)	7EB8 H
Reserved	7EBA H
Channel 8 Receive Data Byte Counter Trigger (W)	7EBC H
Channel 8 Receive Buffer Wraparound (W)	7EBE H
Channel 8 Receive Data Byte Count (R)	7EC0 H
Reserved	7EC2-7EC4 H
Channel 8 Receive Data Current Pointer (R)	7EC6 H
Channel 8 Receive Data End Pointer (W)	7EC8 H
Channel 8 Receive Data Start Pointer (W)	7ECA H
Channel 8 Baud Rate Generator (W)	7ECC H
Channel 8 Configuration (W)	7ECE H

Figure 3-10 Channel 8 Control Register Block Map

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3.2.10 Channel 9 Control Register Block Map

The registers are marked (R) read only or (W) write only – only the Receive Error Count Register is both (R) and (W).

Channel 9 Start Receive (W)	7ED0 H
Channel 9 Start Transmit (W)	7ED2 H
Reserved	7ED4-7ED6 H
Channel 9 Status Register (R)	7ED8 H
Channel 9 Interrupt / Trigger Conditions (W)	7EDA H
Reserved	7EDC H
Channel 9 Transmit Loop Counter (W)	7EDE H
Channel 9 Transmit Instruction Counter (W)	7EE0 H
Channel 9 Transmit Instruction Stack Pointer (W)	7EE2 H
Channel 9 Start Receive Byte Trigger (W)	7EE4 H
Channel 9 Receive Error Count (R/W)	7EE6 H
Channel 9 Receive Interval Counter Trigger (W)	7EE8 H
Reserved	7EEA H
Channel 9 Receive Data Byte Counter Trigger (W)	7EEC H
Channel 9 Receive Buffer Wraparound (W)	7EEE H
Channel 9 Receive Data Byte Count (R)	7EF0 H
Reserved	7EF2-7EF4 H
Channel 9 Receive Data Current Pointer (R)	7EF6 H
Channel 9 Receive Data End Pointer (W)	7EF8 H
Channel 9 Receive Data Start Pointer (W)	7EFA H
Channel 9 Baud Rate Generator (W)	7EFC H
Channel 9 Configuration (W)	7EFE H

Figure 3-11 Channel 9 Control Register Block Map

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Channel Control Registers Definitions

3.2.11 Channel *x* Start Receive Register **WRITE**

When the channel is enabled via the Global Start Register, the Channel *x* Start Receive Register starts or stops the receive operation.

Bit	Description
01-15	Reserved – set to 0
00	1 = Initiates receive according to the receive parameters which were previously set up. 0 = Terminates the receive operation but allows transmission to continue. The register is set to 0, when the condition 'Stopped on Buffer Full' is met.

Channel x Start Receive Register

NOTE While the channel is active, the user can:

- Set this register to 0
- Update the receive parameters
- Restore the register to 1.

3.2.12 Channel *x* Start Transmit Register **WRITE**

When the channel is enabled via the Global Start Register, the Channel *x* Start Transmit Register is used to start or stop the channel's transmit operation.

Bit	Description
01-15	Reserved – set to 0
00	1 = Initiates transmission according to the transmit instruction block data that was previously set up. 0 = Terminates the transmission but allows the receive operation to continue. The register is set to 0, when the requested transmit operation is completed.

Channel x Start Transmit Register

NOTE While the channel is active, the user can:

- Set this register to 0
- Update the transmit Command Block and Data
- Restore the register to 1.

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3.2.13 Channel *x* Status Register **READ**

The Channel *x* Status Register indicates the operational status of the channel. This register can be used to poll the conditions status of the channel or it can be used with interrupts. When used in conjunction with interrupts, the register indicates the condition or conditions, which caused the interrupt.

A logic 1 indicates an active bit. The user must reset status bits, by writing a 0 to this register.

Bit	Description - Interrupt Condition
07-15	Reserved
06	Receive - Stopped on Buffer Full
05	Receive - Error Received
04	Receive - Word Count Trigger
03	Receive - Interval Count Trigger
02	Reserved
01	Transmit – End of Frame
00	Transmit – End of Block

Channel *x* Status Register

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3.2.14 Channel *x* Interrupt / Trigger Condition Register WRITE

The Channel *x* Interrupt /Trigger Condition register sets the Interrupt and Trigger condition or conditions of the channel. The trigger conditions set a pulse on the External Trigger Connector J1.

Trigger Condition Bits 08-15

Bit	Bit Name
15	Reserved
14	Receive – Stopped on Buffer Full
13	Receive – Error Received
12	Receive – Data Byte Count Trigger
11	Receive – Interval Count Trigger
10	reserved
09	Transmit – End of Frame
08	Transmit – End of Block

Interrupt Conditions Bits 00-07

Bit	Bit Name
07	Reserved
06	Receive – Stopped on Buffer Full
05	Receive – Error Received
04	Receive – Data Byte Count Trigger
03	Reserved
02	Receive – Label Received
01	Transmit – End of Frame
00	Transmit – End of Block

Channel *x* Interrupt / Trigger Condition Register

NOTE 1. To activate the Receive – Interval Count Trigger interrupt or trigger, the Channel *x* Receive Interval Counter Trigger Register must also be set.

2. To activate the Receive – Data Byte Count Trigger interrupt or trigger, the Channel *x* Receive Data Byte Counter Trigger Register must also be set.

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3.2.15 Channel *x* Transmit Loop Counter **WRITE**

The Channel *x* Transmit Loop Counter sets the number of times to execute the transmit instruction blocks (the frame): *N* Times or Continuous Loop. If the continuous value is selected, setting the related channel bit in the Global Start/Stop Register to a 0 can terminate the channel's operation.

Bit	Value	Description
00-15	**0000**	= Continuous
	0001	= One Time
	0002	= Two Times
		•
		•
		•
	FFFF	= 65535 Times

Channel *x* Transmit Loop Counter

3.2.16 Channel *x* Transmit Instruction Counter **WRITE**

The Channel *x* Transmit Instruction Counter sets the number of Transmit Instruction blocks to process.

3.2.17 Channel *x* Transmit Instruction Stack Pointer **WRITE**

The Channel *x* Transmit Instruction Stack Pointer sets the starting address of the Transmit Instruction Stack. The address must be a word boundary within the Transmit Instruction Stack area.

For example: to place the Transmit Instruction stack starting at location 0300 (H), write a 0300 (H) to this register.

3.2.18 Channel *x* Receive Start Byte Trigger Register **WRITE**

The Channel *x* Receive Start Byte Trigger Register is used in conjunction with the Receive Byte Trigger bit within the Channel *x* Configuration Register to enable the reception and storage of data upon receipt of a specific byte.

Bit	Description
08-15	Reserved - Set to 0
00-07	Trigger Byte Value

Channel *x* Receive Start Byte Trigger Register

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3.2.19 Channel *x* Receive Error Count Register **READ/WRITE**

The 16-bit Channel *x* Receive Error Count Register indicates the number of errors received on a particular channel. The register wraps around. The user can reset this register by writing 0 to it, even while the channel is running.

3.2.20 Channel *x* Receive Interval Counter Trigger Register **WRITE**

The Channel *x* Receive Interval Counter Trigger Register enables the user to generate an interrupt and set a flag upon the reception of every *N* number of bytes. The appropriate bit must also be set in the Channel *x* Interrupt/Trigger Condition Register.

3.2.21 Channel *x* Receive Data Byte Counter Trigger Register **WRITE**

The Channel *x* Receive Data Byte Counter Trigger Register enables the user to generate an interrupt and set a flag when a certain number of bytes have been received (1-65535). The appropriate bit must also be set in the Channel *x* Interrupt / Trigger Condition Register.

3.2.22 Channel *x* Receive Buffer Wraparound Register **WRITE**

The Channel *x* Receive Buffer Wraparound Register contains two bits for synchronization with the host.

Bit	Description
15	1 = Multiple Wraparound - Data Lost
14	1 = Single Wraparound since the last data read
00-13	0

Channel *x* Receive Buffer Wraparound Register

NOTE Excalibur software drivers handle these bits. If you use these drivers, you don't need to deal with them.

The user should clear bit 14 each time the first word of the buffer is read. When the buffer wraps around the board checks bit 14. If bit 14 is not set, the board sets it. If bit 14 is set, the board sets bit 15.

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3.2.23 Channel *x* Receive Data Byte Count Register

READ

The Channel *x* Receive Data Byte Count Register indicates the number of bytes received (0-65535). This register wraps around. The user may reset the register, only when the channel is stopped.

3.2.24 Channel *x* Receive Data Current Pointer

READ

The Channel *x* Receive Data Current Pointer indicates the address where the next byte will be placed within the buffer. This pointer value is incremented after the entire receive block (Data Byte, Time Tag, and Status) is written into memory.

3.2.25 Channel *x* Receive Data End Pointer

WRITE

The Channel *x* Receive Data End Pointer sets the End Address of the Receive Data buffer. The address must be a word boundary. The data will wrap around or stop when the buffer is full, (when the End Address is reached) depending upon the Receive Wrap Around control bit within the Channel *x* Configuration Register. (See Channel *x* Configuration Register, page 3-27.

3.2.26 Channel *x* Receive Data Start Pointer

WRITE

The Channel *x* Receive Data Start Pointer Register sets the Start Address of the Receive Data Buffer. The address must be on a word boundary.

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3.2.27 Channel *x* Baud Rate Generator Register

WRITE

The 16-bit, Channel *x* Baud Rate Generator Register must be filled in prior to starting the channel. The value of the register should be set as follows:

Channel Oscillator	**7.3728 MHz**	**8.0000 MHz**
Value =	$\frac{7372800}{16 \times baud}$	$\frac{8000000}{16 \times baud}$

Example:

Desired Baud Rate = 38,400 Hz

Channel Oscillator = 8.0000 MHz

$$\text{Register Value} = \frac{8000000}{16 \times 38400} = 13.0208333$$

The Baud Rate Register should be set to 13 (decimal)

The tables below show representative baud rates available for the two oscillators. The minimum baud rate is 50 baud.

7.37280 MHz oscillator (AA/BB/CC/ZZ Channels)		
Desired Baud Rate (Hz)	BR Generator Register Value	% Error
50	9216	-
75	6144	-
134.5	3426	0.001
150	3072	-
300	1536	-
600	768	-
1000	461	0.043
1200	384	-
1800	256	-
2000	230	0.043
2400	192	-
3600	128	-
4800	96	-
7200	64	-
9600	48	-
10000	46	0.174
19200	24	-
38400	12	-
76800	6	-
153600	3	-
230000	2	0.174

8.00000 MHz oscillator (A/B/C/Z Channels)		
Desired Baud Rate (Hz)	BR Generator Register Value	% Error
50	10000	-
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1000	500	-
1200	417	0.080
1800	277	0.080
2000	250	-
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

NOTE Depending on the configuration of the board, for very high baud rates there may be lost bytes on receive if DTR and CTS are not used, and the inter-byte gaps may be extended on transmit. See Baud Rate Limitations, page 3-28.

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3.2.28 Channel *x* Configuration Register **WRITE**

The Channel *x* Configuration Register sets up various run parameters for both the receive and transmit sections. Bits that are not used (for example, receive-related bits while operating as a transmitter) are ignored by the board.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**Receive Byte Trigger**	1 = Start Data Storage upon receipt of byte *xx* 0 = Receive stores data without Start Byte Trigger
08	**Receive Wrap Around**	1 = Data storage is halted when buffer full 0 = Receive wraps around data within the block
07	**Loopback (RS-485 only)**	1 = Channel receives even during transmission 0 = Channel receives at all times except during transmission (when receive is enabled)
06	**H/W Protocol [3] Handshake (RS-232)**	1 = Transmit only when CTS is high, set DTR hi, if in danger of overrun 0 = Ignore CTS and DTR.
04-05	**Parity Type**	This field determines the parity type:
03	**Parity Enable**	1 = Parity 0 = No parity
02	**Stop Bits**	Specifies the number of stop bits transmitted with each character 1= Two Stop bits are used for lengths 6, 7, and 8. 1.5 Stop bits are used for length 5. 0 = One Stop bit is used
00-01	**Character Length**	This field determines the number of bits in each character sent or received

Bit 05	Bit 04	Parity
0	0	Odd
0	1	Even
1	0	Stick 1
1	1	Stick 0

Bit 01	Bit 00	Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Channel *x* Configuration Register

NOTE

1. The register can only be written to when the respective channel is turned *off* (via the Start/Stop Register).
2. Set all active Channel *x* Configuration Registers immediately following the Board Handshake procedure before programming any parameters.
3. If the hardware protocol is enabled for RS-232, there will be an interbyte delay of at least 1 bit time.

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3.3 Baud Rate Limitations

There are configurations of the EXC-3000PC MAGICard for which the baud rate of the RS-232/422/423/485 channels must be less than the maximum of 250K baud. If not, there will be interbyte gaps in transmission, and a possibility of losing received data.

There are two modes of operation (see the description of the RS-232/422/423/485 Operating Mode Register, page 3-3).

Mode	Operation
Regular	Each received byte may be stored **with** Status and Time Tag. The allowed baud rates are relatively low, but concurrent high speed ARINC operation is not disturbed.
Fast	Each received byte is stored **without** Status and Time Tag. High baud rates are acceptable, but high speed ARINC channels may lose data.

The following equations are a guide, to enable the user to determine which baud rates may be used without data loss. The maximum baud rates are approximate as these values are dependent on factors such as the size of transmitted blocks, and whether or not interrupts are used.

Examples:

1. For **fast** operation with channels working *half-duplex*, receiving only, the approximate maximum baud rate which will not result in data loss:

$$BR\ (KHz) = \frac{160{,}000}{120 + (188 \times R) + (50 \times A)}$$

2. For **fast** operation with channels working *full-duplex*, transmitting and receiving, the approximate maximum baud rate which will not result in data loss :

$$BR\ (KHz) = \frac{160{,}000}{120 = (372 \times R) + (50 \times A)}$$

3. For the **regular** operation mode with channels working *full-duplex*, transmitting and receiving, the approximate maximum baud rate will not result in data loss:

$$BR\ (KHz) = \frac{10{,}000}{120 + (51 \times R) + (50 \times A)}$$

Key:

BR	Baud Rate in KHz
R	Number of RS channels running on the board
A	The number of ARINC channels

NOTE The Maximum allowed baud rate for the RS-232/422/423/485 channels is 250K baud even if the calculated value of the baud rate is greater.

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3.4 RS Transmit Channel Operation

To initiate a transmission the user must:

1. Create an Instruction Stack for the transmit channel and write the data into the dual-port RAM before writing to the Channel *x* Start Transmit Register.
2. The Channel Configuration Register and the Channel *x* Baud Rate Generator must be set before writing to the Global Start Register.
3. Write to both the Global Start Register and the Channel *x* Start Transmit Register.

The user may write a 0 to the Channel Start Transmit Register, update the Instruction Stack and data, and then restart transmission by restoring the register to 1, without writing a 0 to the Global Start Register. This is necessary in order not to interfere with the receive operation.

3.4.1 Transmit Instruction Stack

The Transmit Instruction Stack is divided into Instruction Blocks – each containing four words. Each Instruction Block relates to a Data Block. A Data Block consists of one or more bytes that the user desires to transmit *contiguously*. The stack is sequential, so that the first Instruction Block relates to the first Data Block, the second to the second Data Block, and so on.

Instruction Blocks are accessed sequentially and their associated Data Bytes transmitted according to this sequential order.

The fours words in an Instruction Block are:

1st Word: The Control Word – reserved for future use

2nd Word: A 16-bit byte count that instructs the board as to the number of serial bytes to transmit within a particular block.

3rd Word: A 16-bit, user-supplied data pointer. This is a 16-bit address (must be a word boundary) that points to the beginning of the data within the memory.

4th Word: The Interblock Time value that is used to program the time between blocks.

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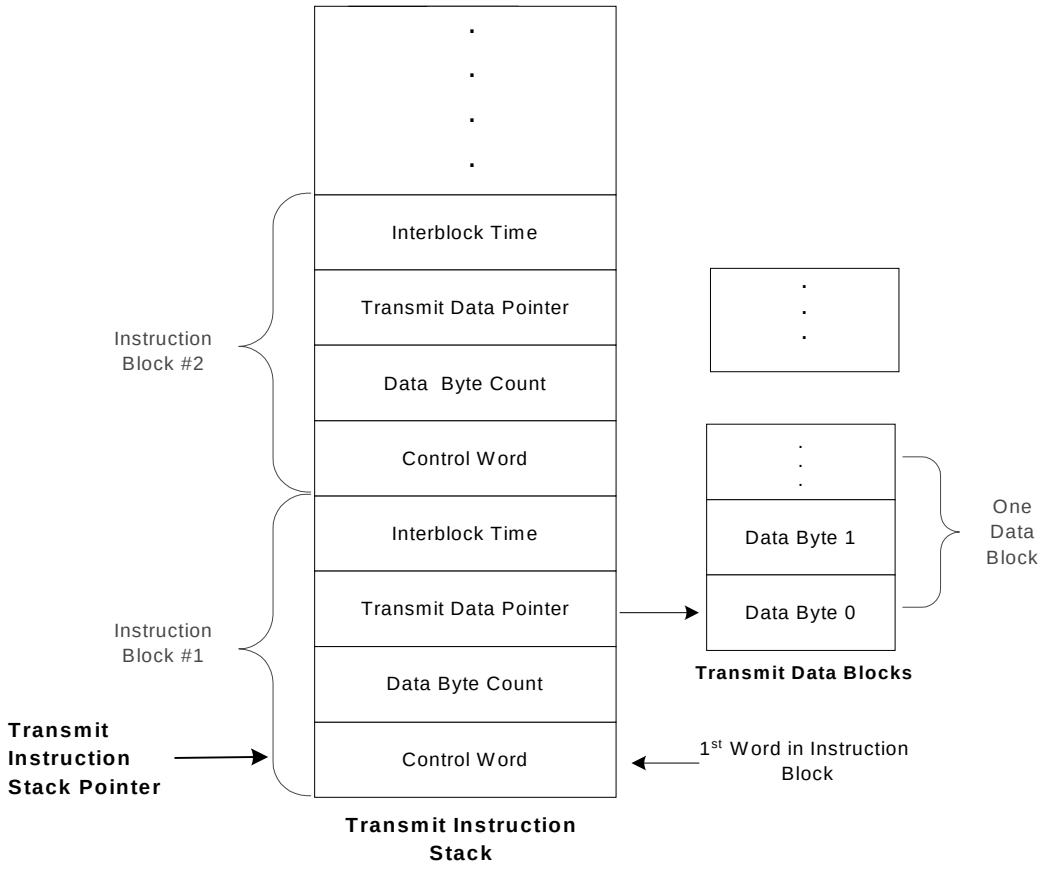


Figure 3-12 RS Channel Transmit Instruction Stack Structure

3.4.1.1 Control Word Definition

The 1st word of the Instruction Block. The field is reserved for future use.

3.4.1.2 Data Byte Count

The 2nd word of the Instruction Block. The Data Byte Count is used to specify the number of data bytes within this Data Block (1-65535).

3.4.1.3 Transmit Data Pointer

The 3rd word of the Instruction block is used to set the start address of the Transmit Data Block. The size of the Data Block is determined by the Data Byte Count value.

3.4.1.4 Interblock Time

The 4th word, the Interblock Time allows the user to specify the time between Data Blocks. The resolution of this 16-bit word is one bit time according to the transmission bit rate. Allowed values are 1-65535.

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3.4.1.5 Transmit Data Block Format

The diagram below illustrates the format of the Transmit data bytes within the memory.

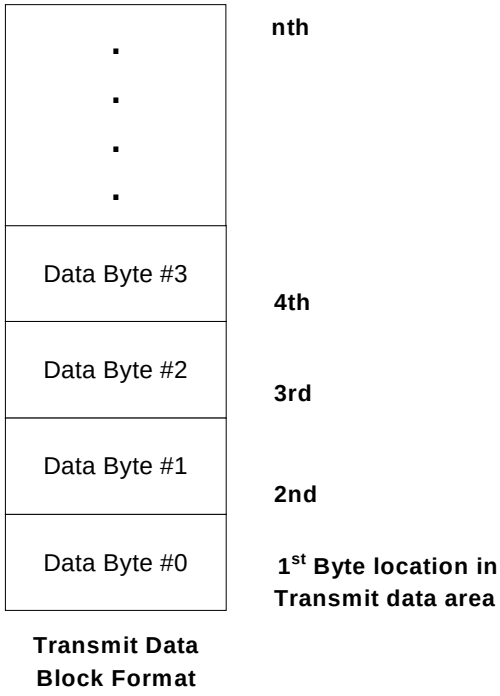


Figure 3-13 Transmit Data Block Format

3.4.1.6 RS-485 Operation - NOTE

RS-485 transmitters go into tristate whenever they are not transmitting a block. This includes the Interblock Time and the time between frames. If there are gaps between bytes within a block (which happens at high baud rates) the transmitter does not enter tristate. The transmitter goes into tristate immediately after the last stop bit of the last byte of a block that was transmitted, and remains tristated until the beginning of the transmission of the start bit of the next byte.

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3.5 RS Receive Channel Operation

The user sets up each channel's receive operation mode by writing to the various Channel *x* Control Registers (one set per channel). There are three receive modes of operation:

Mode	Mode of Operation
Sequential	The data bytes are stored with a Status byte and a 32-bit Time Tag value.
Data Only	Only the data is stored
Fast Operation	Only the data is stored and faster baud rates can be achieved (see Baud Rate Limitations, page 3-28)

The board is initialized in a wait loop – looking for a start command from the computer. This command, issued by writing to the Global Start Register, instructs the board to begin operation on the active channel or channels. The Channel *x* Start Receive Register must also be written to.

The data is stored in sequential order. The data buffer's size and location within the memory is programmed via a Channel *x* Receive Data Start and End Pointer. Each received data byte has an accompanying Status Byte and a 32-bit Time Tag value. These six bytes make up a single receive data block. The data can also be stored without the Time Tag or Status. This is a global selection that affects all RS receive channels, see Receive Data Storage Mode register, page 3-9. Interrupts and pollable status registers allow for numerous event recognition, see the channel register definitions, pages 3-20 to 27.

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3.5.1 Receive Buffer Structure

Sequential Mode

Figure 3-14 RS Channel Sequential Mode Receive Buffer illustrates how the receive Data Blocks are stored within the dual-port RAM while in Sequential mode.

The Start and End pointer set up the buffer size. The receive data storage will stop when the end pointer is reached or will wrap around to the beginning of the buffer, depending upon the condition of the Receive Wrap Around bit within the Channel *x* Configuration Register.

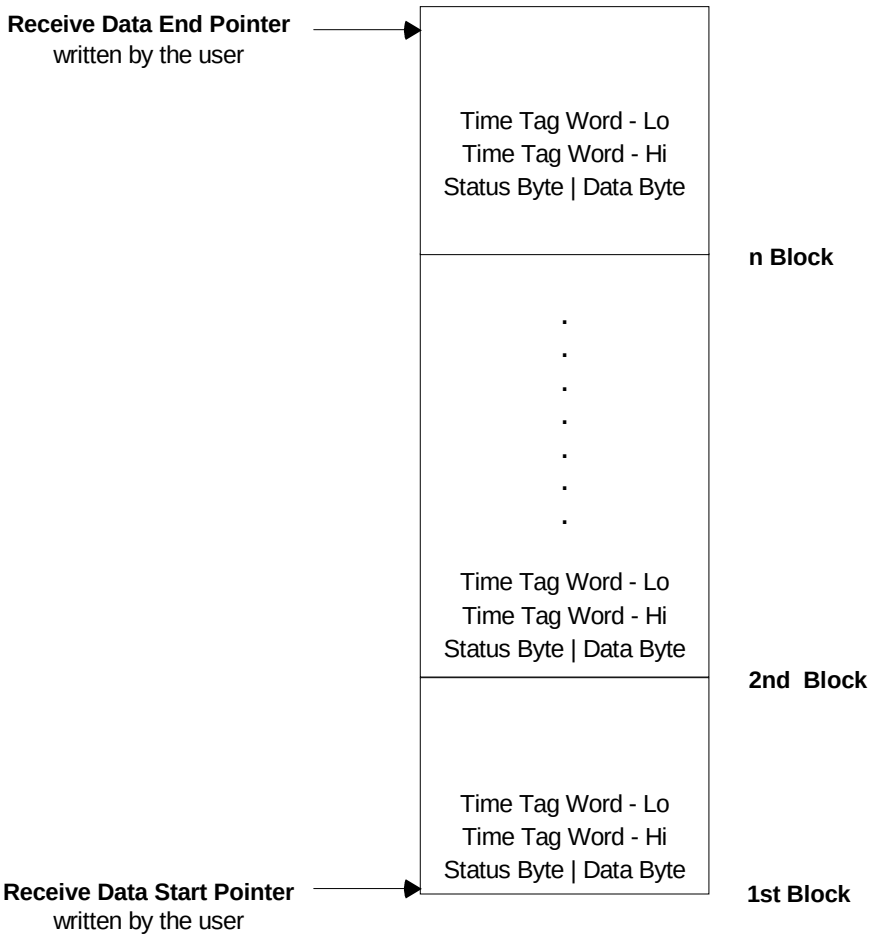


Figure 3-14 RS Channel Sequential Mode Receive Buffer

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Data Only Modes

Figure 3-15 RS Channel Data Only Mode Receive Buffer, shows the format of the Receive Buffer in the Data Only modes (regular and fast).

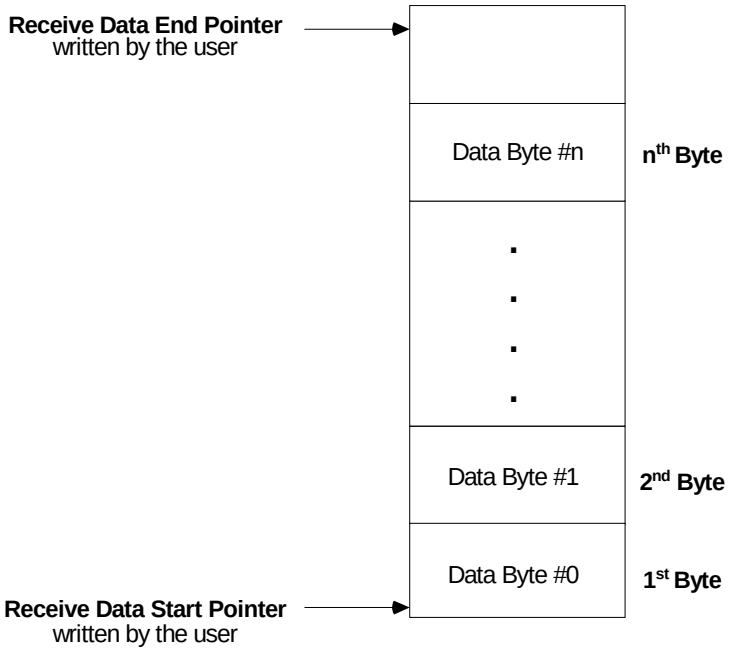


Figure 3-15 RS Channel Data Only Mode Receive Buffer

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3.5.2.1 Time Tag Word Format

The Time Tag is a 32-bit Word made up of two 16-bits Words: Time Tag-Hi and Time Tag-Lo.

The resolution of the Time Tag is 10 µsec/bit.

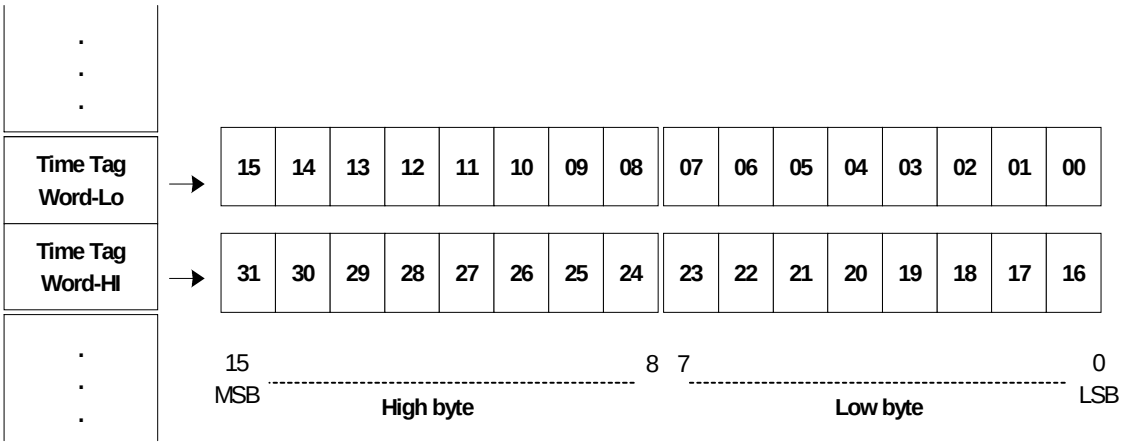


Figure 3-16 RS Time Tag Word Format

3.5.2.2 Receive Status Byte

Bit	Bit Name	Description
05-07	Reserved	Set to 0
04	Break	Indicates receipt of a Break character
03	Frame Error	Indicates received character that did not have a valid stop bit
02	Parity Error	Indicates received parity that did not match the parity chosen in the Channel *x* Configuration register
01	Overrun Error	Indicates a byte was lost. This can occur at speeds greater than 19200 baud when many channels are working simultaneously.
00	Data Ready	Indicates that a Byte has been received.

Status Byte Bit Definitions

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4 Mechanical and Electrical Specifications

Chapter 4 describes the mechanical and electrical specifications of the EXC-3000PC MAGICard.

4.1	Board Layout	page 4-2
	4.1.1 EXC-3000PC Board	page 4-2
	4.1.2 EXC-3000PCH Board	page 4-2
4.2	DIP Switches	page 4-3
4.3	LED Indicators	page 4-4
4.4	Jumpers	page 4-5
4.5	Connectors	page 4-6
4.6	Power Supply Requirements	page 4-13

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4.1 Board Layout

4.1.1 EXC-3000PC Board

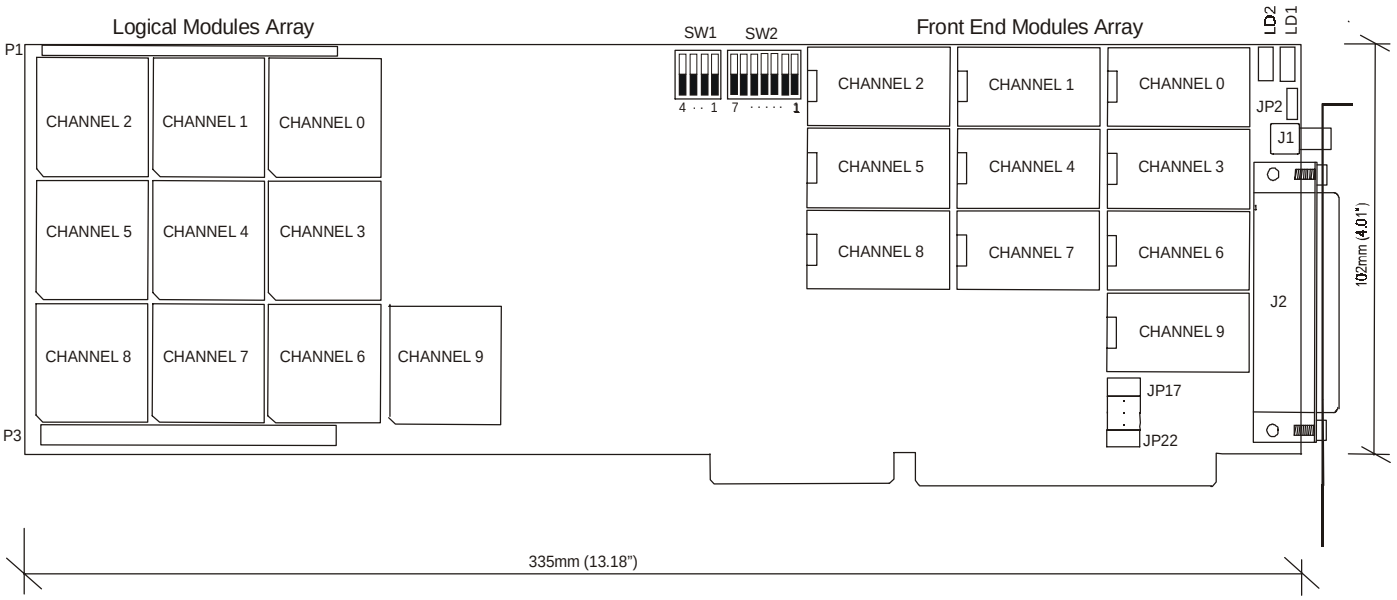


Figure 4-1 EXC-3000PC Board Layout

4.1.2 EXC-3000PCH Board

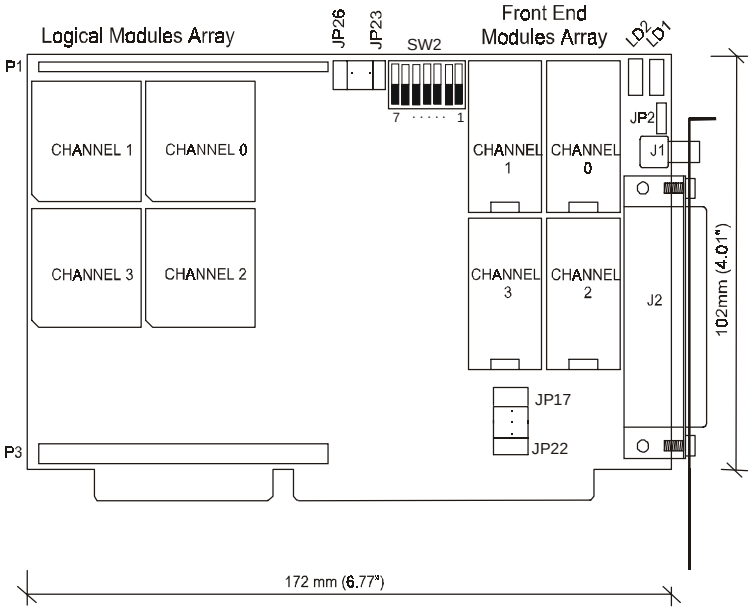


Figure 4-2 EXC-3000PCH Board Layout

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4.2 DIP Switches

The EXC-3000PC contains two DIP switches:

Switch	Description
SW1	Board Configuration DIP switch *EXC-3000PC Only*
SW2	Address Decode DIP switch

DIP Switches

NOTE The EXC-3000PCH has one DIP switch – the SW2 Address Decoding SIP switch.

4.2.1 Board Configuration DIP Switch – SW1 EXC-3000PCH

This 4-position DIP switch is not utilized at present. The switch is reserved to enable the user to add unique, customer-specific functions, in the future.

Switch	Description
1-4	Reserved

Board Configuration DIP Switch – SW1

4.2.2 Address Decode DIP Switch – SW2

The Address Decoding DIP switch SW2 is used to set the board's base address. The EXC-3000PC board occupies 32K (one-half segment) of memory within the PC's lower one megabyte of memory address space. Switch contacts 1-5 of SW2, corresponding to address lines A19-A15, are used to select the base address of this half segment. Switch contact 6 is reserved, and switch contact 7 selects the computer type.

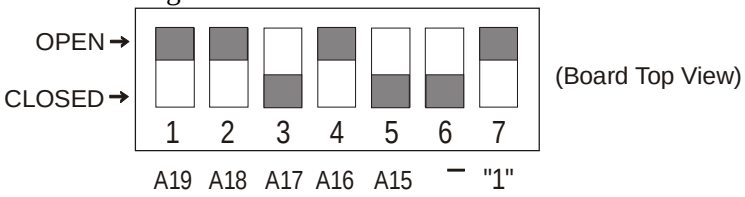
Switch Contact	Description
1	A19
2	A18
3	A17
4	A16
5	A15
6	Don't Care
7	1 = Open: 386, 486, ISA, EISA 0 = Closed: PC, XT, 286-AT

Address Decoding DIP Switch (SW2)

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Set DIP switch SW2 to the desired address by setting the switch contacts OPEN or OFF to represent logic 1 and CLOSED or ON to represent logic 0 (see the example below).

Example To address the board in Segment D, address D0000 (H), set the following switches:



NOTE *A15: The EXC-3000PC allows up to two boards to be addressed within the same memory segment. One board is addressed at (relative) address 0000(H): set A15 to 0. The other board is addressed from (relative) location 8000 (H): set A15 to 1. In this case, for example, the memory of the other board is addressed from offset 8000(H). See the General Memory Map, page 1-6.

4.2.3 Factory Default DIP Switch Settings

The factory default settings are:

Switch	Setting	Description
SW1	All Closed	No configuration
SW2	1,2,4,7 – open 3,5,6 - closed	Segment D0, 386/486 type computer

Default DIP Switch settings

4.3 LED Indicators

The EXC-3000PC contains two LEDS:

LED	Indications
LD1	Board Ready Indicator. After Handshake is completed, the board has finished its Self-test and its initialization procedure; this LED is lit to indicate that the board is ready to communicate with the host.
LD2	Power indicator

LED Inicators

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4.4 Jumpers

Jumpers are provided on the board for various functions. These jumpers are occupied with jumper headers and are shorted with shorting blocks at default places, see Factory Default Jumper Settings, page 4-6.

Jumpers not shown on the board layout diagrams are factory set and should not be used.

4.4.1 External Trigger Polarity Jumper [J2]

This jumpers sets the External Trigger (J1) Polarity:

Positive pulses:	Pins 1 and 2 shorted
Negative pulses:	Pins 2 and 3 shorted

4.4.2 Adapter DMA Channel Select Jumpers [JP17-JP22]

Use this jumper group to select the desired piggyback adapter's DMA channel. These jumpers must be set when installing piggyback adapter boards that use DMA.

Each jumper selects the following

JP17	JP18	JP19	JP20	JP21	JP22
DRQ1	DACK1*	DRQ2	DACK2*	DRQ3	DACK3*

NOTE 1. These jumpers are present on Rev E and later boards.

2. When using DMA Channel: only one pair of six jumpers should be shorted per user requirements.

3. When *not* using DMA: all the jumpers should be left open.

Example: To select the DMA Channel #2

Jumper	Setting
JP17	Open
JP18	Open
JP19	Short
JP20	Short
JP21	Open
JP22	Open

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4.4.3 Board Configuration Jumpers [JP23-JP26] EXC-3000PCH Only

This group is not utilized at present. The jumpers are reserved to enable the user to add unique, customer-specific functions, in the future.

JP26	JP25	JP24	JP23
CNFG3	CNFG2	CNFG1	CNFG0

Board Configuration Jumpers

4.4.4 Factory Default Jumper Settings

The factory default jumper settings are:

Jumpers	Setting	Description
JP2	SHORT	Pins 2 and 1: External Trigger Positive Polarity
JP17-JP22	OPEN	No DMA Channels
JP23-JP26	SHORT	No configurations

Factory Default Jumper Settings

4.5 Connectors

The MAGICard board contains all communication I/O signals on one female, high density DB type 62-pin connector. In addition, a subminiature BNC connector is located on the front panel. Mating connectors are supplied for both.

The MAGICard also contains two, 0.1" spacing socket headers (P1 and P3) for optional installation of a piggyback adapter board.

4.5.1 Subminiature BNC Connector J1 External Trigger

The Subminiature BNC connector supplies an external trigger source output. This front panel connector is under software control and is activated upon the same conditions as interrupts. See Receive Merge Interrupt/Trigger Condition Register, page 2-5, or Channel *x* Interrupt/ Trigger Condition Register, page 3-22.

The external trigger pulse signal is open-collector with a pull-up resistor. The signal polarity and timing is shown below.

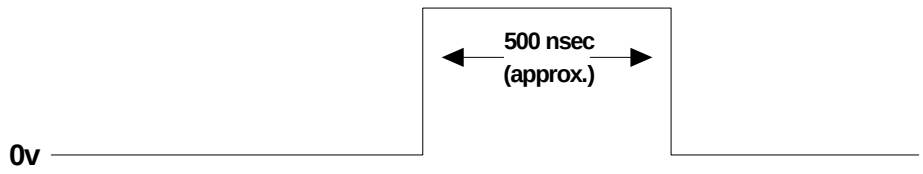


Figure 4-3 External Trigger Positive Pulse Signal

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4.5.2 Connector J2 Pinout Communications I/O

The J2 62-pin connector pinout is defined below. Each channel is allocated six pins (referred to as A-F). The function of each pin depends upon the protocol implemented by the channel.

4.5.3 Connector J2 Layout

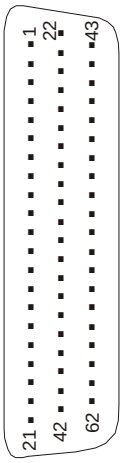


Figure 4-4 Connector J2 Layout: Front View

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4.5.4 Connector J2 Pin Assignments

In Table 4-1 the J2 connector pinout is sorted by Pin number.

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	CH# 0 B	22	Case Ground	43	Digital Ground
2	CH# 0 D	23	CH# 0 A	44	CH# 0 F
3	CH# 1 B	24	CH# 0 C	45	CH# 0 E
4	CH# 1 D	25	CH# 1 A	46	CH# 1 F
5	CH# 2 B	26	CH# 1 C	47	CH# 1 E
6	CH# 2 D	27	CH# 2 A	48	CH# 2 F
7	CH# 3 B	28	CH# 2 C	49	CH# 2 E
8	CH# 3 D	29	CH# 3 A	50	CH# 3 F
9	CH# 4 B	30	CH# 3 C	51	CH# 3 E
10	CH# 4 D	31	CH# 4 A	52	CH# 4 F
11	CH# 5 B	32	CH# 4 C	53	CH# 4 E
12	CH# 5 D	33	CH# 5 A	54	CH# 5 F
13	CH# 6 B	34	CH# 5 C	55	CH# 5 E
14	CH# 6 D	35	CH# 6 A	56	CH# 6 F
15	CH# 7 B	36	CH# 6 C	57	CH# 6 E
16	CH# 7 D	37	CH# 7 A	58	CH# 7 F
17	CH# 8 B	38	CH# 7 C	59	CH# 7 E
18	CH# 8 D	39	CH# 8 A	60	CH# 8 F
19	CH# 9 B	40	CH# 8 C	61	CH# 8 E
20	CH# 9 D	41	CH# 9 A	62	CH# 9 F
21	CH# 9 E	42	CH# 9 C		

Table 4-1 J2 Connector Pinout: Sorted by Pin Numbers

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In Table 4-2 the J2 connector pinout is sorted by Signal Name

Signal Name		Pin #	Signal Name		Pin #
CH# 0	A	23	CH# 5	A	33
CH# 0	B	1	CH# 5	B	11
CH# 0	C	24	CH# 5	C	34
CH# 0	D	2	CH# 5	D	12
CH# 0	E	45	CH# 5	E	55
CH# 0	F	44	CH# 5	F	54
CH# 1	A	25	CH# 6	A	35
CH# 1	B	3	CH# 6	B	13
CH# 1	C	26	CH# 6	C	36
CH# 1	D	4	CH# 6	D	14
CH# 1	E	47	CH# 6	E	47
CH# 1	F	46	CH# 6	F	56
CH# 2	A	27	CH# 7	A	37
CH# 2	B	5	CH# 7	B	15
CH# 2	C	28	CH# 7	C	38
CH# 2	D	6	CH# 7	D	16
CH# 2	E	49	CH# 7	E	59
CH# 2	F	48	CH# 7	F	58
CH# 3	A	29	CH# 8	A	39
CH# 3	B	7	CH# 8	B	17
CH# 3	C	30	CH# 8	C	40
CH# 3	D	8	CH# 8	D	18
CH# 3	E	51	CH# 8	E	61
CH# 3	F	50	CH# 8	F	60
CH# 4	A	31	CH# 9	A	41
CH# 4	B	9	CH# 9	B	19
CH# 4	C	32	CH# 9	C	42
CH# 4	D	10	CH# 9	D	20
CH# 4	E	53	CH# 9	E	21
CH# 4	F	52	CH# 9	F	62
Case Ground		22	Digital Ground		43

Table 4-2 J2 Connector Pinout: Sorted by Signal Name

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4.5.5 J2 Channel Signals Definition per Protocol

ARINC-429/575/582 2-Wire (Transmit Or Receive)

A DATA HI
B DATA LO
C unused
D unused
E CASE GROUND (SHIELD)
F DIGITAL GROUND

ARINC-561/568/582 6-wire (Transmit or Receive)

A DATA HI
B SYNC HI
C CLK HI
D DATA LO
E SYNC LO
F CLK LO

NOTE 1. A common CASE GROUND and a common DIGITAL GROUND is available for these protocols. See Connector J2 Pinout, page 4-8.

2. For channels containing this type of protocol a jumper has to be disconnected on the soldered side of the printed circuit board as follows: CH#n – JPn+5 (n = channel number). For example: for channel #3 cut jumper JP8.

RS-232

A TXD
B RXD
C CTS INPUT
D DTR OUTPUT
E CASE GROUND
F DIGITAL GROUND

RS-422

A DATA TRANSMIT HI
B DATA TRANSMIT LO
C DATA RECEIVE HI (see note 3)
D DATA RECEIVE LO (see note 3)
E CASE GROUND
F DIGITAL GROUND

NOTE 3. The receive inputs are terminated with a 120 ohm resistor between HI and LO inputs.

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RS-485

A DATA HI
B DATA LO
C unused
D unused
E CASE GROUND
F DIGITAL GROUND

RS-423

A DATA TRANSMIT (see note 4)
B DATA TRANSMIT INVERTED (OPTION) (see note 4)
C DATA RECEIVE HI
D DATA RECEIVE LO
E CASE GROUND
F DIGITAL GROUND (Can be paired with DATA TRANSMIT)

NOTE 4. The transmit Driver Rise/Fall time is set to 1 µsec approximately. Replacing the Waveshape resistor R2, located on top of the Front End Module can change this value. Selected values of R2 for different Rise/Fall times are:

Rise/Fall	R2
5 µsec	50K ohm
10 µsec	100K ohm
50 µsec	500K ohm
100 µsec	1M ohm

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4.5.6 PC Bus Edge Connectors Pinout

XT/AT

Pin	Signal		Pin	Signal
A1			B1	GND
A2	D7		B2	RESET
A3	D6		B3	+5V
A4	D5		B4	IRQ2(9)
A5	D4		B5	-5V
A6	D3		B6	DRQ2
A7	D2		B7	-12V
A8	D1		B8	
A9	D0		B9	+12V
A10	I/OCHRDY		B10	GND
A11	AEN		B11	MEMW -
A12	A19		B12	MEMR -
A13	A18		B13	IOW -
A14	A17		B14	IOR -
A15	A16		B15	DACK3 -
A16	A15		B16	DRQ3
A17	A14		B17	DACK1 -
A18	A13		B18	DRQ1
A19	A12		B19	
A20	A11		B20	
A21	A10		B21	IRQ7
A22	A9		B22	IRQ6
A23	A8		B23	IRQ5
A24	A7		B24	IRQ4
A25	A6		B25	IRQ3
A26	A5		B26	DACK2 -
A27	A4		B27	T/C
A28	A3		B28	ALE
A29	A2		B29	+5V
A30	A1		B30	
A31	A0		B31	GND

AT BUS EXTENSION

Pin	Signal		Pin	Signal
C1			D1	
C2			D2	
C3			D3	IRQ10
C4			D4	IRQ11
C5			D5	IRQ12
C6			D6	IRQ15
C7			D7	IRQ14
C8			D8	
C9			D9	
C10			D10	
C11			D11	
C12			D12	
C13			D13	
C14			D14	
C15			D15	
C16			D16	+5V
C17			D17	
C18			D18	GND

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4.6 Power Supply Requirements

The board's power supply requirements are defined below:

MAGICard with no communication channels installed:

+5 volt @ 1.35 Amps
-5 volt @ 40 mA
+12 volt @ 100 mA

Each Channel Requires:

Channel Type	+5 volt	+12 volt
ARINC-429 Transmitter	150mA	100mA
ARINC-429 Receiver	150mA	30mA
ARINC-575 Transmitter	150mA	100mA
ARINC-575 Receiver	150mA	30mA
ARINC-561 Transmitter	150mA	300mA
ARINC-561 Receiver	150mA	30mA
ARINC-568 Transmitter	150mA	300mA
ARINC-568 Receiver	150mA	30mA
ARINC-582 2-wire Transmitter	150mA	100mA
ARINC-582 2-wire Receiver	150mA	30mA
ARINC-582 6-wire Transmitter	150mA	300mA
ARINC-582 6-wire Receiver	150mA	30mA
RS-232 Transmit/Receive	180mA	-
RS-422 Transmit/Receive	180mA	-
RS-485 Transmit/Receive	180mA	-
RS-423 Transmit/Receive	180mA	40mA

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5 Ordering Information

Chapter 5 explains which options to indicate when ordering an EXC-3000PC MAGICard or EXC-3000PCH MAGICard.

BASIC PART

Part Number	Description
EXC-3000PC*option code (s)*	Full-size board, up to 10 channels and 1 piggyback adapter board
EXC-3000PCH*option code (s)*	Half-size board, up to 4 channels and 1 piggyback adapter board

Option Code	Definition	Comments
A*x*	RS-232 TX/RCV – 8.000 MHz	
AA*x*	RS-232 TX/RCV – 7.3728 MHz	
B*x*	RS-422 TX/RCV – 8.000 MHz	
BB*x*	RS-422 TX/RCV – 7.3728 MHz	
C*x*	RS-485 TX/RCV – 8.000 MHz	
CC*x*	RS-485 TX/RCV – 7.3728 MHz	
Z*x*	RS-423 TX/RCV – 8.000 MHz	
ZZ*x*	RS-423 TX/RCV – 7.3728 MHz	
D*x*	ARINC 429 Transmitter	
E*x*	ARINC 429 Receiver	
F*x*	reserved	
G*x*	ARINC 561 Transmitter	
H*x*	ARINC 561 Receiver	
I*x*	ARINC 575 Transmitter	
II*x*	ARINC 575 24-bit Transmitter	
J*x*	ARINC 575 Receiver	
JJ*x*	ARINC 575 24-bit Receiver	
K*x*	ARINC 568 Transmitter	
L*x*	ARINC 568 Receiver	
M*x*	ARINC 582 2-wire Transmitter	
N*x*	ARINC 582 2-wire Receiver	
O*x*	ARINC 582 6-wire Transmitter	
P*x*	ARINC 582 6-wire Receiver	
Q*x*	reserved	
S*x*	reserved	
T*x*	reserved	
W*x*	MB-1553EP (MIL-STD-1553 BC/RT/BM)	Piggyback Adapter board

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NOTE 1. The ***x*** following the Option code denotes the number of channels per board.

For example:

D2 = 2 ARINC 429 Transmitters.

The full-size board supports up to 10 channels and the half-size board supports up to 4 channels.

2. When ordering a board with a number of different protocol channels, the part number must be in the following form:

EXC-3000PC/A*x*B*x*C*x*D*x*

The occupation of channels starts from the left (CH0) to right (CH*n*). If an empty channel is required, insert an asterisk (*).

3. One piggyback adapter board per board.

Part #s for Additional Transmit / Receive Channel Module Sets

Part Number	Description
EXC-3000-AM	RS-232 8.000 MHz module set
EXC-3000-AAM	RS-232 7.3728 MHz module set
EXC-3000-BM	RS-422 8.000 MHz module set
EXC-3000-BBM	RS-422 7.3728 MHz module set
EXC-3000-CM	RS-485 8.000 MHz module set
EXC-3000-CCM	RS-485 7.3728 MHz module set
EXC-3000-ZM	RS-423 8.000 MHz module set
EXC-3000-ZZM	RS-423 7.3728 MHz module set
EXC-3000-DM	ARINC 429 Transmit module set
EXC-3000-EM	ARINC 429 Receive module set
EXC-3000-GM	ARINC 561 Transmit module set
EXC-3000-HM	ARINC 561 Receive module set
EXC-3000-IM	ARINC 575 Transmit module set
EXC-3000-IIM	ARINC 575 24-bit Transmit module set
EXC-3000-JM	ARINC 575 Receive module set
EXC-3000-JJM	ARINC 575 24-bit Receive module set
EXC-3000-KM	ARINC 568 Transmit module set
EXC-3000-LM	ARINC 568 Receive module set
EXC-3000-MM	ARINC 582 2-wire Transmit module set
EXC-3000-NM	ARINC 582 2-wire Receive module set
EXC-3000-OM	ARINC 582 6-wire Transmit module set
EXC-3000-PM	ARINC 582 6-wire Receive module set

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6 Appendices

Chapter 6 contains Appendices describing the ARINC 429 basic word formats and a connections precaution.

Appendix A ARINC 429 Basic Word Formats page 6-2

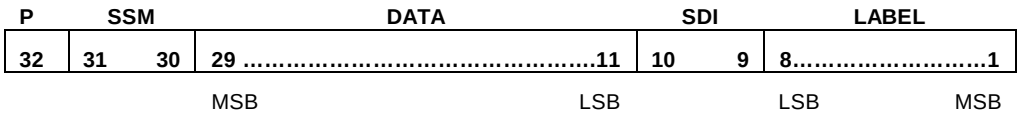
Appendix B ARINC 429 Connection Precautions page 6-4

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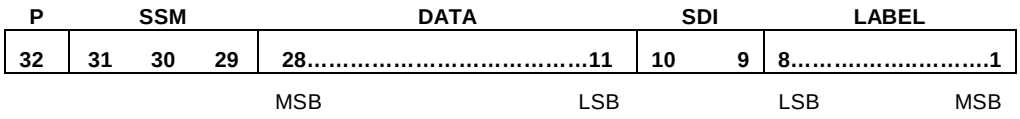
Appendix A ARINC 429 Basic Word Formats

All data sent over the ARINC bus is composed of 32-bit words. A number of different formats can be used, as the following diagrams show:

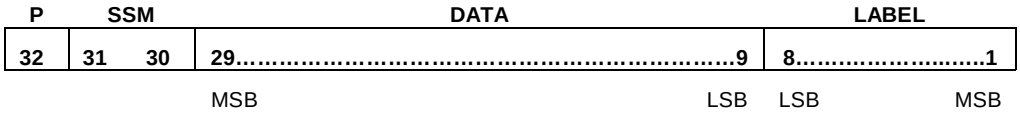
Format 1



Format 2



Format 3



Field	Description
LABEL	Information identifer
SDI	Source/Destination Identifier bits
DATA	Information data: may be presented in one of the following formats
	BNR (Binary)
	BCD (Binary Coded Decimal)
	Discrete
	Maintenance and Acknowledgment
	Alpha Numeric (ISO Alphabet no.5)
SSM	Sign/Status Matrix bits
P	Parity bit (Odd parity)
LSB	Least Significant bit
MSB	Most Significant bit

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Bits are transmitted starting with bit 1, the final bit transmitted is the parity bit, bit 32. The label is transmitted with the most significant bit first while the data is transmitted least significant bit first.

The **LABEL** is a value from 1 to 255 representing a particular type of data. Most labels are defined in the specification though some are reserved for future needs. Many labels are multiply defined in the specification based on the type of equipment being used.

The **SDI** field is used when a transmitter is connected to multiple receivers but not all data is meant to be used by all the receivers. In this case each receiver will be assigned an SDI value and will look only at labels that match its SDI value. While the specification calls for SDI 00 to be universally accepted a good deal of equipment appears to disregard this requirement.

The **DATA** field contains the actual data to be sent. A number of data formats are defined in the specification. Binary Coded Decimal (BCD) format uses each four bits to contain a single decimal digit. BNR data is a binary coding. For both data types the specification calls out the units, the resolution, the range, the number of bits used and how frequently the label should be sent. A discrete type has multiple single bit fields defined within a single label. A number of other formats are described in the specification.

SSM, which is sometime 3 bits long, is used for information which helps interpret the numeric value in the data field. Examples of SSM values might be Plus, North, East, Right, To or Above.

P is the parity bit. ARINC 429 calls for odd parity. The parity bit is the last bit sent over the bus.

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Appendix B ARINC 429 Connection Precautions

This Appendix describes connection precautions for ARINC 429 boards:

1. Verify the ARINC-429 line is not overloaded beyond the spec:

   Rload > 400 ohm
   Cload < 30,000 pF

2. Use shielded twisted pair wires with typical impedance of 60 to 80 ohms.
3. Ensure that there is common ground between the connected systems in order to avoid potential differences.
4. Connect/Disconnect cables while the board is powered OFF or *not* transmitting at least.
5. Special care needs to be taken while applying probes of measuring instruments to avoid shorting out signals.

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