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M4KMMSI

Mini Munitions Store Interface Test and Simulation Module for the EXC-4000 Family of Carrier Boards

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

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1.1 Overview

The *M4KMMSI* is an intelligent, Mini Munitions Store Interface [MMSI] module for the multimode, multiprotocol, Excalibur 4000 family of carrier boards. Each module of the *M4KMMSI* contains 64K bytes of dual-port RAM for Data blocks, Control registers, and Look-up Tables. All Data blocks and Control registers are memory mapped, and may be accessed in real time.

Each *M4KMMSI* module may be programmed to operate in one of three modes of operation: Remote Terminal, Bus Controller/Concurrent-RT/Concurrent Monitor, and Bus Monitor. The module supports three Hub Modes: Spec, Switch and Link.

The *M4KMMSI* comes complete with Windows software, a C-driver software library including source code and may be used with *Exalt Plus*, Excalibur's Analysis and Laboratory Tools, a Windows monitoring application.

The *M4KMMSI*-E option is an extended temperature (-40° to +85°C) version of the module.

The *M4KMMSI* module can be mounted on the following Excalibur carrier boards:

- *EXC-4000PCI[e]*
- *EXC-4000cPCI*
- *EXC-4000P104plus*
- *EXC-4000VME*
- *EXC-4000VXI*
- *EXC-4500ccVPX*
- *EXC-ETHPCIe*

1.1.1 *M4KMMSI* Module Features

- Operates as RT, BC/Concurrent-RT/ Concurrent Monitor or Triggerable Bus Monitor
- Multiple-RT simulation (up to 8 Remote Terminals)
- Supports up to 8 hub ports
- Three Hub Modes: Spec, Switch and Link
- Composite monitor output
- Real-time operation
- Extended Temperature range available – 40º to +85ºC
- Supports broadcast mode
- Service Request Processing
- Multi-mode triggerable Monitor
- Extensive interrupt features
- 64 KB true dual port RAM
- 120 Ohm termination resistors on all ports
- Extensive interrupt features
- Error injection capability:
  - Word Count (+/-3 words)
  - Bit Count (+/-3 bits)
  - Incorrect sync
  - Incorrect RT address
  - Incorrect parity
  - Non-contiguous data
- Service Request Processing
- 1760 Features:
  - Checksum error detection
  - Checksum error injection
  - Header Words

See **Chapter 8: Ordering Information**, for the exact part numbers.

Examples of user selectable parameters are:

- The user can select whether an RT will return a Status Word in the event a message containing a Data Word error is received by the RT.
- Variable response time
- Each bit in the Status Word can be defined by the user

The *M4KMMSI* has three modes of operation:

- Multiple Remote Terminal (RT) mode (up to eight RTs) plus Broadcast
- BC with Concurrent RT operation (up to eight RTs) plus Broadcast
- Triggerable Monitor mode

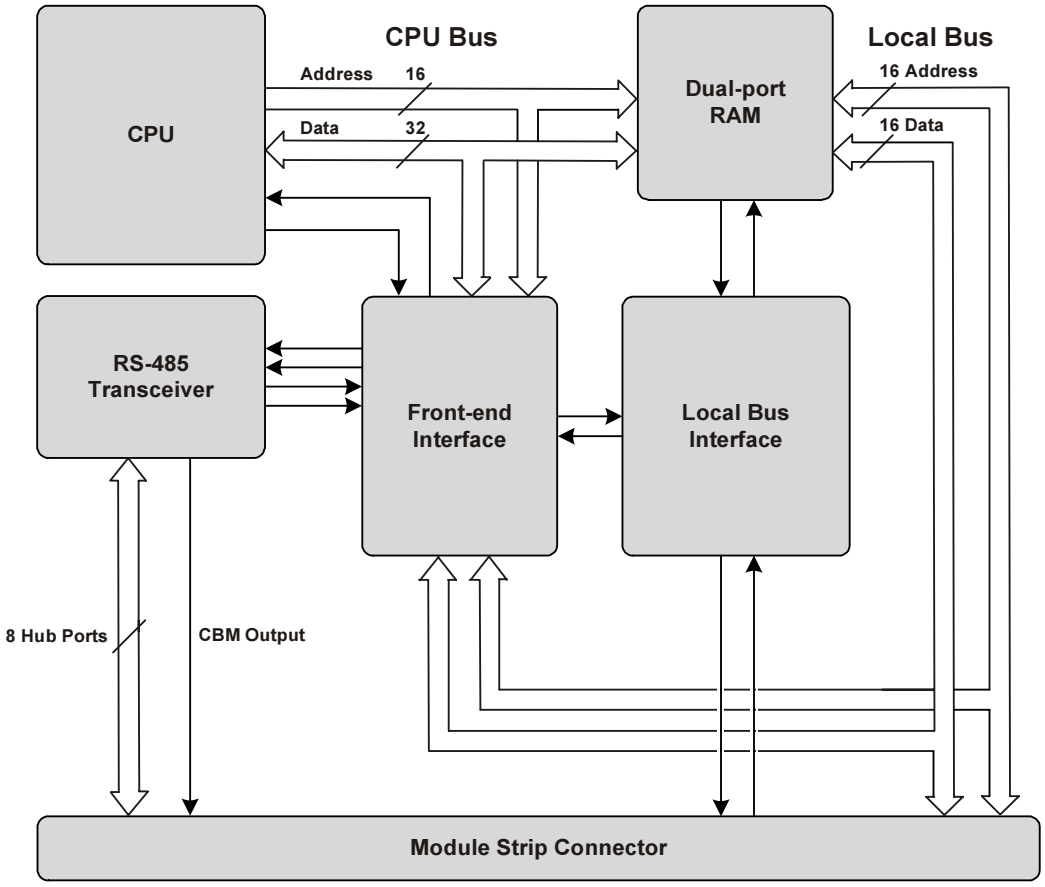


Figure 1-1 *M4KMMSI* Block Diagram

1.1.2 MIL-STD-1760 Features

The *M4KMMSI* module supports MIL-STD-1760 features including checksumming. Checksum is mandated on critical control messages and provisional on the remainder of the messages. Implementing this level of error detection ensures a higher degree of error free data integrity requirements than only odd parity provides.

The MIL-STD-1760 specifications enable:

Checksum generation and checksum error detection capabilities. Checksums are computed as each Data Word is sent or received. If the checksum flag is set on an outgoing message, the checksum will be sent in place of the last Data Word. On an incoming message, the computed checksum is checked against the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status Word.

Checksum error injection in BC/Concurrent-RT mode. The user can set the checksum to intentionally send an error, giving the additional capability to test for checksum errors on the receiving RTs.

Header Words for message identification. The first Data Word of a message may be a Header Word. The Header Word is associated with a specific RT subaddress.

For more details see the sections on **MIL-STD-1760 Features** in **Chapters 3: Remote Terminal Operation** and **4: BC/Concurrent-RT Operation**.

1.2 Installation

For hardware and software installation instructions, see the **readme.pdf** file on the root folder of the installation CD. When downloading new software from the Excalibur website, the **readme.pdf** file is contained in the zip file.

The *Excalibur Installation CD* you received with your package is the most recent release of the CD as of the date of shipping. Software and documentation updates can be found and downloaded from our website: www.mil-1553.com.

The standard software provided with Excalibur boards and modules is for Windows operating systems. For more details, see the **readme.pdf** file. Software for other operating systems may be available. Check on our website or write to excalibur@mil-1553.com.

1.2.1 Module Installation

Warning Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur module.

1. If the module is supplied separately from the carrier board, *very carefully*, insert the module on the carrier EXC-4000 board. The pin #1 marker (marked with a white rectangle) on the module must be aligned with the white rectangles on the carrier board.
2. With the computer power source switched **off**, insert the EXC-4000 carrier board with the *M4KMMSI* module into a slot in the computer.
3. Attach the MMSI adapter cable to the carrier board I/O connector and to the bus. **This is very important:** The cables may be connected to or disconnected from the board while power to the computer is turned on but *not* while the board is transmitting over the bus.

1.3 *M4KMMSI* General Memory Map

The *M4KMMSI* occupies 64K bytes of the module's 128K-memory space. These 64K bytes are shared between the Control registers and the Data block.

Mode Specific Registers	7010 – FFFF H
Hardware Revision Register	700E – 700F H
Mode Specific Registers	700C – 700D H
Time Tag Hi	700A – 700B H
Time Tag Lo	7008 – 7009 H
Time Tag Reset Register	7007 H
Mode Specific Registers	7001 – 7006 H
Module Reset Register	7000 H
Mode Specific Registers	4000 – 6FFF H
Module Configuration Register	3FFF H
Module ID Register	3FFE H
Module Status Register	3FFD H
Start Register	3 FFC H
Mode Specific Registers	3E86 – 3FFB H
Module Options Register	3E84 – 3E85 H
Reserved	3E81 – 3E83 H
Firmware Revision Register	3E80
Mode Specific Registers	0000 – 3E7F H

Figure 1-2 *M4KMMSI* General Memory Map

Chapters 2 to 4 of the *User's Manual* explain the operation of the *M4KMMSI* module in each of the three modes: Remote Terminal, BC/Concurrent RT and Bus Monitor. In each chapter the mode specific Memory Map and Control registers are described. Chapter 5 covers BC/Concurrent-RT operation.

1.4 MMSI Hub Modes

The MMSI specifications call for the implementation of an enhanced bit rate topology where the Bus controller interfaces directly with a Hub which is responsible for controlling the RTs lines of communication.

The *M4KMMSI* module has 9 differential ports, that is, 9 pairs of wires. Eight of these pairs are used to connect to eight Remote Terminals. The ninth set is used for composite monitor output, over which the Bus Controller sends a copy of any message sent on any of the eight other ports. (For pin assignments, see **7.4.1.1 M4KMMSI Module Terminal Stick and Adapter Cable Pinouts** on page 7-4.)

When in Bus Controller mode, the *M4KMMSI* acts as a MMSI Hub. There are three modes defined by the MMSI specification in which the Hub may operate in order to communicate to the attached RTs: Spec Mode, Switch Mode and Link Mode.

In all three modes, responses by Remote Terminals are received only on the connection between the Remote Terminal and the Bus Controller; other RTs never see these responses which means that there are no RT-to-RT messages in the MMSI protocol.

Spec Mode The data bus closely mimics the operation of the MIL-STD-1553 bus. The command word sent by the Bus Controller contain the RT address of the RT with which it is communicating.

- In BC operation, all messages are sent out over all ports. So all RTs see all messages, including message intended for other RTs.
- In RT operation, even if multiple RTs are simulated, the response is sent only over the line associated with the RT. For example, if a message is received for RT2, even though the message will physically be received on all 8 connections, the response will only be sent over the connection for RT2.
- In BC/Concurrent-RT operation RT responses are sent over all ports.

Switch Mode The command word sent by the Bus Controller contains the RT address of the RT with which it is communicating.

- All non-broadcast messages are sent out only over the port associated with the specified RT. In RT operation, even if multiple RTs are simulated, the response is sent only over the line associated with the RT.
- All Broadcast messages (RT address 31) are transmitted to all RTs simultaneously. RTs do not respond to broadcast messages.

Link Mode The data bus eliminates the need for external RT addressing. The command word sent by the Bus Controller does not contain the RT address of the RT with which it is communicating. Since commands are sent only to the port of the RT being communicated with, the RT will respond to all message received on its port.

- Link Mode requires the BC to send out all commands with an RT address of either 0 or 31 (for Broadcast messages). The user writes the commands with the RT address which is used by the module to determine which port to send the messages over, the module will strip out the port number from the command word prior to sending out the command.

- The Concurrent monitor records messages with the RT address not stripped out, making it easier for the user to understand the data flow. The composite monitor transmission over the ninth port reflects the transmission to the RTs and therefore does not include the RT address in the command word.
- In RT operation, the port number is substituted for the RT address (except for Broadcast messages which use RT address 31) for purposes of accessing the Lookup table. Command words placed in the RT Message Stack have the RT address inserted into the command.

The Hub Mode is selected via the Hub Mode registers in RT mode or BC/Concurrent-RT mode. See pages 2-19 and page 3-19.

2 Remote Terminal Operation

Chapter 2 describes *M4KMMSI* operation in Remote Terminal (RT) mode. The following topics are covered:

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2.1 Remote Terminal Mode Overview

The *M4KMMSI* can be configured to simulate up to eight remote terminals. The user selects which terminal or terminals are active and can inject errors into message responses. RT31 is regarded as a Broadcast RT. Message to RT31will be recorded but no Status Word will be sent following receipt of a Broadcast message.

After receiving the Start command, the module handles the transfer of all messages. See section **2.14 Control Register Definitions** on page 2-14. Data is associated with a particular RT subaddress via a 2K × 8 Look-up Table, which points to one of 200 data blocks. The user loads Data Blocks associated with transmit commands with MMSI data to transmit, and reads received MMSI data from Data Blocks associated with receive commands.

The module will respond properly to messages received with an intermessage gap time of 1 μsec.

The remote terminal transmits its Status Word in approximately 2 μsec. Use the RT Response Time Register to increase the time it takes the remote terminal to transmit the Status Word.

TO DETERMINE WHETHER THE MODULE IS INSTALLED AND READY TO OPERATE:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID Register (test for value = 45 H)
2. Check the Module Status Register (test for Module Ready bit = 1)

The module is installed and ready when both registers contain the correct values, as written above. For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset Register.

Note: Throughout this manual, writing a '1' to the Start Register is referred to as "issuing a Start command".

2.1.1 Hub Modes

The Hub Mode determines how the Bus Controller interacts with the Remote Terminals. For a description of the Hub Modes, see **1.4 MMSI Hub Modes** on page 1-6. Use the Hub Mode Register to select the Hub Mode. See **Hub Mode Register** on page 2-19.

2.2 RT Memory Map

Reserved	700C – FFFF H		
Time Tag Hi	700A – 700B H		
Time Tag Lo	7008 – 7009 H	Reserved	3EA2 – 3EAB H
Time Tag Reset Register	7007 H	Serial Number Register	3EA0 – 3EA1 H
Reserved	7004 – 7006 H	Reserved	3E96 – 3E9F H
RT Link Activate Register	7003 H	Double Buffering RTid Register	3E94 – 3E95 H
Reserved	7001 – 7002 H	Double Buffering Bad Block Number Register	3E92 – 3E93 H
Module Reset Register	7000 H	Concurrent Monitor Next Message Pointer	3E90 – 3E91 H
RT Message Stack [512 blocks]	6000 – 6FFF H	Reserved	3E8A – 3E8F H
Reserved	5800 – 5FFF H	Clear Time Tag on Sync Register	3E88 – 3E89 H
RTid Control Table [2K x 16]	4800 – 57FF H	Reserved	3E81 – 3E87 H
Data Block Look-Up Table [2K x 8]	4000 – 47FF H	Firmware Revision Register	3E80 H
Module Configuration Register	3FFF H	Reserved	34C0 – 3E7F H
Module ID Register	3FFE H	RT Vector Words [64 Bytes]	3480 – 34BF H
Module Status Register	3FFD H	RT Bit Words [64 Bytes]	3440 – 347F H
Start Register	3FFC H	RT Last Command Words [64 Bytes]	3400 – 343F H
Message Received Status Register	3FFB H	Reserved	33FD – 33FF H
Reserved	3FFA H	Interrupt Condition Register	33FC H
Hub Mode Register	3FF8 H	Reserved	3300 – 33FB H
Reserved	3FF5 – 3FF7 H	Word Count Error Table	32E0 – 32FF H
RT Response Time Register	3FF4 H	Reserved	32C0 – 32DF H
Error Injection Register	3FF3 H	Bad Block Data [32 Bytes]	3280 – 32BF H
Reserved	3F80 – 3FF2 H	Reserved	3266 – 327F H
1760 Header Value Transmit Table [64 Bytes]	3F40 – 3F7F H		
1760 Header Value Receive Table [64 Bytes]	3F00 – 3F3F H	1760 Checksum Limits Register	3264 – 3265 H
1760 Header Exist Table [64 Bytes]	3EC0 – 3EFF H	Reserved	3260 – 3263 H
RT Message Stack Pointer	3EBE – 3EBF H	RT Status Words [64 Bytes]	3220 – 325F H
Reserved	3EB0 – 3EBD H	Active RT Table [32 Bytes]	3200 – 321F H
Message Counter Lo	3EAE – 3EAF H	Data Blocks [200 Blocks]	0000 – 31FF H
Message Counter Hi	3EAC – 3EAD H		

Figure 2-1 RT Memory Map

2.3 Data Block Look-up Table

Address: 4000 – 47FF (H)

The received Command Word's RT Address, T/R Bit, and Subaddress fields are used to index the entries in the (user-programmed) Look-up table. Each entry in the table represents a data block number (from 0 to 199 decimal). Each block can contain up to 32 Data Words (64 bytes). Data Block 0 begins at address 0000. Data Block 1 begins at address 0040 (H), etc.

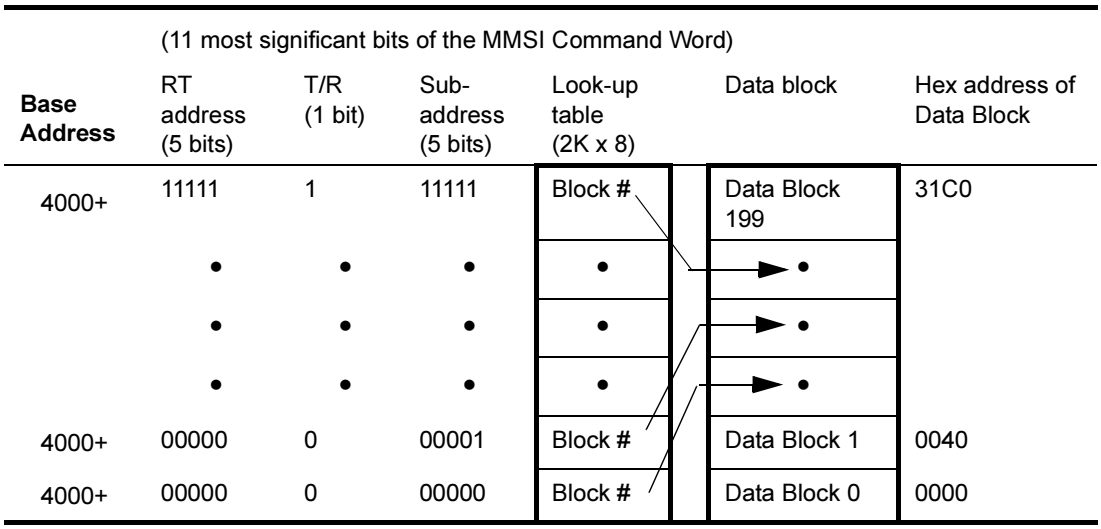


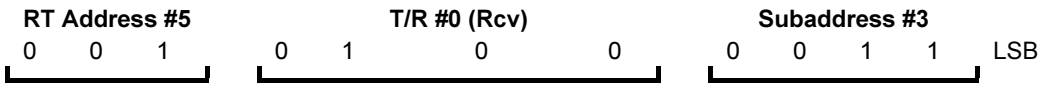
Figure 2-2 Data Block Look-up Table

Note: Data Block 0 represents a default for all unassigned RTid's and is not recommended for use by anyone interested in using the data. If the RT does not assign a Data Block to an RTid, the default Data Block is used for both receive and transmit messages.

TO CREATE AN ADDRESS TO A LOOK-UP TABLE

1. Isolate the eleven most significant bits of the Command Word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example: To allocate a Data Block for a receive message to RT#5, Subaddress 3.



Hex representation = 143 (H)

2. Add the Hex value of this part of the Command Word to the base address of the Look-up table (4000 H).

4000	(H)
+143	(H)
4143	(H)

3. Write the data block number to this location.

Example: Writing a 1 to address 4143 H allocates block #1 for the data of this message. Read the data out by reading block #1, which starts at address 0040 (H). Each data block, beginning at address 0000 is 64 bytes long (for up to 32 Data Words). The address of a block is obtained by multiplying its block number by 64 (40 H).

2.3.1 Data Storage

The Data Words must be stored and/or read in the following format in the data block:

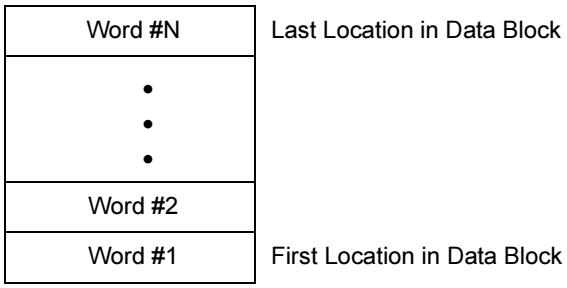


Figure 2-3 Data Storage Sequence

2.4 Active RT Table

Address: 3200 – 321F (H)

The first 31 locations (bytes) of the Active RT table contain the list of active remote terminals. The 32nd location is reserved for Broadcast. To select an RT to be simulated, set bit 00 in the Active Remote Terminal byte to logic 1. The first active RT byte relates to RT #0, the next to RT #1, and the last location relates to RT #30. In addition to setting the RT active (bit 00) various properties of the RT are also set.

The *M4KMMSI* has eight ports to communicate with eight RTs. However, the RT numbers of these eight RTs can be any eight numbers from 0 – 30. To calculate which port an RT corresponds to, use RT# MOD 8. So RTs 0 – 7 use ports 0 – 7, RT #8 uses Port 0, RT #9 uses Port 1, and so on. You cannot use two RT numbers that use the same port, for example, RT #0 and RT #8.

Note: The contents of the Active RT table *cannot* be changed while the module is running.

RT#31 Broadcast byte	32nd byte	321F H	
RT#30 Active RT byte	31st byte	321E H	This RT uses Port 6
• • •	• • •	• • •	• • •
RT#24 Active RT byte	25th byte	3218 H	This RT uses Port 0
• • •	• • •	• • •	• • •
RT#16 Active RT byte	17th byte	3210 H	This RT uses Port 0
• • •	• • •	• • •	• • •
RT#8 Active RT byte	9th byte	3208 H	This RT uses Port 0
• • •	• • •	• • •	• • •
RT#0 Active RT byte	1st byte	3200 H	This RT uses Port 0

Figure 2-4 Active RT Table – RT Mode

Bit	Bit Name	Description
02-07	**0**	Reserved
01	**Interrupt**	1 = Interrupt 0 = No Interrupt If bit 01 is set to 1, if the RT is active and the Interrupt Condition Register is enabled, then this module will generate an interrupt as per the **Interrupt Condition Register** on page 2-23.
00	**Active**	1 = Active 0 = Inactive If bit 00 is set to 0, the RT is not active – none of the other bit settings are relevant. If it is set to 1, the other bits are checked.

Active RT Byte Definition – RT Mode

2.5 RT Status Word

Address: 3220 – 325F H

These locations are reserved for the 32 RT Status Words. Load the desired Status Words into their respective locations in the block. The first word relates to RT#0, the next word to RT#1, while the last word relates to RT#30.

Whenever the RT has to respond with a Status Word, the module sends out the Status Word as the user has defined it with the addition of certain other bits that the module may set, as described below.

The top 5 bits, i.e. the RT Address Field remain unchanged.

Note: If an error occurred in the Command Word, the module cannot send out an RT Status Word – the RT is unknown.

Bit	Name	Description
11-15	RT Address	
10	Message Error	Invalid or illegal word/s received in preceding command
09	Instrumentation	Always 0, to distinguish between Command and Status
08	Service Request (SRQ)	Indicates to BC that RT needs servicing
05-07	Reserved	
04	Broadcast	Preceding Command Word was a Broadcast Command
03	Busy	RT cannot send data in response to BC command
02	Subsystem Flag	RT fault exists; data being requested may be invalid
01	Dynamic Bus	Acceptance of offer by active BC to be the next BC
00	Terminal Flag	RT fault condition (used with Mode Codes 6,7,19)

Table 2-1 RT Status Word Bits

2.5.1 RT Status Word Bits

MESSAGE ERROR BIT [BIT 10]

If an error occured in the data of a message, the module will not send out a Status Word at all. But, on the next message, the module will send out the Status Word with the ME bit set to 1. The ME bit will be reset to the user-defined value when the next valid command is received by the RT (unless the next valid command is a mode code Transmit Status Word or modecode Transmit Last Command).

If the RTid has been set illegal by the user, the module will always set the ME bit to 1 in the Status Word sent back in response to a command for that RTid, whether the message is of type Send or Suppress Status.

SERVICE REQUEST BIT (SRQ) [BIT 8]

Setting the SRQ bit indicates to the BC that a subaddress on this RT requires servicing. (For BC processing of this bit, see section **3.7 Service Request [SRQ] Processing,** on page 3-13).

BROADCAST (BIT 4)

If a Broadcast message is received, the module does not send out a Status Word. But, each active RT, on the next message it receives, will send out the Status Word with the Broadcast Bit set to 1.

The Broadcast Bit will be reset (to the user-defined value) when the next valid command is received by the RT (unless the next valid command is mode code Transmit Status Word or mode code Transmit Last Command).

BUSY (BIT 3)

In the case of Transmit commands, when the user has set the Busy bit, no Data Word will be transmitted by the RT following the transmission of the Status Word.

2.6 RT Message Stack

Address: 6000 – 6FFF H

The module generates a message stack in the dual-port RAM. This stack contains information used for post-processing of RT messages. The stack is divided into 512 blocks, each containing four words, including a 32-bit Time Tag value. The stack operates as a circular buffer. Only active RT messages are stored. **Figure 2-5** illustrates one block.

Control and status information is stored in the memory in the following sequence:	**Byte Offset**
Message Status Word	+6
Time Tag Lo	+4
Time Tag Hi	+2
MMSI Command Word	0

Figure 2-5 Message Stack Block Structure

The RT message stack pointer at 3EBE H points to the beginning of the next unused block.

2.6.1 Message Status Word

The Message Status Word indicates the status of the message transfer. The module creates this word. Do not confuse this word with the Status Word (see section **2.5 RT Status Word** on page 2-7). The contents of the Message Status Word are:

Bit	Bit Name	Description
15	End of Message	Message transfer completed
14	Reserved	Set to 0
13	1760 Checksum Error	The computed checksum (on an incoming message) does not match the last Data Word received See **2.13.2 1760 Checksum Error** on page 2-13.
09-12	Reserved	Set to 0
08	1760 Header Error	Header Word received does not match the value set in the Header Value table. See **2.13.1 1760 Header Word,** on page 2-13.
07	Invalid Word Received	At least one invalid Word received (i.e. bit count, Manchester code, parity)
06	Reserved	Set to 0
05	Word Count Error (Receive Message)	Incorrect number of words received in the message
04	Broadcast Message	Broadcast Command Word received
03	Incorrect Sync Received	Sync of either the Status or the Data Word(s) is incorrect
02	Non- Contiguous Data (Receive Message)	Invalid gap between received MMSI Words
01	Reserved	Set to 0
00	Error	Error occurred (The error type is defined in one of the other message status bit locations)

Remote Terminal Message Status Word

Note:

- A logic 1 indicates the occurrence of a status flag
- The Message Status Word is valid only when bit 15, End of Message, is turned on.

2.6.2 Time Tag

Read only The Time Tag value is a 32-bit word that can be used to determine the time elapsed since the Start command was issued or the time between MMSI messages. The Time Tag uses a 32-bit, free-running counter whose resolution is set by the Time Tag Resolution Register.

This value has a resolution of 4 μsec. per bit. When a message comes in, the current value of the Time Tag counter is written to the Message Stack.

To reset the Time Tag counter (to 0) any time, write to the **Time Tag Reset Register,** see page 2-14. This does not affect existing Message Stack entries.

2.6.3 MMSI Command Word

The Command Word location contains the MMSI Command Word associated with the message.

Only Command Words directed to Active RTs are stored.

2.7 RT Last Command Words

Address: 3400 – 343F (H)

The Last Command Word locations are reserved for the Last Command Words associated with all active RTs. The module writes to these locations at the end of each message transfer (for active RTs only). The first word is for RT#0, the next word is for RT#1, and the last word is for RT#30. These words are used for the implementation of the Transmit Last Command Word Mode code.

Note: Only Command Words of valid messages containing no errors are recorded in this table.

2.8 RT BIT Words

Address: 3440 – 347F (H)

The RT BIT (Built-in Test) word locations are reserved for the BIT words associated with all active RTs. Load the desired BIT words into the corresponding locations in the block. The first word is for RT#0, the next word is for RT#1, and the last word is for RT#30. These words are used to implement the Transmit BIT Word Mode code.

2.9 RT Vector Words

Address: 3480 – 34BF (H)

The RT Vector Word locations are reserved for the Vector words associated with all active RTs. Load the desired Vector words into the corresponding locations in the block. The first word is for RT#0, the next word is for RT#1, and the last word is for RT#30. These words are used to implement the Transmit Vector word Mode code.

Bit	Description
15	1 = Indicates that the contents of the Vector Word represent a subsystem status. 0 = If the BC supports SRQ processing it will build a transmit message (RT-to-BC) to this RT, with the Subaddress and Word Count as indicated in the corresponding bit positions of the Vector Word. If the Vector Word Subaddress field is set to 0 (or if the whole Vector Word is set to 0) this is as if requesting the module to send a mode code of 0 as an RT-to-BC command. This does not make any sense, and therefore, the module ignores this request.
00 – 14	The RT's Vector value

RT Vector Word Format

2.10 Mode Codes

Both 11111 and 00000 are regarded as subaddress Mode Codes.

The module handles all Mode Codes 1, 2, 3, 6, 7, 8, 16, 17, 18 and 19. The Synchronize with Data Word Mode code is operated upon as a standard message transfer, using the Data Block Look-up table. When the module encounters the Synchronize with Data Word Mode code, the Command Word's RT Address, T/R bit, and Subaddress fields are used as a pointer to the Look-up Table. The table entries that are addressed when the T/R bit = 0 and Subaddress = 00000 or 11111 should contain a Data Block number (0 – 199) indicating where the Synchronize with Data Word's data word should be stored.

The data associated with mode codes (Transmit Last Command, Transmit Bit word, and Transmit Vector word) is set using the dedicated blocks in the on-module memory (described in **RT Last Command Words**, **RT BIT Words**, and **RT Vector Words,** on page 2-11).

2.11 Broadcast Mode

For Broadcast messages, the module stores the received message in a data block area in the same way as standard message formats. RT address, T/R bit and subaddress are used as a pointer to the Data Block Look-up table memory.

2.12 Error Injection Feature

The module allows two types of error injection:

- Global (for all RTs)
- Per RT: The global errors such as Sync and Non-Contiguous data are described in **Error Injection Register,** on page 2-20.

These errors are either ON or OFF for all RTs. The ability to inject a MMSI Word Count error, however, can be set per RT.

2.12.1 Word Count Error Table

Address: 32E0 – 32FF (H)

The Word Count Error is selected by writing to the Word Count Error table, which contains 32 bytes (one per Remote Terminal). The first byte is for RT#0, the second to RT #1, and the last byte is for RT#30. The contents of each location controls the number of Words (±3 words) in the message. The variation is an offset, relative to the MMSI Command Word's Word Count field. The resulting message (if an error is programmed) must contain at least one Data Word.

Upon power-up and software reset, the module sets the Word Count Error Table to the default value, 0.

The user must set the Word Count Error Register before issuing a Start command to the module. To modify the Word Count Error Register, issue a Stop command, modify the register, and then issue a Start command. See **Start Register** on page 2-18.

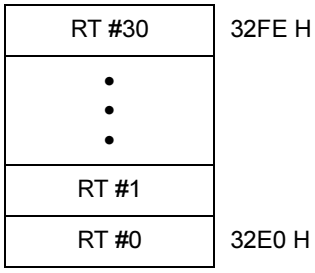


Figure 2-6 Word Count Error Table Address

Register Value	Word Count Offset
FD H	-3 Words
FE H	-2 Words
FF H	-1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Error Byte Values

2.13 MIL-STD-1760 Features

2.13.1 1760 Header Word

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific Subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the Header Exist table to 1. Then set the corresponding entry in the Header Transmit/Receive Value table to the value you expect to receive in the first Data Word of the message. The Header value expected is either the predefined 1760 value, which is the default *M4KMMSI* setting, or another value the user enters in the Header Value Transmit/Receive Table. The module checks that the specified Header receive value was received. In addition, the Internal Concurrent Monitor checks that the specified Header transmit/receive value was received. If the wrong data was received, the **1760 Header error** bit is set in the **Message Status Word,** see page 2-9.

For descriptions of the **1760 Header Value Transmit/Receive Tables** and **1760 Header Exist Table** see page 2-21.

2.13.2 1760 Checksum Error

MIL-STD-1760 implements checksum error detection capabilities. Checksums are computed as each Data Word is received. On an incoming message, the computed checksum is checked against the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status Word.

2.14 Control Register Definitions

RT IDENTIFIER (RTID)

The RTid is referred to frequently in the RT Control registers. The RTid is defined as an RT address, T/R bit value and RT subaddress combination. The structure of the RTid is illustrated below:

5 bits	1 bit	5 bits
RT ADDRESS	T/R[1]	SUBADDRESS

RT Identifier

1. Transmit = 1 / Receive = 0

Example: RT#5, Transmit, Subaddress 6 would be represented as 00101 1 00110 or 0×166. This value can be isolated from a Command Word by shifting the Command Word 5 bits to the right.

Mode Codes: In the case of Mode Code the last 5 bits signify the Mode Code code instead of the Subaddress.

See **To create an address to a Look-up table** on page 2-4.

2.14.1 Time Tag Counter — Address: 7008 – 700B (H)

Read only

The Time Tag is a free-running 32-bit counter on the module. The Time Tag is reset upon a power up or a software reset and starts counting. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset Register.

The user may read the Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

THE COUNTER MUST BE READ IN THE FOLLOWING SEQUENCE:

1. Read 7008 H - Lo word (16 bit, read only)
2. Read 700A H - Hi word (16 bit, read only)

The Time Tag resolution is 4 microsecond per bit.

2.14.2 Time Tag Reset Register — Address: 7007 (H)

Write only

Write any value to the Time Tag Reset Register to reset the module's Time Tag Counter. Immediately after the reset, the counter will start to count from 0.

2.14.3 RT Link Activate Register Address: 7003 H

Each of the 8 bits of the RT Link Activate Register represent one link, indicating whether that link is activated or shut down. When a link is shut down, no messages will be sent over that link, including Broadcast messages.

After power-up, the default for this register is for all links to be active.

Bit	Description	
00	Link 1	1 = Activated 0 = Shut down
01	Link 2	1 = Activated 0 = Shut down
02	Link 3	1 = Activated 0 Shut down
03	Link 4	1 = Activated 0 = Shut down
04	Link 5	1 = Activated 0 = Shut down
05	Link 6	1 = Activated 0 = Shut down
06	Link 7	1 = Activated 0 = Shut down
07	Link 8	1 = Activated 0 = Shut down

Rt Link Activate Register

Set the RT Link Activate Register before issuing a Start command to the module. To modify the register, issue a Stop command, make the required changes, and then issue a Start command. (See **Start Register** on page 2-18)

2.14.4 Module Reset Register Address: 7000 (H)

Write only Write any value to the Module Reset Register to reset the module.

Module Reset erases all locations in the dual-port RAM. Module status, module ID and Firmware registers are written by the module after the reset operation is completed.

2.14.5 RTid Control Table

Address: 4800 – 57FF (H)

The RTid Control Table is a block of memory, one word per RTid, to store settings for a number of features. For the features to be implemented the following conditions must be met:

1. The RT is active
2. The Message is for this specific RTid
3. The bit must be set

Bit	Bit Name	Description
06 – 15	Reserved	
05	Double buffer[1] datablock usage flag	The bit indicates which block of the double buffering pair to use for storing the data for this RTid. 0 = [**Default**] The module detects a receive message. The module stores the data at the even-numbered block number indicated in the Look-up Table. When the module completes writing all the Data Words to the block, the module sets this bit to 1. This indicates to write to the odd-numbered block the next time receive data comes in for this RTid. 1 = The module detects a receive message. The module stores the data at the odd-numbered block, whose number is one more than the even-number indicated in the Look-up Table. When the module completes writing all the Data Words to the block, the module sets this bit to 0. This indicates to write to the even-numbered block the next time receive data comes in for this RTid.
04	Double Buffering (Receive) selected[1]	The bit indicates that the module will double buffer data for the receive messages for this RTid. When the module receives messages for an RTid, the data is stored in the assigned datablock. If no datablock is assigned, data is stored in the default datablock (number 0). When two messages arrive for the same RTid, the data of the second message will overwrite the data of the first message. To preserve the data of the first message long enough to be able to read it before it gets overwritten, use a double buffering scheme to save the data of the last two messages; i.e., use two buffers, alternatively, so that the module can capture data to one buffer, and simultaneously the user can read data from the other buffer. To implement double buffering, the module requires that the datablock assigned to this RTid be an even number. The module then reserves the following odd-numbered block as the paired block for use in double buffering. **Note:** If Double Buffering is enabled for this RTid, and the block number selected is odd, double buffering does not occur. Instead: 1. A flag at bit 02 in the **Message Received Status Register** [3FFB H] is set; 2. The selected (odd) block number is written to the **Double Buffering Bad Block Number Register** [3E92 H] to indicate the error; 3. The RTid is written to the **Double Buffering RTid Register** [3E94 H].

RTid Control Table

Bit	Bit Name	Description
03	Inactive[1]	The RTid is inactive – message is not processed at all; the RT does not send back a Status Word. **Note:** RT response time must be set to at least 5 μsec., otherwise there will be extraneous words on the bus.
02	Illegalization[1]	The ME bit (bit 10) is set in the **RT Status Word**. Only the Status Word is sent back. For **BC-to-RT** (receive) messages – processing continues as per regular algorithm, and the ME bit is written in the STW. For **RT-to-BC** (transmit) messages – no data is sent.
01	Interrupt on Error	Generates an interrupt on error
00	Interrupt on end of message	Generates an interrupt on end of message

RTid Control Table (cont.)

1. Not applicable to Mode Codes

2.14.6 Module Configuration Register

Address: 3FFF (H)

Use the Module Configuration Register to set the operating mode of the module.

Set the Module Configuration Register before issuing a Start command to the module. To modify the Module Configuration Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 2-18)

Bit	Description
00 – 07	02 (H) = RT mode

Module Configuration Register

2.14.7 Module ID Register

Address: 3FFE (H)

The Module ID Register contains a fixed value that can be read by the initialization routine to detect the presence of the module. The one-byte value of this register is 45 (H), ASCII value E.

2.14.8 Module Status Register

Address: 3FFD (H)

The Module Status Register indicates the status of the module. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to '1'.

Bit	Description
07	1 = Module type is always *M4KMMSI*
05 – 06	X "Don't Care"
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit in the Start Register is cleared. Following this, the module sets bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start Register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic '1'.

2.14.9 Start Register

Address: 3FFC (H)

The Start Register controls the Start/Stop operation of the module. The user can Start or Stop the RT operation, modify RT parameters, for example: the Error Injection Register or RT Response Time Register, and then issue a new Start command in real time.

See also **Module Status Register**, bit 04 [Module Halted/Running].

Bit	Description
01 – 07	0
00	1 = Start 0 = Stop

Start Register

Note: The user can start concurrently by sending a low TTL pulse of 100 nsec. Minimum to the **EXSTRTn** pin. See section **7.4.1.1 M4KMMSI Module Terminal Stick and Adapter Cable Pinouts** on page 7-4.

2.14.10 Message Received Status Register

Address: 3FFB (H)

The Message Received Status Register indicates that a 1553 message has been received. A logic '1' indicates active condition. This bit is also set for messages with errors.

Bit	Description
01 – 07	Reserved (set to 0)
00	1 = Message Complete **Note:** Reset this bit after reading it. The module does not reset it.

Message Received Status Register

2.14.11 Hub Mode Register

Address: 3FF8 H

The Hub Mode Register sets the appropriate Hub Mode for RT operation. This register must be set prior to issuing a start to the module. For a description of the Hub Modes, see **1.4 MMSI Hub Modes** on page 1-6.

Bit	Description	Mode of Operation
02 – 07	Reserved (set to 0)	
00 – 01	Hub Mode	0 = Switch mode [**Default**] 1 = Link mode 2 = Spec mode

Hub Mode Register

Set the Hub Mode Register before issuing a Start command to the module. To modify the Hub Mode Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-18.)

2.14.12 RT Response Time Register

Address: 3FF4 (H)

The RT Response Time Register sets the Response Time of the Remote Terminal. The resolution of the Response Time Register is 155 nsec. per bit. The minimum time is approximately 2.5 μsec., which is achieved by writing a 0 to this register. Any value above zero will result is a Response Time equal to the contents of the register × 50 nsec. The actual Response time has a tolerance of ±1 μsec.

Set the Response Time Register before issuing a Start command to the module. To modify the Response Time Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-18)

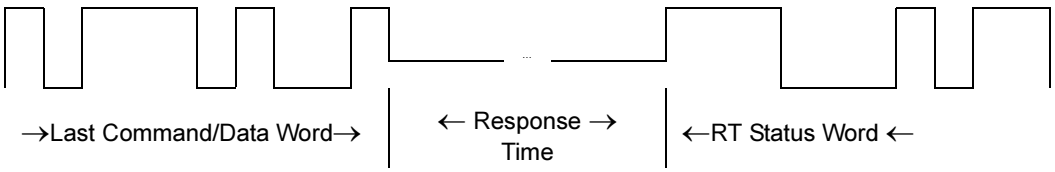


Figure 2-7 RT Response Time Definition

Example: To request a Response time of 4 μsec:
Write 80 to the RT Response Time Register
80 × 0.050 = 4 μsec.

2.14.13 Error Injection Register

Address: 3FF3 (H)

The Error Injection Register is a global register that allows the user to select the type of error to be injected in a transmitted message. When the module receives a Start command (issued by writing to the Start Register), the module reads this Register.

To modify the Error Injection Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-18)

Bit	Description
07	Data Word Sync Error) (Data Words sent with Command Sync)
06	Data Word Parity Error (Data Words sent with Even Parity)
05	Status Word Synchronization Error (Status Word Sent With Data Sync)
04	Status Word Parity Error (Status Word sent with Even Parity)
02 - 03	Reserved (set to 0)
00 – 01	Reserved (set to 0)

Error Injection Register

2.14.14 1760 Header Value Transmit Table

Address: 3F40 – 3F7F H

Write to the 1760 Header Value Transmit table to set the expected value of the first Data Word in a RT-to-BC message. If the wrong data was sent, the Internal Concurrent Monitor will set an error bit. See bit 08 in the **Message Status Word** on page 2-9.

The 1760 option provides predefined values, and these are preset on the *M4KMMSI* module. The user can change the preset values.

Transmit Subaddress	Header Value [Hex]	Address
1	**0421**	3F42 H
11	**0420**	3F56 H
14	**0423**	3F5C H

Predefined 1760 Transmit Header Values

2.14.15 1760 Header Value Receive Table

Address: 3F00 – 3F3F (H)

Write to the 1760 Header Value Receive table to set the expected value of the first Data Word in a BC-to-RT message. The module checks that the specified Header receive value was received. In addition, the Internal Concurrent monitor checks that the specified header value was received. If the wrong data was sent, the **1760 Header Word Error** bit is set in the **Message Status Word,** see page 2-9.

The 1760 option provides predefined values, and these are preset on the *M4KMMSI* module. The user can change the preset values.

Receive Subaddress	Header Value [Hex]	Address
11	**0400**	3F16 H
14	**0422**	3F1C H

Predefined 1760 Receive Header Values

2.14.16 1760 Header Exist Table

Address: 3EC0 – 3EFF (H)

The 1760 Header Exist Table contains 32 entries corresponding to 32 Subaddresses. Each entry may be set to indicate whether the module should expect a Header word for BC-to-RT.

For those Header Value Table entries for which MIL-STD-1760 provides predefined values, the corresponding Header Exist Table entries are preset on the *M4KMMSI* module.

To set other values, enable the Header Exist Table entry for this Subaddress (set it to 1) and write the value to the Header Value [Transmit/Receive] Table.

Bit	Description
09-15	Reserved
08	1 = Module should expect a Header word in a transmit message (RT-to-BC) 0 = Module should **not** expect a Header word in a transmit message
01-07	Reserved
00	1 = Module should expect a Header word in a receive message (BC-to-RT) 0 = Module should **not** expect a Header word in a receive message

1760 Header Exist Table

Associated Subaddress	Header Value [Hex]	Address
1	**0100**	3EC2 H
11	**0101**	3ED6 H
14	**0101**	3EDC H

Predefined 1760 Headers

2.14.17 RT Message Stack Pointer

Address: 3EBE – 3EBF (H)

The RT Message Stack pointer indicates the next word to be written to the RT message stack. After the entire message is received, the message stack pointer is updated (incremented by 8). This word is initialized to 6000 (H) and circulates in the message stack between 6000(H) and 6FFF(H).

2.14.18 Serial Number Register

Address: 3EA0 – 3EA1 (H)

The Serial Number Register holds the board's serial number, which is stored in non-volatile flash memory and loaded at power-up. The value is binary coded. For example, a value of 1234 (H) represents the serial number 4660.

2.14.19 Double Buffering RTid Register

Address: 3E94 – 3E95 (H)

The Double Buffering RTid Register indicates the associated RTid for which the user attempted to set an erroneous odd-numbered block.

2.14.20 Double Buffering Bad Block Number Register

Address: 3E92 – 3E93 (H)

The Double Buffering Bad Block Number Register indicates the erroneous, odd-numbered block selected for use in double buffering.

2.14.21 Clear Time Tag on Sync Register

Address: 3E88 – 3E89 (H)

Set the lower byte [3E88 H] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag registers [7008 – 700B H] (resets to 0) upon receipt of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Set the higher byte [3E89 H] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag registers [7008 – 700B H] (resets to 0) upon receipt of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

Note: This register setting does not effect until the module is restarted.

2.14.22 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision Register indicates the revision level of the on-module firmware. The value 18 (H) would read as revision level '1.8'.

2.14.23 Interrupt Condition Register

Address: 33FC (H)

The Interrupt Condition Register allows the user to enable an interrupt trigger. The bits work in conjunction with the Interrupt bit in the Active RT table. When a message is received by an RT for which the Active RT interrupt bit is set, the module will check the Interrupt Condition Register.

If the module has completed receiving the Command Word and the Begin Data bit is also set, an interrupt trigger will be generated.

If the module has completed processing the message and the Message Complete bit is also set, an interrupt trigger will be generated.

Set the Interrupt Condition Register before issuing a Start command to the module. To modify the Interrupt Condition Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-18.)

Bit	Description
02 – 07	0
01	1 = Message Complete
00	1 = Begin Data

Interrupt Condition Register

2.14.24 1760 Checksum Limits Register

Address: 3264 – 3265 (H)

Write a value to the 1760 Checksum Limits Register to set the data blocks for which the module should compute a checksum value. The module will compute a checksum value for those data blocks whose numerical index is less than the value stored in this register. Maximum value is 200.

Example: Write 20 to the Checksum Limits Register when you want data blocks 0 – 19 to have a checksum value. This causes the module to:

1. Transmit a checksum value as the last word in the data block (transmit message).
2. Check the last word in the data block for a checksum value (receive message).

3 BC/Concurrent-RT Operation

Chapter 3 describes *M4KMMSI* operation in Bus Controller/Concurrent-RT mode. The topics included are:

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3.1.1 Hub Modes . . . 3-2
3.2 BC/Concurrent-RT Memory Map . . . 3-3
3.3 Instruction Stack . . . 3-4
3.3.1 Message Status Word . . . 3-5
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3.1 BC/Concurrent-RT Mode Overview

The *M4KMMSI* can simultaneously operate as the Bus Controller and up to 32 Remote Terminals. The messages and the instruction stack are loaded as for BC operation.

In BC/Concurrent-RT mode, load message blocks with the RT's Status and Data Words for those Remote Terminals that you are actively simulating. These words must be loaded into the appropriate locations in the message blocks in the sequence that the Words appear on the bus.

Note: The requirement for loading the message blocks only applies to RTs that the user is actively simulating. For inactive RTs (not simulated by the module), leave the corresponding locations blank in the associated message blocks.

The Remote Terminals simulated in BC/Concurrent-RT mode have a minimum response time of approximately 4 μsec.

TO DETERMINE IF THE MODULE IS INSTALLED AND READY TO OPERATE:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID Register (test for value = 45 H).
2. Check the Module Status Register (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values. For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset Register.

Note: Throughout this manual, writing a '1' to the Start Register is referred to as issuing a Start command.

3.1.1 Hub Modes

The Hub Mode determines how the Bus Controller interacts with the Remote Terminals. For a description of the Hub Modes, see **1.4 MMSI Hub Modes** on page 1-6. Use the Hub Mode Register to select the Hub Mode. See **Hub Mode Register** on page 3-19.

3.2 BC/Concurrent-RT Memory Map

Concurrent Monitor Message Block Area	8000 – FFFF H
Instruction Stack/Message Block Area	7100 – 7FFF H
Reserved	700C – 70FF H
Time Tag Hi	700A – 700B H
Time Tag Lo	7008 – 7009 H
Time Tag Reset Register	7007 H
Reserved	7001 – 7006 H
Module Reset Register	7000 H
Instruction Stack/Message Block Area	4000 – 6FFF H
Module Configuration Register	3FFF H
Module ID Register	3FFE H
Module Status Register	3FFD H
Start Register	3FFC H
Interrupt Condition Register	3FFB H
Message Status Register	3FFA H
RT Response Time Register	3FF9 H
Hub Mode Register	3FF8 H
Reserved	3FF7 H
Loop Count Register	3FF6 H
Reserved	3FF5 H
Word Count Register	3FF4 H
BC Response Time Register	3FF3 H
Reserved	3FF2 H
Message Stack Pointer	3FF0 – 3FF1 H
Frame Time Lo	3FEE – 3FEF H
Frame Time Hi	3FEC – 3FED H
Instruction Counter	3FEA – 3FEB H
Minor Frame Time Register	3FE8 – 3FE9 H

Minor Frame Time Multiplier Register	3FE6 – 3FE7 H
Reserved	3FD4 – 3FE5 H
SRQ Counter	3FD2 – 3FD3 H
SRQ Message Status Register	3FCE – 3FD1 H
SRQ Message 2 Register	3F88 – 3FCD H
SRQ Message 1 Register	3F80 – 3F87 H
1760 Header Value Transmit Table [64 Bytes]	3F40 – 3F7F H
1760 Header Value Receive Table [64 Bytes]	3F00 – 3F3F H
1760 Header Exist Table [64 Bytes]	3EC0 – 3EFF H
Reserved	3EA2 – 3EBF H
Serial Number Register	3EA0 – 3EA1
Reserved	3E92 – 3E9F H
Concurrent Monitor Next Message Pointer	3E90 – 3E91 H
Reserved	3E8E – 3E8F H
BC Protocol Options Register	3E8C – 3E8D H
Send Time Tag on Sync Register	3E8A – 3E8B H
Clear Time Tag on Sync Register	3E88 – 3E89 H
Reserved	3E81 – 3E87 H
Firmware Revision Register	3E80 H
Reserved	3420 – 3E7F H
Active RT Table [32 Bytes]	3400 – 341F H
Instruction Stack/Message Block Area	0000 – 33FF H

Figure 3-1 BC/Concurrent-RT Memory Map

3.3 Instruction Stack

The Instruction Stack is used to program the module. The stack is divided into instruction blocks, each containing four words. The block contains control information (that the user writes) and status information (that the module writes).

Figure 3-2 Instruction Block Structure – BC/Concurrent-RT Mode illustrates one instruction block.

Control and status information is stored in the memory in the following sequence:	Byte Offset
Message Status Word	+6
Reserved	+4
Intermessage Gap Time	+2
Message Block Pointer	0

Figure 3-2 Instruction Block Structure – BC/Concurrent-RT Mode

3.3.1 Message Status Word

The Message Status Word indicates the status of the message transfer. The module creates this word. Do not confuse this word with the RT Status Word. (See section **2.4 RT Status Word** on page 2-7). The contents of the Message Status Word are described below.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed
14	**Checksum Error**	The computed checksum (on an incoming message) does not match the last Data Word received. See section **3.8.2 1760 Checksum Error** on page 3-14.
13	**Reserved**	Set to 0
12	**Message Error Bit**	Message Error bit (bit 10) in the RT Status Word was set.
11	**RT Status Bit**	A bit was set in the RT Status Word (other than the Message Error bit). The error bit is not set in conjunction with this bit.
10	**Invalid Message Error**	A message-level error occurred (e.g. Word Count, incorrect sync); details in the bits described below.
09	**Response Time Failure**	RT responded late – see **BC Response Time Register,** on page 3-20.
08	**1760 Header Word**	Header Word received does not match the value set in the Header Value Table. See section **3.8.1 1760 Header Word** on page 3-14.
07	**Invalid Word Received**	At least one invalid Word received (e.g., bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	Status Word received did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the Status or Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received Words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. The error type is defined in one of the other message status bit locations.

Message Status Word

Note:

- A logic 1 indicates occurrence of status flag.
- The Message Status Word is valid only when bit 15, End of Message, is turned on.
- To ensure data integrity, the module sets a special status value of 7F00 H [NO_ALTER] to indicate that a message is currently being transmitted or received. Check this value before attempting to change the Data words of the message.

3.3.2 Intermessage Gap Time

The Intermessage Gap Time (IGT) value is a 16-bit word that the user writes, that allows a unique intermessage delay time to be inserted between the current message and the next message. The minimum IGT is approximately 8 μsec. The maximum IGT is approximately 16 msec. that can be extended up to approximately 80 seconds, using the IGT counter value. The value in the word is added to this minimum time. The resolution of this word is 250 nsec. per bit.

3.3.3 Message Block Pointer

The Message Block pointer is a 16-bit word that the user writes to point to the beginning of a message block.

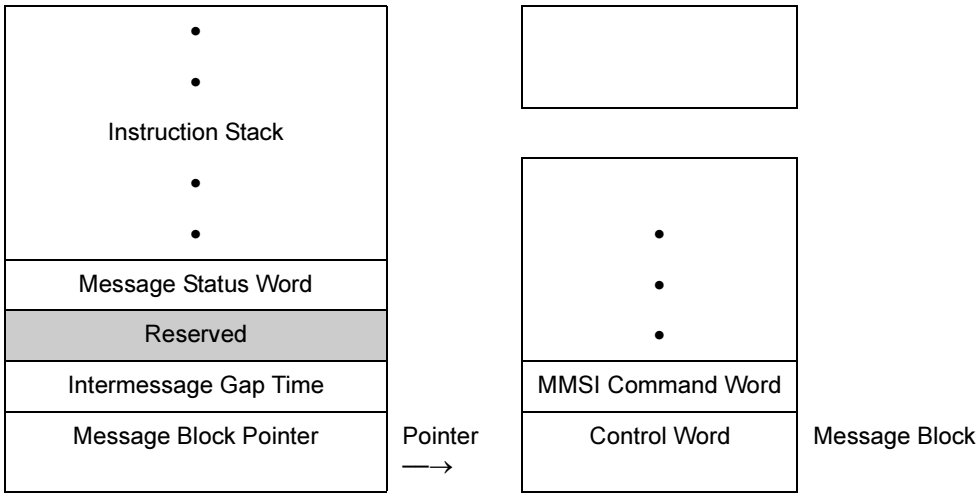


Figure 3-3 Message Block Pointer – BC/Concurrent-RT Mode

3.3.4 Message Block

The message block can be loaded anywhere in the Instruction Stack/Message Block area. (See **Figure 3-1 BC/Concurrent-RT Memory Map,** on page 3-3) Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers point to the message blocks in sequence.

Each block contains a MMSI message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the module which type of message to transmit (i.e. Mode code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats are illustrated in section **3.5 Message Block Formats,** see page 3-11.

For a description of each bit see section **3.3.5 Control Word** on page 3-7.

3.3.5 Control Word

Logic 1 enables the function, 0 disables the function.

Bit	Bit Name	Description
15	**Stop On Error**	Message error stops BC operation. Restart by writing to the Instruction Counter Register and issue a Start command.
14	**Parity Error**	Selects Even parity in Word. Also set bit 8
13	**Halt/Continue**	1 = Halt; stops BC transfer operation. 0 = Run or Continue.
12	**Word Count Error**	Transmits fewer or more words than are indicated by the Word Count field. (See **Word Count Register,** on page 3-20) This function is valid for BC-to-RT messages only.)
11	**Reserved**	
10	**Incorrect Sync**	Transmits incorrect Sync. Data type Sync is transmitted in the Command Word. Also set bit 8
09	**Int_On_Select_Msg**	1 = Generate an interrupt when this specific message is completed. To set general interrupt conditions, see **Interrupt Condition Register,** on page 3-17
08	**Error in Data**	Causes error injection to be performed in Data Words instead of Command Words where applicable
07	**1760 checksum error**	Injects an incorrect value as a checksum. Bit 06 must be set in order to set Chk_Sum_Err_Inj.
06	**1760 Checksum**	For BC-to-RT messages: generate a Checksum For RT-To-BC messages: Checks that the correct Checksum was transmitted
04 – 5	**Auto Retry Code**	On error, selects the number of retries before transferring the next message:

Bit 05	Bit 04	Description
0	0	No Retries
0	1	1 Retry
1	0	2 Retries
1	1	3 Retries

00 – 03 Command Code	03	02	01	00	Description
	0	0	0	0	Transmit Command (RT to BC)
	0	0	0	1	Receive Command (BC to RT)
	0	0	1	0	Reserved
	0	0	1	1	Mode Code
	0	1	0	0	Broadcast Receive Command
	0	1	0	1	Reserved
	0	1	1	0	Broadcast Mode code
	0	1	1	1	Skip Message [1]
	1	0	0	0	Jump Command [2]
	1	1	1	1	Minor Frame Command [3]

BC/Concurrent-RT Control Word

1. See **3.3.7 Skip Message** on page 3-8
2. See **3.3.8 Jump Command Operation** on page 3-8
3. See **3.3.9 Minor Frame Operation** on page 3-9

3.3.6 Halt Operation

Normally set the Halt Operation bit to logic 0 before writing to the Start Register. In realtime (during BC execution), the user sets this bit to logic 1. When operating on that particular message block's Control word, the module will halt transfer operations until the bit is reset to logic 0.

When the module detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status Register. (See **Message Status Register,** on page 3-18.) Use the Wait For Continue bit to find out when the module has arrived at the halted instruction block. When the module detects that the Halt bit (Continue Mode) has been reset, the module will reset the Wait For Continue bit in the Message Status Register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* yet been executed by the module.

Note: The Halt operation can be used in conjunction with the Jump command. See **Jump Command Operation.**

3.3.7 Skip Message

The Skip Message command allows the user to skip a message defined in a certain message block. To do so, modify the Command field in the Control Word. This lets the user selectively send a message in the current frame. The 'skip' takes place immediately and does not wait until the Intermessage Gap Time expires.

3.3.8 Jump Command Operation

The module's BC transfer cycle can be modified by setting the Jump command in the BC Control word. The Jump command instructs the module to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual MMSI Command Word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the module has tested the Halt/Continue bit in the Control word. The 'jump' takes place immediately and does not wait until the Intermessage Gap Time expires.

The memory structure of the jump command is illustrated below.

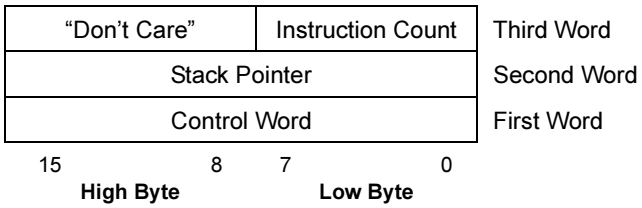


Figure 3-4 Jump Command Memory Structure

3.3.9 Minor Frame Operation

The Minor Frame type of message can be used in the following ways:

- To function as a "delay time" between groups of messages.
- To produce a list of messages that will be sent out over the bus at different frequencies.

Minor frame time is defined as the time elapsed from the beginning of a minor frame to beginning of the next minor frame. To set up minor frame operation, each minor frame must begin with a minor frame command. (See **Minor Frame Time Register** and **Minor Frame Time Multiplier Register,** on page 3-22.) The maximum value possible for the Minor Frame Time is 800 milliseconds.

Example: **Figure 3-5 Minor Frame Sequencing** shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 msec. long, Message A is sent every 10 msec., Message B is sent every 20 msec., and Message C is sent every 40 msec.

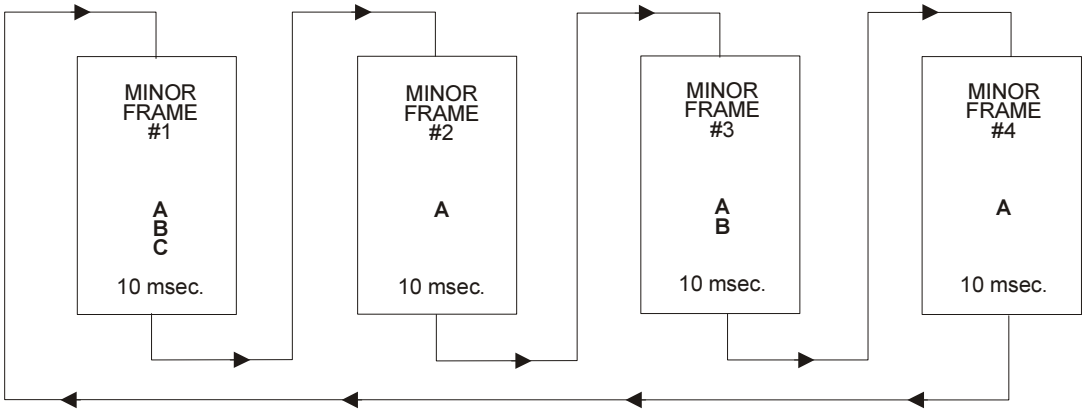


Figure 3-5 Minor Frame Sequencing

Notes:

1. The MINOR_FRAME message does not appear as a real message on the data bus.
2. Frame Time should not exceed the total time of all the minor frames in the minor frame sequence. (See **Frame Time Hi Register,** on page 3-21.)

3.4 Remote Terminal Simulation

When the module is simulating both the Bus Controller and one or more Remote Terminals, the user must write the simulated Remote Terminal Status Word and Data Word(s) into the message block in the sequence in which they are to be transmitted over the bus. (See section **3.5 Message Block Formats** on page 3-11.)

Note: The rules for the RT Status Word **do not** apply when simulating an RT: the user must provide the message Status Word; insert the 1760 header in the data; error injections and interrupts related to RTs are *not* available. (See section **2.5 RT Status Word** on page 2-7.)

The **Service Request bit [SRQ]** is not supported in RT simulation.

To indicate to the module, which Remote Terminals are to be simulated, write to the Active Remote Terminal table. Each entry in the table corresponds to a specific Remote Terminal. The first byte is for RT #0, the second is for RT #1, and so on. A table entry value of 1 enables the Remote Terminal simulation by the module; a value of 0 disables the simulation by the module.

The *M4KMMSI* has eight ports to communicate with eight RTs. However, the RT numbers of these eight RTs can be any eight numbers from 0 – 30. To calculate which port an RT corresponds to, use RT# MOD 8. So RTs 0 – 7 use ports 0 – 7, RT #8 uses Port 0, RT #9 uses Port 1, and so on. You cannot use two RT numbers that use the same port, for example, RT #0 and RT #8.

RT#31 Broadcast byte	32nd byte	341F H	
RT#30 Active RT byte	31st byte	341E H	This RT uses Port 6
• • •	• • •	• • •	• • •
RT#24 Active RT byte	25th byte	3418 H	This RT uses Port 0
• • •	• • •	• • •	• • •
RT#16 Active RT byte	17th byte	3410 H	This RT uses Port 0
• • •	• • •	• • •	• • •
RT#8 Active RT byte	9th byte	3408 H	This RT uses Port 0
• • •	• • •	• • •	• • •
RT#0 Active RT byte	1st byte	3400 H	This RT uses Port 0

Figure 3-6 Active RT Table – BC/Concurrent RT mode

Bit	Description
01 – 07	Reserved – set to 0
00	1 = Enabled 0 = Disabled

Active RT Byte Definition – BC/Concurrent RT mode

3.5 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire message as it appears on the bus, including MMSI Command Word(s), Data Word(s), and Status Word(s). Examples of Message block formats are:

Example 1 Example No. 1 – Transmit Command Operating as BC Only

Block *before* execution

Transmit Command	
Control Word	First Location in Block

Block *after* execution

Data Word	First Transmitting Remote Terminal (not simulated)
•	•
•	•
Data Word	•
RT Status Word	First Transmitting Remote Terminal (not simulated)
Transmit Command	
Control Word	First Location in Block

Example 2 Receive Command Operating as Both BC and Receiving RT

Block *before* execution

RT Status Word	Simulated by *M4KMMSI* (Loaded by user)
Data Word	•
•	•
•	•
Data Word	Simulated by *M4KMMSI* (Loaded by user)
Receive Command	
Control Word	First Location in Block

Block *after* execution

RT Status Word	
Data Word	
•	
•	
Data Word	
Receive Command	
Control Word	First Location in Block

Figure 3-7 Message Block Formats

3.6 Continuous or One-Shot Message Transfers

The module can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

One-shot mode In One-Shot mode, after receiving a Start command, the module transfers all messages, sets the Message Complete bit in the Message Status Register, issues an interrupt (if programmed), turns off bit 00 of the Start Register, and waits for a new Start command. Use the **Start Register,** on page 3-17 to select One-Shot mode.

n-Times mode In n-Times mode, load the Loop Count Register with the number of times to transmit the messages (frame) and set the Loop and Start bits in the Start Register. The user can transmit messages from 1 to 255 times. (See **Start Register,** on page 3-17 and **Loop Count Register,** on page 3-19.) The **Frame Time Registers**, on 3-22, determine the time between frames.

Continuous Loop mode In Continuous Loop mode, the module will retransmit the message frame at a predetermined, user-programmable rate. Use the **Start Register,** on page 3-17 and **Loop Count Register,** on page 3-19, to select Continuous Loop mode. In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the module's operation by clearing bit 00 of the Start Register.

The Loop time or Frame time is set via the Frame Time Hi and Frame Time Lo registers. These registers, taken as a 32-bit quantity represent the time in microseconds from the beginning of a frame to the beginning of the following frame.

Note: If the Frame Time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 10 μsec, measured as dead time on the bus.

3.7 Service Request [SRQ] Processing

The SRQ bit is set by an RT in the **RT Status Word** (see 2-7). Setting the SRQ bit indicates to the BC that the RT/Subaddress requires servicing.

The BC provides the following service:

1. The module will send out a Mode Code 16 (transmit Vector Word) to get the Vector Word from the RT which contains more information about what needs service. This message is stored in SRQ Message 1 [3F80-3F87 (H)], See **SRQ Message 1 Register,** on page 3-23.
2. The BC will then send out a transmit message to the Subaddress (provided that it is not set to 0) identified in the Vector Word. This message is stored in SRQ Message 2 [3F88-3FCD (H)], See **SRQ Message 2 Register,** on page 3-22.

   See section **2.9 RT Vector Words** on page 2-11.
3. If the interrupt SRQ message bit is set in the Interrupt Condition Register (see **Interrupt Condition Register**, on 3-17) an interrupt will be generated when the BC completes steps 1 and 2.
4. The SRQ Counter is incremented by 1. See **SRQ Counter,** on page 3-22.

To disable Service Request processing set Bit 01 in the **BC Protocol Options Register,** on page 3-25.

3.8 MIL-STD-1760 Features

3.8.1 1760 Header Word

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific Subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Transmit/Receive Value table to the value you expect to receive in the first Data Word of the message. The Header value expected is either the predefined 1760 value, which is the default *M4KMMSI* setting, or another value the user enters in the 1760 Header Value Transmit/Receive Table.

For descriptions of the **1760 Header Value Transmit/Receive Tables** and **1760 Header Exist Table**, see 3-23.

3.8.2 1760 Checksum Error

The 1760 option implements checksum generation and checksum error detection capabilities. Checksums are computed as each Data Word is sent or received. If the checksum flag is set on an outgoing message, the checksum will be sent in place of the last Data Word. On an incoming message, the computed checksum is checked against the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status Word.

The user gets to select, per message to generate or check received Checksums in the Message Control Word. See **3.3.5 Control Word,** on page 3-7, bit 06.

If Checksum is selected the user may also request that the Checksum be sent out with an incorrect value as an error injection mechanism. See **3.3.5 Control Word,** on page 3-7, bit 07.

3.9 Control Register Definitions

3.9.1 Instruction Stack/Message Block Area

Address: 7100 – 7FFF (H)

This area is available to the programmer for Instruction Stacks and Message Blocks.

3.9.2 Time Tag Counter

Address: 7008 – 700B (H)

Read only

The Time Tag is a free-running 32-bit counter on the module. The Time Tag is reset to 0 upon a power up or a software reset and starts counting.When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset Register.

The user may read the Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

THE COUNTER MUST BE READ IN THE FOLLOWING SEQUENCE:

1. Read 7008 H - Lo word (16 bit, read only)
2. Read 700A H - Hi word (16 bit, read only)

The Time Tag resolution is 4 μsec.

TO CALCULATE ELAPSED TIME BETWEEN TIME TAGS

Example:

1. Calculate difference between Time Tags:
   150 [Time Tag 2] – 50 [Time Tag 1] = 100
2. Elapsed time:
   100 × 4 = 400 μsec

3.9.3 Time Tag Reset Register

Address: 7007 (H)

Write only

Write to the Time Tag Reset Register to reset the module's Time Tag Counter (data field = "don't care"). Immediately after the reset, the counter will start to count from 0.

3.9.4 Module Reset Register

Address: 7000 (H)

Write only

Write any value to the Module Reset Register to reset the module.

Module Reset erases all locations in the dual-port RAM. Module status, module ID and Firmware registers are written by the module after the reset operation is completed.

3.9.5 Module Configuration Register — Address: 3FFF (H)

Before issuing a Start command to the module, set the operating mode of the module via the Module Configuration Register.

To modify the Module Configuration Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

Bit	Description
00 – 07	04 (H) = BC/Concurrent-RT mode

Module Configuration Register

3.9.6 Module ID Register — Address: 3FFE (H)

The Module ID Register contains a fixed value that can be read by your initialization function to detect the presence of the module. The one-byte value of this register is 45 (H), ASCII value E.

3.9.7 Module Status Register — Address: 3FFD (H)

The Module Status Register indicates the status of the module. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Module type is *M4KMMSI*
05 – 06	X "Don't Care"
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit is cleared in the Start Register. Following this, the module sets bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start Register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic 1.

3.9.8 Start Register

Address: 3FFC (H)

The Start Register controls the Start/Stop operation of the module. Writing the appropriate bit (bit 00) to the Start Register starts the Bus Controller transfer operation. When operating in Continuous Loop or *n*-Times mode, the user must set the Start and Loop bits in the Start Register. The Loop and *n*-Times number are selected via the Loop Count Register. In the One-Shot and *n*-Times modes, the module resets the Start bit in the register after *all* messages have been transferred. The module does not reset any bit while in Continuous Loop mode. To halt the Loop operation between messages, set bit 00 to 0. In order to halt the operation at the end of the entire frame, set bit 02 to 0 (bit 02 is not tested between message transfers). Related data bit 04 in the Module Status Register indicates when the module has been halted. (See **Module Status Register,** on page 3-16.)

Bit	Description
03 – 07	0
02	1 = Loop Mode 0 = One-Shot Mode
01	0
00	1 = Start Operation 0 = Stop

Start Register

Note: The user can start concurrently by sending a low TTL pulse of 100 nsec. Minimum to the **EXSTRTn** pin. See section **7.4.1.1 M4KMMSI Module Terminal Stick and Adapter Cable Pinouts** on page 7-4.

3.9.9 Interrupt Condition Register

Address: 3FFB (H)

The Interrupt Condition Register allows the user to set interrupt triggers. When a condition occurs that is enabled in this register, an interrupt is generated. A logic 1 enables the interrupt condition. To determine which condition caused the interrupt, check the Message Status Register.

The Interrupt Condition Register must be set before issuing a Start command to the module. To modify the Interrupt Condition Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

Bit	Description
06 – 07	0
05	SRQ message
04	End Minor Frame
03	Message Error
02	End of Frame
01	Message Complete
00	0

Interrupt Condition Register

Note: The interrupt will be sent at the end of the message for all interrupt conditions.

3.9.10 Message Status Register

Address: 3FFA (H)

The Message Status Register indicates the status of the current message being processed. The definition of each status bit is given below. Logic 1 indicates that the condition is activated.

Bit	Bit Name	Description
06-07	Reserved	Set to 0
05	SRQ Message	An RT returned a Status with the SRQ bit set and the BC responded with a Vector mode code and Rt-to-BC message
04	End Minor Frame	A Trigger generated an interrupt on End of Minor Frame
03	Message Error	The message has been sent. As a result, the Error bit has been set in the Message Status Word.
02	End of Frame	The last word of the last message in the frame has been sent.
01	Message Complete	The last word of the message has been sent.
00	Wait For Continue	A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue.

Message Status Register

Note: Status bits are *not* reset by the module. After reading them, the user must reset them.

3.9.11 RT Response Time Register

Address: 3FF9 (H)

The RT Response Time Register sets the Response Time of the Remote Terminals being simulated by the module. The resolution of the Response Time Register is 50 nsec. per bit. The minimum time is approximately 1.25 μsec., which is achieved by writing a 0 to this register. Values from 1 to 25 have no affect. The actual response time has a tolerance of ± 1 μsec.

Set the Response Time Register before issuing a Start command to the module. To modify the RT Response Time Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17).

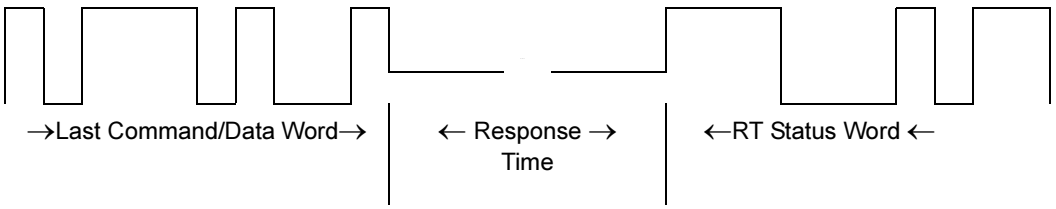


Figure 3-8 RT Response Time Definition

Example: To request a Response time of 4 μsec:
Write an 80 to the RT Response Time Register
80 × 0.50 nanoseconds = 4 μsec

3.9.12 Hub Mode Register

Address: 3FF8 H

The Hub Mode Register sets the appropriate Hub Mode for RT operation. For a description of the Hub Modes, see **1.4 MMSI Hub Modes** on page 1-6.

Bit	Description	Mode of Operation
02 – 07	Reserved (set to 0)	
00 – 01	Hub Mode	0 = Switch mode [**Default**] 1 = Link mode 2 = Spec mode

Hub Mode Register

Set the Hub Mode Register before issuing a Start command to the module. To modify the Hub Mode Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

3.9.13 Loop Count Register

Address: 3FF6 (H)

The Loop Count Register is used in conjunction with the Loop bit in the Start Register. If the Loop bit in the Start Register is set, then set the Loop Count Register to specify the number of times the Message frame will be transmitted. A value of zero is interpreted as a request for continuous looping.

Set the Loop Counter Register before issuing a Start command to the module. To modify the Loop Counter Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

Bit	Value	Description
00 – 07	**0**	Transmits in Continuous Loop
	1 – 255	Sends Message Frame n-times as defined

Loop Count Register

3.9.14 Word Count Register

Address: 3FF4 (H)

The Word Count Register controls the number of Data Words (±3) in the message and allows the user to inject a Word Count error. The error is an offset relative to the MMSI Command Word Word Count field. This register is used by the module only for messages for which the Word Count Error bit is set in the Control word register. (See section **3.3.5 Control Word,** see page 3-7.) If the Word Count Error bit is not set, a correct number of words is transmitted regardless of the contents of the Word Count Register.

Set the Word Count Register before issuing a Start command to the module. To modify the Word Count Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

Register Value	Word Count Offset
FD H	-3 Words
FE H	-2 Words
FF H	-1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Register Values

3.9.15 BC Response Time Register

Address: 3FF3 (H)

The BC Response Time Register sets the BC's Response Time window, whose value determines the maximum wait time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time Register is 50 nsec. per bit, The minimum time window is approximately 2 μsec., the maximum is 12 μsec. The specification allows responses between 1 and 4 μsec.

The BC Response Time Register must be set before issuing a Start command to the module. To modify the BC Response Time Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

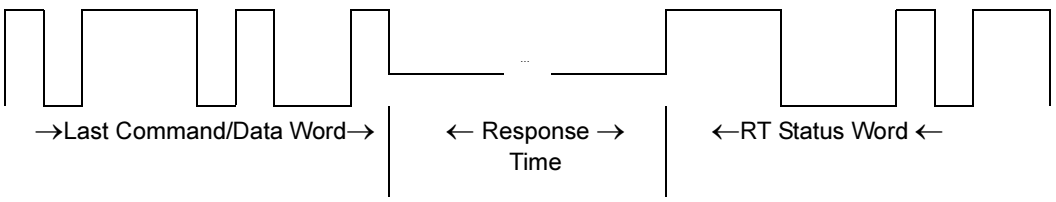


Figure 3-9 BC Response Time Definition

Example: To request a Response time of 6 μsec:
Write 120 to the BC Response Time Register
120 × 50 nano ≅ 6 μsec

3.9.16 Message Stack Pointer

Address: 3FF0 – 3FF1 (H)

The Message Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 – 33FF (H), 4000 – 6FFF (H) and 7100 – 7FFF (H).

The Stack Pointer Register must be set before issuing a Start command to the module. To modify the Stack Pointer Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17)

3.9.17 Frame Time Lo Register

Address: 3FEE – 3FEF (H)

The Frame Time Lo Register contains the low 16 bits of the Frame Time value for Continuous and *n*-Times modes operation. The resolution of this register is 4 μsec. per bit.

Set the Frame Time registers before issuing a Start command to the module. To modify the Frame Time registers, issue a Stop command, modify the register, then issue a Start command. (See **Start Register,** on page 3-17.)

3.9.18 Frame Time Hi Register

Address: 3FEC – 3FED (H)

The Frame Time Hi Register contains the high 16 bits of the Frame Time value for Continuous and *n*-Times modes operation.

Set the Frame Time registers before issuing a Start command to the module. To modify the Frame Time registers, issue a Stop command, modify the register, then issue a Start command. (See **Start Register,** on page 3-17.)

3.9.19 Instruction Counter

Address: 3FEA – 3FEB (H)

The Instruction Counter must be loaded with the number of instructions (MMSI Messages) to execute in the current frame. The value must be greater than 0 before the user writes to the Start Register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The module updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

Set the Instruction Counter Register before issuing a Start command to the module. To modify the Instruction Counter Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.) When in Continuous Loop mode, the Instruction Counter Register cycles from the initial value down to 1.

3.9.20 Minor Frame Time Register

Address: 3FE8 – 3FE9 (H)

Write only

This 16-bit Minor Frame Time Register is used to set the length of a single minor frame. (See section **3.3.9 Minor Frame Operation,** see page 3-9.) The resolution of the Minor Frame Time Register is 1 μsec. per bit. The maximum value is approximately 65 msec., which can be extended by the multiplier set in the Minor Frame Time Multiplier Register.

Set the Minor Frame Time Register before issuing a Start command to the module. To modify the Minor Frame Time Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

3.9.21 Minor Frame Time Multiplier Register

Address: 3FE6 – 3FE7 (H)

Write only

The Minor Frame Time Multiplier Register is a multiplier of the Minor Frame Time Register described above. The value written by the user to the Minor Frame Time Multiplier Register allows the user to extend the Minor Frame Time beyond the 65 msec. maximum in the Minor Frame Time Register. The maximum Minor Frame Time Multiplier is 255. The maximum Minor Frame Time possible using both registers is approximately 800 milliseconds.

Example: To generate a Minor Frame Time of 1 sec., set the Minor Frame Time Register to F424 (H) [62,500 Dec.], and set the Minor Frame Time Multiplier Register to 10 (H) [16 Dec].

Set the Minor Frame Time Multiplier Register before issuing a Start command to the module. To modify the Minor Frame Time Multiplier Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 3-17.)

3.9.22 SRQ Counter

Address: 3FD2 – 3FD3 (H)

The SRQ counter contains the number of messages processed since BC was run.

3.9.23 SRQ Message Status Register

Address: 3FCE – 3FD1 (H)

The SRQ Message Status Register contains the SRQ Message 1 at 3FCE (H) and SRQ Message 2 at 3FD1H).

3.9.24 SRQ Message 2 Register

Address: 3F88 – 3FCD (H)

The SRQ Message 2 Register contains the Transmit message sent to the Subaddress identified in the Vector word received from SRQ processing. The message consists of:

Control Word	Command Word	Status Word	Up to 32 Data Words

3.9.25 SRQ Message 1 Register

Address: 3F80 – 3F87 (H)

The SRQ Message 1 Register contains the Transmit vector mode code message sent out by the BC in response to SRQ by an RT. The message consists of:

Control Word	Command Word	Status Word	Vector Word

3.9.26 1760 Header Value Transmit Table

Address: 3F40 – 3F7F (H)

Write to the 1760 Header Value Transmit table to set the expected value of the first Data Word in a RT-to-BC message. If the wrong data was sent, the Concurrent Monitor will send an error message.

The 1760 option provides predefined values, and these are preset on the *M4KMMSI* module. The user can change the preset values.

Transmit Subaddress	Header Value [Hex]	Address
1	**0421**	3F42 H
11	**0420**	3F56 H
14	**0423**	3F5C H

Predefined 1760 Transmit Header Values

3.9.27 1760 Header Value Receive Table

Address: 3F00 – 3F3F H

Write to the 1760 Header Value Receive table to set the expected value of the first Data Word in a BC-to-RT message. The monitor checks that the specified header value was received. If the wrong data was sent, the 1760 Header Error bit is set in the **Message Status Word**, see page 3-5.

The 1760 option provides predefined values, and these are preset on the *M4KMMSI* module. The user can change the preset values.

Receive Subaddress	Header Value [Hex]	Address
11	**0400**	3F16 H
14	**0422**	3F1C H

Predefined 1760 Receive Header Values

3.9.28 1760 Header Exist Table

Address: 3EC0 – 3EFF (H)

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the module should expect a header word for RT-to-BC messages directed to that Subaddress.

For those Header Value Table entries for which MIL-STD-1760 provides predefined values, the corresponding Header Exist Table entries are preset on the *M4KMMSI* module.

To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value [Transmit/Receive] Table.

Bit	Description
09-15	Reserved
08	1 = Module should expect a Header word in a transmit message (RT-to-BC) 0 = Module should **not** expect a Header word in a transmit message
01-07	Reserved
00	1 = Module should expect a Header word in a receive message (BC-to-RT) 0 = Module should **not** expect a Header word in a receive message

1760 Header Exist Table

Subaddress	Header Value [Hex]	Address
1	**0100**	3EC2 H
11	**0101**	3ED6 H
14	**0101**	3EDC H

Predefined 1760 Headers

3.9.29 Serial Number Register

Address: 3EA0 – 3EA1 (H)

The Serial Number Register holds the board's serial number, which is stored in non-volatile flash memory and loaded at power-up. The value is binary coded. For example, a value of 1234 (H) represents the serial number 4660.

3.9.30 BC Protocol Options Register

Address: 3E8C – 3E8D (H)

Set the BC Protocol Options Register to enable or disable Service Request processing.

Bit	Description
02–15	Reserved
01	1 = No special processing takes place when a Status Word with the SRQ bit set is received
	0 = See section **3.7 Service Request [SRQ] Processing,** on page 3-13
00	Reserved

BC Protocol Options Register

3.9.31 Send Time Tag on Sync Register

Address: 3E8A – 3E8B (H)

Set the Send Time Tag on Sync Register to indicate that the module should send the current Time Tag value (with a resolution of 64 μsec.) as the 16-bit Data Word upon transmitting a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

3.9.32 Clear Time Tag on Sync Register

Address: 3E88 – 3E89 (H)

Set the lower bit [3E88 (H)] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag registers [7008 – 700B (H)] (reset to 0) upon the transmission of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Set the higher bit [3E89 (H)] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag registers [7008 – 700B (H)] (reset to 0) upon the transmission of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

Note: This register setting does not effect until the module is restarted.

3.9.33 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision Register indicates the revision level of the on-module firmware. The value 18 (H) would be read as revision level: 1.8.

4 Bus Monitor Operation

Chapter 4 describes *M4KMMSI* operation in Bus Monitor mode. The topics covered are:

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4.1 Bus Monitor Mode Overview

The Bus Monitor can operate in one of two modes:

Sequential mode: Message Blocks are stored in sequential locations in memory. Sequential mode supports two types of operations:

Fixed-block operation: Messages are stored at fixed sequential blocks in the memory. Sequential Fixed Block mode supports Trigger capability
Linked-list operation: Messages are packed one after another in the memory, separated by a header.

Look-Up Table mode: Each message is stored in a unique Message Block. In Look-Up Table mode, the module addresses the user-programmable Look-up Table when it receives a MMSI Command Word. The Command Word's RT address, T/R bit, and Subaddress fields make up the 11-bit pointer to a Look-up Table with 2048 (2K × 8) locations.

Use the **Module Configuration Register,** on page 4-18, to program the desired mode of operation.

TO DETERMINE IF THE MODULE IS INSTALLED AND READY TO OPERATE:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID Register (test for value = 45 H).
2. Check the Module Status Register (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset Register.

Note: Throughout this manual, writing a '1' to the Start Register is referred to as issuing a Start command.

4.2 Sequential Fixed-block Memory Map

Reserved	700C – FFFF H		
Time Tag Hi	700A – 700B H		
Time Tag Lo	7008 – 7009 H		
Time Tag Reset Register	7007 H		
Reserved	7001 – 7006 H		
Module Reset Register	7000 H		
Reserved	4000 – 6FFF H	Reserved	3F80 – 3FEA H
Module Configuration Register	3FFF H	1760 Header Value Transmit Table [64 Bytes]	3F40 – 3F7F H
Module ID Register	3FFE H	1760 Header Value Receive Table [64 Bytes]	3F00 – 3F3F H
Module Status Register	3FFD H	1760 Header Exist Table [64 Bytes]	3EC0 – 3EFF H
Start Register	3FFC H	Reserved	3EB0 – 3EBF H
Interrupt Condition Register	3FFB H	Message Counter Lo	3EAE – 3EAF H
Message Status Register	3FFA H	Message Counter Hi	3EAC – 3EAD H
Reserved	3FF8 – 3FF9 H	Pretrigger Message Counter Lo	3EAA – 3EAB H
Time Tag Resolution Register	3FF6 – 3FF7 H	Pretrigger Message Counter Hi	3EA8 – 3EA9 H
Current Message Block Register	3FF5 H	Reserved	3EA2 – 3EA7 H
Block Trigger Value Register	3FF4 H	Serial Number Register	3EA0 – 3EA1 H
Trigger Word #1	3FF2 – 3FF3 H	Reserved	3E90 – 3E9F H
Trigger Mask #1	3FF0 – 3FF1 H	Monitor Response Time Reg.	3E8E – 3E8F H
Trigger Word #2	3FEE – 3FEF H	Reserved	3E81 – 3F8D H
Trigger Mask #2	3FEC – 3FED H	Firmware Revision Register	3E80 H
Trigger Control Register	3FEB H	Message Block Area [200 Blocks]	0000 – 3E7F H

Figure 4-1 Bus Monitor – Sequential Fixed-block Memory Map

4.3 Sequential Linked-list Memory Map

Reserved	700C – FFFF H		
Time Tag Hi	700A – 700B H		
Time Tag Lo	7008 – 7009 H		
Time Tag Reset Register	7007 H		
Reserved	7001 – 7006 H		
Module Reset Register	7000 H	1760 Header Value Transmit Table [64 Bytes]	3F40 – 3F7F H
Reserved	4000 – 6FFF H	1760 Header Value Receive Table [64 Bytes]	3F00 – 3F3F H
		1760 Header Exist Table [64 Bytes]	3EC0 – 3EFF H
Module Configuration Register	3FFF H	Reserved	3EB0 – 3EBF H
Module ID Register	3FFE H	Message Counter Lo	3EAE – 3EAF H
Module Status Register	3FFD H	Message Counter Hi	3EAC – 3EAD H
Start Register	3FFC H	Reserved	3EA2 – 3EAB H
Interrupt Condition Register	3FFB H	Serial Number Register	3EA0 – 3EA1 H
Message Status Register	3FFA H	Reserved	3E90 – 3E9F H
Reserved	3FF8 – 3FF9 H	Monitor Response Time Reg.	3E8E – 3E8F H
Time Tag Resolution Register	3FF6 – 3FF7 H	Reserved	3E81 – 3E8D H
End Buffer Pointer	3FF4 – 3FF5 H	Firmware Revision Register	3E80 H
Next Message Pointer	3FF2 – 3FF3 H	Message Block Spill Area	3E00 – 3E7F H
Reserved	3F80– 3FF1 H	Message Block Area	0000 – 3DFF H

Figure 4-2 Bus Monitor – Sequential Linked-list Memory Map

4.4 Sequential Mode Message Block Area

The Sequential Mode Message Block area is partitioned into either blocks of fixed length or into a linked-list of blocks of varying lengths. The **Module Configuration Register,** on page 4-18, determines the type of partitioning.

For a description of the Time Tag function, see section **4.9 Time Tag Word,** on page 4-11.

4.4.1 Message Block Fixed-Block Operation

In Fixed-Block operation, the Message Block area is divided into 200 blocks of 80 bytes each. The first block starts at address 0000 (H), the second at 0050 (H), the third at 00A0 (H), etc. The Trigger option can be used only in Sequential mode with Fixed-Block operation. (See section **4.11 Trigger Operation,** on page 4-12.)

Information is stored in the memory in the following sequence	Byte offset
Data Word	•
•	•
•	•
•	•
Data Word	+8
MMSI Command Word	+6
Time Tag Hi	+4
Time Tag Lo	+2
Message Status Word	0

Figure 4-3 Bus Monitor Message Block – Fixed-block Operation

4.4.2 Message Block Linked-list Operation

In Linked-list operation, the Message Block area is divided into a linked list of message blocks. The length of each message block varies according to message size. The first two locations in each block comprise the message header. This header contains the address of the next Message Block header. The header of the last block received contains *xx*FF (End of File), indicating that there are no more messages stored. After a message is processed and stored in memory, the header of the preceding message block is updated from *xx*FF to the address (of the header in the block) of the newly stored message.

The linked-list method can store more data than Fixed-Block operation.

The buffer never wraps around in the middle of a message. When the buffer is full, or if there is no room left to store the entire next message, the next message will be stored in the first location of the Message Block Area [0000 (H)]. The header of the last message will point to that location in the Message Block Area. In this special case, to know exactly where the message ends, use the **End Buffer Pointer**. The End Buffer Pointer points to the address after the last location of the message, indicating the length of the message.

Figure 4-4 illustrates the contents of the Message block. For a description of the Time Tag function, see section **4.9 Time Tag Word,** on page 4-11.

Information is stored in the memory in the following sequence:	Byte Offset
End Of File: XXFF	•
Data Word	•
•	•
•	•
•	•
Data Word	+A
MMSI Command Word	+8
Time Tag Hi	+6
Time Tag Lo	+4
Message Status Word	+2
Message Header - Address of Next Block	0

Figure 4-4 Bus Monitor Message Block – Linked-list Operation

4.5 Look-up Table Mode Memory Map

Reserved	700C – FFFF H		
Time Tag Hi	700A – 700B H	Reserved	3F80 – 3FF1 H
Time Tag Lo	7008 – 7009 H		
Time Tag Reset Register	7007 H		
Reserved	7001 – 7006 H	1760 Header Value Transmit Table [64 Bytes]	3F40 – 3F7F H
		1760 Header Value Receive Table [64 Bytes]	3F00 – 3F3F H
Module Reset Register	7000 H	1760 Header Exist Table [64 Bytes]	3EC0 – 3EFF H
Reserved	4800 – 6FFF H	Reserved	3EB0 – 3EBF H
Data Block Look-up Table [2K × 8]	4000 – 47FF H	Message Counter Lo	3EAE – 3EAF H
Module Configuration Register	3FFF H	Message Counter Hi	3EAC – 3EAD H
Module ID Register	3FFE H	Reserved	3EA2 – 3EAB H
Module Status Register	3FFD H	Serial Number Register	3EA0 – 3EA1 H
Start Register	3FFC H	Reserved	3E90 – 3E9F H
Interrupt Condition Register	3FFB H	Monitor Response Time Register	3E8E – 3E8F H
Message Status Register	3FFA H	Reserved	3E81 – 3E8D H
Reserved	3FF8 – 3FF9 H		
Time Tag Resolution Register	3FF6 – 3FF7 H	Firmware Revision Register	3E80 H
Reserved	3FF4 – 3FF5 H	Message Block Area	0000 – 3FE7 H
Last Block Register	3FF2 – 3FF3 H		

Figure 4-5 Bus Monitor Look-up Table Mode Memory Map

4.6 Look-up Table Mode

In Look-up Table mode, the module can store 128 unique messages by using a 2K × 8 Look-up Table in on-module memory. Each byte in the table is divided into a 7-bit block number and an Interrupt Select bit, as described below. Data Block numbers (0 – 127 decimal) each consisting of 80 bytes are loaded into the table. The first block starts at address 0, the second at 50 (H), etc. Set the Interrupt Select bit to specify which messages will set the interrupt flag. The Interrupt Condition Register must also be programmed.

Bit	Description
07	1 = Interrupt Select bit is enabled
00 – 06	Block Numbers (0 – 127)

Look-up Table Byte Structure

When a Message is received, the Command Word's RT address, T/R Bit, and Subaddress fields are used as an 11-bit index to the Look-up Table. This index is used to extract the Data block number from the Look-up Table.

Base Address	RT address (5 bits)	T/R (1 bit)	Sub-address (5 bits)	Look-up table (2K x 8)	Data block	Hex address of Data Block
	11 most significant bits of the MMSI Command Word					
4000+	11111	1	11111	Block #	Data Block 127	27B0
	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
4000+	00000	0	00011	Block #	Data Block 3	00F0
4000+	00000	0	00010	Block #	Data Block 2	00A0
4000+	00000	0	00001	Block #	Data Block 1	0050
4000+	00000	0	00000	Block #	Data Block 0	0000

Figure 4-6 Look-up Table

TO CREATE THE ADDRESS TO THE TABLE

1. Isolate the eleven (most significant) bits of the MMSI Command Word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example: To allocate a data block for a receive message to RT#5, Subaddress #3.

RT Address #5			T/R #0 (Rcv)				Subaddress #3				
0	0	1	0	1	0	0	0	0	1	1	LSB

Hex representation = 143 (H)

2. Add the hex value of this part of the Command Word to the base address of the Look-up table [4000 (H)].

4000	(H)
+ 143	(H)
4143	(H)

3. Write the data block number to this location. Each data block, beginning at address 0000 is 80 bytes long (for up to 32 Data words). The address of a block is obtained by multiplying its block number by 80 (50 (H)).

The block addresses are calculated as follows:

- Block 0 is located at location 0000 (H).
- Block 1 is located at location 0050 (H).
- Block *n* is located at location *n* x 50 (H).

To identify the location of the current, or last, message, use the Last Block Register. The Last Block Register is updated at the end of each message reception. See **Last Block Register,** on page 4-21.

4.7 Look-up Table Mode Message Block Area

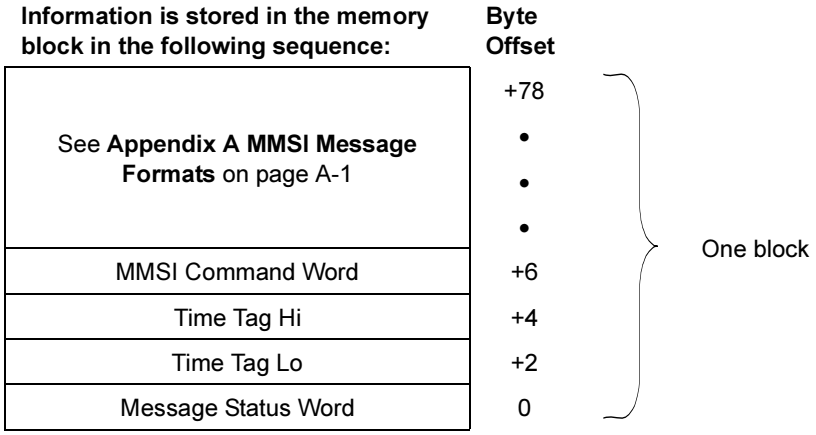


Figure 4-7 Look-up Table Mode Block Structure

4.8 Message Status Word

The Message Status Word is identical for all Bus Monitor modes. The Message Status Word indicates the status of the message transfer. The module creates this Word. Do not confuse it with the Status Word. (See section **2.5 RT Status Word,** on page 2-7.) The contents of the Message Status Word are:

Bit	Bit Name	Description
15	End of Message	Message transfer completed.
14	Trigger Found	Trigger message was received and stored. This status is valid for Sequential Fixed-Block mode with the following modes: **Store After** mode: the Trigger Found bit will be set only in the *first* Trigger message. **Store Only** mode: the Trigger Found bit will be set in *every* Trigger message. (See section **4.11 Trigger Operation,** on page 4-12)
13	Reserved	
12	Message Error Bit	Message Error bit (bit 10) in the RT Status Word was set.
11	RT Status Bit	A bit other than the Message Error bit in the RT Status Word was set. The Error Bit is *not* set in conjunction with this bit.
10	Invalid Message	Message-level error occured [Word Count, Incorrect Sync, etc.] Examine the other bits in this table to determine which error occurred.
09	Checksum Error	The computed checksum (on the incoming message) does not match when checked against the last Data Word received. (See section **4.10 MIL-STD-1760 Features,** on page 4-11)
08	Reserved	
07	Invalid Word Received	At least one invalid Word received (i.e. bit count, Manchester code, parity).
05 – 06	Word Count/ Header Error	**Bit 06** / **Bit 05** / **Description**: 0 / 0 / Reserved 0 / 1 / Low Word Count Error 1 / 0 / High Word Count Error 1 / 1 / 1760 Header Error – Header Word received does not match the value set in the Header Value Table.
04	Incorrect RT Address	Received Status Word did not contain the correct RT address.
03	Incorrect Sync Received	Sync of either the Status or the Data Word(s) is incorrect.
02	Non-Contiguous Data	Invalid gap between received Words.
01	Response Time Error	Response Time error occurred in the message.
00	Error	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word

Note:

- The Message Status Word is valid only when bit 15, End of Message, is turned on.
- When the module completes receiving a message over the bus, it writes the Message Status Word for this message in its message storage location. The module then zeros out the Message Status Word in the next message storage location, in preparation for receiving the next message over the bus.

4.9 Time Tag Word

In all Bus Monitor modes, each incoming message is stored with a Time Tag value. The Time tag value is a free-running 32-bit counter on the module. The Time Tag is reset to 0 upon power-up or a software reset and starts counting. When it reaches the value of FFFF FFFF (H) the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset Register. (See **Time Tag Reset Register,** on page 4-17)

The Time Tag value can be used to determine the time elapsed between messages. The Time tag counter's resolution is fixed at 4 μsec. per bit.

The Time Tag counter's value is written to the dual-port RAM during the reception of the (first) command of each message.

Note: In addition to reading the Time Tag value in the message stack, you can also read the counter's value at any time in the Time Tag counter. See **Time Tag [Hi & Lo],** on page 4-17.

4.10 MIL-STD-1760 Features

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Transmit/Receive Value table to the value you expect to receive in the first Data Word of the message. The Header value expected is either the predefined 1760 value, which is the default *M4KMMSI* setting, or another value the user enters in the 1760 Header Value Transmit/Receive Table.

For descriptions of the **1760 Header Value Transmit/Receive Tables** and **1760 Header Exist Table** see 4-22.

4.11 Trigger Operation

TRIGGERS ARE SUPPORTED ONLY IN SEQUENTIAL FIXED-BLOCK MODE

A trigger is a filter that the user can set to tell the module when and how to store messages. The module can be programmed to store messages in the following ways:

TRIGGER ACTION:

Store All	Stores all messages, without regard to triggers; no triggers are active
Store Only	Stores only messages that meet the trigger condition
Store After	Stores only the trigger message and messages that come after the trigger message

Triggering is done based on a **Trigger Source**. The possible sources are:

- **MMSI Command Word**
- **Message Status Word**

One or two triggers may be defined. Each trigger specifies a condition of the trigger source, which if it is fulfilled, will cause the **Trigger Action** to occur. Only one trigger source can be defined for the two triggers.

When two triggers are specified, if *either* of the trigger conditions is true, the trigger action will occur. Each trigger is defined using two registers:

- **Trigger Word Registers (1 and 2)**
- **Trigger Mask Registers (1 and 2)**

Use the Trigger Word Register to define a particular MMSI Command Word or a Message Status Word as a trigger. See **Trigger Word Registers (1 and 2),** on page 4-13.

The Trigger Mask Register defines which bits of the trigger word (defined in the Trigger Word Register) are relevant and which can be ignored (“don’t care”). The Trigger Mask registers must be defined when using the trigger function. See **Trigger Mask Registers (1 and 2),** on page 4-14.

Set the Trigger Control Register to specify the following trigger conditions:

- Trigger source (MMSI Command Word or Message Status Word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

See **Trigger Control Register,** on page 4-15.

Set the Trigger Word, Trigger Mask and Trigger Control registers before issuing a Start command to the module. To modify these registers, set the Initialize bit in the Start Register to 10 (H), modify the Trigger Word, Trigger Mask and Trigger Control registers, then issue a Start command 81 (H).

4.11.1 Trigger Word Registers (1 and 2)

Address: **Word 1 3FF2 – 3FF3 (H)**
Word 2 3FEE – 3FEF (H)

Use the Trigger Word Register to define a particular MMSI Command Word or a Message Status Word as a trigger. Load these locations (illustrated below) with the desired MMSI Command Word or Message Status Word, which will be used as the trigger source.

The user must also define the Trigger Mask registers when using the trigger function:

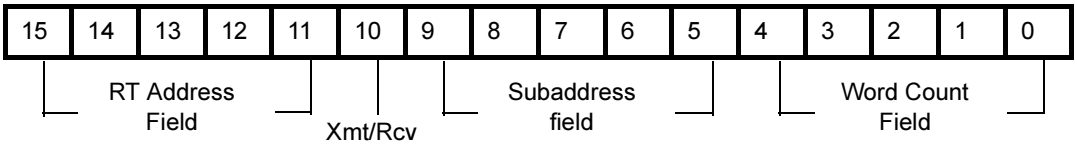
For:	Define:
Trigger Word 1 [3FF2 – 3FF3 H]	Trigger Mask 1 [3FF0 – 3FF1 H]
Trigger Word 2 [3FEE – 3FEF H]	Trigger Mask 2 [3FEC – 3FED H]

See **Trigger Mask Registers (1 and 2),** on page 4-14.

To define which trigger is to be active (Trigger #1, Trigger #2, or both) use the Trigger Control Register. (See **Trigger Control Register,** on page 4-15.)

USING THE MMSI COMMAND WORD – TRIGGER WORD REGISTERS

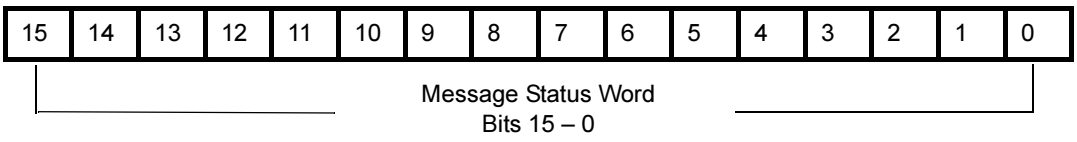
Use a MMSI Command Word as a trigger when it is necessary to filter messages based on information found in the Command Word. For example, to filter messages from a particular RT, or with a particular Word Count, set the Trigger Word Register with those parameters defined in the MMSI Command Word.



USING THE MESSAGE STATUS WORD – TRIGGER WORD REGISTERS

Use a Message Status Word as a trigger when it is necessary to filter messages based on information found in the Message Status Word. Do not confuse the Message Status Word with the Status Word. (See section **2.5 RT Status Word,** on page 2-7.) To filter error messages, set the Trigger Word Register with those parameters defined in the Message Status Word.

For an explanation see **4.8 Message Status Word,** on page 4-10.



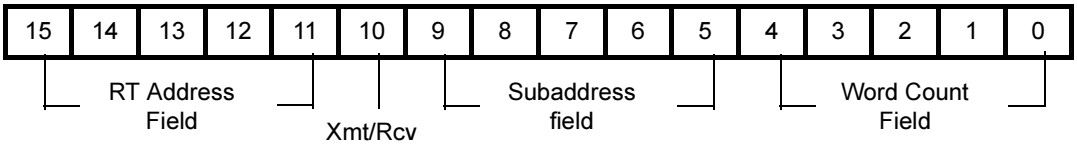
4.11.2 Trigger Mask Registers (1 and 2)

Address: Word 1 3FF0 – 3FF1 (H)
Word 2 3FEC – 3FED (H)

Set the Trigger Mask Register to define which bits of the trigger word (defined in the Trigger Word Register) are relevant and which can be ignored ("don't care"). The Trigger Mask registers must be defined when using the trigger function. All bits in this register should be set to 1, except for those bits you want to be "don't care" in the incoming Command Word or Message Status Word.

USING THE MMSI COMMAND WORD – TRIGGER MASK REGISTERS

After setting the Trigger Word Register with a MMSI Command Word, write 0s to the bits in the Trigger Mask Register that you want to be "don't care" in the MMSI Command Word trigger.

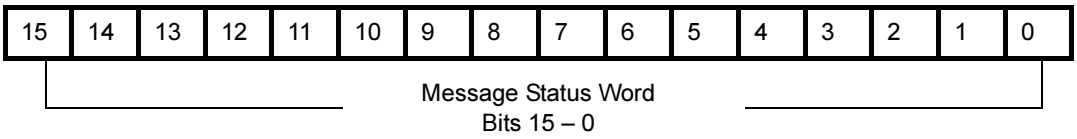


1 = Trigger on corresponding bit value in Trigger Word Register
0 = Corresponding bit value in Trigger Word Register is "don't care"

USING THE MESSAGE STATUS WORD – TRIGGER MASK REGISTERS

After setting the Trigger Word Register with a Message Status Word, write 0s to the bits in the Trigger Mask Register that you want to be "don't care" in the Message Status Word trigger.

For an explanation see **Message Status Word** on 4-10.



1 = Trigger on corresponding bit value in Trigger Word Register
0 = Corresponding bit value in Trigger Word Register is "don't care"

4.11.3 Trigger Control Register

Address: 3FEB (H)

The Trigger Control Register is relevant only in Sequential Fixed-Block mode. Set the Trigger Control Register to specify the following trigger conditions:

a. Trigger source (MMSI Command Word or Message Status Word)
b. Type of storage (Store All, Store Only, or Store After)
c. Active trigger word (Trigger Word #1 and/or #2). If both Trigger Words are active, if either condition a. or b. is met, the trigger will occur.

Note: Logic 1 enables the function.

Bit	Description
07	Trigger Source: 0 = MMSI Command Word 1 = Message Status Word
05 – 06	Reserved
04	1 = Store After
03	1 = Store Only
02	1 = Store All
01	1 = Enable Trigger Word #2
00	1 = Enable Trigger Word #1

Trigger Control Register

Example: Defining a Trigger

CONDITIONS:

- Define the Command Word 0825 (H) as Trigger word #1 (Receive Command for RT#1, Subaddress #1, and 5 words).
- Ignore the Word Count field.
- Use Trigger word #1 (Disable Trigger word #2).

PROCEDURE:

1. Set Trigger Word #1 Register to 0825 (H)
2. Set Trigger Mask #1 Register to FFE0 (H)
3. Set Trigger Control Register to 09 (H)

Note: To use trigger(s), at least one of the bits **Store All**, **Store Only**, or **Store After**, must be set.

4.12 Interrupts

Interrupts are supported in all three Bus Monitor modes.

4.12.1 Sequential Fixed-block Mode

There are various options for setting interrupts in Sequential Fixed-block mode, depending on the values set in the **Interrupt Condition Register**:

Bit Description	Bit No.	Set values in	Cause an Interrupt
Trigger Word Received	00	Trigger Word, Mask and Control registers[1]	Depending on the store condition set in the **Trigger Control Register**: Store Only — *Each* time the trigger word is received Store After — For all messages received *after* the *first* time the trigger is received
Message Complete	01		Each time any message is received
Block Trigger Match	02	Block number [0-199] in the Block Trigger Value Register	Set each time that block is updated [i.e. when the **Current Message Block Register** value equals the **Block Trigger Value Register**.]

1. See **4.11 Trigger Operation,** on page 4-12

4.12.2 Linked-list Mode

Set the **Interrupt Condition Register**, bit 01 [Message Complete]. An interrupt will occur each time any message is received.

4.12.3 Look-up Table Mode

An interrupt may be enabled or disabled for each block number assigned in the Look-up Table. Each byte in the table is divided into a 7-bit block and Interrupt Select bit. Set the Interrupt Select bit for the desired block. In addition, Set the **Interrupt Condition Register**, Bit 01[Message Complete]. This will cause an interrupt each time a message is received by those blocks that have the Interrupt Select bit set.

See section **4.6 Look-up Table Mode,** on page 4-8.

4.13 Control Registers Definitions

4.13.1 Time Tag [Hi & Lo]

Address: 700A – 700B (H)
7008 – 7009 (H)

Read only

The Time Tag is a free-running 32-bit counter on the module. The Time Tag is reset to 0 upon a power up or a software reset and starts counting. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting. To re-initialize to 0, write to the Time Tag Reset Register.

The user may read the Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

THE COUNTER MUST BE READ IN THE FOLLOWING SEQUENCE:

1. Read 7008 H - Lo word (16 bit, read only)
2. Read 700A H - Hi word (16 bit, read only)

The Time Tag Resolution Register sets the resolution of the counter.

TO CALCULATE ELAPSED TIME BETWEEN TIME TAGS

Example:

1. The Time Tag Resolution Register is set to 0. See **Time Tag Resolution Register,** on page 4-20
2. Calculate the Time Tag Resolution:
   [Time Tag Resolution Register value + 1] × 4 = [0 + 1] × 4 = 4 μsec
3. Calculate difference between Time tags:
   150 [Time Tag 2] – 50 [Time Tag 1] = 100
4. Elapsed time
   100 × 4 = 400 μsec

4.13.2 Time Tag Reset Register

Address: 7007 (H)

Write only

Write to the Time Tag Reset Register to reset the module Time Tag Counter (data field = “don’t care”). Immediately after the reset, the counter will start to count from 0.

4.13.3 Module Reset Register

Address: 7000 (H)

Write only

Write any value to the Module Reset Register to reset the module.

Module Reset erases all locations in the dual-port RAM. Module status, Module ID and Firmware registers are written by the module after the reset operation is completed.

4.13.4 Module Configuration Register

Address: 3FFF (H)

Before issuing a Start command to the module, set the operating mode of the module via the Module Configuration Register. To modify the Module Configuration Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 4-19.)

Bit	Description
00 – 07	08 (H) = BM Sequential Fixed-block mode 10 (H) = BM Sequential Linked-list mode 20 (H) = BM Look-up table mode

Module Configuration Register

4.13.5 Module ID Register

Address: 3FFE (H)

The Module ID Register contains a fixed value that can be read by your initialization routine to detect the presence of the module. The one-byte value of this register is: 45 (H), ASCII value E.

4.13.6 Module Status Register

Address: 3FFD (H)

The Module Status Register indicates the status of the module. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	
07	1 = Module type is *M4KMMSI*
05 – 06	X "Don't Care"
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit in the Start Register is cleared. Following this, the module sets bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start Register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic 1.

4.13.7 Start Register

Address: 3FFC (H)

The Start Register controls the Start/Halt operation of the module.

Bit	Bit Name	Description
01 – 07	**Reserved**	Set to 0
00	**Start/Halt**	1 = Start Operation 0 = Halt Operation

Start Register

Note: The user can start concurrently by sending a low TTL pulse of 100 nsec. Minimum to the **EXSTRTn** pin. See **7.4.1.1 M4KMMSI Module Terminal Stick and Adapter Cable Pinouts,** on page 7-4.

4.13.8 Interrupt Condition Register

Address: 3FFB (H)

Set the Interrupt Condition Register to enable interrupt triggers. When a condition enabled in this register occurs, an interrupt is generated. Logic 1 enables the interrupt condition. Check the Message Status Register to determine which condition caused the interrupt. (See **Message Status Register,** on page 4-20.)

Set the Interrupt Condition Register before issuing a Start command to the module. To modify the Interrupt Condition Register, issue a Stop command, modify the register, then issue a Start command (See **Start Register,** on page 4-19.)

Note: For all interrupt conditions, the interrupt will be sent at the end of the message.

Bit	Description
03 – 07	0
02	1 = Block Trigger Match (Valid Only in Sequential Fixed-block mode)
01	1 = Message complete (Valid in All Modes)
00	1 = Trigger Word Received (Valid Only in Sequential Fixed-block mode)

Interrupt Condition Register

4.13.9 Message Status Register

Address: 3FFA (H)

The Message Status Register indicates the status of the current message being processed. Each status bit is described in the table below. Logic 1 indicates that the condition is activated.

Bit	Description
03 – 07	0
02	1 = Block Trigger Match
01	1 = Message Reception In Progress
00	1 = Trigger Word Received - **Sequential Fixed-block mode** *or* Trigger Word Busy - **Linked-list and Look-up table mode** The busy bit is set when the module is processing a message. It is set together with message reception in progress, but is reset approximately 5 msec. after the end of each message. For consecutive messages with short intermessage gap times, the busy bit may not be reset between messages.

Message Status Register

Note: Status bits are not reset by the module. They must be reset after reading them.

4.13.10 Time Tag Resolution Register

Address: 3FF6 – 3FF7 (H)

The 16-bit value in the Time Tag Resolution Register represents the resolution of the Time Tag Counter in units of 4 μsec.

To determine the Time Tag Counter's resolution, use the following equation:

= (Time Tag Resolution Register value + 1) × 4 μsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution Register before issuing a Start command to the module. To modify the Time Tag Resolution Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 4-19.)

4.13.11 Current Message Block Register

Address: 3FF5 (H)

Sequential Fixed-block mode only

Read the Current Message Block Register to determine the Current Message Block number (0 – 199). The value is incremented by the module as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* message transfer operation. To determine the arrival of the first message, check the Message Status Word of the *first* Message block. The End of Message bit (bit 15) in the Message Status Word will be set.

4.13.12 Block Trigger Value Register

Address: 3FF4 (H)

Sequential Fixed-block mode only

Set the Block Trigger Value Register to a block number (0 – 199). This will set a bit in the Message Status Register each time that a block is updated, i.e. when the Current Message Block value equals the Block Trigger Value Register. It will also cause an interrupt each time that block is updated if in the Interrupt Condition Register bit 02 (Block Trigger Match) is set. (See **Interrupt Condition Register,** on page 4-19.)

Set the Block Trigger Value Register before issuing a Start command to the module. To modify the Block Trigger Value Register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 4-19.)

4.13.13 End Buffer Pointer

Address: 3FF4 – 3FF5 (H)

Linked-list mode only

The End Buffer pointer points to the address following the last word in the final message in the Message Block area. The End Buffer pointer is updated each time a final message is written into the buffer. Final messages that are longer than the remaining available space in the Message Block area do not wrap around to the start of the buffer. They are spilled into the Message Block Spill area, which is contiguous to the Message Block area. The value of this register varies from 3400 (H) (end of Message Block area) to 347E (H) (end of Message Block Spill area). Until the first buffer wrap around occurs, this register contains 0000 (H).

4.13.14 Next Message Pointer

Address: 3FF2 – 3FF3 (H)

Linked-list mode only

The Next Message pointer is a 16-bit pointer that indicates the address of the message about to be written. The Next Message Pointer Register is updated at the end of each message storage operation. It cycles from 0 (H) to 33FE (H).

4.13.15 Last Block Register

Address: 3FF2 - 3FF3 (H)

Look-up Table mode only

Read the Last Block Register to determine the (Look-up Table) block number of the current message. This register is used to identify the location of the current message. The Last Block Register is updated at the end of each message reception.

4.13.16 1760 Header Value Transmit Table

Address: 3F40 – 3F7F H

Write to the 1760 Header Value Transmit table to set the expected value of the first Data Word in a RT-to-BC message.

The 1760 option provides predefined values, and these are preset on the *M4KMMSI* module. The user can change the preset values.

Transmit Subaddress	Header Value [Hex]	Address
1	**0421**	3F42 H
11	**0420**	3F56 H
14	**0423**	3F5C H

Predefined 1760 Transmit Header Value

4.13.17 1760 Header Value Receive Table

Address: 3F00 – 3F3F (H)

Write to the 1760 Header Value Receive table to set the expected value of the first Data Word in a BC-to-RT message. The monitor checks that the specified header value was received. If the wrong data was sent, the **1760 Header error** bit is set in the **Message Status Word**, on page4-10.

The 1760 option provides predefined values, and these are preset on the *M4KMMSI* module.The user can change the preset values.

Receive Subaddress	Header Value [Hex]	Address
11	**0400**	3F16 H
14	**0422**	3F1C H

Predefined 1760 Receive Header Values

4.13.18 1760 Header Exist Table

Address: 3EC0 – 3EFF (H)

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the module should expect a header word for messages directed to that subaddress. In Bus Monitor Mode, there is a separate bit to select Header Words for transmit and receive messages.

For those Header Exist table entries for which MIL-STD 1760 provides predefined values, the corresponding Header Exist table entries are preset on the *M4KMMSI*. To set other values, enable the Header Exist table entry for this Subaddress (set it to 1) and write the value to the Header Value [Transmit/ Receive] table.

Bit	Description
09 – 15	Reserved
08	1 = Module should expect a Header word in a transmit message (RT-to-BC) 0 = Module should **not** expect a Header word in a transmit message
01 – 07	Reserved
00	1 = Module should expect a Header word in a receive message (BC-to-RT) 0 = Module should **not** expect a Header word in a receive message

1760 Header Exist Table

Associated Subaddress	Header Value [Hex]	Address
11	0100	**3EC2 H**
14	0101	**3ED6 H**
1	0101	**3EDC H**

Predefined 1760 Header Values

4.13.19 Message Counter Lo & Hi

Address: 3EAE – 3EAF H
3EAC – 3EAD H

The Message Counter Lo & Hi keep track of how many messages were received.

4.13.20 Pretrigger Message Counter Lo & Hi

Address: 3EAA – 3EAB H
3EA8 – 3EA9 H

Sequential Fixed-block mode only

The Pretrigger Message Counters Lo & Hi keep track of how many messages were received *until* the trigger kicked in. This enables the user to know that there is activity, until the trigger condition is fulfilled, causing the monitor to actually begin monitoring.

4.13.21 Serial Number Register

Address: 3EA0 – 3EA1 (H)

The Serial Number Register holds the board's serial number, which is stored in non-volatile flash memory and loaded at power-up. The value is binary coded. For example, a value of 1234 (H) represents the serial number 4660.

4.13.22 Monitor Response Time Register

Address: 3E8E – 3E8F (H)

The Monitor Response Time Register sets the maximum wait time until the Monitor considers an RT's Status Response valid.

The Monitor Response Time Register is measured in microseconds. The default value of the register is 14 μsec, if not set otherwise by the user.

4.13.23 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision Register indicates the revision level of the module firmware. The value 18 (H) would read as revision 1.8.

5 Internal Concurrent Monitor

Chapter 5 describes Internal Concurrent Monitor operation:

5.1 Concurrent Monitor Memory Map 5-1
5.2 Message Block Area 5-2
5.2.1 Message Block Structure 5-2
5.2.2 Message Status Word. 5-3
5.2.3 MMSI Message Words 5-4
5.3 Control Register Definitions. 5-4
5.3.1 Concurrent Monitor Next Message Pointer. 5-4
5.3.2 Module Options Register 5-4

A Concurrent Monitor operates automatically on the *M4KMMSI* when the module is started in BC/Concurrent-RT mode. It operates in Sequential Fixed-block mode, the Message blocks are stored in sequential locations in memory. The storing of messages starts at block 0.

5.1 Concurrent Monitor Memory Map

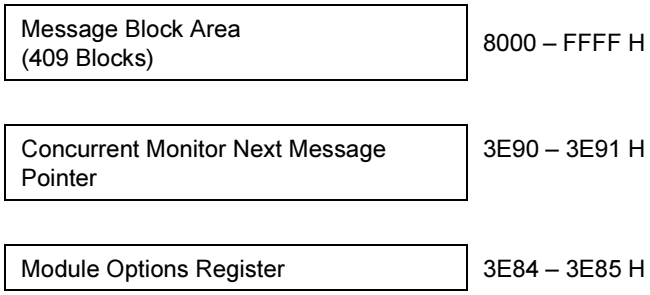


Figure 5-1 Concurrent Monitor Memory Map

5.2 Message Block Area

The message block area is divided into 409 blocks of 80 bytes each. The first block starts at address 8000 (H), the second at 8050 (H), the third at 80A0 (H), etc.

Block #408	FFFF H
•	•
•	•
•	•
Block #2	80A0 H
Block #1	8050 H
Block #0	8000 H

Message Block Area

5.2.1 Message Block Structure

Each message block occupies 40 words. These 40 words include a Message Status Word, 2 consecutive Time Tag words and all the MMSI message words.

Word 40 is a serial counter. The first message will have a serial counter value of 1; the second message will have a value of 2, etc.

Serial Counter Word	+78	One block
See **Appendix A MMSI Message Formats** on page A-1	• • • +8	
MMSI Command Word	+6	
Time Tag Word Hi	+4	
Time Tag Word Lo	+2	
Message Status Word	+0	

Concurrent Monitor Message Block Structure

5.2.2 Message Status Word

The Message Status Word indicates the status of the message transfer. The module creates this word. Do not confuse it with the Status Word. (See section **2.5 RT Status Word** on page 2-7.) The contents of the Message Status Word are shown below. A logic 1 indicates the occurrence of a status flag.

Message Status Word – BC-RT/Concurrent Monitor

Bit	Bit Name	Description
15	**End of Message**	Message transfer completed.
14	**Reserved**	Set to 0
13	**1760 Checksum Error**	The computed checksum (on an incoming message) does not match the last Data Word received. See **3.8.2 1760 Checksum Error,** page 3-14
12	**Message Error**	Message Error bit (bit 10) in the RT Status Word was set.
11	**RT Status**	A bit other than the Message Error bit in the RT Status Word was set. The Error bit is not set in conjunction with this bit.
10	**Invalid Message**	Message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error.
09	**Response Error**	Response time error occurred in the message.
08	**1760 Header Word Error**	Header Word received does not match the value set in the Header Value Table [1760 option only] See section **3.8.1 1760 Header Word,** page 3-14
07	**Invalid Word Received**	At least one invalid Word received (i.e. bit count, Manchester code, parity).
06	**High Word Count Error**	RT transmitted too many words.
05	**Low Word Count Error**	RT transmitted too few words.
04	**Incorrect RT Address**	Received Status Word did not contain the correct RT address.
03	**Sync Error**	Sync of either the Status or the Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received Words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Note: The message contents are valid only after the Message Status Word has been written, which is indicated by the End of Message bit being turned on.

5.2.3 MMSI Message Words

The message words are stored in the sequence they appear on the bus, i.e., MMSI Command Words, Status Words, Data Words - all according to the order of the specific type of message.

5.3 Control Register Definitions

5.3.1 Concurrent Monitor Next Message Pointer Address: 3E90 – 3E91 (H)

The Concurrent Monitor Next Message pointer is a 16-bit pointer that indicates the address of the message about to be written. The register is updated at the end of each message storage operation. It cycles from 8000 (H) to FFFF (H).

5.3.2 Module Options Register Address: 3E84 – 3E85 (H)

Read only The Module Options Register is a 16-bit register that identifies the type of on-module firmware.

Bit	Description
11 – 15	Reserved
10	0 = Nios II Processor 1 = Intel Processor
09	1 = MIL-STD-1760 (always set)
00 – 08	Reserved

Module Options Register

6 Switching Modes of Operation

Many test applications utilizing the *M4KMMSI* simulate only one mode, for example, Remote Terminal mode. For these applications, this chapter is irrelevant.

If your application requires simulation of more than one mode, you can switch from one mode of operation to another, for example, between the Bus Controller/ Concurrent-RT mode and Remote Terminal modes.

TO SWITCH BETWEEN MODES OF OPERATION:

1. Halt the operation of the module (via the Start Register).
2. Modify the Module Configuration Register to the desired mode.

Hex Value	Operating Mode
02	Remote Terminal
04	BC/Concurrent-RT
08	BM Sequential Fixed-block
10	BM Sequential Linked-list
20	BM Look-Up Table

Module Configuration Register Values

3. Set up the memory as required.
4. Set the Start bit in the Start Register.

7 Mechanical and Electrical Specifications

Chapter 7 describes the mechanical and electrical specifications of the *M4KMMSI* module. The following topics are covered:

7.1 *M4KMMSI* Module Layout 7-1
7.2 LED Indicators 7-2
7.3 RS-485 Port Termination Jumpers [JR0–JR8] 7-2
7.4 Connectors 7-3
7.4.1 EXC-4000 Carrier Board 96-pin Connector 7-3
7.5 Power Supply Requirements 7-5

7.1 *M4KMMSI* Module Layout

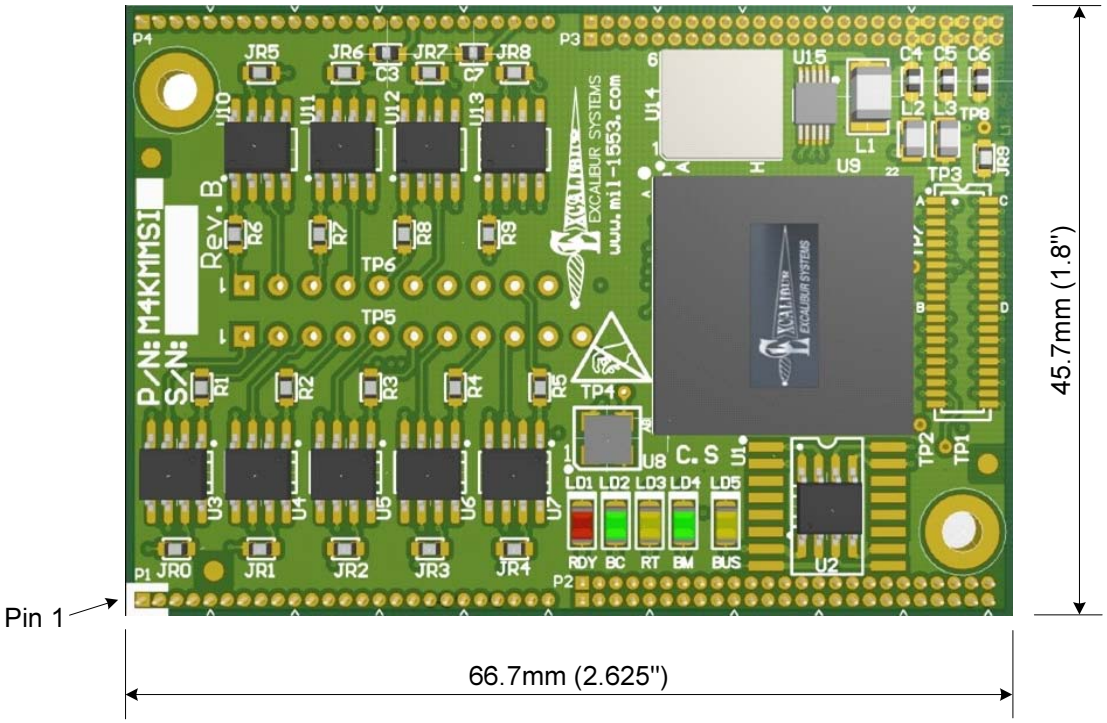


Figure 7-1 *M4KMMSI* Module Layout

7.2 LED Indicators

The *M4KMMSI* module contains four LEDs.

LED	Indication
LD1	Ready
LD2	BC or BC/Concurrent-RT Mode Active
LD3	RT Mode Active
LD4	Bus Monitor Mode Active
LD5	Bus Active

Led Indicators

7.3 RS-485 Port Termination Jumpers [JR0–JR8]

These 0603 surface mount (SMD) 0-Ohm resistors allow you to connect or disconnect the onboard 120-Ohm resistors. When a jumper is installed, the corresponding termination resistor is ON (default). When a jumper is removed, the corresponding termination resistor is OFF. See the following table.

Caution: Keep all antistatic precautions when removing or resoldering these resistors.

Port # to Terminate	Use Jumper
Port0	JR0
Port1	JR1
Port2	JR2
Port3	JR3
Port4	JR4
Port5	JR5
Port6	JR6
Port7	JR7
Port8	JR8

Table 7-1 RS-485 Port Termination Jumpers [JR0–JR8]

7.4 Connectors

The *M4KMMSI* contains four 25-pin, 0.05" spacing strips (P1 – P4) which compromise a total of 100 pins for all the module connections. These pins mate with the carrier board socket strips. Out of these 100 pins, 24 pins are assigned for the communication I/O signals.

On most carrier boards, all the module's 24 I/O signals are wired to a 96-pin female connector. The connector is divided into four rows of 24 pins each. Each row is for one module location on the carrier board. The mating connector contains four Terminal Sticks; one for each module. See **Figure 7-2 EXC-4000 Carrier Board 96-pin Female I/O Connector – Front View.**

For the *EXC-4000P104plus* carrier board connectors, refer to the *EXC-4000P104plus Carrier Board User's Manual*.

For the *EXC-2000PCI[e]* carrier board connectors, refer to the *EXC-2000PCI & EXC-2000PCIe User's Manual*.

7.4.1 EXC-4000 Carrier Board 96-pin Connector

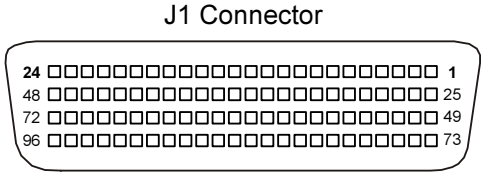


Figure 7-2 EXC-4000 Carrier Board 96-pin Female I/O Connector – Front View

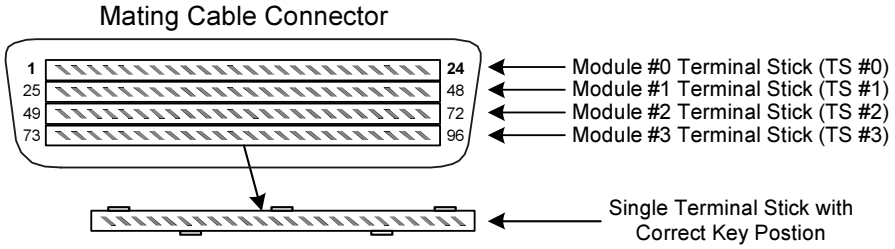


Figure 7-3 EXC-4000 Carrier Board 96-pin Male I/O Mating Cable Connector – Front View

7.4.1.1 *M4KMMSI* Module Terminal Stick and Adapter Cable Pinouts

24-Pin Terminal Stick Pin #	Adapter Cable Connector Pin # (HDB 26-pin Female)	Signal Name	Signal Description
1	1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	2	CH0L	Port 0 low connection
3	3	CH0H	Port 0 high connection
4	4	CH1L	Port 1 low connection
5	5	CH1H	Port 1 high connection
6	6	CH2L	Port 2 low connection
7	7	CH2H	Port 2 high connection
8	8	CH3L	Port 3 low connection
9	9	CH3H	Port 3 high connection
10	10	CH4L	Port 4 low connection
11	11	CH4H	Port 4 high connection
12	12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13	13	CH5L	Port 5 low connection
14	14	CH5H	Port 5 high connection
15	15	CH6L	Port 6 low connection
16	16	CH6H	Port 6 high connection
17	17	CH7L	Port 7 low connection
18	18	CH7H	Port 7 high connection
19	19	CH8L	Composite BM Output low connection
20	20	CH8H	Composite BM Output high connection
21	21	N/C	Not connected
22	22	N/C	Not connected
	23 – 26	N/C	Not connected
23		EXSTRTn	External Start TTL input. Provides an option to start the module externally by applying a negative pulse of 100 nsec/min. with respect to the GND pin. Before applying the pulse, the module should be fully set up in the required mode, except the Start register bit 00, which should be left at 0. To stop the selected operation, follow the normal procedure described under the Start register.
24		GND	Provides ground reference for the EXSTRTn signal

Table 7-2 *M4KMMSI* Module Terminal Stick and Adapter Cable Pinouts

***M4KMMSI* Module Adapter Cable**

A standard adapter cable can be purchased from Excalibur that converts the Molex® terminal stick to a standard 26-pin high density D-type female connector with jack screws (see figure below). The cable is 0.5 meter in length and a mating connector (with hood) is included in the cable package.

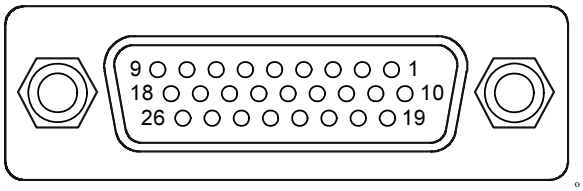


Figure 7-4 *M4KMMSI* Module Adapter Cable Connector – HDB 26-Pin Female – Front View

7.5 Power Supply Requirements

The *M4KMMSI* module maximum power requirements are:

Requirement	Condition
+5V @ 725mA	Standby or receive
+5V @ 920mA	Switch or Link modes, one port transmitting @ 90% duty cycle
+5V @ 1280mA	Spec or Broadcast modes, all eight ports transmitting @ 90% duty cycle

8 Ordering Information

Chapter 8 provides the part numbers for ordering *M4KMMSI* modules.

Basic Part #	Option	Description
M4KMMSI		Mini Munition Store Interface module for the Excalibur 4000 family of carrier boards. Supports RT, BC/Concurrent-RT and Bus Monitor modes, with an Internal Concurrent Monitor in BC/Concurrent-RT mode. Up to eight hub ports EBR-1553 [10 Mbps 1553 protocol using RS-485 transceivers] and 1 composite monitor output.
	-E	Add this suffix for the extended temperature option (-40°C to +85°C)
	-001	Add this suffix for conformal coating
Optional adapter cable:		
X4KR*x*		*M4KMMSI* adapter cable with a standard 26-pin high density D-type female connector. See **7.4.1.1 M4KMMSI Module Terminal Stick and Adapter Cable Pinouts** on page 7-4. Replace the "*x*" at the end of the part number by the number of *M4KMMSI* modules on the carrier board. This part number assumes that the *M4KMMSI* modules are located in the first module locations. For more details, see **Ordering Information** in the user's manual of your carrier board.

Appendix A MMSI Message Formats

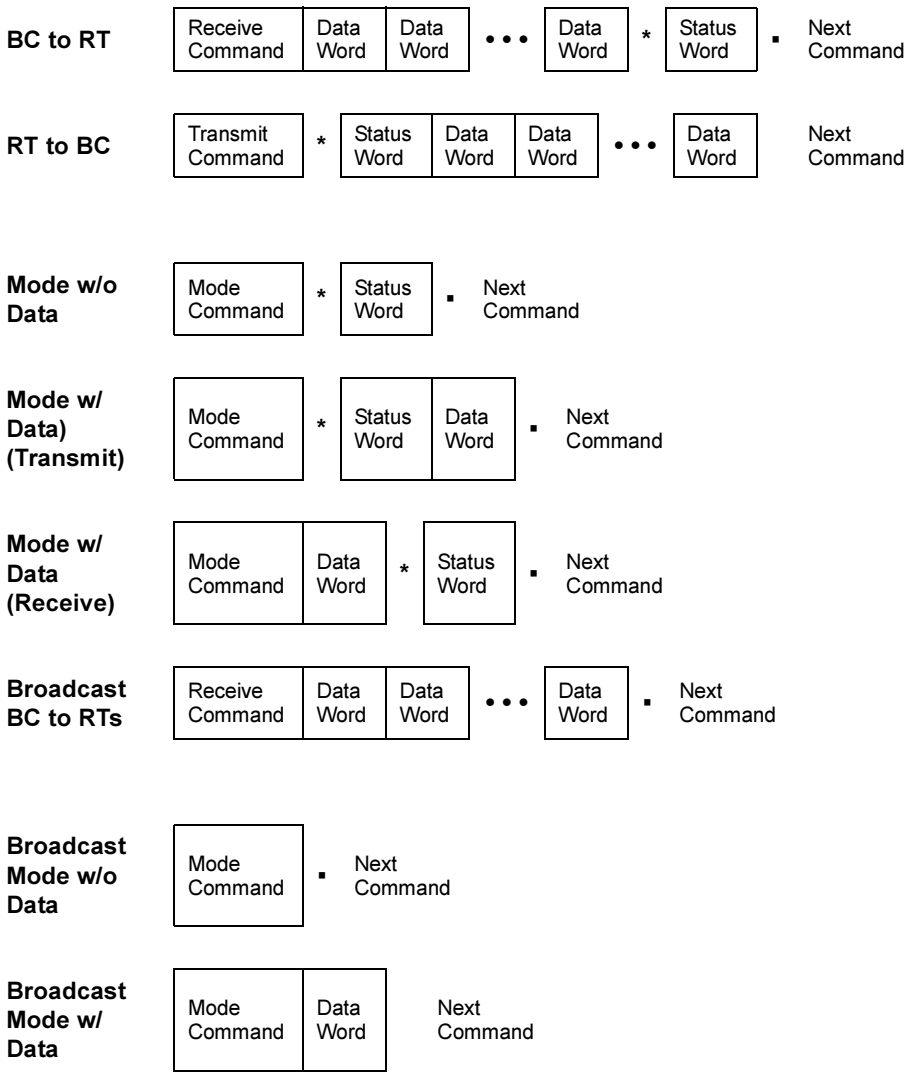


Figure A-1 MMSI Message Formats

Note: * = Response time
▪ = Intermessage Gaptime

Appendix B MMSI Word Formats

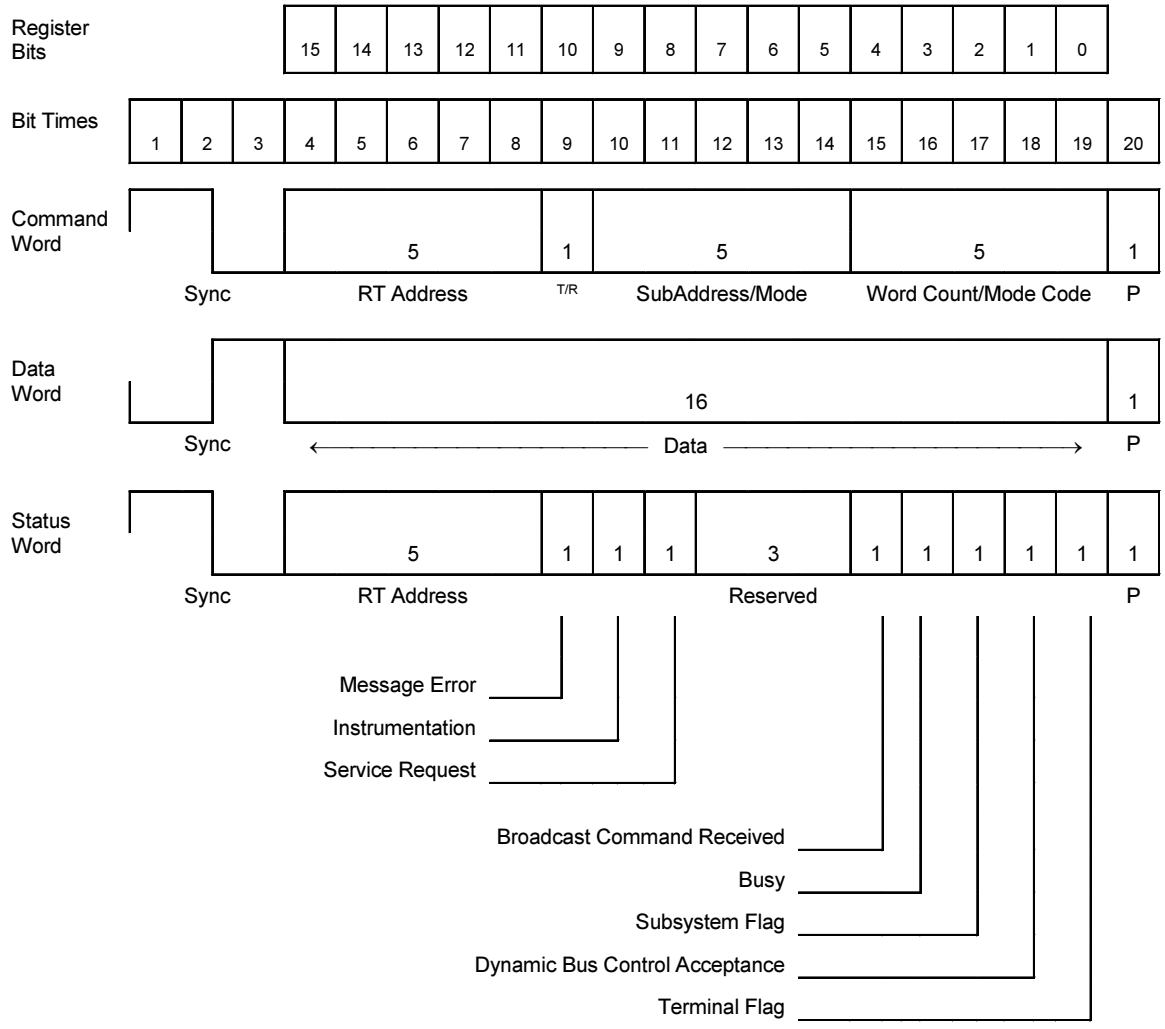


Figure B-1 MMSI Word Formats

Note: T/R = Transmit/Receive
P = Parity

Appendix C Internal Loopback Test

The Internal Loopback Test is used to check the MMSI front-end logic, excluding transceivers.

Note: When running a loopback, all values previously written to registers and memory addresses are erased.

To initiate the Internal Loopback Test:

1. Write ED (H) into the Module Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM beginning at address 0:

	Definition	Address in Dual-Port RAM	Status Value if passed
usint frame_val;		0 H	Reserved
usint frame_status;	frame time counter status	2 H	8000 H
usint resp_status;	response time counter status	4 H	8000 H
usint early_val;		6 H	Reserved
usint receive_data1;	first looped word test, using command sync	8 H	5555 H
usint status_1;		A H	8000 H
usint receive_data2;	second looped word test, using data sync	C H	AAAA H
usint status_2;		E H	8000 H
Reserved			
usint volatile ttag_val_lo;		12 H	Reserved
usint volatile ttag_val_hi;		14 H	Reserved
usint ttag_status;	Time Tag status	16 H	8000 H

Appendix D External Loopback Test

The External Loopback Test is used to test each of the eight ports and then checks the Composite Bus monitor output. A loopback cable is not required for this test. In addition, the eight ports can stay connected to the bus, as long as data is not being received by the module from an external source. If data may be received during the test, the module must be disconnected from the bus.

Note: When running a loopback, all values previously written to registers and memory addresses are erased.

To initiate the External Loopback test:

1. Write FF (H) into the Module Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

	Address in dual-port RAM	Status value if passed
usint frame_val;	0 H	Reserved
usint frame_status;	2 H	8000 H
usint early_val [9]	4 H	Reserved (array of nine items)
usint receive_data1 [9]	16 H	5555 H (array of nine items)
usint status_1 [9]	28 H	8000 H (array of nine items)
usint receive_data2 [9]	3A H	AAAA H (array of nine items)
usint status_2 [9]	4C H	8000 H (array of nine items)
usint volatile ttag_val_lo	5E H	Reserved
usint volatile ttag_val_hi	60 H	Reserved
usint ttag_status;	62 H	8000 H

Release Notes

M4KMMSI Module Rev B

1. Eight new jumpers are provided on the module's component side that allow you to connect/disconnect each RS-485 port's termination.
2. An additional LED has been added to indicate Bus Monitor mode active.
3. The module's FPGA integrated circuit incorporates an additional heat sink plate that makes the module higher by approximately 3 mm.
4. Connectors P2 and P3 have an option to extend to dual-row connector for future 32-bit operation.
5. A Serial Number Register has been added at address 3EA0 (H), which represents the module's serial number.

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