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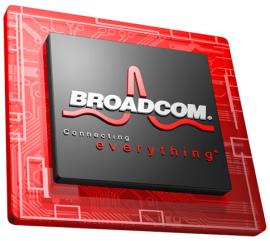
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BCM1125H PRODUCT Brief



BCM1125H HIGH-PERFORMANCE MIPS PROCESSOR

FEATURES

- **Highly integrated single core processor running at 400 MHz - 800 MHz**
- **SB-1 MIPS64™ CPU**
  - Quad-issue in order pipeline; dual execute, dual memory pipes
  - Enhanced skew pipeline enables zero load-to-use penalty
  - 32-KB instruction cache, 32-KB data cache
  - Advanced branch predictors
- **Fast, on-chip memory-coherent bus (ZBbus)**
  - Connects the CPU, L2 cache, memory controller and I/O bridges
  - Runs at half the CPU core clock; 256 bits wide
- **On-chip L2 cache**
  - 256 KB, shared by CPU and I/O bridges
  - Four-way associative, ECC protected
  - Ways can be removed to provide fast on-chip RAM
- **DDR memory controller**
  - One channel with a 64-bit data bus plus ECC
  - Runs up to 200 MHz clock rate, 400 Mbps data rate
  - Support for DDR SDRAM, SGRAM, and FCRAM
- **High-speed packet interfaces**
  - Two 10/100/1000 Ethernet MACs; 802.3 compliant
  - Option to configure MACs into packet FIFOs to enable OC-48 data rates
- **PCI interface**
  - 32-bit, 33/66 MHz PCI 2.2
  - Host bridge or target device
- **HyperTransport™ I/O interface**
  - Complies with HyperTransport standard for high-speed I/O fabric
  - 600-MHz clock rate, 1.2 Gbps data rate
  - Peak bandwidth of 19.2 Gbps on 8-bit link
  - Supports double-ended fabrics (linking two BCM1125Hs or BCM1125H to BCM1250, BCM1280, or BCM1480)
- **Integrated system I/O**
  - Generic I/O for direct connect to boot ROM, FLASH, fast peripherals/ ASICs
  - SMBus serial configuration interface
  - PCMCIA control interface
  - Two serial interfaces
- **Extensive, on-chip debug features**
- **4W @ 400 MHz**
- **Software-compatible with BCM1250, BCM1255, BCM1280, BCM1455, and BCM1480**
- **Support for leading operating systems including VxWorks®, Linux®, NetBSD®, OSE®, QNX® and Teja™ NP OS**
- **Multiple evaluation board platforms available with tools, firmware and software drivers**

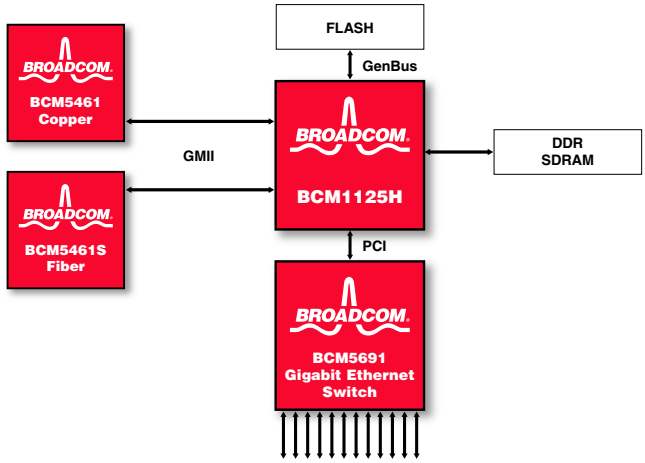
SUMMARY OF BENEFITS

- **Industry-leading performance**
  - 2.5 DMIPS/MHz
  - Processing speed of up to 4.3 Mpps*
  - 128-Gbps on-chip bus bandwidth, 25-Gbps memory bandwidth, 30-Gbps total I/O bandwidth
- **Low power dissipation starting at less than 4W @ 400 MHz**
- **High functional integration**
- **Programming ease and flexibility based on MIPS64 ISA**
- **Scalable system architecture**
- **Broad tools and system software support**
- **Software-compatible with BCM1250, BCM1255, BCM1280, BCM1455, and BCM1480**

*Based on internal Broadcom benchmark, using BCM112x for standard IPv4 L3 look-up/switching.

APPLICATIONS

- **The BCM1125H's world-class performance, power efficiency and integration makes these processors ideal for a broad variety of systems including:**
  - Networking: routers, switches
  - Control plane processing
  - Line cards
  - Broadband access: DSLAM, CMTS, BRAS
  - Wireless base stations
  - Storage: RAID controllers, NAS controllers, HBAs
  - Web/networking/caching appliances
  - Imaging: printers, copiers

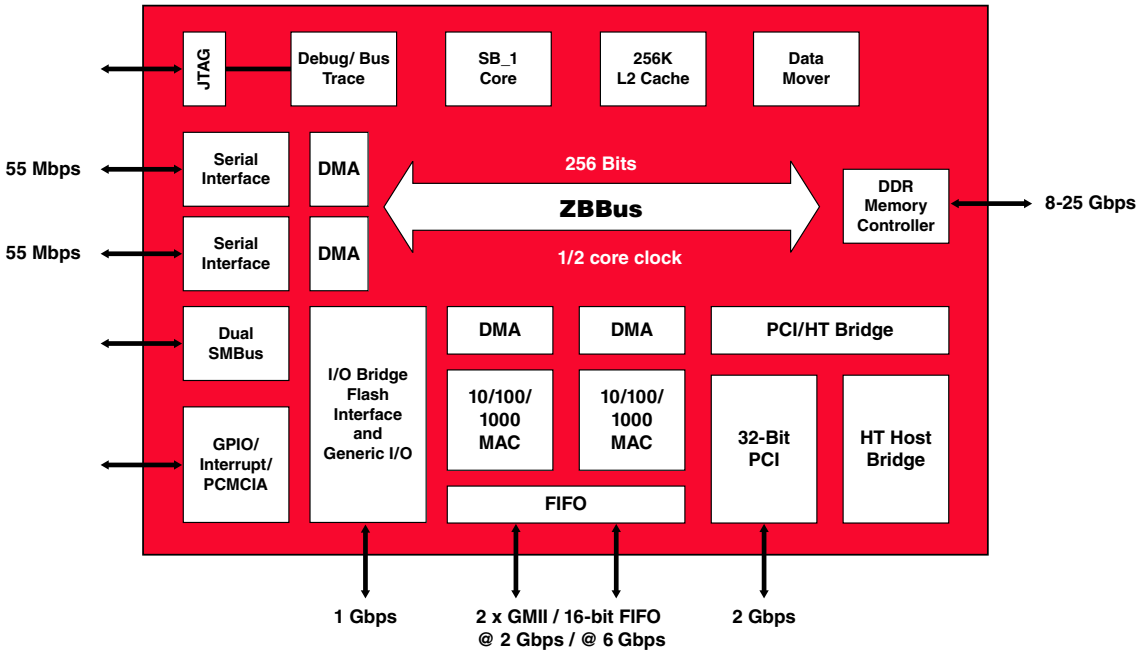


Example: Gigabit Ethernet Control Panel

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OVERVIEW



BCM1125H Block Diagram

Broadcom's BCM1125H product is a state-of-the-art processor solution targeted at the fast-growing networking, wireless communications, storage, server/networking appliance and imaging markets. BCM1125H processors offer industry-leading performance, high functional integration, and low power levels in a small package required by next-generation networking applications.

The BCM1125H is software-compatible with the dual-processors BCM1250, BCM1255, and BCM1280 as well as with the quad-core processors BCM1455 and BCM1480. All these processors and share development and modeling tools, firmware, and operating systems with the processor. The BCM1125H processors are intelligent systems on a chip consisting of a Broadcom SB-1 high performance MIPS64 CPU, a shared 256-KB L2 cache, a DDR memory controller, and an integrated I/O. All major blocks of the processor are connected together via the ZBbus, a high-speed, low-latency, split-transaction, memory-coherent bus. The bus implements the standard MESI protocol to ensure coherency between the CPU, L2 cache, I/O agents, and memory.

Two Gigabit Ethernet MACs (10/100/1000) enable easy interfacing to LANs. To enable higher data rates, or in cases where Ethernet protocol processing is not required, each MAC can be configured as an 8-bit packet FIFO, or both can be combined into a 16-bit packet FIFO. High-speed I/O is provided using a 66-MHz (rev 2.2) PCI local bus and 8-bit wide HyperTransport™ (HT) interface.

Two serial ports are provided for WAN connections at up to T3/OC-1 rates (55 Mbps). To enable low-chip-count systems, the BCM1125H processors also include a configurable generic bus that allows glueless connection of a boot ROM or FLASH memory and simple I/O peripherals. On-chip debugging, tracing, and performance monitoring functions assist both hardware and software designers in debugging and tuning the system. The system can be run in either big- or little-endian mode. The BCM1125H processors are manufactured in TSMC's 0.13-µ process, and are packaged in pin-compatible 31-mm BGA packages.

Implementation of MIPS64 ISA

The SB-1 CPU core is a high-performance implementation of the standard MIPS64 Instruction Set Architecture (ISA), and incorporates the MIPS-3D and MIPS-MDMX Application Specific Extensions (ASEs). The core supports a four-issue enhanced skew pipeline and can dispatch up to two memory and two ALU (Integer, Floating Point, MDMX or MIPS-3D) instructions per cycle.

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