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XPedite6244

Freescale 7448 PowerPC Processor AMC Module with Gigabit Ethernet and SATA Support

User's Manual

Revision 061222

X-ES

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Revision History

Revision	Principal Changes	Date	Board Rev.
061222	Initial Creation	December 22, 2006	SA

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1. Overview

XPedite6244 is a high performance AMC single board computer. With a 1.4GHz Freescale 7448 PowerPC Processor, XPedite6244 is ideal for the high bandwidth processing requirements of today's blade and general computing applications.

A Marvell Discovery III system controller provides a high performance communications channel between the processor, a DDR SDRAM interface, four gigabit Ethernet interfaces, a USB interface, and a SATA AMC interface. XPedite6244 supports up to 1GB of local memory.

To the system designer, XPedite6244 provides a feature rich solution to support the next generation of embedded applications.

A Linux Support Package (LSP) is available.

1.1 Features

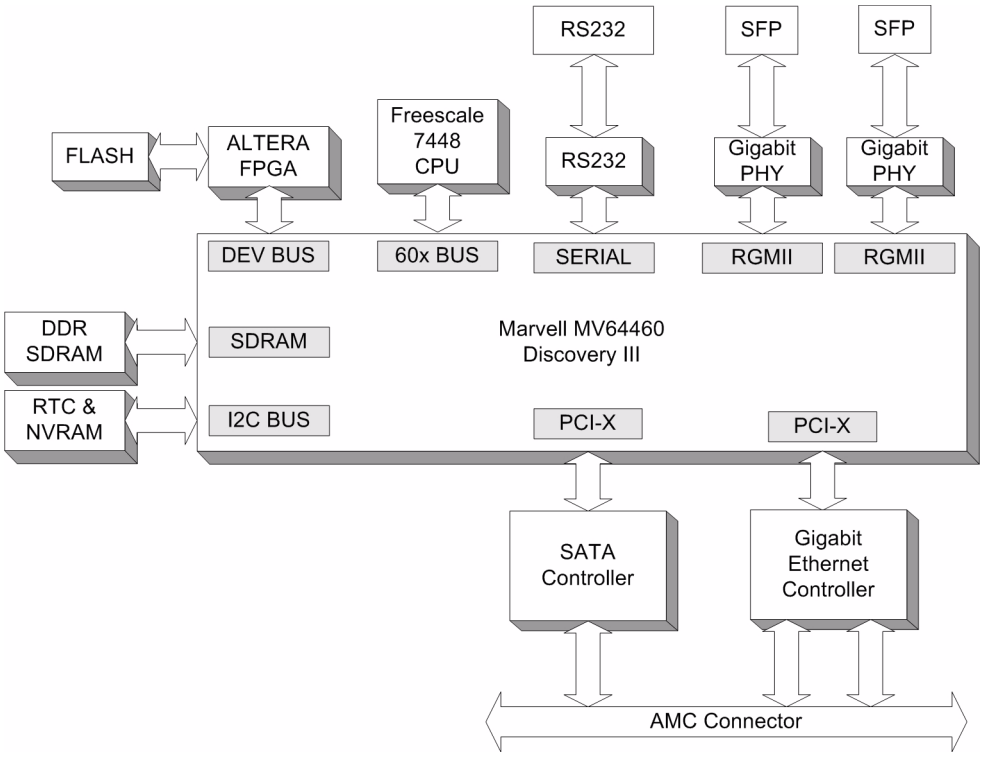
The list below is a brief description of XPedite6244 features. Refer to the specific section in the manual for additional information.

PowerPC PPC7448 Processor	The low power / high performance Freescale PPC7448 PowerPC Processor operates internally at 1.4 GHz. In addition 32KB L1 instruction and data caches are provided, as well as a on-board 512KB L2 Cache.
SATA	Local SATA controller supports two AMC.3 interfaces.
DDR SDRAM	XPedite6244 supports up 1GB of DDR SDRAM.
Flash	Up to128MB of soldered flash is supported.
Gigabit Ethernet Ports	Two SFP front panel ports are available for optical or electrical 10/100/1000 Mbps operation. Two AMC.2 Gigabit Ethernet Ports are also available.
RS232 Ports	Two RS232 ports are available for application and development.
RTOS and Protocols	Board Support packages are available for Integrity, QNX Neutrino, Linux, and vxWorks
USB Port	One USB port is provided via a Cypress Semiconductor SL811HS device. This interface is capable of low speed (1.5 Mbit/s) and full speed (12 Mbit/s) operation.

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1.2 Block Diagram

Figure 1.2.1: Block Diagram



1.3 Terminology / Conventions

Table 1.3.1: Terminology

Term	Definition
byte	8 bits
DMA	Direct Memory Access
double long word	64 bits
DRAM	Dynamic Random Access Memory
JTAG	Joint Test Action Group
long word	32 bits
MII	Media-independent Interface
PCI	Peripheral Component Interconnect
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Synchronous Random Access Memory
word	16 bits

Table 1.3.2: Conventions

Term	Definition

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0x0	This notation denotes a hexadecimal number.
0b0	This notation denotes a binary number.
Active Low Signals	Active Low Signals are listed with a # postfix. IE: RESET#

1.4 Technical Information

The technical information in this manual is intended to describe the unique features of XPedite6244. It is assumed that the reader has familiarity with the devices and interface standards incorporated into the XPedite6244. This information can be found in the following manuals and specifications.

PPC7448	PowerPC 7448 RISC Microprocessor User's Manual	Freescale	
	PowerPC 7448 RISC Microprocessor Datasheet Preliminary Electrical Information	Freescale	
PCI	PCI Local Bus Specification, Revision 2.2	PCI-SIG	
AMC	PICMG Advanced Mezzanine Card Base Specification, R1.0	PICMG	AMC.0
	PICMG Gigabit Ethernet on AdvancedMC, R1.0	PICMG	AMC.2
	PICMG Serial ATA on AdvancedMC, R1.0	PICMG	AMC.3
Discovery III	MV64460, MV64461, MV64462 System Controller for PowerPC Processors	Marvell	MV-S101286-01A, 6/19/2003
FPGA	Altera ACEX 1K Programmable Logic Device Family Datasheet	Altera	A-DS-ACEX-3.3, Version 3.3, 11/2001
M41T00	M41T00 Serial Access Timekeeper	STMicro	**M41T00**, 11/2002
BCM5461S	Broadcom 10/100/1000Base-T Gigabit Ethernet Transceiver	Broadcom	
S29GL512N	**S29GL512N** 512 Megabit Flash Memory	AMD	Rev A, 9/8/03
SL811HS	SL811HS Embedded USB Host/ Slave Controller	Cypress	Doc #: 38-08008 Rev *B. 6/27/2005

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1.5 XPedite6244 Software/Accessories

X-ES offers several software solutions for the XPedite6244, listed below. Other operating systems can be supported by request, please contact X-ES sales!

Table 1.5.1: Available Software

Operating System	Description
VxWorks	VxWorks BSP
Linux	Linux LSP
QNX	QNX BSP
Integrity	Greenhills Integrity BSP
Other / N/A	XPedite6244 xMon Monitor

The following accessories are available for the XPedite6244 board. For more information on any of these items please contact X-ES.

Table 1.5.2: Available Accessories

Part Number	Description
70003555	Mini-USB to DB9 Serial Adapter

The following additional documentation is available for the XPedite6244 board. For more information on any of these items please contact X-ES.

Table 1.5.3: Additional Documentation

Manual	Description
xMonXPedite6244tm.pdf	XPedite6244 xMon Monitor Manual

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2. Printed Circuit Board

This chapter describes details associated with the printed circuit board. These include component maps, installation, ESD handling concerns and environmental and power requirements.

2.1 Electrostatic Discharge

When handling this product, please remember that electrostatic discharge (ESD) can easily damage the components on this module and result in board failure. Unless you ground yourself properly, static can build in your body and cause ESD damage when you touch the board. To ground yourself, wear a grounding wriststrap. Simply placing this module on a static-shielding bag offers no protection -- place it on a grounded ESD-safe mat. Do not place this board on metal or other conductive surfaces. When this board is not in use or in an enclosure, store it in either a static-shielding bag or clamshell provided.

CAUTION: Use proper ESD procedures and handle this board only when absolutely necessary. Always wear a wriststrap while handling this board. Hold this board by the edges. Do not touch any components or circuits. Store in ESD safe bag when not in use.

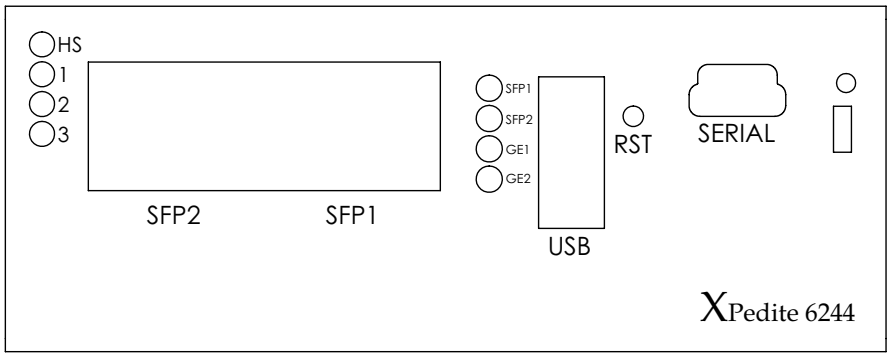
2.2 Physical Specifications

Table 2.2.1: XPedite6244 Physical Specifications

Parameter	Value
Form Factor	AMC
Length	149mm
Width	74mm
Weight	167g

2.3 Front Panel

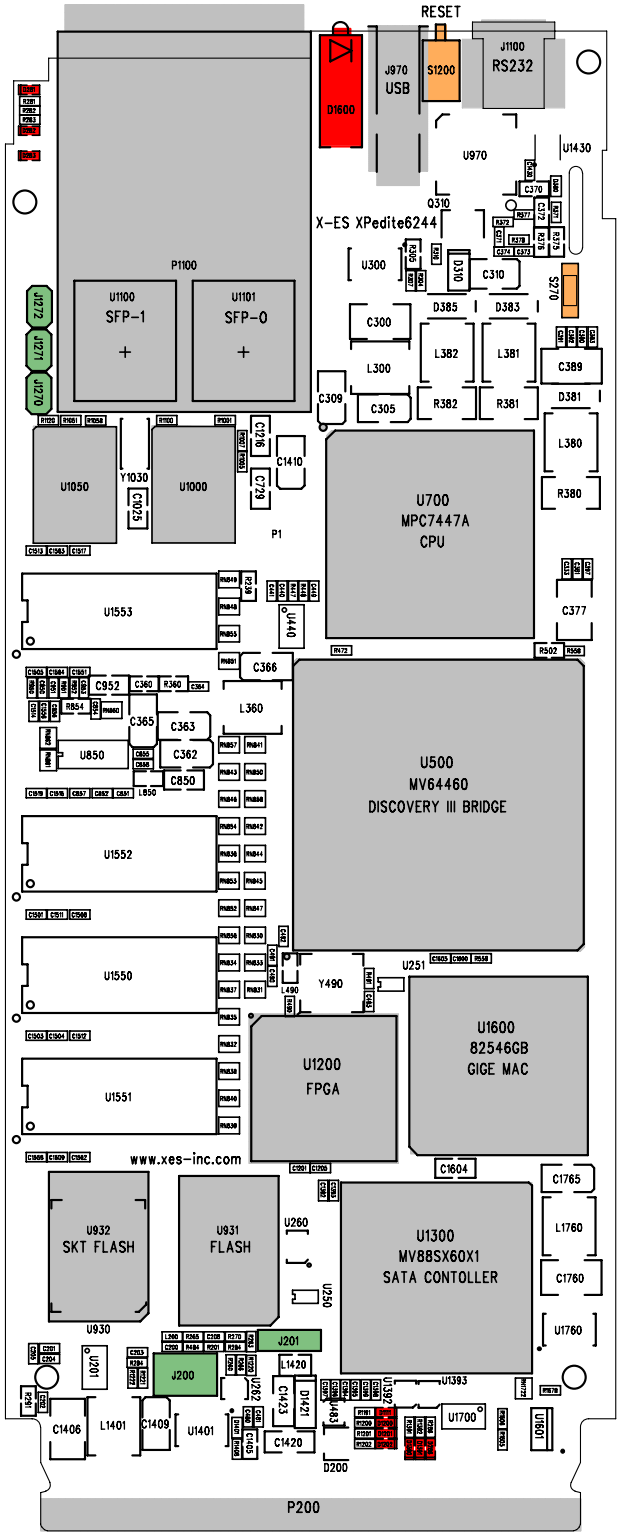
Figure 2.3.1: XPedite6244 Front Panel (Rev. SA)



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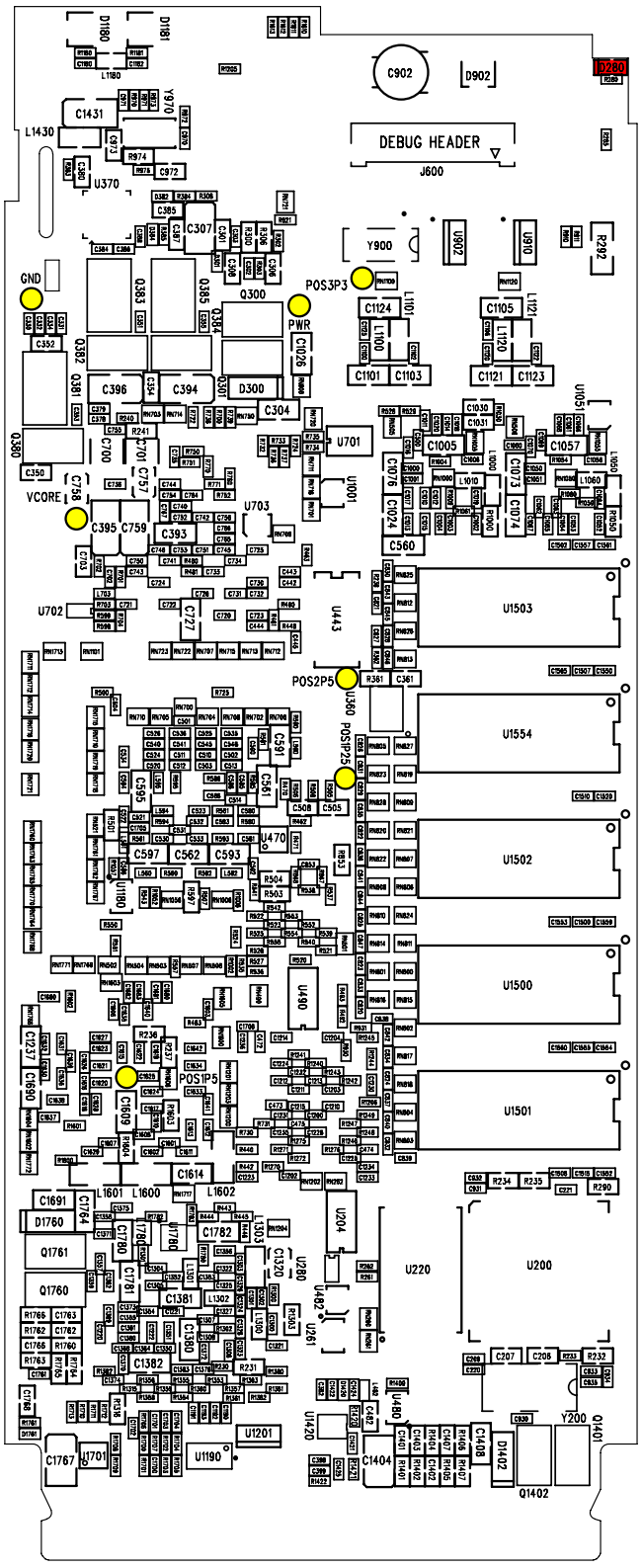
2.4 Component Maps

Figure 2.4.1: XPedite6244 Front (Rev. SA)



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Figure 2.4.2: XPedite6244 Back (Rev. SA)



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2.5 Jumper Definitions

The following table gives a description of jumpers on XPedite6244.

Table 2.5.1: Jumper Definitions

Jumper	Function
J1270	**Socket Boot Flash Select**. When installed, indicates Boot Flash (AMD Mirrorbit 0) will be used as the boot device. Otherwise, Expansion Flash (AMD Mirrorbit 1) will be utilized.
J1271	**CPU Disable**. When installed, holds CPU in reset to allow flash programming over the PCI bus.

2.6 Debug Port

XPedite6244 provides headers to access various debug and programming interfaces. These interfaces are not typically used by the application, but are documented in the following table.

Table 2.6.1: Debug Port Descriptions

Header	Function
J1200	**7448 CPU JTAG Port**. The 7448 debug port is used to connect to external debug equipment.

The JTAG port interface provided by XPedite6244 enables the connection of an external debug tools, such as RISCWatch. XPedite6244 supports this capability by providing a debug header that can be attached to the external debug tools.The JTAG port interfaces directly to the 7448 and is the only device in the JTAG chain. The pinout of the JTAG debug header is defined in the following table.

Table 2.6.2: JTAG Header Pin Assignment

Pin	Function	Pin	Function
1	TDO	9	TMS
2	-	10	-
3	TDI	11	SRESET#
4	TRST	12	GND
5	-	13	HRESET#
6	2.5 V	14	-
7	TCK	15	CKSTOP_OUT#
8	-	16	GND

2.7 Diagnostic LEDs

XPedite6244 provides three surface mount diagnostic LEDs on the back of the PCB board. These LEDs are controlled by the STS, ACT, ALM bits in the MLED FPGA register. Please refer to the FPGA Chapter for more information.

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Table 2.7.1: Diagnostic LEDs

LED	Function
D1800	**Green Status LED**. User definable surface mount LED. Off by default.
D1801	**Yellow Activity LED**. User definable surface mount LED. Off by default.
D1802	**Red Alarm LED**. User definable surface mount LED. On by default.

2.8 Environmental Requirements

Table 2.8.1: Environmental Requirements

Requirement	Specification
Operating Temperature	0C to +55C, Ambient, At Board, with Airflow
Humidity	0 to 85%
Storage Temperature	-40C to +85C
Air flow (15mm Heatsink)	200 LFM

2.9 Voltage Requirements

Table 2.9.1: Voltage Requirements

Requirement	Specification
+12.0V	12.0V +/- 5%

2.10 Power Requirements

The following tables give the maximum power requirements of XPedite6244 at the supported CPU core frequencies and core voltages.

Table 2.10.1: 12V Power Requirements

Configuration	Current	Power
(1.4GHz, 1.15V)	2.17A	26.0W

The following table gives the maximum power that can be drawn by the USB port.

Table 2.10.2: USB Power Specifications

Rail	Maximum Current	Power
+5 V	500mA	2.5W

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3. Setup & Troubleshooting

This chapter describes the setup process and how to check for proper operation once the board has been installed. The chapter also includes troubleshooting, service, and warranty information.

3.1 Electrostatic Discharge

When handling this product, please remember that electrostatic discharge (ESD) can easily damage the components on this module and result in board failure. Unless you ground yourself properly, static can build in your body and cause ESD damage when you touch the board. To ground yourself, wear a grounding wriststrap. Simply placing this module on a static-shielding bag offers no protection -- place it on a grounded ESD-safe mat. Do not place this board on metal or other conductive surfaces. When this board is not in use or in an enclosure, store it in either a static-shielding bag or clamshell provided.

CAUTION: Use proper ESD procedures and handle this board only when absolutely neccessary. Always wear a wriststrap while handling this board. Hold this board by the edges. Do not touch any components or circuits. Store in ESD safe bag when not in use.

3.2 Setup

You need the following items to set up and check the operation of the XPedite6244. Items in bold are supplied by or optionally available from X-ES.

Table 3.2.1: Setup Requirements

	Pre-Startup Checklist
❑	**XPedite6244 module**
❑	Compatible baseboard host
❑	Chassis and/or Power supply
❑	**Serial Cable (optional)**
❑	Terminal

3.3 Check Power Supply

Verify that your power supply or host module is sufficient for the board. See chapter 2 for the XPedite6244 module's power requirements.

3.4 Installation & Removal

To install the XPedite6244, gently insert the module into the AMC slot. While installing XPedite6244, be careful not to force the module into the host card or you may damage one or both devices. If present, secure the XPedite6244 module to the carrier with screws.

CAUTION: To avoid damaging the module and/or baseboard, do not force the module onto the baseboard.

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3.5 Troubleshooting

In case of difficulty, use this checklist:

Table 3.5.1: Troubleshooting Checklist

	Troubleshooting Checklist
❑	Be sure the XPedite6244 is fully seated into the baseboard.
❑	Be sure the system is not overheating
❑	Check the cables and connectors to be certain they are secure.
❑	If you are using the XPedite6244 xMon, check that your terminal is connected to serial port 0 and verify that the baud rate is set to 9600.
❑	If you are using the XPedite6244 xMon, check the results of the power on self-test (POST). Check the serial port 0 output. See XPedite6244 xMon manual for more details.
❑	Check your power supply for proper DC voltages. If possible, use an oscilloscope to look for excessive power supply ripple or noise. On the back of the XPedite6244 PCB are labeled test points for each of the card voltages.

3.6 Technical Support

If you have verified the above items, send an email to support@xes-inc.com (or call 1-608-833-1155) and ask for technical support from our support system. Please have the following information handy:

- XPedite6244 board serial number
- Baseboard model number
- Operating System and version
- xMon monitor version (if applicable)
- Any custom modifications to your board

To determine the serial number of your board, look for the white sticker attached to the PCB. The serial number will be an 8 digit number of the form 9XXXXXXX.

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3.7 Service Information

If you plan to return the board to X-ES for service, send an email to support@xes-inc.com (or call 1-608-833-1155) and ask for a Return Merchandise Authorization (RMA) number. We will ask which items you are returning, the board serial numbers, reason for return, plus your purchase order number. If you are returning hardware that is out of warranty, we will require billing information as well. Contact us at support@xes-inc.com for any warranty questions. When returning any product, be sure to enclose it in an anti-static bag or clam-shell, such as the original shipping material. Send it pre-paid to:

Extreme Engineering Solutions, Inc.
3225 Deming Way, Ste. 120
Middleton, WI 53562-1408

RMA#_____

Our service department cannot accept material returned without an RMA number.

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4. AMC Interface

XPedite6244 is an AMC module that conforms to the PICMG AMC.0 standard. A SATA interface conforms to the PICMG AMC.3 standard. Two Gigabit Ethernet intefaces ar routed to the backplane via the PICMG AMC.2 standard.

4.1 AMC Port Usage

Table 4.1.1: Port Assignments

Port	Group	Device
CLK1	Clocks	Not Used.
CLK2		Not Used.
CLK3		Not Used.
0	Common Options Region	Gigabit Ethernet 0
1		Gigabit Ethernet 1
2		SATA Channel 0
3		SATA Channel 1
4-18	Fat Pipes Region	Not Used.
19		Serial Port 1
20		Serial Port 0

4.2 AMC Gigabit Ethernet

The Intel 82546 is utilized to provide the serdes interfaces to the AMC backplane.

4.3 AMC SATA

The Marvell MV88SX6041 provides the SATA ports.

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4.4 Pin Assignments

Table 4.4.1: AMC Base Pin Assignments

Pin	P11	Pin	P11	Pin	P11	Pin	
1	GND	23	ETH1_RX+	45	NC	67	GND
2	POS12	24	ETH1_RX+	46	GND	68	NC
3	PS1#	25	GND	47	NC	69	NC
4	POS3P3	26	GA2	48	NC	70	GND
5	GA0	27	POS12	49	GND	71	SDA_L
6	NC	28	GND	50	NC	72	POS12
7	GND	29	SATA0_TX+	51	NC	73	GND
8	NC	30	SATA0_TX-	52	GND	74	NC
9	POS12	31	GND	53	NC	75	NC
10	GND	32	SATA0_RX+	54	NC	76	GND
11	ETH0_TX+	33	SATA0_RX-	55	GND	77	NC
12	ETH0_TX-	34	GND	56	SCL_L	78	NC
13	GND	35	SATA1_TX+	57	POS12	79	GND
14	ETH0_RX+	36	SATA1_TX-	58	GND	80	NC
15	ETH0_RX+	37	GND	59	NC	81	NC
16	GND	38	SATA1_RX+	60	NC	82	GND
17	GA1	39	SATA1_RX-	61	GND	83	PS0#
18	POS12	40	GND	62	NC	84	POS12
19	GND	41	ENABLE#	63	NC	85	GND
20	ETH1_TX+	42	POS12	64	GND		
21	ETH1_TX-	43	GND	65	NC		
22	GND	44	NC	66	NC		

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Table 4.4.2: AMC Extended Pin Assignments

Pin	P11	Pin	P11	Pin	P11	Pin	
86	GND	108	NC	130	NC	152	GND
87	NC	109	NC	131	GND	153	NC
88	NC	110	GND	132	NC	154	NC
89	GND	111	NC	133	NC	155	GND
90	NC	112	NC	134	GND	156	NC
91	NC	113	GND	135	NC	157	NC
92	GND	114	NC	136	NC	158	GND
93	NC	115	NC	137	GND	159	RS232_RX1
94	NC	116	GND	138	NC	160	RS232_TX1
95	GND	117	NC	139	NC	161	GND
96	NC	118	NC	140	GND	162	RS232_RX0
97	NC	119	GND	141	NC	163	RS232_TX0
98	GND	120	NC	142	NC	164	GND
99	NC	121	NC	143	GND	165	NC
100	NC	122	GND	144	NC	166	NC
101	GND	123	NC	145	NC	167	NC
102	NC	124	NC	146	GND	168	NC
103	NC	125	GND	147	NC	169	NC
104	GND	126	NC	148	NC	170	GND
105	NC	127	NC	149	GND		
106	NC	128	GND	150	NC		
107	GND	129	NC	151	NC		

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5. CPU

This chapter provides a description of the PPC7448 processorn and it's on-card resources.

XPedite6244 utilizes the Freescale PowerPC PPC7448 processor operating internally up to 1.4 GHz. In addition, 32KB L1 instruction and data caches are provided, as well as a on-board 512KB L2 Cache. The CPU 60x bus interface operates at 166MHz.

5.1 Memory Map

The table below defines the memory map as seen from the PPC7448 while in operation. Please refer to the PowerPC PPC7448 Embedded Processor Data Sheet for more information regarding register maps.

Table 5.1.1: xMon Memory Map

Address	Device
0xFE00,0000 - 0xFFFF,FFFF	Boot Flash (Up to 64 MB)
0xF800.0000 - 0xFDFF,FFFF	Reserved
0xF400,0000 - 0xF7FF,FFFF	Expansion Flash (Up to 64 MB)
0xF111,0000 - 0xF3FF,FFFF	Reserved
0xF110,0000 - 0xF110,FFFF	FPGA Registers and USB
0xF108,0000 - 0xF10F,FFFF	MV64460 Internal SRAM
0xF001,0000 - 0xF107,FFFF	Reserved
0xF100,0000 - 0xF100,FFFF	MV64460 Internal Registers
0xF000,0000 - 0xF0FF,FFFF	PCI IO Space
0x8000,0000 - 0xEFFF,FFFF	PCI Memory Space 1
0x4000,0000 - 0x7FFF,FFFF	PCI Memory Space 0
0x0000,0000 - 0x3FFF,FFFF	SDRAM (Up to 1GB)

5.2 Flash Memory

XPedite6244 supports up to 128MB of surface mount memory via AMD MirrorBit Flash. The Discovery III provides a device bus for interfacing with peripherals. XPedite6244 also supports dual boot mode enabling the user to boot from the alternate flash and have a protected booter in the first flash. The following table gives the peripherals assigned to the chip selects provided by the Discovery III.

Table 5.2.1: Device Chip Select Assignment

Chip Select	Width	Peripheral Device
Device 0	8 bit	Flash0 Boot Flash
Device 1	8 bit	Flash1 Alternate Boot Flash

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5.2.2: Dual Flash Boot

The flash device on chip select 0 or chip select 1 can be used as a boot device. It does this by swapping the chip selects to the device when in Boot Mode. This is useful for loading boot software in the Alternate Boot Flash and reloading it from Flash0 Boot Flash. See the Boot Flash Select in chapter 2 for more information. The memory map remains the same for booting from either flash after the Boot Mode state is exited.

5.3 Real-Time Clock

A real-time clock is provided on XPedite6244 by the ST Microelectronics M41T00 Serial Access Timekeeper.

5.4 Boot Mode

When XPedite6244 is first brought out of reset, the flash interface is initialized in boot-strap mode. In this mode, the first 64KB of the flash boot device is mapped to FFF0,0000. Therefore the first instruction executed is located at offset 0x100 into the flash device. Boot mode is exited when a flash access outside of the 64KB boot window is performed.

An absolute jump instruction to the correct flash memory map must be placed within the first 64KB of the flash to disable boot mode.

5.5 Exception Handling

The XPedite6244 interrupt controller is implemented in the FPGA. Access to the interrupt controller is provided through the device interface bus of the Discovery III. Please refer to the Discovery III user's manual for information on configuring the device interface bus. The following external interrupts are available. Please refer to the FPGA chapter for more information regarding the FPGA.

Table 5.5.1: Interrupt Sources

Interrupt Source	Description
ETH0	Gigabit Ethernet Port 0. The source of this interrupt is the INTR# pin on the BCM5461S Gigabit Ethernet PHY.
ETH1	Gigabit Ethernet Port 1. The source of this interrupt is the INTR# pin on the BCM5461S Gigabit Ethernet PHY.
CPU	CPU Checkstop. Asserted when CPU executes a checkstop.
ETH2 / ETH3	Interrupt from the Intel 82546 Gigabit Ethernet Controller.
DISCC	Discovery III CPU. Asserted when the Discovery III generates a CPU interrupt.
SATA	Interrupt from the Marvell 88SX6041 SATA controller.
USB	Interrupt from the Cypress SL811HS USB controller.

5.6 JTAG Debug Interface

The PPC7448 implements a JTAG interface to support system debugging. The interface enables the connection of an external debug tools, such as RISCWatch. XPedite6244 supports this capability by providing a debug header that can be attached to the external debug tools. The pinout of the debug header is defined in the following table.

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Table 5.6.1: PPC7448 JTAG Header Pin Assignment

Pin	Function	Pin	Function
1	TDO	9	TMS
2	-	10	-
3	TDI	11	SRESET#
4	TRST	12	GND
5	-	13	HRESET#
6	2.5 V	14	-
7	TCK	15	CKSTOP_OUT#
8	-	16	GND

Note: The JTAG port uses 2.5V Signaling

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6. System Controller

This chapter provides a description of the Marvell Discovery III system controller.

The Discovery III provides two integrated PCI bus interfaces, a DDR SDRAM memory controller, three integrated gigabit ethernet controllers, a device bus interface, as well as an elastic 7448 bus interface.

6.1 Reset Configuration

The MV64460 initializes internal registers by sampling IO pins upon removal of reset. The following table describes the configuration as provided by XPedite6244. Please refer to the MV64460 manual for specific configuration details.

Table 6.1.1: Reset Configuration Words

Pins	Configuration Value
DEVAD[31:29]	0b000
DEVAD[28:26]	Configured based on Local PCI Bus Speed and Mode.
DEVAD[25:1]	0b00000111101011000010011001
DEVAD[0]	0b0
DEVWE[3:0]	0b0000
DEVDP[3:0]	0b0000
DEVBA[2:0]	0b101
TXD0[7:0]	0b00000000
TXD1[4:0]	0b00000

6.2 DDR SDRAM Controller

The Discovery III provides an integrated DDR SDRAM controller capable of operating at up 200MHz (400MHz Data Rate). The following table gives the chip select usage for the XPedite6244. Please refer to the MV64460 manual for more information on configuring and operating the memory interface.

Table 6.2.1: SDRAM Chip Select Assignment

Chip Select	Device
CS 0	Bank 0
CS 1	Bank 1 (Stacked Memory)
CS 2	Not Used
CS 3	Not Used

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6.3 Ethernet Controllers

The Discovery III provides three integrated gigabit ethernet controllers. On the XPedite6244, only two of these are used. The following table gives the ethernet controller assignments on XPedite6244. Please refer to the Discovery III hardware manual for configuring and operating the ethernet controllers.

Table 6.3.1: Ethernet Controller Assignment

Ethernet Controller	Port Mode	Usage on XPedite6244
Port 0	RGMII	Front Panel SFP Port.
Port 1	RGMII	Front Panel SFP Port.

The two Discovery III ethernet controller ports interface with two Broadcom BCM5461 10/100/1000 Mbps PHYs. The MV64460 provides a serial management interface (SMI) for configuring and monitoring the Ethernet PHYs. The address assignments of the Broadcom BCM5421s can be found in the following table.

Table 6.3.2: Ethernet Controller Assignment

PHY Address	Device
0x04	BCM5461S Ethernet Controller 0
0x08	BCM5461S Ethernet Controller 1

6.4 Serial Controllers

The Discovery III provides two multi-purpose serial controllers (MPSC). The following table gives the serial controller assignments on XPedite6244. The BClkIn pin (GPP[29]) provides a constant 25Mhz clock for baud rate generation.

Table 6.4.1: MPSC Assignment

Serial Controller	Usage on XPedite6244
MPSC 0	RS232 Port 0
MPSC 1	RS232 Port 1

The MPSC port interfaces with a Maxim 3232 RS232 transceiver.

6.5 I2C Controller

The Discovery III provides an I2C controller. The following devices are located on the I2C bus.

I2C Address	Size	I2C Device Description
1001000	-	ST Microelectronics M41T00 Real Time Clock.
1010000	512 Bytes	Fairchild FM24C04 I2C EEPROM. Used to store non-volatile configuration information and Discovery III configuration information.
1010101	256 Bytes	SDRAM Configuration information.

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6.6 Device Controller

The Discovery III provides a device bus for interfacing with peripherals. The following table gives the peripherals assigned to the chip selects provided by the Discovery III.

Table 6.6.1: Device Chip Select Assignment

Chip Select	Width	Peripheral Device
Boot Device	32 bit	Boot Device / Boot Flash
Device 0	32 bit	Expansion Flash
Device 1	32 bit	FPGA / Local Services / USB
Device 2	-	Reserved
Device 3	-	Reserved

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7. FPGA

This chapter describes details of XPedite6244 local services. This includes the Altera FPGA which performs the following functions:

- Discovery III Device Bus Interface
- Interrupt Controller
- Local control and status registers
- Expansion flash Interface
- USB Interface

7.1 FPGA Register Interface

The following tables describe the details of each register's individual bits.

Table 7.1.1: Configuration Registers

Name	Description	Offset
MFR	Module Family ID	0000H
MID	Module ID	0010H
MRV	Module Revision	0020H
RYBY	Flash Ready/Busy	0050H
MCFG0	Module Configuration 0	0060H
MCFG1	Module Configuration 1	0070H
MCFG2	Module Configuration 2	0080H
TRE	Thermal Reset Enable	0090H
MBM	Module Boot Mode	00A0H
MBME	Module Boot Mode Enable	00B0H

Table 7.1.2: Control Registers

Name	Description	Offset
MRST	Module Reset	0100H
MLED	Module LED Control	0110H

Table 7.1.3: Watch Dog Registers

Name	Description	Offset
WD0C	Watch Dog 0 Control	0120H
WD0S	Watch Dog 0 Service	0130H
WD1C	Watch Dog 1 Control	0140H
WD1S	Watch Dog 1 Service	0150H

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Table 7.1.4: Interrupt Registers

Name	Description	Offset
MIS	Master Interrupt Status	0200H
LIS0	Local Interrupt Status 0	0210H
LIS1	Local Interrupt Status 1	0220H
UIS	User Interrupt Status	0230H
PIS	PCI Interrupt Status	0240H
LIC0	Local Interrupt Control 0	0300H
LIC1	Local Interrupt Control 1	0310H
LIC2	Local Interrupt Control 2	0320H
LIC3	Local Interrupt Control 3	0330H
LIC4	Local Interrupt Control 4	0340H
LIC5	Local Interrupt Control 5	0350H
LIC6	Local Interrupt Control 6	0360H
LIC7	Local Interrupt Control 7	0370H
UIC0	User Interrupt Control 0	0380H
UIC1	User Interrupt Control 1	0390H
UIC2	User Interrupt Control 2	03A0H
UIC3	User Interrupt Control 3	03B0H
PIC0	PCI Interrupt Control 0	03C0H
PIC1	PCI Interrupt Control 1	03D0H
PIC2	PCI Interrupt Control 2	03E0H
PIC3	PCI Interrupt Control 3	03F0H

Table 7.1.5: Masked Interrupt Control

Name	Description	Offset
FEAMSK	Masked Interrupt Control	0400H
IMSK0	Interrupt Masking Register 0	0410H
IMSK1	Interrupt Masking Register 1	0420H
IMSK2	Interrupt Masking Register 2	0430H
ISTS0	Masked Interrupt Status Register 0	0440H
ISTS1	Masked Interrupt Status Register 1	0450H
ISTS2	Masked Interrupt Status Register 2	0460H
FEA	Interrupt Masking Feature Status Register	0480H

Table 7.1.6: I2C 0 Control Registers

Name	Description	Offset
ISCR	I2C Speed / Configuration Register	0800H
IADRL	I2C Address (Lower) Register	0820H

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Name	Description	Offset
IADRU	I2C Address (Upper) Register	0830H
IWCNT	I2C Write Count Register	0840H
IRCNT	I2C Read Count Register	0850H
ICTR	I2C Control Register	0860H

Table 7.1.7: I2C 0 Buffer Registers

Name	Description	Offset
IBUF	I2C Speed / Configuration Register	0C00H - 0FF0H

Table 7.1.8: I2C 1 Control Registers

Name	Description	Offset
ISCR	I2C Speed / Configuration Register	0900H
IADRL	I2C Address (Lower) Register	0920H
IADRU	I2C Address (Upper) Register	0930H
IWCNT	I2C Write Count Register	0940H
IRCNT	I2C Read Count Register	0950H
ICTR	I2C Control Register	0960H

Table 7.1.9: I2C 1 Buffer Registers

Name	Description	Offset
IBUF	I2C Speed / Configuration Register	1000H - 13F0H

Table 7.1.10: SPI Registers

Name	Description	Offset
SRS	SPI Reset Register	0500H
SWD	SPI Write Strobe/Read Data	0510H
SCR	SPI Cycle/Ready Status Register	0520H

7.2 Configuration Register Descriptions

Table 7.2.1: MFM (Module Family Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MFR	R	10H	D7-D0	Module Family Number.

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Table 7.2.2: MID (Module Identification Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MID	R	00H	D7-D0	Module Identification.

Table 7.2.3: MRV (Module Revision Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MRV	R	00H	D7-D0	Module Revision. Indicates revision of XPedite6244 Board.

Table 7.2.4: RYBY (Flash Ready / Busy Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	00H	D7-D2	Reserved (Reads 0)
RB0	R	-	D1	Flash 0 Ready/Busy Indicator
RB1	R	-	D0	Flash 1 Ready/Busy Indicator

Table 7.2.5: MCFG0 (Module Configuration Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CBS	R	-	D7-D6	CPU Bus Speed. Specified by build option. 0 - 150MHz 1 - 200MHz 2 - 100MHz 3 - 133MHz
RSVD	R	00	D5-4	Reserved.
MBS	R	-	D3-2	Expansion Flash Size. Specified by build option. 0 - 8 MB 1 - 16 MB 2 - 32 MB 3 - 64 MB
RSVD	R	0	D1	Reserved.
BFD	R	-	D0	Boot Device Detect 0 - Socketed Flash 1 - Expansion Flash

Table 7.2.6: MCFG1 (Module Configuration Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	-	D7-3	Reserved.

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Field Name	Access Type	Reset Value	Data Bits	Field Description
GA	R	-	D2-0	Module Geographic Address

Table 7.2.7: MCFG2 (Module Configuration Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CPLL	R	-	D7-3	CPU PLL Configuration Multiplier. Specified by build option. 00101 - 2.5 01101 - 6.5 00110 - 3.0 01110 - 7.0 00111 - 3.5 01111 - 7.5 01000 - 4.0 10000 - 8.0 01001 - 4.5 10001 - 8.5 01010 - 5.0 10010 - 9.0 01011 - 5.5 10011 - 9.5 01100 - 6.0 10100 - 10.0
SPLL	R	-	D2-0	System PLL Configuration Speed. Specified by build option. 011 - 100MHz 110 - 166MHz 100 - 133MHz 111 - 200MHz 101 - 150MHz

Table 7.2.8: TRE (Thermal Reset Enable Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-1	Reserved.
EN	RW	0	D0	Thermal Reset Enable 0 - Theremal reset input is disabled 1 - Thermal Reset input will cause a board or cpu reset (depending on MON-ARCH)

Table 7.2.9: MBM (Module Boot Mode Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
BMC	RW	0	D7	Boot Mode Cancel 0 - Boot mode functions as normal 1 - Disables boot mode
RSVD	R	0	D6-1	Reserved.

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Field Name	Access Type	Reset Value	Data Bits	Field Description
BM	R	1	D0	Indicates that the boot flash has been remapped up to the upper address.

Table 7.2.10: MBME (Module Boot Mode Enable Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
BME	W	00H	D7-0	Boot mode enable. Write 5AH to enable boot mode.

7.3 Watch Dog Register Descriptions

Table 7.3.1: WD0S (Watch Dog 0 Service Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
SERV	W	00H	D7-0	Write with alternating pattern of CCH and 33H to maintain this watch dog.

Table 7.3.2: WD0C (Watch Dog 0 Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
SLCT	W	0	D7	Select: 0 - Cause CPU to be reset when the watchdog timer expires. 1 - Cause Board level reset when the watchdog timer expires.
RSVD	R	00H	D6-1	Reserved
ENBL	W	-	D0	0 to disable this watch dog 1 to enable this watch dog

Table 7.3.3: WD1S (Watch Dog 1 Service Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
SERV	W	00H	D7-0	Reserved

Table 7.3.4: WD1C (Watch Dog 1 Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	00H	D7-0	Reserved

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7.4 Configuration Register Descriptions

Table 7.4.1: MRST (Module Reset Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
ERST	RW	0	D7	Ethernet PHY Reset bit. Write 1 to reset. Write 0 to take the PHY out of reset.
RSVD	R	000	D6-D4	Reserved
HRST*	RW	0	D3	CPU HRESET control bit. Writing a 1 to this bit location will cause the CPU to be reset. This is a self clearing bit.
SRST	RW	0	D2	CPU SRESET control bit. Writing a 1 to this bit location will cause an SRESET to be issued. This is a self clearing bit.
PWRST	RW	0	D1	Reset out to Power Supply Monitor. Write 1 to reset. This is a self clearing bit.
PRST	R	0	D0	PCI Bus Reset. Write 1 to reset. This is a self clearing bit.

* Note, causing a HRST will cause the register set to be reset and thus cause the CPU to come out of reset.

Table 7.4.2: MLED (Module LED Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-D5	Reserved
CA2	RW	0	D4	CA2 LED Enable. Writing a 1 to this bit location will light the LED.
CA1	RW	0	D3	CA1 LED Enable. Writing a 1 to this bit location will light the LED.
ALM	RW	1	D2	Red Alarm LED Enable. Writing a 1 to this bit location will light the LED.
ACT	RW	0	D1	Yellow Activity LED Enable. Writing a 1 to this bit location will light the LED.
STS	RW	0	D0	Green Status LED Enable. Writing a 1 to this bit location will light the LED.

7.5 Interrupt Register Descriptions

The following interrupt status registers indicate the state of the pending interrupt from the specified device. A ‘1’ indicates that the interrupt is being driven by the associated device. A ‘0’ indicates that the interrupt is not being driven. Note: The state of the interrupts are always displayed in these registers, even if the interrupt has not been enabled through the interrupt enable registers.

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Table 7.5.1: MIS (Master Interrupt Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
MI	R	-	D7	Master Interrupt Status.
RSVD	R	00	D6-5	Reserved.
FEA	R	-	D4	Masked Interrupt Status.
PIS	R	-	D3	PCI Interrupt Status.
UIS	R	-	D2	User Interrupt Status.
LIS1	R	-	D1	Local Interrupt 1 Status.
LIS0	R	-	D0	Local Interrupt 0 Status.

Table 7.5.2: LIS0 (Local Interrupt Status Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-5	Reserved.
USB	R	-	D4	USB Interrupt Status.
THERM	R	-	D3	Thermal Interrupt Status.
RSVD	R	0	D2	Reserved.
GE1	R	-	D1	Gigabit Ethernet 1 Interrupt Status.
GE0	R	-	D0	Gigabit Ethernet 0 Interrupt Status.

Table 7.5.3: LIS1 (Local Interrupt Status Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	-	D7-5	Reserved.
DISCC0	R	-	D4	Discovery III CPU0 Interrupt Status.
DISCP	R	-	D3	Discovery III PCI Interrupt Status.
RSVD	R	-	D2-1	Reserved.
CPU0	R	-	D0	CPU0 Checkstop Interrupt Status.

Table 7.5.4: UIS (User Interrupt Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7	Reserved.
UINT3	R	-	D6	User Interrupt 3 Status.
RSVD	R	0	D5	Reserved.
UINT2	R	-	D4	User Interrupt 2 Status
RSVD	R	0	D3	Reserved.
UINT1	R	-	D2	User Interrupt 1 Status.
RSVD	R	0	D1	Reserved.

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Field Name	Access Type	Reset Value	Data Bits	Field Description
UINT0	R	-	D0	User Interrupt 0 Status.

Table 7.5.5: PIS (PCI Interrupt Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	-	D7-4	Reserved.
LINTD	R	-	D3	PCI Interrupt D Status.
LINTC	R	-	D2	PCI Interrupt C Status.
LINTB	R	-	D1	PCI Interrupt B Status.
LINTA	R	-	D0	PCI Interrupt A Status.

The following register format applies to the interrupt control registers. Each interrupt control register nibble implements a single interrupt source.

Table 7.5.6: Interrupt Control Register Format

Field Name	Access Type	Reset Value	Data Bits	Field Description
DST	RW	0	D3-0	Interrupt Destination 0x0 - Interrupt Disabled 0x1 - Reserved 0x2 - CPU0 0x3 - Reserved 0x4 - PCI Interrupt A 0x5 - PCI Interrupt B 0x6 - PCI Interrupt C 0x7-0xB - Reserved 0xC - Auxiliary Interrupt 0 0xD - Auxiliary Interrupt 1

Table 7.5.7: LIC0 (Local Interrupt Control Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
GE1	RW	0	D7-4	Gigabit 1 Interrupt Control.
GE0	RW	0	D3-0	Gigabit 0 Interrupt Control.

Table 7.5.8: LIC1 (Local Interrupt Control Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-0	Reserved.

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Table 7.5.9: LIC2 (Local Interrupt Control Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-4	Reserved.
THRM	RW	0	D3-0	Thermal Interrupt

Table 7.5.10: LIC3 (Local Interrupt Control Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-0	Reserved.

Table 7.5.11: LIC4 (Local Interrupt Control Register 4)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-4	Reserved.
CPU0	RW	0	D3-0	CPU0 Checkstop Interrupt Control.

Table 7.5.12: LIC5 (Local Interrupt Control Register 5)

Field Name	Access Type	Reset Value	Data Bits	Field Description
DISCP	RW	0	D7-4	Discovery III Primary PCI Interrupt Control.
RSVD	RW	0	D3-0	Reserved.

Table 7.5.13: LIC6 (Local Interrupt Control Register 6)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
DISCC0	RW	0	D3-0	Discovery III CPU0 Interrupt Control.

Table 7.5.14: LIC7 (Local Interrupt Control Register 7)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-4	Reserved.
USB	RW	0	D3-0	USB Interrupt Control.

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Table 7.5.15: UIC0 (User Interrupt Control Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
UIC0	RW	0	D3-0	User Interrupt 0 Control.

Table 7.5.16: UIC1 (User Interrupt Control Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
UIC1	RW	0	D3-0	User Interrupt 1 Control.

Table 7.5.17: UIC2 (User Interrupt Control Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
UIC2	RW	0	D3-0	User Interrupt 2 Control.

Table 7.5.18: UIC3 (User Interrupt Control Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
UIC3	RW	0	D3-0	User Interrupt 3 Control.

Table 7.5.19: PIC0 (PCI Interrupt Control Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
LINTB	RW	0	D7-4	PCI INTB Interrupt Control.
LINTA	RW	0	D3-0	PCI INTA Interrupt Control.

Table 7.5.20: PIC1 (PCI Interrupt Control Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
LINTC	RW	0	D3-0	PCI INTC Interrupt Control.

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Table 7.5.21: PIC2 (PCI Interrupt Control Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-0	Reserved.

Table 7.5.22: PIC3 (PCI Interrupt Control Register 3)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-0	Reserved.

7.6 Masked Interrupt Control Register Descriptions

This register set controls the FEA interrupt. It is used if a user application needs the capability to combine several interrupts and route them to a single destination. the FEA interrupt is generated by masking all system interrupts and performing a logical OR on the result.

Table 7.6.1: FEAMSK (Masked Interrupt Control)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-4	Reserved.
INTC	RW	0	D3-0	Masked Interrupt Routing Select

Table 7.6.2: IMSK0 (Interrupt Masking Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CPU0	RW	0	D7	CPU0 Interrupt Mask
D_P	RW	0	D6	Discovery III Primary PCI Interrupt Mask
RSVD	R	0	D5	Reserved
CPU0	RW	0	D4	CPU 0 Checkstop Interrupt Mask
THRM	RW	0	D3	Thermal Interrupt Mask
RSVD	R	0	D2	Reserved
GIGE1	RW	0	D1	Gigabit Ethernet 1 Interrupt Mask
GIGE0	RW	0	D0	Gigabit Ethernet 0 Interrupt Mask

Table 7.6.3: IMSK1 (Interrupt Masking Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
LINTC	RW	0	D7	PCI INTC Interrupt Mask
LINTB	RW	0	D6	PCI INTB Interrupt Mask
LINTA	RW	0	D5	PCI INTA Interrupt Mask

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Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D4-2	Reserved
USB	RW	0	D1	USB Interrupt Mask
DISCC0	RW	0	D0	Discovery III CPU0 Interrupt Mask

Table 7.6.4: IMSK2 (Interrupt Masking Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-0	Reserved.

NOTE: For the masked interrupt status registers, writing a 1 to any bit position will clear the interrupt.

Table 7.6.5: ISTS0 (Masked Interrupt Status Register 0)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CPU0	RW	0	D7	CPU0 Interrupt Status
D_P	RW	0	D6	Discovery III Primary PCI Interrupt Status
RSVD	R	0	D5	Reserved
CPU0	RW	0	D4	CPU 0 Checkstop Interrupt Status
THRM	RW	0	D3	Thermal Interrupt Status
RSVD	R	0	D2	Reserved
GIGE1	RW	0	D1	Gigabit Ethernet 1 Interrupt Status
GIGE0	RW	0	D0	Gigabit Ethernet 0 Interrupt Status

Table 7.6.6: ISTS1 (Masked Interrupt Status Register 1)

Field Name	Access Type	Reset Value	Data Bits	Field Description
LINTC	RW	0	D7	PCI INTC Interrupt Status
LINTB	RW	0	D6	PCI INTB Interrupt Status
LINTA	RW	0	D5	PCI INTA Interrupt Status
RSVD	R	0	D4-2	Reserved
USB	RW	0	D1	USB Interrupt Status
DISCC0	RW	0	D0	Discovery III CPU0 Interrupt Status

Table 7.6.7: ISTS2 (Masked Interrupt Status Register 2)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-0	Reserved.

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Table 7.6.8: FEA (Interrupt Masking Feature Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	RW	0	D7-1	Reserved.
PRES	R	1	D0	Interrupt Masking Feature Status Indicator. Reads 1 if feature is enabled.

7.7 I2C Control Register Descriptions

Note: These descriptions apply to both I2C Master 0 and Master 1.

Table 7.7.1: ISCR (I2C Speed / Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
10BT	RW	0	D7	Ten Bit address enable 0 - Do not use 10 bit addressing 1 - Use 10 bit addressing
RSVD	RW	0	D6-3	Reserved.
SPED	RW	0	D2-1	I2C Speed control: 00B - Use 100 KHz 01B - Use 400 KHz 10B - Reserved 11B - Reserved
RSVD	RW	0	D0	Reserved.

Table 7.7.2: IADRL (I2C Address Lower Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
ADRL	RW	0	D7-0	I2C Address (Lower)

Table 7.7.3: IADRU (I2C Address Upper Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
ADRU	RW	0	D7-0	I2C Address (Upper)

Table 7.7.4: IWCNT (I2C Write Count Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
IWCNT	RW	0	D7-0	I2C Write Count

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Table 7.7.5: IRCNT (I2C Read Count Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
IRDCNT	RW	0	D7-0	I2C Read Count

Table 7.7.6: ICTR (I2C Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CYC	RW	0	D7	I2C Cycle indication. Write 1 to start I2C cycle. On read: 0 - No I2C Cycle in progress 1 - I2C Cycle in progress
RSVD	RW	0	D6-1	Reserved.
ERR	RW	0	D0	I2C Error status. Cleared at begining of next I2C cycle. On read: 0 - Last I2C transfer completed sucess-fully 1 - Error occured during last I2C transfer

7.8 I2C Data Buffer Register Description

Note: This description applies to both I2C Master 0 and Master 1.

Table 7.8.1: IBUF (I2C Read/Write Buffer Registers)

Field Name	Access Type	Reset Value	Data Bits	Field Description
IBUF	RW	0	D7-0	I2C write data / read data buffers. Not that the read buffer is read only and the write buffer is write only.

7.9 SPI Register Descriptions

Table 7.9.1: SRS (SPI Reset Status Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RSVD	R	0	D7-1	Reserved.
IRST	R	-	D0	SPI (IPMI) Reset Status.

Table 7.9.2: SWD (SPI Data Write/Read Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
RD	R	-	D7-0	SPI Read Data.
WR	W	-	D7-0	SPI Write Data.

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Table 7.9.3: SCR (SPI Control Register)

Field Name	Access Type	Reset Value	Data Bits	Field Description
CYCLE	RW	0	D7	SPI Cycle Control
RSVD	R	0	D6-0	Reserved.

7.10 USB Interface Description

The USB interface is provided by a Cypress Semiconductor SL811HS device. The interface is located in the FPGA address space at offset 0x8000. Accesses to and from the Cypress device are done via a bus that utilizes a multiplexed address/data bus that is controlled by address line A0. Operation is as follows :

Table 7.10.1: Read Cycle Procedure

Address	Read/ Write	Description
0x8000	Write	Register or Memory Address
0x8010	Read	Read Data

Table 7.10.2: Write Cycle Procedure

Address	Read/ Write	Description
0x8000	Write	Register or Memory Address
0x8010	Write	Write Data

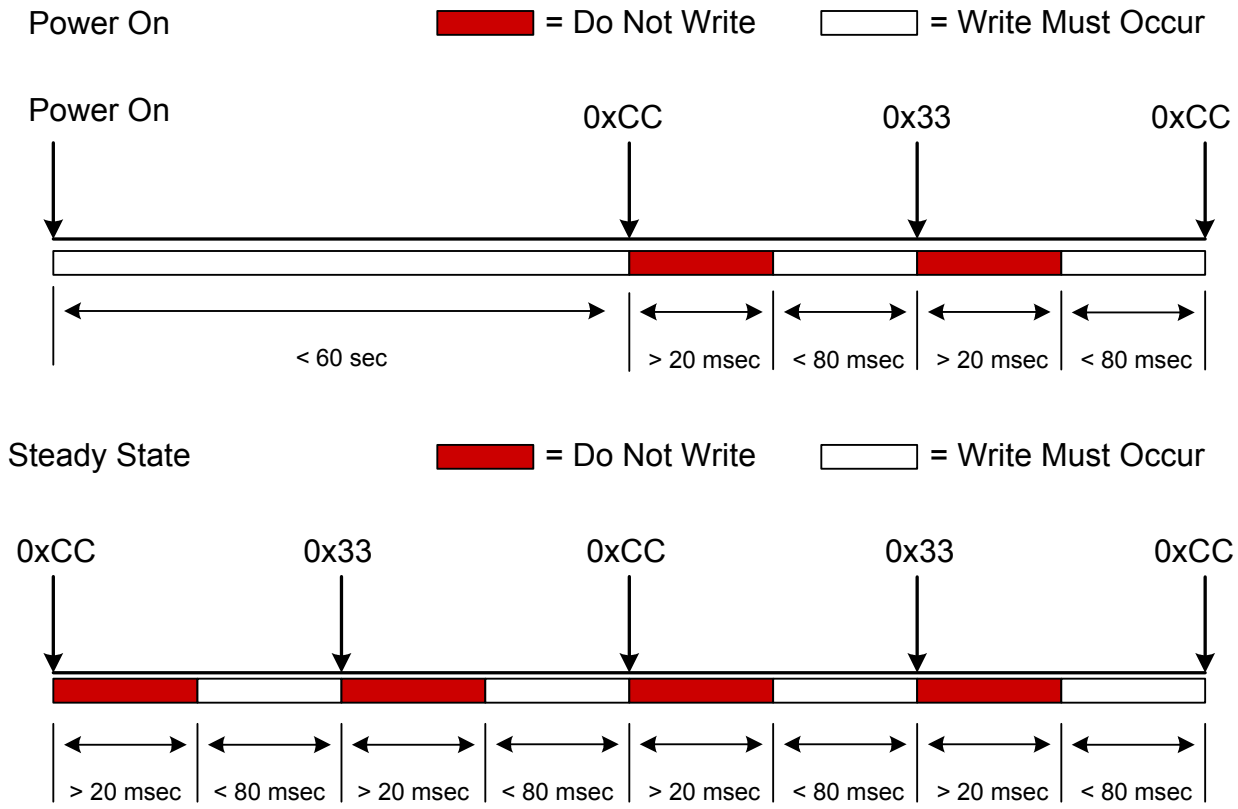
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7.11 Software Watchdog Reset Timer

The FPGA provides two watchdog reset timers (one for each CPU) to prevent system lockup in the case where software becomes trapped in a loop or is stuck in an interrupt handler. The watchdog timer may be enabled or disabled by default depending on a build option. The watchdog timer can be enabled by setting the ENBL bit in the WDnC (Watch Dog Control Register), but after enabled, the watchdog timer will not trigger a reset for 60 seconds. If the watchdog timer's service routine does not begin within 60 seconds, either a cpu reset or a PCI RSTOUT reset (As controlled by the SLCT of the bit of the WDnC register). After the watchdog service routine starts, the software watchdog timer service sequence must be executed periodically. Without this periodic servicing, the software watchdog timer will timeout and issue a reset. The watchdog timer can be disabled by clearing the ENBL bit in the WDnC register.

During the initial 60 second period after enabled, software must write 0xCC to the WDnS (Watch Dog n Service Register) and wait 50ms +/- 30ms to write the next data in the sequence, 0x33. Before starting the 0xCC/0x33 sequence again, software must again wait for the next time period of 50ms +/- 30ms.

Figure 7.11.1: Watchdog Reset Timer



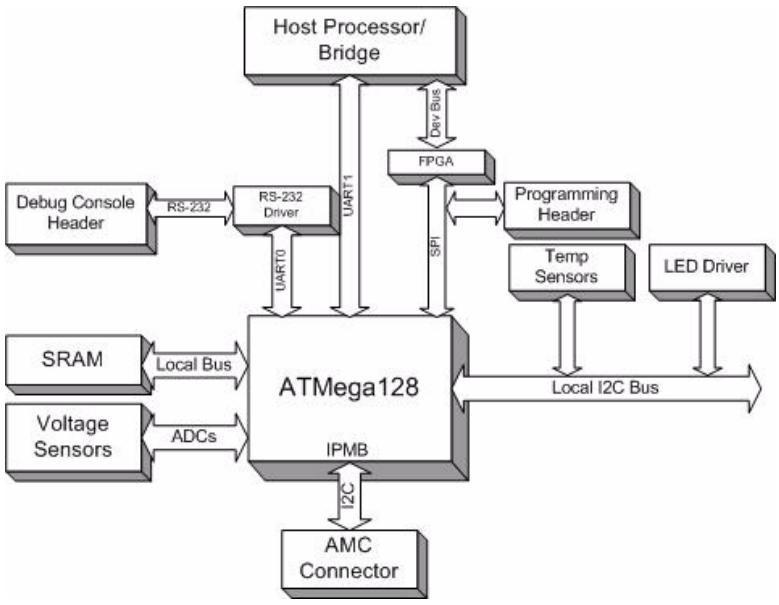
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8. IPMI

XPedite6244 implements an IPMI MMC (Module Management Controller) as per the PICMG AMC.0 R1.0 Specification. It implements an IPMB-L interface to the AMC connector, which the AMC Carrier's or uTCA chassis' IPMC (Intelligent Platform Management Controller) uses to access XPedite6244's sensors and FRU data. XPedite6244 implements a SPI system interface that can be used to field upgrade the MMC firmware from the host processor, as well as a UART interface to allow communication between the MMC and host processor. This chapter covers the implementation of IPMI on XPedite6244.

The IPMI interface is implemented with the Atmel ATMega128 microcontroller. This high-performance, low-power 8-bit AVR microcontroller is capable of up to 8 MIPS at 8MHz. It provides 128K bytes of internal Flash, 4K bytes of internal EEPROM, and 4K bytes of internal SRAM. An additional 64K of external SRAM is provided. A built in I2C controller interfaces with the IPMB (Intelligent Platform Management Bus).

8.1 Block Diagram



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8.2 ATMega128 Pin Usage

The ATMega128 microcontroller provides general purpose input and output pins. This following table documents the usage of these pins.

Table 8.2.1: ATMega128 Pin Assignments

Atmel A/D Port	Assignment
PD4	IPMB-L Geographical Address 0
PB7	IPMB-L Geographical Address 1
PB6	IPMB-L Geographical Address 2
PE7	Hot Swap Microswitch
PE3	Reset control line. Driving a logic zero will reset the XPedite6244.

8.3 I^2C Interfaces

Two I2C buses are implemented using the Atmel ATMega128. The following table documents the pin usage for this function.

Table 8.3.1: I^2C Pin Assignments

Atmel A/D Port	Assignment
PD0	IPMB SCL
PD1	IPMB SDA
PD2	LOCAL SCL
PD3	LOCAL SDA

8.4 Non-Volatile Storage

The Atmega128L internal EEPROM is used for Non-Voltatile Storage.

8.5 Temperature Sensor

Two Dallas DS1631 Digital Thermometers are used to monitor ambient temperature on XPedite6244. This sensor is accurate to 0.5C and has a range from 0C to 70C. The I^2C address of these devices are 1001000B and 1001001B.

8.6 Voltage Sensors

The Atmel ATMega128 provides 8 A/D converters. The following have been assigned to voltage level monitoring.

Table 8.6.1: Voltage Sensor Pin Assignments

Atmel A/D Port	Voltage
ADC0	Reserved
ADC1	Payload 3.3V

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Atmel A/D Port	Voltage
ADC2	Payload 2.5V
ADC3	Reserved
ADC4	Payload 1.5V
ADC5	Payload 1.25V
ADC6	Payload Processor Core
ADC7	Payload 1.0V

8.7 SPI System Interface

The SPI System interface is implemented in the FPGA and allows the MMC's firmware to be field upgraded from the host processor.

8.8 UART Interfaces

Two UART interfaces are provided by the Atmega128L. UART0 is routed to an RS-232 driver, which is routed to a three pin console debug header. UART1 is routed to the host processor's MPSC1 to allow communication between the MMC and the payload.

8.9 Programming Header

The XPedite6244 provides a 6-pin header to allow programming of the Atmega128L via an AVR ISP programming adapter.

8.10 IPMI Command Set

The ATMega128 functions as a Module Management Controller (MMC), implementing the following commands accessible over IPMB-L. Each supported command is listed with its IPMI Network Function Code (NetFn) and Command code number (Cmd). Refer to the IPMI Specification v1.5 for more information about individual commands.

Table 8.10.1: IPMI Command Set

Command	NetFn	Cmd
Get Device ID	Application	0x01
Broadcast 'Get Device ID'	Application	0x01
Cold Reset	Application	0x02
Warm Reset	Application	0x03
Get Self Test Results	Application	0x04
Send Message	Application	0x34
Master Write-Read	Application	0x52
Set Event Receiver	Sensor/Event	0x00
Get Event Receiver	Sensor/Event	0x01
Platform Event	Sensor/Event	0x02
Get Device SDR Info	Sensor/Event	0x20
Get Device SDR	Sensor/Event	0x21

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Command	NetFn	Cmd
Reserve Device SDR Repository	Sensor/Event	0x22
Get Sensor Reading Factors	Sensor/Event	0x23
Set Sensor Threshold	Sensor/Event	0x26
Get Sensor Threshold	Sensor/Event	0x27
Get Sensor Reading	Sensor/Event	0x2D
Set Sensor Type	Sensor/Event	0x2E
Get Sensor Type	Sensor/Event	0x2F
Get FRU Inventory Area Info	Storage	0x10
Read FRU Data	Storage	0x11
Write FRU Data	Storage	0x12
Enter SDR Repository Update Mode	Storage	0x2A
Exit SDR Repository Update Mode	Storage	0x2B
Get PICMG Properties	PICMG	0x00
FRU Control	PICMG	0x04
Get FRU LED Properties	PICMG	0x05
Get LED Color Capabilities	PICMG	0x06
Set FRU LED State	PICMG	0x07
Get FRU LED State	PICMG	0x08
Get Device Locator Record ID	PICMG	0x0D
FRU Control Capabilities	PICMG	0x1E

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8.11 IPMI Sensor Numbers

IPMI Sensor Commands such as ‘Get Sensor Reading’ use Sensor Numbers to address monitoring devices attached to the ATMega128L IPMI Management Controller.

Table 8.11.1: IPMI Sensor Numbers

Sensor Description	LUN	Sensor Number
1.0V Supply Monitor - PEX 8114	0x00	0x41
VCORE Supply Monitor - 7448 CORE	0x00	0x42
1.25V Supply Monitor - DDR MEM	0x00	0x43
1.5V Supply Monitor - MV64460	0x00	0x44
2.5V Supply Monitor - DDR MEM	0x00	0x45
3.3V Supply Monitor - Voltage Rail	0x00	0x46
Temperature Sensor - Board Temp	0x00	0x60
Temperature Sensor - Inflow Temp	0x00	0x61

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