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WAVETEK

MAINTENANCE MANUAL

Model 1375
20 MHz VXI Arbitrary Waveform Generator

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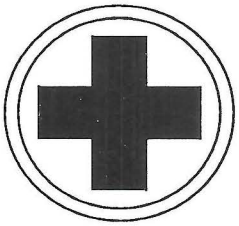
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- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

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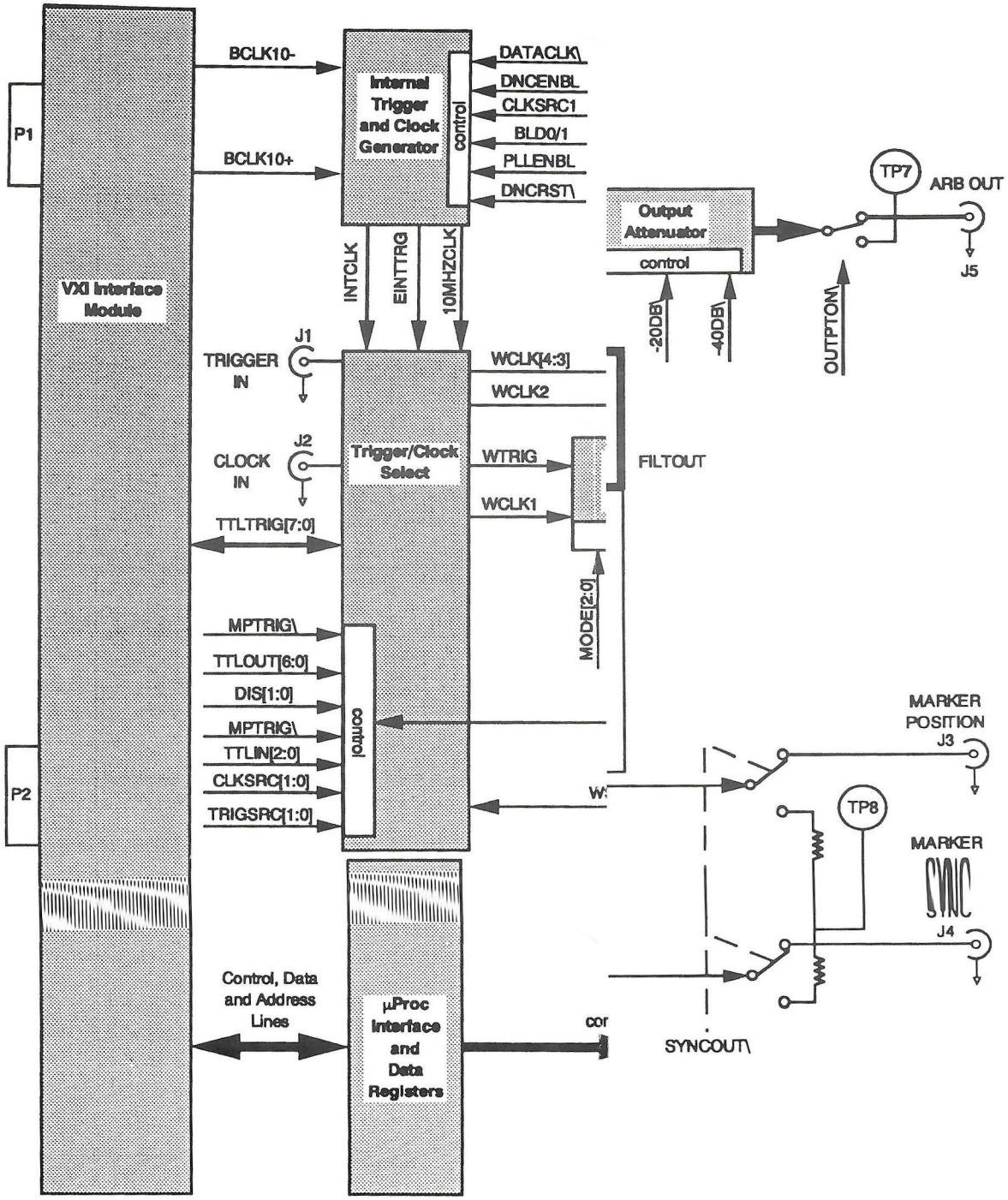


Figure1-1. Model 1375 Overall Block Diagram

SECTION 1
CIRCUIT DESCRIPTION

1.1 INTRODUCTION

Figure 1-1 shows the Wavetek Model 1375 Arbitrary Waveform Generator (Arb) VXI module block diagram. The VXIbus connects to the module at backplane connectors P1 and P2, which supply the module with a VME digital interface, power supplies, trigger lines and a master clock. The module contains three printed circuit boards: the VXI Interface Board, RAM Module and the Arb Board. The VXI Interface Board receives inputs from the P1 and P2 connectors and provides an interface between the VXIbus and the Arb Board. The Arb Board receives control signals and data from the interface and generates arbitrarily defined voltage waveforms. The RAM Module plugs into the Arb Board with a standard 32 k or optional 128 k complement of waveform memory.

Under the direction of its commander (and more directly, the VXI interface board), the Wavetek Model 1375 Arbitrary Waveform Generator module produces: 1) arbitrarily defined waveforms at the ARB OUT BNC connector; 2) a pulse at the MARKER POSITION BNC connector for each point identified by the user as a marker, and; 3) at the MARKER SYNC BNC connector a waveform synchronization signal. It also receives external triggering and clocking inputs at the TRIGGER IN and CLOCK IN BNCs.

1.1.1 General Overview of Arbitrary Waveform Generation

To generate an arbitrary waveform, a sequential definition of the trace amplitude vs time (X/Y plot) is required. This is achieved through the use of Direct Digital Synthesis (DDS) techniques. The DDS Waveform Generation Circuits include the Address Generator, Waveform Memory, and Waveform DAC. The Address Generator employs a DDS technique known as *phase accumulation*. The waveform memory RAM provide a look-up table of the arbitrarily defined waveform. The DAC converts digital data values into voltage levels. Analog circuits prepare the DDS generated waveform for the output connector.

1.1.1.1 Address Generator

For the Model 1375, the Address Generator is the Wavetek proprietary CMOS ASIC device, "PA4800". It generates addresses for the waveform memory through phase accumulation. Figure 1-2 illustrates the Phase Accumulator.

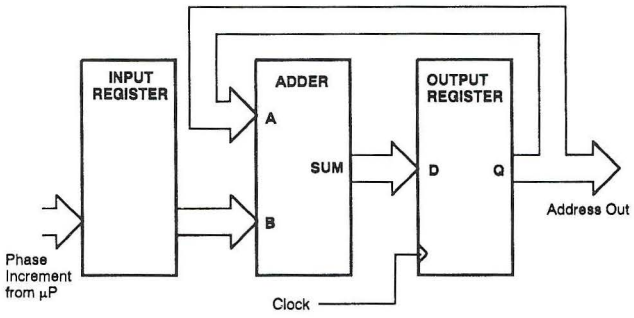


Figure 1-2. Phase Accumulator Block Diagram.

Based on the programmed frequency, the microprocessor calculates a phase increment value and applies it to the Input Register of the PA4800. This phase increment value is then applied to the B input of the adder and held constant until a new frequency is programmed. The sum of the A and B inputs is applied to the Output Register D input, and, on a clock edge, is transferred to the Q output as an address. The address is also sent back to the Adder's A input where it is summed with the phase increment on the next clock edge. Therefore, the value seen at Address Out following each clock cycle is the previous address value increased by the phase increment value. The beginning address is a low value that increases by a fixed amount (the phase increment value) on each "tick" of the time clock. When the Address overflows the adder, it returns to a low value. The programmed frequency, clock frequency, and size of the adder determine the phase increment value, with the adder overflowing at the programmed frequency rate. If this

Address were connected directly to a DAC, the analog output would be a positive-going ramp at the programmed frequency. The PA4800 has a 48 bit adder, so overflow occurs when 2^{48} is exceeded, and extremely small differences in frequency can be expressed (1 part in 2^{48}).

1.1.1.2 Waveform Memory

The Address from the PA4800 is translated by a Waveform Memory RAM programmed with one or more waveform look-up tables. Figure 1-3 shows the resulting data being applied to the DAC.

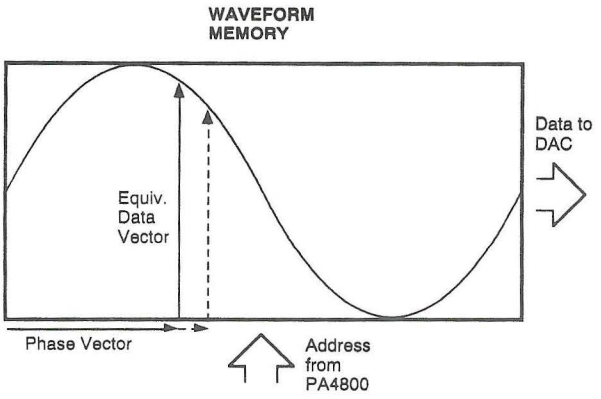


Figure 1-3. Waveform Memory.

The figure represents Address value as a quantity that is increasing from left to right, while the waveform data value increases from bottom to top. A particular address value can be represented as a phase vector (the horizontal arrow), which corresponds to a particular amplitude data vector (the vertical arrow). The next clock cycle adds one phase increment (the dashed horizontal line), which generates a new amplitude vector (the dashed vertical line). Because of the equal time and phase spacing between amplitude vectors, any series of vectors will generate digitized waveforms.

1.1.1.3 Waveform DAC

The Digital to Analog Converter (DAC), shown as U47 on sheet 8 of the Model 1375 schematic, converts digital amplitude values into an analog signal. The instantaneous digital value at the DB1 through DB12 inputs determines the instantaneous current at the OUT+ output, with the complementary current at the OUT- output. The 40 mA full-scale output currents develop a 1 Vp-p differential voltage signals across R39 and R40. The digital inputs are the Waveform Memory data outputs, resynchronized to the clock signal by data registers U45 and U46.

1.1.1.4 Analog Waveform Circuitry

A switchable filter may be used to remove the sampling frequency or to "reconstruct" waveshapes defined by only a few points. An enlarged view of the waveform out of the DAC will show discrete steps instead of a smooth line. The filter smooths the waveform by suppressing hf components that would otherwise be seen at the output. A preamp is placed between the DAC output and the filter input for voltage/current gain and isolation. The output amplifier provides the necessary current and voltage gain to deliver the desired amplitude to the load.

1.2 VXI INTERFACE BOARD

All operating instructions and data for the Model 1375 module originate from its commander, located within the VXI chassis. The VXI Interface Board, mounted within the Model 1375 module, transfers signals between the Arb and the VXIbus. An eight-position rocker switch located on the interface board determines the module's logical address.

Because of its high density, multi-layer printed circuit card utilizing LSI and custom ASIC surface mount parts, the Interface Board is documented in this manual only as necessary to support repair at the factory. Maintenance information is provided to aid in fault isolation to the board level.

1.2.1 VXI Overview

A block diagram of the VXI Interface Board is given in Figure 1-4. The VXIbus is contained in the chassis' backplane, and interconnects to the 1375 module P1 and P2 connectors. Refer to the VXIbus System Specifications for electrical specifications of the P1 and P2 connectors, the CLK10 line, the MODID line, the TTLTRG0-7 lines, and the TTLTRG* protocols if detailed information is needed on the inputs to the VXI Interface Board.

The VXI System Specifications will also provide system architecture information that will be of help to understand the various tasks that the interface board performs. For Wavetek's implementation, the following sections should be understood: Device Overview, Message Based Devices, Message Based Device Communication Protocols, VXIbus and IEEE-488.2 Instrument Protocols, Shared Memory, and Dynamic Configuration. The Wavetek VXI chip is an ASIC device which implements these protocols, under direction of the interface 68HC000 CPU and system firmware.

1.2.2 Interface Board

The block diagram segments the Interface Board into a VXI INTERFACE block, a CPU & MEMORY block and an INSTRUMENT INTERFACE block.

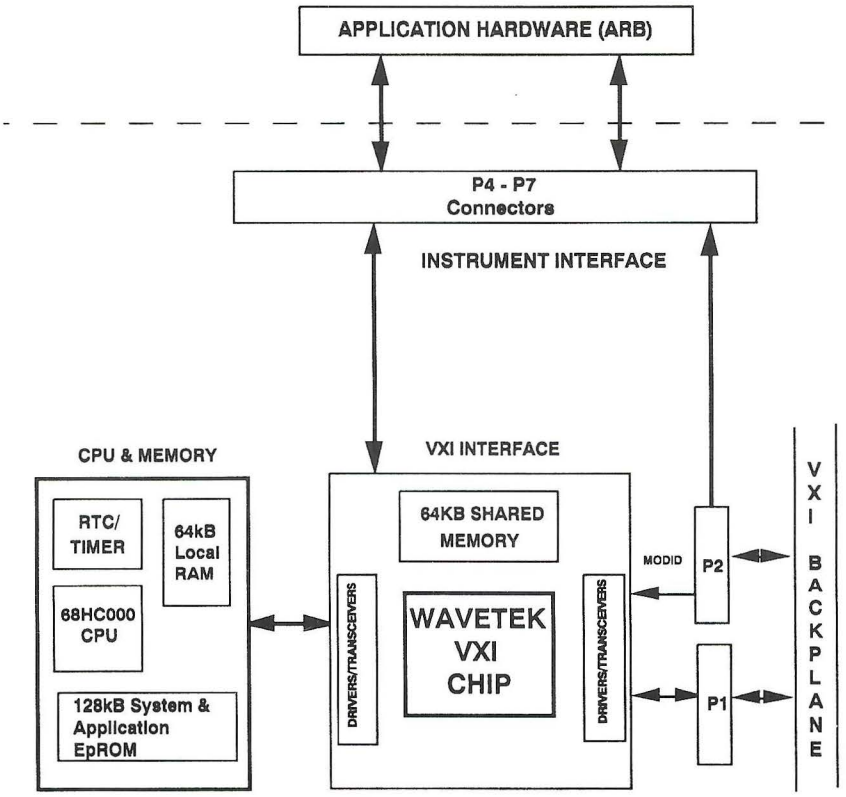


Figure 1-4. VXI Interface Board Block Diagram.

The VXI INTERFACE block contains the P1 and P2 connectors, the VXI ASIC device, the Shared Memory RAM, module addressing, and various drivers and transceivers. The VXI ASIC device implements the complete VXI Message Based Device interface. It generates control signals that regulate the transfer of data between the interface CPU and the VXIbus. The VXI A16 registers are located within the ASIC. It also controls the RUN, FAIL, MODID, A16 and A32 LEDs on the module's front panel. The VXI interface contains 64k x 8 RAM which may be used for Shared Memory Protocols to efficiently move large quantities of data. The Logical Address Switch and Dynamic Configuration jumpers are explained in the 1375 Operator's manual.

The CPU & MEMORY block contains the microprocessor, local RAM and ROM, decoders, a real time clock/timer, the interrupt controller, a bus error timer and various drivers and transceivers. The local ROM consists of 128k of EpROM containing VXI System and Application (the 1375 ARB) memory. There is also 32k of local static RAM to hold transient data required by the microprocessor. The real time clock provides timer and event capability. Up to seven interrupt inputs may be priority encoded; three from the application (not used in the 1375), three from the VXI ASIC, and one from the real time clock. The bus error timer generates a local BERR\ signal if data transfer acknowledgment (local DTACK\) is not given before time-out occurs. BERR\ is generated if a microprocessor access cycle exceeds 16 µs.

The INSTRUMENT INTERFACE block consists of connectors P4 through P7. The pinouts and signal names of the interface between the VXI Interface Board and the Arb Board are shown in sheet 1 of the Arb Board schematic, 1104-00-3286, in Section 4 of this manual. These address, data, and control signals are described in paragraph 1.3.2 and are illustrated in Figure 1-5.

1.3 ARB BOARD AND RAM MODULE

Refer to Figure 1-1, other indicated figures, and the Arb Board schematic 1104-00-3286 in Section 4 of this manual for the following paragraphs.

1.3.1 Interconnect and Power Distribution

Sheet 1 of the Model 1375 schematic shows all of the connections between the VXI Arb and the VXI interface board. All power supplies and instrument control originates from the VXI interface board. Coded lines are identified as follows: 'A' for address; 'D' for

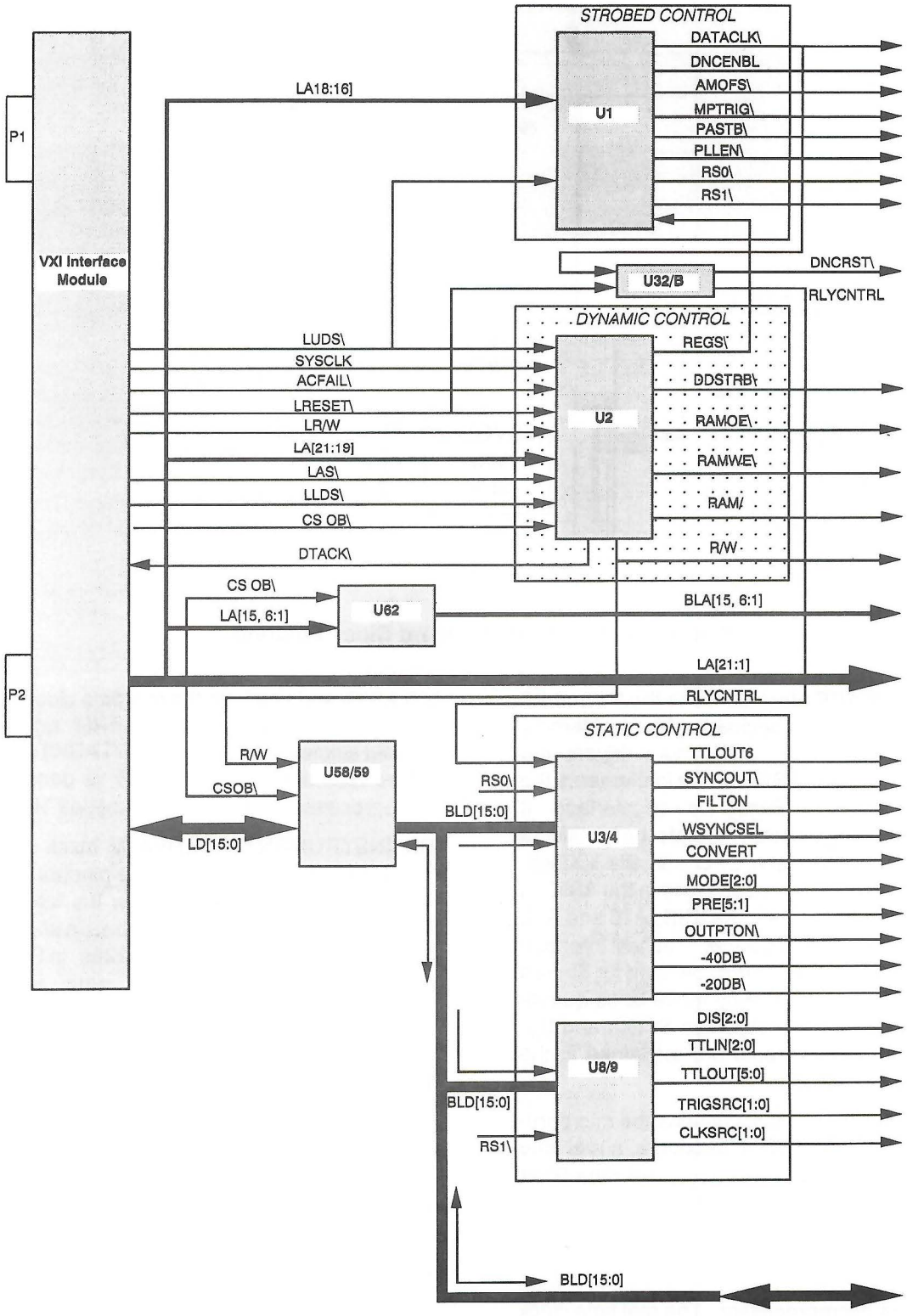


Figure 1-5. Digital Interface and Data Registers

'L' for a VXI Interface Board origin, and 'B' for a buffered line. Each front panel LED is independently enabled (logic low) or disabled (logic high) by the VXI Interface Board through control lines VA16 LD\, MID_LD\, FAIL_LD\ and RUN_LD\.

1.3.2 Digital Interface and Data Registers

Refer to Figure 1-5 and VXI Arb schematic sheet 2. Three types of digital control signals direct the Model 1375 Arb operations: dynamic control, strobed control, and static control. Dynamic control lines originate from programmable logic device U2. These lines are synchronized to SYSCLK (system clock) and are controlled by LAS\ (address strobe) and LUDS\ (data strobe) to insure proper timing. When an address change is made, LAS\ is enabled after the 21 address lines have settled. Similarly, LUDS\ is enabled after the 16 data bus lines have stabilized following a data change. Address lines are always controlled by the VXI Interface Board, and travel one way to the Arb board. Data lines are bidirectional between the interface and Arb.

U2 acknowledges successful data transfer between the Arb and VXI Interface Board (DTACK\), enables the diagnostic circuit (schematic sheet 12) to transfer test results to the VXI Interface Board (DDSTRB\) and controls all RAM MODULE operations (R/W, RAMOE\, RAMWE\, and RAM\). It also enables U1 (REGS\) and determines the direction of data flow through U58 and U59 (R/W). RAM\ is enabled during any read or write operation between the RAM MODULE and the VXI Interface Board, with R/W controlling the direction of data flow to or from RAM. RAMWE\ is pulsed low while data is being written to RAM from the VXIbus interface. RAMOE\ directs the RAM MODULE (schematic sheet 6) to output trace data, and is nearly always enabled (low).

When both REGS\ (from U2) and LUDS\ (from the VXI Interface Board) are low, 3 to 8 line decoder U1 briefly enables (pulses low) one of eight control lines (Y0 through Y7), as determined by the status of address lines LA[18:16]. These eight control lines direct the operation of the internal trigger and clock sources (DATACLK\ and DNCENBL\), burst counter (DNCENBL\), amplitude and offset DAC (AMOFS\), phase accumulator (PASTB\), phase lock loop (PLLEN\ and DATACLK\) and provide the microprocessor trigger (MPTRIG\). In addition, two of these control lines (RS0\ and RS1\) are clocks to the four octal 'D' type flip/flops, U3, U4, U8 and U9 that combine to create two 16 bit registers.

These two registers drive 32 static control lines that are dispersed throughout the instrument to direct the phase lock loop (CLKSRC1), clock source (CLKSRC[1:0]), trigger source (TRIGSRC0), backplane clock output (TTLOUT[3:0]), backplane trigger output (TTLOUT[6:4] and DIS[1:0]), backplane receiver (TTLIN[2:0]), mode controller (MODE[2:0]), filter (FILTON), pre-attenuator (PRE[5\:1\]), output attenuator (-20DB and -40DB), output relay (OUTPTON\), marker circuit (SYNCOUT\ and WSYNCSEL), and diagnostics (CONVERT, DIS[2:0]).

If pin 1 of U3 and U4 is high, all outputs are at a high impedance, blocking any data from exiting the flip flops. With pin 1 of U3, U4, U8 and U9 low, and following the rising edge of pin 11 (RS0\ for U3 and U4, RS1\ for U8 and U9), all output pins (12 through 19) of the four flip flops are latched to the same state as their respective input pins (2 through 9) from U58 and U59.

During power-up, the LRESET\ signal at U32 pin 13 forces pin 9 (DNCRST\) low and pin 8 (RLYCNTRL) high. This disables U3 and U4, and resets U16 (sheet 3), U17 (sheet 3), and U30 (sheet 5). Following power-up, the Arb hardware is initialized by setting up data patterns on registers U3, U4, U8 and U9.

When the VXI interface board initiates an I/O operation external to the microprocessor, address register U62 is enabled by pin 1 (CSOB\) being pulled low, buffering the address bus. The output pins (11 through 17) match each corresponding input pin (3 through 9). If an I/O operation is not initiated, pin 1 remains high, leaving all outputs in a high impedance state.

U58 and U59 combine to make up a 16 bit transceiver. If pin 19 (CSOB\) is high, all data lines are in a high impedance state and therefore isolated. However, if pin 19 is low, data flows from the VXI interface board to the buffered data lines when pin 1 (R/W) is high, and from the buffered data lines to the VXI Interface Board when pin 1 is low.

1.3.3 Instrument Triggering

Figure 1-6 shows the entire trigger circuitry. When in any mode other than continuous, the address generator block must receive a trigger signal (WTRIG) for the Arb to operate.

Sources available for triggering the Arb are, internal (INTTRG\ from U17), external (EXTTRG\), digital bus (MPTRIG\) and the VXI bus TTL trigger lines 0, 2, 4 and 6. MPTRIG\ triggering, controlled by U1 (schematic sheet 2) must be done through U26. Internal or external triggering may be selected directly by U26, or passed through the backplane for use by the Arb and other instruments.

The internal trigger circuit translates the differential ECL CLK10 signals (BCLK10- and BCLK10+) from the backplane to a TTL level signal (10MHZCLK).

Counter U17 divides this signal down to a frequency of between 1mHz and 2MHz. The external trigger originates from the front panel TRIG IN connector. U22 conditions the signal before passing it on to U19 and U26. The zero crossing, beginning bits and marker position signals are all present in the marker sync circuit. See paragraph 1.2.12 for descriptions of these signals.

U19 chooses one of four trigger inputs to be placed on the backplane. U20/B selects one of the four backplane lines. U21/B provides signal drive for the selected TTL trigger line. Selection of the backplane line used to trigger the instrument is made by U23. U26 selects from the internal, external, and TTL trigger sources to trigger the address generator through WTRIG.

1.3.3.1 Internal Trigger Source

Sheet 3 of the VXI Arb schematic shows the internal trigger circuit. U17 divides the 10 MHz signal present at pin 4 by an integer as large as 236. The output period at pin 20 is equal to 100 ns multiplied by the programmed value. For example, if the programmed value is 11, the output period is 11 x 100 ns, or 1.1 μs. This output (pin 20) is a TTL active low pulse equal in width to one clock period (pin 4).

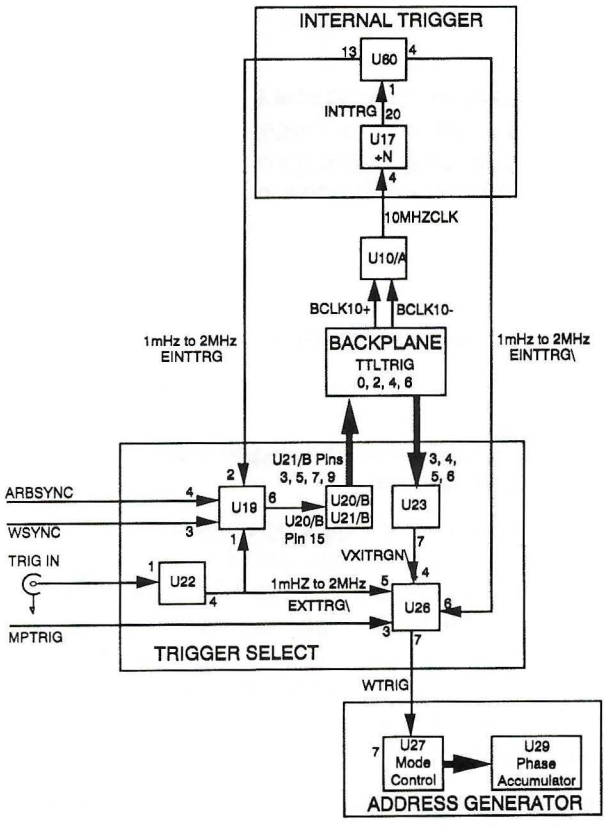


Figure 1-6. Instrument Triggering

Loading of data into this counter is coordinated by the signals at pins 1, 2 and 3 (DATACLK\, DNCENBL and BLD1). With each low-to-high transition of the data clock, one bit of data from BLD1 is serially loaded into a shift register until all bits have been entered. When DNCENBL is high, the data held by the shift register is transferred to a latch, then into the counter when pin 5 is low during the positive transition of pin 4.

U60 increases the pulse width of the signal at U17 pin 20, and also produces differential trigger signals at U60 pins 4 and 13 for use by the trigger select circuit. While not specified, typical pulse widths found at U60 pins 4 and 13 are approximately 250 ns.

1.3.3.2 Trigger Select Circuit

The trigger select circuit is shown on sheet 4 of the VXI Arb schematic. CR6 and CR7 limit the signal voltage from the EXT TRIG IN (J1) connector to slightly above +5V and slightly below 0V before reaching U22. R16 and R18 provide a reference of 1.46V to comparator U22 at pin 2. The TTL level output at pin 4 is in phase with the signal at pin 1 as it swings above and below 1.46V.

Backplane lines TTLTRG[7:0] allow any instrument in the VXIbus chassis to send or receive signals. This feature allows two or more Arbs to be triggered by the same signal. The operator must keep track of how each line is being used. The lines are open collector, active low, and limited by the VXIbus backplane to a maximum frequency of 12.5 MHz. The Arb can place a trigger signal on any one of the four even number TTLTRG lines (from U21/B). It can also receive one even number TTLTRG line through U23. The VXI Arb schematic shows the TTLTRG transmitting lines in coordinate C1, and receiving lines in coordinate B7.

Transmission to the TTLTRIG* lines is controlled by U19, U20/B and U21/B. Depending on the logic level of TTLOUT4 and TTLOUT5, U19 selects ARBSYNC, WSYNC, EINTTRG or EXTTRG for possible transmission on the TTLTRIG* lines. DIS0 and DIS1 determine which one of the four even number TTLTRIG* lines is selected by U20/B. U21/B either allows the selected signal to pass through it, or prevents the signal from reaching the TTLTRIG* lines.

U23 selects pairs of signals from the TTLTRIG* lines. Both odd and even lines are selected, or deselected simultaneously, and they must be done as pairs (1A and 2A, 1B and 2B, 1C and 2C or 1D and 2D). The TTLTRIG* line signal selected is seen at 1Y. TTLIN0 must be low to enable the outputs of U23. TTLIN1 and TTLIN2 select the signal pairs at 1Y and 2Y.

U26 selects one of four trigger inputs as the trigger source for WTRIG. The trigger inputs are EINTTRG\ (internal trigger), EXTTRG\ (external trigger), VXITRGN\ (backplane trigger) and MPTRIG\ (a microprocessor trigger decoded from the *TRG command and the Trigger Word Serial command). TRIGSRC0 and TRIGSRC1 determine which source is selected. Because U26 pin 1 is connected to ground, the selected source is always seen at WTRIG.

1.3.4 Instrument Clocking

Figure 1-7 shows the entire clock circuitry. There must be a clock present at WCLK for the Arb to operate. The three sources that are available for clocking the Arb are, internal (INTCLK), external (EXTCLK) and a signal from another instrument through the backplane (VXICLK). Internal or external clocking may be selected directly by U24, or passed through the backplane for use by the Arb and other instruments.

The internal clock originates from a phase locked loop (PLL) producing an output frequency of between 10 and 20 MHz. The PLL is referenced by differential ECL level 10 MHz signals (BCLK10- and BCLK10+) from the backplane, and translated to a TTL level signal (10MHZCLK). Counter U16 divides the PLL output frequency to a frequency of between 1mHz and 20 MHz. The external clock originates from the front panel CLOCK IN connector. U22 conditions the signal before passing it on to U18 and U24.

U18 chooses either the internal or the external clock to be placed on the backplane. U20/A and U21/A select and enable one of the four backplane lines. Selection of the backplane line used to clock the instrument is made by U23. U24 selects from the internal, external and backplane sources to clock the address generator through WCLK.

1.3.4.1 Internal Clock Source

The VXI Arb schematic, sheet 3, shows the phase locked loop and internal counter circuits.

Phase Locked Loop

When the internal clock is selected, CLKSRC1 is pulled low to enable the output of the ECL to TTL converter U15/D, and therefore the phase locked loop (PLL) consisting of ICs U11 through U15/D (and related components). Figure 1-8 is a simplified diagram of the PLL circuit. The 10 MHz differential signals BCLK10- and BCLK10+ originating from the VXIbus commander are converted to a single TTL level signal (10MHZCLK) by U10/A. This signal provides the PLL reference frequency at U11 pin 1.

When locked, the VCO output signal at U13 pin 3 has a frequency of from 10 to 20 MHz. This signal is halved by U14/B, entering U11 pin 8 at between 5 and 10 MHz. The signals at U11 pins 1 and 8 are each divided by separate counters located within U11, producing two signals, each with a frequency of 1kHz. These signals are phase detected and output at U11 pin 5. The phase detected signal consists of positive (VCO signal lags behind the reference signal) or negative (VCO signal leads the reference signal) pulses (or a high impedance state during phase coincidence or when the phase lock mode is disabled) that are smoothed by low pass filter U12/A and U12/B. There is a maximum swing of approximately 4V (+2.5V to +6.5V) from U12/B acting upon the varactor diode in its resonant circuit (across the input of VCO U13). All VCO output frequency changes are directly proportional to VCO input voltage level changes.

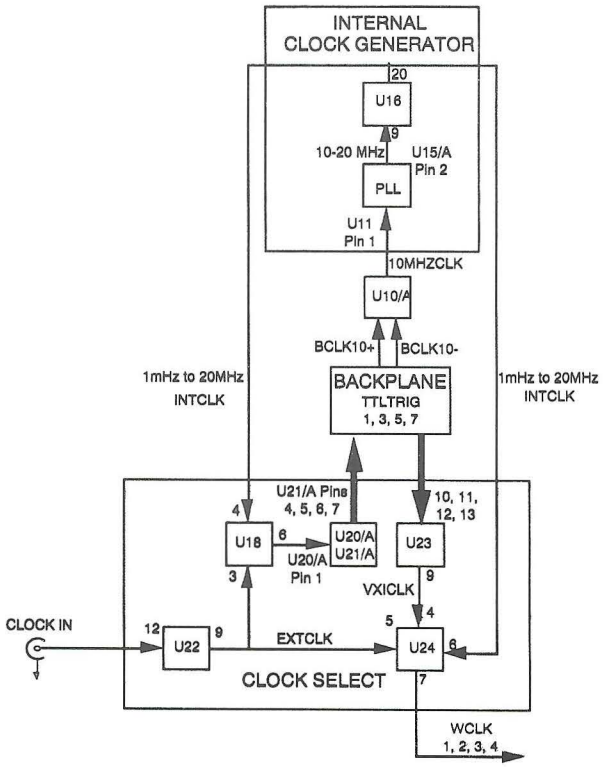


Figure 1-7. Instrument Clocking

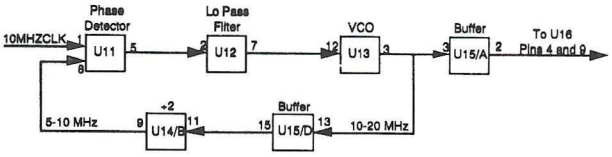


Figure 1-8. Phase Locked Loop

The phase lock loop is inhibited when the CLKSRC1 signal is brought high. This sets the ECL to TTL converter, U15/A and U15/D, to the high impedance

state, effectively opening both the phase locked loop and the input to the internal clock divider, U16.

Loading of data into the U11 PLL frequency synthesizer is handled by DATACLK\, BLD0 and PLLENBL. As shown in Figure 1-9, U11 contains two sets of shift registers, latches and counters. One set divides the 10 MHz reference signal, the other divides the VCO output signal. With each low-to-high transition of DATACLK\ (U11 pin 9), one bit of data from BLD0 (pin 10) is serially loaded into both shift registers until 14 bits have been entered. The 15th and last data bit is a control bit that resides at one input of gates A and B. This bit determines whether latch A (logic high) or latch B (logic low) is selected. When PLLENBL (pin 11) is high, and depending on the last data bit from BLD0, data is transferred from either shift register A to latch A, or shift register B to latch B. Data transferred to either latch is immediately presented to the associated counter. This process is repeated until both latches and counters have been loaded.

Internal Counter

DNC2016 counter U16 provides the internal clock (INTCLK) signal. It divides the PLL output signal at pin 4 by a whole number as large as 2^{36}. The output period at pin 20 is equal to 100 ns multiplied by the programmed value (the number that when multiplied by 100 ns equals the clock period required to clock the phase accumulator). For example, if the programmed value is 11, the output period is 11 x 100 ns, or 1.1 μs. This output (pin 20) is a TTL high with a low pulse equal in width to one clock period (pin 4).

Loading data into this counter is coordinated by the signals at pins 1 through 3. With each low-to-high transition of pin 1, one bit of data at pin 3 is serially loaded into a shift register until all bits have been entered. When pin 2 is high, the data held by the shift register is transferred to a latch, then to the counter when pin 5 is low during a positive transition on pin 4.

1.3.4.2 Clock Select Circuit

The clock select circuit is shown on sheet 4 of the VXI Arb schematic. CR8 and CR9 limit the signal voltage from the EXT CLK IN (J2) connector to slightly above +5V and slightly below 0V before reaching U22. R16 and R18 provide a reference of 1.46V to comparator U22 at pin 11. The TTL level output at pin 9 is in phase with the voltage at pin 12 as it swings above and below 1.46V.

Using the TTLTRG* lines, two or more Arbs can be clocked by the same signal. The operator must keep track of how each line is being used. The lines are open collector, active low, and limited by the VXIbus backplane to a maximum frequency of 12.5 MHz. The VXI Arb can place a clock signal on any one of the four odd number TTLTRIG* lines (from U21/A). It can also receive one odd number TTLTRIG* line through U23. The VXI Arb schematic shows the TTLTRIG* transmitting lines in coordinate D1, and receiving lines in coordinate A7.

Transmission to the backplane is controlled by U18, U20/A and U21/A. Depending on the logic level of TTLOUT0, U18 selects either INTCLK (TTLOUT0 low) or EXTCLK (TTLOUT0 high) for possible transmission on the TTLTRIG* lines. TTLOUT2 and TTLOUT3 determine which one of the four odd number TTLTRIG* output lines is selected by U20/A. U21/A either allows the selected signal to pass through it, or prevents the signal from reaching the TTLTRIG* line at the backplane.

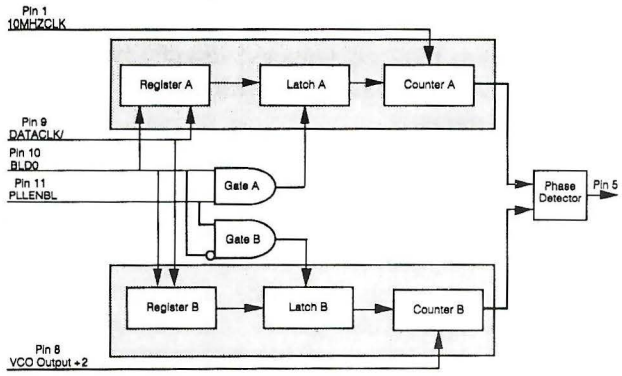


Figure 1-9. Phase Detector (U11)

U23 selects pairs of clock signals from the backplane. Both odd and even lines are selected, or deselected simultaneously, and they must be done as pairs (1A and 2A, 1B and 2B, 1C and 2C or 1D and 2D). The clock signal selected is seen at 2Y. TTLIN0 must be low to enable the outputs of U23. TTLIN1 and TTLIN2 select the signal pairs at 1Y and 2Y.

U24 selects one of three clock inputs as the clock source for U25. The clock inputs are INTCLK (internal clock); EXTCLK (external clock); and VXICLK (VXI clock). CLKSRC0 and CLKSRC1 determine which source is selected. Because U24 pin 1 is connected to ground, the selected source is always seen at U25 pin 1.

Tapped delay line DL1 (and a jumper, replacing switch SW1) allows a signal delay of 6ns at WCLK4 compared to the signals at WCLK1, WCLK2 and WCLK3. This allows data from the RAM module to settle before being transferred to the waveform DAC.

1.3.5 Address Generator and Mode Control Logic

The description of the circuitry on sheet 5 of the VXI Arb schematic is divided into phase accumulation (paragraph 1.3.6.1), followed by a detailed explana-

tion of each mode. Since each division is built on an understanding of previous material, paragraphs 1.1.6 through 1.1.7 must be read in the order given.

1.3.5.1 Model 1375 Phase Accumulation

This circuit directs address lines WA[16:0] to sequentially select locations in Random Access Memory (RAM module, shown on sheet 6 of the VXI Arb schematic) for conversion to an analog voltage by the Digital to Analog Convertor (schematic, sheet 8).

Refer to the RAM diagram, figure 1-10. For standard instruments without option 01, there are four 8k blocks of memory (horizontal dimension), totalling 32768 (32k) locations in RAM. Instruments with option 01 contain sixteen 8k blocks of memory. Address lines WA[16:13] (see schematic, sheet 6) are buffered by U33 to become BRA[16:13], then decoded by the RAM module to select one of these sixteen 8k blocks. For instruments without option 01, the RAM module ignores lines BRA[16:15], leaving lines BRA[14:13] to select one of four 8k blocks. Address lines WA[12:0], are buffered by U33, U34 and U35, becoming BRA[12:0]. These 13 bits select one of 8192 locations (points) within each block.

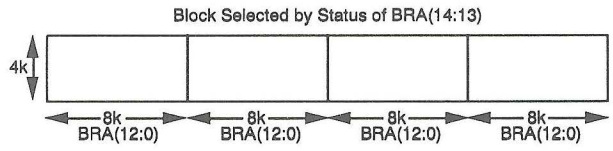


Figure 1-10. RAM Diagram

Mode control IC, U27 (sheet 5), directs the operation of the remaining four IC's shown on this sheet. Counter U30 keeps track of the sequence count in triggered sequence mode, and monitors the burst count in burst mode. U28 controls block sequencing. U31 enables the four address lines from U28 during triggered sequence mode, or the four upper order address lines from U29 while in all but triggered sequence mode.

Control lines MODE0, MODE1 and MODE2 place the instrument in one of the six operator selectable modes, or null mode. The instrument is first placed in null mode each time a different waveform or mode is selected. For example, if the instrument mode is changed from continuous to triggered, it does so by way of null mode. Table 1-1 shows the mode truth table.

Mode Selected	MODE0	MODE1	MODE2
Null	0	0	0
Continuous	1	0	0
Triggered	0	1	0
Sync Gate	1	1	0
Async Gate	0	0	1
Burst	1	0	1
Triggered Seq.	0	1	1
Null	1	1	1

Table 1-1. Mode Truth Table

Trace Modes

The terms 'value' and 'address' are used somewhat interchangeably in this discussion because the instantaneous output 'value' of the phase accumulator (U29 WA[16:0]) used to 'address' the RAM module is derived from several math operations.

During trace playback, the phase accumulator (U29) drives the RAM module address lines, placing a value on lines WD[15:0]. With each clock cycle, the phase accumulator value increases by the phase increment value (the horizontal spacing between trace points shown in Figure 1-10).

Figure 1-11 shows both the internal (fraction) and external (integer) bits of the 48 bit phase accumulator. Only the external bits drive the RAM module, while the internal bits keep track of accumulated values less than one. If the phase increment value is less than one, it may take many clock cycles to achieve an integer (address) change, directing the RAM module to output a new value. Conversely, if the phase increment is much greater than one, many trace address locations are skipped with each clock cycle.

When in raster trace mode, the phase increment value is one, and each point in the trace is addressed sequentially, one per clock cycle. This is the least significant bit of the address applied to the RAM, and is really a phase increment of the value 2^{30}. Instrument frequency at ARB OUT is determined by the equation:

$F_O = F_R / P$

Where: F_O = ARB OUT Frequency

F_R = Raster Frequency

P = Number of trace points

The default raster frequency (WCLK1) is 20 MHz, and the power-up trace in RAM has 2048 points. Therefore, the power-up ARB OUT frequency in raster trace mode is:

F_o = 20,000,000 / 2048

= 9.765625 kHz

The raster (clock) frequency and the number of trace points are both operator selectable and directly affect the trace cycle time. Raster trace mode is used with irregular traces, such as a heartbeat, which has multiple combinations of steep and shallow amplitude changes. In raster mode, each memory location in a trace is addressed sequentially, and each location is held for one clock period. Because each point is addressed, no location (and therefore, no trace information) is skipped.

In continuous wave (cw) trace mode, the phase increment value is determined by the Arb, and may be much less than one to much greater than one. As explained above, the 30 lowest order address bits are internal to U29 and cannot be seen. These bits represent fractions of numbers, allowing generation of output frequencies as low as 100 mHz, with as few as 8 waveform points. The 18 highest order address bits represent integers, and are output from U29 as RA[17:0]. The highest order bit, RA17, is not used and therefore not shown in the figure.

To see how internal phase accumulation of fractional bits affect the integer bits, suppose for example, that the phase accumulator has a value of 0, and that a value of 1.25 is added with each clock cycle. At the first clock, integer 1 (RA0) and internal bit 0.25 are asserted. At the second clock, integer 2 (RA1) (1 + 1) and internal bit 0.5 (.25 + .25) are asserted. With the third clock, integers 1 (RA0) and 2 (RA1), as well as internal bits 0.25 and 0.5 are all asserted (representing a value of 1.25 X 3 = 3.75). When the fourth clock cycles, integer 4 (RA2) is asserted, and the internal bits carry over to also assert integer 1 (RA0).

When the trace size in RAM and frequency of the output signal are relatively small values, each trace point is addressed more than once. The fractional increment value, accumulated by the internal bits, is determined from the following equation:

$$INC = (F_o X P) / CLK$$

Where: INC = Increment Value

F_o = ARB OUT Frequency

P = Number of trace points

CLK = Clock Frequency

At power-up, the ARB OUT frequency is 1kHz, the RAM is holding a 2048 point trace, and the clock frequency is 20 MHz. The increment value is:

INC = (1000 X 2048) / 20,000,000

= .1024

Therefore, it takes an average of approximately 9.8 clock cycles (1/.1024) before integer bits are changed. This trace mode is acceptable for regular, repeatable waveforms such as sine or triangle waves which can be reconstructed by filtering.

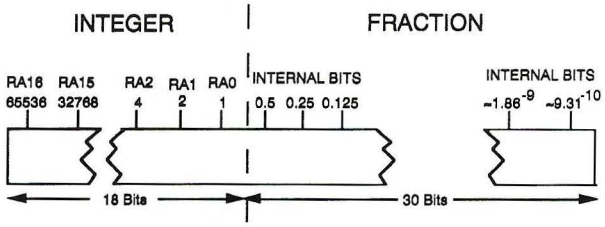


Figure 1-11. 48 Bit Phase Accumulator

To understand phase accumulator operation when the increment value is much greater than one, suppose that an 8 k (8192 point) trace occupying all of the second 8 k block of RAM (from address location 8192 to 16383) has just been selected for playback. First, the Arb loads the start address (8192) into the phase accumulator (U29), the contents of which are always presented to the output (RA[16:0]). The RAM module, monitoring the phase accumulator, immediately outputs the value at address 8192. Next, an increment value (randomly selected to be 5 for this example) equal to the spacing between trace points (the horizontal dimension shown in figure 1-11) is added to the start address with each WCLK1 cycle. The RAM module continues to monitor the phase accumulator, sequentially outputting the values at the identified addresses. Increment summing continues until the accumulated value reaches the stop address (16383). The address locations identified by the phase accumulator to be output by the RAM module for this example are 8192, 8197, 8202, 8207, ... 16382. The stop address (16383) is not identified because the difference between it and the last identified address (16382) is less than 5. When the last address is identified, a 'wrap-around' value equal to the RAM addresses that are not part of the trace being played back, plus the increment value (5), is added to the sum held by U29. In effect, this 'wraps around' the remaining RAM addresses, leaving the phase accumulator output at or near the start address. The beginning address of the second cycle is determined by the equation:

BA = LA + RA + INC - RAM

Where: BA = Beginning address of the new cycle

LA = Last address identified from the previous cycle.

RA = RAM addresses not part of the trace being played back.

INC = Increment value

RAM = Total number of address locations in the RAM module.

In this example, the last address identified is 16382, the remaining RAM addresses are the first, third and fourth 8k blocks of memory (24576 address points), the increment value is 5, and the total number of address locations in the RAM board is 32768. Therefore, the beginning address of the second cycle is:

$$BA = 16382 + 24576 + 5 - 32768$$

$$= 8195$$

The sequential output values from U29 for the second cycle of the example trace would be 8195, 8200, 8205, 8210, ...16380. The wrap-around value (24576 + 5 = 24581) and the last address identified (16380) are again entered into the above equation to arrive at the new beginning address of 8193. This process is repeated for each cycle.

The number that actually causes the wrap-around value to be added to the accumulated value is called the 'magnitude compare' value. This value takes into account the six clock cycles needed to begin a new waveform cycle. The magnitude compare value is calculated from the equation:

$$MAG = SIZE - (6 \times INC) + START$$

Where: MAG = Magnitude Compare value

SIZE = Trace size in points

INC = Increment value

START = Address of the first point

For this example, the trace size and start address are both 8192, and the increment is 5. The magnitude compare value is therefore:

$$MAG = 8192 - (6 \times 5) + 8192$$

$$= 16354$$

For cw trace mode, the increment value is not usually a whole number, as in the previous example. The equation for determining the frequency at the ARB OUT connector in cw mode is:

$$F_o = INC (CLK / P)$$

Where: F_o = ARB OUT Frequency

INC = Increment Value

CLK = Clock Frequency

P = Number of trace points

In the example, the increment value is 5, the clock frequency in cw trace mode is fixed at 20 MHz, and the number of trace points is 8192. Therefore, for the ARB to generate an increment value of 5, the programmed ARB OUT frequency would have been:

$$F_o = 5 (20{,}000{,}000 / 8192)$$

$$\approx 12.207 \text{ kHz}$$

This is not a realistic value. If the frequency had been programmed to 12.2 kHz, the increment would have been:

$$INC = F_o (P / CLK)$$

$$= 12200 (8192 / 20000000)$$

$$= 4.99712$$

As previously explained, fractions of increment values are maintained within the 48 bit phase accumulator (U29), with only the 18 highest order bits seen at the output.

1.3.5.2 Continuous Mode

When continuous mode is selected, all mode controller outputs (U27 on sheet 5 of the VXI Arb schematic) are inactive except IM0, IM1, IMC and PACLR. Both BLCKCLR\ and STEP/DIR are driven high, directing U31 to only accept information from the 'B' input lines (1B, 2B, 3B, 4B).

The mode controller directs the phase accumulator (U29) to sequentially cycle through trace addresses as previously described in paragraph 1.3.6.1. To accomplish this task, U29 requires four numbers to be entered into it; 1) the wrap-around value; 2) the magnitude compare value; 3) the start location of the selected waveform (start address), and; 4) the step size (increment) between each point of the waveform. Each number is entered into a separate register. Address lines BLA[6:1] select the location of data placement, while data lines BLD[7:0] write data to the selected register when PASTB\ goes low. Use of data placed into these registers is controlled by IM0, IM1 and IMC. The magnitude compare value compensates for the six clock cycle delay within the mode controller/phase accumulator loop. Continuous summing of data is handled by the phase accumulator located within U29.

After the phase accumulator feedback register is cleared by U27 asserting PACLR high, the mode controller directs U29 to load the start address from the start register into the phase accumulator by forcing IMC and IM0 low, and IM1 high. The mode controller then reverses control lines IM0 and IM1, so that with each clock pulse at WCLK1, U29 continuously adds the increment to the value being held in the phase accumulator. Due to the pipeline within U29, each value held in the phase accumulator is delayed by four WCLK1 clock pulses before appearing on the output lines, RA0 through RA16. Sum-

ming continues until the accumulated value reaches the magnitude compare value, asserting WMCO high six clock pulses prior to the end of the trace. The wrap-around value, as described in paragraph 1.1.6.1, is then added to the value in the phase accumulator. Repetitive summing of the increment is again initiated. This sequence is repeated until a mode change occurs.

If a different waveform is selected, the instrument is placed in null mode (see paragraph 1.1.6.8). IMC, IM0, IM1 and PACLR are asserted high, and new values are entered into the start, wrap-around, increment, and magnitude compare registers. The instrument then returns to continuous mode.

1.3.5.3 Triggered Mode

The triggered mode is identical to the continuous mode, except that when the mode is first entered, and at the end of each trace cycle, the mode controller directs the phase accumulator to output the start address, then wait for WTRIG to be asserted before beginning to accumulate the increment value. In this way, only one cycle of the waveform is generated with each WTRIG cycle.

1.3.5.4 Synchronous Gate Mode

When in synchronous gate mode, the start address is loaded into the phase accumulator, then waits, as in triggered mode, for WTRIG to be asserted high before beginning increment accumulation. While WTRIG remains high, the trace is continuously cycled (as in continuous mode). When WTRIG goes low, the cycle is completed and the mode controller (U27) directs the phase accumulator to output the start address. Increment accumulation is not initiated until WTRIG returns high.

1.3.5.5 Asynchronous Gate Mode

Asynchronous gate mode is identical to synchronous gate mode except that when WTRIG goes low, the trace cycle is immediately terminated without completing the last cycle, and the start address is loaded into the phase accumulator.

1.3.5.6 Burst Mode

When burst mode is selected, the instrument is placed in null mode (paragraph 1.1.6.8) until the burst count is loaded into U30. One bit of data at U30 pin 3 is loaded into a shift register with each clock pulse at pin 1, then transferred to a latch when pin 2 goes high. Mode control lines, MODE0, MODE1 and MODE2, then enable the burst mode. As in continuous mode, PACLR pulses high, clearing the accumulator in U29, then IMC and IM0 are pulled low, and IM1 is brought high to load the start address of the selected trace into the phase accumulator. CNTLOAD\ goes low, transferring the burst count data held by the latch in U30 into the counter. At this point, all operations cease until WTRIG is asserted high.

When a trigger (WTRIG) is received by U27, IM1 is brought low, IM0 is pulled high, and U29 begins increment accumulation as explained in paragraph 1.1.6.1. At the end of each trace cycle, WMCO pulses high, causing the mode controller to also pulse INC high. With each pulse of INC, the count held by U30 decrements by one until 0 is reached, causing U30 to pulse CNTDONE\ low. U27 now directs U29 to output the start address, then cease operations until WTRIG is again asserted. When WTRIG goes high, the events described in this paragraph after the statement "(WTRIG) is received by U27" are repeated.

1.3.5.7 Triggered Sequence Mode

When triggered sequence mode is selected, the instrument is placed in null mode (paragraph 1.1.6.8) until the triggered sequence count is serially loaded into U30. One bit of data at U30 pin 3 is loaded into a shift register with each clock pulse at pin 1, then transfered to a latch when pin 2 goes high. Mode control lines, MODE0, MODE1 and MODE2, now enable the triggered sequence mode, causing the mode controller (U27) to assert nearly all of its output lines.

The mode controller begins by pulsing PACLR high to clear the accumulator in U29. It then pulls IMC and IM1 low, and IM0 high to load the start address of the first 8k block into the phase accumulator. BLCKCLR\ pulses low to clear the block counter (U28), and STEP/DIR is asserted low, enabling the U31 'A' address lines from U28. Next, the mode controller pulses CNTLOAD\ low to copy the triggered sequence count data from the latch in U30 to the counter. Finally, U27 brings IM1 low and IM0 high. The phase accumulator, U29, begins increment accumulation of the first 8k block as explained in paragraph 1.1.6.1. The trace is repeatedly scanned, as in continuous mode.

U31 selects either the 4 bits from U28, or the 4 most significant bits from U29, and places them on lines WA[16:13]. In triggered sequence or burst modes, STEP/DIR is low, and U31 selects the 4 'A' inputs from U28. In all other modes, STEP/DIR is high, and U31 selects the 4 'B' inputs from U29. In either condition, U31 is transparent to the selected set of input lines.

The trace memory is divided into four 8k blocks (sixteen 8k blocks with option 01). U28 and U31 select the block to be scanned. Each time WTRIG is enabled high, INC is pulsed high, changing the

selected block, and decrementing the count in U30. When INC is pulsed high, the output of U28 (Q0 through Q3) is incremented by one, and the next 8k block is selected by the U31 output lines. When a new block is selected, the trace is not completed, but immediately terminated. Phase accumulation of the new trace is begun at the current address, plus one increment. In addition, pulsing INC high also decrements by one the count held by U30 until it reaches 0 (all blocks sequenced), causing U30 to pulse CNTDONE\ low. This causes BLCKCLR\ to be pulsed low, clearing the block counter (U28) and initiating increment accumulation of the first 8k block. CNTLOAD\ is also pulsed low, again copying the count data from the U30 latch to the counter.

1.3.5.8 Null Mode

Each time a different waveform or mode is chosen, the instrument is placed in null mode, allowing the mode controller (U27) to be reset. When null mode is first enabled, it selects the initial state, where there is no waveform generation. The mode controller then sets PACLR to clear the phase accumulator (U29), and prepares to cycle through the selected trace by loading the trace start, increment, and wrap around addresses into the phase accumulator. The mode controller then waits for a change in the mode inputs (MODE0, MODE1 and MODE2) before initiating further action.

1.3.6 Waveform Memory and Arbitration Logic

The waveform memory and arbitration logic circuit, which directs the flow of trace data into or out of the RAM MODULE, is shown on sheet 6 of the VXI Arb schematic. Interaction of this circuit with peripheral circuitry is shown in Figure 1-12. Three conditions exist for data flowing into or out of the RAM module. These are write (data loaded into RAM from the Interface board), read (data copied from RAM to the Interface board), and playback (data residing in RAM is addressed for playback to the waveform DAC). Control of trace data into or out of RAM is handled by RAM\, R/W, RAMWE\, and RAMOE\.

During a write operation, RAM\ is asserted, making U32/A pin 6 high, and blocking data from phase accumulator registers U33, U34 and U35. U32/A pins 1 and 5 are both low. Read/write address registers U36, U37, and U38 are enabled because pin 1 of each IC is connected to ground. With these registers enabled, address lines LA[17:1] select a location in RAM where trace data write or read activity will take place. The output pins (11 through 18) always match each corresponding input pin (2 through 9). R/W is high (write mode), directing trace data to flow from the interface board, through transceivers U56, U57, U58, and U59 to the RAM board. When all the address (BRA[16:0]) and data lines (WD[15:0]) are ready, RAMWE\ is strobed, loading the data into RAM. This process is repeated for each trace address being loaded.

RAM\ is also asserted during a read operation. As with write, address lines LA[17:1] select a location in RAM for trace data activity. This time, however, R/W is low (read mode), and trace data flows from the RAM board, through transceivers U56, U57, U58, and U59, to the interface board. When all the address lines (BRA[16:0]) have settled, RAMOE\ directs the RAM module to output trace data held in the addressed location onto data lines WD[15:0]. This process is repeated for each trace address being loaded.

The address generator and mode control logic circuitry (schematic sheet 5), through the address register (U33, U34 and U35), controls playback by the waveform DAC (U47) of trace data previously entered into RAM. When a trace is to be played back, U32/A pins 1 and 5 are both high, disabling U36, U37, U38, U56 and U57. U32/A pin 6 is low, allowing the phase accumulator output WA[16:0] to address the RAM MODULE through the phase accumulator register (U33, U34 and U35). Following the rising edge of WCLK2, all bits at the playback address register input pins (2 through 9) are transferred directly to the respective output pins (12 through 19). These address lines then control the waveform DAC (U47 on schematic sheet 8). The default 2048 point sine wave is automatically played back immediately following power-up, and when all operator entered traces are deleted.

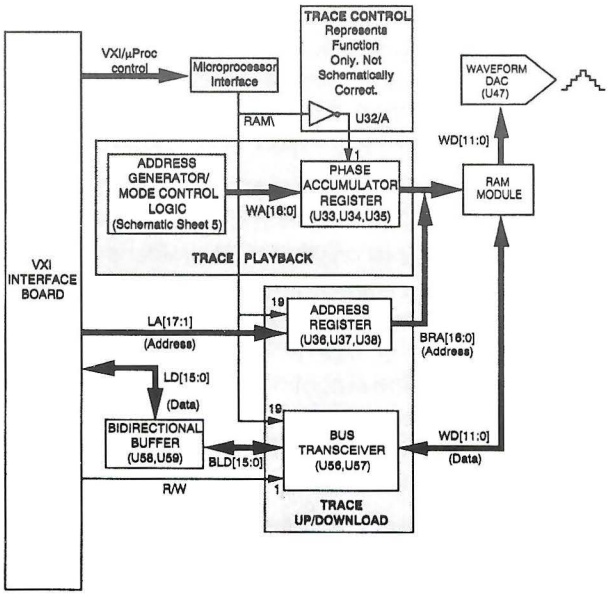


Figure 1-12. Trace Data Control

1.3.7 Amplitude/Offset Control

The Model 1375 provides fine, medium, and coarse amplitude control over a range of 1000:1 at the ARB OUT connector. Fine amplitude adjustment is accomplished by the amplitude/offset control circuit described in this paragraph. The pre-attenuator circuit (paragraph 1.3.10) provides a medium level of control, while course adjustment is made by the output attenuator (paragraph 1.3.11).

The sum of fine (DAC reference) and medium (pre-attenuator) amplitude changes provide continuous amplitude control over a 10:1 range. Medium control is provide by a pre-attenuator in 1/32 amplitude steps. Fine control adjusts amplitude levels between these steps.

The dual digital to analog converter (DAC) U41 shown on sheet 7 of the Model 1375 schematic, provides dc voltage levels that control both offset and fine amplitude setting of the ARB OUT signal. Parallel data from BLD[11:0] is latched on the rising edge of write strobe AMOFS\. This data is converted to an analog voltage by the amplitude DAC and output from U41 pin 24 when BLA15 (pin 18) is high, or converted by the offset DAC and output from pin 2 when BLA15 is low. Both DACs maintain their previous output voltages when not being addressed. U39 and U40/A provide a fixed +5.00V reference for U41. Amplifiers U42 and U44 provide buffering and sufficient gain to drive their respective outputs (+AMP-REF and OFFSET).

When the filter (schematic sheet 9) is connected, the ARB OUT signal is slightly attenuated. Therefore, amplitude compensation is required when the filter is disconnected. This is accomplish by inserting a 2kΩ resistor (R141) between U42/A pin 1 and U42/B pin 6 to limit the voltage at U42/B pin 7, thereby reducing the ARB OUT signal amplitude. R31 adjusts the ARB OUT amplitude when the filter is connected, R34 when the filter is disconnected.

The waveform DAC, U47 (schematic sheet 8), operates best when "REF-" is -1Vdc and an amplitude control voltage more positive than -1Vdc is applied through a current setting resistor. R36, R38 and U40/B combine to convert +5Vdc from U40/A pin 1 to a -1Vdc reference voltage which is applied to "REF-", pin 19, of U47. The output of U42/B is made to vary from approximately +5Vdc to -1Vdc. This puts approximately +6Vdc to 0Vdc across the series combination of R40 and R58 to the "REF+" input of U47.

1.3.8 Waveform DAC and Pre-Amp

Sheet 8 of the VXI Arb schematic contains both the waveform DAC and pre-amp circuitry.

Waveform DAC

At the rising edge of WCLK3, the high speed waveform DAC (U47) converts the binary value present at DB1 through DB12 (from WD0 through WD11) into two differential analog currents (OUT- and OUT+). DAC output gain (affecting output waveform amplitude) is set by the fixed voltage -AMP-REF and the variable voltage +AMP-REF, both from the Amplitude/Offset Control.

Two octal 'D' type flip/flops (U45 and U46) combine to create a 12 bit data bus to provide input for the waveform DAC (U47). With pin 1 held low, and following the rising edge of pin 11, all output pins are at the same state as their respective input pins.

Pre-Amp

The Pre-Amp circuit is connected as a differential amplifier, providing both voltage gain and buffering to the waveform DAC (U47) dual output currents (-DAC-OUT and +DAC-OUT). These outputs are converted to differential voltages by R41 and R42. C35 adjusts waveform quality while R48 sets the offset.

1.3.9 Filter-4 MHz Lo Pass and Pre-Attenuator

Filter-4 MHz Lo Pass

The 6-pole, 4MHz low pass filter shown on sheet 9 of the schematic is used to suppress the high frequency harmonics generated by the synthesizing method of waveform generation. These harmonics are related to the broadband noise components of the waveform clock, the repetitive duplication of the waveform addresses in waveform memory, any inherent nonlinearity in the waveform DAC, and aliasing. Because of this, the filter also smooths out the voltage steps between each trace point, making the jumps more gradual. This is especially true in cw mode or at high raster frequencies. When filtering is selected, relay K1 connects the Pre-Amp output to the 4 MHz filter, providing a minimum harmonic attenuation of 34 dB at 16 MHz.

Pre-Attenuator

The Model 1375 provides fine, medium, and coarse amplitude control over a range of 1000:1 at the ARB OUT connector. Fine amplitude adjustment is accomplished by the amplitude/offset control circuit (paragraph 1.3.8). The pre-attenuator circuit described in this paragraph provides a medium level of control, while course adjustment is made by the output attenuator (paragraph 1.3.11).

The sum of fine (DAC reference) and medium (pre-attenuator) amplitude changes provide continuous amplitude control over a 10:1 range. Medium control

in 1/32 amplitude steps is provide by the pre-attenuator, a 5-bit R-2R ladder network. Fine control adjusts amplitude levels between these steps.

Refer to the VXI Arb schematic, sheet 9. The voltage signal at FILTOUT (K1 pin 4) is converted to current as it passes through the resistor ladder network (R67 to R76 and R78) to the output amplifier summing junction (PASUM). The status of relays K2 through K6, controlled by digital lines PRE1\ through PRE5\, determines how this current is split between the summing junction and ground. These relays switch in or out portions of the resistor network, permitting the selection of any integer multiple of 1 through 32 increments of current. Relay K2 has a value of 1/32, K3 a value of 1/16, K4 a value of 1/8, K5 a value of 1/4, and K6 a value of 1/2.

1.3.10 Power Amplifier and Output Attenuator

Power Amplifier

The power amplifier, U52 (Model 1375 schematic, sheet 10) sums the input currents from the pre-attenuator and offset control circuit, and drives the output attenuator. Offset is adjusted by R55. Regulator modules VR2 through VR5 convert ±24V to the required ±15V. Current limiting is provided by VR2 and VR4, while VR3 and VR5 regulate the ±15V output voltage levels.

Output Attenuator

The Model 1375 provides fine, medium, and coarse amplitude control over a range of 1000:1 at the ARB OUT connector. The sum of fine and medium amplitude changes provide continuous amplitude control over a 10:1 range. Fine amplitude adjustment is accomplished by the amplitude/offset control circuit (paragraph 1.3.8). The pre-attenuator circuit described in paragraph 1.3.10 provides a medium level of control, while course adjustment is made through two decades of attenuation by the output attenuator described in this paragraph.

The output attenuator schematic located on sheet 10 is composed of relays K8 and K9, and their respective resistors. In addition, K10 enables or disables the Arb signal at the output connector. Control for the output attenuator is provided by -20DB\, -40DB\ and OUTPTON\ digital control lines.

When an output voltage greater than 0.501Vp is programmed, neither relay (K8 or K9) is energized, allowing the signal to pass with no attenuation. For output voltages greater than 0.0501 Vp, but not greater than 0.500 Vp, K8 is energized, attenuating the signal by 20 dB. Both K8 and K9 are energized for signals of 0.0500 Vp or less, attenuating the signal by a total of 40 dB.

1.3.11 Marker Output Conditioning and Buffers

In addition to the waveform signal at ARB OUT, the Model 1375 produces either a zero crossing sync or a set of beginning bit pulses at MARKER SYNC, and marker pulses at MARKER POSITION. The circuits that create these signals are located on sheet 11 of the XVI Arb schematic.

When zero crossing sync mode is selected, FILTOUT (the arbitrary waveform) is modified by the zero crossing detector (part of U51) to produce TTL level pulses at U61 pin 7, where the pulse width is equal to any portion of the FILTOUT waveform above 0V. U51 pin 1 is set for 0V, so that the output of the comparator (within U51) is TTL low when the signal at pin 2 becomes greater than 0V, TTL high when the signal at pin 2 becomes less than 0V. The zero crossing sync mode is selected by a high at WSYNC-SEL, enabling the NAND gate to invert (OUT1) the comparator output. This signal is also seen at U51 pin 8. With zero crossing selected, WVFMSYNC is TTL low, and the second NAND gate (OUT2) is inverted from the first NAND gate (OUT1). The signal is again inverted by Q4, then buffered by U61, enabling the signal to drive a 50Ω termination. The buffered signal is seen at J4 if K7 is enabled by SYNCOUT\.

When beginning bits sync mode is selected, a low at WSYNCSEL blocks the FILTOUT signal and forces U51 pins 4 and 8 high. The beginning bits are placed on the WVFMSYNC line, which goes low with each bit. The signals at U51 pins 9 and 12 are in phase, then inverted by Q4, and buffered by U61, enabling the signal to drive a 50Ω termination. The buffered signal is seen at J4 if K7 is enabled by SYNCOUT\.

The Marker Position output is an active high, TTL level pulse produced for each point that has been identified by the user as a marker. This pulse originates from ARBSYNC and is buffered by U61, making it capable of driving a 50Ω termination. The buffered signal is seen at J3 if K7 is enabled by SYNCOUT\.

Data lines WVFMSYNC and ARBSYNC originate from the RAM MODULE trace data bus WD[15:0]. This 16 bit wide bus provides data to the 12 bit wide waveform DAC (U47). Two of the four unused bits, WD[13:12] are sent through U46 (sheet 8) twice to make up for one clock delay within the waveform DAC (U47). This insures that the timing of bit placement at both marker BNCs match the results from the waveform DAC at the ARB OUT connector.

1.3.12 Diagnostic Interface

Sheet 12 of the VXI Arb schematic shows the diagnostic interface circuitry. When the operator initiates an instrument self-test (*TST?), the VXI interface board programs specific parameters to the Model 1375 Arb, producing expected signals at various test points within the instrument. These test points are connected to the signal input pins of U53 where they are selected by DIS0, DIS1 and DIS2 to pin 8. U54/A and U54/B buffers the selected signal before reaching analog to digital converter U55.

The CONVERT and DDSTRB\ lines control conversion of the analog signal (U55 pin 14) to binary data (pins 1 through 10). The positive transition of CONVERT resets U55. During this transition, DDSTRB\ holds pins 19 and 20 high, placing the output pins (1 through 10) in a high impedance state. The conversion cycle is initiated by the falling edge of CONVERT. When this cycle is complete, pins 19 and 20 are brought low, enabling the loading of output pins 1 through 10. This binary data is then read by the VXI interface board and compared against a corresponding range of expected data. If there is an out of range condition, the operator is notified via the *TST? query message.

SECTION 2
CALIBRATION

2.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize the turnaround time.

2.2 REQUIRED TEST EQUIPMENT

The test equipment required to perform the calibration procedure is listed in Table 2-1.

Table 2-1. List of Test Equipment

Equipment	Quantity	Specifications
VXI Requirements	1	VXI chassis
	1	VXI slot-0 controller
	1	VXI "C" size extender board (Optional-see text)
DMM	1	HP 3478A or equivalent
Oscilloscope	1	Tektronix 2465 or equivalent
Adaptor	1	BNC female to double banana jacks
Cable assembly	1	Dual mini-clip/coax
Coaxial cable	1	BNC male connectors, RG58U cable
Probe	2	10MΩ
50Ω Termination	1	Feedthrough, 0.1% accuracy, 2W

2.3 CALIBRATION

WARNING

With the covers removed, potentially dangerous voltage points may be exposed. Do not be misslead by the term "low voltage". Contact with potentials as low as 40 volts could cause serious injury or even death.

Power-down and remove the Arb module from the VXI chassis. Remove the side panel without the address switch cutout. Allow access to the component side of the Arb module during calibration by mounting the module on an extender card, or by installing it into the rightmost slot of the VXI chassis. Allow at least a 30 minute warm-up. Figure 2-1 shows test point and adjustment locations.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Appendix A of this Manual.

2.3.1 Offset Calibration

1. Connect test point PTP1 of the Arb to the DMM inputs (TP13 common) with the dual clip/coax cable assembly. Set the DMM mode to VDC.
2. Send the following commands to the Arb;

```
*rst;:trac:del:all
:trac:def wave,100
:trac:data wave,dc
:trac:sel wave
:volt 5;:freq 1;:outp 1
```

3. Adjust R48 for 0V ±0.5 mV offset.
4. Connect ARB OUT to the DMM through the 50Ω terminator.
5. Adjust R55 for 0V ±1mV offset.
6. Turn on the output filter by sending the command;

```
:outp:filt 1
```

7. Adjust R52 for 0V ±1mV

2.3.2 DC Gain Calibration

1. Connect ARB OUT to the DMM through the 50Ω terminator.
2. Turn off the output filter and reduce the amplitude to 1V by sending;

```
:outp:filt 0;:volt 1
```

3. Change the offset to +4.0V by sending the command;

```
:volt:offs 4
```

4. Adjust R27 for +4V ±1mV.
5. Change the offset to -4.0V by sending;

```
:volt:offs -4
```

6. Adjust R27 to reduce the error at -4.0V by half. This will interact with the offset reading at +4.0V. Note the error at -4.0V.
7. Repeat step 3 and note the error at +4.0V. The offset errors at +4.0V and at -4.0V should be equal and minimum. If necessary, readjust R27 slightly to reduce the error at +4.0V and repeat steps 5 through 7.

2.3.3 AC Gain Calibration

1. Connect the ARB OUT to the DMM through the 50Ω terminator.
2. Set up the ARB with the following commands;

```
*rst;:trac:del:all
:trac:def wave,8192
:trac:data wave,square
:trac:sel wave
:trac:lim wave,2000,2010
:outp 1;:volt 2.5
```

3. Set the DMM mode to VDC.
4. Adjust R34 for +2.5V ±1mV.
5. Turn on the output filter by sending;

```
:outp:filt 1
```

6. Adjust R31 for +2.5V ±1mV.

2.3.4 Waveform Quality

1. Connect the ARB OUT to the scope through the 50Ω termination.
2. Set up the Arb with the following commands;

```
*rst;:trac:del:all
:trac:def wave,1024
:trac:data wave,square
:trac:sel wave
:volt 0.501;:freq 1E6;:outp 1
```

3. Adjust C35 for peak-to-peak aberrations (overshoot plus ringing) of <5% +30 mV of the peak-to-peak waveform amplitude while maintaining a rise/fall time of <30 ns.
4. Send the following command;

```
:volt 5
```

5. Verify peak-to-peak aberrations (overshoot plus ringing) are <5% +30 mV and the rise and fall times are <30 ns. If necessary, readjust C35 and repeat steps 2 through 5.

This completes the Model 1375 Calibration Procedure. Disconnect cables and test equipment, reinstall the module cover, and return the module inside the VXIbus chassis.

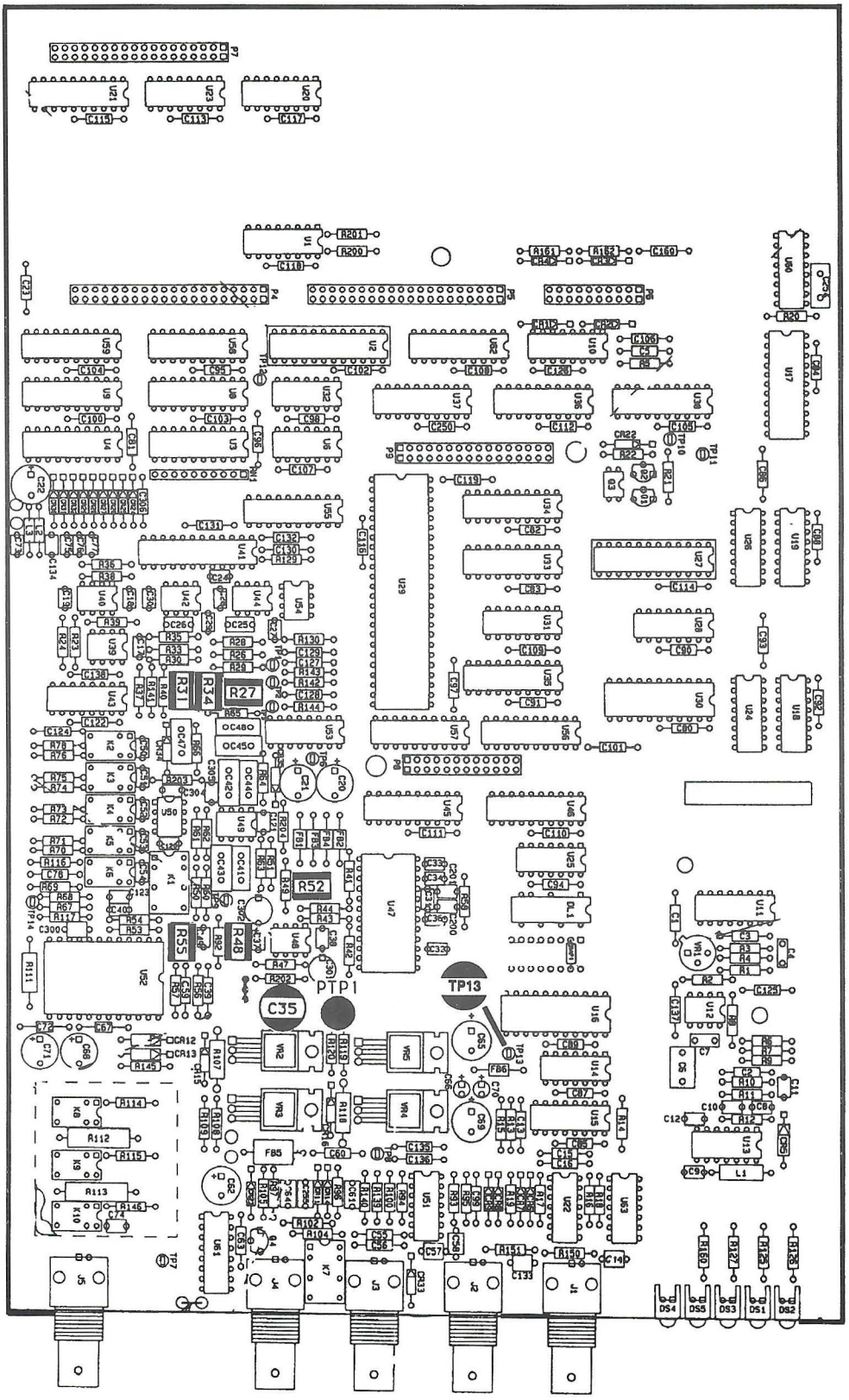


Figure 2-1. Test Points and Adjustments

SECTION 3
TROUBLESHOOTING

3.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned for calibration or repair, a detailed description of the specific problem and any related symptoms should be attached to the instrument. Before returning a unit to the factory, authorization from Customer Service must be obtained by calling or writing to:

Customer Service
Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone: (619) 279-2200
FAX: (619) 565-9558

3.2 BEFORE YOU START

A list of recommended spare parts is included in the drawings section of this manual (section 4). These parts should be ordered prior to an instrument failure to minimize repair turn-around time.

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the circuit description (section 1) in conjunction with the schematics (section 4). Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

WARNING

With covers removed, dangerous voltage points may be exposed. Do not be mislead by the term "low voltage". Contact with potentials as low as 40 volts could cause serious injury or even death.

The intent of this section is to provide the information required to return the instrument to proper operation. Before beginning the troubleshooting process, verify the instrument's subsystems are set correctly. For more information about instrument operation, refer to section 3 of the Operator's Manual. Also, try to rule out calibration as a possible problem. For instance, if the ARB OUT signal is offset with the filter on (even though no offset is programmed), but normal with the filter off, then the filter offset adjust pot, R52, quite possibly needs adjustment. Finally, inspect the instrument's wiring, and circuit boards for heat damage.

3.3 REQUIRED TEST EQUIPMENT

Required tools and test equipment are given in Table 3-1.

Table 3-1. Test Equipment and Tools

Equipment	Comments
Oscilloscope	Bandwidth: 250 MHz
Signal Source	Frequency: 1kHz to 12.5MHz Output: TTL
BNC 50Ω termination (2ea)	Accuracy: 0.1% Power: 2W
BNC Coax Cable (2ea)	RG58U, 3 ft. length
Scope Probe	X10

3.4 ISOLATING A PROBLEM

NOTE

If possible, take all measurements with only the controller and Model 1375 ARB in the chassis. Unless otherwise stated, terminate ARB OUT (and MARKER connectors if that circuit is being tested) into 50Ω.

When taking waveform readings within the instrument, always use a X10 probe to prevent loading and reduce the amount of ringing.

Begin the troubleshooting procedure by sending *TST? now. In most cases, running this test will help to isolate the faulty block. Refer to Appendix B of this manual to identify the failed test. If a number other than zero is returned after running *TST?, refer to Table 3-2 to identify the paragraph containing the information needed to isolate the faulty circuit block and related components.

If the *TST? test returns no fault even though a problem does exists, refer to Table 3-3. This table lists problems that self testing cannot identify.

Table 3-2. Problems Identified By *TST?

Test No.	Test Name	Paragraph
1	Trace Memory	3.5.1
2	Diagnostic Interface	3.5.2
3	DAC -Amplitude Reference	3.5.3
4	DAC +Amplitude Reference	3.5.4
5	Offset	3.5.5
6	Pre-amplifier	3.5.6
7	Power amp (Amplitude/Offset)	3.5.7
8	Filter	3.5.8
9	Pre-attenuator	3.5.9
10	Output Attenuator	3.5.10
11	Marker Position and Sync	3.5.11

Table 3-3. Problems Not Identified By *TST?

Problem	Paragraph
Abnormal LED State	3.5.12
Burst or Triggered Sequence Modes	3.5.13
External Clock Source (others normal)	3.5.14
Bus Trigger Source (others normal)	3.5.15
Internal Trig Source (others normal)	3.5.16
External Trig Source (others normal)	3.5.17
All Trigger Sources faulty	3.5.18
Backplane Clock Transmitting	3.5.19
Backplane Trigger Transmitting	3.5.20
Backplane Signal Receiving	3.5.21
Missing Marker Position or Sync Out	3.5.22

3.5 TROUBLESHOOTING

3.5.1 Test 1 Failure. Trace Memory

If the test number is set to 1, test 1, and the error code = 4, the trace memory failed. If the error code = 2, then a Bus Error occured when the VXI Interface Board tried to acces the Arb Board I/O. A Bus Error (BERR\) is generated by the CPU if the Data Transfer Acknowledge (DTACK\) is not returned from the Arb Board to the CPU before a timer runs out. DTACK\ is generated by a GAL, U2, shown in Figure 1-5 and sheet 2 of the Arb Board schematic. A Bus Error would be limited to U2 and its associated signal lines or to the board interconnect.

Proceed as follows to locate a trace memory failure. During power-up, data is written into, then read out of the RAM Module. This data flows through:

LD[15:0] P4 and P8

BLD[15:0] U56, U57, U58 and U59

WD[15:0]

Data locations are determined by:

LA[17:1] P5 and P9

BRA[16:0] U36, U37 and U38.

Control of data flow is by:

ACFAIL\ RAM\

LR/W RAMOE\

U2 RAMWE\

R/W

In addition, RAM\ controls U32/A.

The following components and signal lines must be working for the instrument to pass this test:

U1, U2, U32/A, U36, U37, U38, U56, U57, U58, U59

P4, P5, P8, or P9

RAM MODULE, Q1, Q2, Q3, or CR22

VXI Interface Board

Control lines ACFAIL\, LR/W, R/W, RAM\, RAMOE\, or RAMWE\

Address lines LA[17:1] or BRA[16:0]

Data lines LD[15:0], BLD[15:0], or WD[15:0]

When any portion of the microprocessor interface and data registers circuit is suspect, troubleshooting can be done by observing the symptoms to decide which checks will be used to locate a faulty digital circuit block. General techniques of troubleshooting digital systems are then applied to these blocks. One valuable technique involves using an oscilloscope to check for "stuck" bits on each line of a constantly varying address or data bus. A "stuck" bit may be constantly high, low, or tri-state (the output floats to a threshold level of 2 to 2.5V). It could also vary between a tri-state and a high or a low level without going to the third level. The cause of a "stuck" bit can

Table 3-4. Signal/Voltage Verification For Test 1

Test Point	Normal Reading	Possible Cause of Wrong Reading
U1 pins 1, 2 and 3	Verify full TTL range.	VXI Interface Board or U1
U1 pin 4	Signal is varying.	VXI Interface Board, U1, or U2
U1 pins 5, 7 and 9 through 15	TTL high	VXI Interface Board, U1, or any component attached to the suspect line
U2 pin 1	16 MHz TTL square	VXI Interface Board, U2, or R200
U2 pins 2, 6-10 and 23	Verify full TTL range.	VXI Interface Board, U1, U2
U2 pins 3 and 21	Signal is varying.	VXI Interface Board, U2, or any
U2 pins 4, 5, 11, 15, 16, 19 and 20	TTL high	component attached to the suspect line
U2 pin 17	TTL low	VXI Interface Board, U2, or RAM module
U32 pin 3	20 MHz TTL square	U24, U25 or any component attached to the suspect line
U32 pin 5	TTL high	U32, or any component attached to the suspect line
U32 pin 6	TTL low	U32, U33, U34, or U35
U36 pins 2, 3	Verify full TTL range.	VXI Interface Board, U1, or U36
U36 pins 4-9	Signal is varying.	VXI Interface Board, U36, or U62
U36 pin 11	2 kHz TTL square	U36 or any component on the suspect line
U36 pin 12	1 kHz TTL square	
U36 pins 13-18	TTL low	
U37 pins 2-9	TTL Signal is varying.	VXI Interface Board, U37, or U62
U37 pin 11	512 kHz TTL square	U36 or any component attached
U37 pin 12	256 kHz TTL square	to the suspect line
U37 pin 13	128 kHz TTL square	
U37 pin 14	64 kHz TTL square	
U37 pin 15	32 kHz TTL square	
U37 pin 16	16 kHz TTL square	
U37 pin 17	8 kHz TTL square	
U37 pin 18	4 kHz TTL square	
U38 pin 2	TTL Signal is varying.	VXI Interface Board, U37, or U62
U38 pin 18	1024 kHz TTL square	U35, U38 or any component attached to the suspect line
U56 pins 11-13	Varying TTL levels	U45, U46, U56, U57, or RAM
U56 pin 14	1 kHz TTL square	module
U56 pins 15-18	TTL low	
U57 pins 11-18	Varying TTL levels	
U58/U59 pins 2-9	TTL Signal is varying.	VXI Interface Board, U58, U59, or any component attached to the suspect line
U58/U59 pins 11-18	High Impedance	
Q1 Base	+4V	Q3 gate not high, Q1, Q3, or R21
Q2 Base		Q3 gate not high, Q2, Q3, or R22
Q3 Base	0V	Q3 gate not high, Q3, RAM module

be found by isolating IC pins and connectors from the line in question. If more than one line is "stuck", make a list of these lines and check for a common IC.

To identify the cause of a trace memory failure, do the following:

1. Verify U2, the RAM module and the VXI Interface Board are firmly in their connectors.
2. Verify +5V (power supply) at U6 pin 14. This supply originates from the VXIbus chassis.
3. Send the `TRACe:STATus?` query to get more information (see the Operator's manual for the figure and table describing the Memory Diagnostic Summary Word).
4. Check for proper voltages and signals as shown in table 3-4.

3.5.2 Test 2 Failure. Diagnostic Interface

If the test number is set to 2, and the error code bit 0 is set high, the diagnostic interface failed. When properly working during *TST?, U53 selects pin 12 (ground), passing 0V through U54/A and U54/B to U55. This analog voltage is converted to its digital equivalent and output to the VXI Interface Board on data lines BLD[9:0]. To pass this test, the analog voltage seen at U55 pin 14 must have a value of 0V ±0.02V.

To troubleshoot this circuit, a predictable set of conditions is achieved by sending `*RST` to the instrument. When this is done, the -AMP REF voltage at pin 4 (S1), which should always be -1V, is selected by U53 and passed through the diagnostic interface circuit to U55.

The following components and signal lines were not verified in the previous test and must be working for the instrument to pass this test:

U8

Control lines DIS0, DIS1, DIS2, CONVERT, or DDSTRB\

All diagnostic interface circuitry shown in sheet 12 of the Arb schematic.

To identify the cause of a diagnostic interface failure, do the following:

1. Verify the power supplies listed below. All supplies originate from the VXIbus chassis.

   +5V at U55 pin 11

   +12V at U54 pin 8

   -12V at U54 pin 4

2. Reset the instrument by sending:

   ```
   *rst;:trac:del:all
   ```

3. Check for proper voltages as shown in table 3-5.

3.5.3 Test 3 Failure. DAC Negative Amplitude Reference

If the test number is set to 3, and the error code bit 0 is set high, the DAC negative amplitude reference failed. This test verifies that the negative reference voltage from U40/B at the Waveform Digital to Analog Converter (TP1) is -1.0V ±5%. U39 and U40/A provide a +5V reference for U40/B.

The following components were not verified in a previous test and must be working for the instrument to pass this test:

U39, U40/A or U40/B

To identify the cause of a DAC negative amplitude reference failure, do the following:

1. Verify the power supplies listed below. All supplies except +10 at U39 pin 6 and +5V at U40/A pin 1 originate from the VXI chassis.

Table 3-5. Voltage Verification For Test 2

Test Point	Normal Reading	Possible Cause of Wrong Reading
U8 pins 17-19	TTL low	VXI Interface Board, U8, or any component attached to the suspect line
U53 pin 4	-1V	-AMP REF circuit (Arb schematic sheet 7. Also see the "Test 3 Failure" paragraph)
U54 pin 3		U53 or U54
U54 pin 1		U54
U54 pin 6	0V	
U54 pin 7	+0.5V	U54 or U55

Table 3-6. Voltage Verification For Test 3

Test Point	Normal Reading	Possible Cause of Wrong Reading
U40 pin 3	+5V	R23, R24, U40
U40 pin 6	0V	R36, R38, U40

Table 3-7. Test 4 Signal/Voltage Verification (Maximum Amplitude)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U41 pin 24	0V	U42/A or U44/B circuits
U41 pin 18	TTL low	U41 or U62
U42 pin 1	-5V	U41, U42/A circuit, U58, or U59
U42 pin 6	0V	U42/A, U42/B, U43/A, or U43/D circuits
U42 pin 7	+5.8V	U42/B, U43/A, 43/D circuits

Table 3-8. Test 4 Signal/Voltage Verification (Minimum Amplitude)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U41 pin 24	0V	U42/A or U44/B circuits
U42 pin 1	-4V	U41, U42/A circuit, U58, or U59
U42 pin 6	0V	U42/A, U42/B, U43/A, or U43/D circuits
U42 pin 7	+4.2V	U42/B, U43/A, 43/D circuits

+12V at U39 pin 2

+10V at U39 pin 6

+5V at U40/A pin 1 and U43 pin 12

-12V at U43 pin 4

2. Verify 0V (ground) at the points listed below:

   U39 pin 4, U40 pin 5 and U43 pin 5

3. Check for proper voltages as shown in table 3-6.

3.5.4 Test 4 Failure. DAC Positive Amplitude Reference

If the test number is set to 4, and either error code bits 0 or 1 are set high, the DAC positive amplitude reference failed. This tests the positive reference voltage from U42/B pin 7 at the Waveform Digital to Analog Converter. The +5V reference from U40/A pin 1 (verified during test 3) is summed at U42/B pin 6 with the amplitude control voltage from U41 pin 24 through U42/A and U43/D (filter off) to produce the positive reference at TP2. Maximum (+2.4V) and minimum (+0.7V) voltages are tested. If the test fails at +2.4V ±20%, error code bit 0 is set high. If the test fails at +0.7V ±20%, error code bit 1 is set high.

The following components and control lines were not verified in a previous test and must be working for the instrument to pass this test:

U1, U41 (amplitude half), U42/A, U42/B, U43/D

Control lines BLA15, AMOFS\ and FILTON

To identify the cause of a DAC positive amplitude reference failure, do the following:

1. Verify +12V at U43 pin 13. This power supply originates from the VXI chassis.
2. Verify 0V (ground) at the points listed below:

   U1 pin 8, U41 pins 1 and 5 and U43 pin 5

3. Turn the filter off and program amplitude to maximum by sending:

```
outp:filt off;:volt max
```

4. Check for normal readings as shown in table 3-7.
5. Change the amplitude to minimum by sending:

```
volt min
```

6. Check for normal readings as shown in table 3-8.

Table 3-9. Test 5 Signal/Voltage Verification (Maximum Offset)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U41 pin 2	0V	U42/A or U44/B circuits
U44 pin 1	-5V	U44/A circuit
U44 pin 2	0V	U44/A or U44/B circuits
U44 pin 7	0V	U44/B circuit

Table 3-10. Test 5 Signal/Voltage Verification (Minimum Offset)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U41 pin 2	0V	U42/A or U44/B circuits
U44 pin 1	+5V	U44/A circuit
U44 pin 2	0V	U44/A or U44/B circuits
U44 pin 7	-5V	U44/B circuit

3.5.5 Test 5 Failure. Offset Control

If the test number is set to 5, and either error code bits 0 or 1 are set high, the offset test failed. This test verifies that the offset control voltage at TP3 ranges from -5.0V to +5.0V ±5%. The +5V reference from U40/A pin 1 (verified during test 3) is summed at U44/A pin 2 with the offset control voltage from U41 pin 2 through U44/B. If the +5V test step fails, error code bit 0 is set high. If the -5V test step fails, error code bit 1 is set high.

The following components were not verified in a previous test and must be working for the instrument to pass this test:

U41 (offset half), U44/A, U44/B

To identify the cause of an offset control failure, do the following:

1. Program offset to maximum by sending:

```
volt:offs max
```

2. Check for normal readings as shown in table 3-9.
3. Change the offset to minimum by sending:

```
volt:offs min
```

4. Check for normal readings as shown in table 3-10.

3.5.6 Test 6 Failure. Pre-Amplifier Circuit

If the test number is set to 6, and either error code bits 0 or 1 are set high, the pre-amplifier test failed. This test verifies that the pre-amp circuit is able to output voltages at PTP1 of from -1.3V to +1.3V when controlled by the amplitude reference voltage. The filter is enabled, connecting PTP1 to TP9 (the actual test monitoring location) through relay K1. If the output fails the negative test step of -1.3V ±10%, error code bit 0 is set high. If the test fails the positive step of 1.3V ±10%, error code bit 1 is set high.

Both the trace value from the RAM MODULE and the AMP_REF voltage determine the waveform DAC output, and therefore the pre-amp output voltage. To control the trace value during this test, location '0' in the RAM MODULE (schematic sheet 6) is copied to the VXI interface board, then the midpoint trace value (2048) is written to the RAM location. The phase accumulator (U29 on schematic sheet 5) selects the location through U33, U34 and U35 (all outputs are low). U45 and U46 load the data from the RAM MODULE into the waveform DAC. After the test is completed, the original value is returned to the RAM MODULE.

The trace midpoint value of 2048 must be continually supplied by the RAM MODULE to the waveform DAC while troubleshooting most circuits that may cause this test to fail. To do this, the instrument is reset, the value '2048' is written to the first 8 RAM MODULE addresses using the line command, and the trace limit command insures that only these 8 addresses are read.

The following components, control and signal lines were not verified in a previous test and must be working for the instrument to pass this test:

The internal clock generator (PLL)

U3, U10/A, U16, U24, U25, U27, U29, U31, U33, U34, U35

Table 3-11. Test 6 Control Line Signal/Voltage Verification

Test Point	Normal Reading	Possible Cause of Wrong Reading
U3 pins 1, 13-15	TTL low	VXI Interface Board, U1, U3, U32, or any component attached to the suspect line
U3 pins 12, 16, 17, 19	TTL high	VXI Interface Board, U1, U3, or any com-
U3 pin 18		ponent attached to the suspect line
U43 pin 1	TTL low	U3 or U6A
U62 pins 3-9	TTL level pulses	VXI Interface Board or U62
U62 pins 11-17	TTL low	VXI Interface Board, U62, or any com-ponent attached to the suspect line

Table 3-12. Test 6 Signal/Voltage Verification

Test Point	Normal Reading	Possible Cause of Wrong Reading
U25 pins 2, 4, 6, 10	20 MHz TTL square	U24, U25 or any component attached to the suspect line
U25 pins 8, 9		DL1, SW1, U24, U25, or U47
U27 pin 7	TTL low	U26 or U27
U27 pin 8		U27 or U30
U27 pin 9	Positive TTL pulse. Pulse width is 0.3 µs. Pulse period is 1.0 ms.	U27 or U29
U27 pin 16	TTL high	U27 or U30
U27 pins 17, 22	TTL low	U27, U28, U29, or U30
U27 pins 18, 19	TTL low	U27 or U29
U27 pins 20, 21, 23	TTL high	U27, U28, U29, or U31
U29 pins 27-31, 33-38, 40, 41, 42	TTL low	U27, U29, U31, U33 or U34
U29 pin 43	1 kHz TTL square	U29 or U34
U29 pin 44	2 kHz TTL square	U29 or U34
U29 pin 45	4 kHz TTL square	U29 or U35
U31 pins 2, 4, 5, 7, 9, 11, 12, 14	TTL low	U28, U29, U31, or U33
U45 pins 12-19	TTL low	U57, U45, U47, or RAM module
U46 pins 8-9, 17-19	TTL low	U56, U46, U47, or RAM module
U46 pin 16	TTL high	U56, U46, U47, or RAM module

Table 3-13. Test 6 Signal/Voltage Verification (Maximum Amplitude)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U47 pins 6 and 7	-0.53V	U47 circuit
U47 pins 19, 20	-1V	R39, R40, R58, U47, or see paragraph 3.5.6
U47 pin 21	-1.5V	U47 or C31
U48 Pins 2 and 3	-0.3V	U48 circuit
U48 Pin 6	0V	U48 circuit

Table 3-14. Test 6 Signal/Voltage Verification (Minimum Amplitude)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U47 pins 6 and 7	-0.42V	U47 circuit
U47 pins 19, 20	-1V	R39, R40, R58, U47, or see paragraph 3.4.6
U48 Pins 2 and 3	-0.23V	U48 circuit
U48 Pin 6	0V	U48 circuit

Table 3-15. Test 6 PLL Control Line Voltage Verification

Test Point	Normal Reading	Possible Cause of Wrong Reading
U11 pin 11	TTL low	VXI Interface Board, U1, U6, or U11
U15 pin 9	TTL low	VXI Interface Board, U9, U15
U16 pin 8	TTL high	VXI Interface Board, U1, U16, U32, or any component attached to the suspect line
U16 pin 2	TTL low	VXI Interface Board, U1, U6, U16, U17, U30, or U32
U24 pin 2	TTL high	U9, U15, U23, or U24
U24 pin 14	TTL low	

Table 3-16. Test 6 PLL Circuitry Signal/Voltage Verification

NOTE

All readings in the PLL circuit are taken with the loop locked.

Test Point	Normal Reading	Possible Cause of Wrong Reading
U10 pins 2, 3	10 MHz ECL square	VXI Interface Board, U10, or any component attached to the suspect line
U10 pin 4	10 MHz TTL square	U10, U11 or U17
U11 pin 8	10 MHz TTL square	Phase lock loop not operating correctly
U11 pin 5	Tri-state	Phase lock loop not operating correctly
U12 pin 1	-3.7V	Phase lock loop not operating correctly
U12 pins 2, 3, 6	+2.5V	U11 pin 4 not +5V, C2 shorted, R1, R2, phase lock loop not operating correctly
U12 pin 7	+7V	Phase lock loop not operating correctly
U13 pins 1, 14 R11	+5V	U11 pin 4 not +5V, C10 shorted, C11 shorted, R10, or
U13 pin 3	20 MHz square, +3V to +4.25V	U13, phase lock loop not operating correctly
U13 pin 5	+1.4V	U11 pin 4 not +5V, R12, C12, or U13
U13 pin 10	+1.5V	Phase lock loop not operating correctly
U13 pin 12	20 MHz sinewave, +1V to +2V	Phase lock loop not operating correctly
U14 Pin 11, U15 pin 2	20 MHz TTL square	Phase lock loop not operating correctly
U15 pin 14	+3.5V	R13, R15, C13, or U15
U16 pin 20	20 MHz TTL square	U16, phase lock loop not operating correctly

U45, U46, U47, U48, K1, DL1

Control lines MODE0, MODE1 and MODE2

Signal lines WCLK1, WCLK2, WCLK3, WCLK4, BCLK10- and BCLK10+

To troubleshoot the circuits that may cause the pre-amplifier test to fail, do the following:

1. Verify U27 is firmly in its socket.
2. Verify power supplies (all supplies except +5V at U11 pin 4 originate from the VXI chassis);

   +12V at U12 pin 8

   +12V at left lead of C1

   +5V at U10 pin 9

   +5V at U11 pin 4

   -2V at bottom lead of R161

   -5.2V at U10 pin 8

   -12V at U12 pin 4
3. Verify 0V (ground) at the points listed below:

   Pin 10 of U3, U33, U34, U35, U45 and U46

   U10 pin 16

   U11 pin 6

   U13 pins 7 and 8

   Pin 7 of U14 and U25

   Pin 8 of U15, U24 and U31

   U16 pins 14 and 17

   U27 pin 12

   U29 pins 15, 32, 39 and 46

   U47 pins 5 and 8
4. Reset the instrument by sending:

   ```
   *rst;:trac:del:all
   ```

   Verify a 20 MHz TTL square wave at U24 pin 7. If not normal, troubleshoot the PLL circuit (see step 10).
5. Enable the filter and set amplitude to maximum, then write "2048" to the first 8 addresses and limit the viewed trace addresses to between '0' and '7' by sending:

   ```
   outp:filt on;:volt max

   trac:def test,8;lim test,0,7;
   line test,0,2048,7,2048
   ```
6. Check for normal control readings as shown in table 3-11.
7. Check for normal readings as shown in tables 3-12 and 3-13.
8. Change the amplitude from maximum to minimum by sending:

   ```
   volt min
   ```
9. Check for normal readings as shown in table 3-14.
10. Check for normal PLL control readings as shown in table 3-15.
11. Check for normal readings as shown in table 3-16. Begin with those test points where the "phase lock loop not operating correctly" statement is **not** listed as a possible cause of a wrong reading.

    NOTE

    All readings in the PLL circuit are taken with the loop locked.

3.5.7 Test 7 Failure. Power Amplifier Circuit

If the test number is set to 7, and error code bits 0, 1, 2 or 3 are set high, the power amplifier test failed. This test, conducted in two parts, verifies that the power amplifier circuit is functioning properly. For the first part of test 7, the pre-attenuator is set for minimum attenuation, offset is set to zero and the amplitude DAC (U41) is set to maximum. Values are loaded into the RAM MODULE (as explained in test 6, but with the filter off for test 7) that cause the waveform DAC (U47) to first set the instrument output for +8.0V, then -8.0V. This voltage is monitored at TP6, and must be within ±10% of the expected results to pass the test. If the positive step (+8V) fails, error code bit 0 is set high. If the negative step (-8V) fails, error code bit 1 is set high. Only the power amplifier and its associated circuitry can cause this test to fail because all other circuitry used in this test has already passed earlier tests.

The second part of test 7 sets the pre-attenuator to 1:32, the waveform DAC to 0V (amplitude DAC remains at maximum), and offset, controlled by U41 pin 2, is set first for +8.0V, then -8.0V, and verified to be within ±10% of the setting. If the positive offset step fails, error code bit 2 is set high. If the negative offset step fails, error code bit 3 is set high. Only K2 of the pre-attenuator and its associated resistors can cause this test to fail because all other circuitry used in this test has already passed earlier tests.

To troubleshoot the power amplifier, do the following:

1. Verify U52 is firmly in its socket.
2. Verify +24V at VR2 "IN", and -24V (power supplies) at VR4 "IN". These supplies originate from the VXI chassis.
3. Verify 0V (ground) at U52 pin 24.

Table 3-17. Test 7 Power Amplifier Voltage Verification

Test Point	Program	Normal Reading	Possible Cause of Wrong Reading
VR3 "IN"	See step 4 (above)	+20V	R107, C66, or VR3
VR5 "IN"		-20V	R118, C70, or VR5
U52 pins 6, 8		0V	U52 and associated circuitry
U52 pin 12		+8V	
U52 pins 6, 8	`trac:lim test,5000,5007`	0V	
U52 pin 12		-8V	
U52 pins 6, 8	`volt min;:volt:offs 4`	0V	
U52 pin 12		+8V	
U52 pins 6, 8	`volt:offs -4`	0V	
U52 pin 12		-8V	

4. Reset the instrument, define a square wave, limit the viewed trace addresses to the positive portion of the waveform, and set the amplitude to +4V by sending:

```
*rst;:trac:del:all

trac:def test,squ;:trac:lim
test,0,7;:volt 4
```

5. Verify -0.55V at TP14. If this is not correct, refer to pre-attenuator test, paragraph 3.3.9.
6. Program the instrument and check for proper voltages as shown in table 3-17.
7. If test 7 and error codes 2 or 3 are set, and if the above steps have not isolated the problem, refer to pre-attenuator test, paragraph 3.3.9.

3.5.8 Test 8 Failure. Filter Offset

If the test number is set to 8, and the error code bit 0 is set high, the filter offset test failed. This test verifies that the filter does not introduce any dc offset. The first part of test 7 is run with the filter off and an output amplitude of +9V used as a reference measurement, then the filter is enabled and the test repeated. The test results must agree within ±2%. Only the filter circuit and relay K1 can cause this test to fail because all other circuitry used in this test has already passed earlier tests.

To troubleshoot the 4 MHz, low pass filter, do the following:

1. Verify +6V at U49 pin 7, and -6V (power supplies) at U49 pin 4.
2. Reset the instrument, define a square wave, limit the viewed trace addresses to the positive portion of the waveform, and set the amplitude to +0.5V by sending:

```
*rst;:trac:del:all

trac:def test,squ;:trac:lim
test,0,7;:volt .5
```

3. Check for proper voltages as shown in table 3-18.
4. Program:

```
outp:filt on
```

Check for proper voltages as shown in table 3-19.

3.5.9 Test 9 Failure. Pre-Attenuator Circuit

If the test number is set to 9, and error code bits 0, 1, 2, 3 or 4 are set high, the Pre-attenuator test failed. The first part of test 7 is run at maximum amplitude and used as a reference measurement, then the signal is attenuated in binary steps of 2, 4, 8, 16, and 32 and verified to be within ±30 mV of the expected values.

By programming two specific amplitudes (0.4V and 1V), as in this procedure, each relay (and therefore each binary step) is fully exercised.

The following components and control lines were not verified in a previous test and must be working for the instrument to pass this test:

U4

Pre-attenuator circuit, including control lines and relays

To troubleshoot the pre-attenuator, do the following:

1. Verify +5V at top of C124. If the +5V supply is not normal, L2 or C134 are likely faulty.
2. Reset the instrument, define a square wave, and limit the viewed trace addresses to the positive portion of the waveform by sending:

Table 3-18. Test 8, Filter Offset Voltage Verification (Filter Off)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U49 pins 3, 6	0 V	K1 or U49 circuit
U50 pins 3, 6	0 V	U50 circuit
R78 Top	-1.4 V	K1

Table 3-19. Test 8, Filter Offset Voltage Verification (Filter On)

Test Point	Normal Reading	Possible Cause of Wrong Reading
U49 pins 3, 6	-1.4 V	K1 or U49 circuit
U50 pins 3, 6		U50 circuit
R78 Top	Maximum ±2% from table 3-18 reading	K1 or filter circuit

Table 3-20. Test 9 Pre-Attenuator Voltage Verification

Error Codes Returned	**0, 1, 4**	**2, 3**
Binary Steps Enabled	2, 4, 32	8, 16
To Enable The Above Binary Steps, Program:	`volt .4`	`volt 1`
Control Lines Low (Relays On)	PRE1\, PRE4\, PRE5\	PRE2\, PRE3\
Relays Energized	K2, K5, K6	K3, K4
Normal Voltage Readings		
R78 (Top)	-1.4V	-1.3V
R78 (Bottom)	-1.0V	-0.75V
R73 (Top)	-0.6V	-0.85V
R73 (Bottom)	-0.5V	-0.75V
R69 (Top)	-0.7V	-0.35V
R69 (Bottom)	-0.55V	-0.14V

```
*rst;:trac:del:all

trac:def test,squ;:trac:lim
test,0,7
```

3. Table 3-20 contains relay information and circuit voltages for the pre-attenuator circuit. If error codes 0, 1 or 4 were returned , program:

   ```
   volt .4
   ```

   Refer to the information in the middle column of table 3-20. If error codes 2 or 3 were returned during the self-test, program:

   ```
   volt 1
   ```

   Refer to the information in the right column of table 3-20. Regardless of the returned error code, it may be necessary to program both voltages and verify the results.

3.5.10 Test 10 Failure. Output Attenuator Circuit

If the test number is set to 10, and error code bits 0, 1, 2, 3, 4 or 5 are set high, the output attenuator failed.

This test verifies that the output attenuator voltage is ±30 mV of its expected positive and negative values for the 10:1 and 100:1 positions at TP7.

The following components and control lines were not verified in a previous test and must be working for the instrument to pass this test:

U4

Output attenuator circuit, including control lines and relays

To troubleshoot the output attenuator, do the following:

1. Verify +5V at the right end of C73. If the +5V supply is not normal, L3, C73 or C74 are likely faulty.
2. Reset the instrument and define a square wave by sending:

   ```
   *rst;:trac:del:all

   trac:def test,squ
   ```

Table 3-21. Test 10 Output Attenuator Voltage Verification

Error Code Re-turned:	0	1	2	3	4	5
Signal Attenuation:	1:1	10:1	100:1	1:1	10:1	100:1
Program to set Attenua-tion:	`volt .9`	`volt .09`	`volt .009`	`volt -.9`	`volt -.09`	`volt -.009`
Control Line Low (Relay On):	None	-20 DB	-20DB and -40 dB	None	-20 dB	-20 dB and -40 dB
Relay(s) Energized		K8	K8 and K9		K8	K8 and K9
Relay Pins Short-ed:						
K8	5-10	1-5	1-5	5-10	1-5	1-5
K9		5-10			5-10	
Normal Voltage Readings:						
R112 (Top)	+1.8V	+1.	7V	-1.8V	-1.7V	-1.7V
R112 (Bottom)		+0.2V	+0.15V		-0.2V	-0.15V
R113 (Bottom)			+20 mV			-20 mV

3. Table 3-21 contains relay information and circuit voltages for the output attenuator circuit. If error codes 0, 1 or 2 were returned during the self-test, limit the viewed trace addresses to the positive portion of the waveform by programming:

   ```
   trac:lim test,0,7
   ```

   Refer toTable 3-21 to set amplitude and check results. If error codes 3, 4 or 5 were returned during the self-test, program:

   ```
   trac:lim test,5000,5007
   ```

   Refer to Table 3-21 to set amplitude and check results.

3.5.11 Test 11 Failure. Marker Position and Sync Circuit

If the test number is set to 11, and error code bits 0, 1, 2, 3, 4 or 5 are set high, the marker position and sync test failed. The marker position and sync signals are summed through a resistive divider at the driver outputs to verify proper voltages.

To troubleshoot the marker position and sync circuit, do the following:

1. Verify +5V at U51 pins 6 and 14, and U61 pin 16. Verify -5.2V at U51 pin 13 (power supplies). These supplies originate from the VXI chassis.
2. Verify 0V (ground) at U51 pin 7 and U61 pin 8.
3. Reset the instrument by sending:

   ```
   *rst;:trac:del:all
   ```

4. Verify the following voltages:

   C56 Bottom = TTL High

   U51 pin 1 = 0V

   U61 pin 1 = TTL High

   NOTE

   Because of programming constraints, troubleshooting of some error code bits is done using conditions which approximate, but are not exactly the same as those that caused the self-test to fail. These differences will not adversely affect the troubleshooting process.

5. Using the returned error code bit that identified the failed test, program the instrument as shown in table 3-22.
6. Using the same error code bit, refer to voltage and signal information in the proper column of table 3-23.

3.5.12 Abnormal LED State

The VXI Interface Board controls each front panel LED. The LED states may be used to fault isolate between the VXI Interface Board and the Arb Board.

RUN LED

The green RUN LED should be on continuously, indicating that the Interface Board CPU is operational. Troubleshoot an off LED as follows:

1. Verify that the 1375 module is in fact non-operational. Verify that other modules are operational in the chassis. If the 1375 module is operational, but the LED is out, troubleshoot the LED and the RUN LD\ line (see sheet 1 of the Arb Board schematic).

Table 3-22. Test 11 Marker Programming

Error Code	Program:
0 and 1	`mark:sync bbit;:trac:def test,8;data test,sin;:trac:sel test`

2 and 3	`mark:sync bbit;:trac:def test,8;data test,sin;:trac;sel test`
	`mark:pos:poin test,0;poin test,1;poin test,2`
	`mark:pos:poin test,3;poin test,4;poin test,5`
	`mark:pos:poin test,6;poin test,7`

4 and 5	Use the default state. Do not program the instrument.

Table 3-23. Test 11 Marker Voltage Verification

Test Point	Error Code		
	0 and 1	2 and 3	4 and 5
U51 Pin 2	Immaterial		±1.25V Sine Wave
U51 Pin 4	TTL High		TTL Level Square Wave
U51 Pin 5	TTL Low		TTL High
U51 Pin 9	TTL Level, 1.0 ms Period, 0.1ms Wide, Negative-Going Pulse		TTL Level Square Wave
U51 Pin 11	+1.5V		0V to +5V Square Wave
U51 Pin 12	TTL Level, 1.0 ms Period, 0.1ms Wide, Negative-Going Pulse		TTL Low
U61 Pin 4	TTL Level, 1.0 ms Period, 0.1ms Wide, Positive-Going Pulse		0V to +5V Square Wave
U61 Pin 7			0V to +3.5V Square Wave
U61 Pin 9	TTL Low	TTL High	TTL Low
U61 Pin 10			

2. If the 1375 module is non-operational, the fault may be in either board. To isolate the problem, power down the system, remove the 1375 module, remove the left side panel and then the VXI Interface Board from the 1375 module. Plug the Interface Board directly on to the P1 and P2 connectors of the VXI chassis and reboot the system. Check the module status using the host computer. If the Interface Board is good, it will identify itself normally in its slot as a Wavetek Model 1375. A SYSTem:ERRor? query would show an error message, but this is because the Interface CPU does not get a DTACK\ response with the Arb Board removed. If the Interface Board is still non-operational, call Wavetek customer service at (619)279-2200 to arrange for repair.
3. If the Interface Board is operational, reinstall it in the module and troubleshoot the interconnect signals, P4 through P7, on the Arb Board (see sheet 1 of the Arb Board schematic).

FAIL LED

The FAIL LED should be off, except during the first 4.9 seconds after power-up. If the LED is on after system power-on, the Interface Board was either not able to initialize its configuration registers or it failed its own self test. This is not to be confused with the Self Test of the Arb Board. If the FAIL LED is on, the Interface is not operational. Use the same procedure as for the RUN LED to fault isolate between the Interface Board and the Arb Board.

NOTE

If the RUN and FAIL LEDs are operating normally, troubleshoot the remaining LEDs in a straight-forward fashion (see sheet 1 of the Arb Board schematic).

MODID LED

The MODID LED flashes on momentarily during power-up. This may be too short in duration to be seen.

A16 LED

The A16 LED flashes on while the VXI Interface Board is being addressed by the VXIbus.

A24 LED

The A24 LED illuminates during a VMEbus access to the A24 shared memory.

Table 3-24. Burst Mode Troubleshooting

Test Point	Normal Reading	Possible Cause of Wrong Reading
U27 pin 1	20 MHz TTL square	U9 or U25
U27 pin 2	TTL high	RN1 or U3
U27 pin 3	TTL low	
U27 pin 4	TTL high	
U27 pin 6	TTL high	VXI Interface Board
U27 pin 7	TTL low	U26
U27 pin 8	Negative pulse coincident with the last cycle	U27 or U30
U27 pin 9	TTL low	U27 or U29
U28 pin 1	TTL high	U27
U28 pin 2	TTL low	U27 or U30
U28 pins 11-14	TTL level pulses with various symmetries	U27, U28 or U30
U30 pins 1, 7, 8	TTL high	U1, U27, or any component attached to the suspect line
U30 pin 2	TTL low	U1, U6, or any component attached to the suspect line
U30 pin 3	High Impedance	VXI Interface Board, U59, or any component attached to the suspect line

3.5.13 Burst or Triggered Sequence Modes Not Working

Neither U28, nor U30 are verified during *TST?. In addition, most control and signal lines attached to them are also not tested. By programming the instrument for burst mode, a fault preventing either burst or triggered sequence modes from operating may be located.

To troubleshoot faulty burst or triggered sequence modes, do the following:

1. Verify +5V at U28 pin 16, and U30 pins 6 and 18. This supply originates from the VXI chassis.
2. Verify 0V (ground) at U28 pin 8 and U30 pins 14 and 17.
3. Reset the instrument and enable the output by sending:

```
*rst;:trac:del:all;:outp on
```

4. Change the output frequency to 10 kHz, enable the burst mode, and set the burst count to 5 by sending:

```
freq 1e4;:mode burs;:burs 5
```

5. Verify the readings in Table 3-24.

3.5.14 External Clock Source Not Working

Since other clock sources are functional, U22 or its input circuitry is most likely faulty.

To troubleshoot the external clock source circuitry, do the following:

1. Verify +5V at U22 pin 5. This supply originates from the VXI chassis.
2. Verify +1.46V at U22 pin 11.
3. Verify the readings in table 3-25 *without* an external clock connected.
4. Inject a 20 MHz, TTL level square wave at the CLOCK IN BNC.
5. Verify the readings in table 3-25 *with* an external clock connected.

3.5.15 BUS Triggering Problem

Because all other sources of triggering are functional, the VXI Interface Board, U1, or U26 are most likely faulty.

To troubleshoot the programmed trigger circuitry, do the following:

1. Verify +5V at U26 pin 16. This supply originates from the VXI chassis.

Table 3-30. Backplane Clock Transmitter Signal Troubleshooting

Backplane Line Being Tested	Program	Control Line Status (U20)		Signal Path
		Pin 2	Pin 3	
TTLTRG1	`outp:cloc0:sour ext` `outp:cloc0 1`	TTL Low	TTL Low	U20 Pin 4, U21 Pin 18
TTLTRG3	`outp:cloc1:sour ext` `outp:cloc1 1`	TTL High	TTL Low	U20 Pin 5, U21 Pin 16
TTLTRG5	`outp:cloc2:sour ext` `outp:cloc2 1`	TTL Low	TTL High	U20 Pin 6, U21 Pin 14
TTLTRG7	`outp:cloc3:sour ext` `outp:cloc3 1`	TTL High	TTL High	U20 Pin 7, U21 Pin 12

Table 3-31. Backplane Clock Transmitter Source Troubleshooting

Test Point	Normal Reading	Possible Cause of Wrong Reading
U18 pin 6	12.5 MHz TTL square	U18
U18 pin 11, U21 pin 1	TTL low	U9

3.5.19 Backplane Clock Transmitting Problem

One of the four backplane clock output paths through U20/A is always selected by the logic levels of pins 2 and 3. The clock signal from pin 1 (a 12.5 MHz, TTL level square for this test) is placed on the selected line (pins 4 through 7). Each unselected path should be TTL high.

The selected clock is isolated from the backplane unless U21/A is enabled by a low at pin 1. U21 pins 12, 14, 16 and 18 should be TTL high unless selected as the backplane clock signal path. If selected during this test, one of these four pins should have a 12.5 MHz, TTL level square.

Before beginning the procedure, if possible, remove all modules from the VXI chassis except the slot 0 controller and the faulty Model 1375. If this cannot be accomplished, verify that no other instrument is transmitting onto the backplane.

To troubleshoot the backplane clock transmitting circuitry, do the following:

1. Verify +5V at U18 and U20 pin 16, and U21 pin 20. This supply originates from the VXI chassis.
2. Verify 0V (ground) at U18 and U20 pin 8, and U21 pin 10.
3. Reset the instrument by sending:

```
*rst;:trac:del:all
```

4. Inject a 12.5 MHz, TTL level square wave (terminated with 50Ω) at the CLOCK IN BNC.
5. Attempt to transmit the external clock signal on the faulty backplane line by sending the appropriate programming statement as shown in table 3-30, but do not yet verify the control line status or signal path as shown in this table.
6. Verify the readings in Table 3-31.
7. Verify proper operation of the control lines and signal paths as shown in table 3-30. If a control line is faulty, the cause is most likely U9 or U20. If a signal line is faulty, the cause is most likely U20, U21, or the backplane.

3.5.20 Backplane Trigger Transmitting Problem

One of the four backplane trigger output paths through U20/B is always selected by the logic levels of pins 13 and 14. The trigger signal from pin 15 (a 2 MHz, TTL level square for this test) is placed on the selected line (pins 9 through 12). Each unselected path should be TTL high.

The selected trigger is isolated from the backplane unless U21/B is enabled by a low at pin 19. U21 pins 3, 5, 7 and 9 should be TTL high unless selected as the backplane clock signal path. If selected during

Table 3-32. Backplane Trigger Transmitter Signal Troubleshooting

Backplane Line Being Tested	Program	Control Line Status (U20)		Signal Path
		Pin 13	Pin 14	
TTLTRG0	`outp:ttlt0 on`	TTL Low	TTL Low	U20 Pin 12, U21 Pin 9
TTLTRG2	`outp:ttlt1 on`	TTL Low	TTL High	U20 Pin 11, U21 Pin 7
TTLTRG4	`outp:ttlt2 on`	TTL High	TTL Low	U20 Pin 10, U21 Pin 5
TTLTRG6	`outp:ttlt3 on`	TTL High	TTL High	U20 Pin 9, U21 Pin 3

Table 3-33. Backplane Trigger Transmitter Source Troubleshooting

Test Point	Normal Reading	Possible Cause of Wrong Reading
U19 pin 2	2 MHz TTL level square	U17 or U60
U19 pin 6		U19
U19 pins 10, 11	TTL low	U8
U21 pin 19		U3

this test, one of these four pins should have a 2 MHz, TTL level square.

Before beginning the procedure, if possible, remove all modules from the VXI chassis except the slot 0 controller and the faulty Model 1375. If this cannot be accomplished, verify that no other instrument is transmitting onto the backplane.

To troubleshoot the backplane trigger transmitting circuitry, do the following:

1. Verify +5V at U19 and U20 pin 16, and U21 pin 20. This supply originates from the VXI chassis.
2. Verify 0V (ground) at U19 and U20 pin 8, and U21 pin 10.
3. Reset the instrument and change the internal trigger frequency to 2 MHz by sending:

```
*rst;:trac:del:all;:trig:freq
2e6
```

4. Attempt to transmit the internal trigger signal on the faulty backplane line by sending the appropriate programming statement as shown in Table 3-32, but do not yet verify the control line status or signal path as shown in this table.
5. Verify the readings in table 3-33.
6. Verify proper operation of the control lines and signal paths as shown in table 3-32. If a control line is faulty, the cause is most likely U8 or U20. If a signal line is faulty, the cause is most likely U20, U21, or the backplane.

3.5.21 Backplane Signal Receiving Problem

One backplane clock and one backplane trigger signal may be selected by U23, but only as a pair (i.e. 1A/2A, 1B/2B, etc.). Selection is made by the logic levels of pins 2 and 14, and enabled by pins 1 and 15. For this test, a 2MHz, TTL level square originating from U21/B, and a 12.5 MHz, TTL level square originating from U21/A will be the signal sources.

U23 pins 3 through 6 and 10 through 13 should be TTL high unless selected as a backplane signal path. If selected during this test, one of these four pins should have a 12.5 MHz, TTL level square.

Before beginning the procedure, if possible, remove all modules from the VXI chassis except the slot 0 controller and the faulty Model 1375. If this cannot be accomplished, verify that no other instrument is

Table 3-34. Backplane Signal Receiving Troubleshooting

Backplane Lines Being Tested	Program	Control Line Status (U23)		Signal Path
		Pin 2	Pin 14	

TTLTRG0/1	`outp:cloc0:sour ext`
	`outp:cloc0 on`
	`rosc:sour cloc0`
	`outp:ttlt0 on`
	`trig:sour ttlt0`
		TTL Low	TTL Low	U23 Pin 6 to U23 Pin 7
				U23 Pin 10 to U23 Pin 9

TTLTRG2/3	`outp:cloc1:sour ext`
	`outp:cloc1 on`
	`rosc:sour cloc1`
	`outp:ttlt1 on`
	`trig:sour ttlt1`
		TTL Low	TTL High	U23 Pin 5 to U23 Pin 7
				U23 Pin 11 to U23 Pin 9

TTLTRG4/5	`outp:cloc2:sour ext`
	`outp:cloc2 on`
	`rosc:sour cloc2`
	`outp:ttlt2 on`
	`trig:sour ttlt2`
		TTL High	TTL Low	U23 Pin 4 to U23 Pin 7
				U23 Pin 12 to U23 Pin 9

TTLTRG6/7	`outp:cloc3:sour ext`
	`outp:cloc3 on`
	`rosc:sour cloc3`
	`outp:ttlt3 on`
	`trig:sour ttlt3`
		TTL High	TTL High	U23 Pin 3 to U23 Pin 7
				U23 Pin 13 to U23 Pin 9

transmitting onto the backplane.

To troubleshoot the backplane receiving circuitry, do the following:

1. Verify +5V at U23 pin 16. This supply originates from the VXI chassis.
2. Verify 0V (ground) at U23 pin 8.
3. Reset the instrument and change the internal trigger frequency to 2 MHz by sending:

   `*rst;:trac:del:all;:trig:freq 2e6`
4. Inject a 12.5 MHz, TTL level square wave at the CLOCK IN BNC.
5. Program the instrument to send and receive the external clock and internal trigger signals on the faulty backplane line(s) by sending the appropriate programming statements as shown in Table 3-34.
6. Verify U23 pins 1 and 15 are TTL low. If not correct, U8 or U23 are most likely faulty.
7. Verify the control line and signal status in table 3-34.
8. Verify U24 pin 2 is TTL high and pin 14 is TTL low to select VXICLK. The VXI clock signal should be on pin 7.
9. Verify U26 pin 2 is TTL high and pin 14 is TTL low to select VXITRGN\. The VXI trigger signal should be on pin 7.

3.5.22 Missing Marker Position or Sync

If the Marker Position Output and/or the Marker Sync Output is missing, even though unit passes self-test (*TST?) only K7, control line SYNCOUT\ or associated circuitry will be at fault.

APPENDIX A
SPECIFICATIONS

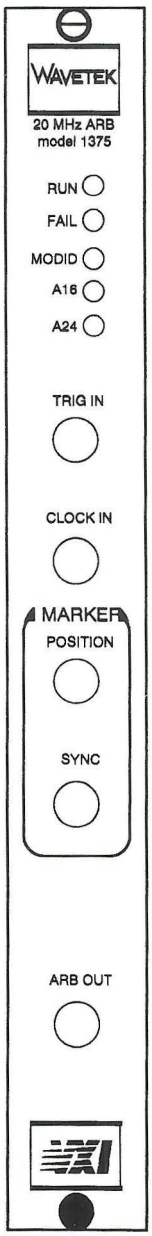


Figure A-1. Wavetek Model 1375 20 MHz VXI Arbitrary Waveform Generator

MODEL 1375

The Arbitrary waveform generator has a variety of applications in scientific research, test and measurement, industrial facilities, and in commercial use, limited only by the users imagination. Using the Arb, waveshapes can be created which simulate a wide range of natural events. Waveshapes can be created based on known data then altered to research a variety of possible malfunctions or improvements. Used in conjunction with other VXI modules, the Model 1375 Arb becomes part of a system that uniquely simulates an event which can be measured by other instruments.

STANDARD FEATURES

The Model 1375 Arb adheres to the Standard Commands for Programmable Instruments (SCPI) remote programming format Version 1.0, April 1990 (refer to the SCPI manual for further information). SCPI is a new industry standard language for remote instrument programming. The Wavetek Model 1375 Arbitrary Waveform Generator is a single slot C size ,VXI module.

Modes of Operation

The Arb has six operating modes: a Continuous mode, two Gated modes, a Triggered mode, a Burst mode, and a Triggered Sequence mode. The Triggered Sequence mode operates on 8192 point blocks, the others operate on the selected waveform.

Resolution

The Model 1375 has a minimum of 8 and a maximum of 32,768 locations (32K) of addressable waveform points (a 128K option is available). The vertical resolution of each point is 12 bits (4096 values). Single waveforms may be assigned any size between 8 points and the maximum memory remaining.

Frequency

The output signal has a frequency range from 100 mHz to 2.5 MHz. The frequency accuracy is dependent on the clock reference used. The default clock uses the VXI Resource Manager 10 MHz clock, CLK10.

Amplitude and Offset

The output amplitude ranges from 5mVp to 5Vp into 50Ω with a resolution of 3-1/2 digits and a default of 1Vp. A dc offset between -5V and +5V may be selected with a resolution of 3-1/2 digits and a default of 0V. Amplitude and Offset are coupled, limiting the output voltage to 5Vp.

Inputs

The Model 1375 Arb has two TTL signal inputs on the front panel, clock and trigger. The external clock frequency may range from DC to 20 MHz, the external trigger may range from 1 mHz to 2MHz. Additionally, four clock and four trigger inputs can be accessed through the VXI backplane TTLTRG lines. The clock and trigger input lines from the backplane are limited by the VXI specifications to a maximum of 12.5 MHz.

Outputs

The Model 1375 Arb has three output signals on the front panel: the arbitrary waveshape that has been created, the Marker Sync and the Marker Position. The Arb also provides both a clock and a trigger output to the selected VXI TTLTRG lines. The source of both the clock and trigger output provided to the backplane is selectable.

Data Sources

The Arb has a variety of ways to create a waveform. External binary data may be down loaded from a host. Internal "standard waveform" algorithms in ROM will create exactly one cycle of the waveform (random and dc, obviously, are not cyclical). Previous user created waveshapes residing in memory may be copied. Waveforms can be built from entered line segments.

Editing

The Model 1375 has several editing features. After filling the allocated memory with data defining the waveform, the user may select the entire waveform or only a portion to be "played back" (Trace-Limit command). Any selected portion may be used for creating a new waveshape (Trace-Data command). An existing trace may be overwritten with new data (Trace-Data command). Any trace may be expanded or reduced by copying it into a different size memory; the integrity of the shape is maintained (Trace-Data command). Wave-shape segments may be copied end to end creating new shapes (Trace-Data command). A trace may be re-sized (Trace-Points command). A line segment can be created (Trace-Line command). Any waveform in the directory can be selected for "play back" (Trace-Select command). Traces may be deleted individually or globally (Trace-Delete command).

SPECIFICATIONS

Modes

Continuous:
Waveform is continuously generated.

Triggered:
One cycle of waveform generated for each trigger.

Asynchronous gated:
Waveform generated only when trigger is high.

Synchronous gated:
Waveform generated only when trigger is high, completes existing cycle after trigger goes low.

Burst:
Waveform repeats between 1 and 10,000,000 times.

Triggered Sequence:
Waveforms generated using 1, 2, 3, or 4 sequentially triggered 8192 point blocks (16 blocks with option 01).

Maximum trigger frequency is 2MHz.

Block switching time: <200 nS in CW mode or 2 clock cycles in Raster Mode.

Waveform Resolution

Horizontal:
32K points, 128K points with option 01.

Vertical:
12 bits.

Trace Output Characteristics

Settling Time:
40 nS to 0.1%.

Square Transition:
<35 ns, 10% to 90% at 5Vp.

Square Aberrations:
Overshoot/ringing
0.501 Vp to 5Vp, <6% + 40 mV
0.0501 Vp to 0.5 Vp, <6% + 4mV
0.00501 Vp to 0.05 Vp, <6% + 1mV

Sine Distortion:
(400 mVpp < V< 10Vpp, 4MHz filter on)
F_O< 20 kHz, harmonics < -60 dBc (< 0.2% THD)

20 kHz < F_O < 100 kHz, harmonics < -50 dBc (< 0.7% THD)
100 kHz <F_O< 2.5 MHz harmonics, -40 dBc.

Intermodulation Products (Spurs):
4MHz filter on
<1MHz, -50dBc, limited by 50μVpp.
≥1MHz, -60dBc, limited by 50≥Vpp.

Output Frequency

Range:
100 mHz to 2.5 MHz.

Resolution:
10 mHz at output frequencies > 100 Hz; 1mHz at output frequencies <100 Hz.

Accuracy:
Provided by the selected clock source.
Internal source, provided by VXIbus CLK10 . Frequency accuracy is equal to the selected source accuracy specification + 10 nHz.

Amplitude

Range:
5mVp to 5Vp into 50Ω, coupled to offset.
Default: 1Vp.

Resolution:
3 1/2 digits.

Accuracy:
±(1.0% + 5mV) at 0.505 Vp to 5.000 Vp.
±(1.0% + 0.5 mV) at 0.0505 Vp to .5000 Vp.
±(1.0% + 0.05 mV) at 5.00 mVp to 50.00 mVp.

Flatness:
Sine response relative to 1kHz sine, filter on.
±2% from 40 Hz to 50 kHz.
±5% from 50 kHz to 1MHz.
±10% from 1MHz to 2.5 MHz.

Monotonicity:
0.2% (9 bits).

Offset

Range:
±5V into 50Ω, coupled to amplitude.

Resolution:
3 1/2 digits.

Accuracy:
±(1.5% + 0.5 mVdc) at 0mVdc to ±50.0 mVdc.
±(1.5% + 5mVdc) at ±50.1 to ±500.0 mVdc.
±(1.5% + 25 mVdc) at ±0.501 to ±5.0 Vdc.

Clocks

CW Mode:
20 MHZ when Internal clock selected.
Accuracy provided by the selected source.
Internal selection accuracy (VXI CLK10) ±100 PPM (0.01%).

Raster Mode:
Range from 1mHz to 20 MHz, user selectable.
Resolution 4 digits limited by 1mHz.
Accuracy provided by the selected source.
Internal selection accuracy (VXI CLK10) ±100 PPM (0.01%).

External Input:
TTL input at front panel BNC.
Selectable by programming.
Range from DC to 20 MHz.
Input impedance is 5kΩ, 33pF shunt.
Protected to ±20 Vdc.

VXI Backplane:
Four odd TTLTRG lines (TTLTRG1, 3, 5, 7).
Selectable by programming, one as an output and/or one as an input.
Maximum backplane frequency 12.5 MHz.

Triggers

Internal:
Range from 1mHz to 2MHz.
Output pulse width to backplane is >100ns.
Resolution can be set in 100ns increments.
Accuracy is provided by the VXIbus CLK10.

External Input:
TTL input at front panel BNC.
Maximum Arb trigger frequency is 2MHz.
Minimum required pulse width: 50ns.
Protected to ±20 Vdc.
Slope: Positive.

VXI Backplane:
Four even TTLTRG lines (TTLTRG0, 2, 4, 6).
Selectable by programming, One as an output and/or one as an input.
Maximum backplane frequency 12.5 MHz.
Slope (input/output): Negative.

Programmed:
***TRG** may be used as a trigger.

Trigger to Trace delay:
maximum 1 clock + (<100ns).

Marker Outputs

Sync:
TTL output into 50Ω, synchronous with waveform. Protected against short circuit to ground. Rise and Fall time <20 ns into 50Ω.

ZERO CROSSING DETECTOR.
Sync is a TTL high when waveform is above 2048 (0V).

BEGINNING BITS
Sync is a TTL high for 1 to n clock cycles at first trace memory location in use (mode sensitive width, 50 ns minimum).

Position:
TTL output into 50Ω, short circuit protected.
User definable marker state for each point.
Rise and Fall time <20 ns into 50Ω.

Accuracy
Low level <0.4V into > 10KΩ.
High level > 2.5V and < 4.0V into >10KΩ.
Low level <0.2V into 50Ω.
High level >2.0V and <2.5V into 50Ω.
Rise and fall time <20 ns into 50Ω

Filtering

Programmable insertion, 4MHz, 6 pole, 0.5 dB flatness to 2.5 MHz.

Pre-defined Waveshapes

Sinusoid: One cycle of a sine wave.

Square: One cycle of a square wave.

Triangle: One cycle of a triangle wave.

Positive Ramp: A positive ramp from 1 to 4095.

Negative Ramp: A negative ramp from 4095 to 1.

Positive Haversine:
Two cycles of an inverted cosine, the most negative point is 2048 (0V).

Negative Haversine:
Two cycles of a cosine, the most positive point is 2048 (0V).

Random: Random point values.

DC: The point value 2048, output range ±5V

SINC (sinx/x): A SINC pulse spanning $\pm 16\pi$ radians.

1.3.12 Memory

Standard 32,768 words of volatile RAM.
Optional 131,072 words of volatile RAM.

VXI Interface

VXIbus P1 and P2 connector.
A16/A24/A32 bus master capability.
Full A16/A24/A32 register access.
All A16 registers provided.
Message based, 1K input buffer

Physical

Weight:
<1.6kg (3.4 lb)

Power:
<32W.
+5V at 2.5A peak.
+12V at 0.15A peak.
-12V at 0.15A peak.
+24V at 0.2A peak.
-24V at 0.2A peak.
-5.2V at 0.35A peak.
-2V at 0.1A peak.

Dimensions:
Single slot, "C" size VXI module.

Specifications temperature:
Calibrated at 23° C ±3° C.

Operating Temperature
0°C to +50°C.

Option

01 128K memory.

APPENDIX B
ERROR CODES

Electrical Check Out

The electrical check out is composed of the automatic power up trace memory validation test, the operator initiated Self test, *TST?, and the operation verification procedure. The *TST? must be initiated to verify the pass/fail status of the trace memory test.

Instrument Operation Tests

Two separate tests are required to verify proper operation of the instrument. One test verifies only the trace memory, while the second verifies the remaining Arb circuitry.

The trace memory test erases all data in memory, it is performed only during power-up as part of initialization. The test results (a value between 0 and 65,535) are available to the operator through the TRAC:STAT? query. If the instrument passes, 0 (or 1 if option 01 is installed) is returned. Any number greater than 1 indicates a faulty RAM module, which is not field repairable. If a faulty module is indicated, use the factory address and telephone number located on the title page of this manual to contact the Wavetek Customer Service Department prior to factory shipment. If the unit is under warranty, return the entire instrument to the factory. If the unit is no longer within warranty, the module may be removed and shipped to the factory.

The remaining Arb circuitry is tested by sending *TST?. When the instrument receives this query, all traces and hardware settings are saved and output relays are opened. The circuitry is then tested in the order shown in table B-1, and the results returned. A returned value of 0 indicates all tests passed. Upon a failure, the program will terminate and return the error value (-32767 to +32768). After the indicated problem is corrected, *TST? should again be sent.

By using the information located in Figure B-1 and Table B-1, the operator is able to decode the returned error value into a 16-bit binary number. To decode the returned decimal value, first subtract the highest ERROR WORD BIT WEIGHT possible that does not exceed the number returned and note the BIT RETURNED. From the remainder, again subtract the highest ERROR WORD BIT WEIGHT possible. Note the BIT RETURNED. This process is continued until the remainder is zero. Refer now to Table B-1. Note the "Test Number" and "Error Code" columns. RETURNED BITS 0 through 7 (from Figure B-1) identify Error Codes, and RETURNED BITS 8 through 15 identify Test Numbers. To identify the Test Number, add the TEST NUMBER BIT WEIGHTS that correspond to the Test Number BITS RETURNED to yield the Test Number. More than one Error Code for a Test Number may be asserted.

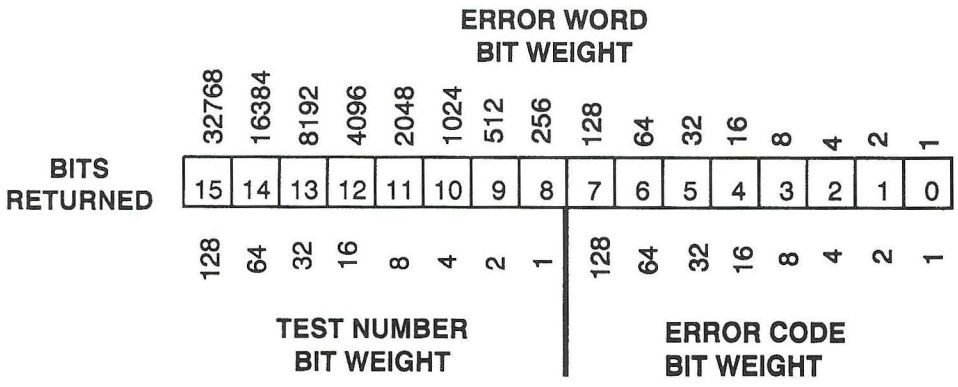


Figure B-1. Self Test Status Word

Table B-1. Self-Test Format

Test Number	Error Code	Circuit Indicated/Parameters		Test Boundaries
1	N/A	Trace Memory		Memory test bit 1
2	1	Diagnostic Interface		0V ±0.02V
3	1	DAC -amplitude reference		–1.0V ±5%
4	1 2	DAC +amplitude reference		2.4V ±20% 0.7V ±20%
5	1 2	Offset		+5.0V ±5% –5.0V ±5%
6	1 2	Pre amplifier		–1.3V ±10% +1.3V ±10%
7	1 2	Power amp (Amplitude)		+8.0V ±10% –8.0V ±10%
	4 8	Power amp (Offset)		+8.0V ±10% –8.0V ±10%
8	2 4 8 16 32	Pre-attenuator:	2:1 Attenuation 4:1 Attenuation 8:1 Attenuation 16:1 Attenuation 32:1 Attenuation	1:1/2 ±30 mV 2:1/2 ±30 mV 4:1/2 ±30 mV 8:1/2 ±30 mV 16:1/2 ±30 mV
9	1	Filter		Vin = Vout ±2%
10	1 2 4 8	Output Attenuator:	10:1 Attenuation 100:1 Attenuation 10:1 Attenuation 100:1 Attenuation	+1:1/10 ±30 mV +10:1/10 ±30 mV –1:1/10 ±30 mV –10:1/10 ±30 mV
11	1 2 4 8 16 32	Marker Position and Sync:	BBIT, 1st bit triggers sync threshold, marker low BBIT, 1st bit set below sync threshold, marker low BBIT, 1st bit triggers sync threshold, marker high BBIT, 1st bit below sync trigger threshold, marker high ZCRO, 1st bit set below zero crossing, marker low ZCRO, 1st bit set above zero crossing, marker low	1.0 < V < 2.5V –0.1 < V < 0.8V 2.0 < V < 5.0V 1.0 < V < 2.5V –0.1 < V < 0.8V 1.0 < V < 2.5V

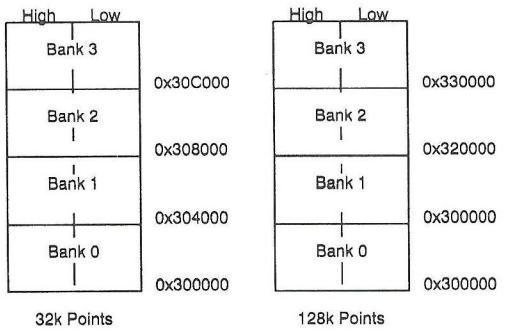
Test 1: Trace Memory

This test checks the integrity of Trace Memory by peforming write/read operations. These operations attempt to locate stuck address and data lines down to the chip level. This test is performed when the instrument is first powered on and when the *RST command is received.

Hardware configuration

The Trace Memory card has eight static RAM chips configured as four pairs of 16-bit wide blocks of memory. The chips are paired such that one chip stores the high byte and the other stores the low byte of a 16-bit word. For the purposes of this test each pair of RAM chips will be refered to as a bank. A

memory map showing the addressing for the 32k point and 128k point Trace Memory cards is shown below. Remember that there are two bytes to each point.

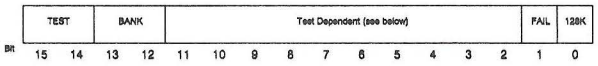


The Trace Memory test is performed in three stages. The first stage determines if each bank can be individually addressed. The second stage looks for struck data lines within each bank and the third stage looks for stuck address lines within each bank. A failure at any stage of the test will cause the test to terminate and an error code to be placed in the AWGStatus variable. This means that only the first fault will be reported in a board with multiple faults.

AWG Status word

When the Trace Memory test fails an error code is placed in the AWGStatus variable. The integer value of AWGStatus can be queried by send the following message to the VXIAWG.

:TRACe:STATus?



AWGStatus

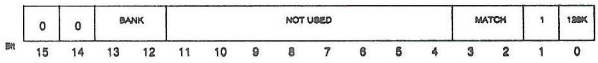
The AWGStatus word contains information regarding the status of the Trace Memory. The meaning of each field is described below.

128K	0	32K point trace memory card installed
	1	128K point trace memory card installed
FAIL	0	Trace Memory test passed
	1	Trace Memory test failed
TEST	00	Trace Memory test failed in sub-test 0
	01	Trace Memory test failed in sub-test 1
	10	Trace Memory test failed in sub-test 2
BANK	00	Failure detected in RAM bank 0
	01	Failure detected in RAM bank 1
	10	Failure detected in RAM bank 2
	11	Failure detected in RAM bank 3

The interpretation of bits 11:2 is dependent on the sub-test in which the failure was detected. Each sub-test is described below.

Sub-test 0

This test checks continuity of the upper order address lines used to generate the select signals for the four banks of RAM chips. If one of these lines is stuck then one or more banks will not be accessible to the CPU. A stuck address line has the effect of making the CPU see the same bank at different addresses. This condition is detected by writing a unique pattern into the base word of each bank. The contents of the word in bank 0 is then compared to the contents of the base word of banks 2, 3 and 4, the contents of the word in bank 2 are compared to 3 and 4, and bank 3 is compared to bank 4. If a match is found then there was a failure. The format of AWGStatus for this test is shown below.



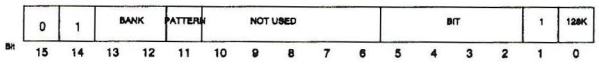
If a failure is detected in this sub-test the code 00 is placed in the TEST field. The BANK field indicates the bank whose base word pattern is being compared. The MATCH field indicate the bank whose base word matches.

When the base words of two banks match then the address line that selects between the banks is stuck. Remember that this test does not indicate where the address line is stuck. The problem may not be on the RAM card.

This test may detect address lines that are shorted together but will not be able to indicate which two are shorted. Test results for problems other than a single stuck address line are undefined.

Sub-test 1

This tests checks for continuity of the data lines to each chip. Starting with bank 0 the pattern 0xAAAA is written to the base word of the bank. The word is then read back and compared to the pattern. If the word does not match the pattern the word is scanned for the first non-matching bit, starting with D0. If the word matches the test is repeated using the pattern 0x5555. This test is repeated for all four banks.



If a failure is detected in this sub-test the code 01 is placed in the TEST field. The bank in which the failure was detected is placed in the BANK field. The PATTERN field is set to 1 if the failure occured when using the 0xAAAA pattern or to 0 if using the 0x5555 pattern. The number of the first bit where the pattern and the contents of the base word failed to match is placed in the BIT field.

Sub-test 2

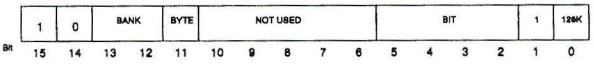
This test checks for continuity of the address lines to each chip. Because the address lines are common to both the upper and lower bytes we need to detect not only which address line has the discontinuity but also whether that address line is connected to the chip containing the high byte or the low byte. This is done by writing a unique pattern into both the upper and lower bytes to selected locations within each bank and then reading each location to see that its contents were not changed.

If an address line is stuck then the same pattern will appear in more than one location. By determining which locations contain the same pattern then address line which is stuck can be identified.

The addresses of the locations are derived by walking a '1' across the address lines of the RAM chips, starting with A0. Thus the addresses are in the sequence:

Bank Base Address + {0x0000, 0x0002, 0x0004, 0x0008, ... }

Since the RAM chips on the 128K card have more address line inputs the test sequence for this card is longer than for the 32K card.



If a failure is detected in this sub-test the code 10 is placed in the TEST field. The bank in which the failure was detected is placed in the BANK field. The BYTE field is set to 1 if the failure occured in the low byte or to 0 if in the high byte. The BIT field contains the number of the address line which was identified as being stuck.

Test 2: Diagnostic Interface

This test verifies the proper functioning of the Analog to Digital Converter, the heart of the self-test hardware. The converter is tested for zero volts output (±0.02V) at zero volts input. If the test fails, the Error Code bit 0 is set high and the Test Number byte is set to 2.

Test 3: DAC -Amplitude Reference

This tests the negative reference voltage at the Waveform Digital to Analog Converter for –1V ± 5%. If this test fails, the Error Code bit 0 is set high and the Test Number byte is set to 3.

Test 4: DAC +Amplitude Reference

The positive reference voltage at the Waveform Digital to Analog Converter ranges from –1.0V to +5.0V. This test checks two points within this range, 0.5V and 2.5V. If the test fails at 2.4V ± 20%, Error Code bit 0 is set high. If the test fails at 0.7V ±20%, Error Code bit 1 is set high. If any part of test 4 fails, the Test Number byte is set to 4.

Test 5: Offset

This test verifies the Offset control voltage end points are –5.0V and +5.0V ± 5%. If the +5V test step fails, Error Code bit 0 is set high. If the –5V test fails, Error Code bit 1 is set high. If any part of test 5 fails, the Test Number byte is set to 5.

Test 6: Preamplifier Output

Tests Waveform DAC and Preamplifier output with filter on. Sets +amplitude reference to maximum and Waveform DAC to maximum and then minimum. Output should be –1.3V and then +1.3V. If the test fails the –1.3V ±5%, Error Code bit 0is set high. If the test fails the+1.3V ±5%, Error Code bit 1is set high. If any part of test 6 fails, the Test Number byte is set to 6.

Test 7: Power Amplifier Output

This test, conducted in two parts, checks the Power Amplifier, Filter relay, and the Pre-attenuator, at the Power Amplifier output. The Filter is turned off. First, with the Pre-attenuator set to 1:1 and Offset set to zero, The Waveform DAC is ranged from +8V to –8V. If the +8V ±5% step fails, the Error Code bit 0 is set high. If the –8V ±5% step fails, the Error Code bit 1 is set high.

Then the Waveform DAC is set to zero amplitude and the Offset voltage is ranged from +8V to –8V. If the +8V ±5% step fails, the Error Code bit 2 is set high. If the –8V ±5% step fails, the Error Code bit 4 is set high. If any part of test 7 fails, the Test Number byte is set to 7.

Test 8: Pre-attenuator

In this test the Waveform DAC is set for +9.5V and Offset is set to zero. The final output is measured with the 5 bit binary Pre-attenuator set for 1:1 (no attenuation). The Pre-attenuator is then set for 2:1

and the output amplitude is measured and compared to half of the previous value. An error of greater than 30 mV sets the Error Code bit 1 high. This process is repeated until all 5 bits of attenuation have been tested, with the Error code bit 5 corresponding to an attenuation of 32:1. If any part of Test 8 fails, the Test Number byte is set to 8.

Test 9: Filter

This test verifies that the Filter has an approximate gain of one and that it does not introduce significant offset. The maximum output voltage is measured with the Filter switched out and then again with the Filter switched in. If the results do not agree within 2%, then the Error Code bit 0 is set high, and the Test Number byte is set to 9.

Test 10: Output Attenuator

This test verifies the 10:1 and 100:1 final attenuators. First a +9V amplitude is measured at 1:1. This value is divided by 10 and compared to the measured voltage with the 10:1 attenuator relay turned on. If these values do not agree within 15%, then Error Code bit 0 is set high. The 10:1 measured value is divided by10 and compared to the voltage measured with the 100:1 relay turned on. If these values do not agree within 15%, then Error Code bit 1 is set high. Then a –9V amplitude is measured at 1:1. This value is divided by 10 and compared to the measured voltage with the 10:1 attenuator relay turned on. If these values do not agree within 15%, then Error Code bit 2 is set high. The 10:1 measured value is divided by10 and compared to the voltage measured with the 100:1 relay turned on. If these values do not agree within 15%, then Error Code bit 4 is set high. If any part of Test 10 fails, the Test Number byte is set to 10.

Test 11. Marker Position and Sync

The Marker Position and Sync signals are summed through a resistive divider at their driver outputs and tested that they are present and that thier amplitudes are approximately correct. This test is completed in six steps.

Step 1: The Marker Position and Sync signals are tested using Beginning Bits. The first trace memory bit is set to trigger the sync threshold. The Marker Position is set low. The test point should be roughly +1.7V. If the voltage is not between +1.0 and +2.5V, then the Error Code bit 0 is set high.

Step 2: The Marker Position and Sync signals are tested using Beginning Bits. The first trace memory bit is set below the sync threshold. The Marker Position is set low. The test point should be roughly 0V. If the voltage is not between –0.1 and +0.8V, then the Error Code bit 1 is set high.

Step 3: The Marker Position and Sync signals are tested using Beginning Bits. The first trace memory bit is set to trigger the sync threshold. The Marker Position is set high. The test point should be roughly +3.4V. If the voltage is not between +2.0 and +5.0V, then the Error Code bit 2 is set high.

Step 4: The Marker Position and Sync signals are tested using Beginning Bits. The first trace memory bit is set below the sync threshold. The Marker Position is set high. The test point should be roughly +1.7V. If the voltage is not between +1.0 and +2.5V, then the Error Code bit 3 is set high.

Step 5: The Marker Position and Sync signals are tested using the Zero Crossing Detector. The first trace memory bit is set below the zero crossing detector threshold. The Marker Position is set low. The test point should be roughly 0V. If the voltage is not between –0.1 and +0.8V, then the Error Code bit 4 is set high.

Step 6: The Marker Position and Sync signals are tested using the Zero Crossing Detector. The first trace memory bit is set above the zero crossing detector threshold. The Marker Position is set low. The test point should be roughly +1.7V. If the voltage is not between +1.0 and +2.5V, then the Error Code bit 5 is set high.

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