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PENT/CPCI-721

Installation Guide

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Using This Manual

This Installation Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), Compact Peripheral Component Interconnect (CPCI), and telecommunications.

Other Sources of Information

For further information on the PENT/CPCI-721 refer to the following documents:

Company	Web Address	Document
Force Computers	www.forcecomputers.com	PENT/IOBP-720 IG (P/N 210615)
		PENT/MEM-720 IG (P/N 208847)
		PENT/CPCI-72x/AccKit IG (P/N 205235)
Hitachi/Micron/Mitsubishi	www.halsp.hitachi.com	EDO DRAM on memory modules, 2Mx8 for 16 and 32 MByte total memory capacity per module (HM51W17805B)
		8Mx8 for 64 and 128 MByte total memory capacity per module (HM5165805A)
Intel	www.developer.intel.com	CPU: Intel Pentium
		BIOS flash: AMD/INtel 512Kx8 (28F400B5T)
		EIDE, PCI-to-ISA bridge, USB: 82371SB
		Ethernet: 21143
		Host-to-PCI bridge: 82439 HX
		PCI-to-PCI bridge: 21150

Company	Web Address	Document
National	www.national.com	Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy, battery-backed NVRAM, RTC: National PC87308 SuperI/O Temperature Sensor: National Semiconductor LM75
NEC Electronics, Inc.	www.necel.com	L2 cache VMC / NEC 32Kx32 (µ PD431232L)
Philips Semiconductor	www.philips.com	The I^2C bus and how to use it (including specifications)
SanDisk	www.sandisk.com	User flash: SanDisk 1.3” Flash Drive (SDIBT)
Texas Instruments	www.ti.com	PCMCIA-PC card: TI-PCI 1131

For further information on the I/O board refer to the following documents:

- Adaptec (www.adaptec.com): Adaptec AIC 7880 SCSI
- Cirrus Logic (www.cirrus.com): Cirrus Logic CL-GD 5446 SVGA
- Intel (www.developer.intel.com): Intel 21150 PCI-to-PCI bridge

Conventions

Notation	Description
	All numbers are decimal numbers except when used with the following notations:
0000.0000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
0000_2	Same for binary numbers (digits are 0 and 1)
Bold	Character format used to emphasize a word
`Courier`	Character format used for on-screen output
`Courier+Bold`	Character format used to characterize user input and to separate it from system output
Italics	Character format for references and for table and figure descriptions.

Notation	Description
<text>	Typical notation used for variables and keys.
Note:	No danger encountered. Pay attention to important information marked using this layout.
Caution 	Possibly dangerous situation: slight injuries to people or damage to objects possible
Danger 	Dangerous situation: injuries to people or severe damage to objects possible

Revision History

Ord. No.	Revision	Date	Description
209172	1.0	April 1997	First print with SAP number 209172
210275	2.0	October 1998	Changed SAP number, changed front-panel design, added register descriptions
210275	3.0	October 1998	Description of IOBP-CPU720 moved to section 2.8.1 Base-720 CompactPCI Interface, extended Installation Prerequisites and Requirements, corrected description of the Base Board LED Control Register
210275	4.0	May 1999	Changed name of HD-AccKit, P1 connector removed from IOBP-IO720, corrected block diagram
210275	5.0	July 1999	3.3V feature removed, editorial changes
210275	6.0	December 1999	Changed base-721 settings, editorial changes
213235	AA	August 2000	Changed SAP number, editorial changes, added VGA-IO720-4 option (see the “SVGA-AccKit” section on page 2-18)
213235	AB	October 2000	Editorial changes
213235	AC	August 2001	Added the “Sicherheitshinweise” section on page -xxiii; updated the the “Standard Compliance” section on page 1-10



Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PENT/CPCI-721. For your protection, follow all warnings and instructions found in the following text.
This Installation Guide provides the necessary information to install and handle the PENT/CPCI-721. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The PENT/CPCI-721 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, uninstall or maintain the PENT/CPCI-721. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A.

These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

The board generates, uses and can radiate radio frequency energy and, if not installed properly and used in accordance with this Installation Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If boards are integrated into open systems, always cover empty slots.

To ensure proper EMC shielding, always operate the PENT/CPCI-721 with the blind panels or with PMC modules installed.



Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing or uninstalling the board, check the "Requirements" section on page 2-3.**
- **Before touching integrated circuits, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the CompactPCI backplane via all assembled connectors and that power is available on all power pins.**
- **Never operate the PENT/CPCI-721 without I/O board.**

Operation

While operating the board ensure that the environmental and power requirements are met.

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the CompactPCI rack and shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Expansion

Check the total power consumption of all components installed (see the technical specification of the respective components).

Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Only replace components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMI and the possibly changed functionality of the product.



RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted pair Ethernet (TPE) connectors. Mismatching the two connectors may destroy your telephone as well as your PENT/CPCI-721. Therefore:

- **TPE connectors near your working area have to be clearly marked as network connectors.**
- **TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The length of the electric cable connected to a TPE bushing must not exceed 100 meter.**

Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**
- **Exchange the battery before five years of actual use have elapsed.**
- **Exchanging the battery always results in a loss of data. Therefore, back up affected data before exchanging the battery.**
- **When installing the new battery, ensure that the '+' on top of the battery stays at the top and therefore is visible when viewing the board from its component side.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation.

CompactPCI

The PENT/CPCI-721 is a system slot board, i.e. it always has to be operated in the system slot of the CompactPCI rack. The I/O-721 is a peripheral slot board, i.e. it always has to be plugged into peripheral slots of the CompactPCI rack. Otherwise the boards and other cards in the system may be damaged.



IOBP-IO720

IOBP-IO720 is especially designed for the I/O board variants of the PENT/CPCI-72x. Do not use any other I/O panels with the I/O-721.

Never connect SCSI devices to both the 16-bit and the 8-bit SCSI connectors onboard the IOBP-IO720. Decide whether you want to use 16-bit or 8-bit SCSI.

Never connect devices to both connectors onboard the IOBP-IO720 which carry the PMC user I/O signals. Decide whether you want to use the full or only the partial range of PMC 2 user I/O signals.

IOBP-CPU720

The IOBP-CPU720 is especially designed for the CPCI-board variants of the PENT/CPCI-72x. Do not use any other I/O panels on the PENT/CPCI-72x.

PMC Slots

The total maximum power consumption per PMC slot at +/-12V, 5V, and 3.3V level must not exceed 7.5W (total over-all used voltages).

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, welche bei der Installation, dem Betrieb und der Wartung des PENT/CPCI-721 zu beachten sind. Beachten Sie zu Ihrem Schutz alle folgenden Warnhinweise und Anleitungen.

Dieses Installationshandbuch enthält alle notwendigen Informationen zur Installation und zum Betrieb des PENT/CPCI-721. Da es sich um ein komplexes Produkt mit einer aufwendigen Bedienung handelt, kann keine Garantie dafür übernommen werden, dass die enthaltenen Informationen vollständig sind. Für weitere Informationen wenden Sie sich bitte an Ihren Vertreter der Firma Force Computers.

Das PENT/CPCI-721 erfüllt die gültigen industriellen Sicherheitsanforderungen. Dieses Produkt darf ausschließlich für Anwendungen innerhalb der Telekommunikationsindustrie und der industriellen Steuerung verwendet werden.

Lediglich von Force Computers eingewiesene oder im Bereich Elektrotechnik oder Elektronik qualifizierte Personen sind zur Installation, zum Betrieb und zur Wartung dieses Produktes befugt. Die in dieser Dokumentation enthaltenen Informationen sollen lediglich als Hilfestellung für entsprechend qualifiziertes Fachpersonal dienen. Keinesfalls kann es dieses ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet und entspricht den Grenzen eines Klasse-A-Produktes gemäß Abschnitt 15 der FCC-Richtlinien, insbesondere EN 55022 Klasse A.

Diese Grenzen sind dafür vorgesehen, einen vernünftigen Schutz gegen störende Einflüsse bei einem Betrieb in einer kommerziellen Umgebung zu gewährleisten.

Das Board erzeugt elektromagnetische Strahlung. Wird das System unsachgemäß installiert oder in anderer Weise als in diesem Installationshandbuch beschrieben betrieben, kann es in der Umgebung von Rundfunksendern und in Wohngegenden zu Störungen kommen. In diesem Fall ist der Benutzer verpflichtet, entstehende Störungen auf seine Kosten beheben zu lassen und die Kosten von Messungen selbst zu tragen.



Werden Boards in offene Systeme eingebaut, müssen freie Steckplätze mit einer Blende abgeschirmt werden.

Um eine ausreichende Abschirmung zu gewährleisten, darf das Board nur mit einer Blindblende oder mit einer installierten PCMCIA-Karte betrieben werden.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Lesen Sie vor Einbau oder Ausbau des Boards den Abschnitt “Action Plan” auf Seite...**
- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie beim Einbau oder Ausbau des Boards nicht auf das Front Panel, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Einbau oder Ausbau von zusätzlichen Geräten oder Modulen das jeweilige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die CompactPCI Backplane angeschlossen ist und Strom an allen Power Pins anliegt.**
- **Betreiben Sie das PENT/CPCI-721 niemals ohne I/O Board.**

Betrieb

Während des Betriebs müssen die Umgebungs- und die Stromsversorgungsbedingungen gewährleistet sein.

Wenn das Board in Gebieten mit starker elektromagnetischer Strahlung betrieben wird, stellen Sie sicher, dass das Board auf dem Compact PCI Rack verschraubt ist und mit einem Gehäuse geschützt ist.

Es ist sicherzustellen, dass Anschlüsse und Kabel des Boards während des Betriebs nicht versehentlich berührt werden können.



Erweiterung

Beachten Sie den Gesamtstromverbrauch aller installierter Komponenten (siehe technische Daten der entsprechenden Komponente).

Vergewissern Sie sich, daß jeder individuelle Ausgangsstrom jedes Stromverbrauchers innerhalb der zulässigen Grenzwerte liegt (siehe technische Daten des entsprechenden Verbrauchers).

Benutzen Sie bei der Erweiterung ausschließlich von Force Computers empfohlene Komponenten und Systemteile. Ansonsten sind Sie für die Auswirkungen auf EMV und die möglicherweise geänderte Funktionalität des Produktes verantwortlich.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:

- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**

Batterie

Muss eine Lithium Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**
- **Tauschen Sie die Batterie aus, bevor die fünf Jahre tatsächlicher Betriebsdauer verstrichen sind.**



- **Ein Batteriewechsel führt immer zu einem Datenverlust. Sichern Sie deshalb vor dem Austausch die betroffenen Daten.**
- **Vergewissern Sie sich beim Einbau der neuen Batterie, dass das '+' auf der Batterie oben und daher sichtbar bleibt, wenn das Board von der Komponentenseite betrachtet wird.**

Umweltschutz

Alte Batterien und/oder Boards oder Systeme müssen stets gemäß der in Ihrem Land gültigen Gesetzgebung entsorgt werden.

CompactPCI

Das PENT/CPCI-721 ist ein System Slot Board, d.h. es muss in einem CompactPCI Rack in einem System Steckplatz betrieben werden. Das I/O-721 ist ein Periphärie-Slot Board, d.h., es darf nicht als System Slot Board betrieben werden. Andernfalls könnte das Board oder andere Karten in dem System beschädigt werden.

IOBP-IO720

Das IOBP-IO720 wurde speziell für die I/O Board-Varianten des PENT/CPCI-721 entwickelt. Verwenden Sie keine anderen IOBPs zusammen mit dem I/O-721.

Verbinden Sie niemals SCSI-Bausteine mit dem 16-bit und dem 8-bit SCSI-Steckern auf dem IOBP-IO720. Entscheiden Sie sich, ob Sie den 16-bit oder 8-bit SCSI verwenden wollen.

Verbinden Sie niemals Bausteine mit beiden Steckern auf dem IOBP-IO720, die die PMC-User I/O Signale leiten. Entscheiden Sie sich, ob Sie die volle oder die partielle Bandbreite der PMC2-User I/O Signal benötigen.

IOBP-CPU720

Das IOBP-CPU720 ist speziell für die CPU Board-Varianten des PENT/CPCI-721 entwickelt worden. Verwenden Sie keine anderen IOBPs zusammen mit dem CPU-Board CPCI-721.



PMC Steckplätze

Der Gesamtstromverbrauch pro PMC-Steckplatz bei +/-12V, 5V und 3,3V darf nicht 7,5W übersteigen (Gesamtspannung).



1

Introduction

Features

The PENT/CPCI-721 familly is a variant of the PENT/CPCI-72x family group consisting of the PENT/CPCI-721 and the I/O-721. It is a CompactPCI system slot board and can be expanded via an I/O board, the I/O-721. The PENT/CPCI-721 provides the base board functions necessary to obtain an operational CPU board. The PENT/CPCI-721 has to be installed in the system slot of a CompactPCI system which is marked by a triangle. Its main features are described in the following subsection.

CPU

The PENT/CPCI-721 offers a mobile module based on a Pentium II processor with 133, 166, 200, 233 MHz speed or higher with 512 KByte L2 cache. Furthermore, the PENT/CPCI-721 features an 8254 compatible 3-channel-timer.

Memory

Memory features include:

- 512 KByte flash BIOS, 8-bit wide
- Burst SRAM as L2 cache
- EDO DRAM (60 ns) with ECC support implemented on lower and upper memory modules
- Motorola 146818 compatible real time clock and CMOS RAM for storing factory settings, both RTC and RAM with battery backup

Interfaces

Both the PENT/CPCI-721 and the I/O-721 provide several interfaces which are described in the following subsections.

PENT/CPCI-721

The interfaces include:

- 10/100 BaseT Ethernet, routable to a front panel or CompactPCI connector via switch-selection
- One parallel interface LPT, IEEE 1284 compatible and with ECP and EPP (1.7/1.9) support (Extended Capabilities Port), available on CompactPCI connector only for the PENT/CPCI-721
- PS/2 keyboard and mouse controller, 8042 compatible, available on front panel and CompactPCI connector
- Two RS-232 serial interfaces COM1 and COM2 via 16550 compatible chip with 115 KBaud maximum data rate and 16 Byte deep FIFO
  - COM1 available on front panel and CompactPCI connector
  - COM2 available on CompactPCI connector
- Two USB interfaces, one available on front panel connector, the other on CompactPCI connector

I/O-721

The I/O-721 is a CompactPCI peripheral board and its interfaces include:

- SCSI interface with 16-bit Fast-SCSI-2 support, programmable active SCSI termination, available on CompactPCI connector
- VGA controller providing an SVGA interface available on front panel and CompactPCI connector. The I/O front panel features include:
  - 1024x768 resolution and 16 colors
  - 800x600 resolution and 256 colors
  - 640x480 resolution and 256 colors

Additional front panel features include an LED for signaling accesses to devices connected via SCSI and one user LED.

Functions

The functions of the PENT/CPCI-721 include:

- ESD protection for all front panel I/Os, switches and LEDs
- Floppy controller, compatible with PC8477 which contains a super-set of NECuPD72065B and N82077, accessible via CompactPCI connector in case of PENT/CPCI-721. The on-board connector supports one drive. Two drives can be connected via the CompactPCI connector.
- IDE controller with primary and secondary EIDE support, the primary IDE interfaces accessible via CompactPCI connector for the PENT/CPCI-721, the secondary via CompactPCI connector only for the PENT/CPCI-721 and the PENT/CPCI-720/2/3. 2.5" IDE devices are intended to be used with the on-board connectors and 3.5" IDE devices via CompactPCI.
- Inrush current protection for basic hot swap support
- One PMC slot, supporting front panel I/O and one supporting I/O via CompactPCI connector
- Support for Hot Swap on the CompactPCI bus via ENUM#
- Two 82C37A compatible DMA controllers on the PCI-to-ISA bridge
- Two 82C29 compatible interrupt controllers on the PCI-to-ISA bridge

Block Diagram

The block diagram gives an overview on how the PENT/CPCI-721 devices work together and which data paths they use.

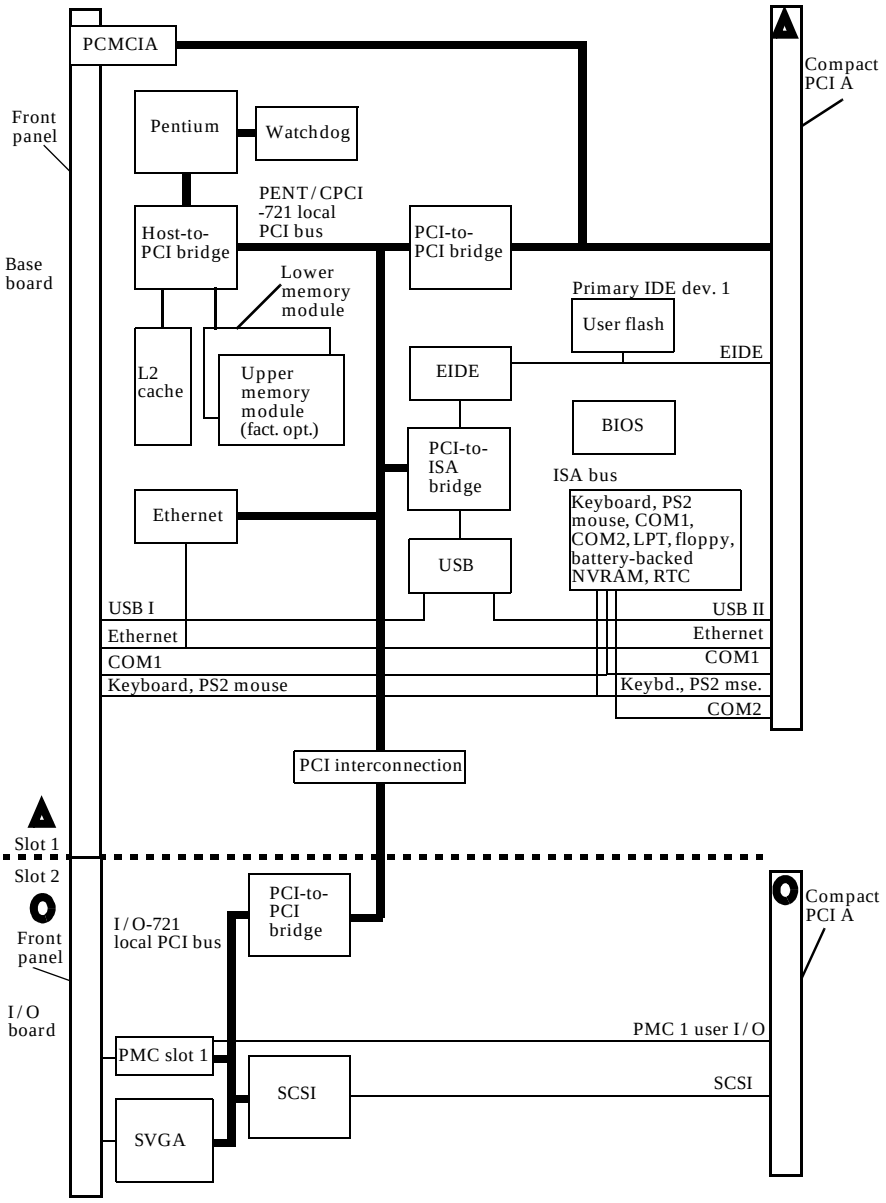


Figure 1: PENT/CPCI-721(Slot 1) and I/O-721 (Slot 2) Block Diagram

Board Expansions

The PENT/CPCI-721 is a 6U CompactPCI board based on an Intel Pentium CPU and consists of the Base-721 and I/O-721. It is two CompactPCI-slots wide and operates at 33 MHz PCI bus frequency.

The PENT/CPCI-721 is designed to run with Windows NT Version 4.0.

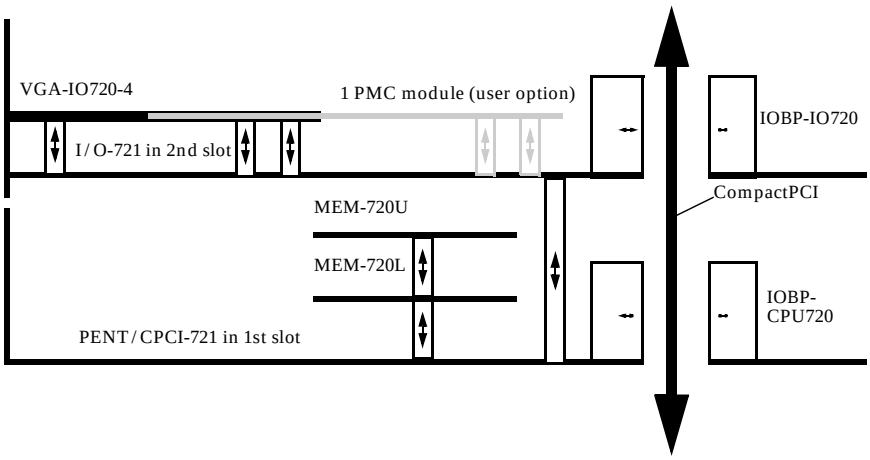


Figure 2: PENT/CPCI-721 with I/O-721

PENT/CPCI-721

The PENT/CPCI-721 provides several expansions which will be described in the following subsection. The PENT/CPCI-721 provides a one-slot front panel and has no carrier board. Therefore there are no Base-721 factory options for floppy drive or hard-disk drive and the LPT1 port is not available on the front panel.

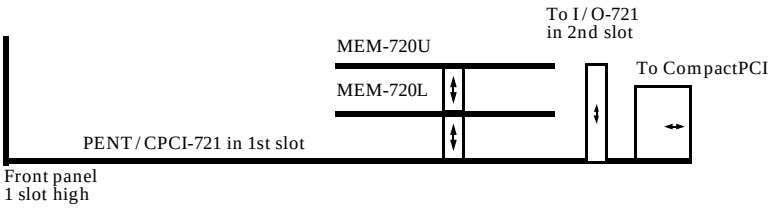


Figure 3: PENT/CPCI-721

Memory

The MEM-720L (lower memory module) is directly connected to the PENT/CPCI-721 whereas the MEM-720U (upper memory module) is connected to the MEM-720L. At least the lower memory module is required.

I/O-721

The I/O-721 extends the functionality of the PENT/CPCI-721. Therefore, it is optional in most cases and provides the flexibility to adjust the PENT/CPCI-721 CPU board solution according to your application´s needs. The I/O-721 is a peripheral board and has to be installed in a peripheral slot of the same CompactPCI backplane as used for the PENT/CPCI-721. Peripheral boards are always marked by a circle.

Note: Due to the CPU's heat sink an I/O board is required for operation of the Base-721.

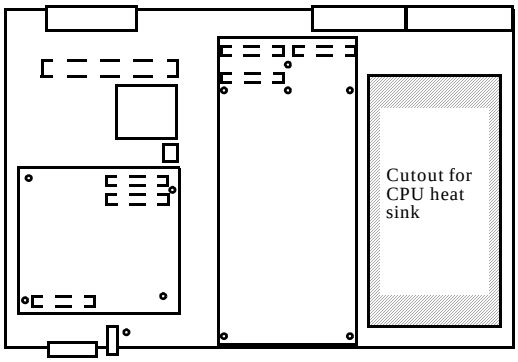


Figure 4: Top View of an I/O-721

The I/O-721 only provides one PMC slot thereby allowing for the CPU´s heat sink and a 2-slot-total design.The I/O-721 features one PMC slot with user I/O routing via the PMC connectors and one VGA board VGA-IO720-4 as a factory option.

IOBP

One rear panel I/O board provides easy access to the signal of the IOBP-CPU720. It is contained in the respective accessory kit (see the“IOBP-CPU720” section on page 2-11).

The IOBP-CPU720 rear panel I/O board allows the connection to the user I/O signals of the base board’s J5 connector via standard connectors and is available for all PENT/CPCI-721 variants.

Standard Compliance

The PENT/CPCI-721 meets the following standard compliance:

Table 1: *Standard Compliance*

Standard	Description
EN 60950 UL/cUL 1950 (pre-defined Force system)	Legal Safety Requirements
FCC Part 15 Class A VCCI Class A EN 55022 Class A EN 55024	EMC requierements on system level

Delivery Information

The following information is helpful when ordering PENT/CPCI-721 board variants as well as upgrades and accessories.

Product Nomenclature

Table 2: *Nomenclature*

PENT/CPCI-721/ddd-ppp-lccc-u	
ddd	DRAM size in MByte
ppp	Processor clock frequency in MHz
Lccc	L2 cache capacity in KByte
u	MByte user flash

Ordering Information

The upgrades and accessories available depend on the variant of the PENT/CPCI-721 under consideration. Consult you local sales representative to confirm availability of specific combinations.

Table 3: *Ordering Information Excerpt*

Ordering No.	**PENT/CPCI-721**	**Description**
105784	.../64-233-L512-0	PENT/CPCI-721 with I/O-721
105233	PENT/MEM-720L/lll	lll = 16 MB lower memory module
104952	PENT/MEM-720L/lll	lll = 32 MB lower memory module
104953	PENT/MEM-720L/lll	lll = 64 MB lower memory module
104993	PENT/MEM-720U/uuu	uuu = 128 MB upper memory module
Accessories PENT/CPCI-721 for the PENT/CPCI-72x family group		
104968	.../CPUP5-AccKit	Rear I/O panel for the PENT/CPCI-721 and related installation components
104960	.../IOP5-AccKit	Rear I/O panel for I/O-721 and related installation components

Table 3: *Ordering Information Excerpt (cont.)*

Ordering No.	PENT/CPCI-721	Description
104985	… / Flash-AccKit / *z*MB	User flash implemented via flash disk with EIDE interface and related installation components; e.g. … / Flash-AccKit / 4MB = flash type "SDIB-4 / SDIBI-4" providing 4 MByte (123 cylinders, 2 heads, 32 sectors / track) using standard transfer mode and without LBA mode control
105119	… / SVGA-AccKit / *cccc*MB	VGA graphics card with video RAM and related installation components for I / O-721; e.g. … / SVGA-AccKit / 2MB = 2 MByte video RAM
Software Accessories PENT/CPCI-721 for the PENT/CPCI-72x family group		
105583	… / BIOS-UpKit	BIOS upgrade utilities
105582	… / NTDrv	Windows NT PCMCIA driver
	… / NT-Support-Package	Windows NT drivers

2

Installation

Requirements

The PENT/CPCI-721 fulfills the standard Force Computers reliability requirements for board products.

The PENT/CPCI-721 is a CompactPCI system slot board, i.e. it provides the clock driver and the arbiter for up to seven peripheral slots. The PCI bus, a high speed local bus, connects different high speed I/O cards with the PENT/CPCI-721. The PCI bus supports 32-bit data bus width with a frequency of 33 MHz.

Environmental Requirements

The environmental values must be tested and proven in the used system configuration. These conditions refer to the surroundings of the board within the user environment.

Note: Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature. To ensure that the operating conditions are met, forced air cooling is required within the chassis environment.

Table 4: *Environmental Requirements*

Feature	Operating	Non-Operating
Temperature[1)]	0°C to +55°C	–40°C to +85°C
Forced Air Flow (in LFM = Linear Feet per Minute)	Depending on processor type: 40 LFM in case of 166 MHz, 200 MHz, or 233 MHz CPU 100 LFM in case of 133 MHz CPU	-
Temp. Change	+/– 0.5°C/min	+/– 1°C/min
Rel. Humidity	5% to 95% non-condensing at +40°C	5% to 95% non-condensing at +40°C
Altitude	-300 m to +3,000 m	-300 m to + 13,000 m

1. For information on the allowed hard disk operating temperature, consult the Installation Guide of the PENT/CPCI-720/HD-AccKit

Caution



If the standard PENT/CPCI-720/HD-AccKit is installed, the operation temperature of the PENT/CPCI-721 is limited by the maximum operation temperature of the hard disk. If the maximum temperature of the hard disk is lower than the maximum temperature of the PENT/CPCI-721, the maximum temperature specified for the hard disk must not be exceeded.

Power Requirements

The PENT/CPCI-721 power requirements depend on the PMC modules and PC cards installed. 3.3V power pins from the CompactPCI backplane are not used. The PENT/CPCI-721 has the following 5V power requirements.

Table 5: *Power Requirements*

PENT/CPCI-721 [1)]	+5V power requirements
PENT/CPCI-721/64-133-L512-0	3.5A
PENT/CPCI-721/64-166-L512-0	4.5A
PENT/CPCI-721/64-200-L512-0	5.5A
PENT/CPCI-721/64-233-L512-0	5.7A

1. if no other boards are installed

Location Overview

The following section shows the diagrams of important board components.

PENT/CPCI-721

The figure below shows the location of important components of the PENT/CPCI-721.

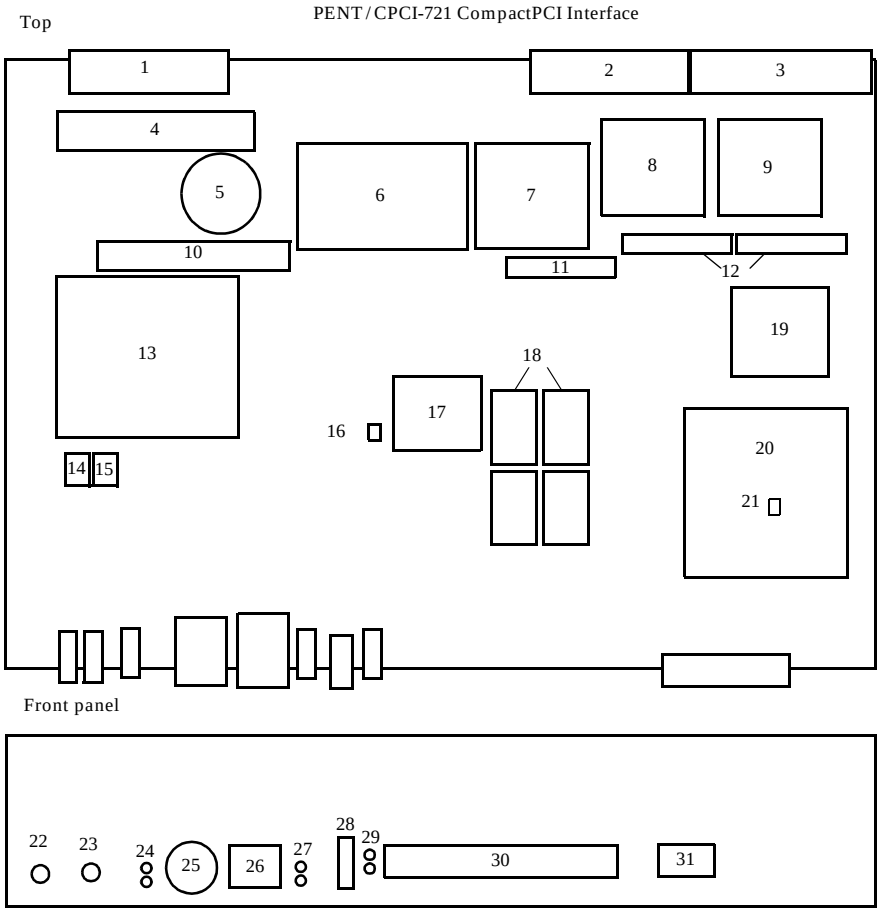


Figure 5: *Location Diagram of the PENT/CPCI-721*

Table 6: *List of Important Components of the PENT/CPCI-721*

No.	Feature	No.	Feature
1	J5	17	Ethernet
2	J2	18	L2 cache
3	J1	19	Host-to-PCI bridge
4	PCI interconnection	20	CPU
5	Battery	21	Temp. sensor 0 below CPU
6	Super I/O: Keyboard, mouse, COMx, LPT, floppy, battery-backed NVRAM, RTC	22	Reset key
7	PCI-to-ISA bridge, USB, EIDE	23	Abort key
8	PCMCIA	24	LEDs
9	PCI-to-PCI bridge	25	Keyboard / Mouse
10	IDE (primary device)	26	ETH
11	Floppy (FD)	27	LEDs
12	Memory modules	28	USB
13	User flash (primary IDE device)	29	LEDs
14	SW0300	30	PCMCIA
15	SW0100	31	COM1
16	Temp. sensor 1		

I/O-721

The figure below shows the location of important components of the I/O-721.

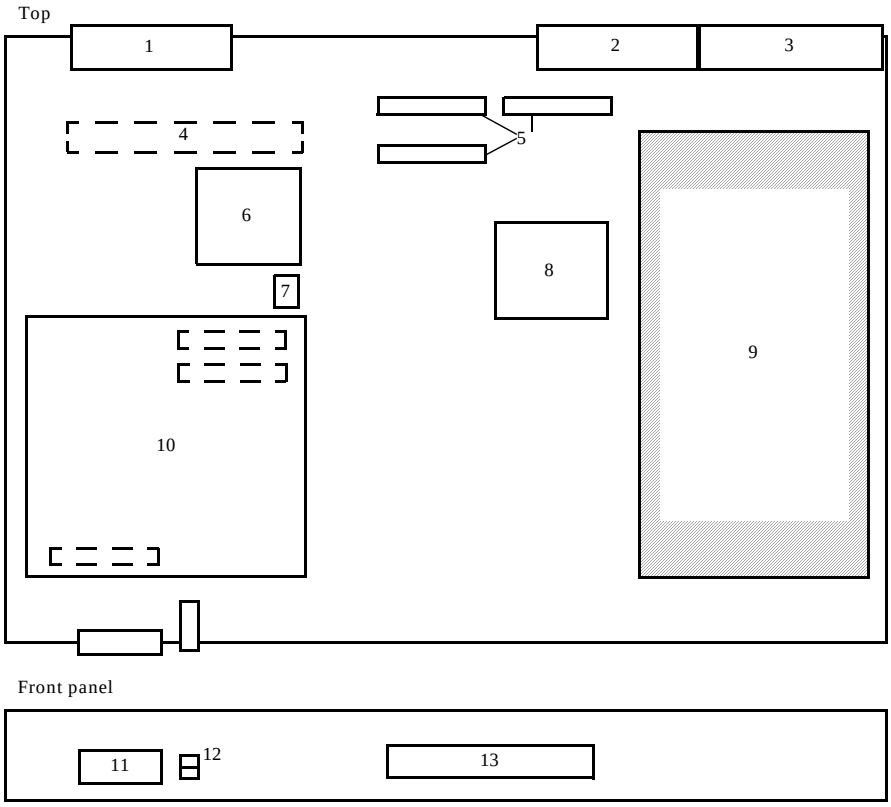


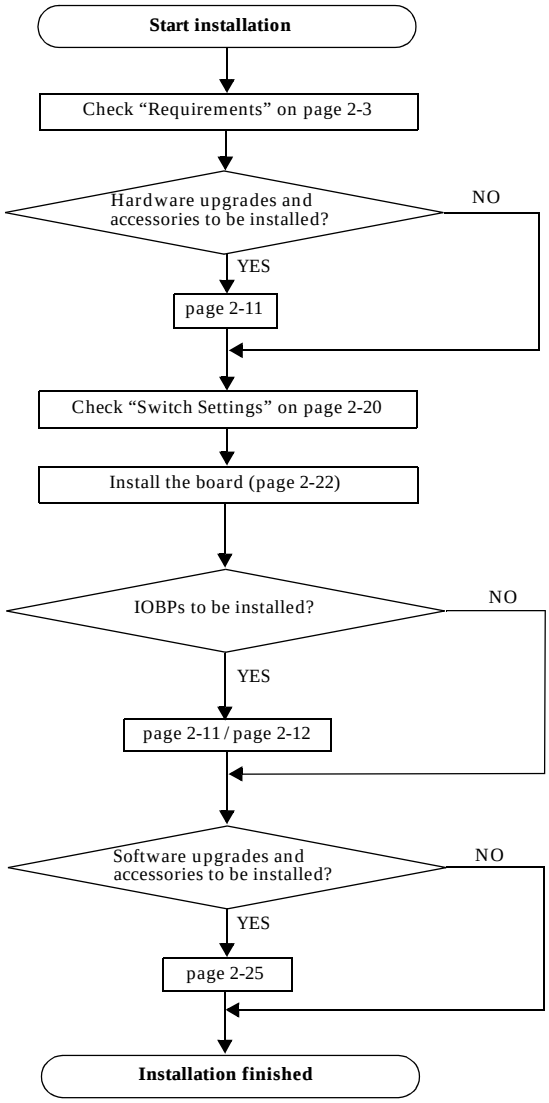
Figure 6: *Location Diagram of the I/O-721*

Table 7: *List of Important Components of the I/O-721*

No.	Feature	No.	Feature
1	J5	8	PCI-to-PCI bridge (to local PCI)
2	J2	9	Cutout for CPU heat sink on PENT/CPCI-721
3	J1	10	VGA-IO720-4 (factory option)
4	I/O-721	11	VGA
5	PMC slot 1	12	LEDs
6	SCSI	13	PMC 1
7	SW0900		

Action Plan

The following action plan gives you an overview of the steps you have to follow while installing the board.



Hardware Upgrades and Accessories

Apart from the extensions which are possible via the CompactPCI system, the PENT/CPCI-72x itself allows for an easy and cost-efficient way of adapting the board to the application's needs.

Memory Modules

The memory configuration is adjustable to the application's needs via selection of the appropriate memory modules:

- MEM-720L: Lower memory modules with 16, 32, 64, and 128 MByte are available.
- MEM-720U: An additional upper memory module allows to increase the memory capacity by 128 MByte.

Out of the extensive list of possible configurations, the following memory configurations have been qualified (others may be tested and qualified on request):

Table 8: *Memory Modules*

Total Capacity	16	32	64	128	256
MEM-720L Cap.	16	32	64	128	128
MEM-720U Cap.	-	-	-	-	128

At least the lower memory module is always required. For installation information see the respective Installation Guide delivered together with the memory module.

IOBP-CPU720

As a separate price list item an I/O panel is available for the PENT/CPCI-721, the IOBP-CPU720. The corresponding PENT/CPCI-720/CPUP5-AccKit contains the following cables in addition to the I/O panel itself:

- One 34-pin floppy cable
- Two 40-pin IDE cables

Two IDE devices can be connected externally to the secondary IDE port via the CompactPCI connector J5 in combination with the IOBP-CPU720.

Note: The IOBP-CPU720 is especially designed for the base board variants of the PENT/CPCI-72x. Do not use any other I/O panel on the Base-720.

IOBP-IO720

Force Computers offers an IOBP-IO720 panel which is plugged into the CompactPCI backplane from its rear. The panel enables easy connection to the I/O signals of an I/O board which are available on the I/O board's J5 connector.

Caution



- **The IOBP-IO720 is especially designed for the I/O board variants of the PENT/CPCI-72x. Do not use any other I/O panels on the I/O-721.**
- **Never connect SCSI devices to both SCSI connectors on board the IOBP-IO720. Decide whether you want to use 16-bit or 8-bit SCSI.**
- **Never connect devices to both connectors on board the IOBP-IO720 which carry the PMC user I/O signals. Decide whether you want to use the full or only the partial range of PMC 2 user I/O signals.**

The I/O panel includes an on-board flat cable and industry standard connector for the PMC user I/O signals and for the SCSI signals.

PMC Module

The I/O-721 provides one PMC slot. If the I/O-721 is shipped without the modules installed, the front panel cutouts are covered by blind panels to ensure proper EMC shielding.

Note:

- **To ensure proper EMC shielding, always operate a PENT/CPCI-721 with the blind panels for the PENT/CPCI-721 front panel or with the modules installed.**
- **If the PENT/CPCI-721 is upgraded, ensure that the blind panels are stored in a safe place to be used again when removing the upgrades.**

The PMC slot supports 32-bit data bus width with a maximum frequency of 33 MHz. A power supply of +/- 12V is available at the PMC slots.

Voltage Keys

The PCI bus uses a 5V voltage signal level on the PMC slots. The voltage keys prevent 3.3V PMC cards from being plugged into the PMC slots.

Connector Configuration

The 32-bit PCI bus requires two PMC connectors. The third PMC connector connects additional user I/O signals of the PMC slot with the I/O-721 CompactPCI J5 connector. The CPU board provides a limited current at the PMC supply pins.

Note: On the I/O-721, the PMC slot 1 provides three PMC connectors (see Figure 7 “Mounting Points 2M1, ..., 2M5 of PMC Module on the I/O-721” on page 2-14).

The different PMC slot numbering also results in a different pinout for the I/O board’s CompactPCI connector and for the PMC user I/O connectors provided on the IOBP-IO720.

Caution



The total maximum power consumption per PMC slot at +/-12V, 5V and 3.3V level must not exceed 7.5W (total over all used voltages).

Installation Procedure

In order to install a PMC module on PMC slot 1, proceed as follows:

1. Remove memory module from PMC slot 1, if necessary

2. Remove blind panel of PMC slot from front panel
3. Store blind panel in a safe place
4. Plug PMC module into connectors of PMC slot (PN11 or PN12) so that standoffs of module fit on the mounting holes of the PENT/CPCI-721 (see figure below)

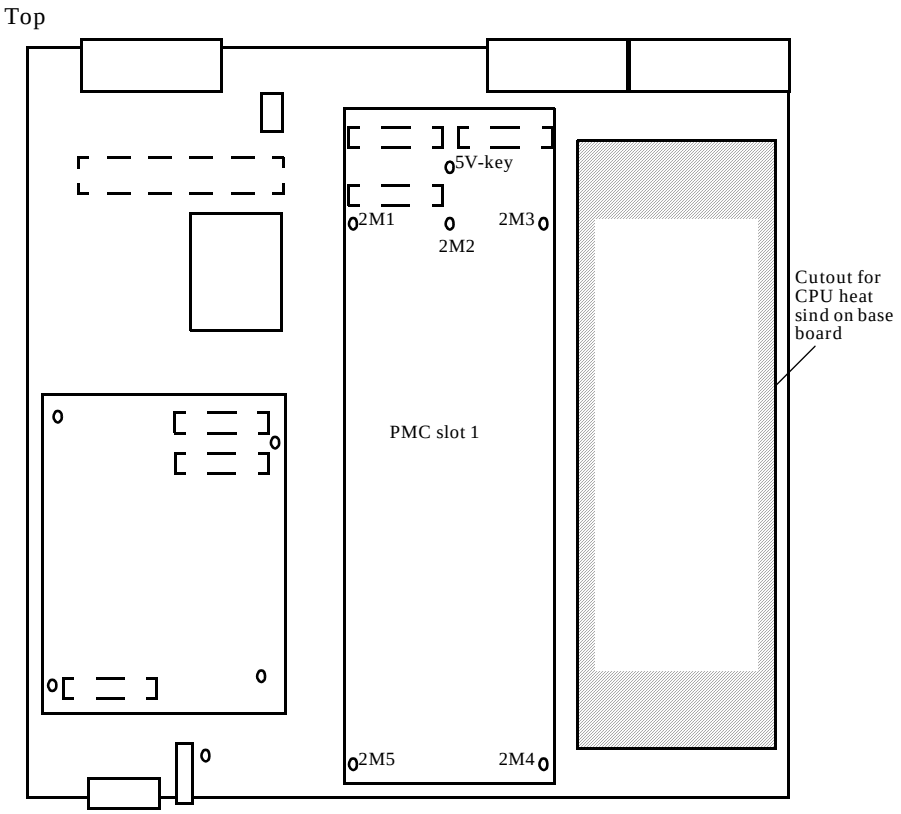


Figure 7: *Mounting Points 2M1, ..., 2M5 of PMC Module on the I/O-721*

Removal Procedure

In order to remove a PMC module from PMC slot 1, proceed as follows:

1. Remove screws S1-4
2. Disconnect PMC module carefully from slot
3. Close front panel gap at free slot with EMC filler

Flash-AccKit

In order to install the user flash accessory kit on the PENT/CPCI-721, proceed as follows:

1. Fasten two standoffs onto flash disk using two of the screws delivered together with accessory kit (see locations marked as 1 and 2 in figure below)

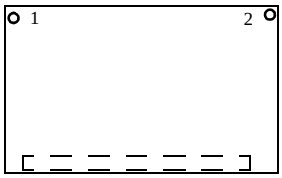


Figure 8: *Mounting Points on the Flash Disk*

2. Plug flash disk onto PENT/CPCI-721 flash disk connector (see ❶ in the figure below)

Note: Verify that all pins are connected.

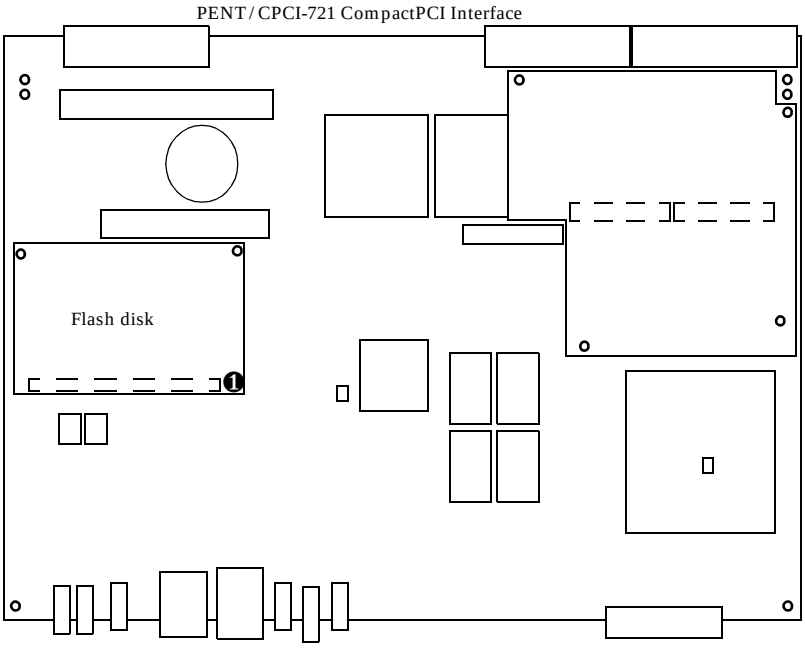


Figure 9: *Flash Disk Connector on the PENT/CPCI-721*

3. Fasten flash disk onto PENT/CPCI-721 with the two remaining screws delivered together with accessory kit (see the locations marked as 1 and 2 in the figure below)

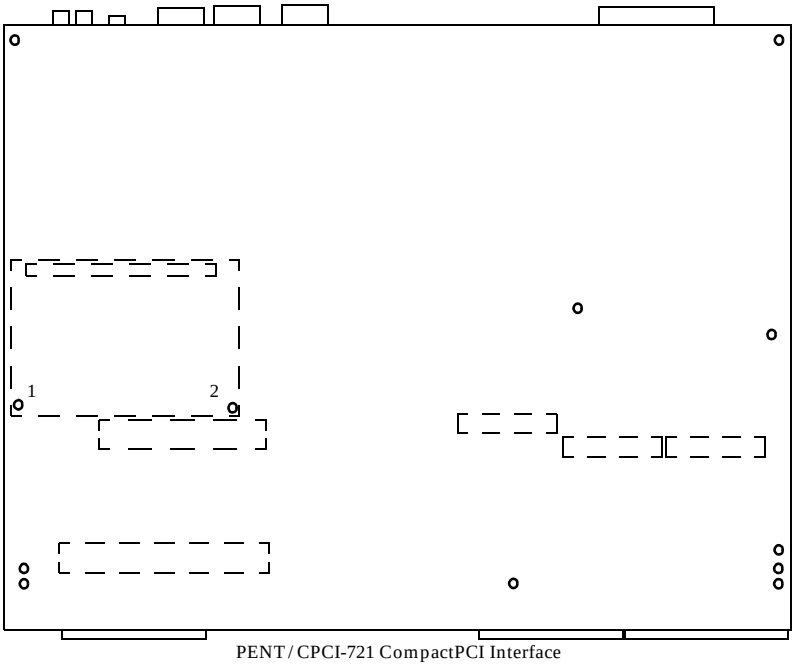


Figure 10: *Mounting Points of the Flash on the Bottom of the PENT/CPCI-721*

4. Check IDE mode configuration for all installed IDE drives (see "PENT/CPCI-721 Switch Settings" on page 2-20) and set SW0100A appropriately. For further information see the "IDE Devices" section on page 2-19

After the hardware installation is completed and the PENT/CPCI-721 is installed in the CompactPCI rack, proceed as follows:

1. Enter BIOS Setup and select correct flash type (see the "Boot Configuration in Setup" section on page 4-5).
2. Enter flash type manually (coded in product name, see Table 3 "Ordering Information Excerpt" on page 1-11)
3. Prepare flash disk which has to be partitioned and formatted for the operating system you use

SVGA-AccKit

1. Uninstall I/O board
   (see the “Removing the I/O-721 from the PENT/CPCI-721” section on page 2-23)
2. Plug VGA-IO720-4 onto respective I/O board connectors
   (see Figure 6 “Location Diagram of the I/O-721” on page 2-8)
3. Fasten VGA-IO720-4 onto I/O board with four screws delivered together with accessory kit
   (see locations marked as V1, V2, V3, and V4 in figure below)

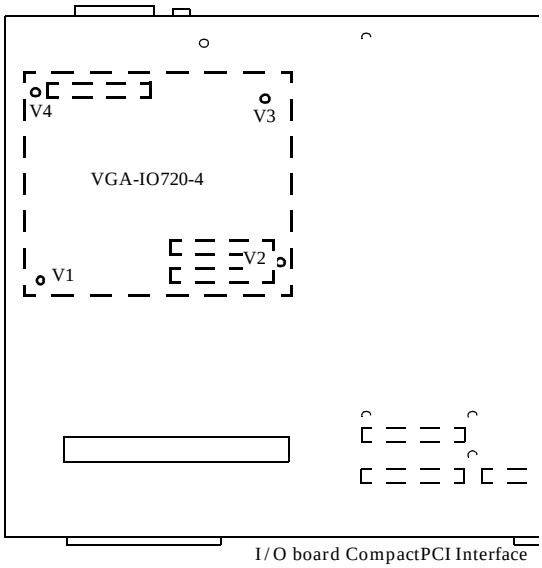


Figure 11: *Mounting Points of the VGA-IO721-4 on the Bottom of an I/O Board*

After the hardware installation is completed and the PENT/CPCI-721 is installed in the CompactPCI rack, enter the BIOS Setup and select VGA as video system type (see the “Boot Configuration in Setup” section on page 4-5).

IDE Devices

It is possible to connect up to four IDE devices to the PENT/CPCI-721:

- As a factory option, a 16 MByte flash disk can be installed to the primary IDE port.
- A HD accessory kit can be installed to the primary IDE port via the on-board connector.

Before connecting IDE devices to the primary or secondary IDE port:

1. Check for IDE devices already connected to the IDE interface
2. Decide which IDE device should be master and which should be slave
3. Check for switch settings and change configuration if necessary

Note: If connecting a device to the secondary IDE port, make sure that the length of the ribbon cable does not exceed 0.45 m (18 inches).

At the first boot after connecting an IDE device, modify the BIOS parameters in setup (see the “Boot Configuration” section on page 4-6).

SCSI Device Connection

8-bit or 16-bit SCSI devices can be connected to the PENT/CPCI-721. Before connecting a SCSI device check the SCSI termination and set the respective PENT/CPCI-721 switch appropriately (see “Action Plan” on page 2-10).
At the first boot after connecting a SCSI device check that the SCSI ID of the device to be installed is not in conflict with the IDs of already installed SCSI devices.

Switch Settings

The PENT/CPCI-721 is configurable via two micro switches. The switches are located on the base board and on the I/O panel. The tabs are in white and are displayed in the off position.

Table 9: *PENT/CPCI-721 Switch Settings*

Name and Default Setting		Description
	SW0100 1 OFF	User flash IDE mode OFF= User flash is primary IDE slave. ON= User flash is primary IDE master.
	SW0100 2 OFF	Keyboard control OFF= Keyboard enabled ON= Keyboard disabled
	SW0100 3 OFF	Reset key control OFF= Reset key enabled ON= Reset key disabled
	SW0100 4 OFF	Abort key control OFF= Abort key enabled ON= Abort key disabled
	SW0300 1 OFF	BIOS flash write protection OFF= Writing enabled ON= Writing disabled
	SW0300 2 OFF	Reserved
	SW0300 3 OFF	Ethernet connector selection OFF= Ethernet via front panel connector ON= Ethernet via CompactPCI connector
	SW0300 4 OFF	BIOS flash bootblock write protection OFF= Write-protected ON= Writing enabled

Table 10: *I/O-721 Switch Settings*

Name and Default Setting		Description
	SW0900 1 OFF	Reserved
	SW0900 2 OFF	Reserved
	SW0900 3 OFF	SCSI termination OFF= Lower 8-bit term disabled ON= Lower 8-bit term enabled
	SW0900 4 OFF	SCSI termination OFF= Upper 8-bit term disabled ON= Upper 8-bit term enabled

Board Installation

Since the PENT/CPCI-721 is a system slot board, it always has to be installed in the system slot which is marked by a triangle. The I/O-721 is a peripheral slot board, i.e. the board has to be operated in a peripheral slot which is marked by a circle. Otherwise the board or other cards in the system may be damaged.

Voltage Supply

The PENT/CPCI-721 is a CompactPCI board operational in 5V CompactPCI systems. A voltage key is provided on the CompactPCI interface.

Caution



- **Always plug the PENT/CPCI-721 into a system slot marked by a triangle.**
- **Always plug the I/O-721 in a peripheral slot marked by a circle.**

Installation in a Non-Powered System

In order for the PENT/CPCI-721 to operate properly, the I/O-721 has to be installed on the PENT/CPCI-721.

Caution



Only operate the PENT/CPCI-721 when the I/O-721 is installed.

Installing the I/O-721 on the PENT/CPCI-721

In order to install the I/O-721 on the PENT/CPCI-721, proceed as follows:

1. Connect I/O-721 to PENT/CPCI-721
2. Fasten I/O-721 board locks to PENT/CPCI-721 board locks
3. Fasten four screws at location I1, I2, I3, and I4

Removing the I/O-721 from the PENT/CPCI-721

In order to uninstall the I/O-721 from the PENT/CPCI-721, proceed as follows:

1. Remove four screws at location I1, I2, I3, and I4 (see figure below)

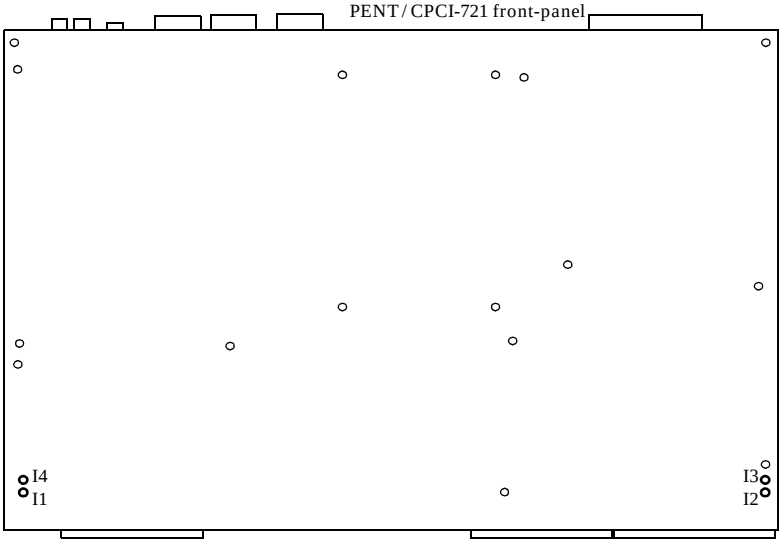


Figure 12: *Mounting Points of the I/O-721 on the PENT/CPCI-721*

2. Disconnect I/O board locks from PENT/CPCI-721locks (see figure below):

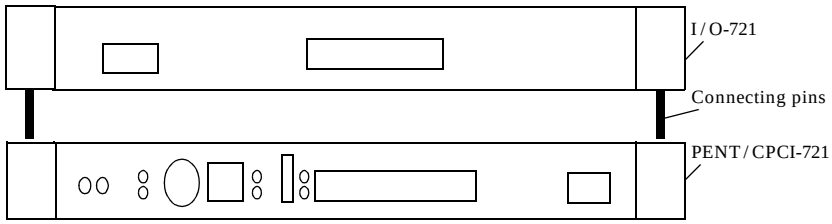


Figure 13: *Connecting Pins between Front Panel Handles*

3. Disconnect I/O board from base board (see ❶ in the figure below):

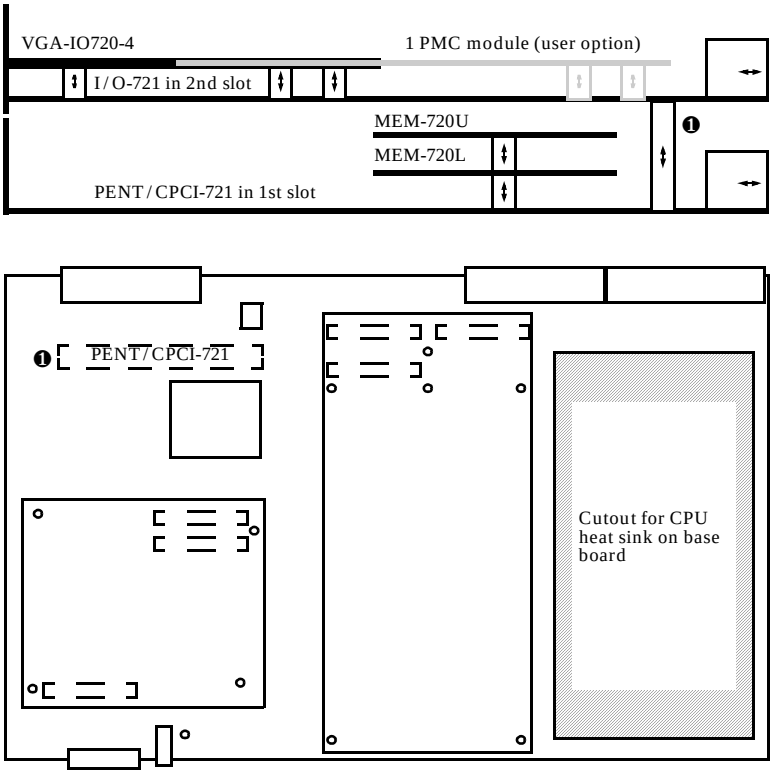


Figure 14: *PCI Interconnection between PENT/CPCI-721 and I/O-721*

Software Upgrades and Accessories

The following software upgrades and accessories are available for the PENT/CPCI-721.

BIOS Upgrade Kit

The BIOS upgrade kit contains a DOS-formatted floppy disk with BIOS upgrade file and upgrade utilities, e.g. to reflect extended hardware support. For installation information, see the README file contained on the floppy disk.

NT Driver Kit

The NT driver kit contains a CD-ROM with the Card Executive 2.0 for NT PCMCIA driver. For installation information, see the README file contained on the CD-ROM.

NT Support Package

The NT support package contains a CD-ROM with Windows NT drivers for extended hardware support (e.g. Ethernet). For installation information see the README file contained on the CD-ROM.

Battery

The board is designed to be maintenance-free. However, note that a Lithium battery is installed on the board. The battery provides a data retention of five years summing up all periods of actual battery use. Therefore Force Computers assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.

Caution



- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is already installed.**
- **If the battery is covered by a PMC module on slot 1 or a memory module, the module must be removed first.**
- **Do not use a screwdriver to remove the battery from its holder to avoid possible damage to the PCB or the battery holder.**
- **When installing the new battery ensure that the '+' on top of the battery stays at the top and therefore is visible when viewing the board from its component side.**
- **If necessary reinstall the PMC or memory module in its correct position.**

3

Controls, Indicators, and Connectors

Front Panel

The following subsections describe the connectors, keys, and LEDs which are available on the PENT/CPCI-721 and on the I/O-721.

Connectors

The PENT/CPCI-721 provides front panel connectors.

These are the available front panel connectors:

- Keyboard and mouse
- Ethernet
- USB
- PC Card
- COM1

If the PENT/CPCI-721 is to be incorporated into larger systems and adapted to specific needs, the following connector pinouts may be useful to give information on which signal is assigned to which pin.

Note: Make sure that the length of keyboard, mouse, and USB cables does not exceed three meters and that the cables are installed apart from other cables.

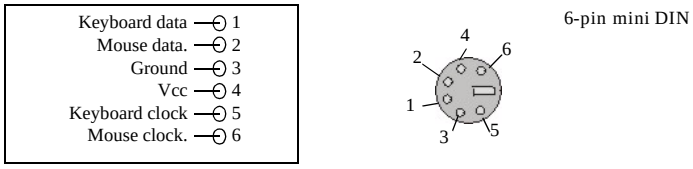


Figure 15: *K/M- Keyboard and Mouse Connector Pinout*

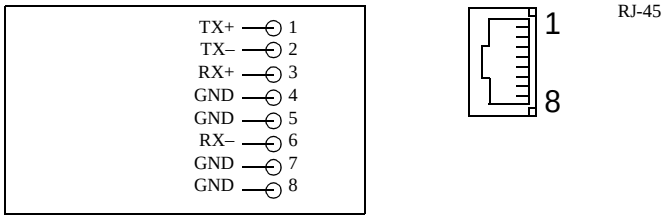


Figure 16: *ETH - Ethernet Connector Pinout*

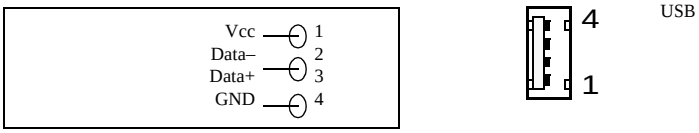


Figure 17: *USB Connector Pinout*

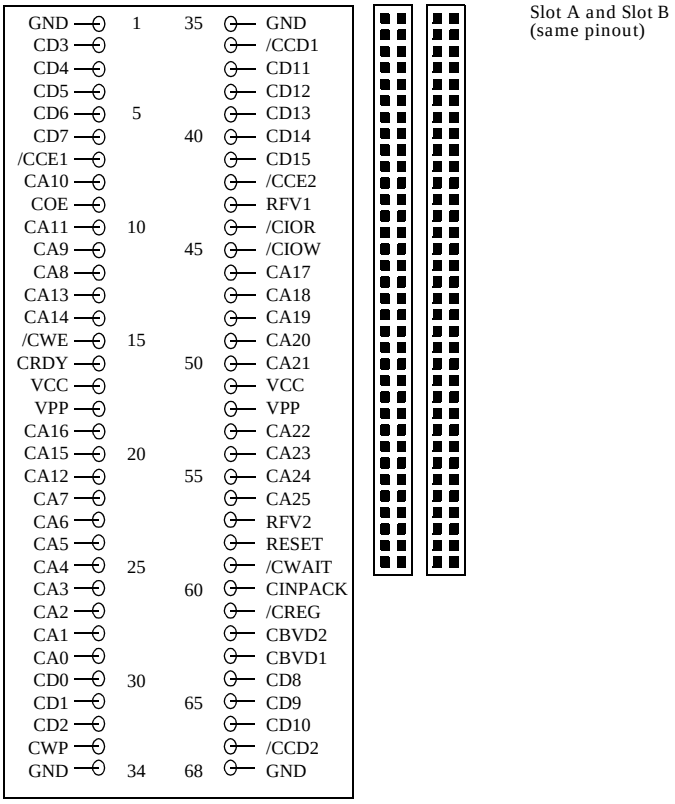


Figure 18: *PCMCIA (PC Card) Connector Pinout*

One Type-III or two Type-II PC cards can be connected. A power supply of +12V is available at the PC card interface.

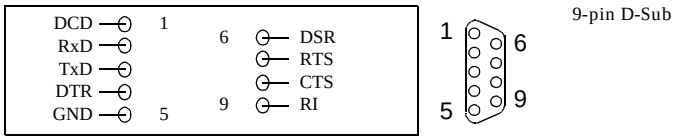


Figure 19: *COM1 Connector Pinout*

Keys

The PENT/CPCI-721 provides front panel keys which will be described below.

Reset Key

When enabled and toggled, it instantaneously affects the CPU board by generating a reset. The reset generates a PCI reset and is programmable to be globally or local to the CPU board via the PCI Bus Control Register.

A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. RESET is held active until the key is back in the inactive position, however at least 200 ms are guaranteed by a local timer. Power fail (below approximately 4.7V) and power up – both lasting at least 200 ms to 300 ms – also force a reset to start the CPU board.

Abort Key

When enabled and toggled, it instantaneously affects the CPU board by generating an interrupt request (NMI) via the PCI-to-ISA bridge. This allows to implement an abort of the current program, to trigger a self-test or to start a maintenance program.

Note: For information on how to disable the keys, see the "Action Plan" section on page 2-10.

LEDs

This section describes the LEDs provided.

PENT/CPCI-721

The following front panel LEDs are provided on the PENT/CPCI-721:

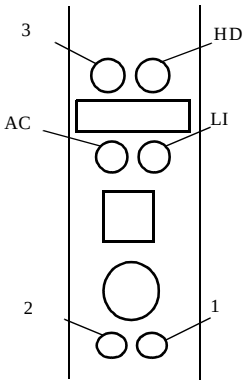


Figure 20: *Front Panel LEDs on the PENT/CPCI-721*

Table 11: *Description of Front Panel LEDs on the PENT/CPCI-721*

LED	Description
1, 2, 3	User LEDs: Software programmable by the Base Board LED Control Register. Possible LED status: green, red, or off.
AC	Activity LED: Signals Ethernet network transfers regardless of the connector used – front panel or CompactPCI connector. Possible LED status: Yellow or off.
HD	Hard disk LED: signals accesses to devices connected via IDE. Possible LED status: flickering during access activity, else off. The LED color is customizable via the Base Board LED Control Register.
LI	Link LED: Signals successful connection to a network regardless of the connector used – front panel or CompactPCI connector. Possible LED status: Green or off.

I/O-721

The following front panel LEDs are provided on the I/O-721:

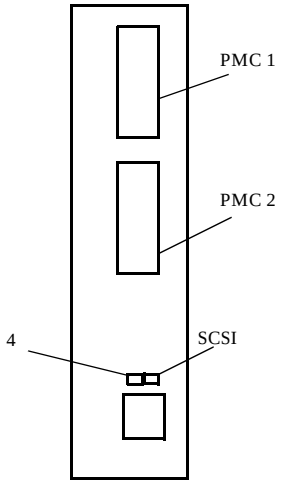


Figure 21: *Front Panel LEDs on the I/O-721*

Table 12: *Description of Front Panel LEDs on I/O-721*

LED	Description
4	User LED: Software programmable by the I/O Board LED Control Register. Possible LED status: green or off.
SCSI	Hard disk LED: signals accesses to devices connected via SCSI. Possible LED status: flickering during access activity, else off.

On-Board Connectors

The following section describes the connectors provided.

PENT/CPCI-721

The PENT / CPCI-721 also provides on-board connectors. The interfaces available on the CompactPCI connectors can be routed to interface-dependent standard connectors via the IOBP-CPU720.

For information on the available PMC modules, see the “PMC Module” section on page 2-12.

J1 and J2

The J1 and J2 connectors implement the ComapctPCI 64-bit connector pinout as specified by the CompactPCI specification. Therefore, this manual only documents the pinout of the J5 connector.

J5

Beside the CompactPCI-specific pinout the following ports are available on the CompactPCI J5 connector of the PENT / CPCI-721 (the name used in the following pinout is given in brackets):

- Primary (1st IDE) and secondary (2nd IDE)
- USB (USB), Keyboard (KBD), PS2 mouse (MSE), COM1 (COM1), COM2 (COM2), LPT (LPT), floppy (FD)
- Ethernet (ETH)

A	B	C		D	E
SMI	reserved	reserved	1	reserved	ETH RX–
ETH TX–	reserved	ETH TX+	2	ETH RX+	reserved
KBD clock	KBD data	MSE clock	3	MSE data	IDE /DIAG
1st IDE A2	2nd IDE A2	1st IDE /CS3	4	USB P1–	USB P1+
2nd IDE A0	1st IDE /CS1	2nd IDE /CS1	5	2nd IDE /CS3	IDE /RST
1st IDE IRQ	2nd IDE IRQ	1st IDE A1	6	1st IDE /LED	2nd IDE /LED
1st IDE /IOR	2nd IDE /IOR	IDE IORDY	7	2nd IDE A1	1st IDE A0
IDE D15	1st IDE DRQ	2nd IDE DRQ	8	1st IDE DAK	2nd IDE DAK
IDE D10	IDE D11	IDE D12	9	1st IDE /IOW	2nd IDE /IOW
IDE D5	IDE D6	IDE D7	10	IDE D13	IDE D14
IDE D0	IDE D1	IDE D2	11	IDE D8	IDE D9
FD /DR1	FD DENSEL	FD DRATE0	12	IDE D3	IDE D4
FD /DSKCHG	FD /WP	FD /MTR0	13	FD MSEN0	Vcc
FD /HDSEL	FD /DIR	FD /STEP	14	FD /MTR1	FD /DR0
Vcc	LPT Pe	FD /RDATA	15	FD /TRK0	FD /INDEX
LPT Busy	LPT /Init	LPT Slct	16	FD /WDATA	FD /WGATE
LPT /Autofeed	LPT Data 5	LPT /Slctin	17	LPT /Error	LPT /Ack
LPT Data 4	LPT Data 0	LPT Data 6	18	LPT Data 7	LPT Strobe
COM2 RI	/PBRESET	LPT Data 1	19	LPT Data 2	LPT Data 3
COM2 RxD	COM2 TxD	COM2 DTR	20	COM2 RTS	COM2 CTS
COM1 RTS	COM1 CTS	COM1 RI	21	COM2 DCD	COM2 DSR
COM1 DCD	COM1 RxD	COM1 TxD	22	COM1 DTR	COM1 DSR

Figure 22: *PENT/CPCI-721 CompactPCI J5 Connector Pinout*

I/O-721

In addition to its CompactPCI interface the I/O-721 provides the following CompactPCI connectors (see below).

The interfaces available on the CompactPCI interface can be routed to interface-dependent standard connectors via the IOBP-IO720.

J1 and J2

The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as defined by the CompactPCI specification. Therefore, this manual only documents the pinout of the J5 connector.

J5

Besides the CompactPCI specific pinout the following ports are available on the I/O-721 CompactPCI J5 connector (the name used in the following pinout is given in brackets):

- 16-bit SCSI (SCSI)
- VGA (VGA)
- User I/O pins for PMC slot 1 (PMC 1 I/O)

A	B	C		D	E
I/O	SCSI D8	SCSI TERMP	1	SCSI D0	ATN–
MSG–	SCSI D9	DPH	2	SCSI D1	BSY–
SEL–	SCSI D10	GND	3	SCSI D2	ACK–
REQ–	SCSI D11	DPL	4	SCSI D3	RST–
SCSI D15	SCSI D12	GND	5	SCSI D4	SCSI D7
SCSI D14	SCSI D13	C/D–	6	SCSI D5	SCSI D6
VGA VSYNC	VGA HSYNC	VGA GND	7	SCL	VGA AGND
VGA R	VGA GND	VGA B	8	SDA	VGA G
3.3V	3.3V	3.3V	9	5V	5V
V(I/O)	PMC 1 I/O 64	PMC 1 I/O 63	10	PMC 1 I/O 62	PMC 1 I/O 61
PMC 1 I/O 60	PMC 1 I/O 59	PMC 1 I/O 58	11	PMC 1 I/O 57	PMC 1 I/O 56
PMC 1 I/O 55	PMC 1 I/O 54	PMC 1 I/O 53	12	PMC 1 I/O 52	PMC 1 I/O 51
PMC 1 I/O 50	PMC 1 I/O 49	PMC 1 I/O 48	13	PMC 1 I/O 47	PMC 1 I/O 46
PMC 1 I/O 45	PMC 1 I/O 44	PMC 1 I/O 43	14	PMC 1 I/O 42	PMC 1 I/O 41
PMC 1 I/O 40	PMC 1 I/O 39	PMC 1 I/O 38	15	PMC 1 I/O 37	PMC 1 I/O 36
PMC 1 I/O 35	PMC 1 I/O 34	PMC 1 I/O 33	16	PMC 1 I/O 32	PMC 1 I/O 31
PMC 1 I/O 30	PMC 1 I/O 29	PMC 1 I/O 28	17	PMC 1 I/O 27	PMC 1 I/O 26
PMC 1 I/O 25	PMC 1 I/O 24	PMC 1 I/O 23	18	PMC 1 I/O 22	PMC 1 I/O 21
PMC 1 I/O 20	PMC 1 I/O 19	PMC 1 I/O 18	19	PMC 1 I/O 17	PMC 1 I/O 16
PMC 1 I/O 15	PMC 1 I/O 14	PMC 1 I/O 13	20	PMC 1 I/O 12	PMC 1 I/O 11
PMC 1 I/O 10	PMC 1 I/O 9	PMC 1 I/O 8	21	PMC 1 I/O 7	PMC 1 I/O 6
PMC 1 I/O 5	PMC 1 I/O 4	PMC 1 I/O 3	22	PMC 1 I/O 2	PMC 1 I/O 1

Figure 23: *I/O-721 CompactPCI J5 Connector Pinout*

IOBP-IO720

The I/O-721 includes a front panel industry standard connector for VGA (same as in Figure 29 “VGA Connector Pinout” on page 3-15).

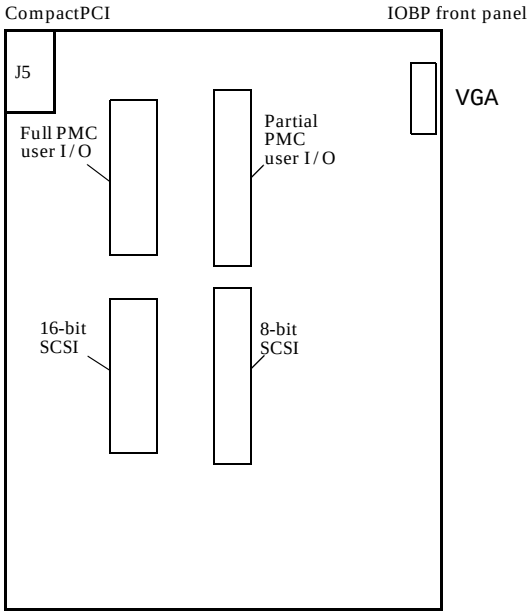


Figure 24: *IOBP-IO720*

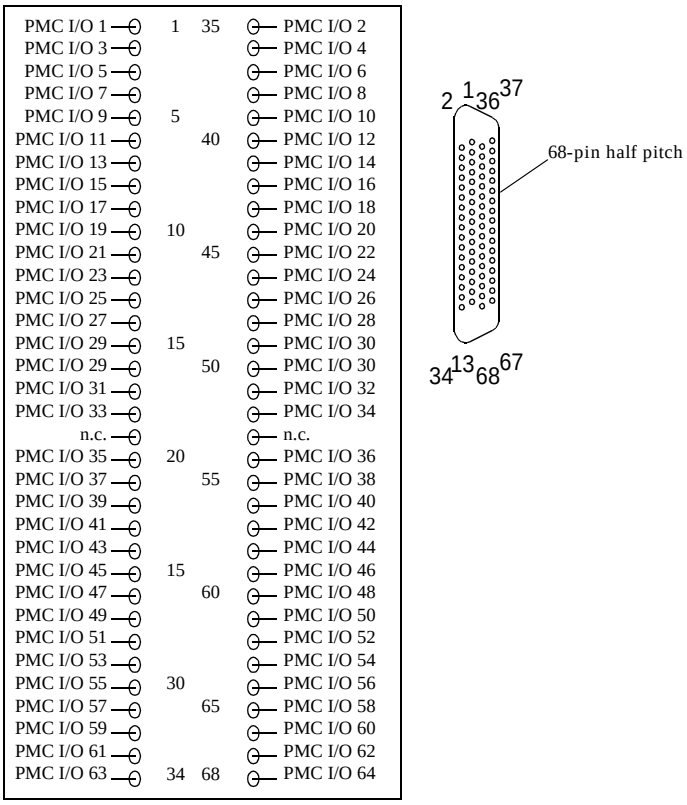


Figure 25: *Connector Pinout for Full PMC User I/O*

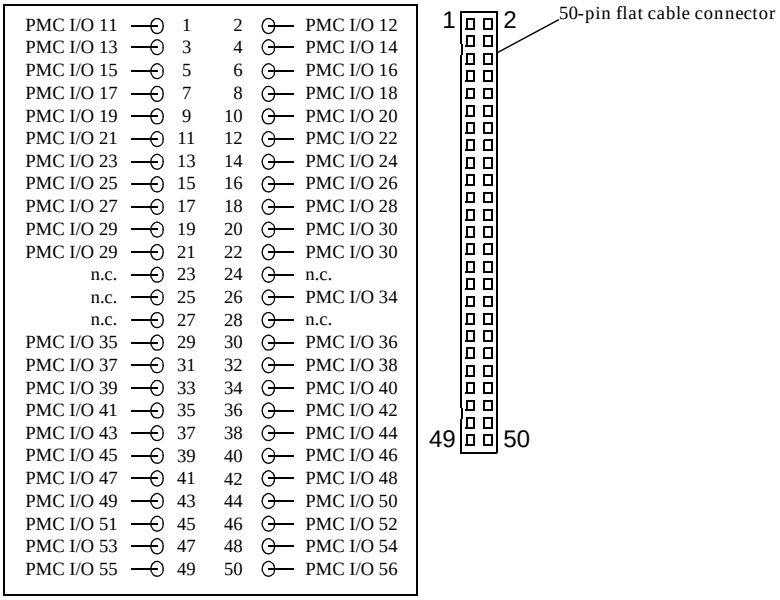


Figure 26: *Connector Pinout for Partial PMC 2 User I/O*

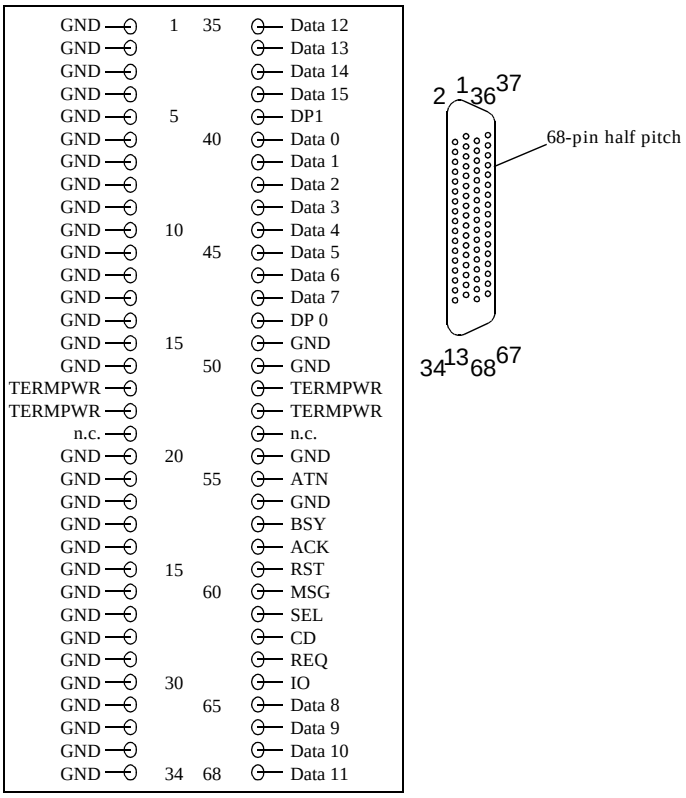


Figure 27: *16-bit SCSI Connector Pinout*

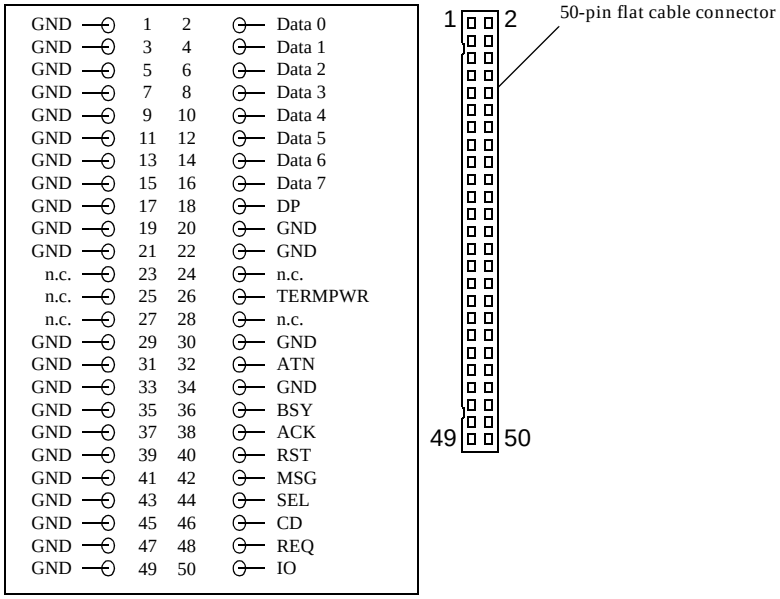


Figure 28: *8-bit SCSI Connector Pinout*

VGA-IO720-4

As a factory option the VGA-IO720-4 graphics controller based on the Chips&Tech 69030 graphics device is installed on the I/O-721 board providing the following graphics modes:

- 1600x1200 dots resolution and max. 65536 colors at max. 60 Hz vertical refresh
- 1280x1024 dots resolution and max. 16.777.216 colors at max. 75 Hz vertical refresh
- 1024x768 dots resolution and max. 16.777.216 colors at max. 100 Hz vertical refresh
- 800x600 dots resolution and max. 16.777.216 colors at max. 100 Hz vertical refresh
- 640x480 dots resolution and max. 16.777.216 colors at max. 100 Hz vertical refresh

Danger



Make sure to use only the graphics modes and refresh rates supported by your monitor or display device. Otherwise temporary malfunction or permanent damage may occur to your monitor or display device. This could cause fire and personal injury. We recommend consulting the manual of the attached monitor or display device before setting the graphics mode. For testing and setting up a low resolution mode

e.g. 640x480 at a low vertical refresh rate e.g. 60Hz should be a safe starting point. If your monitor shows a distorted picture or produces audible sounds, immediately switch off the monitor and check for supported graphics modes and refresh rates.

Note: Although always assembled, the VGA connector will only provide VGA signals if the VGA-IO720-4 has been installed.

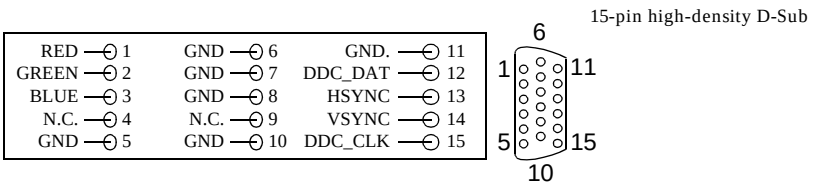


Figure 29: *VGA Connector Pinout*

4

BIOS

Features

The PENT/CPCI-72x is designed to run with Windows NT Version 4.0. The initial boot-up procedure is performed by BIOS which provides the following features:

- Upgradable via software utility
- PCI 2.1 compliant
- Plug-and-Play 4.0 compliant (PnP)
- DMI 2.00.1 BIOS support
- Advanced Power Management
- Hardware setup
- Hardware initialization at boot: At power on or reset, BIOS performs Power-On Self Test (POST) routines to test system resources. Afterwards it loads and starts the operating system.

Boot Selection Menu

BIOS automatically starts during power-up or reset.

Press <Esc> while boot-up screen is displayed to continue with the POST screen until the end of POST. Then the boot selection menu is displayed. In the boot menu, you will find the following options:

1. Override existing boot sequence (for this boot only) by selecting another boot device from boot-order list
   If the specified device does not load the operating system, BIOS reverts to previous boot sequence.
2. Enter Setup
3. Press <Esc> to return to the POST screen and continue with previous boot sequence

Setup

BIOS provides the Setup program to configure the setting of a wide range of system board features.

Press <F2> to enter Setup. The following options are displayed:

- LPT, COM1 and COM 2 can be remapped via the advanced configuration option for integrated peripherals in BIOS setup.
- The IDE devices can be configured via the main configuration options for primary and secondary IDE masters and slaves and via the advanced configuration option for intergrated peripherals. This configuration capability is used for example at the first boot after connecting an IDE device.
- The floppy type can be configured via the respective main configuration options for diskettes. This configuration capability is used for example at the first boot after installing a floppy via the respective I/O panel.
- The video system type can be configured via the related main configuration option. This configuration capability is for example used at the first boot after installing the VGA accessory kit.

Boot Configuration

The boot configuration options in Setup let you select the order of the devices from which BIOS attempts to boot the operating system. During POST, BIOS tries the next one on the list if it is unsuccessful at booting from one device.

Each device listed represents the first of a group of devices if more than one device of this group is installed on the system. For example, if there is more than one hard disk drive, the displayed entry represents the first of these drives as specified in the boot configuration option for fixed media. The same applies to removable media.

The same options determine the order in which POST installs the devices and the operating system assigns device letters. BIOS supports up to two floppy devices, to which the operating system may assign, for example, drive letters A: and B:.

C:, D:, E:, etc. are assigned to hard-disk drives.

Note: There is not always an exact correspondence between the order specified in these menus and the letters assigned by the operating system. Many devices such as legacy option ROMs support more than one device, which can be assigned more than one letter. If you want the CD-ROM drive to be listed before the hard drive, move it in front of the hard drive. The group of bootable add-in cards refers to devices with non-multiboot-compliant BIOS option ROM from which you can boot the operating system.

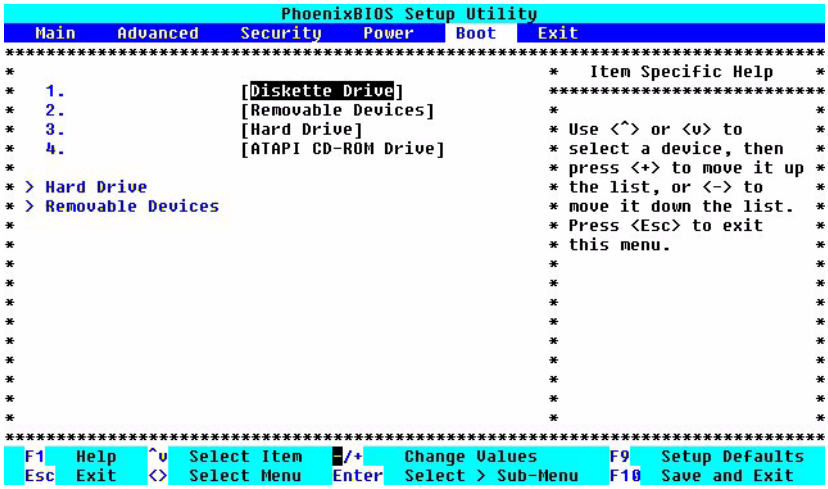


Figure 30: *Sample Setup Showing the Boot Configuration Options*

In the example above BIOS attempts to boot in the following order:

1. Diskette Drive - from floppy disk
2. Removable Devices
3. Hard Drive - from hard disk
4. ATAPI CD-ROM Drive

Note:

- **If you save changes you made in Setup, the selections in the menus are stored in NVRAM (CMOS). The next time the system board boots, BIOS configures the system according to the Setup selections stored in NVRAM (CMOS). If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the default values or try to change the selections that caused the boot to fail.**
- **If you get the default values, note that the displayed default values are not yet stored to be effective for the next boot. They are just loaded to be displayed. However, they are effective when the current boot-up procedure is resumed.**

Depending on the messages displayed, there are other keyboard inputs resulting in calls to special BIOS set-up programs, including, for example, <Ctrl>+<A> to enter the SCSI BIOS for the dual-segment variant. If the BIOS or an Option ROM (e.g. of an add-on card) requests keyboard input, you are prompted to enter the information. POST continues from there with the regular POST screen.

Note: Whenever POST detects a non-fatal error, BIOS displays the errors. It then displays a message asking you to choose between boot continuation or error correction via Setup.

Sample Start-Up

The following figure shows a sample start-up message following the video BIOS message which displays the graphic card type and the video RAM size.

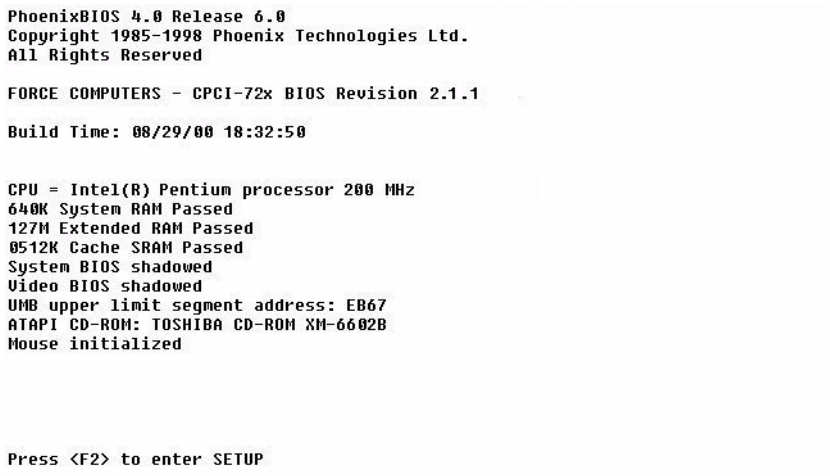


Figure 31: *Sample Start-Up Message*

Note:

- **The NVRAM (CMOS) values may have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS). BIOS detects such problems by verifying a so-called "System CMOS Checksum".**
- **If, during bootup, BIOS detects a problem in the integrity of values stored in NVRAM (CMOS), it displays a message asking you to choose between boot continuation or entering Setup with the ROM default values already loaded into the menus.**
- **After entering Setup with the ROM default values already loaded into the menus, it might be possible to restore some values as saved in NVRAM (CMOS) via the exit configuration option to load previous values.**

BIOS Messages

If your system fails after you have made changes to the set-up menus, you may be able to correct the problem by entering Setup and restoring the original values.

Message	Explanation	Corrective Action
`nnnn Cache SRAM Passed`	Where *nnnn* is the amount of system cache in KBytes successfully tested	None
`CD-ROM Drive Identified`	Autotyping identified CD-ROM Drive	None
`Diskette drive A error` `Diskette drive B error`	Drive A: or B: is present but fails the BIOS POST disk tests. Drive is selected via setup but either not present or defect.	Check that the drive is defined with the proper disk type in Setup, that the disk drive is attached correctly nd the controller is enabled.
`Entering SETUP ...`	Starting Setup program	None
`Extended RAM Failed at offset: nnnn`	Extended memory not working or not configured properly at offset *nnnn*	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.
`nnnn Extended RAM Passed`	Where *nnnn* is the amount of RAM in KBytes successfully tested	None
`Failing Bits: nnnn`	The hex number *nnnn* is a map of the bits at the RAM address (in system, extended, or shadow memory) which failed the memory test. Each `1` (one) in the map indicates a failed bit.	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.

Message	Explanation	Corrective Action

`Fixed Disk 0 Failure`
`Fixed Disk 1 Failure`
`Fixed Disk Controller Failure`
	Fixed disk is not working or not configured properly.	Check to see if fixed disk is attached properly. Run Setup to be sure the fixed-disk type is correctly identified.

`Fixed Disk 0...3 Identified`	Autotyping identified specified fixed disk.	None
`Incorrect Drive A type - run SETUP` `Incorrect Drive B type - run SETUP`	Type of floppy drive not correctly identified in Setup	Check for correct floppy drive in setup.
`Keyboard controller error`	The keyboard controller failed test.	Replace the keyboard.
`Keyboard error`	Keyboard not working	Check for correct keyboard connection.
`Keyboard error nnn`	BIOS discovered a stuck key and displays the scan code *nn* for the stuck key.	Replace keyboard, check for stuck keys.
`Operating system not found`	Operating system cannot be located on either drive A: or drive C:.	Enter Setup and see if fixed disk and drive A: are properly identified.
`Parity Check 1 nnnn`	Parity error found in the system bus. BIOS attempts to locate the address *nnnn* and display it on the screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.
`Parity Check 2 nnnn`	Parity error found in the system bus. BIOS attempts to locate the address *nnnn* and display it on the screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.

Message	Explanation	Corrective Action
`Press <F1> to resume, <F2> to Setup`	Displayed after any recoverable error message	Press <F1> to start the boot process or <F2> to enter Setup and change any settings.
`Previous boot incomplete - Default configuration used`	Previous POST did not complete successfully. POST loads default values and offers to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail.	Run Setup to restore the original configuration. This error is cleared the next time the system is booted.
`Real time clock error`	Real-time clock fails BIOS test.	May require board repair.
`Resource allocation conflict on motherboard - Run Configuration Utility`	Possible interrupt or I/O ressource conflict	Run ISA or EISA Configuration Utility to resolve resource conflict.
`Shadow RAM Failed at offset: nnnn`	Shadow RAM failed at offset *nnnn* of the 64k block at which the error was detected.	Contact your local sales representative or FAE for further support.
`nnnn Shadow RAM Passed`	Where *nnnn* is the amount of shadow RAM in KBytes successfully tested	None
`System battery is dead - Replace and run SETUP`	The NVRAM (CMOS) clock battery indicator shows the battery is dead.	Replace the battery and run Setup to reconfigure the system.
`System BIOS shadowed`	System BIOS copied to shadow RAM.	None
`System cache error - Cache disabled`	RAM cache failed the BIOS test. BIOS disabled the cache.	Contact your local sales representative or FAE for further support.

Message	Explanation	Corrective Action
`System CMOS checksum bad - run SETUP`	System NVRAM (CMOS) has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS).	Run Setup and reconfigure the system either by getting the default values and / or making your own selections.
`System RAM Failed at offset: nnnn`	System RAM failed at offset *nnnn* in the 64k block at which the error was detected.	Check for correct-memory modules . Otherwise contact your local sales representative or FAE for further support.
`nnnn System RAM Passed`	Where *nnnn* is the amount of system RAM in KBytes successfully tested	None
`System timer error`	The timer test failed.	Requires repair of system board.
`UMB upper limit segment address: nnnn`	Displays the address *nnnn* of the upper limit of upper memory blocks, indicating released segments of the BIOS which may be reclaimed by a virtual memory manager.	None
`Video BIOS shadowed`	Video BIOS successfully copied to shadow RAM.	None
`Invalid System Configuration Data – run configuration utility`		Enter Setup and use the advanced configuration option to reset the configuration data (due to corrupted ESCD data).

5

SCSI BIOS

Features

The SCSI BIOS must be enabled if you want the system to boot from a SCSI hard disk drive connected to the adapter. If the devices on the SCSI bus are controlled by device drivers and therefore do not need a BIOS, you can disable the SCSI BIOS to free about 16 KBytes of memory. This also shortens the boot time by up to 60 seconds.

The SCSI BIOS provides two functions to support user configuration:

- Listing of the actually used SCSI IDs and correlated LUNs
- Setup options to adapt the CPU board and its SCSI configuration to the user's needs. The default configuration is marked within SCSI BIOS Setup.

The SCSI IDs are listed during boot up when entering SCSISelect. You can list actually assigned SCSI IDs within the BIOS Setup when you select the SCSI disk utilities from the initial SCSI BIOS Setup screen.

If you need to know the available LUNs, select the SCSI device you want to configure. If there are multiple logical units, SCSI BIOS displays a menu of correlated LUNs.

Some Setup options apply to the host adapter; other options apply individually to each device on the SCSI bus. In some cases the allowable value range depends on the actual SCSI bus width used (8-bit or 16-bit). Some Setup options list the current device settings for each SCSI ID, even IDs not assigned to a device.

Note:

- **In case of display problems press <F5> to toggle the display between color and monochrome. This feature may not work on all monitors.**
- **The default settings are appropriate for most applications, so there usually is no need to change the settings. If you have to change the settings of the advanced configuration options listed below, you should ensure that you thoroughly understand the consequences of the change before actually doing so.**

Selectable Host Adapter SCSI ID

SCSI IDs range from 0…7 if the respective device is operated on an 8-bit SCSI bus and from 0…15 on a 16-bit SCSI bus. For 8-bit devices, ID 7 has the highest priority and ID 0 has the lowest priority. For l6-bit devices, the priority of IDs is 7 … 0, then 15 … 8. In this case, ID 7 has the highest priority and ID 8 has the lowest priority. Each host adapter (8- or 16-bit) has the default SCSI ID of 7, which gives the adapter the highest priority on the SCSI bus.

Note: Host adapter SCSI termination: The configuration of the host adapter SCSI termination within SCSI BIOS is not supported because the SCSI termination is controlled by SW0900C and SW0900D (see page 2-13).

SCSI Parity Checking

Each adapter uses SCSI parity checking to verify the accuracy of data transfer on the SCSI bus. Most currently available SCSI devices support SCSI parity check. If a device on the SCSI bus does not support it, disable parity checking.

Selectable Boot Device

Selectable boot device by specifying the boot target ID (and LUN in case the device has implemented multiple logical units).

Selectable Settings For Synchronous Data Transfer

Synchronous data transfer is faster than asynchronous data transfer:

- If the adapter is set not to negotiate for synchronous data transfer, the value to be selected will be the maximum rate at which the adapter accepts data from the device during negotiation. This is standard SCSI protocol. The values displayed assume that UltraSCSI support is enabled (see the respective advanced configuration option shown below). If not, the speeds are half those shown.
- Most SCSI devices support synchronous negotiation. If a device does not support synchronous negotiation, the adapter will automatically transfer the data in asynchronous mode.
- Specification of the maximum sync transfer rate: The maximum synchronous data transfer rate determines the rate that the adapter negotiates with the device. The adapter automatically negotiates for the rate requested by the device.
- Sync negotiation: Synchronous negotiation is a SCSI feature that allows the SCSI adapter and its attached SCSI devices to transfer data in synchronous mode. The setting determines whether the adapter initiates synchronous negotiation with the SCSI device. However, the adapter always responds to synchronous negotiation if the SCSI device initiates it. If neither the adapter nor the SCSI device negotiates for synchronous data transfers, data will be transferred in asynchronous mode.

Enabling Disconnection

Enabling disconnection allows a SCSI device to disconnect from the SCSI bus (sometimes called Disconnect/Reconnect). It allows the adapter to perform other operations on the SCSI bus while the SCSI device is temporarily disconnected. The SCSI device may choose not to disconnect, however, even if permitted by the adapter (this can usually be configured on the SCSI device). Leave this option set to yes if the adapter connects to two or more SCSI devices. This optimizes SCSI bus performance. If the adapter connects to only one SCSI device, set enable disconnection to no to achieve slightly better performance.

Send Start Unit Command

Enabling the adapter to send the SCSI start unit command to the SCSI device (SCSI command 1B) reduces the load on a system's power supply by allowing the adapter to turn on SCSI devices one by one when the system boots. Otherwise, all SCSI devices are turned on at the same time. Before you enable this option for a device, check the device documentation to make sure the device supports the command. On most devices, you must also change a switch or jumper setting on the device to enable the device to respond to the command. If you enable the SCSI start unit command for more than one SCSI device, the adapter first sends the command to the boot device specified in SCSI BIOS. When this device responds, further commands are sent to the remaining devices, beginning with the device with lowest SCSI ID. The boot time varies depending on how long each drive takes to spin up.

Initiate Wide Negotiation

Initiating wide negotiation is possible: If the host adapter is enabled to initiate wide negotiation, it lets the adapter initiate wide negotiation with a 16-bit SCSI device only. The adapter will not attempt wide negotiation with 8-bit devices. So you can leave this option enabled even if the bus includes 8-bit devices.

Advanced Configuration Options

The SCSI BIOS includes the following advanced configuration options.

Plug-and-Play Support

When Plug-and-Play support is enabled, the adapter automatically assigns a SCSI ID to an attached SCSI device that supports the SCAM-1 protocol. Most non-SCAM devices tolerate SCAM protocol, so this option can usually be enabled even in case of some non-SCAM devices. However, in rare cases, an old SCSI-l device may not tolerate SCAM and may cause the system to hang or operate erratically.

Support for Removable Disks

Setting the support for removable disks under BIOS as fixed disks controls which removable-media drives are supported by the SCSI BIOS. The following choices are available:

- Boot only: Only the removable-media drive designated as the boot device is treated as a hard disk drive.
- All disks: All removable-media drives supported by the SCSI BIOS are treated as hard drives.
- Disabled: No removable-media drives running under DOS are treated as hard disk drives. In this situation, driver software is needed, because the drives are not controlled by the SCSI BIOS.

Extended Translation Scheme for DOS Drives > 1 GByte

All current MS-DOS versions are limited to 1024 cylinders per drive. The standard translation scheme for SCSI host adapters, using 64 heads and 32 sectors, provides a maximum accessible capacity of 1 GByte. To support disk drives larger than 1 GByte, the SCSI BIOS includes an extended translation scheme that supports disk drives as large as 8 GBytes under MS-DOS. With extended translation enabled, drives handled by the SCSI BIOS use extended translation if their formatted capacity is greater than 1 GByte, and drives smaller than 1 GByte use standard translation.

Note: Loss of data: If you decide to change the translation scheme, back up the disk drives first! All data is erased when you change from one translation scheme to another.

When you partition a disk larger than 1 GByte, use the MS-DOS fdisk utility as you normally would. Because the cylinder size increases to 8 MBytes under extended translation, the partition size you choose must be a multiple of 8 MBytes. If you request a size that is not a multiple of 8 MBytes, fdisk rounds up to the nearest whole multiple of 8 MBytes.

Multiple LUN Support

When enabled, the BIOS supports multiple logical units. Enable this option if any devices have multiple logical units.

BIOS Support for Bootable CD-ROM

Leave the BIOS support for bootable CD-ROM enabled to boot from a CD-ROM. If booting from a hard disk or other device, make sure no bootable CD-ROM is installed, or disable this option.

BIOS Support for Int 13h Extensions

When enabled, the SCSI BIOS supports El Torito Int 13h extensions, which are required for bootable CD-ROMs. You can disable this option if the boot device is not a CD-ROM; however, leaving it enabled causes no harm.

Support for UltraSCSI Speed

Enable the UltraSCSI speed option to use fast SCSI speeds with the PENT/CPCI-721.

6

Maps and Registers

Overview

This section gives an overview on the I/O and memory maps and describes all PENT/CPCI-721 specific registers.

Table 13: *Register Overview*

Register	Description
Base Board LED Control Register	page 6-17
ENUM# Interrupt Control Status Register CPCI-Bus A	page 6-10
ENUM# Interrupt Control Status Register CPCI-Bus B	page 6-8
Hot Swap I^2C Register CPCI-Bus A	page 6-11
Hot Swap I^2C Register CPCI-Bus B	page 6-9
I^2C Register	page 6-7
I/O Board LED Control Register	page 6-18
Lock/Unlock Register	page 6-6
NMI Status Register	page 6-16
PCI Bus Control Register	page 6-15
Switch and Interrupt Control Register	page 6-12
Watchdog Control and Retrigger Registers	page 6-13 and page 6-14

I/O and Memory Maps

The following section gives an overview over the I/O and memory maps of the PENT/CPCI-721.

Table 14: *I/O Map*

I/O Address	Device		
	EIDE, PCI-to-ISA bridge, USB: Intel 82371SB		
		Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy	
0000_{16}...$001F_{16}$	x		DMA controller 1
0020_{16}...$003F_{16}$	x		Interrupt controller 1
0040_{16}...$005F_{16}$	x		Counter and timer
0060_{16}		x	Keyboard controller
0061_{16}	x		NMI status and control
0064_{16}		x	Keyboard controller
0070_{16}...0071_{16}		x	RTC and NMI mask
0080_{16}...$009F_{16}$	x		DMA page register
0110_{16}...0113_{16}		(x)	PENT/CPCI-721 specific registers (partially implemented in separate PLD)
$00A0_{16}$...$00BF_{16}$	x		Interrupt controller 2
$00C0_{16}$...$00DF_{16}$	x		DMA controller 2
$00E0_{16}$...$00FF_{16}$	n.a.		Coprocessor
0170_{16}...0177_{16}	x		Secondary EIDE / ATAPI
$01F0_{16}$...$01F7_{16}$	x		Primary EIDE / ATAPI
$02F8_{16}$...$02FF_{16}$		x	COM2
$03BC_{16}$...$03BF_{16}$		x	LPT1
$03C0_{16}$...$03DA_{16}$	n.a.		Graphic controller
$03F2_{16}$...$03F7_{16}$		x	Floppy-EIDE / ATAPI
$03F8_{16}$...$03FF_{16}$		x	COM1

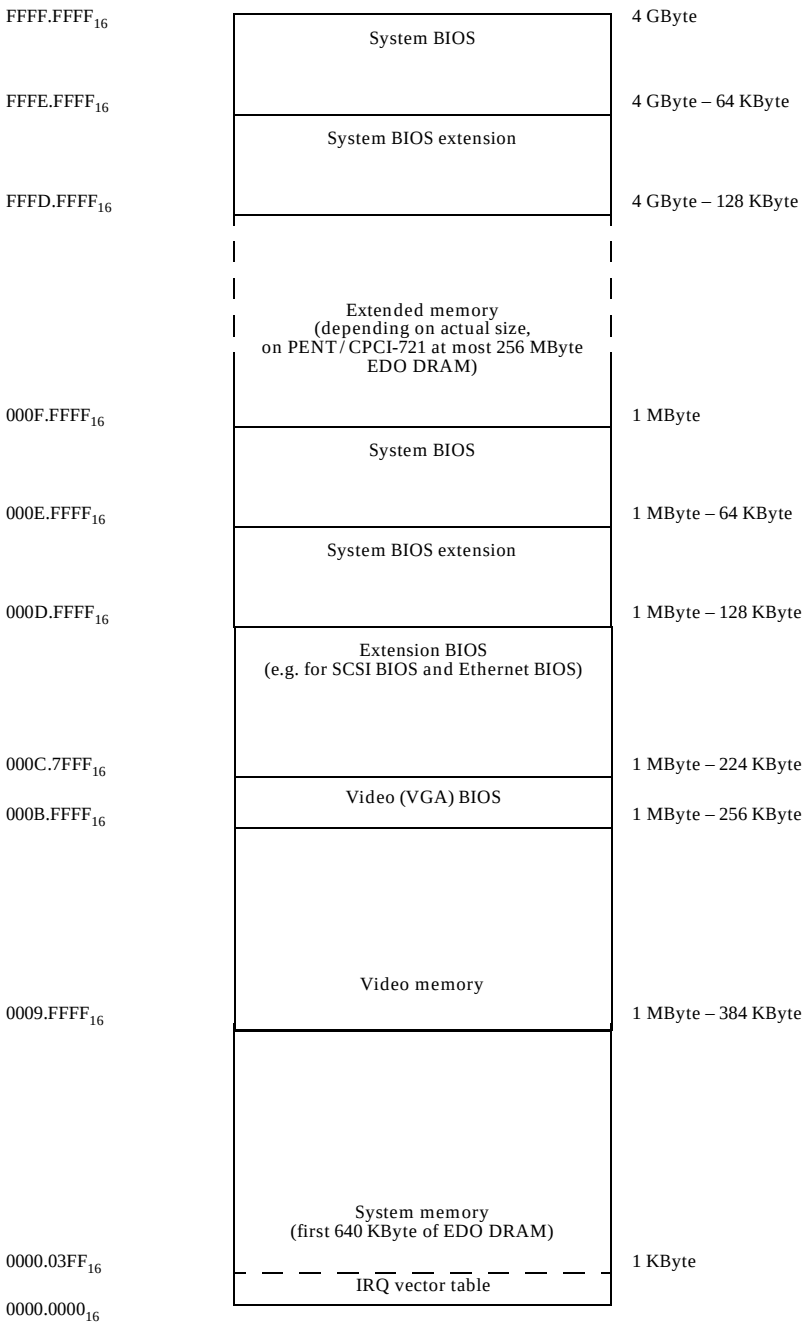


Figure 32: *Memory Map*

PENT/CPCI-720/2/3 Registers

The following section gives an overview of the board-specific registers.

Lock/Unlock Register

The Lock / Unlock register enables or disables read and write access to the PENT / CPCI-720 / 2 / 3 specific registers.

Table 15: *Lock/Unlock Register*

Address: $010E_{16}$				
Bit	**Value**	**Description**	**Access**	**Settings**
2...0	B2...B0	B2...B0 specifies whether the PENT / CPCI-720 / 2 / 3-specific registers are unlocked or locked	r / w	$=010_2$ unlocked $\neq 010_2$(default)
3	Reserved	Reserved	r	Undefined

I^2C Register

The I^2C register is used for data transfer settings on the I^2C bus and provides access to the program-readable vintage registers for the base board, the I/O board, the lower and upper memory modules, the VGA-IO720 as well as the registers controlling the configuration of the temperature sensors.

Table 16: *I^2C Register*

Address: 0108_{16}				
Bit	**Value**	**Description**	**Access**	**Settings**
0	DIR	Direction bit for I^2C data	r/w	=0 Data is written to the data line. =1 (default) Data is read from the data line.
1	CLK	Clock line of the I^2C bus	r/w	=0 Clock line is low. =1 (default) Clock line is high.
2	DATA_IN	Stores the current value of the data line.	r	=0 Data line is low. =1 Data line is high.
3	Reserved	Reserved	5	Undefined

ENUM# Interrupt Control Register CPCI Bus B

The ENUM register is used to detect the assertion of the hot swap ENUM signal. The ENUM signal can either be polled via the register or an enumeration can cause an interrupt on level 5, 9, 10, or 11 (factory option).

Note: This function is supported starting from PCB revision 1.0.

Table 17: *ENUM# Interrupt Control Status Register B*

Address: 0110_{16}				
Bit	**Values**	**Description**	**Access**	**Settings**
0	ENUM	Shows the logic level of the ENUM signal at the CompactPCI backplane.	r	=0 Signal is asserted. =1 (default) ENUM is not asserted.
1	MASK	Masks the ENUM interrupt.	r / w	= 0 (default) The ENUM interrupt is masked and no interrupts will occur. = 1 The ENUM interrupt is unmasked and an interrupt will occur if the ENUM signal on the CompactPCI backplane is asserted.
2	IRQ	Shows status of interrupt line.	r	= 0 (default) No ENUM interrupt is pending. = 1 The ENUM interrupt line has been asserted and is still active.
3	Reserved	Reserved	r	Undefined

Hot Swap I²C Register CPCI Bus B

The I²C register is used for data transfer between the CPCI-720 and a hot-swap controller on the backplane. The geographical address line GA[3] is used as the CLK line. The geographical address line GA[4] is used as the DIR and DATA_IN line.

Note: This function is supported starting from PCB revision 1.0.

Table 18: *Hot Swap I²C Register B*

Address: 0111_{16}				
Bit	**Value**	**Description**	**Access**	**Settings**
0	DIR	Specifies direction of data transfer.	r / w	= 0 Data is written to the data line. = 1 (default) Data is read from the data line.
1	CLK	Clock line of the I²C bus	r / w	
2	DATA_IN	Stores current value of data line.	r	
3	EN	Enables line drivers and pull-up resistors of the hot swap I²C bus.	r / w	= 0 (default) The line drivers are tristated and the pull-up resistors are disabled. All register bits can still be written or read. =1 The line drivers and pull-up resistors are enabled.

ENUM# Interrupt Control Status Register CPCI Bus A

The ENUM register is used to detect the assertion of the hot-swap ENUM signal. The ENUM signal can either be polled via the register or an enumeration can cause an interrupt on level 11.

Table 19: *ENUM# Interrupt Control Status Register A*

Address: 0112_{16}				
Bit	**Value**	**Description**	**Access**	**Settings**
0	ENUM	Shows logic level of ENUM signal at the CompactPCI backplane.	r	= 0 ENUM signal is asserted. = 1 (default) ENUM is not asserted.
1	MASK	Masks the ENUM interrupt.	r / w	= 0 (default) The ENUM interrupt is masked and no interrupts will occur. = 1 The ENUM interrupt is unmasked and an interrupt will occur if the ENUM signal on the CompactPCI backplane is asserted.
2	IRQ	Shows the status of the interrupt line.	r	= 0 (default) No ENUM interrupt is pending. = 1 The ENUM interrupt line has been asserted and is still active.
3	Reserved			Undefined

Hot Swap I^2C Register CPCI Bus A

The I^2C register is used for data transfer between the PENT/CPCI-720/2/3 and a hot-swap controller on the backplane. The geographical address line GA[3] is used as the CLK line. The geographical address line GA[4] is used as the DIR and DATA_IN line.

Table 20: *Hot Swap I^2C Register A*

Address: 0113_{16}				
Bit	**Value**	**Description**	**Access**	**Settings**
0	DIR	Specifies direction of data transfer.	r/w	= 0 Data is written to the data line. = 1 (default) Data is read from the data line.
1	CLK	Clock line of the I^2C bus	r/w	
2	DATA_IN	Stores current value of data line.	r	
3	EN	Enables line drivers and pull-up resistors of the hot swap I^2C bus.	r/w	= 0 (default) The line drivers are tristated and the pull-up resistors are disabled. All register bits can still be written or read. =1 The line drivers and pull-up resistors are enabled.

Switch and Interrupt Control Register

The Switch and Interrupt Control register specifies switch and interrupt related settings.

Table 21: *Switch and Interrupt Control Register*

Address: 0109_{16}				
Bit	**Value**	**Description**	**Access**	**Settings**
0	SW_RESET	SW_RESET and SW0100C control whether the reset key is enabled or disabled.	r / w	= 0 Reset key disabled. = 1 (default) Reset key enabled, if SW0100C = OFF.
1	SW_ABORT	SW_ABORT and SW0100D control whether the abort key is enabled or disabled.	r / w	= 0 Abort key disabled. =1 (default) Abort key enabled, if SW0100D = OFF.
2	TEMP	Controls whether an NMI is caused when passing a predefined upper limit temperature value at the temperature sensor 0 below the CPU. The trigger value can be set via the I^2C Register.	r / w	=1 (default) No action is caused when passing the temperature value. = 0 An NMI is caused when passing the temperature value.
3	Reserved			

Watchdog Control and Retrigger Register

The Watchdog Control and Retrigger register specifies watchdog related settings. The watchdog time-out value is fixed to approximately 1.5 s.

Table 22: *Watchdog Control Register*

Address: 010A$_{16}$				
Bit	**Value**	**Description**	**Access**	**Settings**
0	WDOG_ON	Controls whether the watchdog timer is enabled or disabled.	r / w	= 0 Watchdog timer is enabled. = 1 (default) Watchdog timer is disabled.
1	WDOG_RESET / NMI	Controls whether an NMI or a reset is caused when the watchdog timer is not retriggered within the time-out period.	r / w	= 0 An NMI is caused. =1 (default) A reset is caused. For information whether the reset is local or global, see the RESET_BUS (r / w) bit in the PCI Bus Control Register.
2	WDOG_HW / SW	Controls whether the watchdog timer has to be retriggered by software or by hardware.	r / w	= 0 Software control mode: The watchdog timer has to be retriggered by software using the WDOG_RETR (w) bit in the Watchdog Retrigger Register. = 1 (default) Hardware control mode: The PENT / CPCI-721 retriggers the watchdog timer.
3	Reserved		r	Undefined

Note: WDOG_HW/SW must be 0 if no hardware watchdog is implemented. The hardware watchdog is a factory option.

Table 23: *Watchdog Retrigger Register*

Address: $010D_{16}$				
Bit	**Value**	**Description**	**Access**	**Settings**
0	WDOG_RETR	Retriggers watchdog timer when watchdog is in software control mode.	w	
1	Reserved		r	Undefined
2	Reserved		r	Undefined
3	Reserved		r	Undefined

PCI Bus Control Register

Table 24: *PCI Bus Control Register*

Address: $010B_{16}$				
Bit	**Value**	**Description**	**Access**	**Settings**
0		Controls whether a reset stays local to the PENT/CPCI-721 or is routed globally to the CompactPCI system.	r/w	= 0 Only a local reset is caused. =1 (default) A global reset is caused.
1	Reserved		r	Undefined
2	Reserved		r	Undefined
3	Reserved		r	Undefined

Note: In case of the PENT/CPCI-720/2/3 the term 'global' refers to all segments the PENT/CPCI-720/2/3 is connected to.

NMI Status Register

The NMI Status register indicates the device which caused an NMI and enables clearing all of its status bits via a write access to the register.

Table 25: *NMI Status Register*

Address: $010C_{16}$				
Bit	**Value**	**Description**	**Access**	**Settings**
0	TEMP	Indicates whether temperature sensor 0 below the CPU caused an NMI since the last clearance of the status bits via a write access to the register.	r	=0 (default) No NMI has been caused. =1 Temperature sensor 0 caused an NMI.
1	WDOG	Indicates whether the watchdog timer caused an NMI since the last clearance of the status bits via a write access to the register.	r	=0 (default) No NMI has been caused. =1 The watchdog timer caused an NMI.
2	CLEAR	Write access sets TEMP and WDOG bits to 0.	w	
3	ECC	Indicates whether an unrecoverable ECC error was detected in the EDO DRAM causing an NMI since the last clearance of the status bits via a write access to the register.	r	=0 (default) No NMI has been caused. =1 An unrecoverable ECC error caused an NMI.

Base Board LED Control Register

The LED Control register specifies the status of the LEDs.

Table 26: *Base Board LED Control Register*

Address: 0100_{16}				
Bit	**Values**	**Description**	**Access**	**Settings**
0	1_LEDSTAT	Specifies status of the user LED *x* for *x* = 1, 2, 3 on the Base-721 front panel.	r / w	$= 00_2$ Off $=01_2$ Red $=10_2$ (default) Green other values reserved
1				
2	2_LEDSTAT			
3				
4	HD_LEDSTAT			$= 01_2$ Red $=10_2$ (default) Green other values reserved
5				
6	3_LEDSTAT	Specifies status of the user LED *x* for *x* = 1, 2, 3 on the Base-721 front panel.	r / w	$= 00_2$ Off $= 01_2$ Red $=10_2$ (default) Green other values reserved
7				

I/O Board LED Control Register

The I/O board LED control register is implemented on-board the I/O board via the General Purpose I/O register (GPIO) of the PCI-to-PCI-bridge. The PCI-to-PCI-bridge with device number 19_{10} (IDSEL 30_{10}) is located at PCI bus 0. The GPIO is integrated in the PCI configuration space of this PCI-to-PCI-bridge at offset 64_{16}. It controls the status of the I/O board front panel user LED.
The front panel LED 4 of the I/O board is connected to GPIO3 of the PCI-to-PCI-bridge on-board the I/O board.

Note: The bits denoted as 'x' in the following values must remain unaltered.

LED Off

To switch off the user LED, set the GPIO register to the following value via a 32-bit write access (from left to right 67_{16} to 64_{16}):
xxxx.xxxx.0001.0000.0000.0001.xxxx.xxxx$_2$

LED Green

To switch on the user LED, set the GPIO register to the following value via a 32-bit write access (from left to right 67_{16} to 64_{16}):
xxxx.xxxx.0000.0001.0000.0001.xxxx.xxxx$_2$

Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

☞ Send this report to the nearest Force Computers headquarter listed on the address page.

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