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SPARC/CPCI-52x(G)
Installation Guide

P/N 208913 Revision AB
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Using This Manual

This section does not provide information on the product, but on standard features of the manual itself:

- its structure,
- special layout conventions,
- and related documents.

Audience of the Manual and Overview of the Manual

This *Installation Guide* is intended for hard- and software developers as well as support and service engineers installing the SPARC/CPCI-52x(G). It is packaged and shipped together with the product.

This *Installation Guide* includes the installation instructions for powering up the SPARC/CPCI-52x(G), in detail:

- safety notes, see section 1 “Safety Notes” on page 1
- a mechanical overview of the product, its safety note and initialization prerequisites and requirements see section 3 “Installation” on page 9
- the default configuration of the base board, for example, the default switch setting and the connector pinouts see section 4 “Base-520(G) Installation” on page 19
- the default configuration of the I/O-board, for example, the default switch setting and the connector pinouts see section 5 “I/O-52x(G) Installation” on page 51

The installation instructions are also published in the product’s *Technical Reference Manual* – a separate manual delivered as separate price list item. The *Technical Reference Manual* includes additionally:

- an overview of the product, its specification and ordering information
- a detailed hardware description
- the data sheets of SPARC/CPCI-52x(G) components that are relevant for configuring and integrating the board in systems
- a detailed software description

Publication History of the Manual

Table a History of manual publication

Ed./Rev.	Date	Description
1.0	Feb/1998	First print
2.0	Dec/1998	Thoroughly revised, extended memory module and audio description and extended battery safety note Added descriptions for installing Solaris
3.0	Mar/1999	Battery maintenance safety note changed SPARC/MEM-50-5 information added SMART Service information added Solaris installation updated Maximum power supply values for SPARC/CPCI-520/mm-33-4-2 added
4.0	October 1999	Section “Safety Notes” included, Solaris versions for required software packages specified, maximum power supply data revised
5.0/AA	August 2001	Section “Sicherheitshinweise” added, editorial changes
AB	November 2001	Updated title page and address page, added copyright page, editorial changes

Fonts, Notations and Conventions

Table b **Fonts, notations and conventions**

Notation	Description
	All numbers are decimal numbers except when used with the following notations:
0000.0000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
0000_{8}	Same for octal numbers (digits are 0 through 7)
0000_{2}	Same for binary numbers (digits are 0 and 1)
`Program`	Typical character format used for names, values, and the like. It is used to indicate when to type literally the same word. Also used for on-screen output.
Variable	Typical character format for words that represent a part of a command, a programming statement, or the like, and that will be replaced by an applicable value when actually applied.

Table c **Product naming conventions**

Used Name	Description
SPARC/CPCI-52x(G)	General name for all available product configurations
Base-520(G)	General name for all available base board configurations
Base-520G	Name for base board with UPA64S slot
Base-520	Name for base board with 1 slot front panel
I/O-52x(G)	General name for all available I/O-board configurations
I/O-52xG	General name for I/O-board configurations, G stands for an additional slot
I/O-522(G)	General name for peripheral slot I/O-board
I/O-523G	Name for system slot I/O-board with second CompactPCI interface

Icons for Ease of Use: Safety Notes

The following 3 types of safety notes appear in this manual. Be sure to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

Danger



Dangerous situation: serious injuries to people or severe damage to objects.

Caution



Possibly dangerous situation: slight injuries to people or damage to objects possible.

Note: **No danger encountered. Pay attention to important information marked using this layout.**



1 Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the SPARC/CPCI-52x(G). For your protection, follow all warnings and instructions found in the following text.

General notes

This *Installation Guide* provides the necessary information to install and handle the SPARC/CPCI-52x(G). As the product is complex and its usage manifold, we do not guarantee that the given information is complete. In case you need additional information, ask your Force Computers representative.

The SPARC/CPCI-52x(G) has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or qualified persons in electronics or electrical engineering are authorized to install, uninstall or maintain the SPARC/CPCI-52x(G). The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing the board, check section 3.1.1 “Requirements” on page 12.**
- **Before touching integrated circuits, ensure that you are working in an electrostatic-free environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling the board, read section 3 “Installation” on page 9.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**



- **Ensure that the board is connected to the CompactPCI backplane via both the J1 and the J2 connectors and that power is available on both CompactPCI connectors.**

Operation

- **While operating the board ensure that the power and environmental requirements as given in table 1 “Maximum power supply values without UPA64S card and PMC modules” on page 13 and table 2 “Environmental requirements of the SPARC/CPCI-52x(G)” on page 13 are met.**
- **When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the CompactPCI rack and shielded by closed housing.**

EMC

- **If boards are integrated into open systems, always cover empty slots.**

Expansion

- **Check the total power consumption of all components installed (see the technical specification of the respective components). For the total power consumption of the SPARC/CPCI-52x(G), see table 1 “Maximum power supply values without UPA64S card and PMC modules” on page 13.**
- **Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).**
- **Only replace components or system parts with those recommended by Force Computers. In case you use components other than those recommended by Force Computers, you are fully responsible for the impact on EMI and the eventually changed functionality of the product.**

Battery change

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**

Protect your environment

Always dispose used batteries and/or old boards according to your country’s legislation.



RJ-45 connector

An RJ-45 connector is available on the board. Take into account that the RJ-45 connector type is used for telephone connectors and for twisted pair Ethernet (TPE) connectors. Note that mismatching these 2 connectors may destroy your telephone as well as your SPARC/CPCI-52x(G). Therefore:

- **Make sure that TPE connectors near your working area are clearly marked as network connectors.**
- **Make sure that TPE bushing of the system is connected only to safety extra low voltage (SELV) circuits.**
- **Verify that the length of the electric cable connected to a TPE bushing does not exceed 1 kilometer outside the building.**
- **If in doubt, ask your system administrator.**



2 Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, welche bei der Installation, dem Betrieb und der Wartung des SPARC/CPCI-52x(G) zu beachten sind. Beachten Sie zu Ihrem Schutz alle folgenden Warnhinweise und Anleitungen.

Dieses Installationshandbuch enthält alle notwendigen Informationen zur Installation und zum Betrieb des SPARC/CPCI-52x(G). Da es sich um ein komplexes Produkt mit einer aufwendigen Bedienung handelt, kann keine Garantie dafür übernommen werden, dass die enthaltenen Informationen vollständig sind. Für weitere Informationen wenden Sie sich bitte an Ihren Vertreter der Firma Force Computers.

Das SPARC/CPCI-52x(G) erfüllt die gültigen industriellen Sicherheitsanforderungen. Dieses Produkt darf ausschließlich für Anwendungen innerhalb der Telekommunikationsindustrie und der industriellen Steuerung verwendet werden.

Lediglich von Force Computers eingewiesene oder im Bereich Elektrotechnik oder Elektronik qualifizierte Personen sind zur Installation, zum Betrieb und zur Wartung dieses Produktes befugt. Die in dieser Dokumentation enthaltenen Informationen sollen lediglich als Hilfestellung für entsprechend qualifiziertes Fachpersonal dienen. Keinesfalls können sie dieses ersetzen.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Lesen Sie vor Einbau oder Ausbau des Boards den Abschnitt 3.1.1 “Requirements” auf Seite 12.**
- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie beim Einbau oder Ausbau des Boards nicht auf das Front Panel, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor Einbau oder Ausbau des Boards den Abschnitt 3 “Installation” auf Seite 9.**
- **Lesen Sie vor dem Einbau oder Ausbau von zusätzlichen Geräten oder Modulen das jeweilige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die CompactPCI Backplane angeschlossen ist und Strom an allen Power Pins anliegt.**



Betrieb

Während des Betriebs müssen die Umgebungs- und die Stromsversorgungsbedingungen gewährleistet sein.

Wenn das Board in Gebieten mit starker elektromagnetischer Strahlung betrieben wird, stellen Sie sicher, dass das Board auf dem Compact PCI Rack verschraubt ist und mit einem Gehäuse geschützt ist.

EMV

Werden Boards in offene Systeme eingebaut, müssen freie Steckplätze mit einer Blende abgeschirmt werden.

Erweiterung

Beachten Sie den Gesamtstromverbrauch aller installierter Komponenten (siehe technische Daten der entsprechenden Komponente).

Vergewissern Sie sich, daß jeder individuelle Ausgangsstrom jedes Stromverbrauchers innerhalb der zulässigen Grenzwerte liegt (siehe technische Daten des entsprechenden Verbrauchers).

Benutzen Sie bei der Erweiterung ausschließlich von Force Computers empfohlene Komponenten und Systemteile. Ansonsten sind Sie für die Auswirkungen auf EMV und die möglicherweise geänderte Funktionalität des Produktes verantwortlich.

Batterie

Muss eine Lithium Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium Batterien kann zu lebens-gefährlichen Explosionen führen.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**

Umwelt-schutz

Alte Batterien und/oder Boards oder Systeme müssen stets gemäß der in Ihrem Land gültigen Gesetzgebung entsorgt werden.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:



- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**



3 Installation

This section describes the SPARC/CPCI-52x(G) variants you may purchase from FORCE COMPUTERS. It is intended to get an overview over all possible configurations with named components which will help to find the information necessary for your configuration in this manual.

How to begin installation

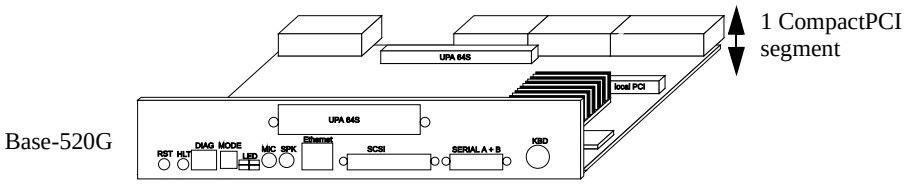
First read the Safety Notes and the Installation Prerequisites and Requirements (see section 1 “Safety Notes” on page 1 and section 3.1 “Installation Prerequisites and Requirements” on page 12).
Then go through the Base-520(G) installation section and the I/O-52x(G) installation section, depending on the variant you have purchased from FORCE COMPUTERS (see section 4 “Base-520(G) Installation” on page 19 and see section 5 “I/O-52x(G) Installation” on page 51).

SPARC/ CPCI-52x(G) variants

There are 4 variants available:

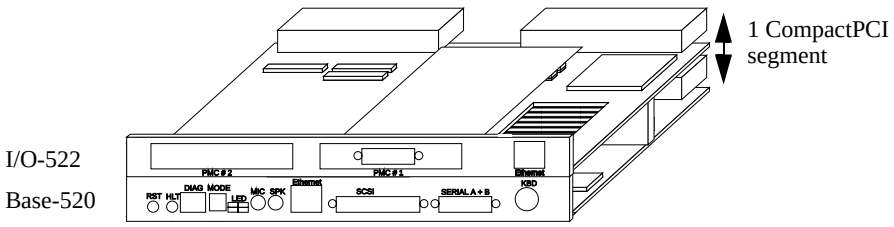
- a SPARC/CPCI-520G
  obtaining the 2 slot high base board with UPA64S card option named in this manual as Base-520G (or in general as Base-520(G)).

Figure 1 SPARC/CPCI-520G (schematic view)



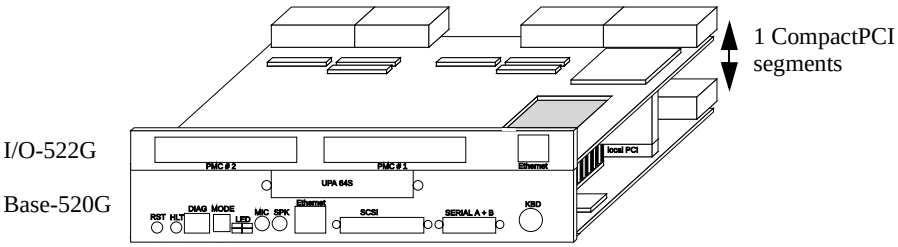
- a SPARC/CPCI-522
  obtaining the 1 slot Base-520 with the peripheral slot I/O-522.

Figure 2 SPARC/CPCI-522 (schematic view)



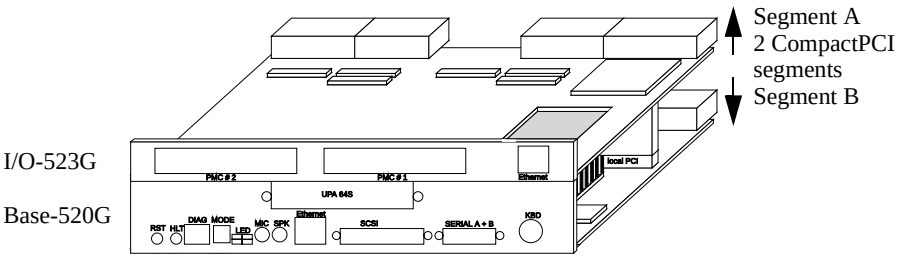
- a SPARC/CPCI-522G
  obtaining the 2 slot base board with UPA64S card option (Base-520G) and with the peripheral slot I/O-522G.

Figure 3 SPARC/CPCI-522G (schematic view)



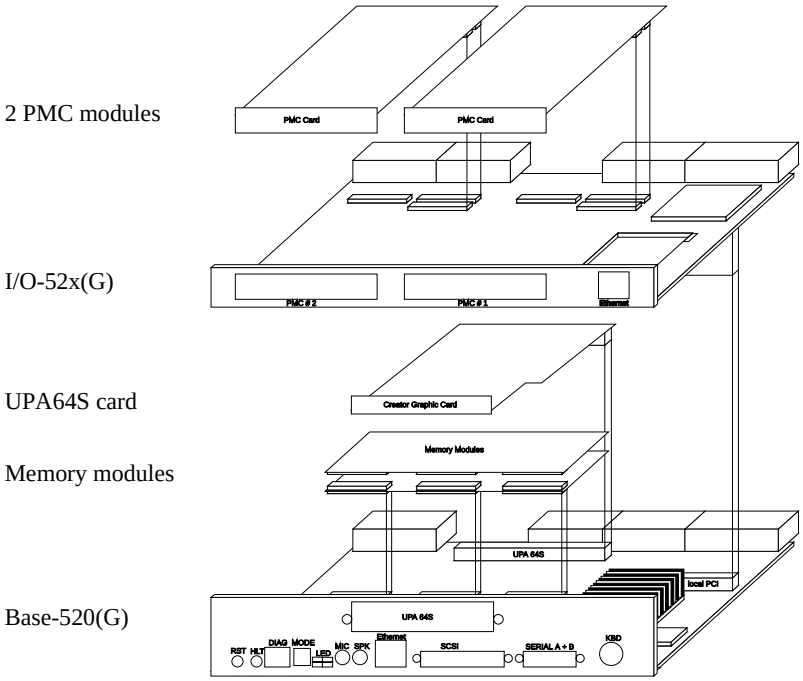
- and a SPARC/CPCI-523G
  which is a dual-segment CompactPCI variant obtaining the 2 slot base board with UPA64S card option (Base-520G) and with the system slot I/O-523G. The dual-segment variant is designed for CompactPCI systems with a backplane consisting of 2 CompactPCI bus segments.

Figure 4 SPARC/CPCI-523G (schematic view)



The following figure is intended to get an overview over all available main components of a SPARC/CPCI-52x(G).

Figure 5 **Schematic exploded mechanical construction view**



Caution



The SPARC/CPCI-52x(G) is a sytem board. According to the *CompactPCI Specification PICMG 2.0 R2.1*, the front panel of the SPARC/CPCI-52x(G) shows a triangle. To ensure proper functioning of the board, plug it exclusively in a system slot marked by a triangle.

Danger



The Lithium battery of the RTC/NVRAM provides a data retention of at least 7 years summing up all periods of actual battery use. Therefore FORCE COMPUTERS assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.
Please observe the following:

- **Exchange the battery before 7 years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is already installed.**

- **Use appropriate tools to remove the battery.**
- **When installing the new battery ensure that the marked dot on top of the battery covers the dot marked on the chip.**
- **Used batteries have to be disposed according to your country's legislation.**

3.1 Installation Prerequisites and Requirements

Caution



Before powering up check:

- **this section for installation prerequisites and requirements**
- **and the consistency of the current switch setting (see section 4.4 "Switch Settings" on page 25).**

3.1.1 Requirements

The installation requires at least

- a power supply
- a minimum airflow meeting the thermal requirements,
- and free CompactPCI backplane slots due to your SPARC/CPCI-52x(G) variant:
  - a system CompactPCI bus slot for the Base-520(G)
  - an additional system CompactPCI bus slot for the IO-523G on the right side of the Base-520(G)
  - an additional system or peripheral CompactPCI bus slot for the IO-522(G) on the right side of the Base-520(G).

Peripheral slot — A peripheral slot of a CompactPCI rack is marked by a circle.

System slot — A system slot of a CompactPCI rack is marked by a triangle.

Signaling level — The SPARC/CPCI-52x(G) is a CompactPCI-universal board operational in 3.3 V or 5 V CompactPCI systems. Therefore, no voltage keys are provided on the CompactPCI interface.

Power supply — The power supply must meet the specifications given in the following table. The values in the table below are maximum values without an UPA64S card installed and without PMC modules.

Table 1 Maximum power supply values without UPA64S card and PMC modules

CPU board	+5 V	+3.3 V	+/-12 V	V I/O
SPARC/CPCI-520	6.5 A	4.6 A	not required	200 mA
SPARC/CPCI-520G	6.5 A	4.6 A	not required	200 mA
SPARC/CPCI-522	7.8 A	5.6 A	not required	200 mA
SPARC/CPCI-522G	7.8 A	5.6 A	not required	200 mA
SPARC/CPCI-523G	7.8 A	5.6 A	not required	400 mA
Creator Graphic Card	1.3 A	2.2 A	not required	not required

Thermal requirements

The operating temperature is 0 ×C to +55 ×C (humidity 5 % to 95 % noncondensing at +40 ×C), when operating the SPARC/CPCI-52x(G) in systems providing a minimum forced airflow of 300 LFM (linear feet per minute). The typical operating temperature of the system is 0 °C to +40 °C.

Table 2 Environmental requirements of the SPARC/CPCI-52x(G)

	Operating	Non-operating
Temperature	0 °C to +55 °C	–40 °C to +85 °C
Forced air flow	300 LFM (linear feet per minute)	–
Temp. change	+/– 0.5 °C/min	+/– 1 °C/min
Rel. humidity	5 % to 95 % noncondensing at +40 °C	5 % to 95 % noncondensing at +40 °C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m

Audio interfaces

Simultaneous use of the audio interfaces available on the front panel and on the backplane can damage on-board hardware or connected devices. For example: never use the headphone/line audio output at the backplane, if a headphone is plugged into the front-panel jack.

- Always use at most one of the interfaces if an audio interface is available on both the front panel and the backplane.

Table 3 Audio interfaces requirements

Interface	Description
Stereo Micro In (op-amp pre-amp with 18 dB gain)	• Signal level: single-ended condensator microphones with signal level –up to 12 mV with 20 dB gain inside Codec enabled –and up to 120 mV with 20 dB gain inside Codec disabled • Availability: on front panel and as factory option on backplane instead of Aux#2 In
Stereo Head-phone/ Line Out	• Signal level: maximum 2 V_{RMS} line-level signal output (also designed to directly drive headphones) • Availability: on front panel and on backplane
Stereo Line In	• Signal level: typical 47 kΩ audio input impedance; maximum full scale input of 2 V_{RM} • Availability: on backplane
Stereo Aux#1 In	• Signal level: ~10 kΩ input impedance; maximum full scale input of 2 V_{RMS} • Availability: on backplane
Stereo Aux#2 In	• Signal level: ~10 kΩ input impedance; maximum full scale input of 2 V_{RMS} • Availability: on backplane
Mono In	• Signal level: typical 47 kΩ audio input impedance; nominally 1 V_{RMS} maximum (centered around 2.1 V) input signal level • Availability: as factory option on front panel instead of Micro In and as factory option on backplane instead of Aux#1 In
Mono Out	• Signal level depends on the setting of `OLB` which is a bit in the Codecs Alternate Feature Enable I register (I16) –maximum 1 V_{RMS} output (centered around 2.1 V) if `OLB` = `1` –or maximum 0.707 V_{RMS} (centered around 2.1 V) if `OLB` = `0` Default is `OLB` = `0`. • Availability: as factory option on backplane instead of Head-phone/Line Out

3.1.2 Memory Modules

The main memory capacity is adjustable via installation of the appropriate memory modules.
The qualified memory modules depend on the SPARC/CPCI-52x(G) processor frequency. They are given in the following table.

Table 4 Qualified memory modules

Processor frequency	Memory modules
up to 300 MHz	SPARC/MEM-50x
	SPARC/MEM-50x-5
333 MHz and above	SPARC/MEM-50x-5

Caution



Do not install SPARC/MEM-50x and SPARC/MEM-50x-5 memory modules on the same board, otherwise system malfunction may occur.

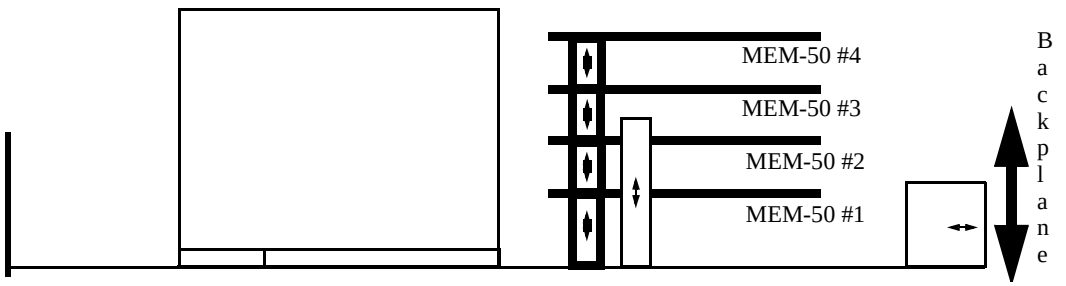
In the following it will be refered to all memory module types as SPARC/MEM-50x.
The Base-520(G) can hold 1 to 4 memory modules providing up to 1 GByte DRAM capacity. 1 memory module can carry 2 memory banks.

Note: **At least 1 lower memory module MEM-50L is required.**

See the following figure for the memory module numbering scheme:

- Memory modules #1 and #2 are located in the first CompactPCI slot the SPARC/CPCI-52x(G) occupies.
- Memory modules #3 and #4 are located in the second CompactPCI slot the SPARC/CPCI-52x(G) occupies.

Figure 6 MEM-50 – memory module numbering scheme



The memory configuration is adjustable to the application's needs via selection of the appropriate memory modules. The memory configuration must fulfill the following requirements:

- The lowest memory module (#1) must be a SPARC/MEM-50L – which is a lower memory module.
- The top memory module (with the greatest number in your configuration given the number scheme in the figure above) can be a SPARC/MEM-50M or SPARC/MEM-50U – which is a middle (M) or upper (U) memory module. The upper module misses the connectors for another memory module to be stacked on top.
- The memory modules between the lowest and the top memory module must be SPARC/MEM-50M, i.e. middle memory modules.
- If a UPA64S card is installed, at most 2 memory modules can be installed and memory module #2 must be a SPARC/MEM-50U, i.e. an upper memory module.
- Note the limitations given by the SPARC/CPCI-52x(G) configuration under consideration (see section 4.2 "Mechanical Construction" on page 21).

Out of the extensive list of possible configurations the following memory module configurations have been qualified (others may be tested and qualified on request):

Table 5 Qualified memory configurations (all data in MByte)

Total capacity	**32**	**64**	**128**	**256**	**384**	**512**	**768**	**1024**
Mem. module #4	–	–	–	–	–	–	–	256
Mem. module #3	–	–	–	–	–	–	256	256
Mem. module #2	–	–	–	–	128	256	256	256
Mem. module #1	32	64	128	256	256	256	256	256

For installation information see the respective *Installation Guide* delivered together with the memory module.

3.1.3 Solaris Installation

When installing Solaris, there are some general installation guidelines to be followed before and during Solaris installation and a specific guideline related to SCSI to be followed after Solaris installation (see "SCSI" on page 18).

General Installation Guidelines

Note: **Solaris versions and hardware updates prior to 2.5.1 11/97 and 2.6 03/98 are not supported.**

Required software packages

In case of Solaris 2.5.1 and Solaris 2.6 the following Solaris software packages must be installed, otherwise Solaris fails to boot.

Table 6 **Required Solaris Packages**

Package	Description
`SUNWvplr.u`	SMCC sun4u new platform links
`SUNWvplu.u`	SMCC sun4u new usr/platform links

When setting up Solaris interactively, these packages can be installed by selecting the proper software group in the `Software` dialog. Customize the software groups as follows:

Table 7 **Customizing Solaris**

	Customization required for	
Software Group	**Solaris 2.5.1**	**Solaris 2.6**
Entire distribution plus OEM support	No customization is required	
Entire distribution	Select the following clusters: • SMCC platform links	
Developer system support		
End user system support		
Core system support		

SCSI

The Solaris SCSI driver may revert Wide-SCSI devices, which are connected to the front-panel SCSI connector, to asynchronous mode. However, it is possible to operate such a configuration in synchronous mode also by inserting the following line into `/kernel/drv/glm.conf`:

`target`*`n`*`-scsi-options=0x5f8`

where n is the SCSI ID of the Wide-SCSI device under consideration. In case of several Wide-SCSI devices insert the respective line per device. Terminate the file with a `";"`.

3.1.4 Terminal connection

The SPARC/CPCI-52x(G) provides 2 serial interfaces (A and B) which are implemented on the Base-520(G). For the initial power up, a terminal can be connected to interface A via the front-panel 26-pin-MicroD-Sub connector SERIAL A+B. Per default, all serial I/O interfaces provide an RS-232 interface. As factory option the 2 interfaces can be configured as RS-422 interface.
For information on the serial interface connector pinout, see section 4.5.4 “Serial I/O Interface Connector Pinout” on page 32.

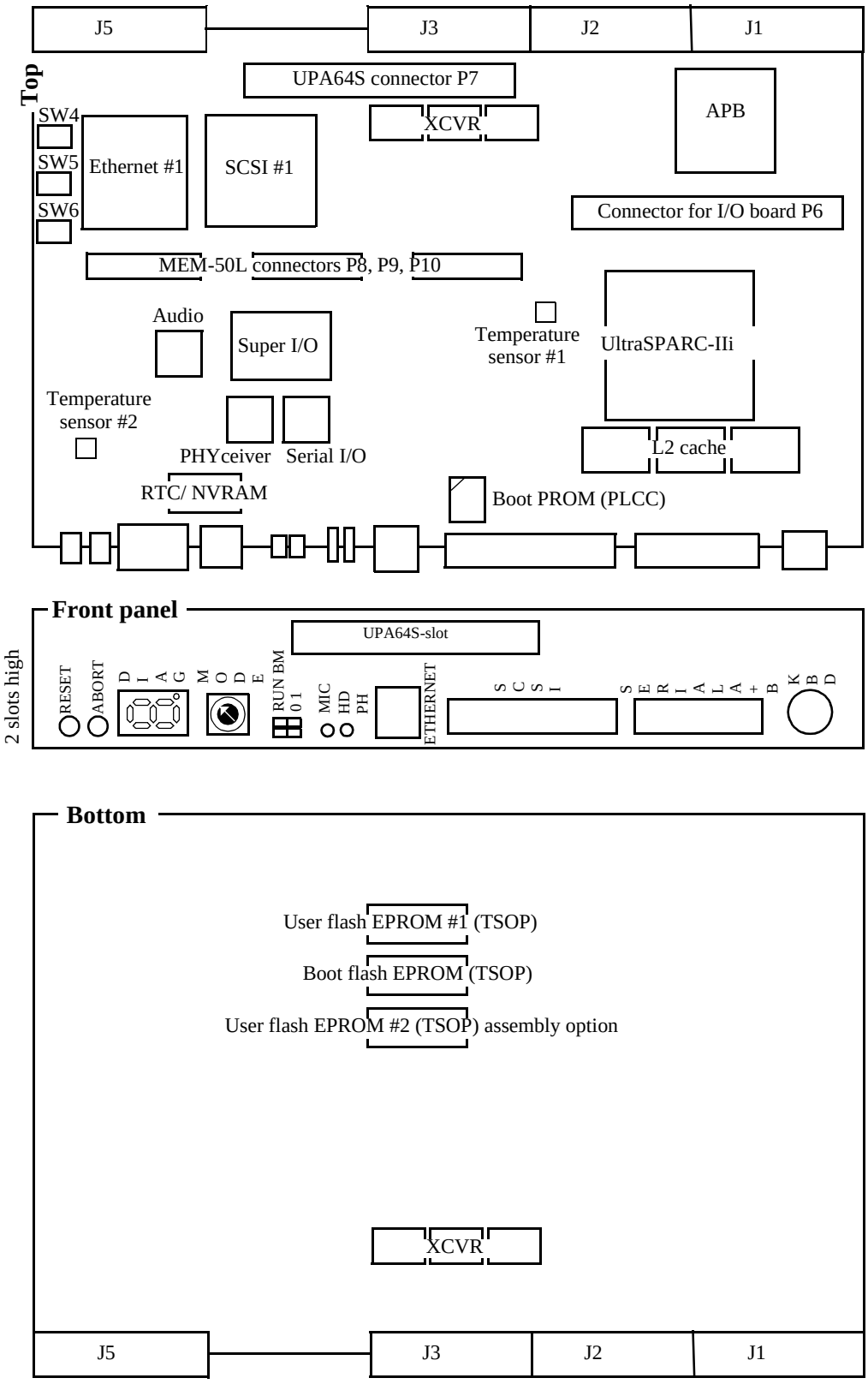
4 Base-520(G) Installation

4.1 Location Overview

The Base-520(G) contains the following main components:

- a UltraSPARC-IIi processor,
- a second level cache (L2 cache),
- a CompactPCI interface,
- a boot PROM (PLCC),
- a boot flash EPROM (TSOP) and an user flash EPROM (TSOP),
- 3 connectors for the memory modules,
- a connector for interfacing to a UPA64S card,
- a connector for interfacing to the I/O-52x(G),
- switches,
- temperature sensors,
- and the following I/O interfaces: SCSI #1, Ethernet #1, floppy, keyboard and mouse, audio, parallel interface as well as the 2 serial interfaces A+B.

Figure 7 Location diagram of the Base-520(G) (schematic)



4.2 Mechanical Construction

The Base-520(G) is a CompactPCI computer. It occupies 2 CompactPCI slots and consists of the following major components:

- an I/O connector for the I/O-52x(G),
- an UPA64S connector for an UPA64S card (only Base-520G),
- 3 memory module connectors for up to 4 memory modules. With an installed UPA64S card only 2 memory modules are possible.

The following figures show the Base-520(G) in possible configurations:

Figure 8 Mechanical construction of a Base-520G

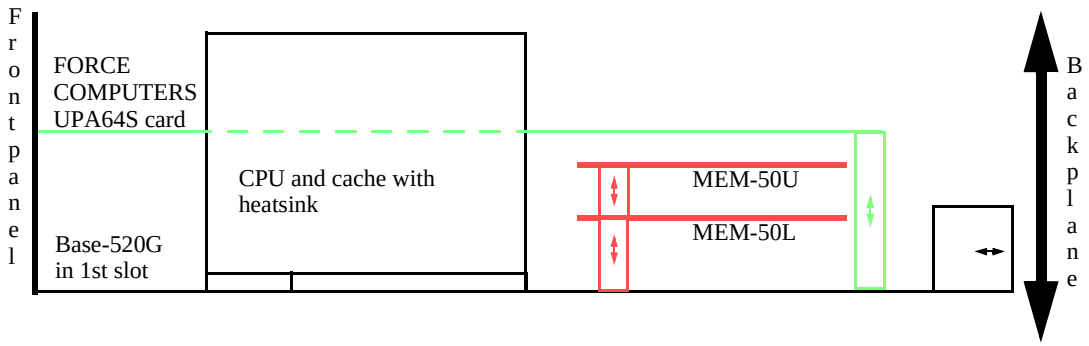


Figure 9 Mechanical construction of a Base-520G with 4 memory modules

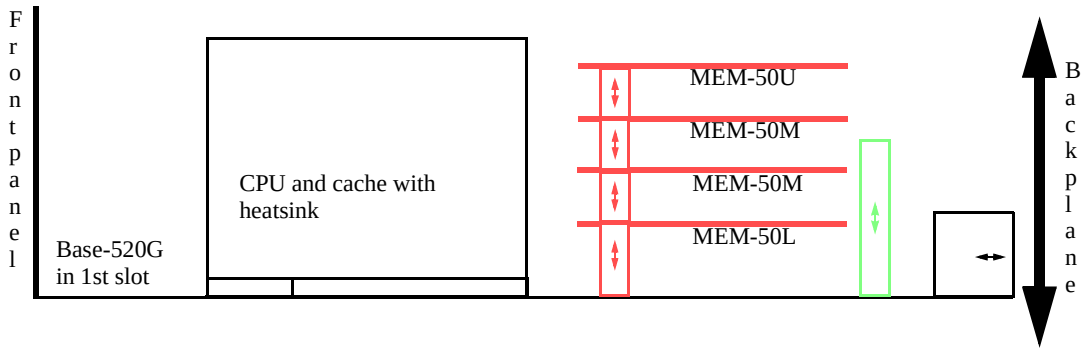
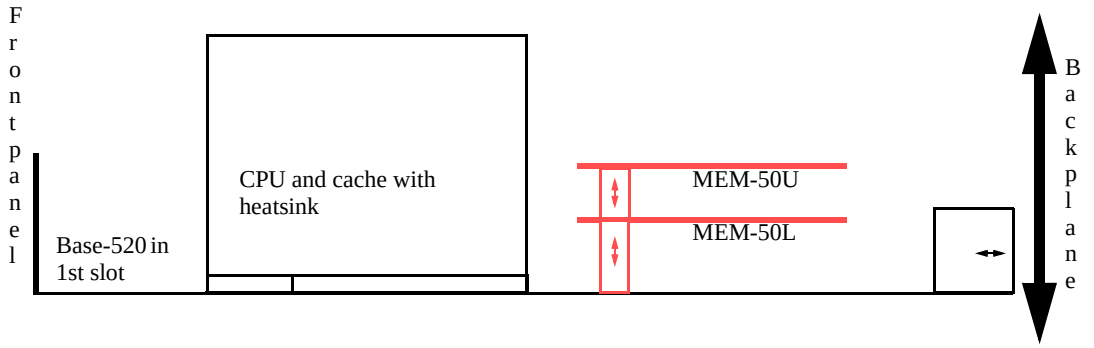


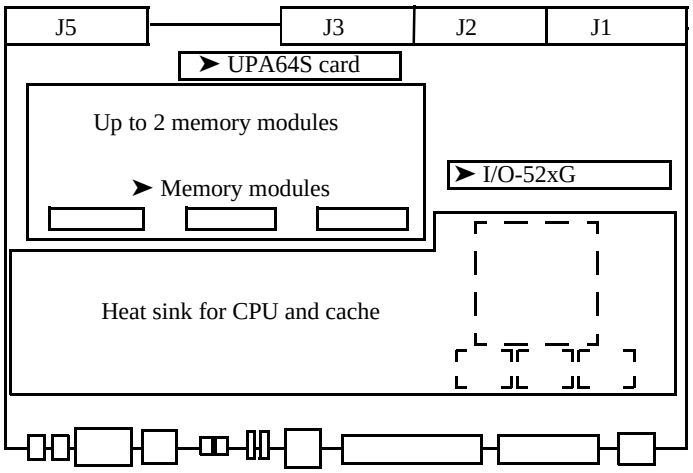
Figure 10 Mechanical construction of a Base-520



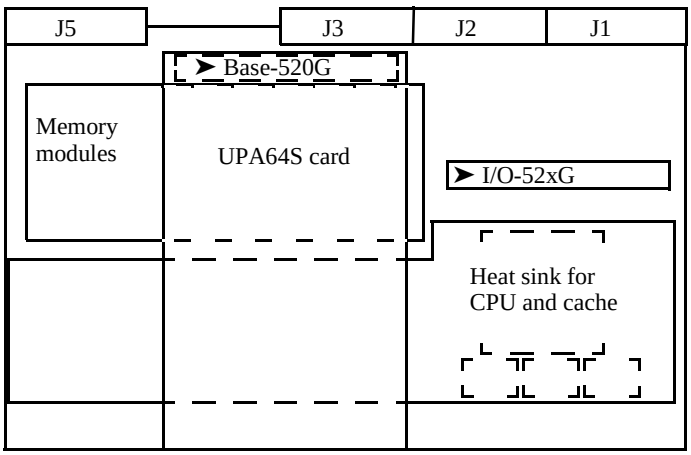
The Base-520 is only available as a 2-slot solution with an I/O-522.

Figure 11 Components of a 2-slot configuration with UPA64S card (schematic)

1st of 2 slots Base-520G with up to 2 memory modules



2nd of 2 slots UPA64S card



4.2.1 FORCE COMPUTERS UPA64S Card Installation

You can only install a FORCE COMPUTERS UPA64S card if you purchased a SPARC/CPCI-52xG version. It is connected to the Base-520G via the UPA64S connector P7 (see figure 7 “Location diagram of the Base-520(G) (schematic)” on page 20).

Note: **Use only UPA64S cards from FORCE COMPUTERS. Throughout this section the term “UPA64S card” always refers to a card purchased from FORCE COMPUTERS and specified for use with a SPARC/CPCI-52xG.**

For the locations mentioned in the description see figure 12 “Installing/Deinstalling an UPA64S card” on page 24.

Installation of a UPA64S card

1. If an I/O-52xG is installed, remove it as described in the I/O-52x(G) installation section. Remove the 2 z-standoffs at location 5 and 6 from the Base-520G by loosing the respective 2 screws. Keep them in a save place to have them available for reusing the I/O-52xG without UPA64S card.
2. If you do not install an I/O-52xG afterwards: Remove the 2 z-standoffs fixed on the UPA64S card by loosing the respective 2 screws and fix the UPA64S card again with 2 of the 4 shorter screws delivered with the UPA64S card on the 2 standoffs which connect it to the Base-520G.
3. Remove the blind panel fixed in the UPA64S front panel slot. Store it in a safe place for later use.
4. Plug the prepared UPA64S card from FORCE COMPUTERS to the respective UPA64S connector on the Base-520G.
5. Fix the UPA64S card with 2 of the 4 short screws at location 5 and 6 on the bottom side of the Base-520G and with the 4 screws and 2 nuts from the blind panel on the front panel at location 1...4.

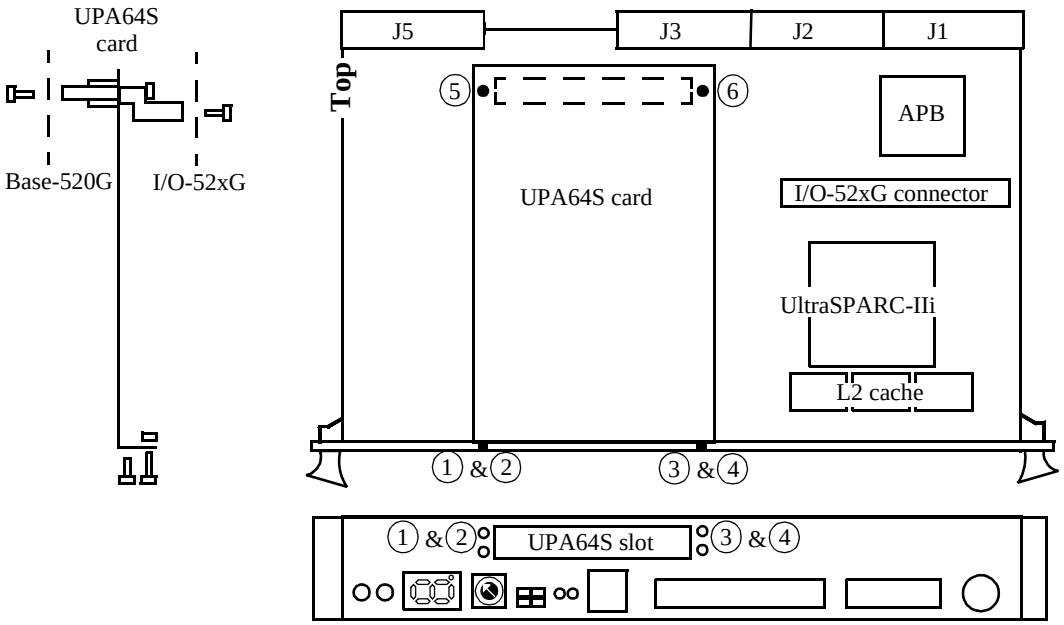
   Now the UPA64S card is installed.
6. If an I/O-52xG was installed, fix it again as described in the I/O-52x(G) installation section.

Uninstalling a UPA64S card

1. If an I/O-52xG is installed, remove it as described in the I/O-52x(G) installation section.
2. Remove the 4 screws and 2 nuts on the front panel at location 1...4. Remove the 2 screws at location 5 and 6 on the bottom side of the Base-520G.
3. Remove the UPA64S card by lifting it.

4. If you do not install the UPA64S card again, fix the blind panel.
5. To install the I/O-52xG again refer to the installation section of the I/O-52x(G).

Figure 12 Installing/Deinstalling an UPA64S card



4.3 Powering Up

The initial powering up can be done by connecting a terminal to the front panel serial I/O interface A. The advantage of using a terminal is that you do not need any frame buffer, monitor, or keyboard for initial powering up.

Booting

The SPARC/CPCI-52x(G) boot PROM consists of a 1 MByte PROM (OTP) PLCC socket device (not writeable). Alternatively a 2 MByte TSOP boot flash EPROM device can be enabled by SW6-2. This boot flash EPROM device is writeable if enabled by SW4-3.

Note: **If you have an unformatted floppy disk in a floppy connected to your SPARC/CPCI-52x(G) then the OpenBoot does not come up.**

Per default the SPARC/CPCI-52x(G) is shipped with its boot PROM containing the OpenBoot firmware (see section 4.8 “OpenBoot Firmware” on page 40).

User application

The SPARC/CPCI-52x(G) provides 1 user flash EPROM devices (2M*8) to store user applications. As factory option 2 user flash EPROM devices (2M*8) are possible. For write-protection of the user flash EPROM see SW4-4 in section 4.4 “Switch Settings” on page 25.

4.4 Switch Settings

The following table lists the functions and the default settings of all switches shown in figure 7 “Location diagram of the Base-520(G) (schematic)” on page 20.

Note: **Before powering up the board check the current switch settings for consistency. Do not switch during operation.**

Table 8 Default switch settings

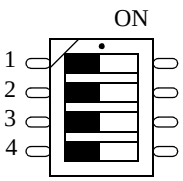
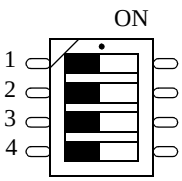
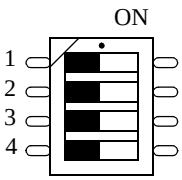
Name and default setting		**Function**
	SW4-1 OFF	Reset key on front-panel control OFF = RESET key enabled ON = RESET key disabled
	SW4-2 OFF	Abort key control OFF = ABORT key enabled ON = ABORT key disabled
	SW4-3 OFF	Boot flash EPROM write protection (only relevant if SW6-2 = ON) OFF = boot flash EPROM write protected ON = boot flash EPROM write enabled
	SW4-4 OFF	User flash EPROM write protection OFF = user flash EPROM write protected ON = user flash EPROM write enabled

Table 8 Default switch settings (cont.)

Name and default setting		Function
	SW5-1 OFF	SCSI termination for SCSI #1 on front panel OFF = front panel termination automatic ON = front panel termination disabled
	SW5-2 OFF	SCSI termination for SCSI #1 on backplane OFF = backplane termination disabled ON = backplane termination enabled
	SW5-3 OFF	Reserved, must be OFF
	SW5-4 OFF	Reserved, must be OFF
	SW6-1 OFF	Reserved, must be OFF
	SW6-2 OFF	Select boot device OFF = boot from boot PROM ON = boot from boot flash EPROM
	SW6-3 OFF	Reserved, must be OFF
	SW6-4 OFF	Watchdog enable switch OFF = disabled ON = enabled

4.5 Front Panel and Connectors

Front panel features

The features of the front panel are described in the following table. For a location diagram see figure 7 “Location diagram of the Base-520(G) (schematic)” on page 20.

Table 9 Front panel features

Device	Description
RESET	Mechanical reset key: When enabled and toggled it instantaneously affects the SPARC/CPCI-52x(G) by generating a push-button Power On Reset (POR) to the UltraSPARC-IIi. Push-button Power On Reset has the same effect as a Power On Reset from the power supply, with the only difference, that the corresponding status bit (`B_POR`) in the UltraSPARC-IIi `Reset_Control` Register is set and the DRAM refresh is not influenced. For information on disabling the reset key, see “SW4-1” on page 25.
ABORT	Mechanical abort key: When enabled and toggled it instantaneously affects the SPARC/CPCI-52x(G) by generating a push-button external initiated reset (XIR). Push-button external initiated reset allows a user-reset (abort) of part of the processor without resetting the whole system. UltraSPARC-IIi sets the `B_XIR` bit in the `Reset_Control` Register when a push-button external initiated reset is detected. For information on disabling the abort key, see “SW4-2” on page 25.
DIAG	Software programmable hexadecimal display for diagnostics.
MODE	Hexadecimal rotary switch, decoded with 4 bit. Default setting: F_{16}.
RUN	CPU status LED: green normal operation red the processor is halted or reset is active; it starts blinking to signal that the processor did not access the PCI bus for more than 1 second.
BM	CompactPCI busmaster LED: green if the SPARC/CPCI-52x(G) accesses the CompactPCI as master off otherwise

Table 9 **Front panel features (cont.)**

Device	Description
0, 1	2 software programmable user LEDs. Possible status: off, red, yellow, or green, all colors either permanent or with a blinking frequency of approximately 0.5, 1, or 2 Hz.
MIC	Standard 3.5 mm microphone jack
HDPH	Standard 3.5 mm headphone jack
ETHERNET	Standard Twisted-Pair-Ethernet RJ45 connector for 10BaseT/100BaseTX Ethernet.
SCSI	50-pin shielded fine-pitch connector for standard SCSI
SERIAL A+B	26-pin shielded fine-pitch connector for 2 serial interfaces
KBD	Standard 8-pin mini-DIN connector for keyboard and mouse

On-board connectors

In addition to the front-panel connectors, the Base-520(G) provides on-board connectors for memory modules and for the I/O-52x(G), only the Base-520G provides the UPA64S interface connector. An overview of the on-board connectors is shown in the following table.

Table 10 **On-board connectors**

Connector description and location	Connector type
CompactPCI backplane connector J1, J2, J5	Standard CompactPCI metric, 5 row shielded connectors female
I/O-52x(G) connector P6	100-pin MBus connector male
UPA64S interface connector P7	120-pin UPA connector female
Memory module connectors P8, P9, P10	80-pin SMD connector

Available interfaces on J5

The following list shows the available interfaces on the J5 backplane connector. For the J5 connector pinout see Figure 13, “CompactPCI J5 connector pinout,” on page 34.

- Ultra Wide SCSI #1
- MII #1 Ethernet interface

- Floppy interface
- Parallel interface
- Serial interface A and B
- Keyboard and mouse
- Audio In:

  Stereo Line In,

  Stereo Aux#1 In,

  Stereo Aux#2 In (or Microphone In as factory option)
- Audio Out:

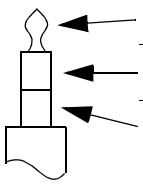
  Stereo Line Out

4.5.1 Audio Interface

The 2 front panel audio interfaces use standard 3.5-mm-phono jacks supporting

- 1 single-ended condenser microphone
- 1 line level signal output, also designed to directly drive low impedance headphones

Table 11 Audio interface signals

Connector		**Headphone**	**Microphone**
	Tip	Left channel	
	Ring	Right channel	
	Shield	Analog GND	

4.5.2 Ethernet Interfaces

The full duplex Ethernet interface is available at the front panel via a 10BaseT/100BaseTx Twisted-Pair-Ethernet connector.

Table 12 Twisted-Pair-Ethernet #1 connector pinout

Connector	Pin	Signal
RJ-45 TPE 	1	TX+
	2	TX–
	3	RX+
	4	GND
	5	GND
	6	RX–
	7	GND
	8	GND

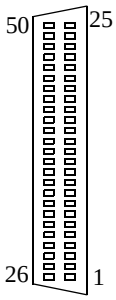
The Ethernet #1 interface is also accessible at the J5 back panel connector via an MII #1 interface. If Ethernet #1 gets accessed via I/O panel, the front panel connector is normally disabled automatically, for other configurations see the respective jumper settings in the *SPARC/IOBP-520 Installation Guide*. For the J5 connector pinout see Figure 13, “Compact-PCI J5 connector pinout,” on page 34.

4.5.3 SCSI #1 Connector Pinout

TERMPWR The SCSI #1 interface is single-ended and supports TERMPWR.

AUTOTERM Automatic termination mode means the respective termination is disabled when you connect a standard SCSI cable to the front panel connector.

Table 13 50-pin SCSI connector pinout

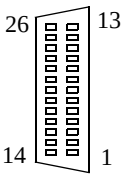
Signal	Pin	Connector	Pin	Signal
GND	1		26	D0
GND	2		27	D1
GND	3		28	D2
GND	4		29	D3
GND	5		30	D4
GND	6		31	D5
GND	7		32	D6
GND	8		33	D7
GND	9		34	DP0
GND	10		35	GND
GND	11		36	AUTOTERM
n.c.	12		37	n.c.
n.c.	13		38	TERMPWR
n.c.	14		39	n.c.
GND	15		40	GND
GND	16		41	ATN
GND	17		42	GND
GND	18		43	BSY
GND	19		44	ACK
GND	20		45	RST
GND	21		46	MSG
GND	22		47	SEL
GND	23		48	CD
GND	24		49	REQ
GND	25		50	IO

4.5.4 Serial I/O Interface Connector Pinout

Both serial I/O interfaces of the Base-520(G) are independent full-duplex channels. For each of them the 4 signals RXD, TXD, RTS, and CTS are also provided via the respective CompactPCI J5 connector (for interface A and B see figure 13 “CompactPCI J5 connector pinout” on page 34).

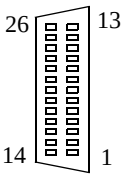
SERIAL A+B on the Base-520(G)’s front panel holds the signals for the 2 serial interfaces A and B.

Table 14 26-pin serial A+B connector pinout RS232

Signal	Pin	Connector	Pin	Signal
n.c.	1		14	TxD_B (Output)
TxD_A (Output)	2		15	RxC_A (Input)
RxD_A (Input)	3		16	RxD_B (Input)
RTS_A (Output)	4		17	RTxC_A (Input)
CTS_A (Input)	5		18	RxC_B (Input)
DSR_A (Input)	6		19	RTS_B (Output)
GND_A (Ground)	7		20	DTR_A (Output)
DCD_A (Input)	8		21	DSR_B (Input)
n.c.	9		22	RTxC_B (Input)
n.c.	10		23	GND_B (Ground)
DTR_B (Output)	11		24	TxC_A (Output)
DCD_B (Input)	12		25	TxC_B (Output)
CTS_B (Input)	13		26	n.c.

SERIAL A+B on the Base-520(G)’s front panel holds the signals for the 2 serial interfaces A and B.

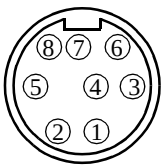
Table 15 **26-pin serial A+B connector pinout RS422 (factory option)**

Signal	Pin	Connector	Pin	Signal
n.c.	1		14	CTS+_B (Input))
CTS+_A (Input))	2		15	nc
RTS–_A (Output)	3		16	RTS–_B (Output)
RTS+_A (Output)	4		17	nc
CTS–_A (Input)	5		18	nc
nc	6		19	RTS+_B (Output)
RxD–_A (Input)	7		20	RxD+_A (Input)
TxD–_A (Output)	8		21	nc
n.c.	9		22	nc
n.c.	10		23	RxD–_B (Input)
RxD+_B (Input)	11		24	TxD+_A (Output)
TxD–_B (Output)	12		25	TxD+_B (Output)
CTS–_B (Input)	13		26	n.c.

4.5.5 Keyboard/Mouse Connector

The SUN-type keyboard/mouse interface is available at the front panel via an 8-pin mini-DIN connector.

Table 16 **Keyboard/mouse connector pinout**

Connector	Pin	Function
	1	GND
	2	GND
	3	+5 V DC
	4	Mouse In
	5	Keyboard Out
	6	Keyboard In
	7	Mouse Out
	8	+5 V DC

4.5.6 CompactPCI Backplane Connector Pinout

J1 and J2

The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as specified by the CompactPCI Specification. Therefore, this section only documents the pinout of the J5 connector.

J3

J3 is reserved.

J5

Besides the CompactPCI specific pinout the following interfaces are available on the CompactPCI J5 connector (the names used in the following pinout is given in brackets):
SCSI (`SCSI`), MII (`MII`), parallel (`LPT`), floppy (`FDC`), serial interface A (`SerA`), serial interface B (`SerB`), audio (`AUD`), keyboard (`KBD`), mouse (`MSE`), fused 5 V power for the I/O panel (`VP5`).

The pinout shown in the figure below applies to RS-232 configuration of the Base-520(G)'s serial I/O interfaces. Serial I/O interfaces configured for RS-422 (factory option) are only available via the front panel connector.

Figure 13 CompactPCI J5 connector pinout

A	B	C		D	E
SCSI #1 D8	SCSI #1 D9	SCSI #1 D10	1	SCSI #1 D11	n.c.
SCSI #1 SEL	SCSI #1 CD	SCSI #1 REQ	2	SCSI #1 IO	WIDETERMPWR
SCSI #1 ATN	SCSI #1 BSY	SCSI #1 ACK	3	SCSI #1 RST	SCSI #1 MSG
SCSI #1 D4	SCSI #1 D5	SCSI #1 D6	4	SCSI #1 D7	TERMPWR
SCSI #1 D0	SCSI #1 D1	SCSI #1 D2	5	SCSI #1 D3	SCSI #1 DP0
SCSI #1 D12	SCSI #1 D13	SCSI #1 D14	6	SCSI #1 D15	SCSI #1 DP1
MII #1 RXD3	MII #1 RXD2	MII #1 RXD1	7	MII #1 RXD0	MII #1 RX_CLK
MII #1 RX_DV	MII #1 COL	MII #1 CRS	8	MII #1 RX_ER	MII #1 MGT_DIO
MII #1 TXD3	MII #1 TXD2	MII #1 TXD1	9	MII #1 TXD0	MII #1 TX_CLK
FDC HDSEL	FDC DSKCHG	MII #1 TX_EN	10	MII #1 TX_ER	MII #1 MGT_CLK
FDC WDATA	FDC WGATE	FDC TRK0	11	FDC WP	FDC RDATA
FDC DR0	FDC DR1	FDC MTR0	12	FDC DIR	FDC STEP
FDC EJECT	FDC DENSEL	FDC DSENS	13	FDC INDEX	VP5_IOBP
LPT BSY	LPT ERR	LPT SLIN	14	LPT INIT	n.c.
VP5_IOBP	LPT PE	LPT SLCT	15	LPT AFD	n.c.
LPT D4	LPT D5	LPT D6	16	LPT D7	LPT ACK
LPT D0	LPT D1	LPT D2	17	LPT D3	LPT STB
SerA RXD	SerA CTS	SerB DCD	18	SerB CTS	SerB RXD
SerA TXD	SerA RTS	SerA DCD	19	SerB RTS	SerB TXD
SerA DTR	KBD DOUT	KBD DIN	20	MSE DIN	SerB DTR
AUD RLINEIN	AUD RAUX2IN	AUD RAUX1IN	21	AUD ROUT	AUD MOUT
AUD LLINEIN	AUD LAUX2IN	AUD LAUX1IN	22	AUD LOUT	AUD AGND

Audio factory option

As factory option the following signals are routed to the mentioned pins instead of the signals mentioned in the connector pinout above:

- Pin 21 row C: AUD MIN (Mono In)
- Pin 21 row B: AUD RMICIN (Right Micro In)
- Pin 22 row B: AUD LMICIN (Left Micro In)

I/O panel

As a separate price list item an I/O panel is available for the Base-520(G), the SPARC/IOBP-520/CPU. An extended variant is the SPARC/CPCI-520/AccKit/CPU which contains additionally to the I/O panel the following cables:

–a serial splitter cable for the front panel and the I/O panel

–a flat ribbon SCSI cable for the I/O panel

–a Micro D-Sub SCSI cable for the front panel

–and a Twisted-Pair-Ethernet cable for the front panel or I/O panel.

The I/O panel supports the following interfaces:

- Fast/Wide SCSI #1,
- MII #1 Ethernet,
- Serial A/B interface,
- Audio interface,
- Keyboard/Mouse,
- Parallel interface,
- and Floppy interface.

Danger



The SPARC/IOBP-520/CPU and the SPARC/CPCI-520/AccKit/CPU is especially designed for the Base-520(G). Do not use any other I/O panels on the Base-520(G).
Use only the front panel or the backpanel Ethernet interface, not both. Check the configuration of your I/O panel.
All switches on the Base-520(G) concerning the SCSI-bus termination must be configured so, that the corresponding backplane terminator (SW5-2) is disabled! This is necessary as the I/O panel includes automatic termination for the backplane SCSI-bus.

4.6 SCSI #1 Configuration

Note: **Correct SCSI bus selection: The Base-520(G) provides 1 SCSI bus, SCSI #1. A further SCSI controller, SCSI #2, is available with the I/O-52x(G). Its termination is described in the I/O-52x(G) installation section.**

SCSI #1 termination

The Base-520(G)'s SCSI #1 bus is accessible via the Base-520(G)'s front-panel SCSI #1 connector (8-bit SCSI) and via the Base-520(G)'s J5 connector (Wide SCSI). Therefore, the Base-520(G) holds 2 distinct SCSI bus terminations to enable correct termination of the SCSI #1 bus. Associated to the 2 terminations there are 2 switches – SW5-1 and SW5-2 – which allow easy selection of a valid SCSI #1 bus configuration.

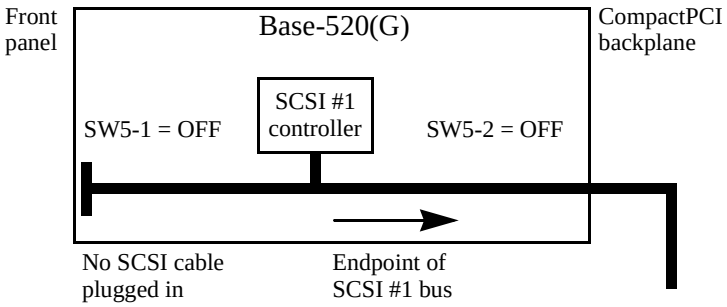
There are 4 valid Base-520(G) switch settings corresponding to valid SCSI #1 bus configurations. The following factors differentiate the valid SCSI #1 bus configurations:

- the Base-520(G)'s location within the SCSI #1 bus: Is the Base-520(G) located at an endpoint of the SCSI #1 bus?
- the connector(s) being used from the SCSI #1 bus:
  - Is a SCSI cable plugged into the Base-520(G)'s front-panel SCSI connector?
  - Is the Base-520(G)'s CompactPCI J5 connector used by the SCSI #1 bus?
  - Are both Base-520(G) connectors used by the SCSI #1 bus?
- the SCSI device type being connected to the SCSI #1 bus: Is a Wide-SCSI device connected to the J5 connector?

Each of the following configuration descriptions starts with identifying the SCSI #1 bus configuration being covered and ends with defining the correct switch setting corresponding to the configuration under consideration.

Default configuration 1 for 8 bit SCSI

- The default configuration 1 is covered by the default switch setting: The Base-520(G) is located at an endpoint of the SCSI #1 bus, the SCSI #1 bus is extended via the CompactPCI backplane (J5 connector), but no SCSI cable is plugged into the front-panel SCSI connector:



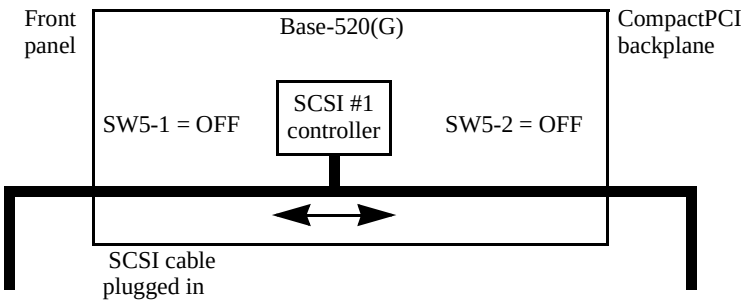
In this configuration (default switch setting):

– SW5-1 must be set to OFF = front panel termination automatic (automatic enabling or disabling of termination by sensing whether a SCSI cable is plugged in)

– and SW5-2 must be set to OFF = backplane termination disabled.

Default configuration 2 for 8 bit SCSI

- The default configuration 2 is also covered by the default switch setting: the Base-520(G) is not located at an endpoint of the SCSI #1 bus, the SCSI 1 bus is extended via the CompactPCI backplane and via the front-panel SCSI connector:



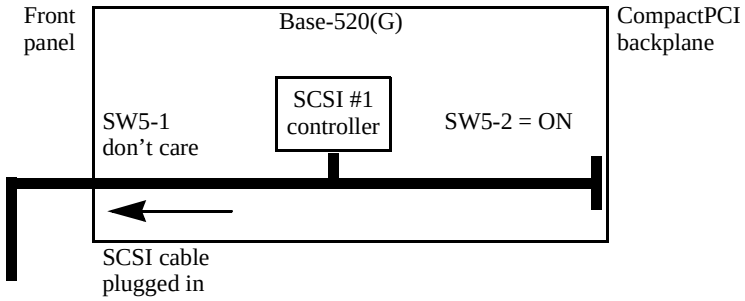
In this configuration (default switch setting):

– SW5-1 must be set to OFF = front panel termination automatic (automatic enabling or disabling of termination by sensing whether a SCSI cable is plugged in)

– and SW5-2 must be set to OFF = backplane termination disabled.

Alternative configuration for 8 bit SCSI

- Alternative configuration: the Base-520(G) is located at an endpoint of the SCSI #1 bus and the CompactPCI backplane is not used for SCSI #1 bus signalling, but the SCSI #1 bus is extended via the front panel connector:



In this configuration

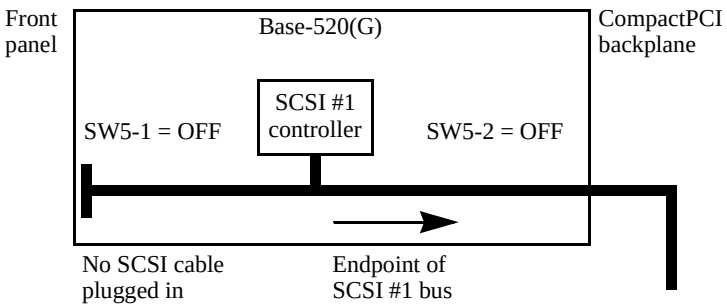
– both settings of SW5-1 are valid

– and SW5-2 must be set to ON = backplane termination enabled.

Default configuration for Wide SCSI

Wide SCSI is only available on the J5 connector of the CompactPCI backplane.

- The Wide SCSI configuration is covered by the default switch setting: The Base-520(G) is located at an endpoint of the SCSI #1 bus, the SCSI #1 bus is extended via the CompactPCI backplane, but no SCSI cable is plugged into the front-panel SCSI connector:



The Wide SCSI termination is always enabled and it is located near the SCSI #1 controller.

In this configuration (default switch setting):

– SW5-1 must be set to OFF = automatic enabling or disabling of termination by sensing whether a SCSI cable is plugged in,

– and SW5-2 must be set to OFF = backplane termination disabled.

4.7 Ethernet Address and Host ID

In order to see the Ethernet address and host ID, type the following command at the prompt:

```
ok banner
```

The information below explains how the SPARC/CPCI-52x(G) Ethernet address and the host ID are determined.

Figure 14 **The 48-bit (6-byte) Ethernet address**

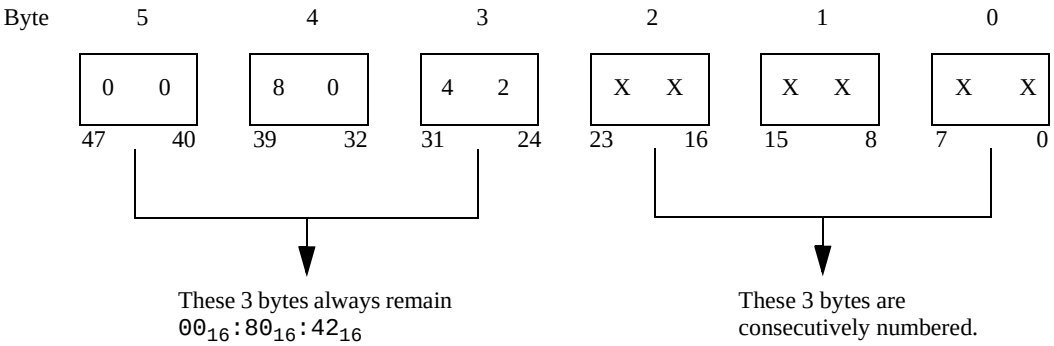
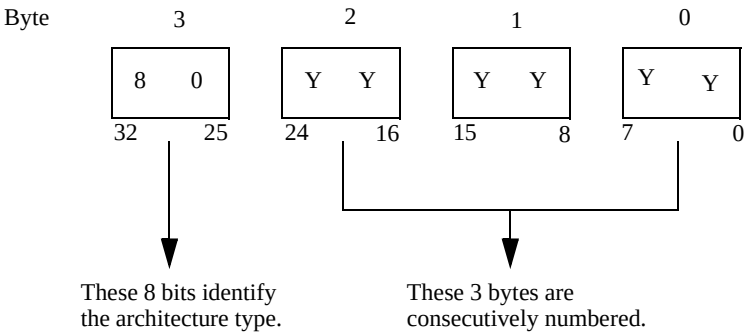


Figure 15 **The 32-bit (4-byte) host ID**



4.8 OpenBoot Firmware

This chapter describes the use of the OpenBoot firmware. The following tasks will be described in detail:

- Boot the system
- Run diagnostics
- Display system information
- Reset the system
- OpenBoot help

Note: **The examples in this section can differ from the appearance on your monitor according to your device tree (CPU architecture).**

For more information on the OpenBoot firmware see the *Open Boot 3.x Manual Set*.

The OpenBoot firmware is subject to changes. For newest version and how to upgrade refer to the SMART service accessible via the FORCE COMPUTERS World Wide Web site.

4.8.1 Boot the System

The most important function of OpenBoot firmware is the booting of the system. Booting is the process of loading and executing a stand-alone program such as the operating system. After it is powered on, the system usually boots automatically after it has passed the power-on self-test (POST). This occurs without user intervention.
If necessary, you can explicitly initiate the boot process from the Open-Boot command interpreter. Automatic booting uses the default boot device specified in nonvolatile RAM (NVRAM); user initiated booting uses either the default boot device or one specified by the user.
To boot the system from the default boot device, enter the following command at the Forth monitor prompt `ok`:

```
ok boot
```

The boot command has the following format:
`boot [`*`device-specifier`*`] [`*`filename`*`] [-`*`bootoption`*`]`

Optional Boot Parameters

Note: **These options are specific to the operating system and may differ from system to system.**

`[device-specifier]` The name (full path or alias) of the boot device. Typical values are `cdrom`, `disk`, `floppy`, `net`, or `tape`.

[*filename*] The name of the program to be booted. *`filename`* is relative to the root of the selected device. If no filename is specified, the boot command uses the value of *`boot-file`* NVRAM parameter. The NVRAM parameters used for booting are described in the following section.

[*-bootoption*] Boot option may be one of the following:

`[-a]` `-a` prompt interactively for the device and name of the boot file.

`[-h]` `-h` halt after loading the program.

`[-r]` `-r` reconfigure Solaris device drivers after changing the hardware configuration.

`[-v]` `-v` print verbose information during boot procedure.

Devices to Boot from

To explicitly boot from the internal disk using the Forth monitor enter:

```
ok boot disk
```

To retrieve a list of all device alias definitions, type `devalias` at the Forth Monitor command prompt. The following table lists some typical device aliases:

Table 17 Device alias definitions

Alias	Description
	Defined for SCSI
`scsi`	SCSI
`disk`	Default disk SCSI-target-ID 0
`disk6`	disk SCSI-target-ID 6
`disk5`	disk SCSI-target-ID 5
`disk4`	disk SCSI-target-ID 4
`disk3`	disk SCSI-target-ID 3
`disk2`	disk SCSI-target-ID 2
`disk1`	disk SCSI-target-ID 1
`disk0`	disk SCSI-target-ID 0
`tape (or tape0)`	1st tape drive SCSI-target-ID 4
`tape1`	2nd tape drive SCSI-target-ID 5
`cdrom`	CD-ROM partition f, SCSI-target-ID 6
	Defined for Ethernet
`net`	Ethernet
`floppy`	Floppy disk
`audio`	Audio
`keyboard`	Keyboard
`mouse`	Mouse
`ebus`	EBus2
`pcia`	secondary PCI bus A
`pcib`	secondary PCI bus B
`pci`	primary PCI bus
`flash-prog`	Flash EPROM programming mode
`flash`	Flash EPROM
`ttya`	Serial interface A
`ttyb`	Serial interface B

4.8.2 NVRAM Boot Parameters

The OpenBoot firmware holds its configuration parameters in NVRAM. At the Forth monitor prompt enter `printenv` to see a list of all available configuration parameters.

Note: **Per default the SPARC/CPCI-52x(G) boots the OS automatically. If not, ensure that the `auto-boot?` parameter is always set to `true`.**

To set parameters

The OpenBoot command `setenv` may be used to set specific parameters in the order below:
`setenv [`*`configuration_parameter`*`] [`*`value`*`]`

The configuration parameters in Table 2 are involved with the boot process.

Table 18 Setting configuration parameters

Parameter	Default value	Description
`auto-boot?`	`true`	If `true`, automatic booting after power on or reset
`boot-device`	`disk`	Device from which to boot
`boot-file`	`empty string`	File to boot
`diag-switch?`	`false`	If `true`, run in diagnostic mode
`diag-device`	`net`	Device from which to boot in diagnostic mode
`diag-file`	`empty string`	File to boot in diagnostic mode

When booting an operating system or another stand-alone program, and neither a boot device nor a filename is supplied, the `boot` command of the Forth monitor takes the omitted values from the NVRAM configuration parameters. If the parameter `diag-switch?` is `false`, `boot-device` and `boot-file` are used. Otherwise, the OpenBoot firmware uses `diag-device` and `diag-file` for booting.

4.8.3 Diagnostics

At Hardware Power On or Button Power On the OpenBoot firmware executes POST. The extent of certain tests executed within the POST depend on the state of the configuration parameter `diag-level`. The operator can choose between minimal or maximal testing by setting this configuration parameter to `min` or `max`. Furthermore an enhanced diagnostic menu is available if setting this parameter to `menu`. If the NVRAM con-

figuration parameter `diag-switch?` is `true` for each test, a message is displayed on a terminal connected to the serial I/O interface A. If the system does not work correctly, error messages are displayed which indicate the problem. After POST the OpenBoot firmware boots an operating system or enters the Forth monitor, if the NVRAM configuration parameter `auto-boot?` is `false`.
The Forth Monitor includes several diagnostic routines. These on-board tests let you check devices such as network controller, SCSI devices, floppy disk system, clock, keyboard and audio. User installed devices can be tested if their firmware includes a self-test routine.
The table below lists several diagnostic routines followed by examples for each of these routines:

Table 19 Diagnostic routines

Command	Description
`probe-scsi`	Identifies devices connected to the primary SCSI bus
`probe-scsi-all [`*`device-path`*`]`	Performs probe-SCSI on all SCSI buses installed in the system below the specified device tree node. If *`device-path`* is omitted, the root node is used.
`test` *`device-specifier`*	Executes the specified device's self-test method. *`device-specifier`* may be a device path name or a device alias. **Example:** • `test net` – test network connection
`test-all [`*`device-specifier`*`]`	Tests all devices that have a built-in self-test method and that reside below the specified device tree node. If *`device-path`* is omitted, the root node is used.
`watch-clock`	Monitors the clock function.
`watch-net-all`	Monitors network connection via all Ethernet interfaces installed in the system.
`watch-net`	Monitors network connection via primary Ethernet.

Examples:

SCSI bus

To check the SCSI #1 for connected devices enter:

```
ok probe-scsi
Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
ok
```

All SCSI buses

To check all the SCSI buses installed in the system enter the following (The actual response depends on the devices on the SCSI buses).:

```
ok probe-scsi-all
/pci@1f,0/scsi@2

Target 6
Unit 0 Disk Removable Read Only Device SONY CD-ROM CDU-8012 3.1a

/pci@1f/pci@4,1/scsi@2

Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
ok
```

Note: **The command `probe-scsi-all` can last up to 2 minutes without terminal message.**

Single device

To test a single installed device enter:

```
ok test device-specifier
```

This executes the `self-test` device method of the specified device node.
`device-specifier` may be a device path name or a device alias as described in Table 17, “Device alias definitions,” on page 43. The response depends on the self-test of the device node.

Group of devices

To test a group of installed devices enter:

```
ok test-all
```

All devices below the root node of the device tree are tested. The response depends on the devices having a self-test routine. If a device specifier option is supplied at the command line, all devices below the specified device tree node are tested.

Clock

To test the clock function enter:

```
ok watch-clock
Watching the ‘seconds’ register of the real time clock
chip.
It should be ‘ticking’ once a second.
Type any key to stop.
22
ok
```

The system responds by incrementing a number once a second. Press any key to stop the test.

Network

To monitor the network connection enter:

```
ok watch-net
Internal loopback test -- succeeded.
Transceiver check -- Using Onboard transceiver -- Link Up.
passed
Using Onboard transceiver -- Link Up.
Looking for Ethernet packets.
‘.’ is a good packet. ‘X’ is a bad packet.
Type any key to stop.
..........X.........................X.............
ok
```

The system monitors the network traffic, displaying a dot (`.`) each time it receives a valid packet and displaying an `X` each time it receives a packet with an error which can be detected by the network hardware interface.

4.8.4 Display System Information

The Forth monitor provides several commands to display system information. These commands let you display the system banner, the Ethernet address for the Ethernet controller, the contents of the ID PROM, and the version number of the OpenBoot firmware.
The ID PROM contains specific information to the individual machine, including the serial number, date of manufacture, and assigned Ethernet address.
The following table lists these commands:

Table 20 Commands to display system information

Command	Description
`banner`	Displays system banner
`show-pci-devs-all`	Displays list of installed and probed PCI Bus devices
`.enet-addr`	Displays the Ethernet address
`.idprom`	Displays ID PROM contents, formatted
`.traps`	Displays a list of SPARC trap types
`.version`	Displays version and date of the boot PROM
`show-devs`	Displays a list of all device tree nodes
`devalias`	Displays a list of all device aliases

4.8.5 Reset the System

If your system needs to be reset, you either press the reset button on the front panel or, if you are in the Forth Monitor, type **reset** on the command line.

```
ok reset
```

The system immediately begins executing the initialization procedures and executes the POST if having pressed the reset button. Then the system either boots automatically or enters the Forth Monitor, just as it would have done after a power-on cycle.

4.8.6 OpenBoot Help

The Forth Monitor contains an online help which can be activated by entering:

```
ok help
Enter ‘help command-name’ or ‘help category-name’ for more help
(Use ONLY the first word of a category description)
Examples: help select -or- help line
Main categories are:
Numeric output
Radix (number base conversions)
Arithmetic
Memory access
Line editor
System and boot configuration parameters
Select I/O devices
Floppy eject
Power on reset
Diag (diagnostic routines)
Resume execution
File download and boot
Nvramrc (making new commands permanent)
ok
```

A list of all available help categories is displayed. These categories may also contain subcategories. To get help for special Forth words or subcategories just type **`help [name]`**.

- The online help shows you the Forth word, the parameter stack before and after execution of the Forth word (before -- after), and a short description.
- The online help of the Forth monitor is located in the boot PROM, that means that there is not an online help for all Forth words.

Example:

How to get help for special Forth words or subcategories:

```
ok help power
reset-all         reset-machine, (simulates power cycling )
power-off         Power Off
ok
```

```
ok help memory
dump ( addr length -- ) display memory at addr for length bytes
fill ( addr length byte -- ) fill memory starting at addr with byte
move ( src dest length -- ) copy length bytes from src to dest address
map? ( vaddr -- ) show memory map information for the virtual address
x? ( addr -- ) display the 64-bit number from location addr
l? ( addr -- ) display the 32-bit number from location addr
w? ( addr -- ) display the 16-bit number from location addr
c? ( addr -- ) display the 8-bit number from location addr
x@ ( addr -- n ) place on the stack the 64-bit data at location addr
l@ ( addr -- n ) place on the stack the 32-bit data at location addr
w@ ( addr -- n ) place on the stack the 16-bit data at location addr
c@ ( addr -- n ) place on the stack the 8-bit data at location addr
x! ( n addr -- ) store the 64-bit value n at location addr
l! ( n addr -- ) store the 32-bit value n at location addr
w! ( n addr -- ) store the 16-bit value n at location addr
c! ( n addr -- ) store the 8-bit value n at location addr
ok
```

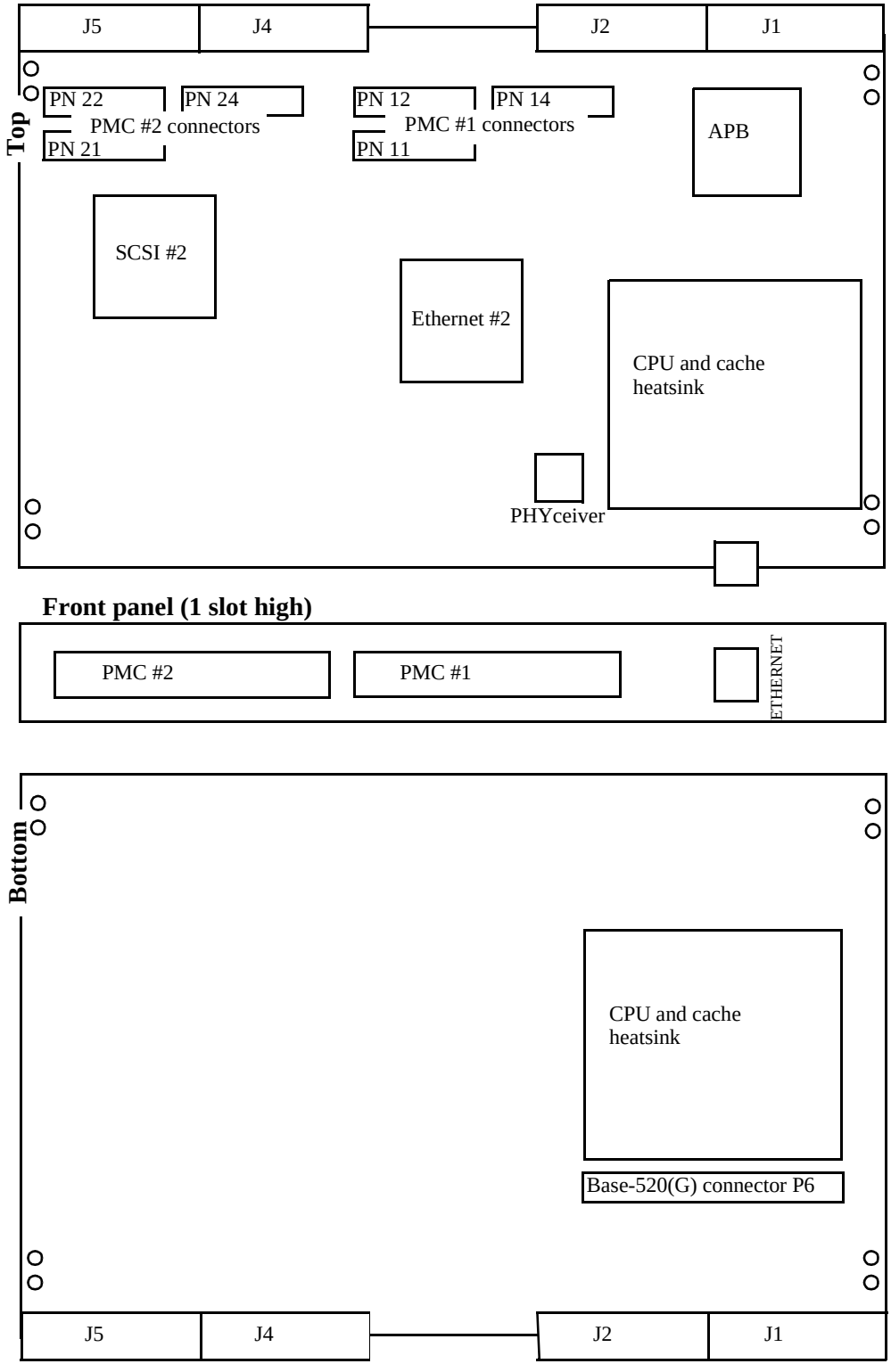
5 I/O-52x(G) Installation

5.1 Location Overview

The I/O-52x(G) contains the following main I/O interfaces:

- SCSI #2,
- Ethernet #2,
- PMC #1 and PMC #2.

Figure 16 Location diagram of the I/O-52x(G) (schematic)



5.2 Mechanical Constructions

The I/O-52x(G) is an extension to the Base-520(G). It occupies 1 CompactPCI slot and consists of the following major components:

- 2 PMC connectors,
- 1 SCSI #2 interface,
- and 1 Ethernet #2 interface.

The following figures show the SPARC/CPCI-52x(G) in 2-slot and 3-slot configurations.

Figure 17 Mechanical construction of the SPARC/CPCI-522

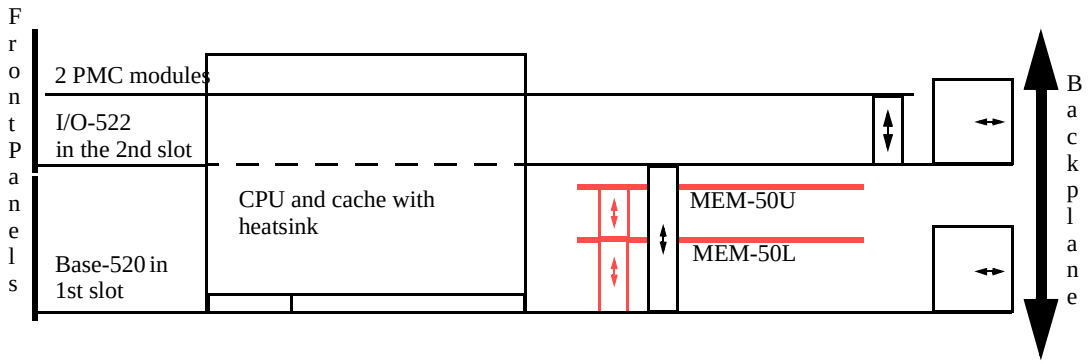


Figure 18 Mechanical construction of the SPARC/CPCI-52xG

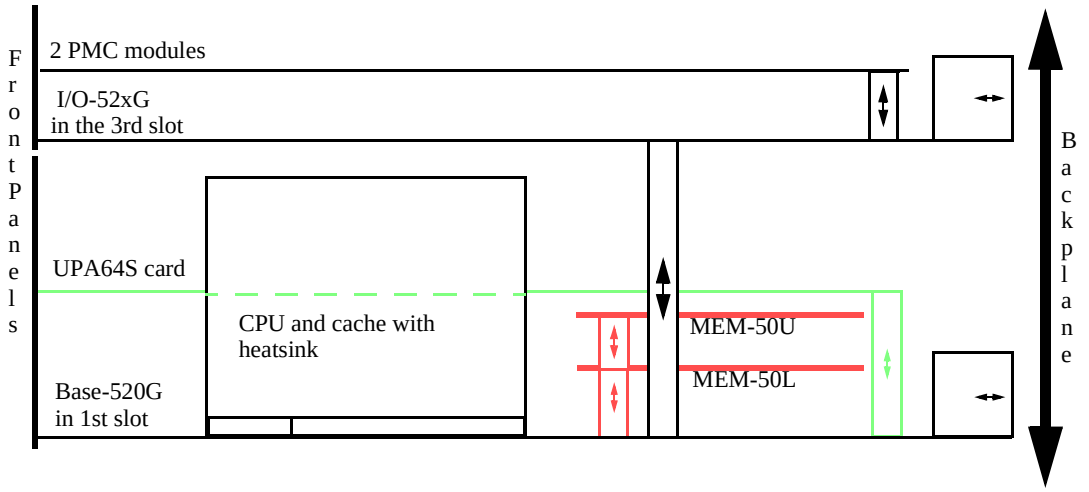
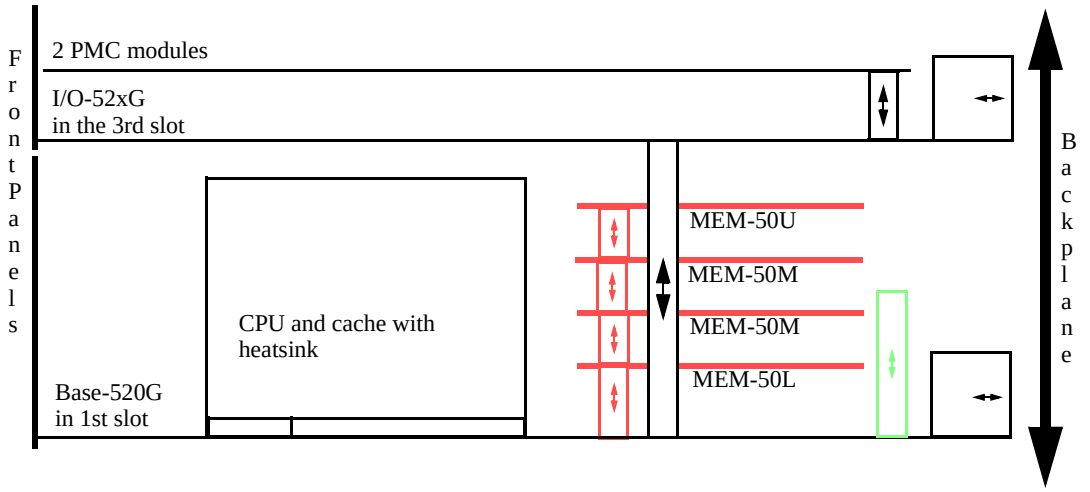


Figure 19 Mechanical construction of the SPARC/CPCI-52xG (option)



5.2.1 Installation/Deinstallation of the I/O-52x(G)

This section describes the installation and deinstallation procedure for the I/O-52x(G) with the mentioned location shown in the figure below.

Installation of the I/O-52x(G)

To install the I/O-52x(G) follow the steps below:

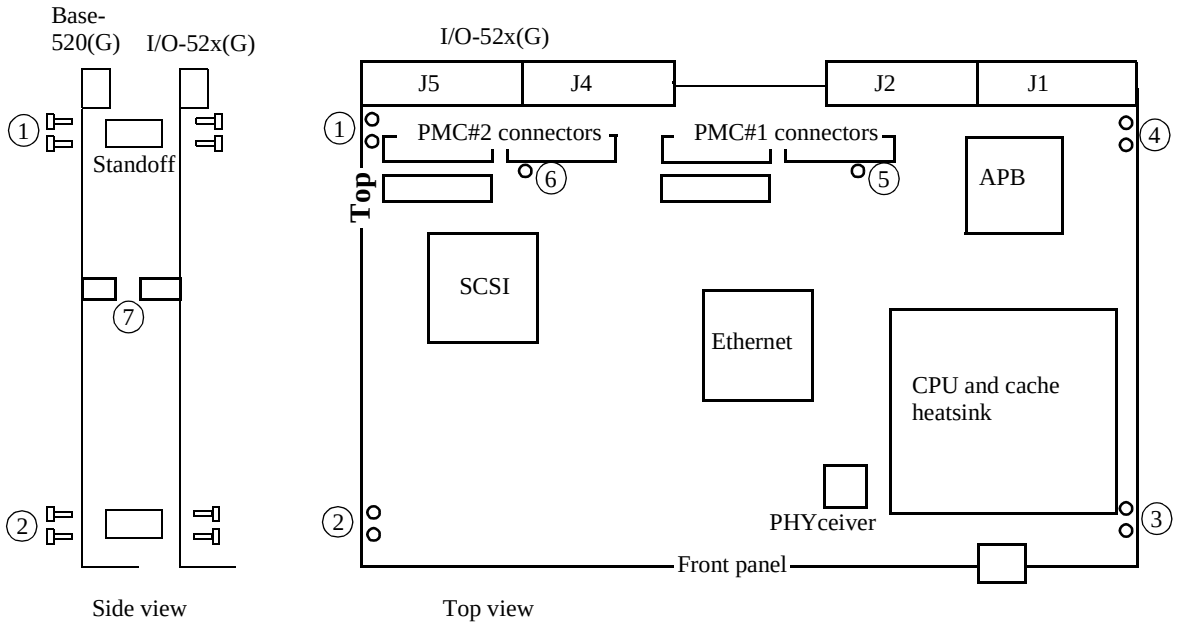
1. If there is an UPA64S card installed on your Base-520(G) ensure that you use the 2 z-standoffs delivered with the UPA64S card.
2. Remove the 10 screws at location 1...6 on the open end off the stand-offs of the I/O-52x(G).
3. Plug the I/O-52x(G) to the Base-520(G) via the I/O-52x(G) to Base-520(G) connector at position 7 and fix it with the 10 removed screws on the standoffs at location 1...6.

Deinstallation of the I/O-52x(G)

To deinstall the I/O-52x(G) follow the steps below:

1. Remove the 8 screws at location 1...4 on the bottom side of your Base-520(G).
2. Remove the 2 screws at location 5 and 6 on the top side of the I/O-52x(G).
3. Remove the I/O-52x(G) from the Base-520(G) by lifting it.
4. Fix the removed 10 screws on the open ends of the standoffs to have them available when installing the I/O-52x(G) again.

Figure 20 Installation/Deinstallation of the I/O-52x(G)



5.3 Powering Up

For powering up see the respective installation section of the Base-520(G).

5.4 Front Panel and Connectors

Front panel features

The features of the front panel are described in the following table. For a location diagram see figure 14 “Location diagram of the I/O-board (schematic)” on page 47.

Table 21 Front panel features

Device	Description
ETHERNET	Standard Twisted-Pair-Ethernet RJ45 connector for 10BaseT/100BaseTX Ethernet
PMC #1	Hole for the PMC #1 front panel
PMC #2	Hole for the PMC #2 front panel

On-board connectors

In addition to the front-panel connectors, the I/O-52x(G) provides on-board connectors for connection to the Base-520(G), to the CompactPCI bus and for 2 PMC modules. An overview is shown in the following table.

Table 22 On-board connectors

Connector description and location	Connector type and sample manufacturer part number
CompactPCI J1, J2, J4, J5	Standard CompactPCI metric, 5-row shielded connectors female
I/O-52x(G) extension connector P6	100-pin MBUS connector female low: for 2 slot solution high: for 3 slot solution
PMC #1 PN11, PN12, PN14	64-pin SMD connector
PMC #2 PN21, PN22, PN24	64-pin SMD connector

5.4.1 Ethernet #2 Interfaces

The full duplex 10BaseT/100BaseTx Ethernet #2 interface is available at the front panel via a Twisted-Pair-Ethernet connector.

Table 23 Twisted-Pair-Ethernet connector pinout

Connector	Pin	Signal
RJ-45 TPE 	1	TX+
	2	TX-
	3	RX+
	4	GND
	5	GND
	6	RX-
	7	GND
	8	GND

The Ethernet #2 interface is also accessible at the J5 back panel connector via an MII #2 interface. If Ethernet #2 gets accessed via I/O panel, the front panel connector is normally disabled automatically, for other configurations see the respective jumper settings in the *SPARC/IOBP-520*

Installation Guide. For the J5 connector pinout see figure 22 “CompactPCI J5 connector pinout” on page 58.

5.4.2 PMC Slots

The I/O-52x(G) provides 2 PMC slots compliant with IEEE P1386 ("Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC"). The PCI bus, a high speed local bus, connects different high speed I/O cards with the SPARC/CPCI-52x(G). Both PMC slots support 32-bit data bus width with a maximum frequency of 33 MHz.

PMC Voltage Keys

The PCI bus uses a 5V voltage to signal bus levels. The voltage keys prevent 3.3V PMC cards from being plugged into the PMC slots.

Connector Configuration

The 32-bit PCI bus requires 2 PMC connectors. The 3rd PMC connector (PNx4) connects additional user I/O signals of PMC slot 1 and PMC slot 2 to the CompactPCI J4 connector.

PMC slot 1 connectors

- for the PCI bus: PN11 and PN12
- for 64 user I/O signals: PN14

PMC slot 2 connectors

- for the PCI bus: PN21 and PN22
- for 32 user I/O signals: PN24

5.4.3 CompactPCI Backplane Connector Pinout

J1 and J2

The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as specified by the CompactPCI specification. Therefore, this manual only documents the pinout of the J4 and J5 connector.

J4 and J5

Besides the CompactPCI specific pinout the following interfaces are available on the CompactPCI J4 and J5 connector.

- SCSI #2, MII #2
- User I/O pins for PMC #1 and #2 (`PMC #1, PMC #2`)

Figure 21 **CompactPCI J4 connector pinout**

A	B	C		D	E
PMC #1 I/O 61	PMC #1 I/O 62	PMC #1 I/O 63	1	PMC #1 I/O 64	n.c.
PMC #1 I/O 56	PMC #1 I/O 57	PMC #1 I/O 58	2	PMC #1 I/O 59	PMC #1 I/O 60
PMC #1 I/O 51	PMC #1 I/O 52	PMC #1 I/O 53	3	PMC #1 I/O 54	PMC #1 I/O 55
PMC #1 I/O 46	PMC #1 I/O 47	PMC #1 I/O 48	4	PMC #1 I/O 49	PMC #1 I/O 50
PMC #1 I/O 41	PMC #1 I/O 42	PMC #1 I/O 43	5	PMC #1 I/O 44	PMC #1 I/O 45
PMC #1 I/O 36	PMC #1 I/O 37	PMC #1 I/O 38	6	PMC #1 I/O 39	PMC #1 I/O 40
PMC #1 I/O 31	PMC #1 I/O 32	PMC #1 I/O 33	7	PMC #1 I/O 34	PMC #1 I/O 35
PMC #1 I/O 26	PMC #1 I/O 27	PMC #1 I/O 28	8	PMC #1 I/O 29	PMC #1 I/O 30
PMC #1 I/O 21	PMC #1 I/O 22	PMC #1 I/O 23	9	PMC #1 I/O 24	PMC #1 I/O 25
PMC #1 I/O 16	PMC #1 I/O 17	PMC #1 I/O 18	10	PMC #1 I/O 19	PMC #1 I/O 20
PMC #1 I/O 11	PMC #1 I/O 12	PMC #1 I/O 13	11	PMC #1 I/O 14	PMC #1 I/O 15
Coding key area			12		
			13		
			14		
PMC #1 I/O 6	PMC #1 I/O 7	PMC #1 I/O 8	15	PMC #1 I/O 9	PMC #1 I/O 10
PMC #1 I/O 1	PMC #1 I/O 2	PMC #1 I/O 3	16	PMC #1 I/O 4	PMC #1 I/O 5
PMC #2 I/O 61	PMC #2 I/O 62	PMC #2 I/O 63	17	PMC #2 I/O 64	VP5_IOBP
PMC #2 I/O 56	PMC #2 I/O 57	PMC #2 I/O 58	18	PMC #2 I/O 59	PMC #2 I/O 60
PMC #2 I/O 51	PMC #2 I/O 52	PMC #2 I/O 53	19	PMC #2 I/O 54	PMC #2 I/O 55
PMC #2 I/O 46	PMC #2 I/O 47	PMC #2 I/O 48	20	PMC #2 I/O 49	PMC #2 I/O 50
PMC #2 I/O 41	PMC #2 I/O 42	PMC #2 I/O 43	21	PMC #2 I/O 44	PMC #2 I/O 45
PMC #2 I/O 36	PMC #2 I/O 37	PMC #2 I/O 38	22	PMC #2 I/O 39	PMC #2 I/O 40
PMC #2 I/O 31	PMC #2 I/O 32	PMC #2 I/O 33	23	PMC #2 I/O 34	PMC #2 I/O 35
PMC #2 I/O 26	PMC #2 I/O 27	PMC #2 I/O 28	24	PMC #2 I/O 29	PMC #2 I/O 30
PMC #2 I/O 21	PMC #2 I/O 22	PMC #2 I/O 23	25	PMC #2 I/O 24	PMC #2 I/O 25

As factory option the PMC #1 I/O 1...32 signals can be connected to the PMC #2 I/O 33...64 signals.

Figure 22 **CompactPCI J5 connector pinout**

A	B	C		D	E
SCSI #2 D8	SCSI #2 D9	SCSI #2 D10	1	SCSI #2 D11	n.c.
SCSI #2 SEL	SCSI #2 CD	SCSI #2 REQ	2	SCSI #2 IO	WIDETERMPWR
SCSI #2 ATN	SCSI #2 BSY	SCSI #2 ACK	3	SCSI #2 RST	SCSI #2 MSG
SCSI #2 D4	SCSI #2 D5	SCSI #2 D6	4	SCSI #2 D7	TERMPWR
SCSI #2 D0	SCSI #2 D1	SCSI #2 D2	5	SCSI #2 D3	SCSI #2 DP0
SCSI #2 D12	SCSI #2 D13	SCSI #2 D14	6	SCSI #2 D15	SCSI #2 DP1
MII #2 RXD3	MII #2 RXD2	MII #2 RXD1	7	MII #2 RXD0	MII #2 RX_CLK
MII #2 RX_DV	MII #2 COL	MII #2 CRS	8	MII #2 RX_ER	MII #2 MGT_DIO
MII #2 TXD3	MII #2 TXD2	MII #2 TXD1	9	MII #2 TXD0	MII #2 TX_CLK
PMC #2 I/O 19	PMC #2 I/O 20	MII #2 TX_EN	10	MII #2 TX_ER	MII #2 MGT_CLK
PMC #2 I/O 14	PMC #2 I/O 15	PMC #2 I/O 16	11	PMC #2 I/O 17	PMC #2 I/O 18
PMC #2 I/O 9	PMC #2 I/O 10	PMC #2 I/O 11	12	PMC #2 I/O 12	PMC #2 I/O 13
PMC #2 I/O 5	PMC #2 I/O 6	PMC #2 I/O 7	13	PMC #2 I/O 8	VP5_IOBP
PMC #2 I/O 1	PMC #2 I/O 2	PMC #2 I/O 3	14	PMC #2 I/O 4	n.c.
VP5_IOBP	n.c.	n.c.	15	n.c.	n.c.
n.c.	n.c.	n.c.	16	n.c.	n.c.
n.c.	n.c.	n.c.	17	n.c.	n.c.
n.c.	n.c.	n.c.	18	n.c.	n.c.
n.c.	n.c.	n.c.	19	n.c.	n.c.
n.c.	n.c.	n.c.	20	n.c.	n.c.
n.c.	n.c.	n.c.	21	n.c.	n.c.
n.c.	n.c.	n.c.	22	n.c.	n.c.

I/O panel

As a separate price list item an I/O panel is available for the I/O-52x(G), the SPARC/IOBP-520/IO. An extended variant is the SPARC/CPCI-520/AccKit/IO which contains additionally to the I/O panel the following cables:

– a flat ribbon SCSI cable for the I/O panel

– and a Twisted-Pair-Ethernet cable for the front panel or the I/O panel.

The I/O panel supports the following interfaces:

- Fast/Wide SCSI #2,
- MII #2 Ethernet,
- and PMC user I/O.

Danger



The SPARC/IOBP-520/IO and the SPARC/CPCI-520/AccKit/IO is especially designed for the I/O-52x(G).
Do not use any other I/O panels on the I/O-52x(G). Use only the front panel or the backpanel Ethernet interface, not both. Check the configuration of your I/O panel.

5.5 SCSI #2 Configuration

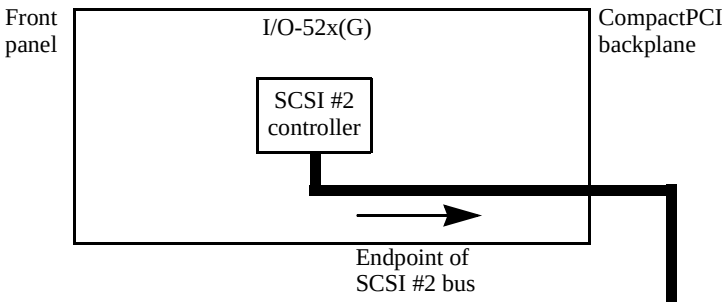
Note: **Correct SCSI bus selection: The I/O-52x(G) provides a second SCSI bus, SCSI #2. Its configuration is described as follows.**

The I/O-52x(G)'s SCSI #2 bus is only available at the I/O-52x(G)'s CompactPCI J5 connector.

Valid configuration

There is only 1 valid I/O-52x(G) SCSI #2 bus configuration:

- The I/O-52x(G) is located at an endpoint of the SCSI #2 bus, the SCSI #2 bus is extended via the CompactPCI backplane:



The SCSI #2 bus is always terminated at the SCSI #2 controller.

5.6 Ethernet #2 Configuration

Note: **Correct Ethernet selection: The I/O-52x(G) provides the following 2 Ethernet #2 interfaces:**

- via a TPE #2 interface connected to a front-panel RJ-45 connector
- or an MII #2 interface available at the CompactPCI J5 connector

Ethernet address and host ID

For the SPARC/CPCI-52x(G) exists only 1 ethernet address and host ID, see "Ethernet Address and Host ID" section of the Base-520(G)'s installation section. Therefore you can use the Ethernet #2 TPE or MII interface of the I/O-52x(G) only in a separate network according to Ethernet #1 TPE or MII of the Base-520(G).

5.7 OpenBoot Firmware Alias Definitions for I/O-52x(G)

This chapter describes additional features used with reference to the I/O-52x(G) enhancements.

Table 24 Device alias definitions

Alias	Description
	Defined for SCSI #2:
scsi-2	SCSI #2
disk26	disk SCSI #2-target-ID 6
disk25	disk SCSI #2-target-ID 5
disk24	disk SCSI #2-target-ID 4
disk23	disk SCSI #2-target-ID 3
disk22	disk SCSI #2-target-ID 2
disk21	disk SCSI #2-target-ID 1
disk20	disk SCSI #2-target-ID 0
tape2 (or tape20)	1st tape drive SCSI #2-target-ID 4
tape21	2nd tape drive SCSI #2-target-ID 5
cdrom2	CD-ROM partition f, SCSI #2-target-ID 6
	Defined for Ethernet #2:
net	Ethernet #2
pcia-io	secondary PCI bus A
pcib-io	secondary PCI bus B

Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

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Responsible Dept.: ❑ Marketing ❑ Production

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