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PENT/CPCI-730

Installation Guide

P / N 215922 Revision AB
March 2002

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Using This Guide

This Installation Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), Compact Peripheral Component Interconnect (CPCI) and telecommunications.

Conventions

Notation	Description
1234	All numbers are decimal numbers except when used with the notations described below
00000000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal point indicator is signaled
Bold	Character format used to emphasize a word
`Courier`	Character format used for on-screen output
`Courier+Bold`	Character format used to characterize user input
Italics	Character format for references, table, and figure descriptions
<text>	Typical notation used for variables and keys
[text]	Typical notation for buttons
...	Repeated item
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges
:	Extents
|	Logical OR

Notation	Description
Note:	No danger encountered. Pay attention to important information marked using this layout
Caution 	Possibly dangerous situation:slight injuries to people or damage to objects possible
Danger 	Dangerous situation:injuries to people or severe damage to objects possible

Revision History

Order No.	Revision	Date	Description
212399	AA	March 2000	Preliminary Installation Guide
212399	AB	April 2000	Added restriction to I/O front panel features page 1-5, added restriction to “Block Diagram” page 16, corrected “Order Numbers” page 18, added frequencies to Table 4 “Environmental Requirements” page 2-5, removed note in section “IOBP-CPU720” page 2-13; added footnote 8) to Table 14 “Register Location” page 6-6, added Bit 2 WDOG_TIMEOUT to Table 18 “Watchdog Control Register” page 6-10, corrected settings for Bit 1..0 in Table 25 “Flash Device and SERR Register” page 6-15, editorial changes
212399	AC	October 2000	Editorial changes: restructured document

Order No.	Revision	Date	Description
212399	AD	January 2001	Corrected connector pinout in Figure 11 “J4 Connector Pinout on Standard PENT/CPCI-730” page 3-9, updated Table 3 “Ordering Information Excerpt” page 1-8 editorial changes: modified register tables, corrected Table 4 “Environmental Requirements” page 2-5.
212399	AE	July 2001	Changed SW1-4 in Table 7 “Default Settings” page 2-14 from “Serial EEPROM Write Protection” to “Not used”, changed “Flash Device and SERR Register” page 615 by removing WP_BIB Select Register. Editorial changes: changed text flow and font size of procedures throughout the document, moved “Other Sources of Information” page xvii, modified “Action Plan” page 23 reformatted sentence in “Environmental Requirements” page 25 to Note, modified Table 7 “Default Settings” page 2-14, modified sentence structure in “Board Installation” page 216, removed “Supporting Hot Swap” from heading “Installation in a Powered System” page 217, modified sentence in “Software Upgrades and Accessories” page 219, modified “Installation Procedure” page 218, modified Figure 8 “KBD/MS – Keyboard and Mouse Connector Pinout” page 3-7, modified Figure 9 “COM1 Connector Pinout” page 3-7, Removed note and moved note from “J5” page 311 to “IOBP-CPU720” page 213, restructured and modified the “BIOS” chapter, renamed heading to “Board-Specific Registers” page 66, renamed Table 14 “Register Location” page 6-6, restructured and moved “Troubleshooting” from Chapter 7 to Appendix B “Troubleshooting”, added “Index”

Order No.	Revision	Date	Description
212399	AF	August 2001	Added the “Sicherheitshinweise” section on page -xxiii
212399	AG	August 2001	Editorial changes
215922	AA	October 2001	Completely revised the “Safety Notes” section on page -xix and the “Sicherheitshinweise” section on page -xxiii; removed picture from title page; added manufacturing requirements to Table 2 “Standard Compliance” page 1-7
215922	AB	March 2002	Moved battery exchange description from Maintanance section to Appendix A Editorial changes

Other Sources of Information

For further information, refer to the following documents:

Company	www.	Document
Force Computers	forcecomputers.com	PENT / CPCI-72x AccKit Installation Guide (P / N 205235)
		PENT / CPCI-730 / HD-AccKit Installation Guide (P / N 210821)
		PENT / IOBP-CPU720 Installation Guide (P / N 210615)
		PENT / MEM-700 (P / N 210822)
		PMC / VGA-4 Installation Guide (P / N 210952)
Hitachi / Micron / Mitsubishi	halsp.hitachi.com	8Mx8 (M5M4V64S30A) Synchronous DRAM
Integrated Circuit Systems	icst.com	PHY ICS1890
Intel	developer.intel.com	1Mx8, 28F800B5T BIOS flash
		21143, 82559 Ethernet
		21150 PCI-to-PCI bridge
		82371AB (82371EB) EIDE, PCI-to-ISA bridge, USB
		82443BX Host-to-PCI bridge
		Intel Arch. Software Dev. Manual: Volume 1: Basic Architecture, Volume 2: Instruction Set Ref. Manual, Volume 3: System Programming Guide
		Mobile Module Connector 2 (MMC-2) for Pentium II or III Mobile Module
Maxim	maxim-ic.com	MAX.1617 Temperature sensor on mobile module
Memory Corporation	memcorp.com	MY20-80 IDE flash disc
National	national.com	PC87309 Super I / O, Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy

Company	www.	Document
Philips Semiconductor	philips.com	The I^2C bus and how to use it (including specifications)
Texas Instruments	ti.com	COM3 TL16C550C Asynchronous Communications Element
Winbond	winbond.com	W83781D Hardware monitor



Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PENT/CPCI-730.

We intend to provide all necessary information to install and handle the PENT/CPCI-730 in this Installation Guide. However, as the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The PENT/CPCI-730 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, maintain, and operate the PENT/CPCI-730. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial, business or industrial environment.

The board generates and uses radio frequency energy and, if not installed properly and used in accordance with this Installation Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If you use the board without a PMC module, cover empty slots with blind panels to ensure proper EMC shielding. If boards are integrated into open systems, always cover empty slots.



Installation

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life. Therefore:

- **Before installing or removing the board, read the “Action Plan” section page 2-3.**
- **Before touching boards or electronic components, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or removing an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the CompactPCI back-plane via all assembled connectors and that power is available on all power pins.**
- **Ensure that the total max. power consumption per PMC slot at +/-12V, 5V, and 3.3V level does not exceed 7.5W (total over all used voltages).**

Wrong slot positions may cause system deadlocks and destroy back-planes or boards. Therefore, plug the PENT/CPCI-730 always into a system slot marked by a triangle.

Before powering up the board, check the switch settings for consis-tency.

Hot Swap

The PENT/CPCI-730 provides hot-swap support, i.e. it may be installed in or removed from a powered system. Never install the board in or remove it from a system under hot-swap conditions unless a basic hot- swap platform is used and the system documentation explicitly includes appropriate guidelines for these tasks. For detailed information on the hot-swap support and the relevant safety notes, see “Installation in a Powered System” on page 2-17. All the follow-ing safety notes refer to the installation and removal of the board in a nonpowered system or a system not supporting hot swap.



Operation

While operating the board ensure that the environmental and power requirements are met.

When operating the board in areas of electromagnetic radiation ensure that the board is bolted on the CompactPCI system and the system is shielded by enclosure.

If the standard PENT/CPCI-730/HD-AccKit is installed, the operation temperature of the CPCI-730 is limited by the maximum operation temperature of the hard disk. If the maximum temperature of the hard disk is lower than the maximum temperature of the CPCI-730, the maximum temperature specified for the hard disk must not be exceeded.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Replacement/Expansion

Only replace or expand components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMC and the possibly changed functionality of the product.

Check the total power consumption of all components installed (see the technical specification of the respective components). Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).



Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**
- **Do not use a screwdriver to remove the battery from its holder to avoid possible damage to the PCB or the battery holder.**
- **When installing the new battery ensure that the '+' on top of the battery stays at the top and therefore is visible when viewing the board from its component side.**

Environment

Always dispose of old boards according to your country's legislation, if possible in an environmentally acceptable way.



Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Einbau, Betrieb und Wartung des PENT/CPCI-730 zu beachten sind.

Wir sind darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem PENT/CPCI-730 in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem PENT/CPCI-730 um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Ihnen Informationen fehlen sollten, wenden Sie sich bitte an Ihren Vertreter von Force Computers.

Das PENT/CPCI-730 erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Force Computers ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Boards in Geschäfts-, Gewerbe- sowie Industriebereichen gewährleisten.

Das Board arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten. Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Wenn Sie das Board ohne ein PMC Modul verwenden, schirmen Sie freie Steckplätze mit einer Blende ab, um einen ausreichenden EMV Schutz



zu gewährleisten. Wenn Sie Boards in Systeme einbauen, schirmen Sie freie Steckplätze mit einer Blende ab.

Installation

Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Beachten Sie deshalb die folgenden Punkte:

- **Bevor Sie Boards oder elektronische Komponenten berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Lesen Sie vor Ein- oder Ausbau des Boards den Abschnitt “Action Plan” auf Seite 2-3.**
- **Drücken Sie bei Ein- oder Ausbau des Boards nicht auf die Frontplatte, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Ein- oder Ausbau von zusätzlichen Geräten oder Modulen das dazugehörige Benutzerhandbuch.**
- **Vergewissern Sie sich, daß der gesamte max. Leistungsverbrauch pro PMC-Steckplatz bei einer Spannung von +/- 12V, 5V und 3,3V 7,5W nicht übersteigt (Gesamtsumme aller verwendeten Spannungen).**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die CompactPCI Backplane angeschlossen ist und Strom an allen Spannungskontakten anliegt.**

Ein falscher Steckplatz kann zur Systemblockade führen und System und Boards zerstören. Stecken Sie deshalb das PENT/CPCI-730 immer in einen Systemsteckplatz, der mit einem Dreieck markiert ist.

Überprüfen Sie die Schalter-Positionen, bevor Sie das Board hochfahren.

Hot Swap

Das PENT/CPCI-730 unterstützt Hot Swap, d.h. es kann in ein laufendes System installiert werden oder daraus entfernt werden. Einbau oder Ausbau des Boards in einem System unter Hot Swap Bedingungen darf nur dann stattfinden, wenn die grundlegende Hot Swap Plattform, die vollständige Hot Swap Plattform, oder die Hochverfügbarkeits Hot Swap Plattform benutzt wird und die Systembeschreibung ausdrücklich die geeigneten Richtlinien vorgibt.



Detaillierte Informationen zum Thema Hot Swap Unterstützung und die entsprechenden Sicherheitshinweise finden Sie im Abschnitt “Installation in a Powered System” auf Seite 2-17. Alle folgenden Sicherheitshinweise beziehen sich auf die Installation eines Boards in oder sein Entfernen aus einem nicht laufenden System oder einem System, das Hot Swap nicht unterstützt.

Betrieb

Achten Sie darauf, dass die Umgebungs- und die Leistungsanforderungen während des Betriebs eingehalten werden.

Wenn Sie das Board in Gebieten mit elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Board mit dem CompactPCI System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Wenn das Standard PENT/CPCI-730/HD-AccKit installiert wird, ist die Betriebstemperatur des CPU Boards durch die maximale Betriebstemperatur der Festplatte begrenzt. Wenn die maximale Betriebstemperatur der Festplatte niedriger ist als die des CPU Boards, darf die maximale Betriebstemperatur der Festplatte nicht überschritten werden.

Stellen Sie sicher, dass Anschlüsse und Kabel des Boards während des Betriebs nicht berührt werden können.

Austausch/Erweiterung

Verwenden Sie bei Austausch oder Erweiterung nur von Force Computers empfohlene Komponenten und Systemteile. Andernfalls sind Sie für mögliche Auswirkungen auf EMV und geänderte Funktionalität des Produktes voll verantwortlich.

Überprüfen Sie die gesamte aufgenommene Leistung aller eingebauten Komponenten (siehe die technischen Daten der entsprechenden Komponente). Stellen Sie sicher, dass die Ausgangsströme jedes Verbrauchers innerhalb der zulässigen Grenzwerte liegen (siehe die technischen Daten des entsprechenden Verbrauchers).



Batterie

Muss eine Lithium Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**
- **Verwenden Sie keinen Schraubendreher, um die Batterie aus der Halterung zu entfernen, um Schaden an der Platine oder der Halterung zu vermeiden.**
- **Vergewissern Sie sich bei der Installation der neuen Batterie, dass das '+' oben und damit sichtbar bleibt, wenn das Board von der Komponenten-Seite aus betrachtet wird.**

Umweltschutz

Entsorgen Sie alte Boards gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich umweltfreundlich.

1

Introduction

Features

The PENT/CPCI-730 is a 6U CompactPCI system board based on the Intel Pentium II or III CPU running with Windows NT Version 4.0 or higher. It requires the space of one slot. All PENT/CPCI-730 PCI buses including the CompactPCI interface are 32-bit wide and operate at 33 MHz PCI bus frequency. On-board are:

- Two 82C37A compatible DMA controllers on the PCI-to-ISA bridge
- Two 82C29 compatible interrupt controllers on the PCI-to-ISA bridge
- Program-readable vintage registers for board information protocol
- Inrush current protection for hot swap

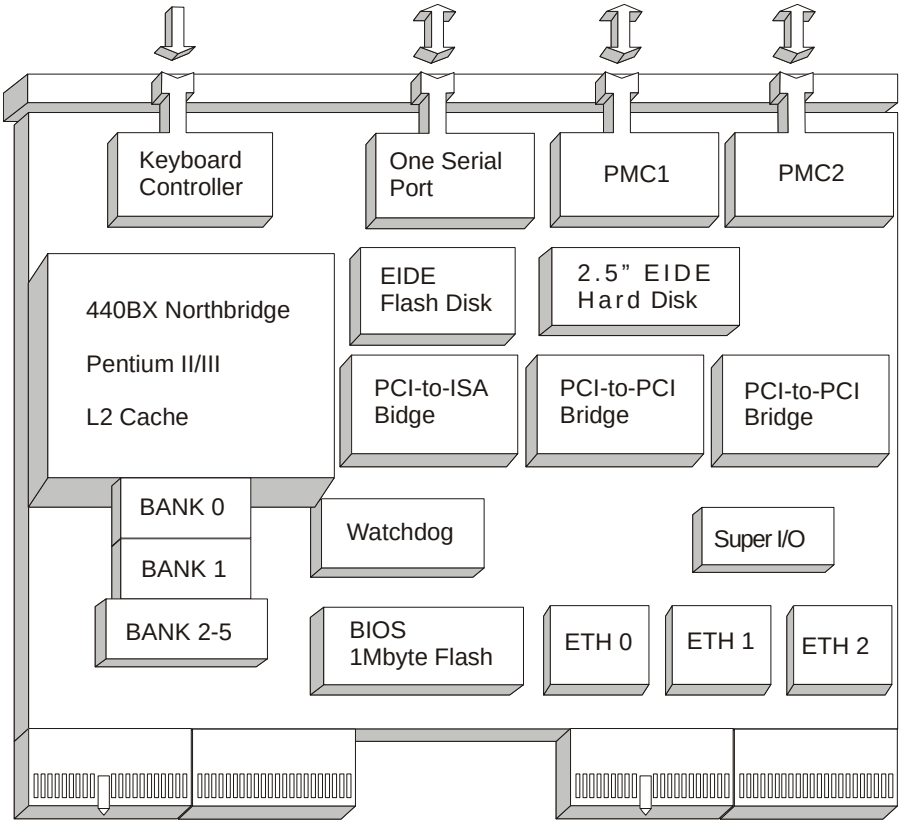


Figure 1: *Function Blocks*

CPU

The CPCI-730 offers:

- Low power Pentium II / III mobile module with e.g. 256 or 512 KByte L2 cache
- Software controllable watchdog, which controls the CPU activity and causes a RESET or an NMI in case of malfunction
- 8254 compatible three-channel timer

Memory

Memory features include:

- Synchronous DRAM (SDRAM) with ECC support running at 66 or 100 MHz clock frequency
- Motorola 146818 compatible real time clock and CMOS RAM for storing factory settings, both RTC and RAM with battery backup
- 1 or 4 MByte flash BIOS, 8-bit wide
- Optional 16 MByte flash disk

Interfaces

The front panel and on-board interfaces of the PENT/CPCI-730 are shown in the table below:

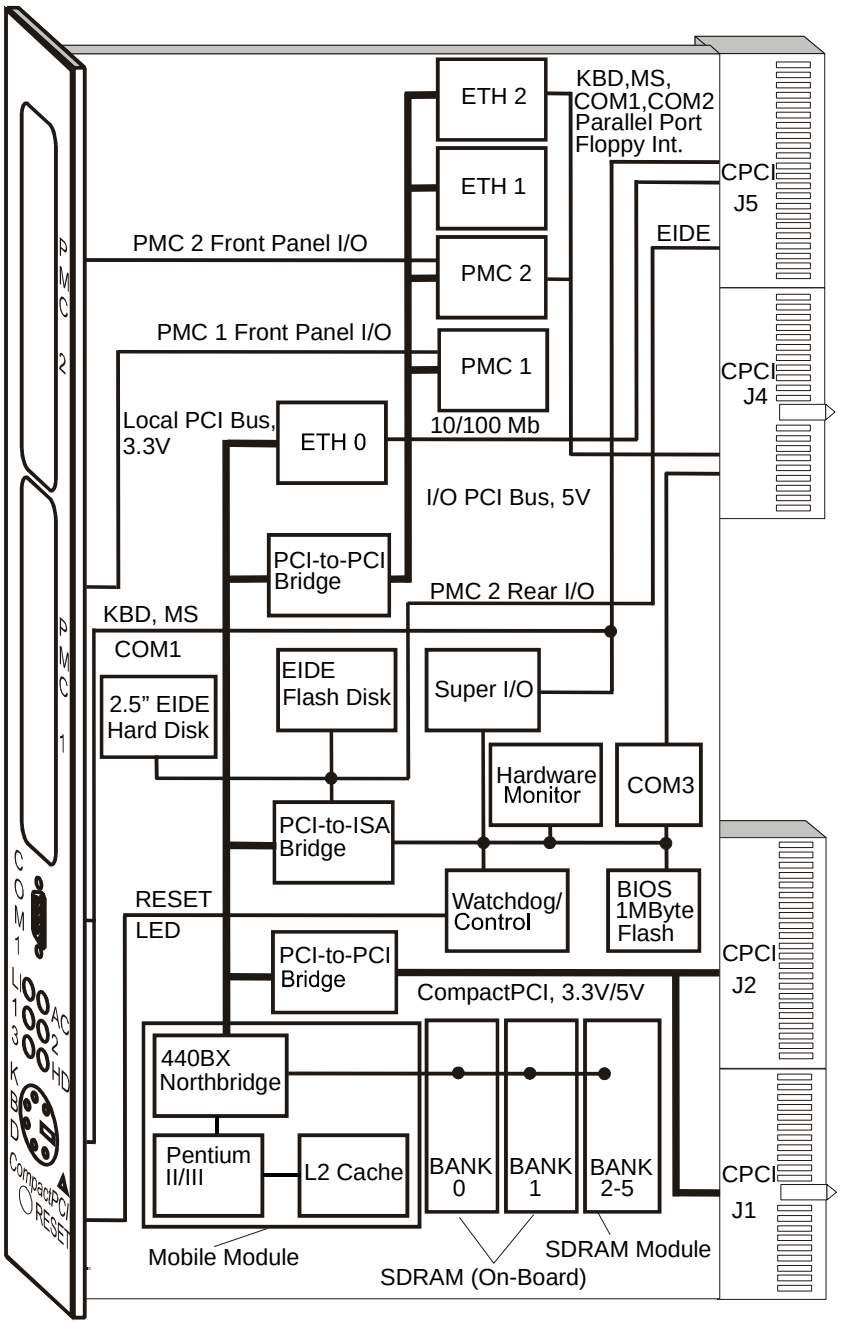
Table 1: *Interfaces*

PCI interface	Description
Ethernet	Three 10/100 BaseT Ethernet: ETH0 on connector J5 ETH1 on connector J4 as assembly option[1)] ETH2 on connector J4 as assembly option[1)]
Floppy	Floppy controller via connector J5
IDE	Primary IDE interface via on-board connector, the secondary via connector J5 2.5''IDE devices are to be used with the on-board connector and 3.5''IDE devices via connector J5.
Keyboard/Mouse	PS/2 keyboard and mouse interface on the front panel and connector J5
Parallel I/O	Parallel interface LPT, IEEE 1284 compatible and with ECP (Extended Capabilities Port) and EPP (Extended Parallel Port) support, at connector J5
PMC	Two PMC slots, both supporting the front panel interface and one supporting the interface via connector J4
Serial I/O	Three RS-232 interfaces: COM1 on front panel and connector J5 COM2 on connector J5. COM3 on connector J4[1)]
USB	USB interface on connector J5

1) Not supported with IOBP-CPU720

Block Diagram

The block diagram shows how the PENT/CPCI-730 devices work together and which data paths they use.



Standard Compliances

The PENT/CPCI-730 meets the following standards:

Table 2: *Standard Compliance*

Standard	Description
EN 60950 UL/cUL 1950 (predefined Force Computers system)	Legal Safety Requirements
EN 50081-2 EN 50082-2 EN 55022 Class A FCC Part 15 Class A VCCI Class A	EMC requirements on system level
ANSI/IPC_A-610 Rev. C ANSI/IPC-7711 ANSI/IPC-7721 ANSI-J-001...003	Manufacturing requirements

Ordering Information

When ordering CPCI-730 board variants, upgrades, and accessories, use the order number given below.

Product Nomenclature

In the following you find the key for the product name extensions.

PENT/CPCI-730/xxx-ccc-Lyyy-zz	
xxx	DRAM size in MByte
ccc	Processor clock frequency in MHz
Lyyy	L2 cache capacity in KByte
zz	IDE flash disk capacity in MByte

Order Numbers

Depending on the PENT / CPCI-730 type, the available upgrades and accessories may differ. Consult your local sales representative to check the possibility of combinations.

Table 3: *Ordering Information Excerpt* [1)]

Order No.	PENT/CPCI-730	Description
107078	.../ 256-500-L256-16	Intel Pentium-III 500 MHz with 256 MByte main memory, 256 KByte 2nd level cache, 16 MByte flash disk
107031	PENT / MEM-700 / lll	lll = 256 MByte memory module
107092	PENT / MEM-700 / lll	lll = 512 MByte memory module
107088	PMC / VGA-4	PMC based VGA graphics card and related installation components
Hardware Accessories PENT/CPCI-730		
104968	PENT / CPCI-720 / CPUP5-AccKit	Rear transition board and related installation components
106092	.../ HD-AccKit	Hard disk and related installation components

Table 3: *Ordering Information Excerpt (cont.)*[1)]

Order No.	PENT/CPCI-730	Description
Software Accessories PENT/CPCI-730		
105583	… / BIOS-Upgrade Kit	BIOS upgrade utilities
105757	... / NT-Support-Package	Windows NT drivers

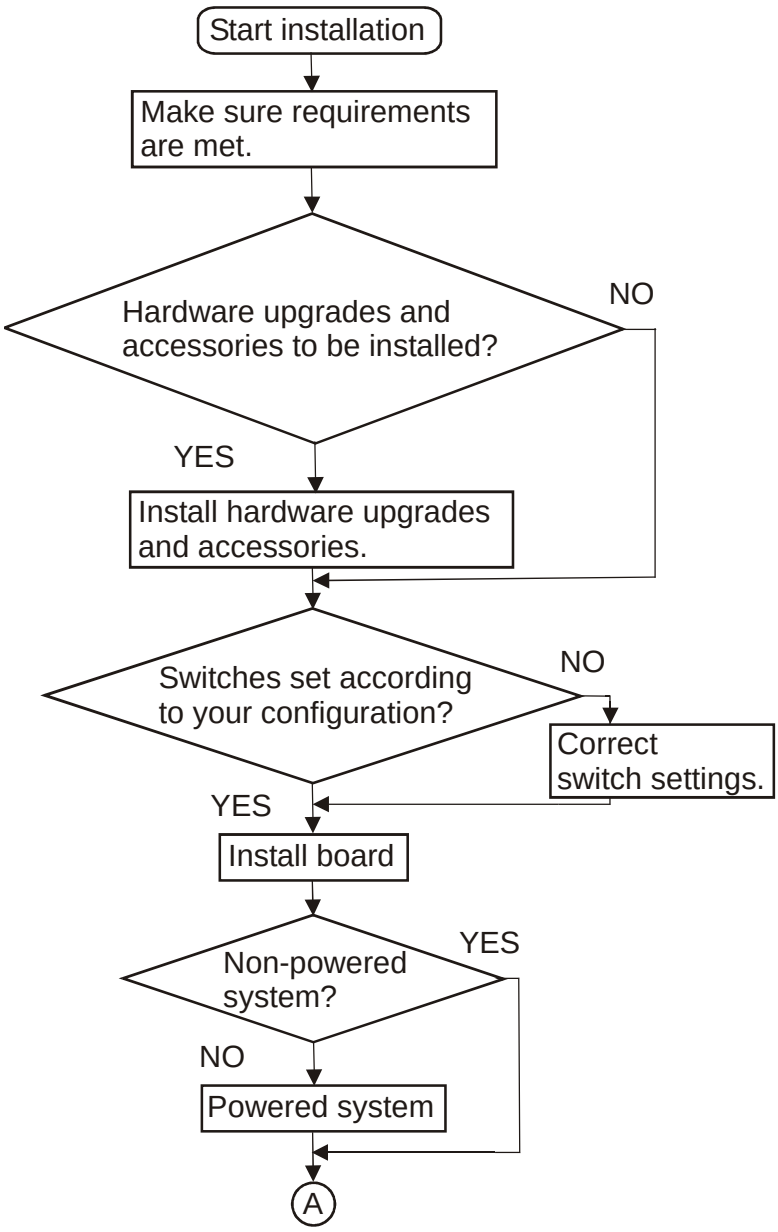
1) Status: July 2001

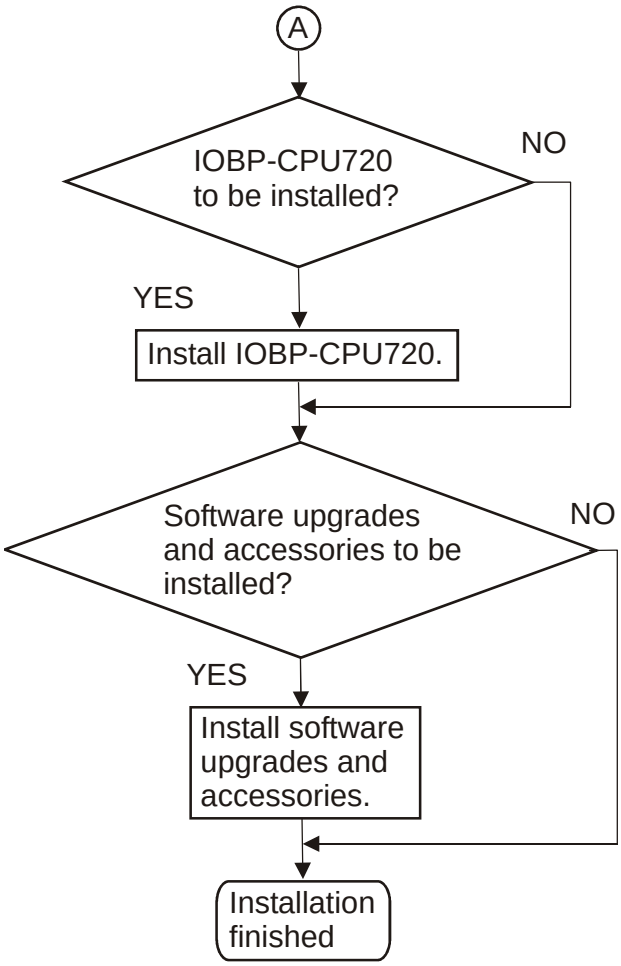
2

Installation

Action Plan

To install the board, the following steps are necessary:




A
IOBP-CPU720
to be installed?
NO
YES
Install IOBP-CPU720.
Software upgrades
and accessories to be
installed?
NO
YES
Install software
upgrades and
accessories.
Installation
finished

Requirements

To meet the environmental requirements, the PENT/CPCI-730 has to be tested in the system where it is to be installed. Before you power up the board, calculate the power needed according to your combination of board upgrades and accessories.

Environmental Requirements

The environmental values must be tested and proven in the used system configuration. The conditions listed below refer to the surroundings of the board within the user environment.

Note: Operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.

Caution



- **To ensure that the operating conditions are met, forced air cooling is required within the chassis environment.**
- **If the standard PENT/CPCI-730/HD-AccKit is installed, the operation temperature of the CPCI-730 is limited by the maximum operation temperature of the hard disk. If the maximum temperature of the hard disk is lower than the maximum temperature of the CPCI-730, the maximum temperature specified for the hard disk must not be exceeded.**

Table 4: *Environmental Requirements*

Feature	Operating	Non-Operating
Temperature[1)]	0°C to +50°C	–40°C to +85°C
Forced Air Flow	300 LFM for CPUs with 266, 333 and 500 MHz.	–
Temp. Change	+/– 0.5°C/min.	+/– 1°C/min.
Rel. Humidity	5% to 95% non-condensing at +40°C	5% to 95% non-condensing at +40°C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m
Vibration[2)]		
10 to 15 Hz	2 mm amplitude	5 mm amplitude
15 to 150 Hz	2 g	5 g

Table 4: *Environmental Requirements (cont.)*

Feature	Operating	Non-Operating
Shock	5 g / 11 ms halfsine	15 g / 11 ms halfsine
Free Fall	100 mm / 3 axis	1,200 mm / all edges and corners (packed state)

1) For information on the allowed hard disk operating temperature, consult the Installation Guide of the PENT / CPCI-730 / HD-AccKit.
2) For information on shock and vibration values that are valid when using the CPCI-730 together with the PENT / CPCI-730 / HD-AccKit, refer to the Installation Guide of the PENT / CPCI-730 / HD-AccKit.

Power Requirements

The CPCI-730 power requirements depend on the installed hardware accessories. The following table gives examples of typical power requirements for 5V and 3.3V for the CPCI-730 without any accessories. If you want to install any accessories, the load of the respective accessory has to be added to the load of the used board variant. For information on the accessories' power requirements, refer to the documentation coming with the respective accessory or ask your local Force Computers representative.

Table 5: *Power Requirements Without Accessories*

PENT/CPCI-730	+5V	+3.3V
.../64-266-L512-0	8.5W	4.62W
.../128-266-L512-16	8.5W	4.95W
.../256-333-L256-16	8W	8.25W
.../256-500-L256-16	10.5W	9.24W

Hardware Upgrades and Accessories

The CPCI-730 itself allows an easy and cost-efficient way to adapt the system board to your application needs.

The following tables gives an overview on the possible combinations of products, described in “Ordering Information Excerpt” page 1-8.

Table 6: *Possible on-board Upgrades and Accessories Combinations*

Option	Mem. Module	PMC Mod.	PMC/VGA	HD Acc. Kit
Mem. Module	-	Mem.: slot 1 PMC: slot 2	Mem.: slot 1 VGA: slot 2	Mem.: slot 1 HD Acc.: slot 2
PMC Mod.	PMC: slot 2, Mem.: slot 1	1 PMC: slot 1 1 PMC: slot 2	PMC: slot 1 VGA: slot 2 or PMC: slot 2 VGA: slot 1	PMC: slot 1 HD Acc.: slot 2
PMC/VGA	VGA: slot 2, Mem: slot 1	VGA: slot 2, PMC: slot 1 or VGA: slot 1. PMC: slot 2	-	VGA: slot 1, HD Acc.: slot 2
HD Acc. Kit	HD Acc.: slot 2 Mem.: slot 1	HD Acc.:slot 2 PMC: slot 1	HD Acc.: slot 2 VGA: slot 1	-

Memory Module

In addition to the local SDRAM of the CPCI-730, the memory module PENT/MEM-700 with SDRAM chips can be installed. The maximum possible memory size of synchronous system memory is 768 MByte. The minimum possible memory size of synchronous system memory is 64 MByte.

For installation information, refer to the Installation Guide delivered together with the memory module.

PMC Module

The board provides two PMC slots. Both slots support a 32-bit data bus width with a maximum frequency of 33 MHz. At the PMC slots +/–12V power applies.

Note: Slot 1 is only available if no memory module is installed. Slot 2 is only available if no on-board hard disk is installed.

PMC slot 1 can be used to install a standard PMC module with front panel interface on the board. It provides no user I/O connector.
PMC slot 2 can be used to install a standard PMC module with front panel interface and rear interface on the board. The third PMC connector connects additional user I/O signals of PMC slot 2 with the J4 connector.

Note:

- **To ensure proper EMC shielding, either operate the board with the blind panels for the PENT/CPCI-730 front panel or with the modules installed.**
- **If the board is upgraded, ensure that the blind panels are stored in a safe place in order to be used again when removing the upgrades.**

Voltage Keys

The PCI bus uses a 5V voltage signal level on the PMC slots. The voltage keys prevent 3.3V PMC cards from being plugged into the PMC slots.

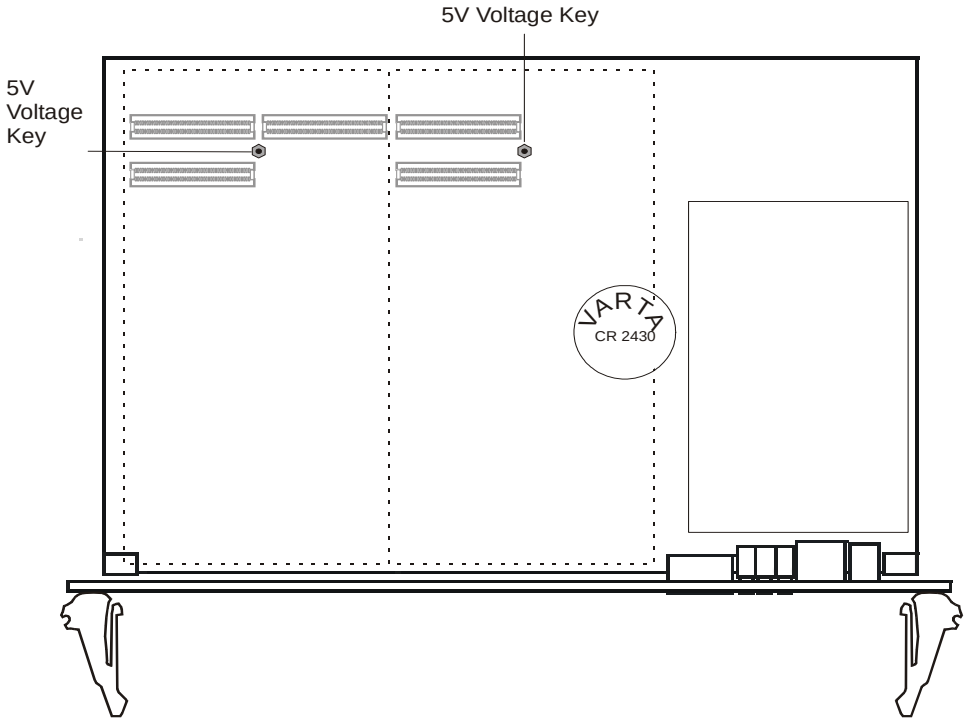


Figure 2: *Voltage Keys*

Installation Procedure

In order to install a PMC module on PMC slot 1 or 2, proceed as follows:

1. Remove memory module from PMC slot 1 or remove hard disk from PMC slot 2, if necessary
2. Remove blind panel of the respective PMC slot from front panel
3. Store blind panel in a safe place

Caution



The total max. power consumption per PMC slot at +/–12V, 5V and 3.3V level must not exceed 7.5W (total over all used voltages).

4. Plug PMC module into connectors of PMC slot 1 (PN11 and 12) or PMC slot 2 (PN21, 22 and 23)

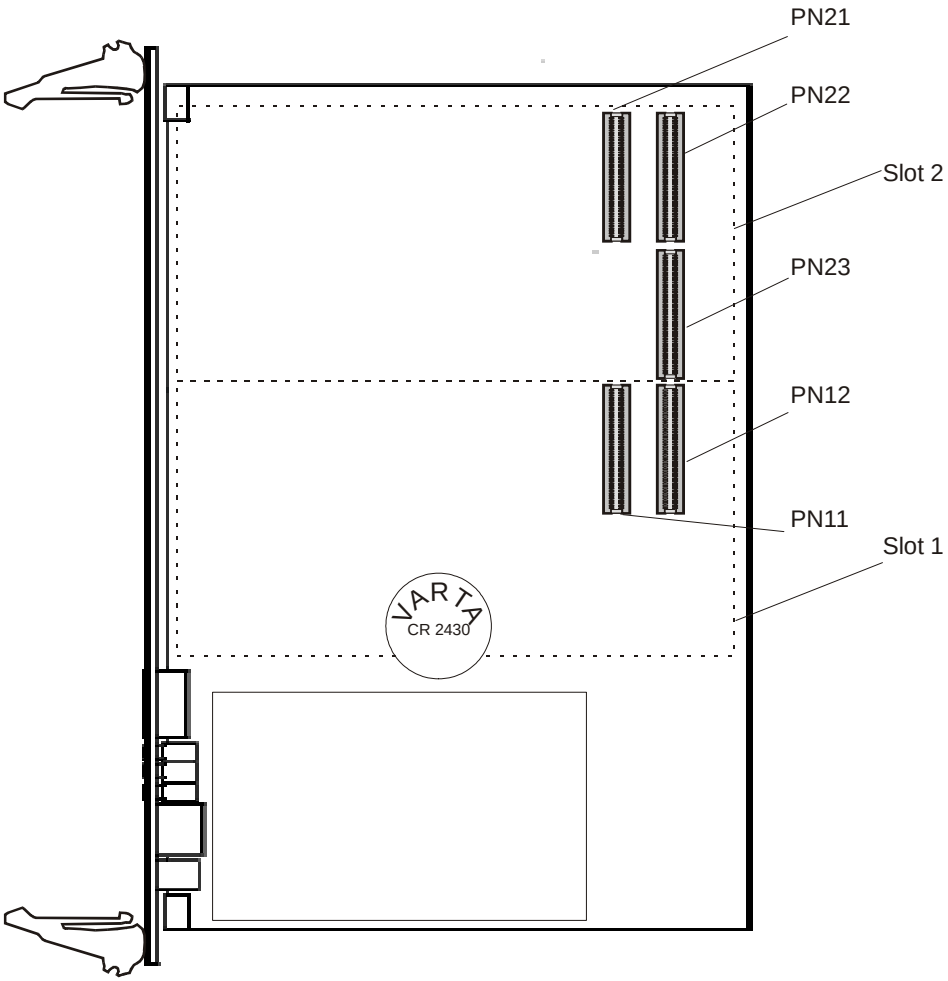


Figure 3: *PMC Connectors and Slots*

5. Check whether the stand-offs of the module cover the mounting holes of the CPCI-730

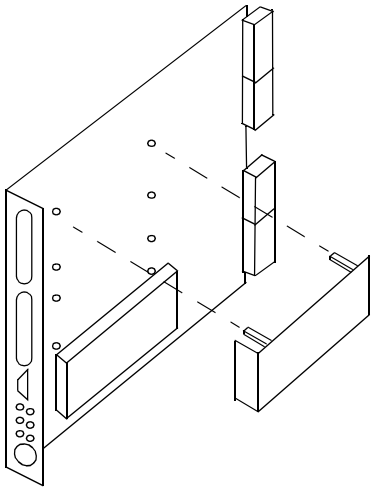


Figure 4: *Position of Mounting Holes*

6. Place screws delivered with PMC module into the mounting holes
7. Fasten screws

Removal Procedure

In order to remove a PMC module, proceed as follows:

1. Remove screws
2. Disconnect PMC module carefully from slot
3. Close front panel gap at free slot with blind panel

PMC/VGA

The PMC/VGA is a PMC based VGA card for the CPCI-730. It can be installed in one of the PMC slots of the CPCI-730.

For installation information, refer to the Installation Guide coming with the PMC/VGA card.

IDE Devices

It is possible to have up to two IDE devices on the CPCI-730:

- As factory option, a 16 MByte flash disk can be installed on the board. It is connected to the primary IDE port.
- A HD-AccKit can be installed at the primary IDE port via the on-board connector.

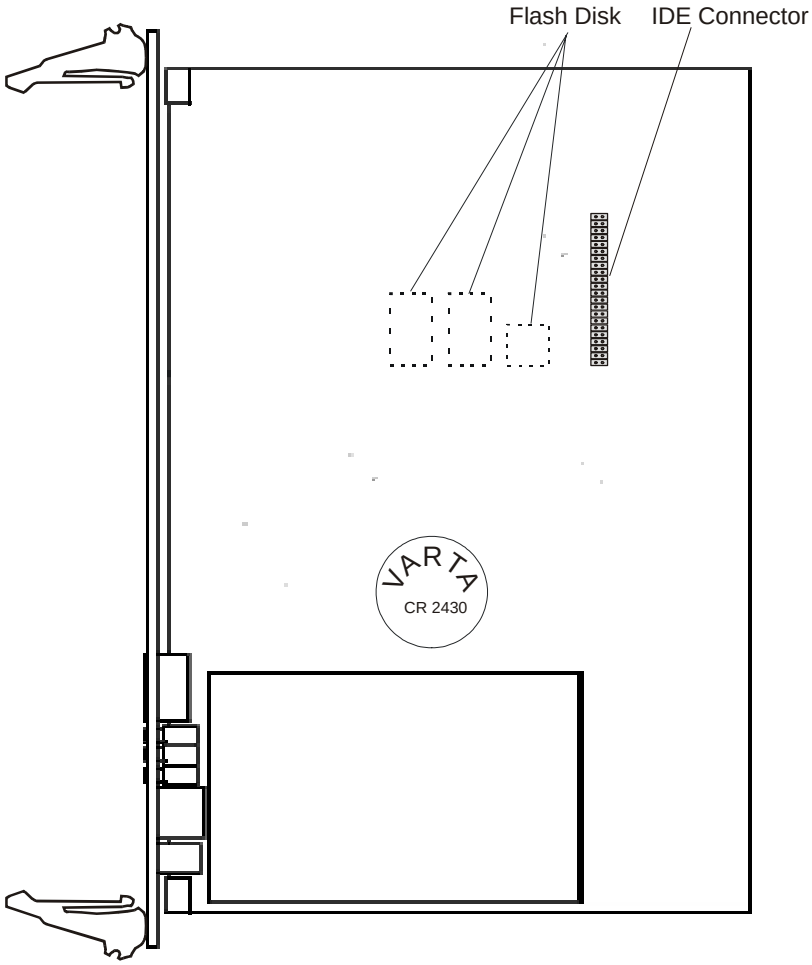


Figure 5: *Flash Disk and IDE Connector*

HD-Accessory Kit

The PENT/CPCI-730/HD-AccKit is a local mass storage device. It has to be connected to the primary IDE port via the on-board connector.

For installation information, refer to the Installation Guide coming with the HD-AccKit.

Caution



If the standard PENT/CPCI-730/HD-AccKit is installed, the operation temperature of the board is limited by the maximum operation temperature of the hard disk. If the maximum temperature of the hard disk is lower than the maximum temperature of the board, the maximum temperature specified for the hard disk must not be exceeded.

Note: If the hard disk is installed on a board with 16 MByte flash disk, either the hard disk or the flash disk has to be set to IDE master. For the configuration options, refer to the Installation Guide coming with the hard disk accessory kit and to "Switch Settings" page 2-14.

IOBP-CPU720

As a separate price list item, the IOBP-CPU720 is offered. It has to be connected to the CPCI-730 after board installation.

The IOBP-CPU720 provides access to the base board's CompactPCI user I/O interfaces via industry standard connectors. It is part of the rear I/O panel PENT/CPCI-720/CPUP5-AccKit, containing the I/O panel itself and the cabling.

Note: Although the IOBP-CPU720 has a primary IDE connector, the primary IDE interface of the CPCI-730 is not connected to it. Any devices connected to the primary IDE connector of the IOBP-CPU720 will not be accessible from the CPCI-730. Signals which are inputs to a connected IDE device are pulled high on the CPCI-730 and will keep the IDE device in an inactive state.

For further information, refer to the Installation Guide coming with the PENT/CPCI-720/CPUP5-AccKit.

Switch Settings

The PENT/CPCI-730 provides two configuration switches, SW1 and SW2.

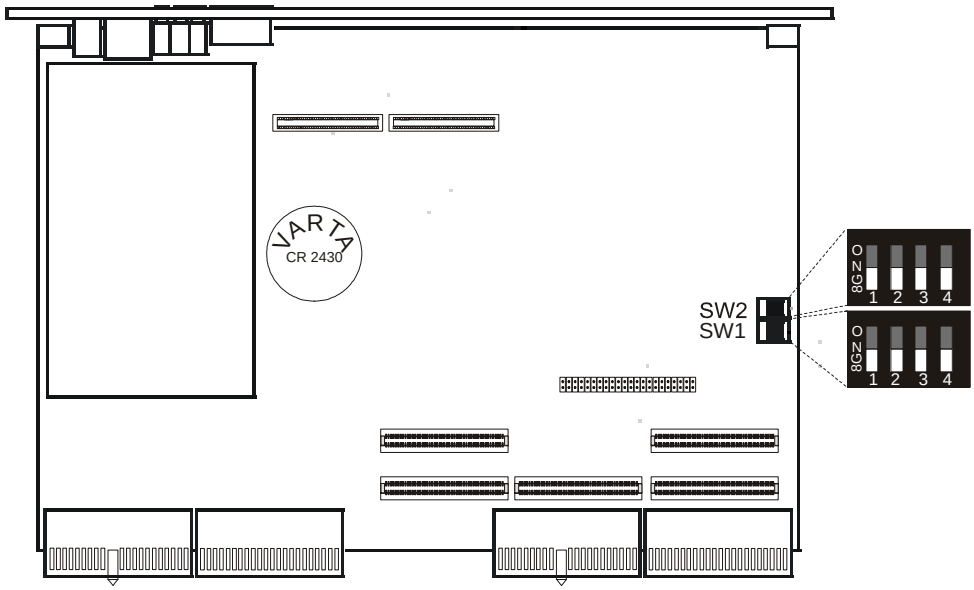


Figure 6: *Switch Sets*

For default settings, the white switches are moved to the OFF position.

Table 7: *Default Settings*

Switch	Number	Description
SW1		
	1	BIOS page select OFF: Normal BIOS operation (default) ON: Alternate BIOS
	2	Page select control OFF: Controlled by switch setting (default) ON: Controlled by software
	3	BIOS Flash memory boot block write protection OFF: Write-protected (default) ON; Writing enabled
	4	Not Used

Table 7: *Default Settings (cont.)*

Switch	Number	Description
SW2		
	1	Reserved for Force Computers internal use, must always be OFF (default)
	2	Flash disk enable OFF: Flash disk disabled (default) ON: Flash disk enabled
	3	Flash disk boot enable OFF: On-board flash disk is primary IDE slave (default). ON: On-board flash disk is primary IDE master.
	4	Front panel reset key enable OFF: Reset key enabled (default) ON: Reset key disabled

Board Installation

The CPCI-730 is a system slot board. It can be used in both, non-hot-swap and hot-swap platforms.

Installation in a Nonpowered System

The CPCI-730 is a CompactPCI-universal board and can be run with either 3.3V or 5V. It automatically probes the power pins to find out whether it is in a 3.3V or a 5V system.

Note: Before installing the board install the accessory kits, if necessary (refer to "Hardware Upgrades and Accessories" page 2-7).

Installation Procedure

In order to install the board in a nonpowered system, proceed as follows:

1. Turn off system power

Caution



Always plug the PENT/CPCI-730 into a system slot of a CompactPCI rack marked by a triangle. Otherwise the board or other cards in the system may be damaged.

2. Plug board in a system slot
3. Press handles inwards to lock board on CompactPCI rack
4. Fasten board with screws
5. Plug in interface cables into front panel connectors, if applicable

Caution



Before powering up the board, check the switch settings for consistency.

6. Turn on system power

Removal Procedure

In order to remove the board from a nonpowered system, proceed as follows:

1. Turn off system power
2. Unfasten two screws of front panel until board is detached from rack frame
3. Press handles outwards to disconnect board from backplane
4. Remove board from rails of slot position

Installation in a Powered System

Note: Before installing the board install the accessory kits, if necessary (refer to "Hardware Upgrades and Accessories" page 2-7).

As a system board the PENT/CPCI-730 can support basic hot swap only. Basic hot swap support allows to install a board in and remove it from a powered system without adversely affecting the system. This is helpful when exchanging faulty boards or reconfiguring a system.

The CPCI-730 is a CompactPCI-universal board and can be run with either 3.3V or 5V. It automatically probes the V (I/O) power pins to find out whether it is a 3.3V or a 5V system.

Note: The PENT/CPCI-730 is compliant to the Hot Swap Specification PICMG 2.1 Rev. 1.0 which defines hot swap only for 5V signaling.

Caution



- **Never install a board in or remove it from a system under hot-swap conditions unless a hot-swap platform is used and the system documentation explicitly includes appropriate guidelines.**
- **Removing a system board will cause the whole CompactPCI system to stop operation.**

Note: When installing or removing the board, refer to the documentation of all installed boards and to the system documentation.

Installation Procedure

In order to install the board in a basic hot-swap system, proceed as follows:

1. Check board configuration (switch settings, accessories)
2. Check installation configuration of rear interface for slot in which board is to be plugged in
3. Insert board into powered system
4. Press handles inwards to lock board on CompactPCI rack
5. Fasten board with two screws on front panel
6. Connect software manually according to system documentation
7. Reboot system

Removal Procedure

In order to remove a board from a basic hot-swap system, proceed as follows:

1. Start removing board by software disconnect using system documentation
2. Check that system disconnection process is completed
3. Unfasten two screws of front panel until board is detached from rack frame
4. Press handles outwards to disconnect board from backplane
5. Remove board from powered system

Software Upgrades and Accessories

As software upgrades and accessories for the board you can get the BIOS-upgrade kit and the NT-Support-Package.

BIOS-Upgrade Kit

The BIOS-upgrade kit PENT/CPCI-730/BIOS-UpKit contains a DOS-formatted floppy disk with BIOS upgrade file and upgrade utilities e.g. to reflect extended hardware support. For installation information, refer to the README file provided on the floppy disk.

NT-Support-Package

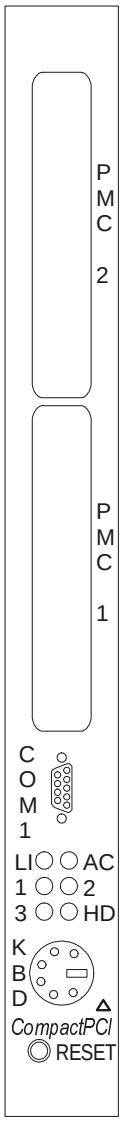
With the PENT/CPCI-730/NT-Support-Package comes a CD-ROM with Windows NT drivers e.g. to reflect extended hardware support for Windows NT (e.g. Ethernet driver). For installation information, refer to the README file on the CD-ROM.

3

Controls, Indicators and Connectors

Front Panel

The following figure highlights the position of cutouts for PMC modules, connectors and LEDs on the CPCI-730 front panel.



PMC Cutouts

The front panel provides two cutouts to install PMC modules.

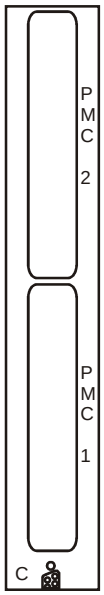


Figure 7: *Cutouts for PMC Module*

LEDs

The following front panel LEDs are provided on the board:

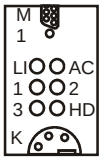


Table 8: *Description of Front Panel LEDs*

LED	Description
1, 2, 3	User LEDs: software programmable by the LED Control Register. Possible LED status: green, red or off
AC	Activity LED: signals network interface activity. This LED is turned on if the PENT / CPCI-730 receives or transmits data via the network interface. Possible LED status: yellow or off
HD	Hard disk LED: signals accesses to devices connected via IDE. Possible LED status: flickering during access activity, else off. The LED color can be customized via the LED Control Register.
LI	Link LED: signals incoming link pulses. This LED is turned on if the network interface has connection to other network devices. Possible LED status: green or off

Keys

The only front panel key used is the mechanical reset key.



When enabled and toggled, it instantaneously affects the system board by generating a main reset. The main reset generates a CompactPCI reset on segment A and B.

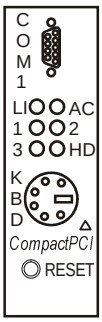
A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. Reset is held active until the key is back in the inactive position, however at least 200 ms are guaranteed by a local timer. Power fail (below approximately 4.7V) and power up – both lasting a minimum of 200 ms to 300 ms – also force a reset to start the system board.

For information on how to disable the key, see Table 7 “Default Settings” on page 2-14 and Table 17 “Switch Control Register” on page 6-9.

Connectors

The PENT / CPCI-730 provides the following front panel connectors:

- Keyboard / Mouse
- COM1



If the board is to be incorporated in larger systems and adapted to specific needs, the following connector pinouts may be useful to give information on which signal is assigned to which pin.

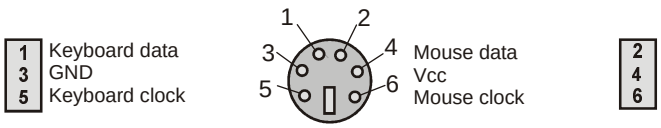


Figure 8: *KBD/MS – Keyboard and Mouse Connector Pinout*

Note: Make sure that the length of keyboard and mouse cables does not exceed three meters and that the cables are installed apart from other cables.

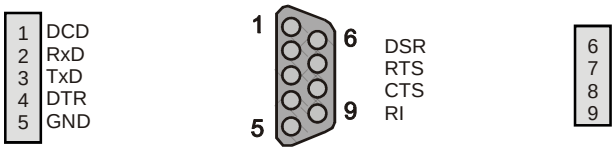


Figure 9: *COM1 Connector Pinout*

CompactPCI Connectors

The board provides the connectors J1, J2, J4 and J5. The interfaces available on the CompactPCI interface can be routed to interface-dependent standard connectors via the IOBP-CPU720.

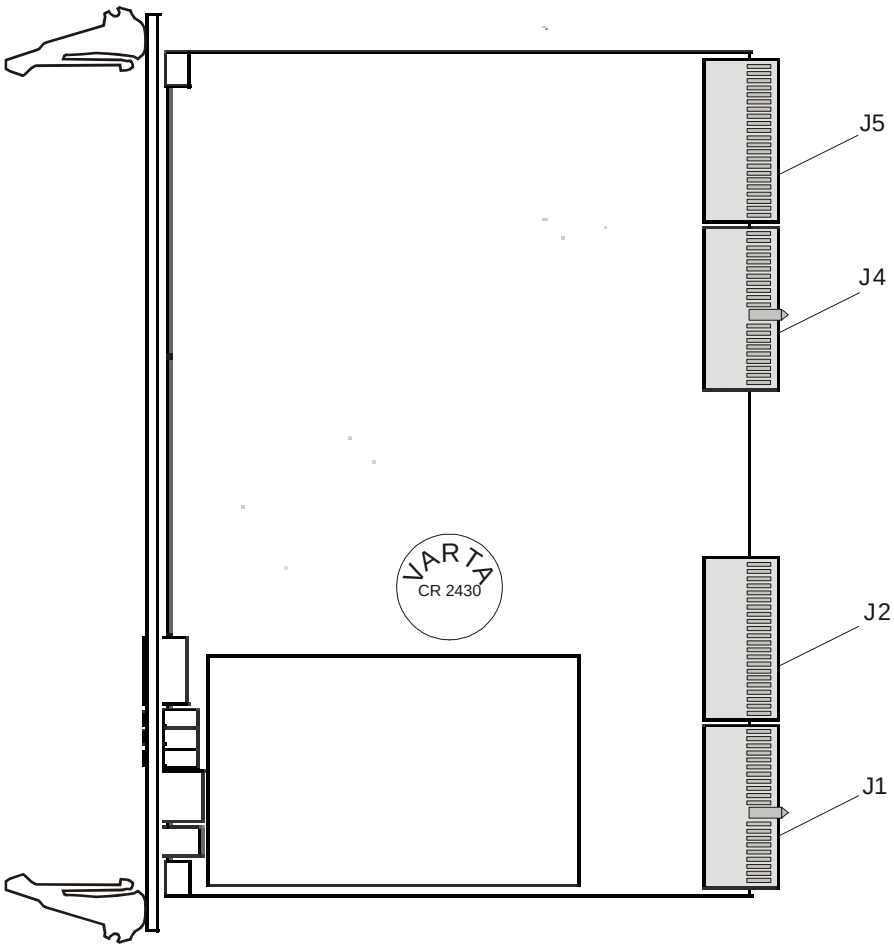


Figure 10: *CompactPCI Connectors*

J1 and J2

The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as specified by the CompactPCI specification. Therefore, this manual only documents the pinout of the J4 and J5 connectors.

J4

The following ports are available on the CPCI-730 J4 connector:

- PMC slot 2 I/O signals (PMC2IOx)
- COM3 (COM3)

	A	B	C	D	E
25	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1
24	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6
23	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11
22	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16
21	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21
20	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26
19	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31
18	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36
17	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41
16	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46
15	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51
14	Key	Key	Key	Key	Key
13	Key	Key	Key	Key	Key
12	Key	Key	Key	Key	Key
11	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56
10	Vcc	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61
9	Reserved	Reserved	Reserved	Reserved	Reserved
8	Reserved	Reserved	Reserved	Reserved	Reserved
7	Reserved	Reserved	Reserved	Reserved	Reserved
6	Reserved	Reserved	Reserved	Reserved	Reserved
5	Reserved	Reserved	Reserved	Reserved	Reserved
4	Reserved	Reserved	Reserved	Reserved	Reserved
3	Reserved	Reserved	Reserved	Reserved	Reserved
2	COM3 RTS	COM3 CTS	COM3 R1	Reserved	Reserved
1	COM3 DCD	COM3 RxD	COM3 TxD	COM3 DTR	COM3 DSR

Figure 11: *J4 Connector Pinout on Standard PENT/CPCI-730*

As a customer assembly option, two additional Ethernet interfaces are available on connector J4 with PCB revision 1.2 or higher. The following ports are available on connector J4:

- PMC slot 2 I/O signals (PMC2IOx)
- COM3 (COM3)
- Ethernet 1 (ETH1)
- Ethernet 2 (ETH2)

	A	B	C	A B C D E	D	E	
25	PMC2IO5	PMC2IO4	PMC2IO3		PMC2IO2	PMC2IO1	25
24	PMC2IO10	PMC2IO9	PMC2IO8		PMC2IO7	PMC2IO6	24
23	PMC2IO15	PMC2IO14	PMC2IO13		PMC2IO12	PMC2IO11	23
22	PMC2IO20	PMC2IO19	PMC2IO18		PMC2IO17	PMC2IO16	22
21	PMC2IO25	PMC2IO24	PMC2IO23		PMC2IO22	PMC2IO21	21
20	PMC2IO30	PMC2IO29	PMC2IO28		PMC2IO27	PMC2IO26	20
19	PMC2IO35	PMC2IO34	PMC2IO33		PMC2IO32	PMC2IO31	19
18	PMC2IO40	PMC2IO39	PMC2IO38		PMC2IO37	PMC2IO36	18
17	PMC2IO45	PMC2IO44	PMC2IO43		PMC2IO42	PMC2IO41	17
16	PMC2IO50	PMC2IO49	PMC2IO48		PMC2IO47	PMC2IO46	16
15	PMC2IO55	PMC2IO54	PMC2IO53		PMC2IO52	PMC2IO51	15
14	Key	Key	Key		Key	Key	14
13	Key	Key	Key		Key	Key	13
12	Key	Key	Key		Key	Key	12
11	PMC2IO60	PMC2IO59	PMC2IO58		PMC2IO57	PMC2IO56	11
10	Vcc	PMC2IO64	PMC2IO63		PMC2IO62	PMC2IO61	10
9	Gnd	Gnd	ETH1LILED		Reserved	Reserved	9
8	ETH1 TX+	ETH1 RX+	ETH1 ACTLED		Reserved	Reserved	8
7	ETH1 TX-	ETH1 RX-	ETH1 SPDLED		Reserved	Reserved	7
6	Gnd	Gnd	ETH2LILED		Reserved	Reserved	6
5	ETH2 TX+	ETH2 RX+	ETH2 ACTLED		Reserved	Reserved	5
4	ETH2 TX-	ETH2 RX+	ETH2 SPDLED		Reserved	Reserved	4
3	Gnd	Gnd	Gnd		Reserved	Reserved	3
2	COM3 RTS	COM3 CTS	COM3 R1		Reserved	Reserved	2
1	COM3 DCD	COM3 RxD	COM3 TxD		COM3 DTR	COM3 DSR	1

Figure 12: *J4 Connector Pinout on PENT/CPCI-730 (Three Ethernet Interfaces)*

J5

The following ports are available on the board's J5 connector:

- Secondary IDE (2nd IDE); primary IDE signals (1st IDE) are shown here but are high-pulled passive signals.
- USB (USB), Keyboard (KBD), PS2 mouse (MS), COM1 (COM1), COM2 (COM2), LPT (LPT), floppy (FD)
- Ethernet 0 (ETH0)

	A	B	C	A B C D E	D	E	
22	COM1 DCD	COM1 RxD	COM1 TxD		COM1 DTR	COM1 DSR	22
21	COM1 RTS	COM1 CTS	COM1 R1		COM2 DCD	COM2 DSR	21
20	COM2 RxD	COM2 TxD	COM2 DTR		COM2 RTS	COM2 CTS	20
19	COM2 R1	/PBRESET	LPT DATA1		LPT DATA2	LPT DATA3	19
18	LPT DATA4	LPT DATA0	LPT DATA6		LPT DATA7	LPT Strobe	18
17	LPT /Autofeed	LPT DATA5	LPT /Slct		LPT /Error	LPT /Ack	17
16	LPT Busy	LPT /Init	LPT /Slct		FD /WDATA	FD /WGATE	16
15	Vcc	LPT Pe	FD /RDATA		FD /TRK0	FD /INDEX	15
14	FD /HDSEL	FD /DIR	FD /STEP		FD /MTR1	FD /DR0	14
13	FD /DSKCHG	FD /WP	FD /MTR0		FD /MSN0	Vcc	13
12	FD /DR1	FD DENSEL	FD DRATE0		IDE D3	IDE D4	12
11	IDE D0	IDE D1	IDE D2		IDE D8	IDE D9	11
10	IDE D5	IDE D6	IDE D7		IDE D13	IDE D14	10
9	IDE D10	IDE D11	IDE D12		1st IDE /IOW	2nd IDE /IOW	9
8	IDE D15	1st IDE DRQ	2nd IDE DRQ		1st IDE DAK	2nd IDE DAK	8
7	1st IDE /IOR	2nd IDE IOR	IDE IORDY		2nd IDE A1	1st IDE A0	7
6	1st IDE /IRQ	2nd IDE IRQ	1st IDE A1		1st IDE /LED	2nd IDE /LED	6
5	2nd IDE A0	1st IDE /CS1	2nd IDE /CS1		2nd IDE /CS3	IDE /RST	5
4	1st IDE A2	2nd IDE A2	1st IDE /CS3		USB P1-	USB P1+	4
3	KBD clock	KBD DATA	MSE clock		MS DATA	Reserved	3
2	ETH0 TX-	SPEAKER	ETH0 TX+		ETH0 RX+	ETH0 RX-	2
1	SMI	APMVCCH	APMONCNTL		APMSWITCH	Reserved	1

Figure 13: *J5 Connector Pinout*

4

BIOS

Introduction

BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the board. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the board for the initial boot-up procedure. BIOS offers the following features:

- Hardware set-up utility for setting configuration data
- Multiboot for a flexible boot order
- Software upgrade utility

The BIOS complies to the following specifications:

- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.1
- BIOS Boot Specification 1.01
- PXE 2.0

The BIOS set-up program is required to configure the hardware of the board. This configuration is necessary for operating the board and connected peripherals. It is stored in the CMOS memory. A battery preserves configuration data when the board is powered off.

When you are not sure about configuration settings, restore the default values. They are provided in case that a value has been changed and one wishes to reset settings.To restore the default values, press <F9> in setup.

Note:

- **Loading the BIOS default values will affect all set-up items and will reset options previously altered.**
- **If you set the default values, the displayed default values are not yet stored to be effective for the next boot. They are just loaded to be displayed. However, they become effective if the BIOS setup is exited after changes have been saved.**

Changing Configuration Settings

When the system is turned on or rebooted, the presence and functionality of the system components is tested by POST (power-on self-test). Press <F1> while the message `Press <F1> to enter SETUP` appears on the screen. The main menu appears.



Figure 14: *Main Menu*

Note:

- **Make sure that BIOS is properly configured prior to installing the operating system and its drivers.**
- **If you save changes in setup, the next time the board boots, BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter Setup to get the default values or to change the selections that caused the failure.**

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the menu window.

Selecting The Boot Device

There are two possibilities to determine the device from which BIOS attempts to boot:

- Via setup to select a permanent order of boot devices
- Via boot selection menu to select any device for the next boot-up procedure only

Via Setup

To determine the order of boot devices in setup, proceed as follows:

1. In the menu line, select [Boot]
2. Select the order of the devices from which BIOS attempts to boot the operating system

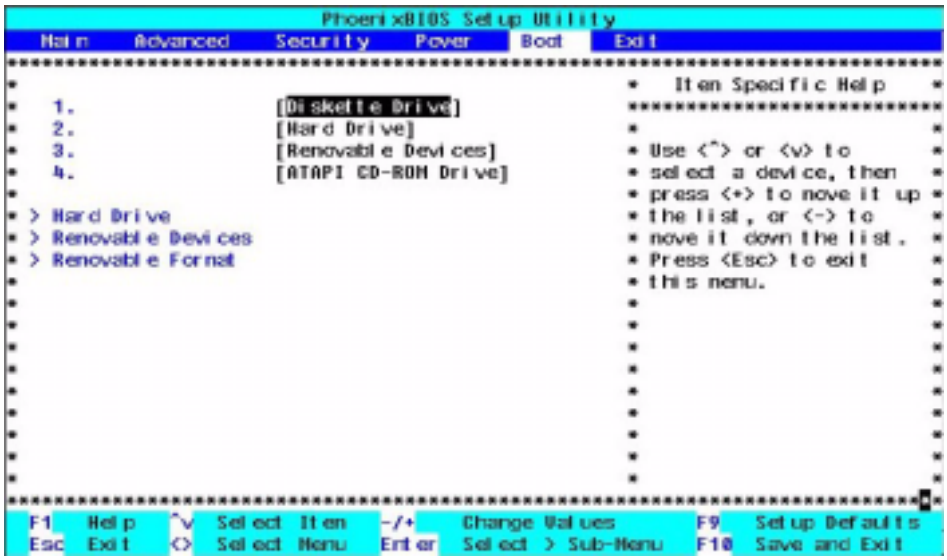


Figure 15: *Boot Device Order*

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list.

If there is more than one device of the same type, e.g. several hard disks, the displayed entry represents the first of these devices as specified in the boot configuration via setup.

The same options determine the order in which POST installs the devices and the operating system assigns device letters. BIOS supports up to two floppy devices to which the operating system may assign drive letters A: and B:. The drives C:, D:, E: etc. are reserved for hard-disk drives.

Note: There is not always an exact correspondence between the order specified in setup and the letters assigned by the operating system. Many devices, such as legacy option ROMs, support more than one device that can be assigned to several letters. If the CD-ROM drive should have a letter coming before the one assigned to the hard drive, move it in front of the hard drive. The group of bootable add-in cards refers to devices with non-multiboot compliant BIOS option ROM from which you can boot the operating system.

Via Boot Selection Menu

To enter the boot menu, press <ESC> during POST.



Figure 16: *Boot Menu*

Continue with one of the following options:

a) Override existing boot sequence by selecting another boot device from the boot order list

Note: If the selected device does not load the operating system, BIOS reverts to the previous boot sequence.

b) Select [Enter Setup] to enter setup utility

c) Press <Esc> to return to POST screen and continue with previous boot sequence

Updating BIOS via Software

For the board the BIOS upgrade kit PENT/CPCI-730/BIOS-UpKit is offered. It contains a DOS-formatted floppy disk with BIOS upgrade file and upgrade utilities e.g. to reflect extended hardware support. For installation information, refer to the README file provided on the floppy disk.

BIOS Messages

The following messages may be displayed, e.g. if your system fails after you made changes in the setup menus. If it is not possible to fix a problem with the help of this section, contact your local sales representative or FAE for further support.

Message	Explanation	Corrective Action
`nnnn Cache SRAM Passed`	*nnnn* is amount of system cache in KBytes successfully tested	None
`CD-ROM Drive Identified`	Autotyping identified CD-ROM Drive	None
`Diskette drive A error` `Diskette drive B error`	Drive A: or B: fails the BIOS POST disk tests. Drive is selected via setup but either not present or defect.	Check that drive is defined with proper disk type in Setup, that disk drive is attached correctly and that controller is enabled.
`Entering SETUP ...`	Starting set-up program	None
`Extended RAM Failed at offset:nnnn`	Extended memory not working or not configured properly at offset *nnnn*	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.
`nnnn Extended RAM Passed`	*nnnn* is amount of RAM in MBytes successfully tested.	None

Message	Explanation	Corrective Action
`Failing Bits:nnnn`	*nnnn* is a map of the bits at the RAM address (in system, extended or shadow memory) which failed the memory test. Each `1` (one) in the map indicates a failed bit.	Check if memory modules are installed correctly. Otherwise contact your local sales representative or FAE for further support.

`Fixed Disk 0 Failure`
`Fixed Disk 1 Failure`
`Fixed Disk Controller Failure`
	Fixed disk not working or not configured properly	Check if fixed disk is attached properly. Run setup to be sure the fixed-disk type is correctly identified.

`Fixed Disk 0...3 Identified`	Autotyping identified specified fixed disk.	None
`Incorrect Drive A type - run SETUP` `Incorrect Drive B type - run SETUP`	Type of floppy drive not correctly identified in setup	Check for correct floppy drive in setup.
`Keyboard controller error`	Keyboard controller failed test	Replace keyboard
`Keyboard error`	Keyboard not working	Check for correct keyboard connection.
`Keyboard error nnn`	BIOS discovered a stuck key and displays scan code *nn* for stuck key.	Replace keyboard, check for stuck keys.
`Operating system not found`	Operating system cannot be located on either drive A:or drive C:.	Enter setup and check if fixed disk and drive A: are properly identified.
`Parity Check 1 nnnn`	Parity error found in system bus. BIOS attempts to locate address *nnnn* and display it on screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.

Message	Explanation	Corrective Action
`Parity Check 2 nnnn`	Parity error found in system bus. BIOS attempts to locate address *nnnn* and display it on the screen. If it cannot locate the address, it displays ????.	Check for correct memory module types.
`Press <F1> to resume, <F2> to set up`	Displayed after any recoverable error message	Press <F1> to start boot process or <F2> to enter setup and change any settings.
`Previous boot incomplete - Default configuration used`	Previous POST did not complete successfully. POST loads default values and offers to run setup. If failure was caused by incorrect values and they are not corrected, the next boot will likely fail.	Run setup to restore original configuration. This error is cleared the next time the system is booted.
`Real time clock error`	Real-time clock fails BIOS test.	May require board repair
`Resource allocation conflict on motherboard - Run Configuration Utility`	Possible interrupt or interface resource conflict.	Run ISA or EISA Configuration Utility to resolve resource conflict.
`Shadow RAM Failed at offset:nnnn`	Shadow RAM failed at offset *nnnn* of the 64k block at which error was detected.	Contact your local sales representative or FAE for further support.
`nnnn Shadow RAM Passed`	*nnnn* is amount of shadow RAM in KBytes successfully tested.	None
`System battery is dead - Replace and run SETUP`	The NVRAM (CMOS) clock battery indicator shows the battery is dead.	Replace battery and run setup to reconfigure system.
`System BIOS shadowed`	System BIOS copied to shadow RAM	None
`System cache error - Cache disabled`	RAM cache failed BIOS test. BIOS disabled cache.	Contact your local sales representative or FAE for further support.

Message	Explanation	Corrective Action
`System CMOS checksum bad - run SETUP`	System NVRAM (CMOS) has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in NVRAM (CMOS).	Run setup and reconfigure system either by getting default values and / or making your own selections.
`System RAM Failed at offset:nnnn`	System RAM failed at offset *nnnn* in the 64k block at which the error was detected.	Check for correct memory modules. Otherwise contact your local sales representative or FAE for further support.
`nnnn System RAM Passed`	*nnnn* is amount of system RAM in KBytes successfully tested.	None
`System timer error`	Timer test failed.	Requires repair of system board.
`UMB upper limit segment address:nnnn`	Address *nnnn* of the upper limit of upper memory blocks indicates released segments of BIOS which may be reclaimed by a virtual memory manager.	None
`Video BIOS shadowed`	Video BIOS successfully copied to shadow RAM.	None
`Invalid System Configuration Data – run configuration utility`		Enter setup and use advanced configuration option to reset configuration data (due to corrupted ESCD data).

5

Buses

I^2C Bus

The board contains three serial busses which use the I^2C serial protocol. Via these serial busses the CPU can access board status sensors (temperature, voltages), memory sizes etc.

The CPCI-730 contains a serial EEPROM free for applications. The EEPROM has a size of 256 bytes. The I^2C bus is also available on the CompactPCI backplane where more serial devices can be connected.

Table 9: *Module Information I^2C Bus*

Device Name	Device Type	Function	Location	Address
Reserved	24C04	Reserved	Base board	1010000_2
	24C02		Memory module	1010011_2
MEEPROM3	24C02	Free for applications	Base board	1010010_2

System Management Bus

This serial bus is used for the PC-compatible serial devices which comply with the SBus specification from Intel. The bus contains the temperature sensor on the Pentium II Mobile Module, the hardware monitor chip W83781D and one SPD serial EEPROM for the first and second memory bank. If the memory module is installed, two SPD serial EEPROMs on the module are visible on this bus as well. They contain information for memory banks two to five. The SPD serial EEPROMs are built with the 24C02 version.

Table 10: *System Management I^2C Bus*

Device Name	Device Type	Function	Location	Address
SPDEEPROM1	24C02	Memory bank 0, 1 information	Base board	1010000_2
SPDEEPROM2	24C02	Memory bank 2, 3 information	Memory module	1010001_2
SPDEEPROM3	24C02	Memory bank 4, 5 information	Memory module	1010010_2
TEMPSENSE1	MAX.	Temperature sensor	Pentium II mobile module	1001110_2
HWMON	W83781D	Hardware monitor chip	Base board	0101101_2 1)

1) Power on default value, can be altered via software

Hot-Swap Bus

This bus is connected to the geographical address line GA[3] and GA[4] of the CompactPCI bus. It is intended to communicate with a hot-swap controller placed on the CompactPCI backplane. This is the only device which can be seen on this serial bus if existent. The hot-swap controller is not part of the board but may reside on the system's backplane.

Table 11: *Hot-Swap I^2C Bus*

Device Name	Device Type	Function	Location	Address
HSWAPCNTR	Depends on backplane implementation	Hot-swap controller	Backplane	Depends on backplane implementation

6

Maps and Registers

Overview

Following the block diagram for the CPCI-730, this section gives an overview on the I/O and memory maps and describes all board-specific registers.

Table 12: *Register Overview*

Register map	Description:
Flash Page Select	Page 6-14
Flash Device and SERR	Page 6-15
Flash Write Enable	Page 6-16
Hot-Swap ENUM	Page 6-13
Hot-Swap I^2C Bus	Page 6-12
I^2C	Page 6-8
LED Control	Page 6-16
Lock / Unlock	Page 6-7
NMI Status	Page 6-11
PCI Bus Control	Page 6-11
Serial Port 3 Control	Page 6-17
Switch Control	Page 6-9
Watchdog Control and Retrigger	Page 6-10

I/O and Memory Maps

Table 13: *I/O Map*

I/O Address	Device EIDE, PCI-to-ISA bridge	Keyboard, PS2 mouse, COM1, COM2, LPT1, floppy	
$0000_{16}..001F_{16}$	x		DMA controller 1
$0020_{16}..003F_{16}$	x		Interrupt controller 1
$0040_{16}..005F_{16}$	x		Counter and timer
0060_{16}		x	Keyboard controller
0061_{16}	x		NMI status and control
0064_{16}		x	Keyboard controller
$0070_{16}..0071_{16}$	x		RTC and NMI mask
$0080_{16}..009F_{16}$	x		DMA page register
$0100_{16}..010F_{16}$		(x)	Board-specific registers (partially implemented in separate programmable logic device (PLD))
$00A0_{16}..00BF_{16}$	x		Interrupt controller 2
$00C0_{16}..00DF_{16}$	x		DMA controller 2
$00E0_{16}..00FF_{16}$	n.a.		Coprocessor
$0170_{16}..0177_{16}$	x		Secondary EIDE / ATAPI
$01F0_{16}..01F7_{16}$	x		Primary EIDE / ATAPI
$0295_{16}..0296_{16}$	n.a.		Hardware monitor
$02E8_{16}..02EF_{16}$			COM3, if enabled via serial Port 3 control register
$02F8_{16}..02FF_{16}$		x	COM2
$03BC_{16}..03BF_{16}$		x	LPT1
$03C0_{16}..03DA_{16}$	n.a.		Graphic controller
$03E8_{16}..03EF_{16}$			COM3, if enabled via serial port 3 control register
$03F2_{16}..03F7_{16}$		x	Floppy-EIDE / ATAPI
$03F8_{16}..03FF_{16}$		x	COM1

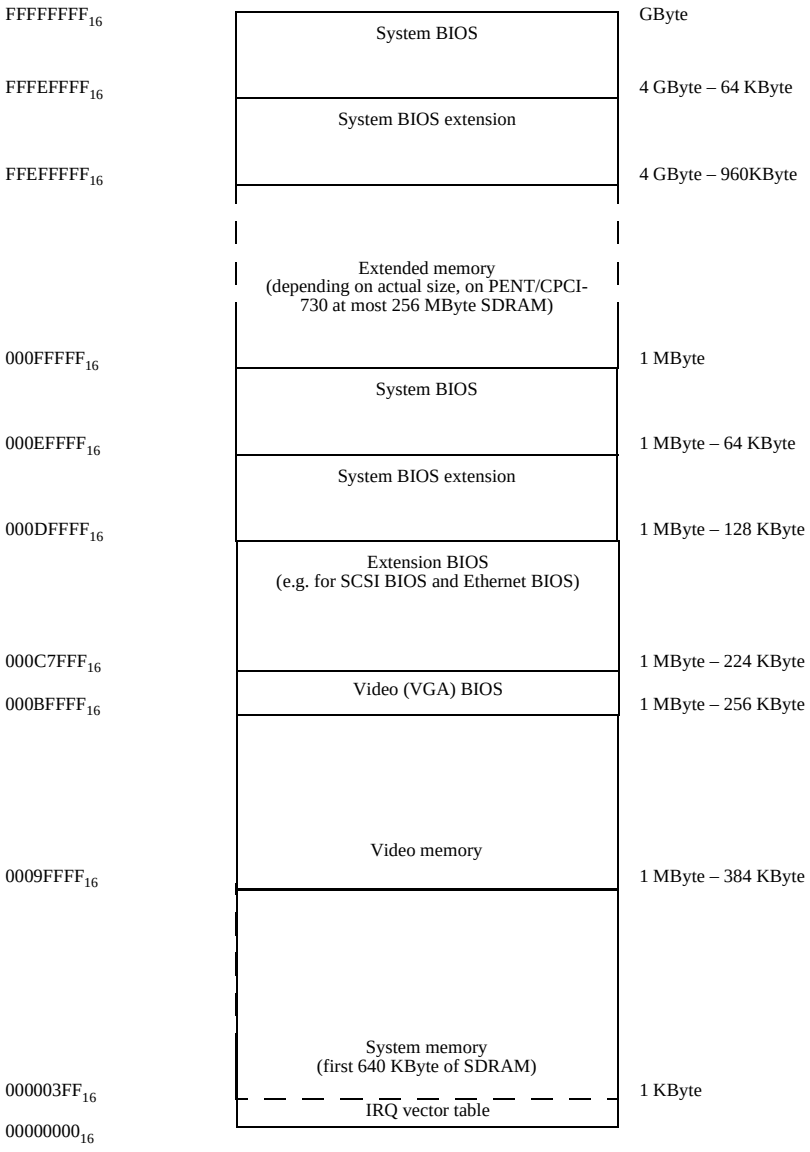


Figure 17: *Memory Map*

Board-Specific Registers

Table 14: *Register Location*

I/O Base$_{16}$	Chip Select	I/O Offset$_{16}$	Function	Comment
100	PCS0 PCI-to-ISA bridge	0	LED Control register	1) 3)
		1-2	Reserved	
		3	Flash Write Enable register	2) 3)
		4	Flash Page Select register	2) 3)
		5	Serial Port 3 Control register	2) 3)
		6	Hot-Swap ENUM register	2) 3)
		7	Hot-Swap bus	2) 3)
		8	I^2C register	1) 3)
		9	Switch Control register	1) 3)
		A	Watchdog Control register	1) 3)
		B	PCI Bus Control register	1) 3)
		C	NMI Status register	1) 3)
		D	Watchdog Retrigger register	1) 3)
		E	Lock / Unlock register	1)
		F	Flash Selection register	2) 4)
Via PCI configuration space, Intel21150	Within PCI-to-PCI bridge	65,66,67	PMC Slot identification	2) 5) 6)
Dynamically by BIOS 7)	Within PCI-to-ISA bridge	32	Geographical address	2) 4) 8)
295, 296	PCS1 PCI-to-ISA bridge	0	Hardware monitor	2) 4)

1) Already implemented on PENT/CPCI-720
2) Feature introduced with PENT/CPCI-730
3) Register controlled by lock feature
4) Register not implemented on PENT/CPCI-730-C1/256-333-L256-0

5) Register not controlled by lock feature
6) General purpose I/O local PCI-to-PCI bridge
7) Read base via PIIX4 PCI configuration space for function 3, offset 40_{16}-43_{16}
8) General purpose inputs GPI<20..16> (PIIX4) == GA<4..0> (CPCI)

Lock/ Unlock Register

The Lock/Unlock register enables or disables read and write access to the board-specific registers.

Table 15: *Lock/ Unlock Register*

Address: $010E_{16}$			
Bit	**Signal**	**Description**	**Access**
2..0	B2..B0	Specifies whether board-specific registers are unlocked or locked. 010_2: Unlocked Other values: Locked (default)	r/w
3	Reserved	Reserved	r

I^2C Register

The I^2C register is used for data transfer settings on the I^2C bus and provides access to the program-readable vintage registers for the base board, and the memory modules.

Table 16: *I^2C Register*

Address: 0108_{16}			
Bit	**Signal**	**Description**	**Access**
0	DIR	Direction bit for I^2C data 0: Data is written to the data line. 1: Data is read from the data line (default).	r / w
1	CLK	Clock line of I^2C bus 0: Clock line low 1: Clock line high (default)	r / w
2	DATA_IN	Stores current value of data line 0: Data line low 1: Data line high	r
3	Reserved	Reserved	r

Switch Control Register

The Switch Control register specifies switch and interrupt related settings.

Table 17: *Switch Control Register*

Address: 0109_{16}			
Bit	**Signal**	**Description**	**Access**
0	SW_RESET	SW_RESET and SW2D control whether reset key is enabled or disabled. 0: Reset key disabled 1: Reset key enabled if SW2D is OFF (default)	r / w
3..1	Reserved	Reserved	r

Watchdog Control and Retrigger Register

The Watchdog Control register specifies watchdog related settings. The default watchdog time-out value is set to approximately 1.5s.

Table 18: *Watchdog Control Register*

Address: $010A_{16}$			
Bit	**Signal**	**Description**	**Access**
0	WDOG_ON	Controls whether watchdog timer is enabled or disabled. 0: Watchdog timer enabled 1: Watchdog timer disabled (default)	r / w
1	WDOG_RESET / NMI	Controls whether an NMI or a RESET is caused if watchdog timer is not retriggered within time-out period 0: NMI is caused 1: Reset is caused (default). For information whether the reset is local or global, refer to the RESET_BUS (r / w) bit in the PCI Bus Control register (Page 6-11).	r / w
2	WDOG_TIME-OUT	Controls whether watchdog time-out is 1.5s or 6s 0: Watchdog time-out set to approximately 6s 1: Watchdog time-out set to approximately 1.5s (default)	r / w
3	Reserved	Reserved	r

Table 19: *Watchdog Retrigger Register*

Address: $010D_{16}$			
Bit	**Signal**	**Description**	**Access**
0	WDOG_RETR	Toggling this bit retriggers watchdog timer if watchdog is enabled. This must be done at least every 1.5 s / 6s to prevent a watchdog time-out.	w
3..1	Reserved	Reserved	r

PCI Bus Control Register

The PCI Bus Control register is used to control the function of the reset signal of the PENT/CPCI-730 CompactPCI interface.

Note: The term 'global reset' refers to all segments the PENT/CPCI-730 is connected to.

Table 20: *PCI Bus Control Register*

Address: $010B_{16}$			
Bit	**Signal**	**Description**	**Access**
0	RESET_BUS	Controls whether a PCI reset stays local on PENT/CPCI-730 or is routed globally to CompactPCI system 0: Local PCI reset is caused. 1: Global reset is caused (default).	r/w
3..1	Reserved	Reserved	r

NMI Status Register

The NMI Status register indicates the device which caused an NMI and enables clearing all of its status bits via a write access to the register.

Table 21: *NMI Status Register*

Address: $010C_{16}$			
Bit	**Signal**	**Description**	**Access**
0	Reserved	Reserved	r
1	WDOG	Indicates whether watchdog timer caused an NMI since last clearance of the status bits via a write access to the register. 0: No NMI caused 1: NMI caused	r
3..2	Reserved	Reserved	r

Hot-Swap I^2C Register

The I^2C register is used for data transfer between the PENT/CPCI-730 and a hot-swap controller on the backplane. The geographical address line GA[3] is used as the CLK line. The geographical address line GA[4] is used as the DIR and DATA IN line. The output bus drivers and the pull-up resistors at the I^2C bus must be enabled via EN before a data transfer between the PENT/CPCI-730 and the hot-swap controller can take place.

Table 22: *Hot-Swap I^2C Register*

Address: 0107_{16}			
Bit	**Signal**	**Description**	**Access**
0	DIR	Specifies direction of data transfer. 0: Data is written to data line. 1: Data is read from data line (default).	r/w
1	CLK	Clock line of I^2C bus	r/w
2	DATA IN	Stores current value of data line.	r
3	EN	Enables line drivers and pull-up resistors of hot-swap I^2C bus 0: Line drivers tree-stated and pull-up resistors disabled All register bits can be written or read (default) 1: Line drivers and pull-up resistors enabled	r/w

Hot-Swap ENUM Register

The ENUM register is used to detect the assertion of the hot-swap ENUM signal. The ENUM signal can either be polled via the register or an enumeration can cause an interrupt on level 11.

Table 23: *Hot-Swap ENUM Register*

Address: 0106_{16}			
Bit	**Signal**	**Description**	**Access**
0	ENUM	Shows logic level of ENUM at CompactPCI backplane 0: ENUM asserted 1: ENUM not asserted	r
1	MASK	Used to mask ENUM interrupt 0: ENUM interrupt masked, no interrupts will occur 1: ENUM interrupt unmasked, interrupt will occur if ENUM signal on CompactPCI backplane is asserted	r / w
2	IRQ	Shows the status of the interrupt line 0: No ENUM interrupt pending (default) 1: ENUM interrupt line has been asserted and is still active.	r
3	Reserved	Reserved	r

Flash Page Select Register

The Flash Page Select register is used to switch the on-board flash device into two different modes. In normal operation the complete flash address range is visible to the CPU (1 MByte). The second mode switches the second memory half of the flash onto the first half thus resulting in 512 KByte memory. The page select feature can be used to boot from the second page after a warm reset e.g. to load an embedded operating system located within the flash chip.

The register only takes effect if switch SW1B is set to the ON position. If the switch is set to the OFF position, the page select can be done via switch SW1A (see the “Switch Settings” section on page 2-14).

Table 24: *Flash Page Select Register*

Address: 0104_{16}			
Bit	**Signal**	**Description**	**Access**
0	PAGE	Selects between two page modes of flash memory 0: Complete flash memory address range visible to CPU (default) 1: Second memory half of flash becomes the first one and only 512 KByte of flash memory are visible to CPU.	r / w
3..1	Reserved	Reserved	r

Flash Device and SERR Register

The default flash memory capacity on the board is 1 MByte in one device. By assembly option the flash memory capacity can be extended to 4 MByte in four devices. The BIOS address range is only 1 MByte. Therefore this register is used to select one out of four flash memory devices that can be accessed in the 1 MByte BIOS address range.

Besides this register controls the routing of the BX SERR (System Error) output.

Table 25: *Flash Device and SERR Register*

Address: $010F_{16}$			
Bit	**Signal**	**Description**	**Access**
1..0	FLASH_SEL	Selects one of four flash memory devices 00: Flash memory device 0 selected (default) 01: Flash memory device 1 selected 10: Flash memory device 2 selected 11: Flash memory device 3 selected	r/w
2	SERR_SEL	Selects routing of the BX SERR (System Error) output 0: SERR routed to the PIIX4 EXTSMI input 1: SERR routed to the PIIX4 SERR input (default)	r/w
3	Reserved	Reserved	r

Flash Write Enable Register

The Flash Write Enable register is used to allow write accesses to the on-board flash memory device for update purposes. In normal operation the flash device is write-protected via this register, i.e. the programming voltage is turned off.

Table 26: *Flash Write Enable Register*

Address: 0103_{16}			
Bit	**Signal**	**Description**	**Access**
0	WE	Selects between write protect and write enable mode of flash memory device 0: Flash memory device write-protected (default) 1: Flash memory device enabled for write accesses	r / w
3..1	Reserved	Reserved	r

LED Control Register

The LED Control registers specify the status of the LEDs.

Table 27: *LED Control Register*

Address: 0100_{16}			
Bit	**Signal**	**Description**	**Access**
1..0	2_LEDSTAT	Status LED 2 00_2: LED off 01_2: LED red 10_2: LED green 11_2: LED off	r / w
3..2	1_LEDSTAT	Status LED 1 00_2: LED off 01_2: LED red 10_2: LED green 11_2: LED off	r / w
5..4	HD_LEDSTAT	Specifies color of HD LED 01_2: LED red during HD access 10_2: LED green during HD access Other values: Reserved	r / w
7..6	3_LEDSTAT	Status LED 3 00_2: LED off 01_2: LED red 10_2: LED green 11_2: LED off	r / w

Serial Port 3 Control Register

The Serial Port 3 Control register is used to control serial port 3.

Table 28: *Serial Port 3 Control Register*

Address: 0105_{16}			
Bit	**Signal**	**Description**	**Access**
0	SEN	Enables serial controller. 0: Serial controller disabled 1: Serial controller enabled on I/O address defined with IOA.	r/w
1	IOA	Defines I/O base address of serial port 3. 0: I/O base address of serial port 3 is $03e8_{16}$ (default) 1: I/O base address of serial port 3 is $02e8_{16}$.	r/w
2	MASK	Enables/disables interrupt output of serial port 3 controller. 0: Interrupt output masked (disabled) 1: Interrupt output enabled (default) The interrupt of the serial controller is connected to interrupt IRQ9.	r/w
3	Reserved	Reserved	r

PMC Slot Identification

The PMC slot identification mechanism is used to detect if a PCI bus compliant module (i.e. PMC) is plugged on one of the PMC module sockets. For the detect mechanism four signals (BUSMODE4-BUSMODE1) are used. BUSMODE2, 3, and 4 is a signal group generated by the PMC host. Each PMC socket has one BUSMODE1 signal which is pulled high on the host side. BUSMODE2, 3 and 4 are fixed to a certain logic level (001_2) to indicate that the host board is capable of driving the PCI bus protocol. A module using the PCI bus protocol should drive the BUSMODE1 pin low to indicate the host that it is capable of driving the PCI bus protocol.

Note: The board accepts PMC cards which do not drive the BUSMODE1 pin low. Application software may use the described detect mechanism to verify if a PMC card is installed.

The BUSMODE1 signal of PMC slot 1 and 2 are connected to general purposes I/O pins of the PCI-to-PCI bridge. This bridge is used to connect the PMC slots to the local PCI bus of the CPCI-730. The general purpose I/O pins used to read the logic level of the BUSMODE1 signals must be configured as inputs (default setting).The general purpose registers are accessible via the PCI configuration space of the Intel21150 PCI-to-PCI chip.

Table 29: *Busmode/GPIO Routing*

General Purpose I/O Pin	PMC slot
GPIO0	2
GPEI1	1

Table 30: *General Purpose I/O Registers in Intel21150*

Base Address	I/O Offset	Function
Via PCI configuration space, Intel21150	0x65	GPIO output data register
	0x66	GPIO output enable control register
	0x67	GPIO input data register

For a complete description of the general purpose I/O registers, refer to the data sheet of the Intel21150 PCI-to-PCI chip (see “Other Sources of Information” page xvii).

Geographical Address

The CompactPCI geographical address can be read via a general purpose register within the PCI-to-ISA bridge.

The geographical address lines GA[4..0] of the CompactPCI bus are connected to the general purpose pins GPI[20..16]. The logic levels of these inputs can be read via the general purpose input register of the PCI-to-ISA bridge.

The base address of the general purpose inputs of the PCI-to-ISA bridge is set by the BIOS during run-time. Prior to an access to the GPI registers, the actually used base address must be read by the user software at offset 40_{16}-$43h_{16}$ in the PCI configuration space for function 3.

For a complete description of the general purpose input registers, refer to the data sheet of the 82371AB PCI-to-ISA chip.

Table 31: *Geographical Address Lines/GPI Routing*

General Purpose I/O Pin	Geographical Address Line
GPI16	GA0
GPI17	GA1
GPI18	GA2
GPI19	GA3
GPI20	GA4

Table 32: *General Purpose Input Registers in the 82371AB*

Base Address	I/O Offset	Function
Dynamically by BIOS	30, 31, 32_{16}	General purpose input register
	4C, 4D, 4E, $4F_{16}$	General purpose input control register

Hardware Monitor

The PENT/CPCI-730 contains a hardware monitor chip which monitors the local board temperatures and voltages.

Temperatures are monitored via three temperature sensors located on top of the board.

Monitored voltages are +5V, +3.3V, +12V, -12V and the two +2.5V voltages from the mobile module which are used for the clock reference.

Note: The maximum input voltage at the hardware monitor is 4.095V except the 5V input. To measure +/-12 V, the respective inputs are scaled with resistors. Software which sets up the hardware monitor must consider this scale.

Table 33: *Monitored Board Voltages versus Hardware Monitor Voltage Inputs*

Board Voltage	Voltage Input	Scale
+5V	+5VIN	1.0
Short to GND	-5VIN	None
+3.3V	+3.3VIN	1.0
+12V	+12VIN	0.26
-12V	-12VIN	-0.28
VCPUIO, 2.5V	VCOREA	1.0
VCLK, 2.5V	VCOREB	1.0

You can program thresholds for voltages and temperatures. If any voltage is out of the predefined range or the threshold temperature is reached, the chip generates an alarm (external system management interrupt, EXTSMI). The hardware monitor can be addressed either by using the system management bus (SMB) via the PCI-to-ISA bridge or directly via CPU I/O cycles at the ISA bus.

Table 34: *Hardware Monitor Base Address*

Base Address	PCI-to-ISA Chip Select	Used Bus
295_{16},296_{16}	1	ISA
0101101_2	None	SMB

In order to initialize the hardware monitor chip, Winbond Hardware Doctor is provided on the CD coming with the product, providing a user interface under WinNT. For further information on how to use the software, refer to the README file on the CD.

A

Battery Exchange

Dear Customer,

The battery provides a data retention of five years summing up all periods of actual battery use. Force Computers therefore assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.

Caution



- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, backup affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is installed, for example 3V Li-MN battery of type CR2430.**

The battery is located at the side of the heatsink.

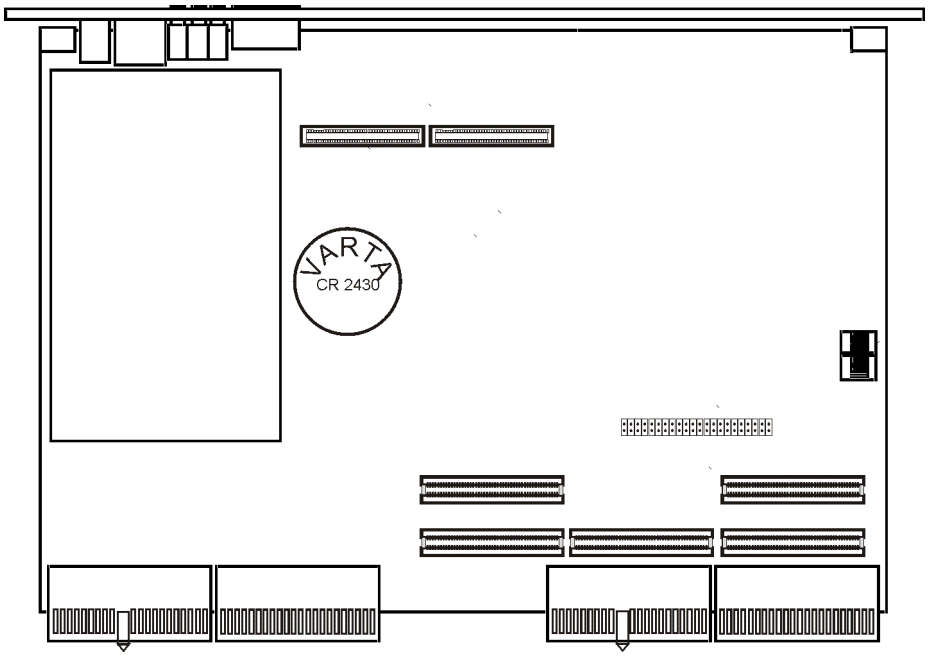


Figure 18: *Battery Location*

1. If battery is covered by PMC module or memory module, remove module first

Caution



To avoid possible damage to the PCB or the battery holder do not use a screwdriver but a pair of tweezers to remove the battery from its holder.

2. Remove battery
3. When installing new battery ensure that the '+' on top of battery stays at top and therefore is visible when viewing board from its component side
4. If necessary, reinstall PMC or memory module in its correct position

B

Troubleshooting

Dear Customer,

a typical CompactPCI system is highly sophisticated. This chapter can be taken as a hint list for detecting erroneous system configurations and strange behaviors. It cannot replace a serious and sophisticated pre- and post- sales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or FAE for further support.

Problem	Possible Reason	Solution
Application software does not work	Memory ranges of system and peripheral boards do not match.	Change application software so that memory ranges match I/O cards and host.
	Not enough disk capacity on mass storage device	Add disk capacity
	Not enough system memory	Add system memory
	Used I/O ranges do not match	Change application software so that I/O ranges match I/O cards and host.
Board does not boot	Boot device is not partitioned according to used operating system	Check partition according to the operating system's needs.
	Boot sequence not correct	Correct the boot sequence.
	Interrupts are not set correctly	Set interrupts correctly.
	Memory's timing parameters in firmware are outside specified ranges of used memory type	Set timing parameters correctly if configurable.
	Wrong configuration of boot devices	Configure boot devices correctly
Board does not work	Backplane defect	1. Check CompactPCI slot position to be used for bent or broken pins 2. Replace damaged backplane
	Backplane voltages wrong or missing	1. Check that all backplane voltages are within their specific ranges 2. Check that power supply is capable to drive the respective loads

Problem	Possible Reason	Solution
	Board connected to wrong slot	Connect system boards to system slots only. System slots are marked with a triangle around the slot number. Connect peripheral boards to I/O slots only. I/O slots are marked with a circle around the slot number.
	Board defect	Replace board
	Cables not connected	Connect all cables.
	Cables connected to wrong connector	Check if plug fits into connector. Reconnect all cables to right connectors.
	Damaged plugs, bent or broken pins	Replace board.
Board functions do not work	Functions are disabled	Configure board correctly.
Board runs unstable	Disregard of environmental requirements	1. Check that temperature inside system stays within specified ranges for all system devices 2. Check for hot-spots within system Improve cooling system if necessary 3. Check that other environmental values like moisture or altitude are kept within specified ranges
Connected devices do not work	Backplane voltages for device not within the specified range	1. Check that all backplane voltages are within their specific ranges 2. Check that power supply is capable to drive the respective loads
	Device defect	Replace device.
	Device not connected to power supply	Connect device to power supply.
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective device.
Devices collide with each other	Devices might have been moved to wrong address location	Configure board / devices correctly (e.g. switch settings.
Low system performance	Caches are disabled	Enable caches
Memory / PMC Module does not work	Module defect	Replace module

Problem	Possible Reason	Solution
	Module not defined for the used board	1. Check if module specification matches with interface specification of board (e.g. clock frequency, voltage) 2. Replace module if specifications do not match
	Module not installed correctly	Check if module fits perfectly in socket.
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective module
Operating system runs unstable	Drivers are missing, faulty or do not match hardware.	1. Check that all used hardware parts have a driver matching the hardware 2. Reinstall hardware drivers
RTB does not work	RTB defect	Replace RTB
	RTB installed on wrong slot position	Install RTB on adjacent slot position of the used board.
	RTB not defined for the used peripheral or system board	Install RTB defined for the used peripheral or system board.

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Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

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