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SPARC/CPU-5CE
Installation Guide

Edition No. 3.0
October 1996

P/N 203510
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1. Introduction

This *Installation Guide* provides instructions for powering up the SPARC CPU-5CE board. The *Installation Guide*, which you have in your hand now, appears both as Section 2 of the *SPARC CPU-5CE Technical Reference Manual* and as a stand-alone *Installation Guide*. This stand-alone Installation Guide is delivered by FORCE COMPUTERS with every board.

1.1 Caution



Read the following safety note before handling the board.

To ensure proper functioning of the product over its usual lifetime, take the following precautions before handling the board.

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime.

- Before installing or uninstalling the board, read this *Installation* section.
- Before installing or uninstalling the board in a VME rack:
  - Check all installed boards for steps that you have to take before turning off the power.
  - Take those steps.
  - Finally turn off the power.
- Before touching integrated circuits, ensure that you are working in an electrostatic free environment.
- Ensure that the board is connected to the VMEbus via both connectors, the P1 and the P2 and that power is available on both.
- When operating the board in areas of strong electro-magnetic radiation, ensure that the board
  - is bolted on the VME rack
  - and shielded by closed housing.

1.2 Location Diagram of the SPARC CPU-5CE Board

A location diagram showing all the components of the CPU-5CE appears on the next page. On the page next to it, there is a location diagram of the CPU-5CE which highlights components that are of particular interest to the user.

1.3 SPARC CPU-5CE Technical Reference Manual Set

Also available from FORCE COMPUTERS is the SPARC CPU-5CE Technical Reference Manual Set. This set includes the *SPARC CPU-5CE Technical Reference Manual* as well as two additional books. *The SPARC CPU-5CE Technical Reference Manual* provides a comprehensive hardware and software guide to your board and is intended for those persons who require complete information. The titles and contents of the two additional books are listed here:

The *Set of Data Sheets for the SPARC CPU-5CE* contains the following data sheets.

NCR SBus I/O Chipset Data Manual	Sun Microsystems S4 Chip Set (Rev.4)
microSPARC-II Data Sheet	AMD Flash EPROM (AM28F020)
SGS-THOMSON MK48T08(B)-10/12/15/20	Intel Flash Memory (28F008SA-L)

The *OPEN BOOT PROM 2.0 MANUAL SET* contains the following three sections.

Open Boot 2.0 Quick Reference	FCODE Programs
Open Boot 2.0 Command Reference	

FIGURE 1. Diagram of the CPU-5CE

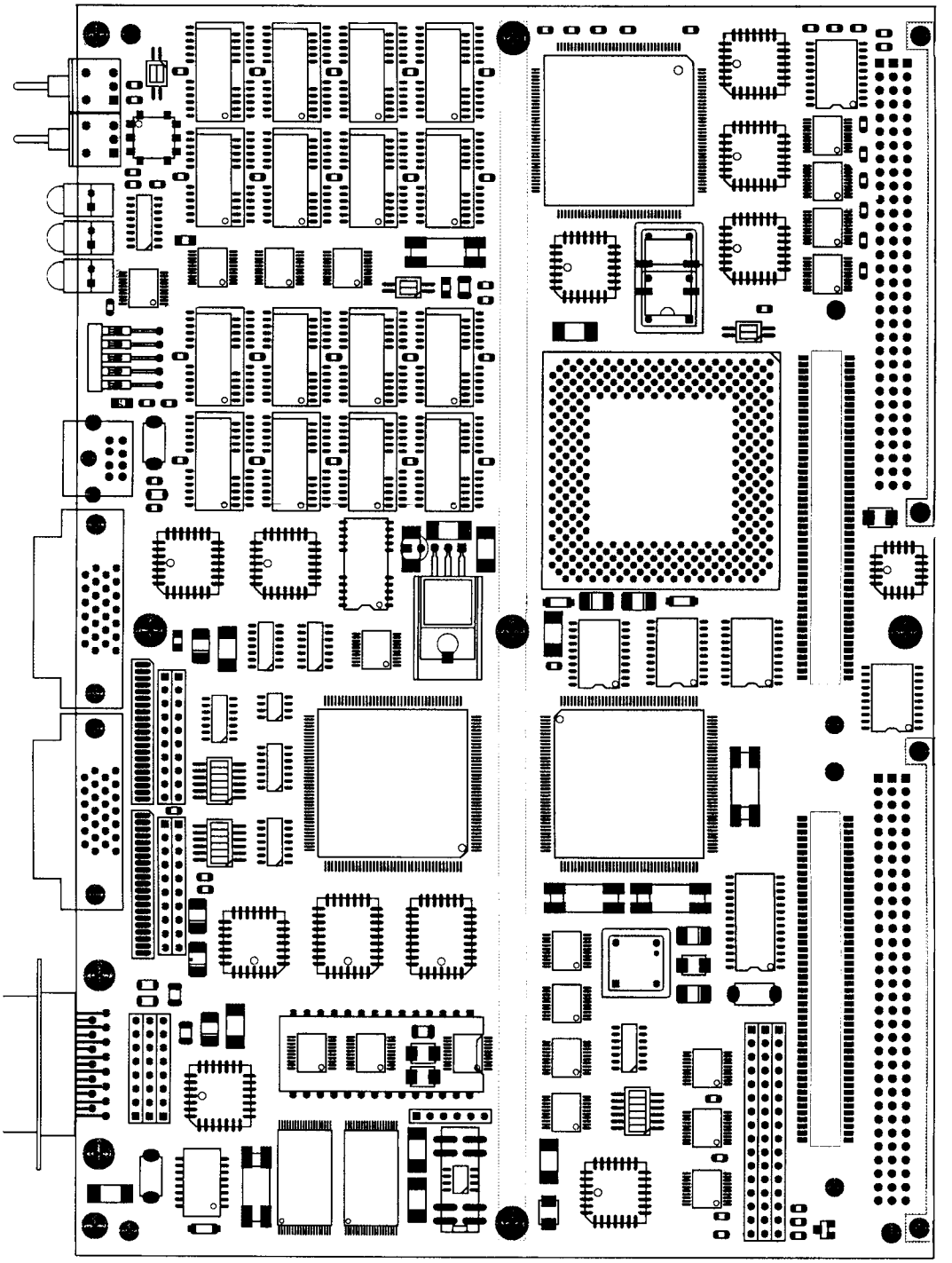
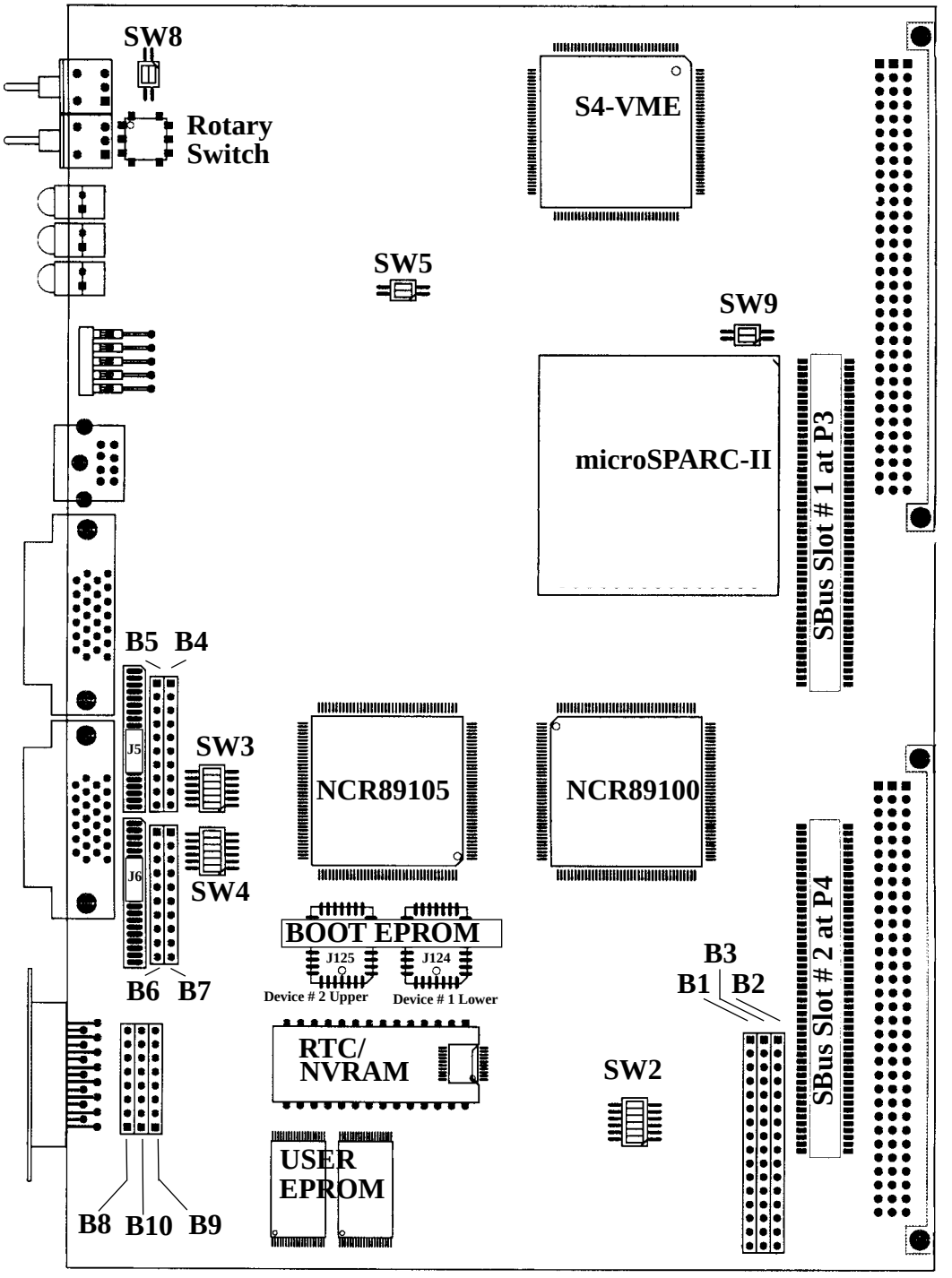


FIGURE 2. Highlighted Diagram of the CPU-5CE



1.4 Before Powering Up

WARNING: Switch off the power before installing the board into a VME rack.

Before powering up, please make sure that the default switch settings are all set according to the table below. For the position of the switches on the board, please see the "Highlighted Diagram of the CPU-5CE" on page 4. Now is an excellent time to examine the switches to confirm that they are correctly set.

1.4.1 Default Switch Settings

Table 1: Default Switch Settings

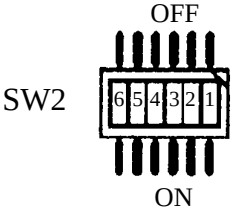
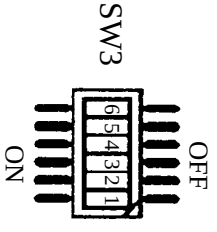
Diagram of Switch	Switches	Default Setting	Function
SWITCH 2			
	SW2-6	ON	**SCSI termination** ON = enable, OFF = disable
	SW2-5	OFF	**Test Switch**, must be OFF
	SW2-4	OFF	**User Flash EPROM write protection** ON = disable, OFF = enable
	SW2-3	OFF	**Boot Flash EPROM write protection** ON = disable, OFF = enable
	SW2-2	ON	**Test Switch**, must be ON
	SW2-1	OFF	**Test Switch**, must be OFF
SWITCH 3 (Controls Serial Channel A)			
	SW3-1	ON	TRXC on Front Panel Connector for RS-232 ON=Available, OFF=Not Available
	SW3-2	OFF	RTS functions as TEN for RS-485 ON=TEN function enabled OFF=TEN function disabled
	SW3-3	OFF	TRXC +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
	SW3-4	ON	RTS on Front Panel Connector for RS-232 or RTS +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
	SW3-5	ON	CTS on Front Panel Connector for RS-232 or CTS +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
	SW3-6	OFF	RTXC +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available

Table 1: Default Switch Settings (cont.)

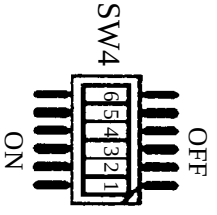
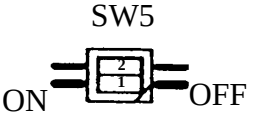
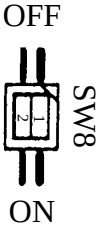
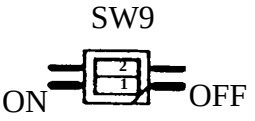
Diagram of Switch	Switches	Default Setting	Function
SWITCH 4 (Controls Serial Channel B)			
	SW4-1	ON	TRXC on Front Panel Connector for RS-232 ON=Available, OFF=Not Available
	SW4-2	OFF	RTS functions as TEN for RS-485 ON=TEN function enabled OFF=TEN function disabled
	SW4-3	OFF	TRXC +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
	SW4-4	ON	RTS on Front Panel Connector for RS-232 or RTS +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
	SW4-5	ON	CTS on Front Panel Connector for RS-232 or CTS +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
	SW4-6	OFF	RTXC +/- on Front Panel Connector for RS-422 ON=Available, OFF=Not Available
SWITCH 5			
	SW5-2	OFF	**Test Switch**, must be OFF
	SW5-1	ON	**VMEbus Slot1 Device** ON = Slot-1 Device, OFF = Not Slot-1 Device
SWITCH 8			
	SW8-2	ON	**Abort Key Control** ON=Abort Key enable, OFF=Abort Key disable
	SW8-1	ON	**Reset Key Control** ON=Reset Key enable, OFF=Reset Key disable

Table 1: Default Switch Settings (cont.)

Diagram of Switch	Switches	Default Setting	Function
SWITCH 9			
	SW9-2 SW9-1	ON ON	**External VMEbus SYSRESET** ON = VMEbus SYSRESET generates on-board RESET OFF = VMEbus SYSRESET does not generate on-board RESET **VMEbus SYSRESET generation** ON = SYSRESET is driven to VMEbus, if board is Slot-1 Device OFF = SYSRESET is not driven to VMEbus

CAUTION: To avoid damaging the serial ports, please consider the following regarding Switch 3 and Switch 4. Do not set the switches (SW3-1 and SW3-2), or (SW3-3 and SW3-4), or (SW3-5 and SW3-6) to ON at the same time and do not set the switches (SW4-1 and SW4-2), or (SW4-3 and SW4-4), or (SW4-5 and SW4-6) to ON at the same time!

1.5 Powering Up

The initial power up can easily be done by connecting a terminal to ttya (serial port A). The advantage of using a terminal is that no frame buffer, monitor, or keyboard is used for initial power up, which facilitates a simple start up.

Please see the chapter “Boot the System” on page 12 for more detailed information on booting the system.

1.5.1 VME Slot-1 Device

The SPARC CPU-5CE can be plugged into any VMEbus slot; however, the default configuration sets the board as a VME slot-1 device, which functions as VME system controller. To configure your CPU-5CE so it is not a VME slot-1 device, the default configuration must be changed so that SW5-1 is OFF.

CAUTION

Before installing the SPARC CPU-5CE in a miniforce chassis, please first disable the VMEbus System Controller function by setting switch SW5-1 to OFF.

1.5.2 VMEbus SYSRESET Switches

When the SPARC CPU-5CE is a VMEbus slot-1 device, it generates the SYSRESET signal to the VMEbus. This can be disabled by setting the switch SW9-1 to OFF.
An external SYSRESET generates an on-board RESET in the default switch setting, i.e., SW9-2 is ON. When SW9-2 is OFF, the external SYSRESET does not generate an on-board RESET.

1.5.3 Serial Ports

By default, both serial ports are configured as RS-232 interfaces. It is also possible to configure both ports as RS-422 or RS-485 interfaces. This optional configuration is achieved with the special FORCE Hybrids FH-003 and FH-005.

The chapter “Default Switch Settings” on page 5 shows the necessary switch settings for RS-232 operation, where SW3 controls serial port A and SW4 controls serial port B. Please check that the switches are set accordingly.

1.5.4 RESET and ABORT Key Enable

To enable the RESET and the ABORT functions on the front panel, set switches SW8-1 (RESET) and SW8-2 (ABORT) to ON.

1.5.5 SCSI Termination

Termination for the SCSI interface is enabled when SW2-6 is ON. This is the default setting.

CAUTION

Before installing the SPARC CPU-5CE in a microforce chassis, please first disable the SCSI termination by setting switch SW2-6 to OFF.

1.5.6 Boot Flash EPROM Write Protection

Both Boot Flash EPROMs are write protected via the switch SW2-3. When SW2-3 is OFF, the devices are write protected.

1.5.7 User Flash EPROM Write Protection

The optional User Flash EPROMs are write protected via SW2-4. When SW2-4 is OFF, the User Flash EPROMs are write protected.

1.5.8 Reserved Switches

SW2-1, SW2-2 , SW2-5 and SW5-2 are reserved for test purposes. SW2-1, SW2-5 and SW5-2 should always be OFF. SW2-2 should always be ON.

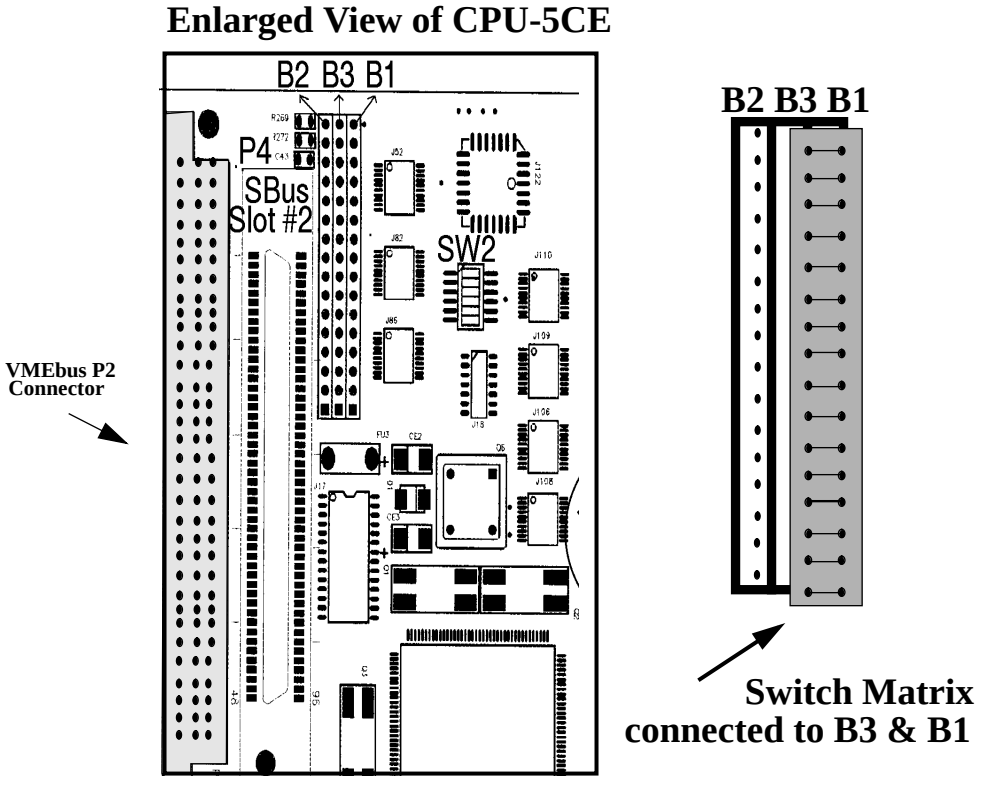
1.5.9 Parallel Port or Floppy Interface via VME P2 Connector

Via a 16-pin configuration switch matrix, it is possible for either the parallel port interface or the floppy interface to be available on the VME P2 connector.

The default setting enables the floppy interface via the VME P2 connector, with the configuration switch matrix plugged into B2 and B3. This means, of course, that by default the parallel port interface is not available via the VMEbus P2 connector.

To enable the parallel port interface via the VME P2 connector, plug the configuration switch matrix in sockets B1 and B3. The following drawing shows this configuration.

FIGURE 3. Parallel Port Interface Via VME P2 Connector



The switch matrix plugs into connectors B1 and B3 and the parallel port is accessible through the VMEbus P2 connector.

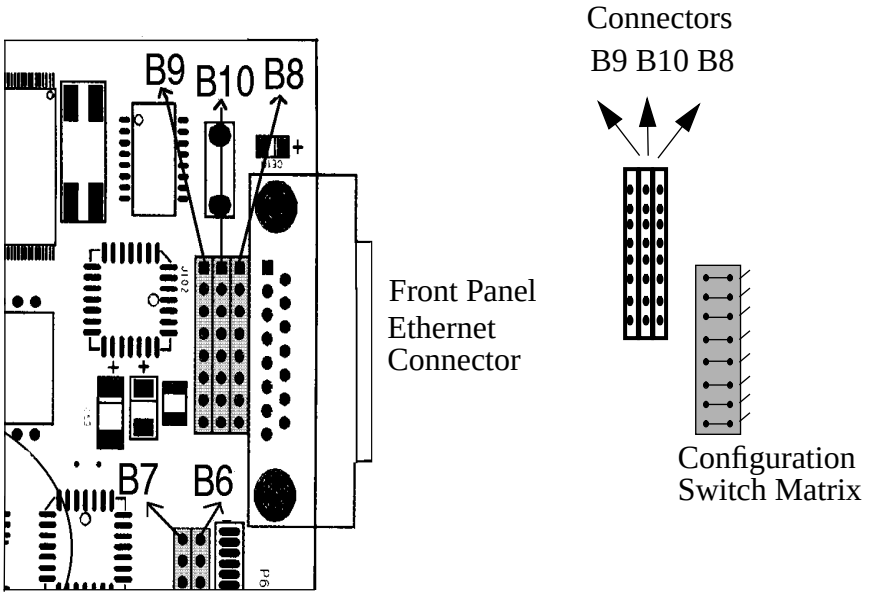
1.5.10 Ethernet via Front Panel or VME P2 Connector

Via an 8-pin configuration switch matrix, it is either possible for the Ethernet interface to be available via the front panel or the VME P2 connector. The default configuration provides the Ethernet through the front panel connector.

In order to have the Ethernet interface accessible via the VME P2 connector, the default configuration must be changed.

Take a moment to examine the diagram to see how one achieves the desired configuration.

FIGURE 4. Ethernet Interface Availability



By default, the Ethernet interface is available through the front panel with the configuration switch matrix plugged into connectors B9 and B10.

To configure the Ethernet interface to be accessible from the VMEbus P2 connector, the configuration switch matrix must be plugged into connectors B8 and B10.

WARNING

When the Ethernet interface is configured via P2, do not connect the Ethernet at the front panel.

1.6 OpenBoot Firmware

This chapter describes the use of OpenBoot firmware. Specifically, you will read how to perform the following tasks.

- Boot the System
- Run Diagnostics
- Display System Information
- Reset the System
- OpenBoot Help

For detailed information concerning OpenBoot, please see the *OPEN BOOT PROM 2.0 MANUAL SET*. This manual is included in the *SPARC CPU-5CE Technical Reference Manual* Set.

1.6.1 Boot the System

The most important function of OpenBoot firmware is booting the system. Booting is the process of loading and executing a stand-alone program such as the operating system. After it is powered on, the system usually boots automatically after it has passed the Power On SelfTest (POST). This occurs without user intervention.

If necessary, you can explicitly initiate the boot process from the OpenBoot command interpreter. Automatic booting uses the default boot device specified in non-volatile RAM (NVRAM); user initiated booting uses either the default boot device or one specified by the user.

To boot the system from the default boot device, type the following command at the Forth Monitor prompt.

```
ok boot
```

or, if you are at the Restricted Monitor Prompt, you have to type the following:

```
> b
```

The boot command has the following format:

boot [device-specifier] [filename] [-ah]

The optional parameters are described as follows.

[device-specifier]	The name (full path or alias) of the boot device. Typical values are cdrom, disk, floppy, net or tape.
[filename]	The name of the program to be booted. *filename* is relative to the root of the selected device. If no filename is specified, the boot command uses the value of *boot-file* NVRAM parameter. The NVRAM parameters used for booting are described in the following chapter.
[-a]	-a prompt interactively for the device and name of the boot file.
[-h]	-h halt after loading the program.

NOTE: These options are specific to the operating system and may differ from system to system.

To explicitly boot from the internal disk, type:

```
ok boot disk
```

or at the Restricted Monitor prompt:

```
> b disk
```

To retrieve a list of all device alias definitions, type *devalias* at the Forth Monitor command prompt. The following table lists some typical device aliases:

Table 2: Device Alias Definitions

Alias	Boot Path	Description
disk	/iommu/sbus/espdma/esp/sd@3,0	Default disk (1st internal) SCSI-ID 3
disk3	/iommu/sbus/espdma/esp/sd@3,0	First internal disk SCSI-ID 3
disk2	/iommu/sbus/espdma/esp/sd@2,0	Additional internal disk SCSI-ID 2
disk1	/iommu/sbus/espdma/esp/sd@1,0	External disk SCSI-ID 1
disk0	/iommu/sbus/espdma/esp/sd@0,0	External disk SCSI-ID 0
tape	/iommu/sbus/espdma/esp/st@4,0	First tape drive SCSI-ID 4
tape0	/iommu/sbus/espdma/esp/st@4,0	First tape drive SCSI-ID 4
tape1	/iommu/sbus/espdma/esp/st@5,0	Second tape drive SCSI-ID 5
cdrom	/iommu/sbus/espdma/esp/sd@6,0:d	CD-ROM partition d, SCSI-ID 6
net	/iommu/sbus/ledma/le	Ethernet
floppy	/obio/SUNW,fdtwo	Floppy drive

1.6.2 NVRAM Boot Parameters

The OpenBoot firmware holds configuration parameters in NVRAM. At the Forth Monitor prompt, type *printenv* to see a list of all available configuration parameters. The OpenBoot command *setenv* may be used to set these parameters.

setenv [configuration parameter] [value]

This information refers only to those configuration parameters which are involved in the boot process. The following table lists these parameters.

Table 3: Setting Configuration Parameters

Parameter	Default Value	Description
auto-boot?	true	If true, boot automatically after power on or reset
boot-device	disk	Device from which to boot
boot-file	empty string	File to boot
diag-switch?	false	If true, run in diagnostic mode
diag-device	net	Device from which to boot in diagnostic mode
diag-file	empty string	File to boot in diagnostic mode

When booting an operating system or another stand-alone program, and neither a boot device nor a filename is supplied, the boot command of the Forth Monitor takes the omitted values form the NVRAM configuration parameters. If the parameter diag-switch? is false, boot-device and boot-file are used. Otherwise, the OpenBoot firmware uses diag-device and diag-file for booting.

For a detailed description of all NVRAM configuration parameters, please refer to the *OPEN BOOT PROM 2.0 MANUAL SET.*

1.6.3 Diagnostics

At power on or after reset, the OpenBoot firmware executes POST. If the NVRAM configuration parameter diag-switch? is true for each test, a message is displayed on a terminal connected to the first serial port. In case the system is not working correctly, error messages indicating the problem are displayed. After POST, the OpenBoot firmware boots an operating system or enters the Forth Monitor if the NVRAM configuration parameter auto-boot? is false.

The Forth Monitor includes several diagnostic routines. These on-board tests let you check devices such as network controller, SCSI devices, floppy disk system, memory, clock and installed SBus cards. User installed devices can be tested if their firmware includes a selftest routine.

The table below lists several diagnostic routines.

Table 4: Diagnostic Routines

Command	Description
probe-scsi	Identify devices connected to the on-board SCSI bus
probe-scsi-all [*device-path*]	Perform probe-scsi on all SCSI buses installed in the system below the specified device tree node. (If *device-path* is omitted, the root node is used.)
test *device-specifier*	Execute the specified device's selftest method. device-specifier may be a device path name or a device alias. For example: test net - test network connection test /memory - test number of megabytes specified in the selftest-#megs NVRAM parameter or test all of memory if diag-switch? is true
test-all [*device-specifier*]	Test all devices (that have a built-in selftest method) below the specified device tree node. (If *device-path* is omitted, the root node is used.)
watch-clock	Monitor the clock function
watch-net	Monitor network connection

To check the on-board SCSI bus for connected devices, type:

```
ok probe-scsi
Target 3
        Unit 0 Disk MICROP 1684-07MB1036511AS0C1684
ok
```

To test all the SCSI buses installed in the system, type

```
ok probe-scsi-all
/iommu@0,10000000/sbus@0,10001000/esp@2,100000
Target 6
        Unit 0 Disk Removable Read Only Device SONY CD-ROM CDU-8012 3.1a

/iommu@0,10000000/sbus@0,10001000/espdma@4,8400000/esp@4,8800000
Target 3
        Unit 0 Disk MICROP 1684-07MB1036511AS0C1684

ok
```

The actual response depends on the devices on the SCSI buses.

To test a single installed device, type:

```
ok test device-specifier
```

This executes the device method name selftest of the specified device node.
device-specifier may be a device path name or a device alias as described in Table 2, “Device Alias Definitions,” on page 14.The response depends on the selftest of the device node.

To test a group of installed devices, type:

```
ok test-all
```

All devices below the root node of the device tree are tested. The response depends on the devices that have a selftest routine. If a device specifier option is supplied at the command line, all devices below the specified device tree node are tested.

When you use the memory testing routine, the system tests the number of megabytes of memory specified in the NVRAM configuration parameter selftest-#megs. If the NVRAM configuration parameter diag-switch? is true, all memory is tested.

```
ok test /memory
testing 32 megs of memory at addr 0 27
ok
```

The command **test-memory** is equivalent to **test /memory**. In the example above, the first number (0) is the base address of the memory bank to be tested, the second number (27) is the number of megabytes remaining. If the CPU board is working correctly, the memory is erased and tested and you will receive the **ok** prompt. If the PROM or the on-board memory is not

working, you receive one of a number of possible error messages indicating the problem.

To test the clock function, type

```
ok watch-clock
Watching the 'seconds' register of the real time clock chip.
It should be 'ticking' once a second.
Type any key to stop.
22
ok
```

The system responds by incrementing a number once a second. Press any key to stop the test.

To monitor the network connection, type:

```
ok watch-net
Using AUI Ethernet Interface
Lance register test -- succeeded.
Internal loopback test -- succeeded.
External loopback test -- succeeded.
Looking for Ethernet packets.
'.' is a good packet. 'X' is a bad packet.
Type any key to stop.
.....X.....X.....
ok
```

The system monitors the network traffic, displaying "." each time it receives a valid packet and displaying "X" each time it receives a packet with an error that can be detected by the network hardware interface.

1.6.4 Display System Information

The Forth Monitor provides several commands to display system information. These commands let you display the system banner, the Ethernet address for the Ethernet controller, the contents of the ID PROM, and the version number of the OpenBoot firmware.

The ID PROM contains information specific to each individual machine, including the serial number, date of manufacture, and assigned Ethernet address.

The following table lists these commands.

Table 5: Commands to Display System Information

Command	Description
banner	Display system banner.
show-sbus	Display list of installed and probed SBus devices.
.enet-addr	Display current Ethernet address.
.idprom	Display ID PROM contents, formatted.
.traps	Display a list of SPARC trap types.
.version	Display version and date of the Boot PROM.
show-devs	Display a list of all device tree nodes.
devalias	Display a list of all device aliases.

1.6.5 Reset the System

If your system needs to be reset, you either press the reset button on the front panel or, if you are in the Forth Monitor, type **reset** on the command line.

```
ok reset
```

The system immediately begins executing the Power On SelfTest (POST) and initialization procedures. Once the POST completes, the system either boots automatically or enters the Forth Monitor, just as it would have done after a power on cycle.

1.6.6 OpenBoot Help

The Forth Monitor contains an on-line help. To get this, type:

```
ok help
Enter ‘help command-name’ or ‘help category-name’ for more help
(Use ONLY the first word of a category description)
Examples: help select -or- help line
Main categories are:
File download and boot
Resume execution
Diag (diagnostic routines)
Power on reset
>-prompt
Floppy eject
Select I/O devices
Ethernet
System and boot configuration parameters
Line editor
Tools (memory,numbers,new commands,loops)
Assembly debugging (breakpoints,registers,disassembly,symbolic)
Sync (synchronize disk data)
Nvramrc (making new commands permanent)
ok
```

A list of all available help categories is displayed. These categories may also contain subcategories. To get help for special forth words or subcategories just type help [name]. An example is shown on the next page.

An example of how to get help for special forth words or subcategories.

```
ok help tools
Category: Tools (memory,numbers,new commands,loops)
Sub-categories are:
Memory access
Arithmetic
Radix (number base conversions)
Numeric output
Defining new commands
Repeated loops
ok
ok help memory
Category: Memory access
dump ( addr length -- ) display memory at addr for length bytes
fill ( addr length byte -- ) fill memory starting at addr with byte
move ( src dest length -- ) copy length bytes from src to dest address
map? ( vaddr -- ) show memory map information for the virtual address
l? ( addr -- ) display the 32-bit number from location addr
w? ( addr -- ) display the 16-bit number from location addr
c? ( addr -- ) display the 8-bit number from location addr
l@ ( addr -- n ) place on the stack the 32-bit data at location addr
w@ ( addr -- n ) place on the stack the 16-bit data at location addr
c@ ( addr -- n ) place on the stack the 8-bit data at location addr
l! ( n addr -- ) store the 32-bit value n at location addr
w! ( n addr -- ) store the 16-bit value n at location addr
c! ( n addr -- ) store the 8-bit value n at location addr
ok
```

The on-line help shows you the forth word, the parameter stack before and after execution of the forth word (before -- after), and a short description.

The on-line help of the Forth Monitor is located in the boot PROM, so there is not an online help for all forth words.

1.6.7 How to Install an OpenBoot ROM

This section describes how to install the OpenBoot ROM delivered to you by FORCE COMPUPTERS. This information is useful in the case that OpenBoot ROM is exchanged or upgraded.

For the location of the OpenBoot ROMs on the board, see “Highlighted Diagram of the CPU-5CE” on page 4.

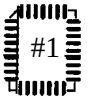
1.6.7.1 Caution



Avoid touching integrated circuits except in an electrostatic free environment. Electrostatic discharge can damage circuits or shorten their lifetime. Turn off the power before handling the board or its components. Turn off the power before installing the board in a VMEbus rack.

1.6.7.2 Replacing the ROMs

1. Remove the existing OpenBoot ROM from socket J124 and store it in a safe place.



2 Insert the new OpenBoot ROM labeled ROM #1 (2.15.2) in socket J124. Note the position of the diagonally cut edge on the ROM and place the new ROM on the board accordingly.

3. Remove the existing OpenBoot ROM from socket J125 and store it in a safe place.

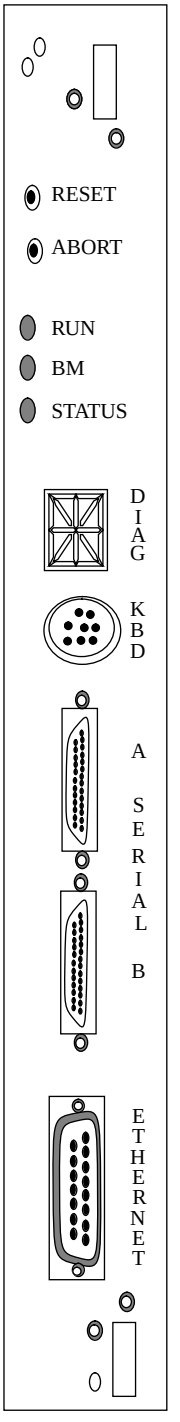


4. Insert the new OpenBoot ROM labeled ROM #2 (2.15.2) in socket J125. Note the position of the diagonally cut edge on the ROM and place the new ROM on the board accordingly.

5. Install the SPARC CPU-5CE in the VMEbus rack. You are now ready to power up.

1.7 Front Panel

FIGURE 5. Diagram of the Front Panel



1.7.1 Features of the Front Panel

- Reset and Abort key
- Status LEDs on the front panel
- Hex display on the front panel

These features are described in detail in Section 3 of the *SPARC CPU-5CE Technical Reference Manual*.

Table 6: Features of the Front Panel

Device	Function	Name
Switch	Reset	RESET
Switch	Abort	ABORT
LED	RUN/RESET	RUN
LED	VMEbus Bus Master	BM
LED	Status	STATUS
HEX Display	Diagnostic	DIAG
Mini DIN Connector	Keyboard/Mouse	KBD
Serial Connector	Serial Interface	SERIAL A
Serial Connector	Serial Interface	SERIAL B
D-Sub Connector	Ethernet Interface	ETHERNET

1.8 SPARC CPU-5CE Connectors

The connectors on the SPARC CPU-5CE are listed in the following table.

Table 7: SPARC CPU-5CE Connectors

Function	Location	Type	Manufacturer Part Number
Ethernet	Front Panel	15-pin D-Sub	AMP 747845-4
Serial Port A	Front Panel	26-pin Fine Pitch	AMP 749831-2
Serial Port B	Front Panel	26-pin Fine Pitch	AMP 749831-2
Keyboard/Mouse	Front Panel	8-pin Mini DIN	AMP 749232-1
SBus Slot1	P3	96-pin SMD	FUJITSU FCN-234J096-G/V
SBus Slot2	P4	96-pin SMD	FUJITSU FCN-234J096-G/V
VMEbus P1	P1	96-pin VGA	Various
VMEbus P2	P2	96-pin VGA	Various

The following pages show the pinouts of the connectors.

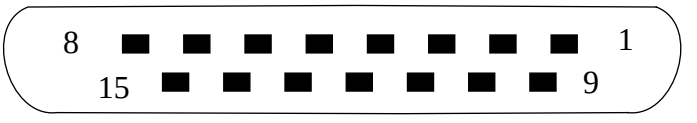
1.8.1 Ethernet Connector Pinout

The following table is a pinout of the Ethernet connector. The figure below shows the Ethernet connector and pin numbers.

Table 8: Ethernet the Connector Pinout

Pin	Function
1	GND
2	Collision+
3	Transmit Data+
4	GND
5	Receive Data+
6	GND
7	N.C.
8	GND
9	Collision-
10	Transmit Data-
11	GND
12	Receive Data-
13	+12VDC
14	GND
15	N.C.

FIGURE 6. Pinout of theEthernet Cable Connector



1.8.2 Serial Ports A and B Connector Pinout

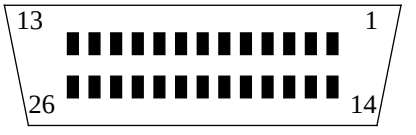
The two serial I/O ports are available on the front panel via two 26-pin shielded connectors which are compatible to the CPU-2CE and to the CPU-3CE.

Both channels are available via the VMEbus P2 connector, each with four signals (RXD, TXD, RTS, CTS). Each of the two serial I/O ports are independent full-duplex channels. The table below shows the pinout of serial ports A and B. The table is valid for both serial I/O connectors A and B.

Table 9: Serial Ports A and B Connector Pinout for RS-232

Pin	Transmitted Signals	Pin	Received Signals
2	TxD-Transmit Data	3	RxD-Receive Data
4	RTS-Request To Send	5	CTS-Clear To Send
7	GND	6	SYNC
20	DTR-Data Terminal Ready	8	DCD-Data Carrier Detect
24	TRXC-DTE Terminal Clock	15	TRXC-DCE Terminal Clock
		17	RTXC-DCE Terminal Clock

FIGURE 7. Serial Ports A and B Connector Pinout



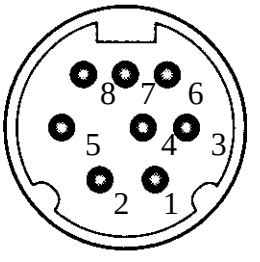
1.8.3 Keyboard/Mouse Connector Pinout

The keyboard and mouse port is available on the front panel via a Mini DIN connector.

Table 10: Keyboard/Mouse Connector Pinout

Pin	Function
1	GND
2	GND
3	+5VDC
4	Mouse In
5	Keyboard Out
6	Keyboard In
7	Mouse Out
8	+5VDC

FIGURE 8. Keyboard/Mouse Connector



1.8.4 VME P2 Connector Pinout

Table 11: VME P2 Connector Pinout

ROW A	Signal	ROW B	Signal	ROW C	Signal for Floppy Interface [1]	Signal for Parallel Port Interface [1]
1	SCSI Data 0	1	+5VDC	1	FPY DENSEL	CENTR DS
2	SCSI Data 1	2	GND	2	FPY DENSENS	CENTR Data 0
3	SCSI Data 2	3	RESERVED	3	N.C.	CENTR Data 1
4	SCSI Data 3	4	VME A24	4	FPY INDEX	CENTR Data 2
5	SCSI Data 4	5	VME A25	5	FPY DRVSEL	CENTR Data 3
6	SCSI Data 5	6	VME A26	6	N.C.	CENTR Data 4
7	SCSI Data 6	7	VME A27	7	N.C.	CENTR Data 5
8	SCSI Data 7	8	VME A28	8	FPY MOTEN	CENTR Data 6
9	SCSI DP	9	VME A29	9	FPY DIR	CENTR Data 7
10	GND	10	VME A30	10	FPY STEP	CENTR ACK
11	GND	11	VME A31	11	FPY WRDATA	CENTR BSY
12	GND	12	GND	12	FPY WRGATE	CENTR PE
13	TERMPWR	13	+5VDC	13	FPY TRACK0	CENTR AF
14	GND	14	VME D16	14	FPY WRPROT	CENTR INIT
15	GND	15	VME D17	15	FPY RDDATA	CENTR ERR
16	SCSI ATN	16	VME D18	16	FPY HEADSEL	CENTR SLCT IN
17	GND	17	VME D19	17	FPY DISKCHG	CENTR SLCT
18	SCSI BSY	18	VME D20	18	FPY EJECT	RESERVED
19	SCSI ACK	19	VME D21	19	+12VDC [2]	+12VDC [2]
20	SCSI RST	20	VME D22	20	GND	GND
21	SCSI MSG	21	VME D23	21	GND	GND
22	SCSI SEL	22	GND	22	ETH REC+ [2]	ETH REC+ [2]
23	SCSI CD	23	VME D24	23	ETH REC- [2]	ETH REC- [2]
24	SCSI REQ	24	VME D25	24	ETH TRA+ [2]	ETH TRA+ [2]

Table 11: VME P2 Connector Pinout (cont.)

ROW A	Signal	ROW B	Signal	ROW C	Signal for Floppy Interface [1]	Signal for Parallel Port Interface [1]
25	SCSI IO	25	VME D26	25	ETH TRA- [2]	ETH TRA- [2]
26	RESERVED	26	VME D27	26	ETH COL+ [2]	ETH COL+ [2]
27	RESERVED	27	VME D28	27	ETH COL- [2]	ETH COL- [2]
28	RESERVED	28	VME D29	28	GND	GND
29	TxD Port A	29	VME D30	29	TxD Port B	TxD Port B
30	RxD Port A	30	VME D31	30	RxD Port B	RxD Port B
31	RTS Port A	31	GND	31	RTS Port B	RTS Port B
32	CTS Port A	32	+5VDC	32	CTS Port B	CTS Port B

Notes:

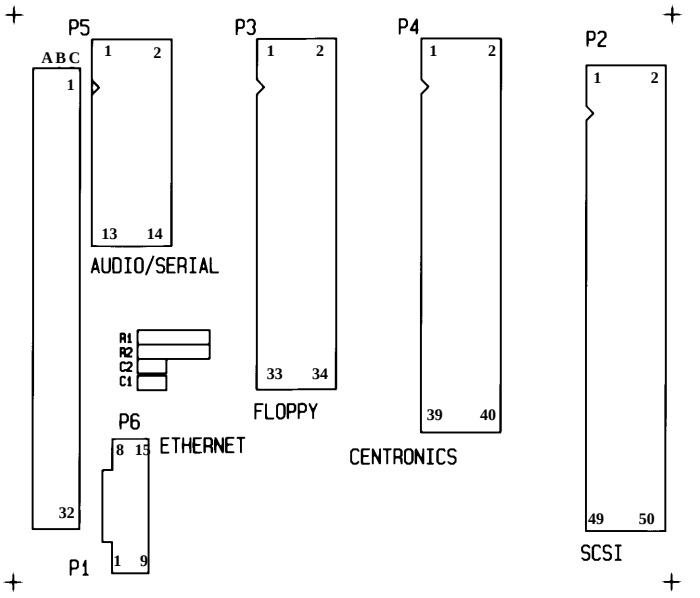
1) For further information, see “Parallel Port Interface Via VME P2 Connector” on page 10.

2) For further information, please see “Ethernet Interface Availability” on page 11.

1.8.5 The IOBP-10 Connectors

The IOBP-10 is an I/O back panel on VMEbus P2 with flat cable connectors for SCSI, serial I/O, Centronics/floppy interface, and a micro D-Sub connector for an Ethernet interface. This back panel can be plugged into the VMEbus P2 connector. The diagram below shows all the connectors. This IOBP-10 back panel is especially designed for the SPARC CPU-5CE. Do not use any other I/O back panels on the SPARC CPU-5CE, for example, the IOBP-1.

FIGURE 9. The IOBP-10



The pinouts of the connectors (P1) ... (P6) are shown in the following tables.

CAUTION

This IOBP-10 back panel is especially designed for the SPARC CPU-5CE. Do not use any other I/O back panels on the SPARC CPU-5CE, for example, the IOBP-1.

Table 12: IOBP-10 P1 Pinout

ROW A	Signal	ROW B	Signal	ROW C	Signal for Floppy Interface [1]	Signal for Parallel Port Interface [1]
1	SCSI Data 0	1	N.C.	1	FPY DENSEL	CENTR DS
2	SCSI Data 1	2	GND	2	FPY DENSENS	CENTR Data 0
3	SCSI Data 2	3	N.C..	3	N.C.	CENTR Data 1
4	SCSI Data 3	4	N.C.	4	FPY INDEX	CENTR Data 2
5	SCSI Data 4	5	N.C.	5	FPY DRVSEL	CENTR Data 3
6	SCSI Data 5	6	N.C.	6	N.C.	CENTR Data 4
7	SCSI Data 6	7	N.C.	7	N.C.	CENTR Data 5
8	SCSI Data 7	8	N.C.	8	FPY MOTEN	CENTR Data 6
9	SCSI DP	9	N.C.	9	FPY DIR	CENTR Data 7
10	GND	10	N.C.	10	FPY STEP	CENTR ACK
11	GND	11	N.C.	11	FPY WRDATA	CENTR BSY
12	GND	12	GND	12	FPY WRGATE	CENTR PE
13	TERMPWR	13	N.C.	13	FPY TRACK0	CENTR AF
14	GND	14	N.C.	14	FPY WRPROT	CENTR INIT
15	GND	15	N.C.	15	FPY RDDATA	CENTR ERR
16	SCSI ATN	16	N.C.	16	FPY HEADSEL	CENTR SLCT IN
17	GND	17	N.C.	17	FPY DISKCHG	CENTR SLCT
18	SCSI BSY	18	N.C.	18	FPY EJECT	RESERVED
19	SCSI ACK	19	N.C.	19	+12VDC [2]	+12VDC [2]
20	SCSI RST	20	N.C.	20	GND	GND
21	SCSI MSG	21	N.C.	21	GND	GND
22	SCSI SEL	22	GND	22	ETH REC+ [2]	ETH REC+ [2]
23	SCSI CD	23	N.C.	23	ETH REC- [2]	ETH REC- [2]
24	SCSI REQ	24	N.C.	24	ETH TRA+ [2]	ETH TRA+ [2]
25	SCSI IO	25	N.C.	25	ETH TRA- [2]	ETH TRA- [2]
26	RESERVED	26	N.C.	26	ETH COL+ [2]	ETH COL+ [2]

Table 12: IOBP-10 P1 Pinout (cont.)

ROW A	Signal	ROW B	Signal	ROW C	Signal for Floppy Interface [1]	Signal for Parallel Port Interface [1]
27	RESERVED	27	N.C.	27	ETH COL- [2]	ETH COL- [2]
28	RESERVED	28	N.C.	28	GND	GND
29	TxD Port A	29	N.C.	29	TxD Port B	TxD Port B
30	RxD Port A	30	N.C.	30	RxD Port B	RxD Port B
31	RTS Port A	31	GND	31	RTS Port B	RTS Port B
32	CTS Port A	32	N.C.	32	CTS Port B	CTS Port B

Notes:

1) For further information, see “Parallel Port Interface Via VME P2 Connector” on page 10.

2) For further information, please see “Ethernet Interface Availability” on page 11.

Table 13: IOBP-10 P2 Pinout (SCSI)

Pin No.	Signal	Pin No.	Signal
1	GND	2	SCSI Data 0
3	GND	4	SCSI Data 1
5	GND	6	SCSI Data 2
7	GND	8	SCSI Data 3
9	GND	10	SCSI Data 4
11	GND	12	SCSI Data 5
13	GND	14	SCSI Data 6
15	GND	16	SCSI Data 7
17	GND	18	SCSI DP
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	GND	26	TERMPWR
27	N.C.	28	GND
29	GND	30	GND
31	GND	32	SCSI ATN
33	GND	34	GND
35	GND	36	SCSI BSY
37	GND	38	SCSI ACK
39	GND	40	SCSI RST
41	GND	42	SCSI MSG
43	GND	44	SCSI SEL
45	GND	46	SCSI CD
47	GND	48	SCSI REQ
49	GND	50	SCSI IO

Table 14: IOBP-10 P3 Pinout (Floppy)

Pin No.	Signal	Pin No.	Signal
1	FPY EJECT	2	FPY DENSEL
3	GND	4	FPY DENSENS
5	GND	6	N.C.
7	GND	8	FPY INDEX
9	GND	10	FPY DRVSEL
11	GND	12	N.C.
13	GND	14	N.C.
15	GND	16	FPY MOTEN
17	GND	18	FPY DIR
19	GND	20	FPY STEP
21	GND	22	FPY WRDATA
23	GND	24	FPY WRGATE
25	GND	26	FPY TRACK0
27	N.C.	28	FPY WRPROT
29	GND	30	FPY RDDATA
31	GND	32	FPY HEADSEL
33	GND	34	FPY DISKCHG

Table 15: IOBP-10 P4 Pinout (Centronics)

Pin No.	Signal	Pin No.	Signal
1	CENTR DS	2	GND
3	CENTR Data 0	4	GND
5	CENTR Data 1	6	GND
7	CENTR Data 2	8	GND
9	CENTR Data 3	10	GND
11	CENTR Data 4	12	GND
13	CENTR Data 5	14	GND
15	CENTR Data 6	16	GND
17	CENTR Data 7	18	GND
19	CENTR ACK	20	GND
21	CENTR BSY	22	GND
23	CENTR PE	24	GND
25	CENTR SLCT	26	CENTR INIT
27	CENTR AF	28	CENTR ERR
29	N.C.	30	GND
31	GND	32	N.C.
33	N.C.	34	N.C.
35	N.C.	36	CENTR SLCT IN
37	N.C.	38	N.C.
39	N.C.	40	N.C.

Table 16: IOBP-10 P5 Pinout (Serial)

Pin No.	Signal	Pin No.	Signal
1	GND	2	RESERVED
3	RESERVED	4	RESERVED
5	TxD Port B	6	TxD Port A
7	RxD Port B	8	RxD Port A
9	RTS Port B	10	RTS Port A
11	CTS Port B	12	CTS Port A
13	GND	14	GND

Table 17: IOBP-10 Pinout (Ethernet)

Pin	Function
1	GND
2	Collision+
3	Transmit Data+
4	GND
5	Receive Data+
6	GND
7	N.C.
8	N.C.
9	Collision-
10	Transmit Data-
11	GND
12	Receive Data-
13	+12VDC
14	GND
15	N.C.

1.9 How to Determine the Ethernet Address and Host ID

In order to see the Ethernet address and host ID, type the following command at the prompt:

```
ok banner
```

The information below explains how the SPARC/CPU-5CE Ethernet address and the host ID are determined.

FIGURE 10. The 48-bit (6-byte) Ethernet address

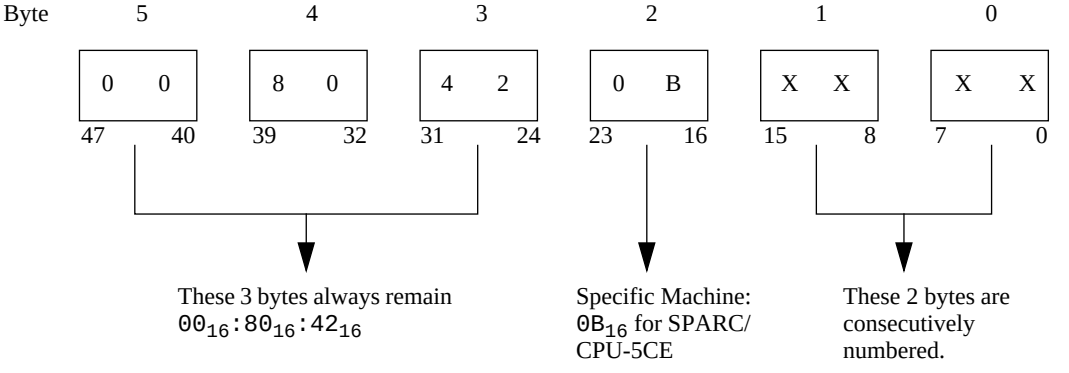
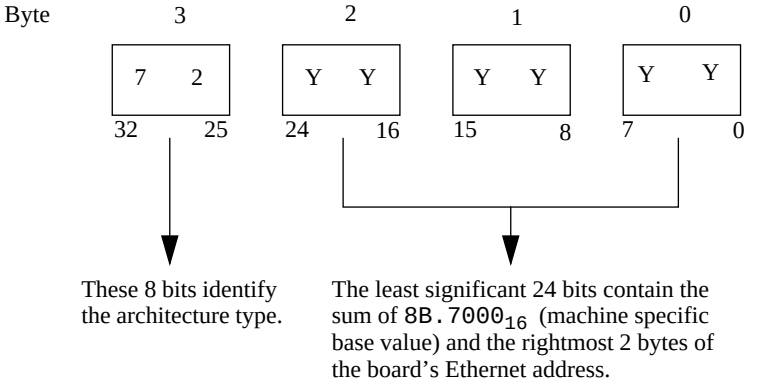


FIGURE 11. The 32-bit (4-byte) host ID



1.10 Publication History of the Manual

Below is a description of the publication history of this *SPARC CPU-5CE Installation Guide.*

Table 18: History of Manual

Revision No.	Description	Date
1	First Print	July 1994
2	Editorial Changes	July 1995
3	BusNet and How to Install the OpenBoot ROM sections have been added. The Ethernet and Host ID chapter has been updated.	October 1996

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