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SYS68K/IBC-20 Rev.2

Hardware User's Manual

Edition No. 2
April 1997

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INTRODUCTION

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1. GENERAL DESCRIPTION

The IBC-20 is a high performance basic controller board which uses the Motorola MC68020 32-bit microprocessor.

The board design provides System Control functions for the VMEbus environment. It uses all features of the powerful FORCE COMPUTERS Gate Array FGA-002A.

A total of up to 4 Mbytes of static RAM is provided for the Shared Main Memory which is also accessible from VME.

The IBC-20 can be upgraded with the Floating Point Unit MC68882. The IBC-20 can also be upgraded with up to 8 Mbyte System Memory with FLASH EPROM devices by installing the IBC MOD-1 module on the board. The IBC MOD-1 is described in detail in Section 8 of this manual.

Additional features include a serial I/O debugging port, three 16-bit counters/timers, 128 Kbytes of nonvolatile read/write RAM by Flash Memory, a Real Time Clock/Calendar and 32 Kbytes of local SRAM, with battery backup on board.

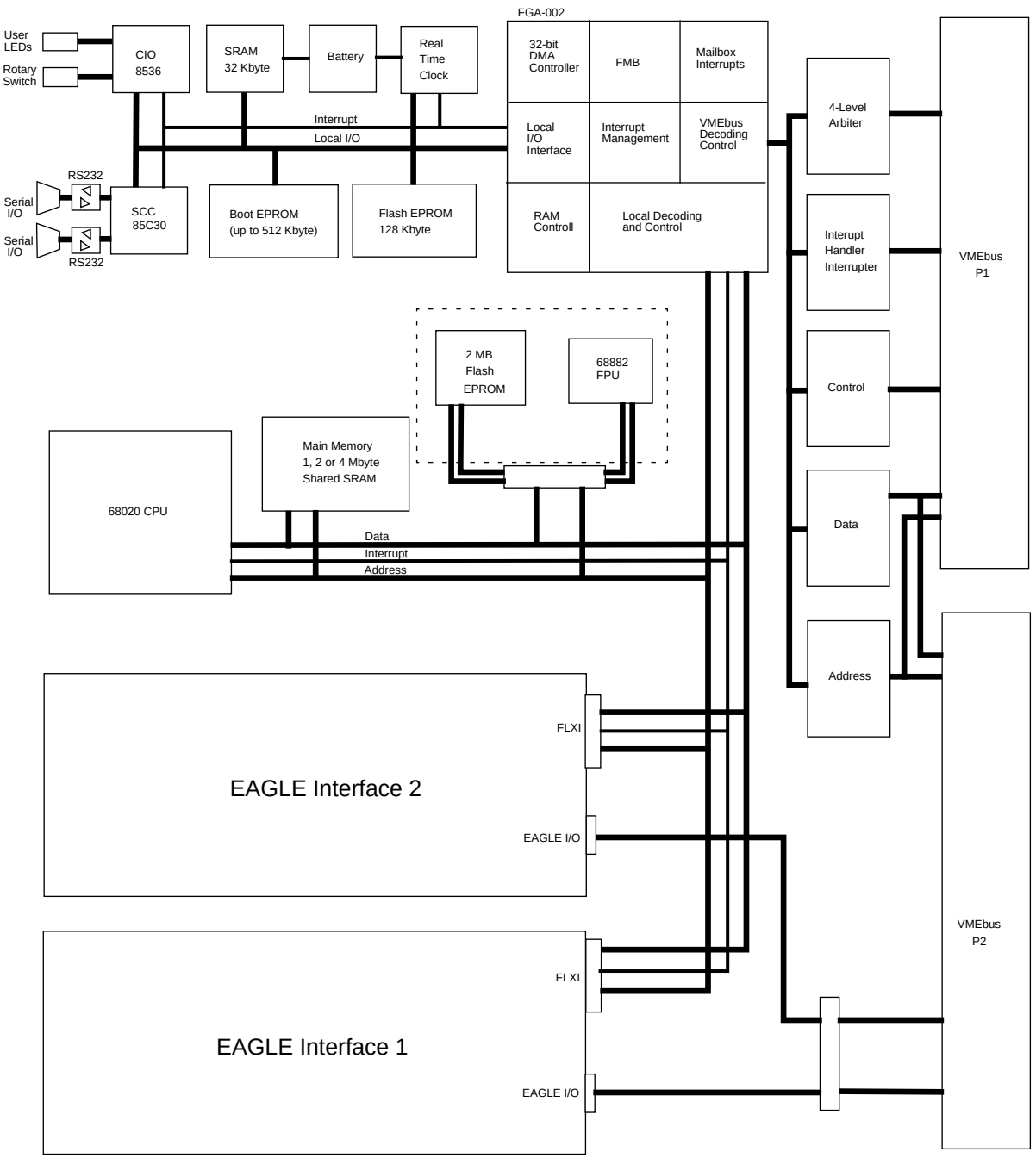
The powerful real-time monitor VMEPROM with file manager and Real Time Kernel (PDOS compatible) is included.

The IBC-20 board is compatible to the following standards:

IEEE 1014-87
IEC 821
IEC 297

The block diagram is presented on the next page in Figure 1-1.

FIGURE 1-1: Block Diagram of the IBC-20



2. FEATURES OF THE IBC-20

- **MC68020 Microprocessor**

  The board provides the MC68020 microprocessor running at 25 MHz clock frequency for onboard intelligence and performance.

- **32-bit DMA Controller**

  An independent 32-bit DMA Controller provides high speed data transfer between the VMEbus and the Main RAM. The DMA controller is contained in the FGA-002A. The DMA Controller transfers data entirely independent from the local processor and is able to transfer data across the VMEbus without affecting the performance of the processor. To increase the data throughput, the DMA controller uses a 32-byte FIFO for internal data storage. The read and write operations are executed in bursts of eight transfer cycles.

- **MC68882 Floating Point Coprocessor Upgrade**

  The IBC-20 board may be upgraded with MC68882 Floating Point Coprocessor by installing the module IBC MOD-1 on the baseboard.

- **FLXi/EAGLE Module Interfaces**

  Two EAGLE Module interfaces on the base board are provided for the installation of one or two EAGLE modules. The interfaces are built according to the EAGLE Module specification of FORCE COMPUTERS, which allows installing any module that conforms to this standard. The EAGLE module interfaces provide the nonmultiplexed, asynchronous FLXibus, supporting 32-bit data and address bus architecture with dynamic bus sizing and master/slave capability. The FLXibus allows the EAGLE module to access all resources on the base board and the VMEbus. In addition, the 64 VMEbus user I/O pins are connectable to the I/O Connector of the EAGLE Module Interface 1, or may be shared by the two EAGLE modules, one using the pins of row A and the other using the pins of row C.

- **4 Mbyte Shared Main Memory**

  The Main RAM is built with low power static memory devices which provide up to 4 Mbyte capacity. Backup capability is given through the VMEbus +5V STBY line. The Main memory is accessible by the DMA controller, by any FLXibus master and also from the VMEbus.

- **8 Mbyte System Flash-EPROM Upgrade**

  Up to 8 Mbyte System Memory (FLASH EPROM devices) is available by using the module IBC MOD-1.

- **32 Kbyte Local SRAM**

  32 Kbyte of battery backed up memory is provided by the local SRAM. The battery backs up the SRAM during power-off for at least one year. Backup capability is also given through the +5V STDBY line of the VMEbus.

- **128 Kbyte FLASH EPROM**

  The local FLASH EPROM provides 128 Kbyte of nonvolatile read/write memory without the need of battery backup for saving data.

- **512 Kbyte Boot EPROM Socket**

  A single EPROM socket is provided for 128Kx8 to 512Kx8 JEDEC compatible memory devices. The base board EPROM contains the boot firmware and the real-time monitor VMEPROM.

- **Two RS-232 Serial I/O Ports**

  Two serial I/O ports are available on the front panel providing RS-232C compatible interface signals at the 9-pin micro D-Sub connectors. This enables direct connection to standard terminals and allows the channels to be used as console and debugging ports.

- **RTC 72423 Real Time Clock**

  The Real Time Clock (RTC 72423) provides battery backed up time-of-day, date counter with auto leap year, 12 and 24 hour format and interrupt capability.

- **4 Timers**

  A total of four independent timers are available on the IBC-20 board. The FGA-002A gate array contains an 8-bit timer with programmable source clocks. Three 16-bit timers are located in the 8536 Counter/Parallel-I/O device (CIO), two of them internally linkable to a 32-bit timer unit. Each timer can be used for interrupt generation to the microprocessor. The FGA-002A timer is also usable as system watchdog timer which is able to assert the SYSFAIL* signal of the VMEbus.

- **VMEbus Master/Slave Interface**

  The VMEbus interface of the IBC-20 allows the board to act as master and slave for data transfers on the VMEbus. The 32-bit addressing capability together with support of extended, standard, and short I/O address modifier codes allows the user to interface to a wide range of VMEbus products. Unaligned transfers and Read-Modify-Write cycles are fully supported.

- **VMEbus Interrupter and Interrupt Handler**

  The IBC-20 provides an Interrupter function which enables the board to send interrupts to the VMEbus on each of the seven interrupt lines. Interrupt requests from the VMEbus are handled by the FGA-002A device, which is able to convert the VME interrupt level to any interrupt level for the local processor.

- **4-Level VMEbus Arbiter**

  A four-level bus arbiter allows arbitration of the data transfer bus in the round robin, the prioritized and the prioritized round robin algorithm. Several bus release functions are implemented for multiprocessor applications.

- **VMEbus System Control Functions**

  The board features Slot-1 system control functions such as SYSCLOCK driver, IACK Daisy Chain driver and 4-Level bus arbiter with Bus clear generation. The VMEbus system control signal lines ACFAIL* and SYSFAIL* are supported and may generate interrupts to the local processor. SYSRESET is driven to and received from the VMEbus.

- **2 Message Broadcast Channels (FMB)**

  Two independent 8-bit wide Message Broadcast Channels provide a fast and effective mechanism to communicate with and synchronize up to 20 CPU boards in VMEbus system in only one write cycle.

- **8 Mailboxes**

  Multiprocessing support is provided by the eight Mailboxes. The Mailboxes are local, VME addressable and generate an interrupt to the local processor on a programmable level.

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3. SPECIFICATIONS OF THE IBC-20

CPU type		68020
CPU clock frequency		25.0 MHz
Coprocessor	IBC-20/x-2	68882
DMA controller (FGA-002)		32-bit
Shared SRAM capacity	IBC-20/1 IBC-20/2 IBC-20/4	1 Mbyte 2 Mbyte 4 Mbyte
SRAM capacity with on-board battery backup		32 Kbyte
FLASH EPROM capacity	IBC-20/x IBC-20/x-2 IBC-20/x-2N	128 Kbyte 2 Mbyte 2 Mbyte
No. of EPROM Sockets Maximum capacity		1 512 Kbyte
Serial I/O interfaces (85C30)		2 (RS232C)
16-bit timer 8-bit timer		3 1
Real Time Clock with on-board battery backup		72423
VMEbus interface	A32, A24,A16:D8,D16,D32,UAT,RMW A32,A24:D8,D16,D32,RMW	Master Slave
Four-level arbiter SYSCLK driver		yes yes
EAGLE module interfaces with FLXibus (Master/Slave) EAGLE module interfaces with access to VMEbus P2		2 of 2 2 of 2
Mailbox interrupts		8

Specifications of the IBC-20 are continued on the next page.

Specifications of the IBC-20 continued

FORCE Message Broadcast FMB-FIFO 0 (standard priority) FMB-FIFO 1 (high priority)	8 byte 8 byte
VMEbus and local interrupt handler VMEbus interrupter Software programmable IRQ level and vector IACK Daisy Chain Driver	1 to 7 1 to 7 yes yes
RESET/ABORT Switch	yes
VMEPROM based firmware installed on all versions	yes
Power requirements + 5V max (without EAGLE modules) +12V max -12V max	3.0A 100 mA 70 mA
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing in %) Board Dimensions No. of slots used, with optional EAGLE modules installed	0°C to +50°C -40°C to +85°C 5 to 95 234 x 160 mm / 9.2 x 6.3 in. 1

4. ORDERING INFORMATION

SYS68K/IBC-20/1	25.0 MHz MC68020 based intelligent I/O controller board with DMA, 1 Mbyte shared SRAM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/2	25.0 MHz MC68020 based intelligent I/O controller board with DMA, 2 Mbyte shared SRAM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/4	25.0 MHz MC68020 based intelligent I/O controller board with DMA, 4 Mbyte shared SRAM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/2-2	25.0 MHz MC68020, MC68882 based intelligent I/O controller board with DMA, 2 Mbyte shared SRAM, 2 Mbyte FLASH-EPROM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/2-2N	25.0 MHz MC68020 based intelligent I/O controller board with DMA, 2 Mbyte shared SRAM, 2 Mbyte FLASH-EPROM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/4-2	25.0 MHz MC68020, MC68882 based intelligent I/O controller board with DMA, 4 Mbyte shared SRAM, 2 Mbyte FLASH-EPROM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/4-2N	25.0 MHz MC68020 based intelligent I/O controller board with DMA, 4 Mbyte shared SRAM, 2 Mbyte FLASH-EPROM, 2 serial I/O ports, 2 EAGLE module interfaces (FLXibus), VMEPROM. Documentation included.
SYS68K/IBC-20/UM	User's Manual set for the SYS68K/IBC-20 product including hardware, firmware and FGA-002 manuals.
SYS68K/CABLE MICRO-9/1	Adapter cable 9-pin micro D-sub male connector to 9-pin D-sub female connector, length 2 meters.
EAGLE MODULE SPEC/UM	EAGLE Module Specification including FLXibus and software interface description.

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5. HISTORY OF MANUAL REVISIONS

Revision No.	Description	Date of Last Change
0	This manual describes the IBC-20 revision 2 printed circuit board.	FEB/05/1993
1	Editorial changes have been made throughout this manul	SEP/06/1993
2	Editorial changes have been made.	APRIL/1997

INSTALLATION

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W A R N I N G

TO AVOID MALFUNCTIONS AND COMPONENT DAMAGE, PLEASE READ THE COMPLETE INSTALLATION PROCEDURE BEFORE THE BOARD IS INSTALLED IN A VMEBUS ENVIRONMENT.

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1. GENERAL

The IBC-20 comes ready to be installed in a VMEbus environment. The battery is installed on the board with an isolation strip on top of it. Please remove the isolation strip on the battery to enable it.

The front panel accessible rotary switch is set to $F to boot the VMEPROM monitor after powerup. The monitor sets all necessary board functions enabling a standard terminal connected to the micro-D-Sub front panel connector to communicate with VMEPROM. Set the terminal for 9600 baud, 8 bits per character, no parity, one stop bit.

By default the IBC-20 acts as VME system controller and can become VMEbus master. The board should be installed in slot 1 of the VMEbus system and no other board should be generating SYSCLK or functioning as Arbiter. To disable the system controller function of the board, switch SW5-8 must be set to the OFF position.

1.1 The MODE Switch

The Mode switch which is accessible through the front panel, configures the startup of the VMEPROM or a user program. By default, the switch is set to $F.

The various setup functions determined by the Mode switch are described in detail in the *"Firmware User's Manual"*.

1.2 The Toggle Switches

The IBC-20 board contains two toggle switches mounted on the top of the front panel. The switches are:

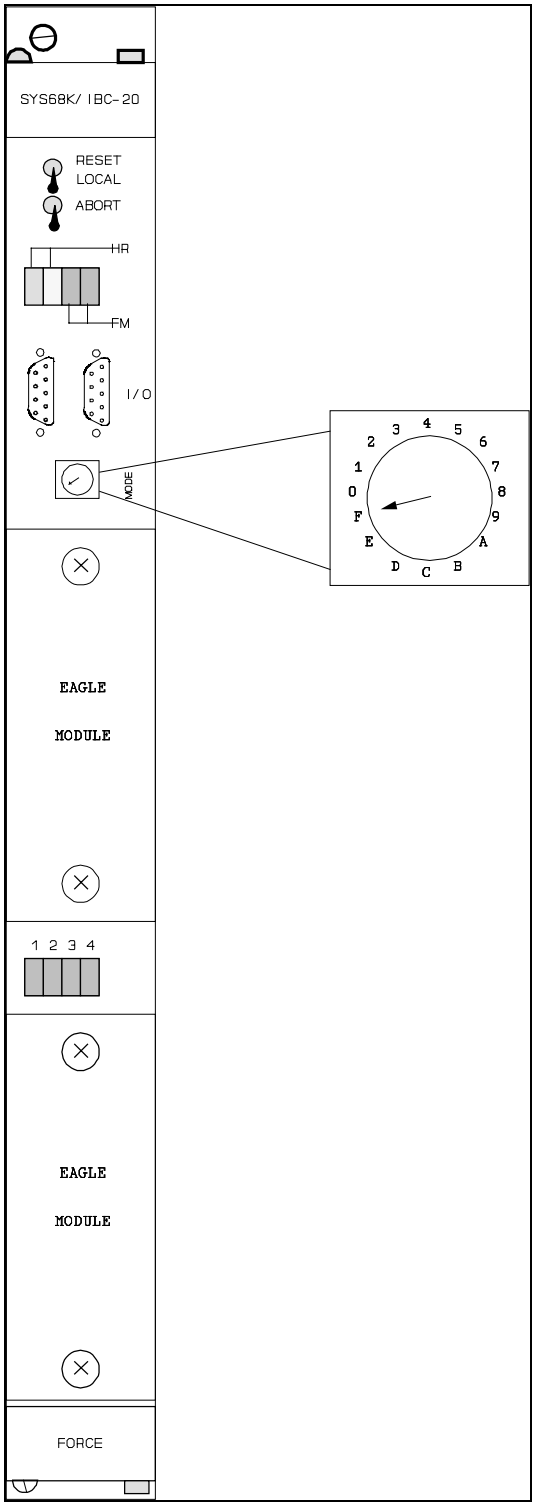
- RESET/LOCAL Switch
- ABORT Switch

Both switches are double function switches which have their normal position in the middle. The upper position of the switches activates the function momentarily, while in the down position the function is enabled continuously.

Set the switches to the middle position for proper operation.

In order to detect mechanical damage to the switches during transport, please toggle each switch before installing the board in the rack.

Figure 1-1: Front Panel of the Board



1.3 Connection of the Terminal

A terminal can be connected to either of the two 9-pin Micro D-Sub connectors on the front panel.

An adapter cable from 9-pin Micro D-Sub to 9-pin D-Sub adapter cable is optionally available.

The following communication setup is used for interfacing the terminal. Please configure the terminal to this setup.

No Parity
8 Bits per character
1 Stop Bit
9600 Baud
Asynchronous Protocol

The hardware interface is RS-232C compatible. The following signals are supported on both 9-pin Micro D-Sub connectors on the front panel:

Signal	Input	Output	Required	9-Pin Micro D-Sub Connector	Description	9-Pin D-Sub of the Adapter Cable
DCD	X			1	Data Carrier Detect	1
RXD	X		X	2	Receive Data	2
TXD		X	X	3	Transmit Data	3
DTR		X		4	Data Terminal Ready	4
GND				5	Signal GND	5
DSR	X			6	Data Set Ready	6
RTS		X	X	7	Request to Send	7
CTS	X		X	8	Clear to Send	8
GND			X	9	Signal GND	9

CAUTION

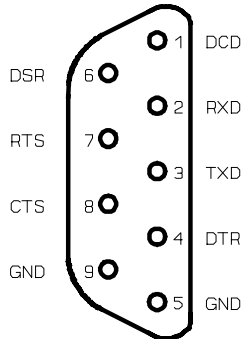
1) The terminal used must not drive a signal line which is marked to be an output of the board.

2) All signals marked as "Required" must be supported from the terminal to enable the transmission.

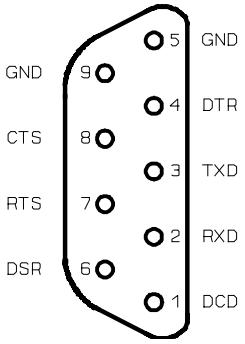
3) If the terminal is configured to the listed setup, please connect the 9-pin Micro D-Sub connector to the terminal with a cable which supports all of the required signals.

Figure 1-2: Pinout of the Micro D-Sub and D-Sub Connector

A) Micro D-Sub Male Connector Soldered on the Board



B) Micro D-Sub and D-Sub Female Connectors on the Adapter/Terminal Cable



1.4 The Default Hardware Setup

The IBC-20 is configured to be used immediately. This results in a default hardware setup which may conflict with other boards installed in the rack.

The following VMEbus signals are driven/received by the board:

Signal	Driven	Received
SYSCLK	X	
BR3*	X	
BR[3..0]*		X
BG[3..0]OUT*	X	
ACFAIL*		X
SYSFAIL*		X
SYSRESET*	X	X

CAUTION

1) The on-board 4-level arbiter is enabled and responds to every Bus Request.

2) The board is configured as a VMEbus system controller (Slot 1 functions enabled).

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2. INSTALLATION IN THE RACK

The board can immediately be mounted into a VME rack at slot 1.

CAUTION

1) Switch off power before installing the board to avoid electrical damage to the components.

2) The board contains a special ejector (the handles). The board must be plugged in, and the screws on the front panel tightened up to guarantee proper installation.

3) Unplug every other VMEbus board to avoid conflicts.

2.1 Power ON

Power the VMEbus rack when the board is correctly installed, the switches are in the correct positions, and the terminal is correctly configured and under power.

Initially, the red "H"-LED (HALT/RESET) will light up until the green "R"-LED (RUN) ist turned on. Now the VMEPROM banner should appear on the screen.

The terminal is now at the user's discretion. At this point, it is advised to make a few carriage returns, to obtain the question mark (?_) prompt.

2.2 Correct Operation

To test the correct operation of the board, the following command should be typed in:

? SELFTEST<cr>

It is a matter of a few seconds until all tests are completed. Once all tests are completed, the following messages will appear on the screen:

VMEPROM Hardware Selftest

I/O test . . . . . .passed

Memory test . . . . .passed

Clock test . . . . . .passed

Any errors will be reported as they occur.

If an error message is displayed, please refer to *Firmware User's Manual* containing the command description "*SELFTEST*".

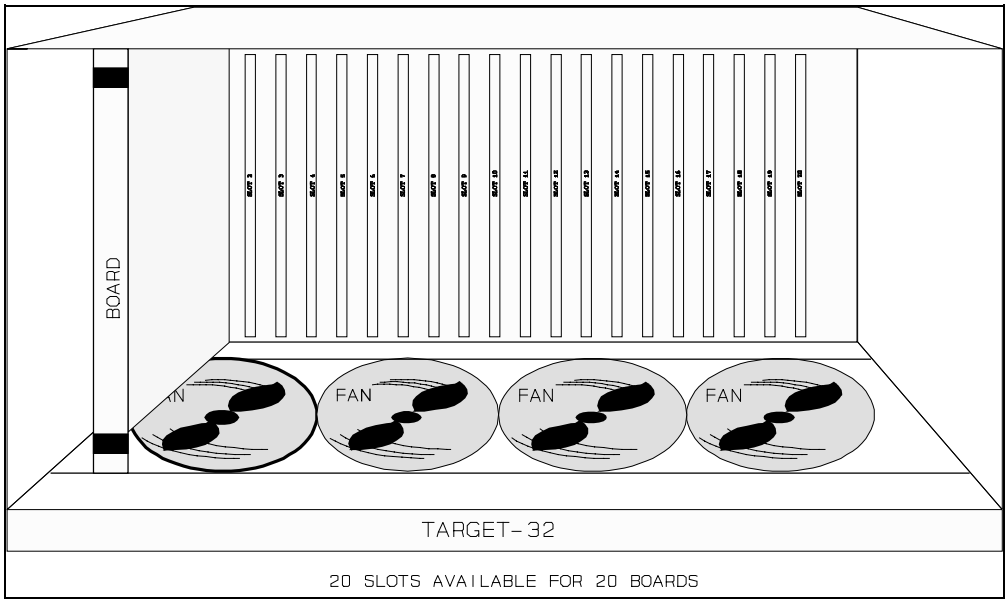
3. ENVIRONMENTAL REQUIREMENTS

This board was specified and tested for reliable operation under certain environmental conditions. Based on our performance tests, this board is capable of operating within the temperature range of 0°C to 50°C when used inside of a FORCE TARGET-32 chassis. The following chart details the calculated rate of forced air cooling.

Rate of Forced Air Cooling

Air Cooling per Board	Total Air Cooling - Target-32
5.5 CFM* = 0.0026 cubic meter/sec	131 CFM = 0.062 cubic meter/sec
275 LFM** = 1.4 meter/sec	275 LFM = 1.4 meter/sec
* CFM = Cubic Feet per Minute ** LFM = Linear Feet per Minute	

The TARGET-32 chassis performs forced air cooling using four axial fans. The amount of airflow needed for cooling and normal operation is reflected by certain factors such as ambient temperature, number and location of boards in the system, and outside heat sources. Sufficient air cooling is normally obtained when 5.5 CFM and 275 LFM is circulating around each board at an ambient temperature between 0°C and 50°C. Allowable storage temperatures may range between -40°C and 85°C. The rate of relative humidity (non-condensing) should not be less than **5**%, and should not exceed **95**%. The following illustration is a pictorial view of the fan placement in the chassis.



HARDWARE USER'S MANUAL

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I. GENERAL DESCRIPTION

The IBC-20 is an 68020 based intelligent basic controller board for the VMEbus, providing the FLXibus (FORCE Local eXpansion interface) for local I/O and memory expansion capability. The FLXibus is available at two slots which allow the installation of up to two EAGLE modules. The 32-bit wide FLXibus supports master as well as slave operation and enables intelligent I/O subsystems which are built on an EAGLE module to communicate with the base board at high data transfer rates.

The IBC-20 board uses the features of the FORCE COMPUTERS Gate Array FGA-002A, providing a high performance 32-bit DMA Controller, two independent Message Broadcast Channels (FMB), eight Mailboxes, an 8-bit watchdog timer, Interrupt Management and support for local control logic.

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II. DEFAULT CONFIGURATION OF THE IBC-20

1. The Switches of the IBC-20 board

It is easy to configure the IBC-20 since there are only two slide switches to set for the required board functions. Descriptions of these two slide switches, SW5 and SW6, follow here. The switch functions of SW5 are printed on the solder side of the printed circuit board near switch SW5.

Slide switch SW5 selects various system functions. Slide switch SW6 enables the secondary battery (NiCd Accumulator) to backup the SRAM and the RTC. By default, both switches of SW6 are set to the "ON" position.

The rotary switch (also designated MODE switch) is accessible through the front panel. There is also a second on-board rotary switch SW4. Firmware reads these two switches and selects the startup conditions of VMEPROM or a user program. For detailed information, please see the *"IBC-20 Firmware User's Manual"*. By default, both switches are set to $F.

Located on the front panel are the toggle switches RESET/LOCAL and ABORT. These switches remain idle when set to their middle position.

Figure 3, on page 2-6, shows the location diagram of slide switches SW5 and SW6.

1.1 The Slide Switch SW5

The following table describes the functions which are controlled by the slide switch SW5.

Table 1: Slide Switch SW5

SWITCH	FUNCTION-CONTROL
SW5-1	Selects whether the Local Flash EPROM on the IBC-20 base board can be written to be erased/reprogrammed
SW5-2	Selects whether the board drives the SYSRESET* signal to the VMEbus
SW5-3	Selects whether the board receives the SYSRESET* signal from the VMEbus
SW5-4	Sets the power-fail reset voltage to 4.85V/4.20V. (The board will be reset as long as the +5V supply voltage is lower than the selected voltage).
SW5-5	Selects whether the System Flash EPROM on the IBC MOD-1 module can be written to be erased/re-programmed. (The System Flash-EPROM is only available with the IBC MOD-1 module)
SW5-6 SW5-7	Select the VMEbus request level
SW5-8	Enables/disables the SLOT 1 functions (VMEbus System controller functions) of the board. If the SLOT 1 function is enabled (Board is System Controller), the 4-level-Arbiter will be enabled, the SYSCLOCK* line and the BCLR* line will be driven.

Figure 1: Default Settings for Slide Switch SW5

The following figure shows default setting of the SW5 switches with the selected board function.

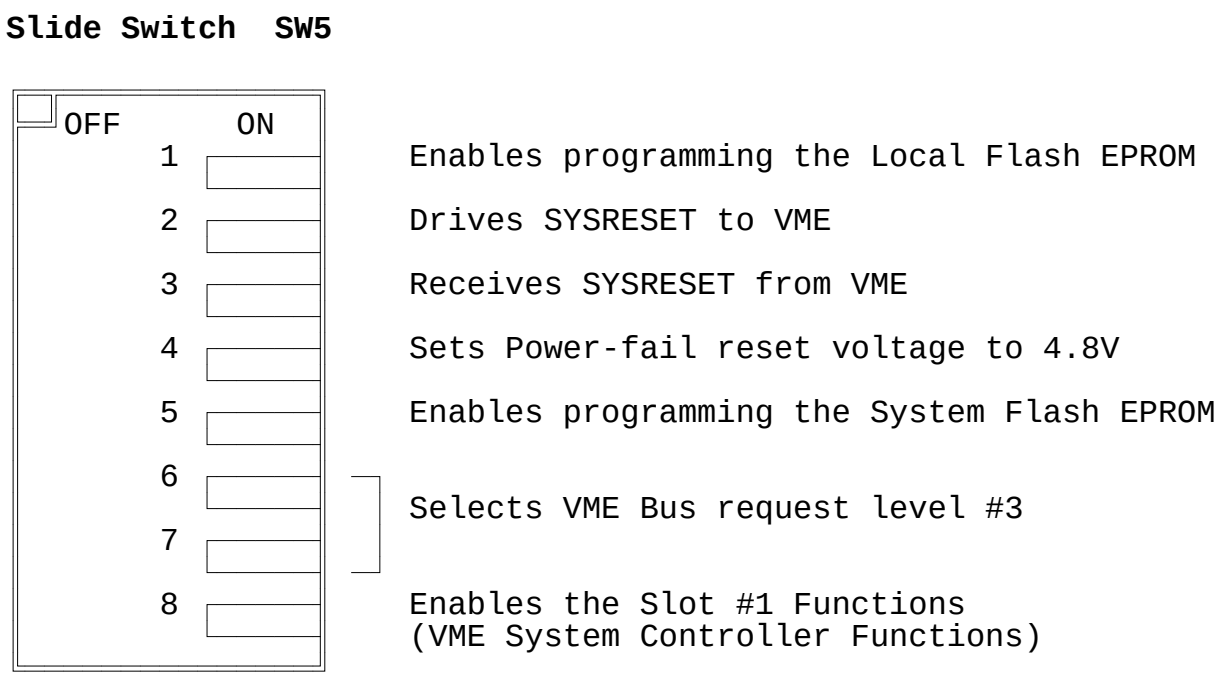


Figure 3, on page 2-6, shows the location diagram of slide switches SW5 and SW6.

Table 2: Functions of Slide Switch SW5

Switch	Name	Selections
SW5-1	IBCFLASH	ON Local Flash EPROM is writable OFF Local Flash EPROM write protected
SW5-2	VMERESOT	ON SYSRESET driven OFF SYSRESET not driven
SW5-3	VMERESIN	ON SYSRESET received OFF SYSRESET not received
SW5-4	MIN4.85V	ON Power-fail reset voltage 4.8V OFF Power-fail reset voltage 4.2V
SW5-5	MODFLASH	ON Module Flash EPROM programmable OFF Module Flash EPROM write protected
SW5-6 SW5-7	BRSEL1 BRSEL0	**BR0 BR1 BR2 BR3** OFF OFF ON ON OFF ON OFF ON
SW5-8	SLOT 1	ON Slot #1 function enabled OFF Slot #1 function disabled

1.2 The Slide Switch SW6

The switches SW6-1 and SW6-2 connect the chargeable secondary battery with the battery backup logic for the local SRAM and the RTC. When the switches are set "ON", the Real Time Clock and the local SRAM will be backed up by the secondary battery. This saves the SRAM and RTC during replacement of the primary battery (Lithium Battery CR2032). In order to guarantee the charging of the secondary battery during run time of the board, the switches have to be set to "ON". If the STDBY-line of the VMEbus supplies power to the board, both switches must be set to the "OFF" position. Otherwise, damage to the chargeable secondary battery may occur.

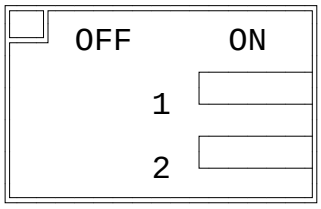
Switches SW6-1 and SW6-2 are functionally considered one switch. Figure 3, on page 2-6, shows the location diagram of slide switches SW5 and SW6.

Table 3: Functions of Slide Switch SW6

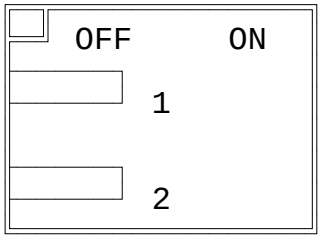
Switch SW6	Selections
SW6-1 and SW6-2	ON/ON Secondary Battery enabled
SW6-1 and SW6-2	OFF/OFF Secondary Battery disabled

Figure 2: Default Setting for Slide Switch SW6

Slide Switch SW6

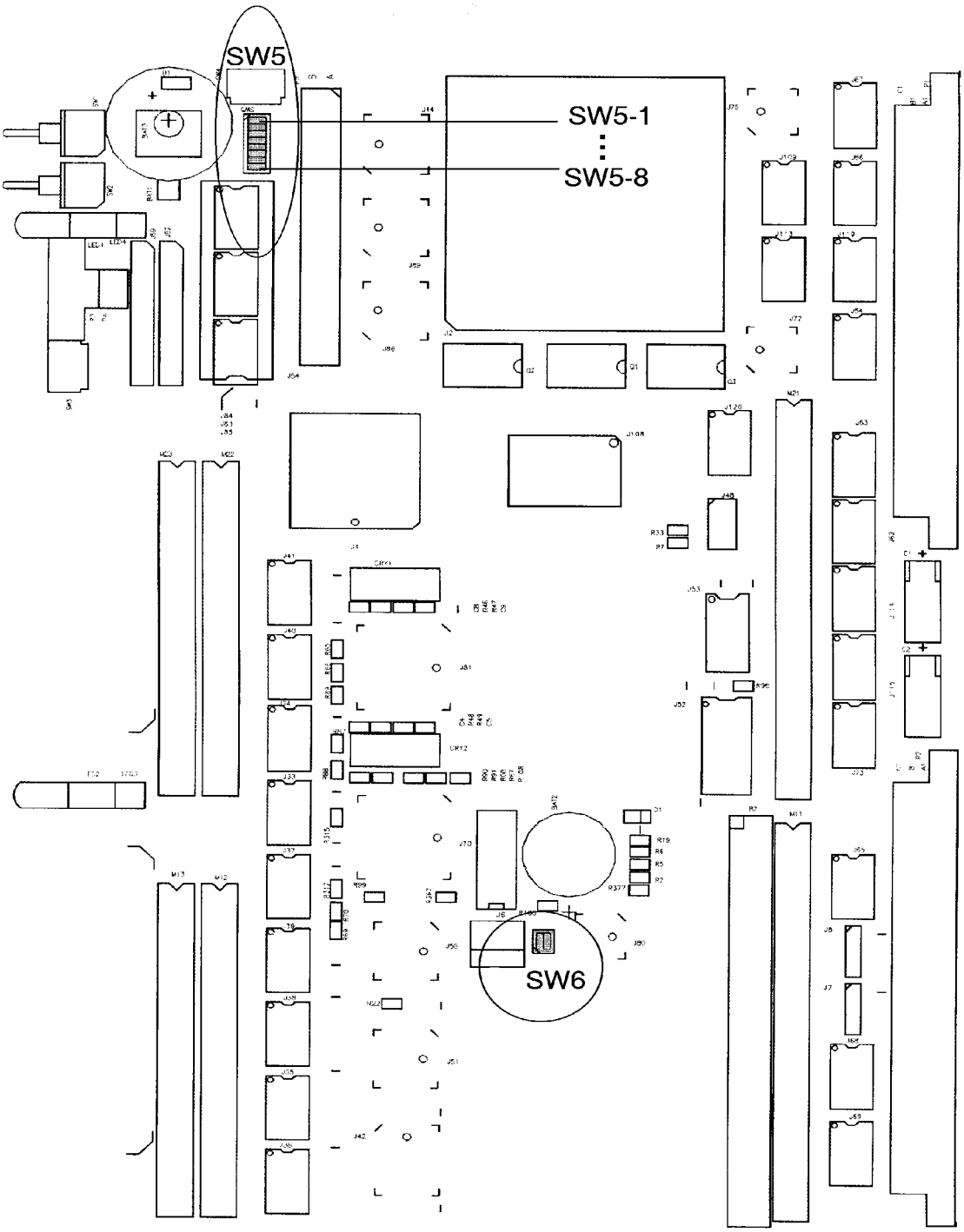


Connects the secondary battery to the battery backup logic. (DEFAULT)



Disconnects the secondary battery from the battery backup circuitry. Switch SW6 must be OFF if the STDBY line of the VMEbus supplies stand-by power.

Figure 3: Location Diagram of Slide Switches SW5 and SW6



III. ADDRESS MAP OF THE IBC-20

The 68020 processor of the IBC-20 board addresses four gigabytes by its 32-bit address bus. This address space is decoded by the FGA-002A Gate Array. Table 5, which appears on the next page, shows the Address Map of the decoded areas.

The address range of the Main memory is software selectable and will be programmed by the onboard firmware depending on the assembled memory capacity. Other addresses are hard decoded by FGA-002A. One area is provided to address devices on EAGLE Modules via the FLXibus interface.

The following table shows the base addresses of the local I/O devices.

Table 4: Base Addresses of the Local I/O Devices

Base Address	Device
$FF802000	SCC Z85C30 Serial Comm. Controller
$FF800C00	CIO Z8536 Counter-Timer I/O Unit
$FF803E00	LCA XC3042 VME Arbiter/Interrupter
$FF803000	RTC 72423 Real Time Clock

Table 5: The Address Map

Address Range		Access to
From	To	
00000000 00000000 00000000 00000000	0007FFFF 000FFFFF 001FFFFF 003FFFFF	Main Memory (512 Kbyte) or Main Memory (1 Mbyte) or Main Memory (2 Mbyte) or Main Memory (4 Mbyte)
00080000 00100000 00200000 00400000	F9FFFFFF F9FFFFFF F9FFFFFF F9FFFFFF	VMEbus (512 Kbyte Main Memory) VMEbus (1 Mbyte Main Memory) VMEbus (2 Mbyte Main Memory) VMEbus (4 Mbyte Main Memory) A32: D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (FMB) (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus A24: D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus A16: D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus A24: D16, D8
FCFF0000	FCFFFFFF	VMEbus A16: D16, D8
FD000000	FEFFFFFF	EAGLE Module Devices via FLXibus
FF000000	FF7FFFFF	System EPROM (optional with Expansion Module)
FF800000	FFBFFFFF	Local I/O Devices
FFC00000	FFC7FFFF	Local SRAM
FFC80000	FFCFFFFF	Local FLASH EPROM
FFD00000	FFDFFFFF	FGA-002A Registers
FFE00000	FFEFFFFF	BOOT EPROM
FFF00000	FFFFFFFF	Reserved

IV. HARDWARE DESCRIPTION

1. THE MICROPROCESSOR MC68020

The IBC-20 board is equipped with the MC68020 processor running at 25 MHz. The chip is housed in a 132-pin plastic quad flat pack (PQFP). The processor features 32-bit wide internal and external data paths. A 32-bit address bus allows to address a total of 4 gigabyte physical memory. The 68020 incorporates a 256 byte onchip cache memory used to store the instruction prefetches from the main memory. The instruction cache offers 64 long word entries with a tag field for each cache entry. The 68020 is object code compatible with earlier 68000 microprocessors. Its instruction set includes eight addressing modes and supports 8-, 16-, and 32-bit data types.

1.1 General Operation

The MC68020 uses a nonmultiplexed bus with 32-bit wide address and 32-bit wide data bus. The asynchronous bus structure allows easy interfacing to the outside world. The processor can transfer data in a minimum of three clock cycles. Otherwise, wait states in clock period increments will be inserted. The processor drives the address lines (A0-A31), the size lines (SIZ0, SIZ1) and the function code signals (FC0-FC2) on every cycle, independent of a cache hit or miss.

The address and data strobes indicate that the current cycle is not a cache cycle and that the outputs are strobed to be valid.

The MC68020 supports accesses to 8/16/32 bit devices with its dynamic bus sizing mechanism. During operand transfer cycles, the size of the data transfer is indicated by the SIZ0, SIZ1 output signals. The slave device uses the DSACK0, DSACK1 signal according to its data bus width to terminate the cycle. If the cycle is terminated with bus error (BERR signal sensed by the processor), exception handling starts based on the current cycle. The exception vector table occupies 1 Kbyte memory space.

The bus controller inside the MC68020 manages the bus mastership of the local bus FLXibus. The bus controller arbitrates the local bus in such a way that the processor itself has lowest priority in becoming bus master. This means that on request of an alternate master, the MC68020 will grant the bus to the alternate device as soon as possible.

1.2 The Instruction Set

For the 68020 instruction set as well as further information, please refer to the *"MC68020 User's Manual"*.

1.3 Exception Vector Table of the 68020

The following table lists all exception vectors defined for the 68020 Processor.

Table 6: Exception Vector Assignments

Vector Number(s)	Vector Offset (Hex)	Assignment
0	000	Reset Initial Interrupt Stack Pointer
1	004	Reset Initial Program Counter
2	008	Access Fault (Bus Error)
3	00C	Address Error
4	010	Illegal Instruction
5	014	Integer Divide by Zero
6	018	CHK, CHK2 Instruction
7	01C	FTRAPcc, TRAPcc, TRAPV Instructions
8	020	Privilege Violation
9	024	Trace
10	028	Line 1010 Emulator (Unimplemented A-Line Opcode)
11	02C	Line 1111 Emulator (Unimplemented F-Line Opcode)
12	030	(Unassigned, Reserved)
13	034	Defined for MC68020/MC68030, not for MC68040
14	038	Format Error
15	03C	Uninitialized Interrupt
16-23	040-05C	(Unassigned, Reserved)
24	060	Spurious Interrupt
25	064	Level 1 Interrupt Autovector
26	068	Level 2 Interrupt Autovector
27	06C	Level 3 Interrupt Autovector
28	070	Level 4 Interrupt Autovector
29	074	Level 5 Interrupt Autovector
30	078	Level 6 Interrupt Autovector
31	07C	Level 7 Interrupt Autovector
32-47	080-0BC	TRAP #0-15 Instruction Vectors
48	0C0	FP Branch or Set on Unordered Condition
49	0C4	FP Inexact Result
50	0C8	FP Divide by Zero
51	OCC	FP Underflow
52	ODO	FP Operand Error
53	OD4	FP Overflow
54	0D8	FP Signaling NAN
55	ODC	FP Unimplemented Data Type
56	0E0	Defined for MC68030 and MC68851, not for MC68040
57	0E4	Defined for MC68851, not for MC68040
58	0E8	Defined for MC68851, not for MC68040
59-63	0EC-0FC	(Unassigned, Reserved)
64-255	100-3FC	User Defined Vectors (192)

2. THE GATE ARRAY FGA-002A

The IBC-20 board is equipped with the powerful FORCE Computers Gate Array FGA-002A. It provides a 68020/30 processor compatible interface, a local I/O bus supporting 68000- and 8080- family I/O devices and a VMEbus interface with system controller facility. The 281-pin device features a high performance 32-bit DMA Controller, two independent Message Broadcast Channels (FMB), eight Mailboxes, an 8-bit watchdog timer, Interrupt Management and local control logic. The gate array contains decoding and timing circuitry and controls access to the Local I/O bus, the VMEbus and to the Main Memory. The FGA-002A is clocked by a 32.0 MHz clock and a 25.0 MHz clock. The 32.0 MHz clock is used by internal control logic and the Timer. The 25.0 MHz clock drives the DMA controller and control logic which is associated with the processor bus. The registers of FGA-002A are accessible by the processor and by alternate FLXibus masters. Detailed description of the FGA-002A features with corresponding registers can be found in the FGA-002A Gate Array User's Manual.

2.1 The Processor Interface

The processor interface signal lines of the FGA-002A are connected to the MC68020 microprocessor and to the FLXibus (Force Local eXpansion interface bus). The gate array monitors the FLXibus/68020 signals and decodes accesses to the Main RAM, the VMEbus, the local I/O devices and to its own registers. The FGA-002A becomes bus master of the FLXibus if the VMEbus or the DMA Controller accesses the shared Main memory or the EAGLE Module.

2.2 The VMEbus Interface

The VMEbus compatible interface of FGA-002A provides control of the data transfer bus, the priority interrupt bus and features system control functions. **Since there is a 4-level arbiter provided outside in the LCA device, the single level arbiter of FGA-002A cannot be used on this board.** By default, the board boots up with the single level arbiter disabled. The VMEbus control-, address-, and data-lines are connected to the gate array through buffers and transceivers.

2.3 The Local I/O Interface

The Local I/O interface of FGA-002A is 8-bits wide. It supports 68000 family devices as well as 8080 family devices with separate read and write strobes. The FGA-002A manages the data flow to/from the onboard devices of IBC-20 and generates the access cycle to the Local I/O bus. The devices which are connected to the Local I/O interface of FGA-002A are the Boot EPROM, the Local SRAM, the FLASH EPROM, the SCC Serial I/O controller, the CIO Counter/Timer unit, the LCA and the Real Time Clock.

2.4 The 32-bit DMA Controller

The 32-bit DMA Controller provides high speed data transfer between the VMEbus and through the FLXibus interface to the on-board Main RAM and to devices on the EAGLE modules.

The DMA Controller can be programmed and started by the processor or alternate masters of the FLXibus.

The DMA controller supports aligned and unaligned data transfers. Internal logic first aligns the data transfers to take full advantage of the 32-bit structure of the VMEbus and the local FLXibus. The DMA transfers data in bursts of 32 byte. After being started, the DMA reads the data from the source port into a 32 byte deep internal FIFO. Then the bus of the source port will be released and the bus of the destination port will be requested for the next transfer burst. This operation scheme guarantees that the DMA does not block any bus and therefore increases overall system performance. It will also maintain real time capability of the system. Data transfers by the DMA Controller on the VMEbus will let the processor access all local I/O devices, the EPROM area, the shared Main RAM and the FLXibus without performance degradation. Data transfers between VME and the Main RAM allows the local processor to operate at 60-70%.

The DMA Controller runs with 25.0 MHz clock and executes 68020/30 processor compatible cycles to the FLXibus. The access time of the Main Memory devices guarantee the DMA a 5-clock access cycle what results in a maximum transfer speed of 20 Mbytes/second. Depending on the successful completion of the task, the DMA generates either a normal termination interrupt or an error termination interrupt, if the task has been aborted or a bus error occurred.

2.5 The FORCE Message Broadcast Channels (FMB)

The FGA-002A provides two fully independent message broadcast channels supporting high level multiprocessor communication. Channel A is capable of storing eight byte messages and channel B stores a single byte message. Each channel receives the message from a VMEbus master through a dual ported FIFO. After having received the message byte, the addressed channel (A or B) requests interrupt service from the processor. The interrupt level is selectable individually for the channels inside the FGA-002A. The address range in which FGA-002A decodes FMB message cycles from VME is software programmable inside the gate array. This area only can be used for cycles according to the FMB message protocol.

2.6 Mailboxes

The FGA-002A includes eight Mailboxes. Each of them may interrupt the local processor. The interrupt level is programmable with individual interrupt vector for the Mailboxes. The Mailboxes are accessible from VMEbus side as well as by the processor or a FLXibus master.

2.7 The Timer

The timer of FGA-002A consists of an 8-bit synchronous down counter/timer and can be clocked by frequencies from 1 MHz to 0.5 Hz. The clock frequencies and the operation modes are selectable by software. The counter/timer may generate periodical interrupts or a single interrupt after timeout. It can also be used as a watchdog timer which may indicate a hardware failure of the board by asserting the VMEbus signal line SYSFAIL* to low state.

2.8 The Interrupt Management

The FGA-002A gate array handles interrupt requests of the onboard I/O devices, the seven VMEbus interrupts and the interrupt sources inside FGA-002A. The request level of an interrupt source can be programmed to interrupt the processor at any level. The interrupt vector can be created by the FGA-002A itself or may be fetched from the I/O device or the VMEbus. Prioritization of the interrupt sources which are supported by FGA-002A is done inside the gate array.

3. THE EXPANSION MODULE CONNECTOR (IBC MOD-1)

This new IBC-20 revision 2 board includes the Expansion Module Connector P5, which allows the user to enhance the functions of the base board by using the optionally available IBC MOD-1 Module. The IBC-20 board may be upgraded with a Floating Point Coprocessor and additional Flash EPROM with the IBCMOD-1.

The IBC MOD-1 module is described in Section 8 of this manual.

4. THE EAGLE INTERFACE

The IBC-20 board features I/O and memory expansion capability by providing two EAGLE slots. The slots are interfaced to the Force Local eXpansion interface bus (FLXibus). Both I/O connectors of the EAGLE slots can use the VME/P2 I/O signals.

The EAGLE interface is built according to the EAGLE MODULE Specification by FORCE COMPUTERS.

4.1 The EAGLE Module Slots

The IBC-20 provides two slots at which EAGLE modules can be mounted. Both EAGLE slots of the IBC-20 board are able to hold the same EAGLE Module. Each module may become local bus master on the FLXibus and send interrupts to the processor.

The IBC-20 board recognizes an EAGLE module as being plugged in when the module drives the MODINS pin to low level. In this case, the IACK Daisy Chain (IACKIN/IACKOUT) and the local arbitration daisy chain (BGIN/BGOUT) pass through the EAGLE module. If the MODINS pin is high, the daisy chain signals bypass the EAGLE module slots.

The bus mastership of the FLXibus is prioritized by a local Bus Grant daisy chain signal line. The order of the bus mastership on the FLXibus is as follows:

1st (highest)	priority:	EAGLE Slot 2
2nd	priority:	EAGLE Slot 1
3rd	priority:	FGA-002A Gate Array
4th (lowest)	priority:	MC68020 microprocessor

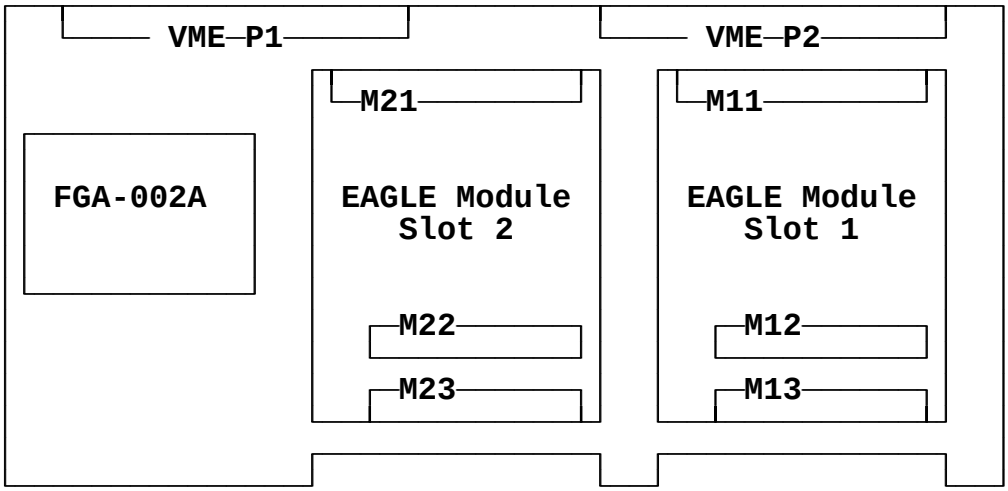
Additional information is given in ***" Bus Arbitration of the FLXibus"***.

Interrupts which use the same request level are prioritized by a local IACKIN/IACKOUT daisy chain line. Please refer to *"The Interrupt Structure of the Board"* for more details.

The pinout of the EAGLE I/O interface connectors can be found in Section 4, *"The Appendix to the Hardware User's Manual."*

Figure 4 shows the location of the EAGLE Module slots 1 and 2 with their FLXibus connectors M12, M13, M22, M23, and the EAGLE I/O connectors M11 and M21.

Figure 4: The EAGLE Module Slots



4.2 The EAGLE I/O Connectors (Slots 1 & 2) and VME/P2 Connection

A new feature on the IBC-20 revision 2 board is that the EAGLE I/O connector of module slot #2 can now be connected to the VME/P2 connector. On previous board revisions, the 64 I/O pins of the VME/P2 were connected to the EAGLE I/O connector of slot #1 only.

The connection of EAGLE slot #2 to the VME/P2 is achieved through the I/O selection field B2.
The I/O selection field connects 32 pins of the VME/P2 connector (P2/C1-C31) either to Eagle slot #1 (default) or to Eagle slot #2. The VME/P2 A1-31 pins are hard wired to the Eagle Slot #1.

4.2.1 The I/O Selection Field B2

The I/O selection field B2 allows both Eagle module slots to be connected to the VME/P2 connector.

The I/O selection field B2 is a socket with 3 x 32 pin matrix. A bridge array with 32 bridges is plugged into the B2 socket. This connects the VME/P2 pins to the I/O connectors of the corresponding eagle slot. The bridge array can be used for both configurations.

By default, the bridge array connects rows A and B of the I/O selection field. It attaches the VME/P2 pins C1-31 to the I/O connector of Eagle slot #1. This configuration is compatible to earlier revisions of the IBC-20.

If the application requires that the I/O connector of Eagle slot #2 needs to be attached to the VME/P2 pins C1-31, the bridge array must be plugged in so that it connects the rows B and C of the I/O selection field.

4.2.2 The Pin Assignment of the I/O Selection Field B2

The table on the following page shows the pin assignment of the I/O selection field. The A row pins are connected to the Eagle slot #1, while the C row pins go to Eagle slot #2. The B row pins are attached to the VME/P2 connector.

Please note that Eagle slot #2 is connected to the I/O selection field by its A1-31 pins, while the A1-31 pins of slot #1 are hard wired to the VME/P2 connector. This layout allows the A1-31 pins of both eagle module slots to be available at the VME/P2 connector.

The I/O selection field also allows various connections between the VME/P2 connector and the Eagle I/O connectors.

The following pages contain figures which highlight the VME/P2 connection to the I/O connectors of EAGLE slots #1 and #2. Figure 5 shows a simplified block diagram of the EAGLE I/O and VME/P2 Connection. Figure 6 shows a connection diagram of I/O Selection Field B2 and Figure 7 is a location diagram of B2. Figure 8 shows the two possible configurations for the installation of the bridge array on selection field B2.

Table 7: Pin Assignments of the I/O Selection field B2

PIN	ROW		
	A	B	C
1	MOD1-C1	VME/P2-C1	MOD2-A1
2	MOD1-C2	VME/P2-C2	MOD2-A2
3	MOD1-C3	VME/P2-C3	MOD2-A3
4	MOD1-C4	VME/P2-C4	MOD2-A4
5	MOD1-C5	VME/P2-C5	MOD2-A5
6	MOD1-C6	VME/P2-C6	MOD2-A6
7	MOD1-C7	VME/P2-C7	MOD2-A7
8	MOD1-C8	VME/P2-C8	MOD2-A8
9	MOD1-C9	VME/P2-C9	MOD2-A9
10	MOD1-C10	VME/P2-C10	MOD2-A10
11	MOD1-C11	VME/P2-C11	MOD2-A11
12	MOD1-C12	VME/P2-C12	MOD2-A12
13	MOD1-C13	VME/P2-C13	MOD2-A13
14	MOD1-C14	VME/P2-C14	MOD2-A14
15	MOD1-C15	VME/P2-C15	MOD2-A15
16	MOD1-C16	VME/P2-C16	MOD2-A16
17	MOD1-C17	VME/P2-C17	MOD2-A17
18	MOD1-C18	VME/P2-C18	MOD2-A18
19	MOD1-C19	VME/P2-C19	MOD2-A19
20	MOD1-C20	VME/P2-C20	MOD2-A20
21	MOD1-C21	VME/P2-C21	MOD2-A21
22	MOD1-C22	VME/P2-C22	MOD2-A22
23	MOD1-C23	VME/P2-C23	MOD2-A23
24	MOD1-C24	VME/P2-C24	MOD2-A24
25	MOD1-C25	VME/P2-C25	MOD2-A25
26	MOD1-C26	VME/P2-C26	MOD2-A26
27	MOD1-C27	VME/P2-C27	MOD2-A27
28	MOD1-C28	VME/P2-C28	MOD2-A28
29	MOD1-C29	VME/P2-C29	MOD2-A29
30	MOD1-C30	VME/P2-C30	MOD2-A30
31	MOD1-C31	VME/P2-C31	MOD2-A31
32	MOD1-C32	VME/P2-C32	MOD2-A32

MOD1-C01..32: Eagle Slot #1 I/O Connector pins row C
MOD2-A01..32: Eagle Slot #2 I/O Connector pins row A
VME/P2-C01..32: VME/P2 Connector pins row C

Figure 5: Block Diagram of the EAGLE I/O Connectors to the VME/P2

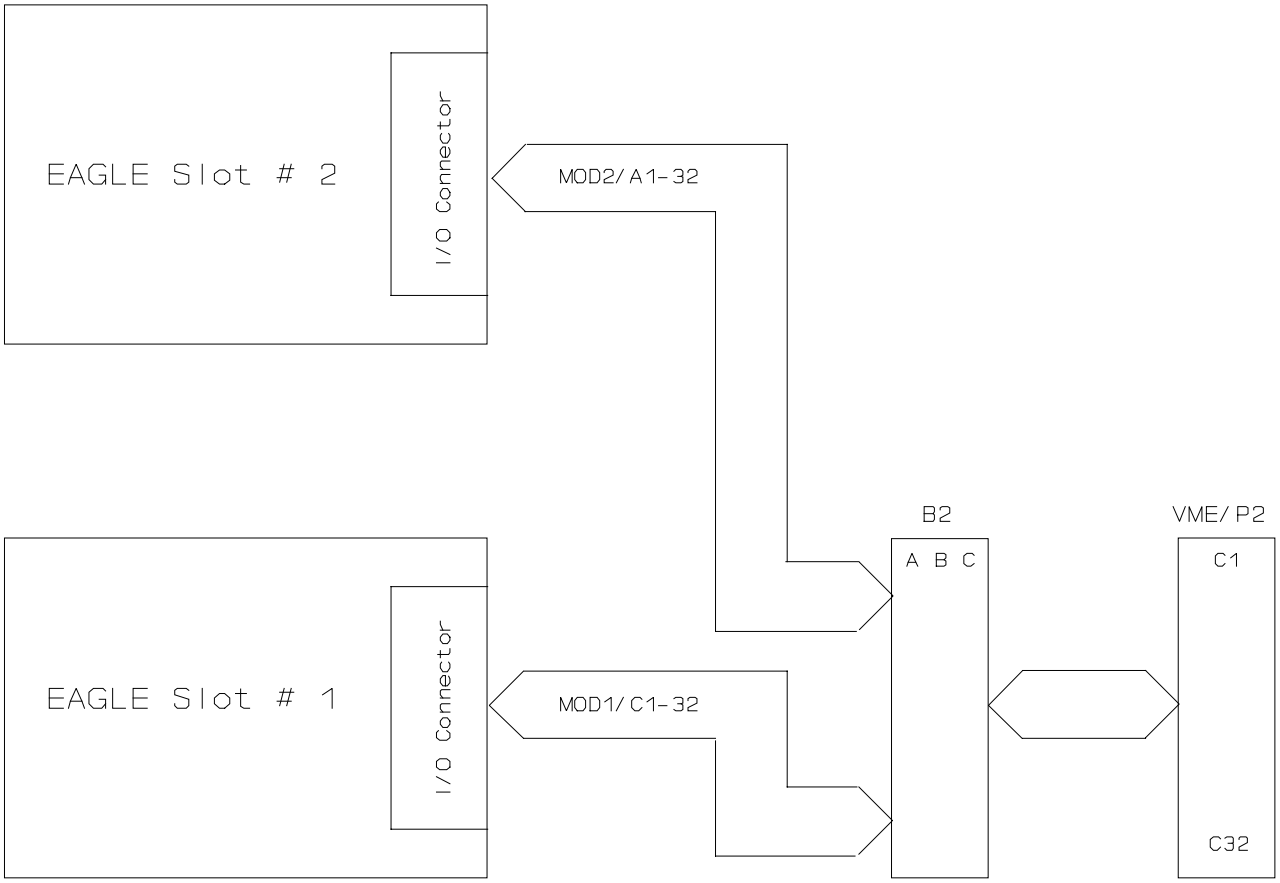


Figure 6: Connection Diagram of the I/O Selection Field

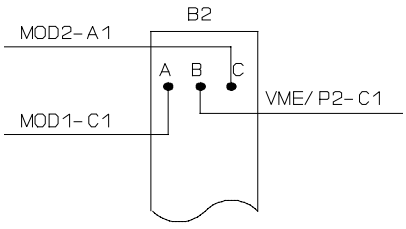


Figure 7: Location Diagram of the I/O Selection Field B2

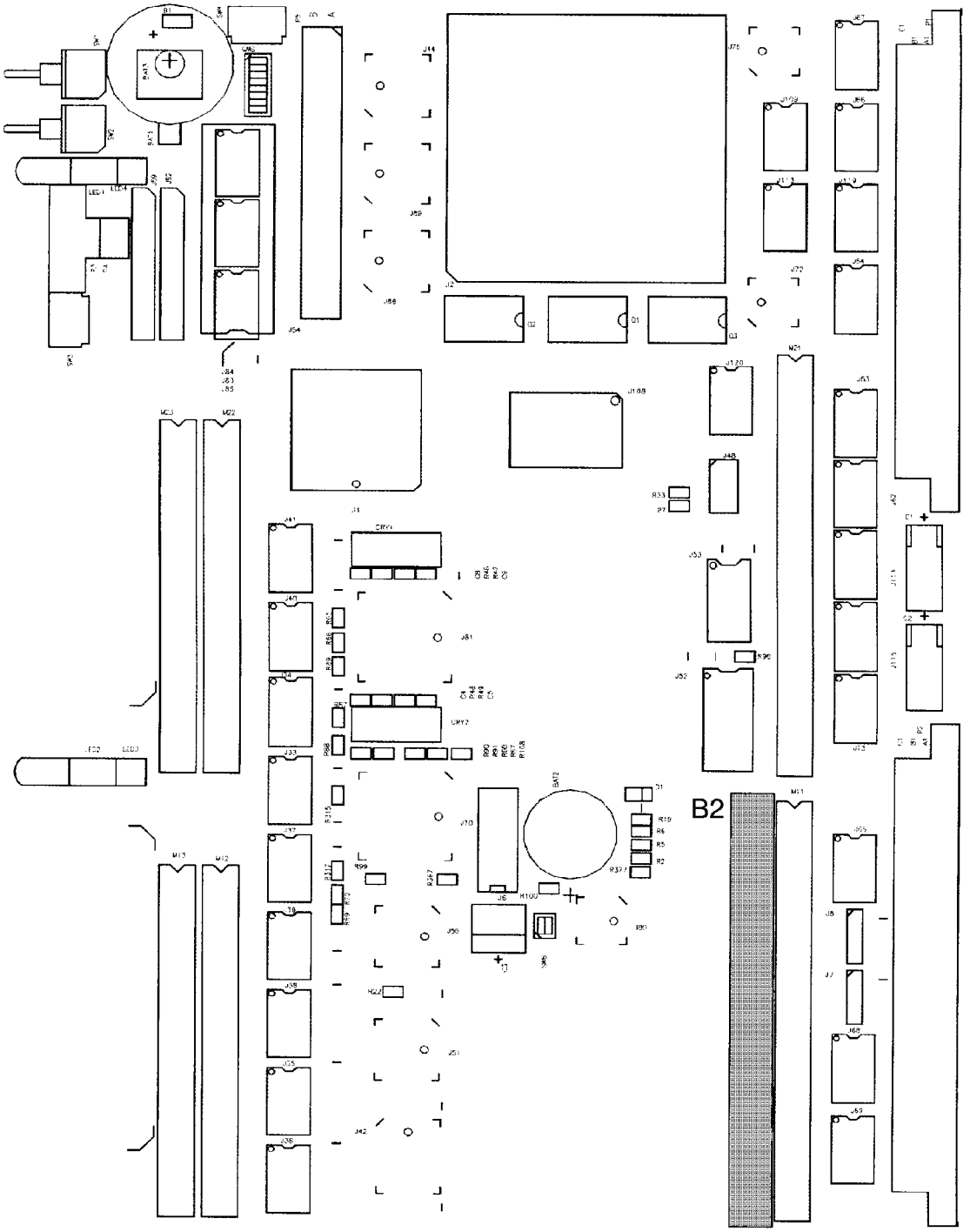
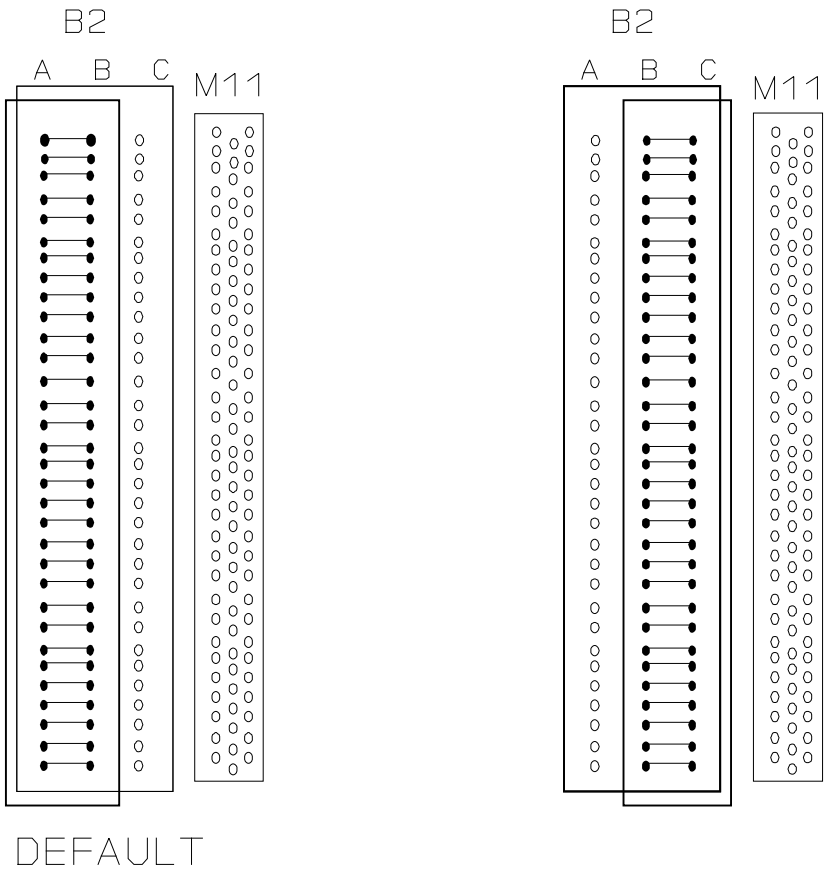


Figure 8: Installation of the I/O Bridge Array



By default, the bridge array connects rows A and B of the I/O selection field. This attaches the VME/P2 pins C1-31 to the I/O connector of EAGLE slot #1. This configuration is compatible to earlier revisions of the IBC-20.

If the I/O connector of EAGLE slot #2 needs to be attached to the VME/P2 pins C1-31, the bridge array has to be plugged in so that it connects rows B and C of the I/O selection field.

5. THE SHARED MAIN MEMORY

The IBC-20 board is available with 512 Kbyte, 1 Mbyte, 2 or 4 Mbyte Main memory capacity for system and user code and data. The Main memory of the IBC-20 board is built of static RAM which can be backed up by the +5VSTDBY line of the VMEbus. When power is applied to the +5VSTDBY line data is saved.

The Main RAM is accessible by the local processor, the DMA controller, the VMEbus and by EAGLE modules through the FLXibus. Accesses from the VMEbus to the Main RAM is handled via the FGA-002A gate array.

The size of the Main memory is software selectable inside FGA-002A and is determined by the Boot software. Assuming that the Main memory covers the maximum memory size of 4 Mbyte, the routine tests this space in 64 Kbytes steps for writable/readable memory. After having found the last writable/readable memory location, the required FGA-002A registers will then be set to the appropriate memory size.

In the following address ranges, the Main memory is accessible for the processor, the EAGLE modules and the FGA-002A DMA controller:

Table 8: Shared Main Memory

512 Kbyte memory capacity:	$00000000 - $0007FFFF
1 Mbyte memory capacity:	$00000000 - $000FFFFF
2 Mbyte memory capacity:	$00000000 - $001FFFFF
4 Mbyte memory capacity:	$00000000 - $003FFFFF

5.1 Main Memory Access by the MC68020

The processor accesses the Main memory by using the control, address and data lines of the FLXibus. However, the access will be terminated by a private DSACK for the processor and no DSACK will be generated to the FLXibus. The access time of the SRAM devices guarantees a 1-wait-state access to the Main memory for the local processor.

5.2 Main Memory Access by the DMA Controller

The DMA controller accesses the Main memory via the local FLXibus. The DMA controller operates with 25 MHz clock frequency and drives 68020 compatible cycles to the FLXibus. The access time of the Main memory permits a 2-wait-state operation for the DMA controller.

When the DMA controller is started, the FGA-002A requests mastership of the FLXibus. After the control of the bus has been granted, the DMA controller starts to read the first data block, filling its internal 32 byte deep FIFO. After that, the bus mastership will be relinquished for an alternate FLXibus master before the gate array requests the bus again, in order to let the DMA controller transfer the next data block.

The DMA controller transfers data in blocks of maximum 32 bytes. If source and destination addresses are aligned, the DMA controller performs eight long-word transfers during one local bus mastership. Data transfers from unaligned addresses are made aligned and only the first and/or last transfer of a data block will be a 1 byte, 2 byte or 3 byte transfer.

5.3 Main Memory Access by EAGLE Modules

EAGLE modules may access the Main memory of the IBC-20 base board by using the local FLXibus. The access time of the Main memory for accesses from an EAGLE module is typically 160 ns.
Due to the synchronous operation of the memory control logic and propagation delay tolerances, the access time may vary +/- 40ns.

5.4 Main Memory Access by VME

The Main memory is accessible from the VMEbus via the FGA-002A Gate Array and the FLXibus. The address range, the AM codes and write access protection is software selectable in the gate array.

The start address and end address defines the access address window of the shared RAM and is programmable in 4 Kbyte steps. The selected address range can be made write protected together with the address modifier code selection. For example, the selection could be made so that read/write permission to the shared RAM may only be given to accesses with supervisor code, whereas with user AM code only read accesses may be allowed.

When a VMEbus master accesses the shared RAM, the FGA-002A gate array requests mastership of the FLXibus. After the bus has been granted to the FGA-002A by the processor, the access cycle is executed. On completion of the local read/write cycle, the FGA-002A immediately releases bus mastership of the FLXibus while completing the VMEbus cycle asynchronously.

The access time of the Main memory from VMEbus side depends not only on the board hardware, but also on the opportunity of FGA-002A to become bus master on the FLXibus.

Since FGA-002A is at least in the bus grant daisy chain, the behavior of potential FLXibus masters on EAGLE modules determines the bus mastership of FGA-002A. Therefore, the access time may vary significantly.

5.5 Summary of the Main Memory

Capacity	512 Kbyte (IBC-20) 1 Mbyte (IBC-20/1) 2 Mbyte (IBC-20/2) 4 Mbyte (IBC-20/4)
Address Range	$00000000 - $0007FFFF (IBC-20) $00000000 - $000FFFFF (IBC-20/1) $00000000 - $000FFFFF (IBC-20/2) $00000000 - $003FFFFF (IBC-20/4)
Port Width	32 bit (long word)

6. THE BOOT EPROM

The IBC-20 board provides a 32 pin JEDEC compatible socket for EPROM devices, permitting boot code, monitor and application code to be stored. Devices with capacities from 128 Kbyte up to 512 Kbyte are usable. The EPROM port is 8-bit wide.

Access to the Boot EPROM is controlled by FGA-002A with a fixed timing. This requires that EPROM devices with an access time not slower than 200 ns must be used.

The board is furnished with a 512 Kbyte EPROM device which is installed at the location J54. It contains the boot firmware and the VMEPROM.

Resistor R45 must be removed if EPROM devices with 128/256 Kbyte capacity are going to be used.

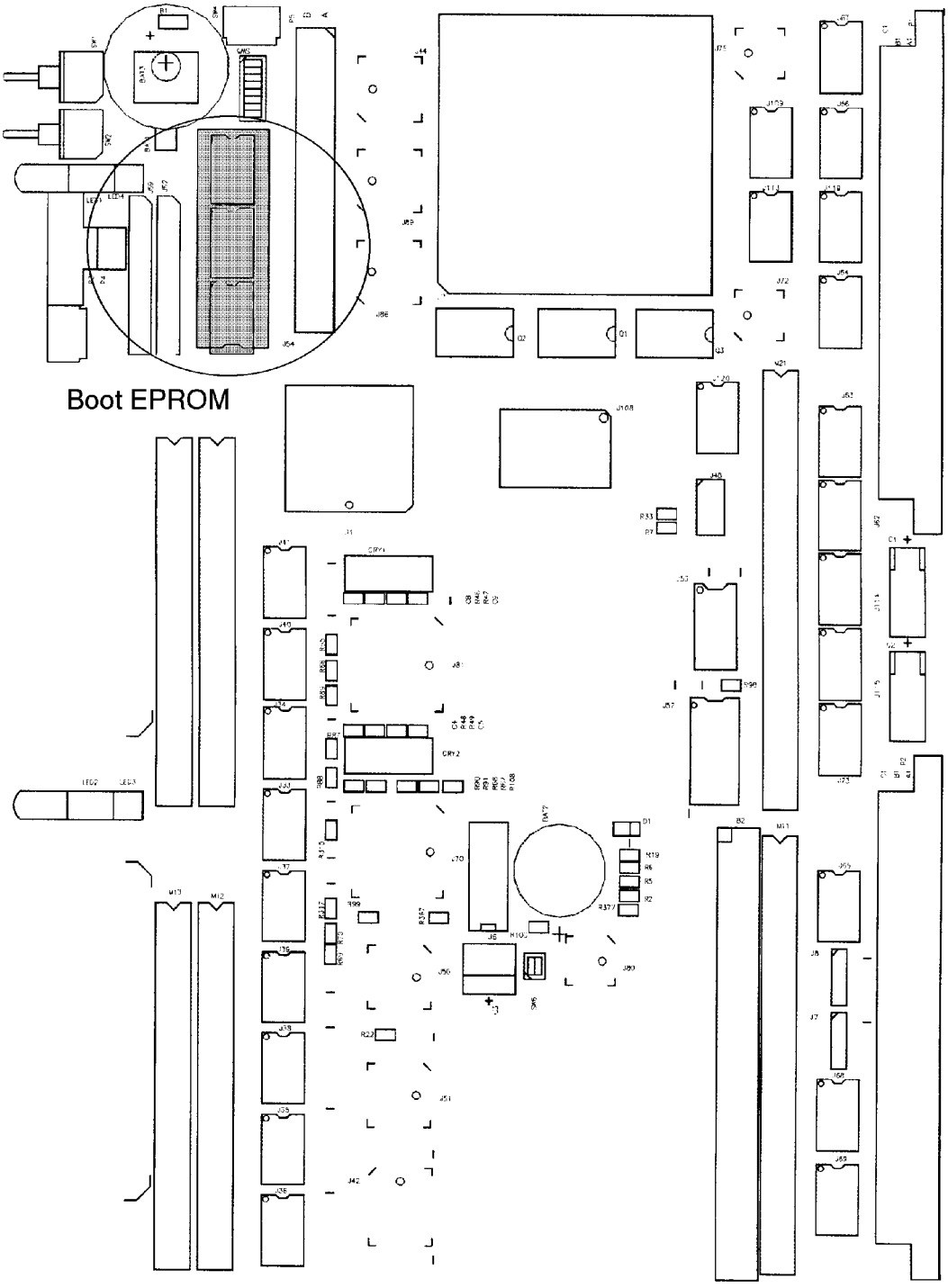
The Boot EPROM is present in the whole area, which is decoded by FGA-002A in the address range

$FFE00000 - $FFEFFFFF

Detailed information covering the boot firmware can be found in the Boot Software Description of *the FGA-002A User's Manual*.

The next figure is a location diagram which shows the Boot EPROM at J54.

Figure 9: Location Diagram of the Boot EPROM



7. THE LOCAL SRAM

The IBC-20 provides a battery backed up local SRAM with 32 Kbyte memory capacity.
The low power static memory is backed up by two on-board batteries (primary and secondary batteries). This saves the data for more than a year.

The +5V STDBY line of the VMEbus is also usable for backing up the local SRAM.

More details concerning the battery backup can be found in the chapter *"Battery Backup Facilities"* of this manual.

The Local SRAM is accessible in the address range **$FFC00000 - $FFCFFFFF**. It appears as a byte port to the processor.

Note

The VMEPROM firmware uses the local SRAM to store parameters for the board set-up. Therefore, the local SRAM is not completely available to the user. Please refer to the *"IBC-20 Firmware User's Manual"* for more information.

8. THE FLASH EPROM

The IBC-20 board holds a FLASH EPROM with 128 Kbyte capacity. The local FLASH EPROM provides a nonvolatile read/writable memory without the need of battery backup for saving data.

The FLASH EPROM can be programmed without removing the device from the board or the board from the System. The FLASH EPROM port is byte wide. It is located in the address range

$FFC80000 - FFCFFFFF

For data security, the FLASH EPROM can be protected from being erased erroneously. Switch SW5-1 selects whether the Flash-EPROM on the IBC-20 base board can be erased or re-programmed. When SW5-1 is set to "OFF", the Flash EPROM is write protected. If set "ON" the Flash EPROM is writable. Figure 10 on the next page shows the location diagram of SW5.

Programming the FLASH EPROM requires a special programming algorithm. Please refer to the FLASH EPROM data sheet in Section 5 of this manual.

The "PROG" command, which is provided by the VMEPROM on-board firmware, allows easy programming of the FLASH EPROM by the user.

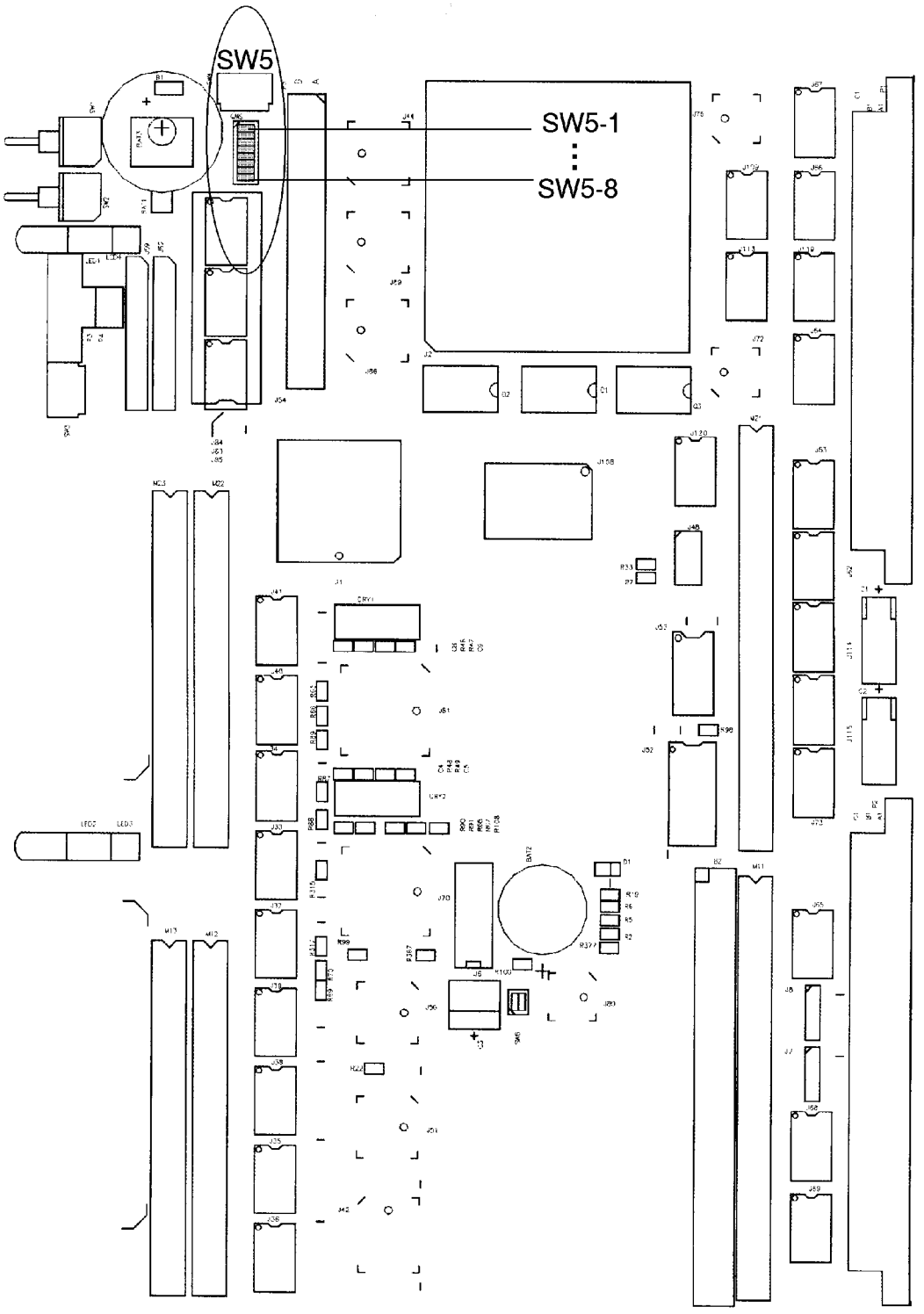
The programming voltage, which is required to program the on-board FLASH EPROM, is supplied by the +12VSWITCH signal line. This line is also available at the FLXibus connectors to support FLASH EPROMS on EAGLE modules. The pins M12/C21 and M22/C21 of the FLXibus connectors supply this programming voltage.

The +12V programming voltage is controlled by a register bit contained in the LCA device. The access address of the register is $FF803E11. Bit "0" is used to control this function. Other bits of this register are don't care, but should be written with their value with regard to future usage of these bits. User program routines should reset the register bit to "0" after the programming sequence has been terminated to achieve data security during power down.

Table 9: Setting the FLASH EPROM Programming Voltage

Register Address	Mode	Description	Bit 0
$FF803E11	R/W	FLASH EPROM Programming Voltage Off	0
		FLASH EPROM Programming Voltage On	1

Figure 10: Location Diagram of Switch SW5



9. THE LOGIC CELL ARRAY LCA

The Logic Cell Array (LCA) device is a programmable gate array whose function is configured each time the board is powered-up. The configuration data is held in a dedicated serial EPROM device and will be read by the LCA automatically. During the loading procedure the board is held under reset by a local configuration-reset signal.

The LCA device which is installed on the IBC-20 is used for local control and contains several board- and system functions.

The following functions are provided by the LCA:

- VMEbus Interrupter
- 4-Level VMEbus Arbiter
- Support for "A24" Standard VME access to Shared RAM
- FLASH EPROM programming voltage

The functions are described in the corresponding chapters.

The LCA holds several registers for the control of these functions. The data port of the LCA is byte wide. The following table displays the register summary of the LCA.

Table 10: LCA Register Summary

Address HEX	Label	Reset Value	Mode	Description
FF803E00	IRQGEN	$01	R/W	Interrupt Generation Reg.
FF803E01	IRQVEC	$00 Note 1	R/W	Interrupt Vector Reg.
FF803E02	ARBCON	-- Note 2	R/W	Arbitration Control Reg.
FF803E10	A24REG	-- Note 3	R/W	A24 Register (External)
FF803E11	CTL1	-- Note 4	R/W	Control Register 1

Note 1: Only after power-up reset.
Note 2: See bit description of this register
Note 3: Register is not reset. Content is not readable. Returns always $FF.
Note 4: Register bit 0 is forced to '0' by reset.

9.1 Interrupt Generation Register IRQGEN

The IRQGEN register is assigned to the VME Interrupter function of the IBC-20 board. Each register bit controls an interrupt level of VME. Bits D7-D1 are assigned to the VME interrupt levels IRQ 7-1. Bit 0 is not present since there is no interrupt level #0 defined by VME. This bit can be written but returns always "1" if the register is read. VMEbus interrupts are generated when the register bit(s) are written "1". The interrupt will be cleared automatically by the acknowledge cycle which resets the register bit to zero. Reset clears the register to $01.

Table 11: Interrupt Generation Register ($FF803E00)

D7	D6	D5	D4	D3	D2	D1	D0
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	--

Bits D7-D1: VME interrupt level IRQ7-IRQ1

"1" = VME Interrupt active
"0" = VME Interrupt not active

Bit D0: Not existing. Returns always "1".

9.2 Interrupt Vector Register IRQVEC

The Interrupt Vector Register holds the byte wide interrupt vector, which will be output by the LCA during an interrupt acknowledge cycle. The register is read/writable. If there is an interrupt request pending, the content must not be altered until the interrupt has been serviced. The Interrupt Vector Register is reset only after power-up to $00.

Table 12: Interrupt Vector Register ($FF803E01)

D7	D6	D5	D4	D3	D2	D1	D0
INTERRUPT VECTOR CODE							

Bits D7-D0: Interrupt Vector Code

9.3 The Arbiter Control Register ARBCON

The Arbitration Control Register provides the selection of the Bus Request level (BR3-BR0) on VME and the Arbitration Mode of the 4-level VMEbus arbiter by software.

Table 13: Arbiter Control Register ARBCON ($FF803E02)

D7	D6	D5	D4	D3	D2	D1	D0
SOURCE CTL	SYSCON STATE	RESERVED		ARBITRATION MODE		BR LEVEL SELECTION	

Bit D7: **Request Level Source Control**
This bit controls whether the selection of the VMEbus request level is done by hardware (Switch SW5-6/7) or by bits D1-D0 of the ARBCON register. This bit can only be set to "1" if both switches SW5-6/7 are in the **"OFF"** position. The bit is cleared to "0" with reset.

0 = Switches SW5-6/7 determine the VMEbus request level
1 = Bits D1-D0 determine the VMEbus request level

Bit D6: **System Controller Status**
The bit displays whether the "Slot 1" System Controller functions of the IBC-20 are enabled or not. If the bit is read "1", the 4-level arbiter is enabled and the board drives the SYSCLK and BCLR signal. In this case, the board has to reside in Slot #1 of the VMEbus environment. Writing this bit is without influence.

0 = System Controller Functions are disabled (SW5-8 = "OFF")
1 = System Controller Functions are enabled (SW5-8 = "ON")

Bits D5-D4: These bits are reserved. When read, "1" is returned. They should be written with the value which is actually returned.

Bits D3-D2: Arbitration Mode Selection
These bits select the arbitration mode of the VMEbus arbiter. Reset clears the bits to "0".

D3	D2	Arbitration Mode
0	0	Prioritized
0	1	Round-Robin
1	0	Prioritized Round-Robin
1	1	Prioritized Round-Robin

Bits D1-D0: BR3-BR0 Level Selection
These bits select the bus request level of the board on VME if bit D7 is set to 1.

D1	D0	VME Request Level
0	0	BR0
0	1	BR1
1	0	BR2
1	1	BR3

9.4 The Register A24REG

The A24-Register is used to support accesses to the Shared Main RAM from VME with Standard Addressing Mode A24. The A24 Register is physically built outside the LCA device. It appears to be an LCA internal register since its access address is decoded by the LCA device at $FF803E10. The content of the register is not readable. When read, $FF will be returned. The register will not be cleared by reset. Additional information concerning the value which has to be written to the register can be found in the chapter, "*RAM Access with Standard Addressing AM Code*".

Table 14: The A24-Register ($FF803E10)

D7	D6	D5	D4	D3	D2	D1	D0
A31-A24 ADDRESS BYTE							

Bits D7-D0: Correspond to the A31-A24 Address Value.

9.5 The Register CTL1

Bit D0 of the CTL1 Register controls the programming voltage for the on-board FLASH EPROM and for FLASH EPROM devices on EAGLE modules. The register is read/writable. Reset forces the bit to "0".

Table 15: The CTL1 Register ($FF803E11)

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED							PROG CTL

Bit D0: Programming Voltage Control

The register bit controls the +12V programming voltage for the local and EAGLE module mounted FLASH EPROM devices.

0 = Programming voltage off
1 = Programming voltage on.

10. THE SERIAL COMMUNICATION CONTROLLER SCC Z85C30

The Serial Communication Controller Z85C30 (SCC) is a dual channel, multiprotocol communication device in CMOS technology, which satisfies a wide variety of serial communications protocols. The SCC provides two multiprotocol, full duplex receiver/transmitter channels, each with separate crystal oscillator, baud rate generator and Digital Phase Locked Loop (DPLL).

Both serial channels A and B of the SCC are interfaced with FH-002 hybrids providing two RS-232C compatible serial ports.

The clock for the baud rate generator is derived from the 14.7456 MHz crystal. The baud rate can be selected via VMEPROM, which allows baud rates up to 38400 baud. The default baud rate set by VMEPROM after power-up is 9600 baud.

The interrupts are handled via the LOCAL #5 interrupt channel of FGA-002A.

Accesses to the control registers of the SCC are only done with indirect addressing. In this process, a pointer register is used to address the desired control register. This means that writing to a control register requires two write cycles, and reading from a control register requires both a write and read operation. The receive/transmit data registers of the Z85C30 are accessed directly.

10.1 Address Map of the SCC Registers

The complete address map of the SCC Read/Write registers is provided in the data sheet of the device, which is provided in Section 5 of this manual.

The following table shows access address of the address pointer registers and the data registers, which are directly accessible registers of the SCC.

Table 16: SCC Register Address Map

SCC Base Address: FF802000			
Address HEX	**Mode**	**Description**	**Channel**
$FF802000	R/W	Control Register WR0/RR0 (Pointer)	B
$FF802001	R/W	Data Receive/Transmit	B
$FF802020	R/W	Control Register WR0/RR0 (Pointer)	A
$FF802021	R/W	Data Receive/Transmit	A

10.2 Summary of the SCC

Device	Z85C30 SCC
Base Address	$FF802000
Port Width	Byte
Interrupt Request Level	Software programmable
FGA-002A Interrupt Channel	Local IRQ #5

11. THE SERIAL I/O PORTS

The board contains two serial I/O ports which are built around the Z80C30 Serial Communications Controller (SCC). The TTL level signals are converted to RS-232C level by the field replaceable hybrid devices FH-002. The interface signals are available at the 9-pin micro D-Sub connectors on the front panel and allow the channels to be used as console and debugging ports. A 1:1 adapter cable, which is optionally available, provides the front panel connector signals at a 9-pin female D-Sub connector allowing direct connection of a terminal with standard cable.

Note

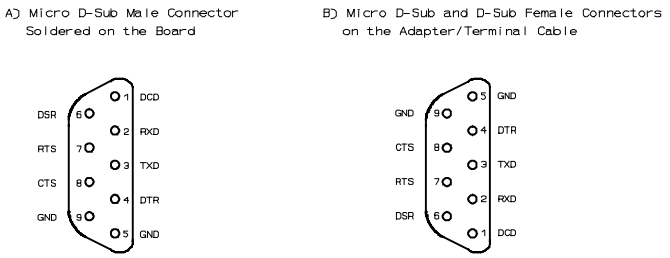
The firmware uses the CTS and DCD signal lines to check if there is a terminal connected. In order to communicate with the board via the debugging port, the terminal must support these signals. Also, the terminal has to be connected prior to the board boots up. Otherwise, a special port which is provided by the firmware will be used. For detailed information please refer to the *"IBC-20 Firmware User's Manual"*.

11.1 The Front Panel Connector Pinout

The following table lists the I/O signals available at each of the two 9-pin micro D-Sub front panel connectors. Figure 11 shows the pinout of the male micro D-Sub front panel connectors and the 9-pin female D-type connectors on the adapter cable.

I/O Signal	Input	Output	Front Panel Connector Pin	Description
DCD	X		1	Data Carrier Detect
RXD	X		2	Receive Data
TXD		X	3	Transmit Data
DTR		X	4	Data Terminal Ready
GND			5	Signal GND
DSR	X		6	Data Set Ready
RTS		X	7	Request to Send
CTS	X		8	Clear to Send
GND			9	Signal GND

Figure 11: Pinout of the Front Panel Connector and Adapter Cable Connector



12. THE COUNTER/TIMER-I/O UNIT CIO Z8536

The Z8536 (CIO) unit is a general purpose counter/timer and I/O device. It provides two 8-bit I/O ports, a 4-bit I/O port and three independent 16-bit counter/timers. The Z8536 unit is driven with a 4 MHz clock frequency.
The I/O ports feature programmable polarity, direction and pattern recognition logic. Each of the three counters provides pulse, one-shot and square-wave duty cycles. Counter/timer 1 can be linked with counter 2 to establish a 32-bit counter.

12.1 CIO Interrupt Support

The CIO unit is able to respond to an interrupt acknowledge cycle with its own interrupt vector.

While the Timers share a common vector, the ports A and B have individual vectors.

Additional interrupt support is provided for Timer 2 and Timer 3. The outputs of these timers are connected to separate interrupt channels of FGA-002A, so they can use the dedicated interrupt vectors.

The following table shows the CIO interrupts and their corresponding interrupt channels of FGA-002A:

CIO Interrupt	FGA-002A Interrupt Channel
I/O Port	LOCAL #4
Counter/Timer 2	LOCAL #3
Counter/Timer 3	LOCAL #2

12.2 The I/O Port Control Functions

The I/O ports of the CIO are used to control local functions on the board. The ports are configured by the firmware during the startup sequence of the board.

The ports PA0-PA3 are used to read the value of the "MODE" switch SW3, the second rotary switch SW4 and the assembly code of the IBC MOD-1 module. The assembly code of the IBC MOD-1 module is available at the connector P5 (pins B36-39). Please refer to Section 8 for details about the IBC MOD-1. User LEDs 1-4 are controlled by the Ports PA4-PA7. The further ports are used for special features of the board.

The following table outlines the control functions assigned to the ports and the I/O configuration of the ports when the IBC-20 board boots up with VMEPROM.

Table 17: The I/O Port Control Functions

Port Pin	Pin #	Control Function	Input/Output
PA0	37	Bit 0: "MODE"-Switch/ Rotary Switch SW4 / Assembly Code	I
PA1	36	Bit 1: "MODE"-Switch/ Rotary Switch SW4 / Assembly Code	I
PA2	35	Bit 2: "MODE"-Switch/ Rotary Switch SW4 / Assembly Code	I
PA3	34	Bit 3: "MODE"-Switch/ Rotary Switch SW4 / Assembly Code	I
PA4	33	User LED 1	O
PA5	32	User LED 2	O
PA6	31	User LED 3	O
PA7	30	User LED 4	O
PB0	10	Interrupt Timer 2. Connected to LIRQ3 of FGA-002A	I
PB1	11	Reserved	I
PB2	12	Reserved	I
PB3	13	Reserved	I
PB4	14	State Flash EPROM programming voltage Vpp.	I
PB5	15	Enables A24 Access to Main RAM from VME	O
PB6	16	Distinguishes among PCB Revisions	I
PB7	17	Abort Switch "down" recognition	I
PC0	21	Interrupt Timer 3	O
PC1	22	Reserved	I
PC2	23	Reserved	I
PC3	24	Reserved	I

12.3 Description of the I/O Port Control Functions

Port Pins	Description
PA0-PA3	These four I/O signals are used to read the value of the "MODE" rotary switch SW3, which is accessible through the front panel. In addition, these signals provide the value of the second rotary switch SW4 and the assembly code of the IBC MOD-1 module. The switch values are hexadecimal coded, providing at port PA0 the least significant bit of the 4-bit code and the most significant bit at PA3. The IBC MOD-1 assembly code is described in section 8 of this manual. The switch and assembly code values are found by reading the Port A data register at the following addresses: $FF800C02 = "MODE"-Switch SW3 $FF800C0A = Rotary Switch SW4 $FF800C0E = Module Assembly Code
PA4-PA7	These ports are used to turn on/off the four User LEDs 1-4 on the front panel. The LEDs are turned off with low level at the port pin. If the port pins are not configured, the I/O pins are at high level and the LEDs are turned on.

Description of the I/O port control functions is continued on the next page.

Description of the I/O Port Control Functions (Continued)

Port Pins	Description
PB0	This port provides the output of Counter/Timer 2. It is connected to the FGA-002As interrupt channel LOCAL #3.
PB1-PB3	Reserved
PB4	This port allows to determine whether the 12V programming voltage Vpp for the Flash EPROMs is switched on/off. Logical 0 is read when Vpp is switched off. Logical 1 is read when Vpp is switched on.
PB5	This port is used to enable the access to the Shared Main SRAM of the board with A24 Standard Addressing Mode from VME. After power-up, the port is at high level and the board refuses A24 accesses from VME to the shared Main memory.
PB6	The port is used to determine the actual PCB revision. On PCB revisions 1, logical 1 is read at this port. Logical 0 is read if the PCB revision is 2 or greater. This enables the firmware to support the additional features of the IBC-20 revision 2 board.
PB7	This port is connected to the ABORT switch. Low level can be read if the switch is in the down position. The port can be used as a general purpose input.
PC0	This port is used as output of Counter/Timer 3. It is connected to the FGA-002A's interrupt channel Local IRQ#2. By default, Timer 3 is enabled and provides the system clock for VMEPROM.
PC1-PC3	Reserved

12.4 CIO Register Address Map

The IBC-20 revision 2 board provides an additional rotary switch (SW4) and the expansion module connector P5 to install the optionally available IBC MOD-1 module with a Floating Point Coprocessor and Flash EPROM memory.

To support these additional features of the IBC-20 revision 2 board, the CIO register address map is extended by two addresses.

The two addresses are used to read the rotary switch SW4 and the assembly code, which is supplied by the IBC MOD-1 module. The assembly code determines the amount of memory and the presence of a Floating Point Coprocessor. Please refer to Section 8 for more information about the assembly code of the IBC MOD-1 module.

The additional addresses both access the Port A data register. On the IBC-20 revision 2 board, the Rotary Switch SW4, the Rotary Switch SW5 (also called "MODE" Switch) and the status lines of the IBC MOD-1 module are multiplexed to the port A pins PA0..PA3 of the CIO unit. The multiplexers are controlled by the address lines A2 and A3. Depending on the state of the address lines, one of the connected devices will be read through port A.

The CIO unit data registers of port A, B and C and the pointer register are directly accessible.
The other registers of the Z8536 CIO device must be accessed in a two step operation. To access an internal control register, the address of the target register has to be written to the pointer register in the first step. In the second step, data can be read from or written to the target register.
The register map for the internal control registers can be found in the data sheet of the CIO unit.

Table 18 shows the address map of the directly accessible CIO registers.

Table 18: Directly accessible CIO Registers

CIO Base Address: FF800C00		
Address HEX	**Register**	**Description**
$FF800C00	Port C Data	
$FF800C01	Port B Data	
$FF800C02	Port A Data	PA0..PA3: "MODE" Rotary Switch SW3
$FF800C03	Pointer Register	
$FF800C0A	Port A Data	PA0..PA3: Rotary Switch SW4
$FF800C0E	Port A Data	PA0..PA3: Module Assembly Code

12.5 Summary of the CIO

Device	Z8536 CIO
Base Address	$FF800C00
Port Width	Byte
Interrupt Request Level	Software programmable
FGA-002A Interrupt Channel	Local IRQ #2 (Counter/Timer 3) Local IRQ #3 (Counter/Timer 2) Local IRQ #4 (I/O Port)

13. THE REAL TIME CLOCK RTC 72423

The IBC-20 board provides the Real Time Clock RTC 72423 for clock/calendar function. The RTC features time-of-day, date counter with auto leap year and 12/24 hour format. It may generate periodical interrupts at different rates.

The interrupt output of the RTC is connected to the interrupt channel LOCAL #0 of the FGA-002A gate array. The FGA-002A supports vectored interrupt and allows any interrupt level (1 to 7) to be selected.

When the +5V power is not present the RTC will be supplied by the onboard battery backup system, which also powers the local SRAM. The battery backup saves the RTC function for at least one year after power down.

More information concerning the battery backup system can be found in chapter *"The Battery Backup Facilities."*

13.1 Address Map of the RTC Registers

The RTC 72423 is a four bit device. It must be accessed in byte mode and the upper four bits are "don't care" during read and write access. The base address of the RTC is $FF803000. The following table shows the register layout of the RTC 72423.

Table 19: RTC Register Layout

Address HEX	Offset	Label	Description
FF803000	00	RTC1SEC	1 Second Digit Register
FF803001	01	RTC10SEC	10 Second Digit Register
FF803002	02	RTC1MIN	1 Minute Digit Register
FF803003	03	RTC10MIN	10 Minute Digit Register
FF803004	04	RTC1HR	1 Hour Digit Register
FF803005	05	RTC10HR	PM/AM and 10 Hour Digit Register
FF803006	06	RTC1DAY	1 Day Digit Register
FF803007	07	RTC10DAY	10 Day Digit Register
FF803008	08	RTC1MON	1 Month Digit Register
FF803009	09	RTC10MON	10 Month Digit Register
FF80300A	0A	RTC1YR	1 Year Digit Register
FF80300B	0B	RTC10YR	10 Year Digit Register
FF80300C	0C	RTCWEEK	Week Register
FF80300D	0D	RTCCOND	Control Register D
FF80300E	0E	RTCCONE	Control Register E
FF80300F	0F	RTCCONF	Control Register F

13.2 RTC Programming

The following programming example shows how to read from or write to the RTC. Please note that the RTC must be stopped prior to reading the date and time registers. For further details, please refer to the RTC 72423 Data Sheet in Section 5 in this manual.

Figure 12: RTC Programming Example

```
/***************************************
**  read RTC 72421 and load to RAM      **
**      30-Oct-87  M.S.                 **
***************************************/

setclock(sy)
register struct SYRAM *sy;
{
register struct rtc7242 *rtc = RTC2;
register long count=100000l;

rtc->dcontrol = 1;                      /* hold clock */
while(count--)
    if(rtc->dcontrol&0x02)
          break;
if(!count)
   { printf("\nCannot read Realtime Clock");
     rtc->dcontrol = 0;
     return; }
sy->_ssec[0] = (unsigned char)((rtc->sec10reg&0x07)*10 +
(rtc->sec1reg&0x0f));
sy->_smin    = (unsigned char)((rtc->min10reg&0x07)*10 +
(rtc->min1reg&0x0f));
sy->_shrs    = (unsigned char)((rtc->hou10reg&0x03)*10 +
(rtc->hou1reg&0x0f));
sy->_syrs[0] = (unsigned char)((rtc->yr10reg&0x0f)*10 +
(rtc->yr1reg&0x0f));
sy->_sday    = (unsigned char)((rtc->day10reg&0x03)*10 +
(rtc->day1reg&0x0f));
sy->_smon    = (unsigned char)((rtc->mon10reg&0x01)*10 +
(rtc->mon1reg&0x0f));
rtc->dcontrol = 0;                      /* start clock */
}

/***************************************
**     write RTC 72421 from RAM         **
**      30-Oct-87  M.S.                 **
***************************************/

writeclock(sy)
register struct SYRAM *sy;
{
register struct rtc7242 *rtc = RTC2;
register long count=100000l;
rtc->dcontrol = 1;                      /* hold clock */
while(count--)
   if(rtc->dcontrol&0x02)
          break;
if(!count)
   { printf("\nCannot read Realtime Clock");
     rtc->dcontrol = 0;
     return; }
rtc->fcontrol = 5;
rtc->fcontrol = 4;                      /* 24-hour clock */
rtc->sec10reg = sy->_ssec[0]/10;/
rtc->sec1reg  = sy->_ssec[0]%10;
rtc->min10reg = (char)(sy->_smin/10);
rtc->min1reg  = (char)(sy->_smin%10);
rtc->hou10reg = (char)(sy->_shrs/10);
rtc->hou1reg  = (char)(sy->_shrs%10);
rtc->yr10reg  = sy->_syrs[0]/10;
rtc->yr1reg   = sy->_syrs[0]%10;
rtc->day10reg = sy->_sday/10;
rtc->day1reg  = sy->_sday%10;
rtc->mon10reg = sy->_smon/10;
rtc->mon1reg  = sy->_smon%10;
rtc->dcontrol = 0;                      /* start clock */
}
```

13.3 Summary of the RTC

Device	RTC 72423
Access Address	$FF803000
Port Width	Byte
Interrupt Request Level	Software programmable
FGA-002A Interrupt Channel	Local IRQ #0

14. SWITCHES AND LED INDICATORS

The IBC-20 board contains two front panel toggle switches, two rotary switches and two slide switches. Four status LEDs and four user LEDs are visible through the front panel.

The two front panel toggle switches provide the RESET/LOCAL and ABORT functions. Both switches are double function switches which have their normal position in the middle. The upper position of the switches activates the function momentarily, while in the down position the function is enabled continuously.

Set the switches to the middle position for proper operation.

A window in the front panel allows access to the 16 position (hexadecimal coded) "MODE" rotary switch. There is also a second on-board switch SW4 (default $F). Firmware reads these two switches and selects the startup conditions of the VMEPROM or a user program. The switches are readable via the CIO unit. For further information, please see the *"IBC-20 Firmware User's Manual"*.

The slide switches configure the hardware functions of the IBC-20 board. These switches are described in chapter II, ***"Default Configuration of the Board."***

The status LEDs indicate the halt/run state of the processor (red/green). The status LEDs also indicate the VME access or main RAM access of the board (yellow).

The user LED group has four yellow indicators (designated "1 2 3 4"). The LEDs are controlled by I/O ports of the CIO device and are used for general status indication.

14.1 The RESET/LOCAL Switch

The RESET/LOCAL toggle switch at the top of the front panel provides a system reset when pushed in the momentary up position (RESET). This resets the MC68020 microprocessor, the FGA-002A and all on-board I/O devices. In addition, the SYSRESET* signal is driven to VME if this is enabled by switch SW5-2.

The down position (LOCAL) of the switch can be enabled permanently. In this position, the IBC-20 board is locally under reset. This means that the processor, the FGA-002A and local hardware is reset and the board is not accessible from VMEbus side. In this state, the board does not generate the SYSFAIL* and SYSRESET* signal. The Slot-1 functions of the board (SYSCLOCK* generation, 4-level bus arbitration) are not affected by the local reset state and work continuously. The local reset function can be used to debug multiprocessor software packages and to disable the board in an application when a failure has occurred but power cannot be switched off.

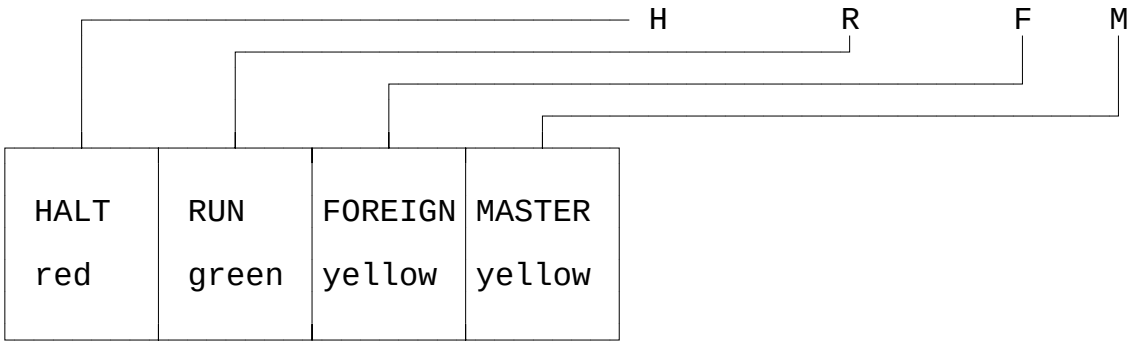
14.2 The ABORT Switch

The ABORT switch function is active when pushed in the momentary up position. When in the down position, the ABORT switch does not have a function during power-up, but this state is readable via the CIO device. Please refer to the chapter *"The Counter/Timer-I/O Unit Z8536 CIO"* for more information.

The ABORT switch forces a non-maskable interrupt to the MC68020 processor. The interrupt level is programmable inside FGA-002A for user applications.

14.3 The STATUS LEDs

The status LED array displays the following functions of the board:



HALT: The red "HALT" LED indicates the RESET/HALT state of the processor. The processor's RESET and HALT signal lines are monitored by the LED control logic and the LED lights up if one or both signals are asserted low. In case of coinciding accesses of the processor to the VMEbus and shared RAM access from VME, the HALT LED may glimmer since the HALT signal line will be asserted to request the processor to relinquish the bus and to retry the current cycle.

RUN: Indicates running state of the processor (reverse of HALT state).

FOREIGN: Indicates access of a foreign master to the shared Main RAM, e.g. the FGA-002A DMA-Controller, a VME master, or an EAGLE module.

MASTER: Indicates that the IBC-20 board is bus master on the VMEbus.

14.4 The MODE Switch

The MODE switch is accessible through the front panel and can be used by systems or applications programmer as a general purpose input channel for setup and test functions.

The sixteen switch positions (hexadecimal coded) are readable via I/O pins PA0-PA3 on port A of the CIO device (Z8536 Counter I/O Unit), with PA0 providing the least significant bit and PA3 the most significant bit of the 4-bit word. Additional information on how the CIO ports are read can be found in chapter *"The Counter/Timer-I/O Unit CIO Z8536"* and the data sheet respectively.

The MODE switch position is read by the boot routine and VMEPROM to setup board parameters and system startup conditions. For detailed information please refer to the *"IBC-20 Firmware User's Manual"*

The switch is set to position $F as default.

14.5 The USER LEDs

The user LEDs have four yellow indicators designated with "1 2 3 4" on the front panel. These LEDs are software controlled and fully at the user's disposal. They may be used to provide general status indication in application or diagnostic software.

The user LEDs are controlled by the CIO device. Please refer to chapter *"The Counter/Timer-I/O Unit CIO Z8536"* for more information.

15. THE RESET STRUCTURE

In this chapter the hardware reset sources and software triggerable reset calls of the board are described. Additional information concerning the reset calls and reset options which are controlled by FGA-002A can be found in the FGA-002A User's Manual, *Section 8, "Miscellaneous"*.

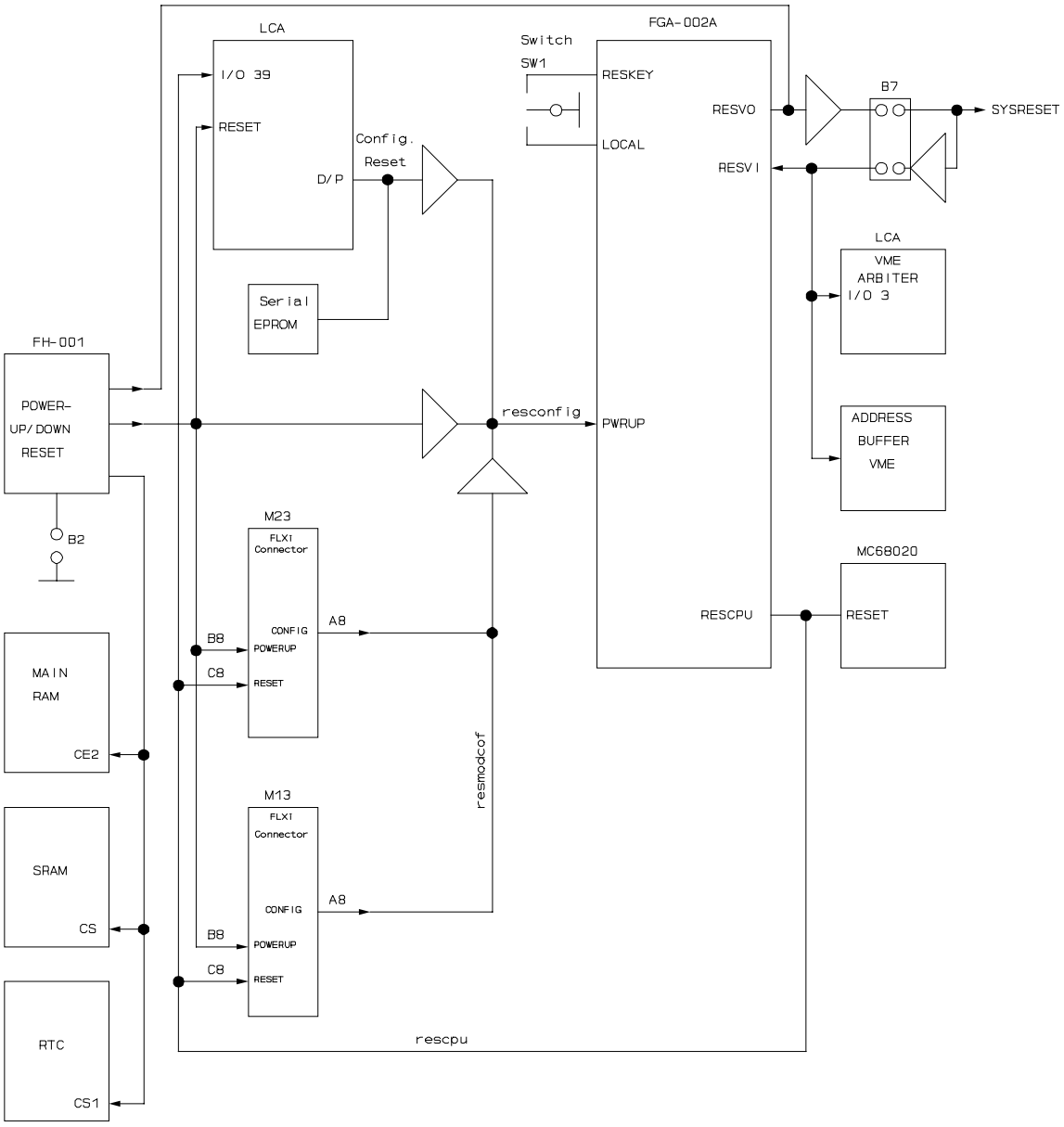
15.1 Power-Up/Down Reset

Power-Up/Down Reset is generated by a power monitor which senses the supply voltage and resets the board if the +5V DC supply voltage is lower than 4.8V.

With Switch SW5-4 the sense voltage of the power monitor can be set to 4.2V DC for test purposes (SW5-4 = OFF). Under normal conditions the sense voltage should be set to 4.8V, that is, when the switch is set to ON.

During power-up and power-down, the processor, the FGA-002A and all I/O devices are reset. SYSRESET* will be generated and driven to VME if this is enabled by the switch SW5-2.

Figure 13: The Reset Structure



15.2 The RESET/LOCAL Function Switch

Please refer to chapter *"SWITCHES AND LED INDICATORS"* in this manual for a description of the RESET/LOCAL switch reset source.

15.3 The Reset Instruction

The RESET instruction of the microprocessor is designed to reset peripherals under program control, without resetting the processor itself. This feature is fully supported by the board. The RESET instruction resets all peripherals on the board but does not reset any registers inside FGA-002A.

A register bit of FGA-002A controls whether the VMEbus signal line SYSRESET* will be driven low as well. A detailed description of this feature is given in Section 8 of the *"FGA-002A User's Manual",* "Processor OPCODE Reset".

15.4 The Local Reset Call

A local Reset Call is executed when the FGA-002A Gate Array is accessed at address $FFD00E00 in a read or write cycle. The Reset Call resets the complete board. The SYSRESET* signal line will be asserted as well.

15.5 The VME Reset Call

The VME reset call feature allows to reset the board by another VMEbus master. The local processor has to enable the reset call by programming a register bit inside FGA-002A. The VME reset call resets all devices on board. The VME signal line SYSRESET* will not be driven. The SYSCLK generation, the 4-level arbiter and the bus arbitration will be left untouched by the VME Reset Call. Please refer to the *"FGA-002A User's Manual"*, Section 8 for further information.

15.6 The VME Signal SYSRESET*

The VMEbus signal SYSRESET* is driven to VME and received from VME only if this is enabled by the switches SW5-2 (drive) and SW5-3 (receive).

If the SYSRESET* signal from VME is detected low, the IBC-20 board will be reset completely, including the 4-Level arbiter. Please refer to chapter *"VME SYSTEM CONTROLLER FUNCTIONS"* for further information.

The SYSRESET* signal is triggered by several onboard reset sources. Detailed information about the generation of SYSRESET* can be found in the description of the onboard reset sources contained in the *"FGA-002A User's manual"*.

16. THE INTERRUPT STRUCTURE OF THE BOARD

The microprocessor on the IBC-20 board can be interrupted by the FGA-002A gate array, the EAGLE slot # 1 and EAGLE slot # 2. The interrupts are prioritized by 7 interrupt levels. EAGLE slots provide the IPL[0-2] signals for interrupts generated by EAGLE modules.

The active low IPL[0-2] signals encode seven interrupt levels which are evaluated by the processor as follows:

IPL[2-0]	Interrupt Level	Priority
HHH	No interrupt condition	
HHL	Level 1	Lowest
HLH	Level 2	
HLL	Level 3	
LHH	Level 4	
LHL	Level 5	
LLH	Level 6	
LLL	Level 7	Highest

Interrupts are acknowledged by the processor according to their priority. Interrupts which use the same interrupt level are scheduled by the local Interrupt Acknowledge (IACK) daisy chain according to the interrupt's position within the chain. The IACK daisy chain begins at EAGLE slot #2 and propagates to EAGLE slot #1. After leaving this slot, the daisy chain ends at the FGA-002A gate array.

EAGLE modules participate on the IACK daisy chain if it asserts the "MODINS" pin low. The daisy chain also allows cascading interrupters on the EAGLE module (such as the FORCE COMPUTERS' gate array FC68165) and ensures that only one interrupter responds to the IACK cycle of the processor.

16.1 The On-Board Interrupt Sources

The on-board interrupt sources of the IBC-20 base board generally use the FGA-002A gate array to request service from the local processor.

The interrupt sources are FGA-002A internal sources, the VMEbus interrupts and interrupts from the local I/O devices RTC, CIO and SCC, and from the battery backup circuitry.

The interrupt management of FGA-002A allows software to select any interrupt level for each source. The gate array can provide the interrupt vector by either using an internal vector number or fetch the vector from the external interrupting device.

Interrupts of the local I/O devices are handled by the local interrupt channels LIRQ0-LIRQ7 of the FGA-002A gate array.

The CIO port interrupt and the SCC interrupt is supported by FGA-002A in that it is selectable if the vector either is generated internally from the assigned channel or will be fetched from the external interrupting device. Both options are programmable inside the gate array.

When a VMEbus interrupt is acknowledged by FGA-002A, the vector will always be fetched from the VMEbus interrupter.

The table below shows the assignment of the SCC-, CIO-, RTC- and Battery Alarm-interrupts to the local interrupt channels of the FGA-002A gate array.

A complete description of the interrupt handling capabilities of the gate array is given in the *FGA-002 User's Manual*.

FGA-002 Interrupt Channel	Device	Device Vector
LIRQ0	RTC	no
LIRQ1	Battery ALARM 1	no
LIRQ2	CIO Timer #3	yes
LIRQ3	CIO Timer #2	yes
LIRQ4	CIO Port	yes
LIRQ5	SCC	yes
LIRQ6	Battery ALARM 2	no
LIRQ7	---	---

17. BUS ARBITRATION OF THE FLXibus

The following devices may become bus master of the local FLXibus:

- EAGLE Slot #2
- EAGLE Slot #1
- FGA-002A Gate Array
- MC68020 microprocessor

The mastership of the local FLXibus is managed by the bus control unit inside the MC68020 microprocessor. The bus controller arbitrates the local bus in such a way that the processor itself has lowest priority in becoming bus master.

On request of an alternate master (e.g. EAGLE Module), the processor will grant the bus to the alternate device immediately. This is normally when the BR signal has been recognized asserted by the 68020. After synchronization of the BR signal, the BG signal will go active.

A local BGIN/BGOUT daisy chain prioritizes the bus requests of alternate masters on the IBC-20 board.

The FGA-002A requests mastership of the FLXibus if a VMEbus master wants to access the onboard Main memory or if the DMA controller addresses the Main RAM or the EAGLE module address range.

The order of the FLXibus mastership priority, which is given through the arbitration daisy chain, is as follows:

Device	**Priority**
EAGLE Slot #2	1st (highest) priority
EAGLE Slot #1	2nd priority
FGA-002A Gate Array	3rd priority
MC68020 microprocessor	4th (lowest) priority

18. THE VME MASTER INTERFACE

The IBC-20 board supports 8, 16, and 32 bit data transfers on the VMEbus. The 32-bit addressing capability and support of extended, standard, and short I/O address modifier codes allows the user to interface to a wide range of VMEbus products. Unaligned transfers and Read-Modify-Write cycles are fully supported. Several bus release functions are implemented for multiprocessor applications.

18.1 The VME Address Space

The VME address space of the board is decoded by the FGA-002A Gate Array. Depending on the Main memory size, which is assembled on the board, the VME address space will be decoded in the area which follows the Main memory.

The VME address space is split into several ranges. The ranges determine the data bus size and the address lines which are used for the transfer.

Two ranges have assigned a fixed data bus size of 16 bit. The transfer size of the remaining areas is selectable to 16 bits (D16) or 32 bits (D32). The selection is made by a control bit in the FGA-002A gate array. (See FGA-002A Users Manual under VME Interface, "D16 Master Option").

The data bus size can be modified by the "MEM" command of VMEPROM. In addition, VMEPROM uses the setup of the front panel "MODE" switch to set the data bus size.

By default, the data bus size is set to 32 bits (D32).

The following table lists the VMEbus ranges with their data bus sizes and addressing capability for VME accesses of the processor or alternate FLXibus masters.

Note: The addressing capabilities which are given for the decoded VMEbus ranges are not effective for the DMA controller of FGA-002A. Please refer to the *"FGA-002 User's Manual"*, Section "The 32-Bit DMA Controller".

Table 20: VME Address Ranges

Address Range		Addressing Capability	Data Bus Size 32/16 Bit
From	To		
(See Note 1)	FAFF FFFF	A32	Selectable 32 or 16 bit
FB00 0000	FBF3 FFFF	A24	
FBFF 0000	FBFF FFFF	A16	
FC00 0000	FCFE FFFF	A24	Fixed to 16 bit
FCFF 0000	FCFF FFFF	A16	

Note 1:
The boundary between the Main memory and the VME address range is set automatically with the Main memory size. The VME address space follows behind the Main memory decoding.

Table 21: VME Data Bus Usage with Bus Size D32

Transfer Type	D31-D24	D23-D16	D14-D8	D7-D0
Byte				x
Byte			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Word		x	x	
Unaligned Long Word A		x	x	
Unaligned Long Word B	x	x	x	x
RMW Byte				x
RMW Byte			x	x
RMW Word			x	x
RMW Long Word	x	x	x	x
RMW = Read Modify Write				

Table 22: VME Data Bus Usage with Bus Size D16

Transfer Type	D31-D24	D23-D16	D14-D8	D7-D0
Byte Byte			 x	x
Word			x	x
RMW Byte				x
RMW Byte			x	
RMW Word			x	x
RMW = Read Modify Write				

19. SUPPORTED AM CODES

The IBC-20 board supports AM codes for supervisor/user and program/data access within the Extended and Standard VME Addressing Ranges. In the short Addressing Range, only AM-Codes for Data Access are being used.

The AM code which is generated when the processor addresses the VME space depends on the VME address and the processor's address space type.

The AM codes for extended, standard or short addressing will be generated in different VME address ranges of the board.

The processor's function code signal lines define the address space type of the current bus cycle. This determines whether the VME access is a supervisor/non-privileged program or data access.

Note: The DMA controller of FGA-002A supports any AM code in the whole VME address space, since the AM code generation is under control of software.

The next table shows the VME address map and the supported AM Codes.

Table 23: Supported AM-Codes as VME Master

Address Range		Addressing Capability	Function	AM Code	Data Bus Size
From	To				
(See Note 1)	FAFF FFFF	Extended (A32)	SPA SDA NPA NDA	0E 0D 0A 09	32/16 bit
FB00 0000	FBFE FFFF	Standard (A24)	SPA SDA NPA NDA	3E 3D 3A 39	
FBFF 0000	FBFF FFFF	Short (A16)	SDA NDA	2D 29	
FC00 0000	FCFE FFFF	Standard (A24)	SPA SDA NPA NDA	3E 3D 3A 39	16 bit
FCFF 0000	FCFF FFFF	Short (A16)	SDA NDA	2D 29	

SPA = Supervisor Program Access
SDA = Supervisor Data Access
NPA = Nonprivileged Program Access
NDA = Nonprivileged Data Access

The Address Modifier (AM) Codes specified by VME are listed in table 12. The AM codes supported by the IBC-20 are marked with an asterisk (*).

Table 24: VME Address Modifier Codes

HEX Code	Address Modifier						Function
	5	4	3	2	1	0	
3F	H	H	H	H	H	H	Standard Supervisory Block Transfer
3E*	H	H	H	H	H	L	Standard Supervisory Program Access
3D*	H	H	H	H	L	H	Standard Supervisory Data Access
3C	H	H	H	H	L	L	Reserved
3B	H	H	H	L	H	H	Standard Nonprivileged Block Transfer
3A*	H	H	H	L	H	L	Standard Nonprivileged Program Access
39*	H	H	H	L	L	H	Standard Nonprivileged Data Access
38	H	H	H	L	L	L	Reserved
37	H	H	L	H	H	H	Reserved
36	H	H	L	H	H	L	Reserved
35	H	H	L	H	L	H	Reserved
34	H	H	L	H	L	L	Reserved
33	H	H	L	L	H	H	Reserved
32	H	H	L	L	H	L	Reserved
31	H	H	L	L	L	H	Reserved
30	H	H	L	L	L	L	Reserved
2F	H	L	H	H	H	H	Reserved
2E	H	L	H	H	H	L	Reserved
2D*	H	L	H	H	L	H	Short Supervisory Access
2C	H	L	H	H	L	L	Reserved
2B	H	L	H	L	H	H	Reserved
2A	H	L	H	L	H	L	Reserved
29*	H	L	H	L	L	H	Short Nonprivileged Access
28	H	L	H	L	L	L	Reserved
27	H	L	L	H	H	H	Reserved
26	H	L	L	H	H	L	Reserved
25	H	L	L	H	L	H	Reserved
24	H	L	L	H	L	L	Reserved
23	H	L	L	L	H	H	Reserved
22	H	L	L	L	H	L	Reserved
21	H	L	L	L	L	H	Reserved
20	H	L	L	L	L	L	Reserved

L = low signal level H = high signal level

The VME Address Modifier Codes (cont'd)

HEX Code	Address Modifier						Function
	5	4	3	2	1	0	
1F	L	H	H	H	H	H	User Defined
1E	L	H	H	H	H	L	User Defined
1D	L	H	H	H	L	H	User Defined
1C	L	H	H	H	L	L	User Defined
1B	L	H	H	L	H	H	User Defined
1A	L	H	H	L	H	L	User Defined
19	L	H	H	L	L	H	User Defined
18	L	H	H	L	L	L	User Defined
17	L	H	L	H	H	H	User Defined
16	L	H	L	H	H	L	User Defined
15	L	H	L	H	L	H	User Defined
14	L	H	L	H	L	L	User Defined
13	L	H	L	L	H	H	User Defined
12	L	H	L	L	H	L	User Defined
11	L	H	L	L	L	H	User Defined
10	L	H	L	L	L	L	User Defined
0F	L	L	H	H	H	H	Extended Supervisory Block Transfer
0E*	L	L	H	H	H	L	Extended Supervisory Program Access
0D*	L	L	H	H	L	H	Extended Supervisory Data Access
0C	L	L	H	H	L	L	Reserved
0B	L	L	H	L	H	H	Extended Nonprivileged Block Transfer
0A*	L	L	H	L	H	L	Extended Nonprivileged Program Access
09*	L	L	H	L	L	H	Extended Nonprivileged Data Access
08	L	L	H	L	L	L	Reserved
07	L	L	L	H	H	H	Reserved
06	L	L	L	H	H	L	Reserved
05	L	L	L	H	L	H	Reserved
04	L	L	L	H	L	L	Reserved
03	L	L	L	L	H	H	Reserved
02	L	L	L	L	H	L	Reserved
01	L	L	L	L	L	H	Reserved
00	L	L	L	L	L	L	Reserved

L = low signal level H = high signal level

20. THE VME SLAVE INTERFACE

The slave interface of the IBC-20 board allows access from VME to the Shared Main RAM and to several FGA-002A functions, such as the FORCE Message Broadcast (FMB), Mailbox Interrupts and Status Report Registers.

Table 25 shows the AM codes which are demanded to access the IBC-20 board from VME. A description of the FORCE Message Broadcast concept (FMB), the Mailboxes, the Reset call and the SYSFAIL/HALT status-report readout can be found in section "CPU and VME Interface" of the *FGA-002A User's Manual.*

The slave access to the IBC-20 board can be enabled/disabled inside FGA-002A by software. Individual selection of the supported AM codes is provided.

Table 25: Supported AM-Codes for Slave Access

Access to	Addressing Capability	AM Code	Function
Shared Main Memory	Extended (A32:D32,D16,D8)	0E 0D 0A 09	SPA SDA NPA NDA
	Standard (A24:D32,D16,D8)	3E 3D 3A 39	SPA SDA NPA NDA
FMB	Extended (A32:D32)	0E 09	SDA NDA
Mailbox	Short (A16:D8)	2D 29	SDA NDA
SYSFAIL & HALT State Reset Call	Short (A16:D8)	2D 29	SDA NDA

SPA = Supervisor Program Access
SDA = Supervisor Data Access
NPA = Nonprivileged Program Access
NDA = Nonprivileged Program Access

20.1 Access to the Shared Main Memory

The shared main memory is accessible with 32/16 and 8-bit wide data. Unaligned transfers (UAT) and Read-Modify-Write (RMW) cycles are fully supported.

Both the access address window and the supported AM Codes are selectable by registers in the FGA-002A chip. The address window to the Shared Main RAM is programmable in 4-Kbyte steps. The RAM can be made write protected.

The registers are programmed by the local firmware.

By default, the VME address of the main memory is set to **$8000 0000** and the complete memory is accessible in the extended addressing mode with the following AM Codes:

HEX Code	Address Modifier						Function
	5	4	3	2	1	0	
0D	L	L	H	H	L	H	Extended Supervisory Data Access
09	L	L	H	L	L	H	Extended User Data Access

L = low signal level H = high signal level

20.2 RAM Access with Extended Addressing AM Code

The shared main memory of the CPU board is accessible with AM codes for Extended Addressing (A32). The AM Code register and the address range registers inside FGA-002A must be programmed accordingly to allow the access.

The AM Code register determines the AM Code which is to be sent by the accessing master. AM Codes for the supervisor/user mode and for program/data access can be selected individual. Read and read/write permission can be selected for each AM Code.

Table 26 shows the AM Codes which can be used for accesses to the Main memory in the extended address mode. Details for the programming of the AM Code register can be found in the *FGA-002A User's Manual* in the section entitled "CPU and VME Interface".

Table 26: Valid Extended Addressing AM Codes

HEX Code	Address Modifier						Function
0E	L	L	H	H	H	L	Extended Supervisor Program Access
0D	L	L	H	H	L	H	Extended Supervisor Data Access
0A	L	L	H	L	H	L	Extended User Program Access
09	L	L	H	L	L	H	Extended User Data Access

20.3 RAM Access with Standard Addressing AM Code

The IBC-20 supports accesses from VME to the Main memory with standard addressing AM codes. This allows VME masters with A24 addressing capability to access the Main RAM. The A24 standard addressing mode has to be enabled by the local software before the access from VME can be performed.

Accesses using the A24 AM-code require the local software to take the actions, which are described in the following chapters:

- The A24 register must be programmed to contain the upper address byte of the Main RAM's extended VME address.

- The A24 mode Control pin must enable the access.

If the A24 mode is enabled, access to the shared memory can be performed not only with standard AM codes but also with extended AM codes. The type of valid AM codes (Supervisor/User, Program/Data) are to be selected by the AM code register of FGA-002A.

The following table shows the AM codes supported in the A24 addressing mode setup.

Table 27: Valid AM Codes with the A24 Mode

HEX Code	Address Modifier						Function
3E	H	H	H	H	H	L	Standard Supervisor Program Access
3D	H	H	H	H	L	H	Standard Supervisor Data Access
3A	H	H	H	L	H	L	Standard User Program Access
39	H	H	H	L	L	H	Standard User Data Access
OE	L	L	H	H	H	L	Extended Supervisor Program Access
OD	L	L	H	H	L	H	Extended Supervisor Data Access
OA	L	L	H	L	H	L	Extended User Program Access
O9	L	L	H	L	L	H	Extended User Data Access

20.4 Programming the A24 Register

The A24 register on the IBC-20 board is utilized to complete the 24-bit address of a VME Standard access to a 32-bit address. This is required because the FGA-002A always uses 32-bit addresses to decode an access cycle from VME to the Shared RAM.

In order that the FGA-002A recognizes the VME access as valid, the A24 register must contain the value which corresponds to the upper address byte (A24-A31) of the Main RAM's Extended VME access address (32-bit address).

The register is programmed by the local firmware to the default value $80.

The bits D0-D7 of the A24 register correspond to the address bits A24-A31 of the 32-bit longword address.

The byte wide A24 register is accessible at $FF803E10. It is not readable and will not be cleared by reset.

A24 Register Summary:

Access address: $FF803E10
Port Width: Byte
Access mode: Write

20.5 Enabling the A24 Mode

The A24 access mode is controlled by an I/O pin of the CIO device Z8536 (J70). The I/O pin (device pin #15) corresponds to Bit 5 of Port B (PB5).

To **enable** the A24 addressing mode, the PB5 I/O must pin drive **low level**.

Programming the I/O ports of the CIO device can be found in chapter *"The Counter/Timer-I/O Unit CIO Z8536"*.

Since the CIO device features programmable port polarity, please refer to the data sheet of the Z8536 for writing the port control and data registers with the proper values.

By default, A24 access mode is disabled.

21. THE VME INTERRUPTER

The VMEbus Interrupter function allows the IBC-20 board to generate interrupts to the VMEbus on any level of IRQ1-7. The interrupt generation is fully under software control. The interrupt vector is programmable. The Interrupter operates with D08(O) capability, providing the interrupt vector at the VME data lines D00-D07. The VMEbus Interrupter function is contained in the LCA device and has associated two read/writable 8-bit registers, the Interrupt Generation Register IRQGEN and the Interrupt Vector Register IRQVEC. The IRQGEN is used to generate the VMEbus interrupt. The IRQVEC register contains the interrupt vector.

Table 28: VMEbus Interrupter Registers

Address HEX	Label	Default Value	Mode	Description
FF803E00	IRQGEN	01	R/W	Interrupt Generation Reg.
FF803E01	IRQVEC	--	R/W	Interrupt Vector Register

21.1 The Interrupt Generation Register IRQGEN

This register controls the generation of VME interrupts by the IBC-20 board. Bits 1-7 of the Interrupt Generation register are assigned the VME interrupt levels IRQ 1-7 accordingly. Bit 0 of the register is not present since there is no interrupt level #0 defined by VME. This bit can be written but always returns "1" if the register is read.

A VMEbus interrupt will be generated when the corresponding register bit is logical "1". The interrupt will be cleared automatically by the interrupt acknowledge cycle, which resets the register bit to "0".

The following table shows the format of the register.

Table 29: Interrupt Generation Register Format

	Register Bits							
	7	6	5	4	3	2	1	0
VME Interrupt	#7	#6	#5	#4	#3	#2	#1	--

Bits 7-1	Function
0	VMEbus interrupt is inactive
1	VMEbus interrupt is active

21.2 The Interrupt Vector Register IRQVEC

The Interrupt Vector Register holds the byte wide interrupt vector which is returned to the VMEbus in an interrupt acknowledge cycle. The register must be written with the proper vector before the interrupt is made active on VME by the IRQGEN register. The register is read/writable. Its content must not be altered until the pending interrupt has been serviced.

The Interrupt Vector Register is cleared only after powerup to $00.

22. THE VME INTERRUPT HANDLER

The IBC-20 board provides the Interrupt Handler with "IH7-1" capability, receiving and servicing all VMEbus interrupt levels. It behaves as a D08(O) interrupt handler, reading the byte wide interrupt status/ID from data lines D00-D07.

The seven interrupt request lines of VME (IRQ1-7) are routed to the FGA-002A gate array. It controls the interrupt levels which may be enabled or disabled separately.

The complete VMEbus interrupt management is done inside FGA-002A. Please refer to the *"FGA-002A User's Manuals"* for a detailed description of the programming of the interrupt management functions.

Each VMEbus interrupt can be mapped to any interrupt level for the local processor. So for example a VMEbus interrupt request on level #2 can be mapped to cause an interrupt request on level 5 to the processor.

NOTE: The IBC-20 board only supports interrupters with a byte interrupt vector. This capability is implemented on most of the existing boards because the VMEbus Specification Rev. A and B do not include a word or long word interrupt vector. Therefore, older VMEbus boards should be useable together with this board.

23. VMEbus SYSTEM CONTROL FUNCTIONS

The IBC-20 board provides all functions of a VMEbus system controller.

This includes the SYSCLK generation, VMEbus Arbiter, IACK Daisy Chain Driver, SYSRESET generation, Bus Timeout Counter and support for the VMEbus signals ACFAIL* and SYSFAIL*.

The VMEbus signals ACFAIL* and SYSFAIL* can generate interrupts to the local processor. Both signals use dedicated interrupt channels within FGA-002A.

The SYSRESET* signal is driven to and received from the VMEbus. For test purposes, both functions can be disabled individually by the switches SW5-2 and SW5-3.

A single switch SW5-8 configures the board as system controller. When switched ON, the BCLR* and SYSCLK signals are driven. The 4-level arbiter is enabled and may assert BCLR* depending on the arbitration mode. These functions are called "Slot 1" functions and must be enabled only if the board resides in the first slot of a VMEbus environment. By default, Switch SW5-8 is set ON and enables the Slot #1 functions.

NOTE

Only that board which is located in slot 1 of a VMEbus environment is permitted to drive the SYSCLK signal and the BCLR* signal.

23.1 The SYSCLK Signal

The SYSCLK signal is a continuous 16 MHz signal with a 50/50 high/low cycle. The SYSCLK signal is driven to the VMEbus when the Slot 1 system controller functions are enabled by switch SW5-8.

23.2 The SYSRESET* Signal

The IBC-20 board drives and receives the VMEbus SYSRESET* signal by default. For test purposes, both functions can be disabled individually by the switches SW5-2 and SW5-3. Setting the switches "ON" enables the functions (default). The SYSRESET* signal will be asserted low for a minimum of 220 ms, providing a VME compatible reset period.

A location diagram showing slide switch SW5 is found in Figure 14 on page 4-67.

23.3 The SYSFAIL* Signal

The SYSFAIL* signal is driven to and received from the VMEbus.

The assertion of the SYSFAIL* signal by the IBC-20 board is controlled with register bits in the FGA-002A gate array. These register bits allow software to select under which conditions the SYSFAIL* signal is asserted.

By default, the firmware initializes the register bits so that the IBC-20 board asserts the SYSFAIL* signal after any reset and releases the signal after the selftest is complete.

The timer/counter of FGA-002A is usable as watchdog timer, which is programmable to trigger the SYSFAIL* signal on VME. Please refer to the description of the timer in the *"FGA-002A User's Manual"*.

NOTE

SYSFAIL* will not be asserted by the board if the RESET/LOCAL function switch is in the LOCAL position (down).

The SYSFAIL* signal is received from the VMEbus to indicate a system failure to the local processor. Receiving the SYSFAIL* signal asserted, allows interrupting the local processor.

The SYSFAIL* signal is assigned an individual interrupt channel of FGA-002A.
The interrupt level is software programmable by FGA-002A registers and allows selecting any interrupt priority for the SYSFAIL* interrupt.

The features provided for the control of the SYSFAIL* signal are described in detail in the FGA-002A User's Manual, *Chapter 8, "MISCELLANEOUS"*.

The following registers are involved:

FGA-002A Register	Address	Bit	Bit Name
CTL8	$FFD00278	3 2	BSYSBIT SSYSBIT
SPECIAL	$FFD00420	7	-

23.4 The ACFAIL* Signal

The ACFAIL* signal is monitored by the board and may interrupt the local processor on a programmable level. The corresponding interrupt channel inside FGA-002A has to be enabled to use this feature. Please refer to the *"FGA-002A User's Manual"*, Section 3, "Interrupt Management" for details.

23.5 The IACK Daisy Chain Driver

Required by the VMEbus specification as a basic slot 1 function, the IACK daisy chain driver completes the system controller functions of the IBC-20 board. The IACK daisy chain driver module is part of the VME Interrupter logic, which is realized in the LCA device. This logic generates a timed IACKOUT signal to the VMEbus.

Because of the VMEbus Interrupter, which is provided by the board, the IACK daisy chain driver is always in function.

24. THE 4-LEVEL VMEbus ARBITER

The 4-Level Arbiter on the IBC-20 board is provided in addition to the single level arbiter, which is contained in the FGA-002A gate array. The single level arbiter of FGA-002A is not usable and **must not** be enabled in any case. Single level arbitration is supported as a subset of the 4-level arbitration algorithms.

The 4-level VMEbus arbiter supports three arbitration modes which are selectable by software.
The arbitration modes are:

- Prioritized Arbitration
- Round Robin Arbitration
- Prioritized Round Robin Arbitration

24.1 Enabling/Disabling the Arbiter

The 4-level Bus Arbiter is enabled when switch SW5-8 is set ON (default). This switch is named "SLOT1" and enables the slot 1 functions of the board (see also "VME SYSTEM CONTROLLER FUNCTIONS").

The setting of switch SW5-8 is readable by software in the Arbiter Control Register ARBCON ($FF803E02). Data Bit 6 reflects the state of the switch. Logical 0 is returned when the switch is ON, OFF returns logical 1.

For detailed information please refer to chapter *"The Logic Cell Array LCA"*. The VMEPROM command "ARB" uses this register bit to display the enabled/disabled state of the 4-level arbiter.

A location diagram showing slide switch SW5 is found in Figure 14 on page 4-68.

NOTE: The VMEbus specification requires an arbiter to be installed at slot 1 of a VME rack. This board is configured with the 4-level arbiter ***enabled*** by default. Therefore, the board has to be installed in slot 1 of the VME rack. Otherwise, the 4-level arbiter must be disabled and an external arbiter has to be used.

24.2 The Arbitration Modes

The 4-level Bus Arbiter provides three modes of arbitration:

1. Prioritized Arbitration Mode
2. Round-Robin Arbitration Mode
3. Prioritized Round-Robin Arbitration Mode

The arbitration modes are selectable by software, using two bits in the ARBCON register. Detailed information is given in the chapter "Arbitration Control Register".

After reset, the Prioritized algorithm is selected. This mode is set up by default from the boot software.

24.2.1 Prioritized Arbitration Mode

An arbitration algorithm suggested by the VMEbus specification is the prioritized arbitration mode. This mode schedules the bus requests in the following sequence:

BR3* has priority over BR2*, BR1*, BR0*
BR2* has priority over BR1*, BR0*
BR1* has priority over BR0*.

If a pending bus request has higher priority than the current bus master, then the arbiter asserts the bus clear signal BCLR*, which demands the current master to release the bus. Please also refer to the chapter *"Bus Clear Generation"*.

24.2.2 Round-Robin Arbitration Mode

If this type of arbitration is selected, all bus request levels appear to be of equal priority. The BCLR* signal will not be generated.

24.2.3 Prioritized Round-Robin Arbitration Mode

The Prioritized Round-Robin arbitration mode schedules bus requests in the following way:

BR3* has priority over BR2*, BR1* and BR0*
BR2*, BR1* and BR0* have equal priority and are arbitrated according to the round robin algorithm.

If there is a Bus Request pending on BR3* while the bus is in use by another master, the arbiter asserts the BCLR* signal.

This mode should only be used with one master requesting the bus with request level BR3*.

24.3 Bus Clear Generation (BCLR*)

The BCLR* signal line of the VMEbus is provided as a means to demand the current bus master to relinquish the bus.

The BCLR* signal is generated by the 4-level arbiter module. Depending on the selected arbitration mode, the arbiter generates BCLR* if a higher prioritized bus request level than the one currently acknowledged is pending.

A high current driver (64mA) drives the BCLR* signal to the VMEbus.

The BCLR* driver is in tristate, when the arbiter is disabled by the "Slot 1" function switch SW5-8.

Note: In spite of the active BCLR* signal, the bus masters release the mastership only at their own discretion.

25. VMEbus REQUEST and RELEASE

25.1 VMEbus Request Level

The IBC-20 board can be configured to request the VMEbus mastership at any of the four bus request levels BR0-BR3. The request level is selectable by hardware or by software.

Software selection of the bus request level is made in the ARBCON register, which is contained in the Logic Cell Array. Please refer to chapter *"The Logic Cell Array LCA"* for detailed information.

The slide switches SW5-7 and SW5-6 select the bus request level by hardware. By default, both switches are set ON which selects the request level BR3 for the board. On the following page, Figure 14 shows the location diagram of slide switches SW5 and SW6.

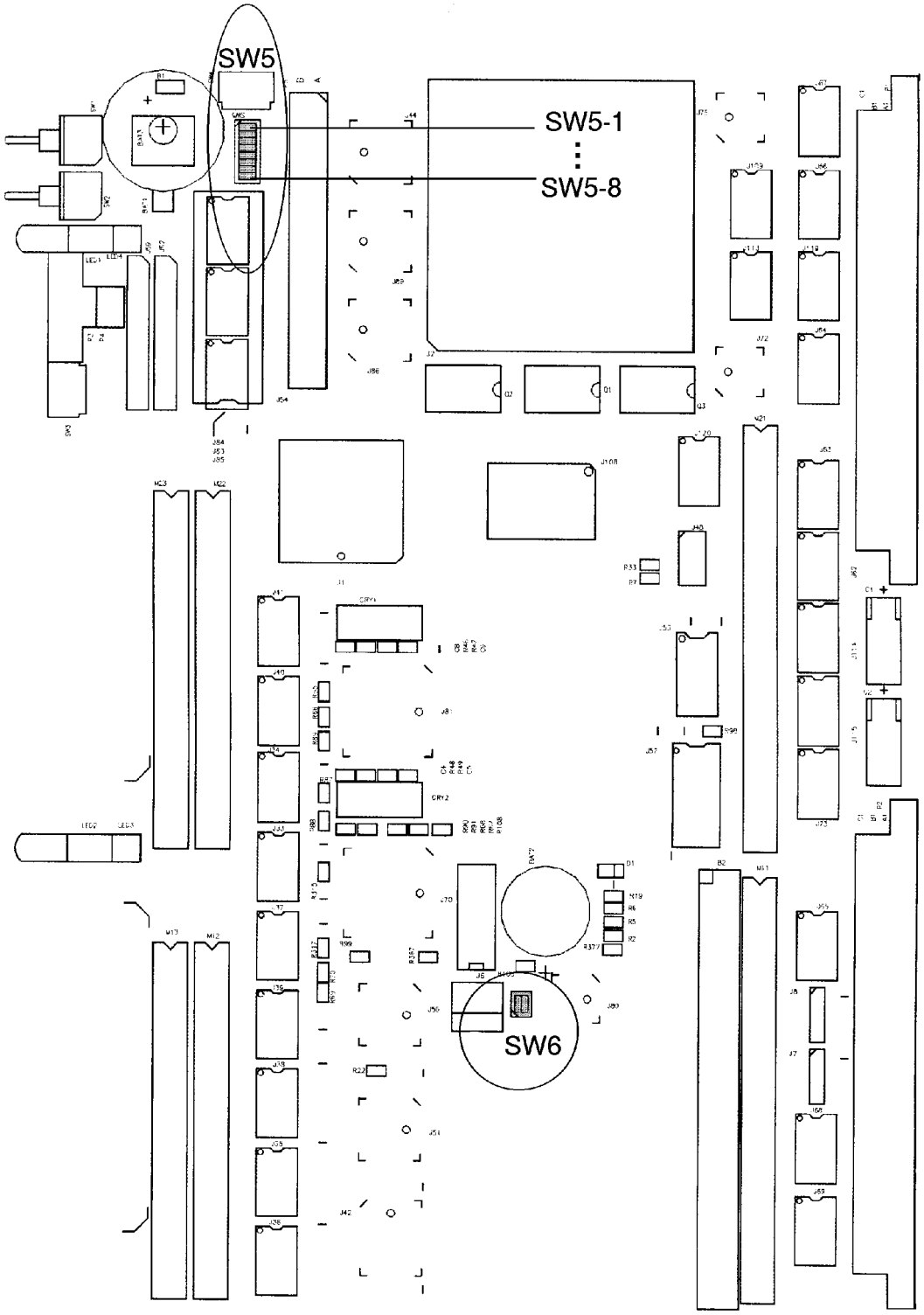
NOTE

The Bus Grant daisy chain which corresponds to the selected bus request level is selected automatically. The remaining bus grant daisy chain passes through the board via onboard logic. Therefore, remove all bus grant daisy chain jumpers which are installed on the backplane for the used VME slot because they will interfere.

A special option, called the FAIR Request Option, is selectable by a register bit of the FGA-002A Gate Array. Please refer to the *"FGA-002A User's Manual"*, Section No. 2 entitled "CPU and VME Interface", where this feature is described.

The VMEPROM command "ARB" allows the user to enable/disable the FAIR request option. Please refer to the *"IBC-20 Firmware User's Manual"*.

Figure 14: Location Diagram of Slide Switches SW5 and SW6



25.2 VMEbus Release

The IBC-20 board contains software selectable options for the release of the VMEbus mastership.

Easy handling and usage of the bus release functions is provided through the FGA-002A Gate Array.

VMEPROM allows the user to change the release function through the "ARB" command. Please refer to the *"IBC-20 Firmware User's Manual"* for details.

The ROR, RAT, RBCLR and FAIR release modes are enabled by default.

The release modes are described in the following sections.

25.3 Release Every Cycle (REC)

The REC mode causes the board to release the VMEbus mastership after the initiated transfer cycle has been completed.

If the REC mode is enabled, all other bus release functions will be ignored.

The programming of the REC mode is described in the FGA-002A Gate Array Manual, *Section 2 "CPU and VME Interface"*.

By default, the REC option is disabled.

25.4 Release on Request (ROR)

The ROR mode demands the IBC-20 board to release the bus mastership if there is a bus request pending by another master. Any bus request level is monitored and will be considered.

The bus will be relinquished with a delay (release inhibit time). This guarantees the board a minimum amount of time being VMEbus master.

The delay can be selected by a register of FGA-002A.

Please refer to the *"FGA-002A Gate Array Manual"*, Section No. 2 "CPU and VME Interface".
The ROR mode cannot be disabled.

By default, the release inhibit time is 0.5 µs.

25.5 Release Voluntary (RV)

A timer with a fixed clock rate is installed on the FGA-002A gate array to provide for voluntary release of VMEbus mastership. This function cannot be disabled.

The Release Voluntary function is described in the FGA-002A Gate Array Manual.

25.6 Release on Bus Clear (RBCLR)

The RBCLR function allows release of bus mastership if an arbiter asserts the BCLR* signal of the VMEbus. This function overrides the ROR function timing limitations.

The RBCLR mode is described in the FGA-002A Gate Array Manual.

By default, the Boot Software selects the RBCLR mode.

25.7 Release on ACFAIL (RACFAIL)

The RACFAIL feature is implemented in the FGA-002A Gate Array. By default, this release option is enabled and the board releases the VMEbus in case the ACFAIL* signal line is detected low.

The RACFAIL option will be disabled if the board is initialized to be the ACFAIL handler.

More information about the RACFAIL option and the ACFAIL handler can be found in the FGA-002A User's Manual, *Section No. 2 "CPU and VME Interface"*, and *Section No. 8* "*Miscellaneous*".

26. THE BATTERY BACKUP FACILITIES

26.1 General

The IBC-20 board features battery backup for the 32 Kbyte Local SRAM and the Real Time Clock (RTC). The backup power is provided by two onboard batteries (primary and secondary battery), or the backup power may be supplied by the VMEbus STDBY line.

The primary battery is installed in a battery holder and is easily replaceable in the field. The secondary battery is an on-board soldered NiCd Accumulator, which is charged when the board is under power. During replacement of the primary battery, the secondary battery supplies the backup power for the SRAM and the RTC so that the data is saved. If the primary battery is insufficiently charged, a two-level alarm interrupt is provided to indicate the need for a battery replacement.

26.2 Functional Description

The power for the SRAM and RTC is controlled by a battery backup circuitry, which switches between the +5V system power or the battery power. The circuitry switches from the system power to battery power if the system voltage decreases under 4.85V. In this case, either the primary battery or the secondary battery is selected for backup, whichever has the higher voltage level.

The primary battery is used as the main source for the backup power. The voltage level of the primary battery is observed by the battery backup circuitry. Two detection levels are specified to indicate a low voltage condition of the primary battery. At each detection level, one of the alarm outputs goes low and initiates an alarm interrupt.

The first low voltage detection level (2.55V min.) indicates that the primary battery should be replaced, but the voltage is still sufficient for saving the data. If the second low voltage detection level (2.27V min.) is reached, saving data is no longer guaranteed.

As secondary battery, the on-board soldered NiCd Accumulator is used. The accumulator is enabled when the switches of SW6 are set "ON". In this case, the accumulator will be charged by the backup circuitry when the board is under power. Instead of the accumulator, the "STDBY" VME-line can be used to backup the SRAM and RTC data.

Note

When using the VMEbus "STDBY" line to save data, the accumulator **must** be protected from being charged by the STDBY voltage. This is achieved by switching both parts of switch SW6 to the OFF position, which disconnects the accumulator from the logic.

26.3 Low Voltage Alarm Interrupt

The IBC-20 revision 2 provides two alarm interrupts which indicate when the charge condition of the primary battery is insufficient for a safe battery backup of the local SRAM and the RTC.

The charge condition of the primary battery is observed by the battery backup circuitry. This circuitry provides two alarm outputs which are asserted low when the battery voltage drops under a specified level.

The first detection level is at 2.55V and triggers the Alarm1 output. The second detection level is at 2.27V and triggers the Alarm2 output. The alarm outputs are connected to local interrupt channels of FGA-002A to indicate this fault condition.

The following table shows which FGA-002A interrupt channels are used for the Alarm interrupts.

Interrupt	Voltage Level	FGA-002A Interrupt Channel
Alarm1	2.55V	LOCAL #1
Alarm2	2.27V	LOCAL #6

26.4 Primary Battery Backup

As primary battery, a 3V Li-Mn button cell battery type CR2032 is used. The battery is installable in a battery holder which allows easy replacement in the field. Under normal storage and operating conditions (0-50°C), the battery provides a backup time of about 1.5 years.

In order to avoid discharge of the primary battery during shipment, the primary battery is not installed by default.

26.5 Primary Battery Insertion

The battery is inserted correctly into the battery holder when the "+" terminal faces down on the printed circuit board and the "-" terminal is visible.

If the battery is installed incorrectly, there is neither data loss nor damage to the battery logic. In this case, the second battery (NiCd Accumulator) is backing up the data of the SRAM and RTC, but when the board is powered up, both alarm interrupts will be active.

Primary Battery	
Battery Type:	CR2032 (Li-Mn)
Voltage:	3V
Capacity:	180 mAh

26.6 Secondary Battery Backup

The NiCd Accumulator is provided as a secondary backup medium, which supplies power to the local SRAM and the RTC if the primary battery must be replaced. The accumulator is enabled if both SW6 switches (SW6-1 and SW6-2) are in the "ON" position (default). When enabled, the accumulator is charged with a current of 1mA/2,4V by the battery backup IC. The NiCd Accumulator has a capacity of 35 mAh which provides a continuous backup time of about 3 months.

Secondary Battery	
Battery Type:	NiCd Accumulator
Voltage:	2.4V
Capacity:	35 mAh

26.7 VMEbus STDBY-line

The IBC-20 allows the VME STDBY-line to backup the Local SRAM and RTC. The STDBY line can be used as an alternative to the on-board Ni-Cd Accumulator.

If the STDBY line is used, the accumulator must be disabled by opening both switches of SW6 (OFF position).

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APPENDIX A

CIRCUIT SCHEMATICS OF THE IBC-20 BOARD

APPENDIX A-1

CIRCUIT SCHEMATICS OF THE IBC MOD-1 MODULE

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APPENDIX B

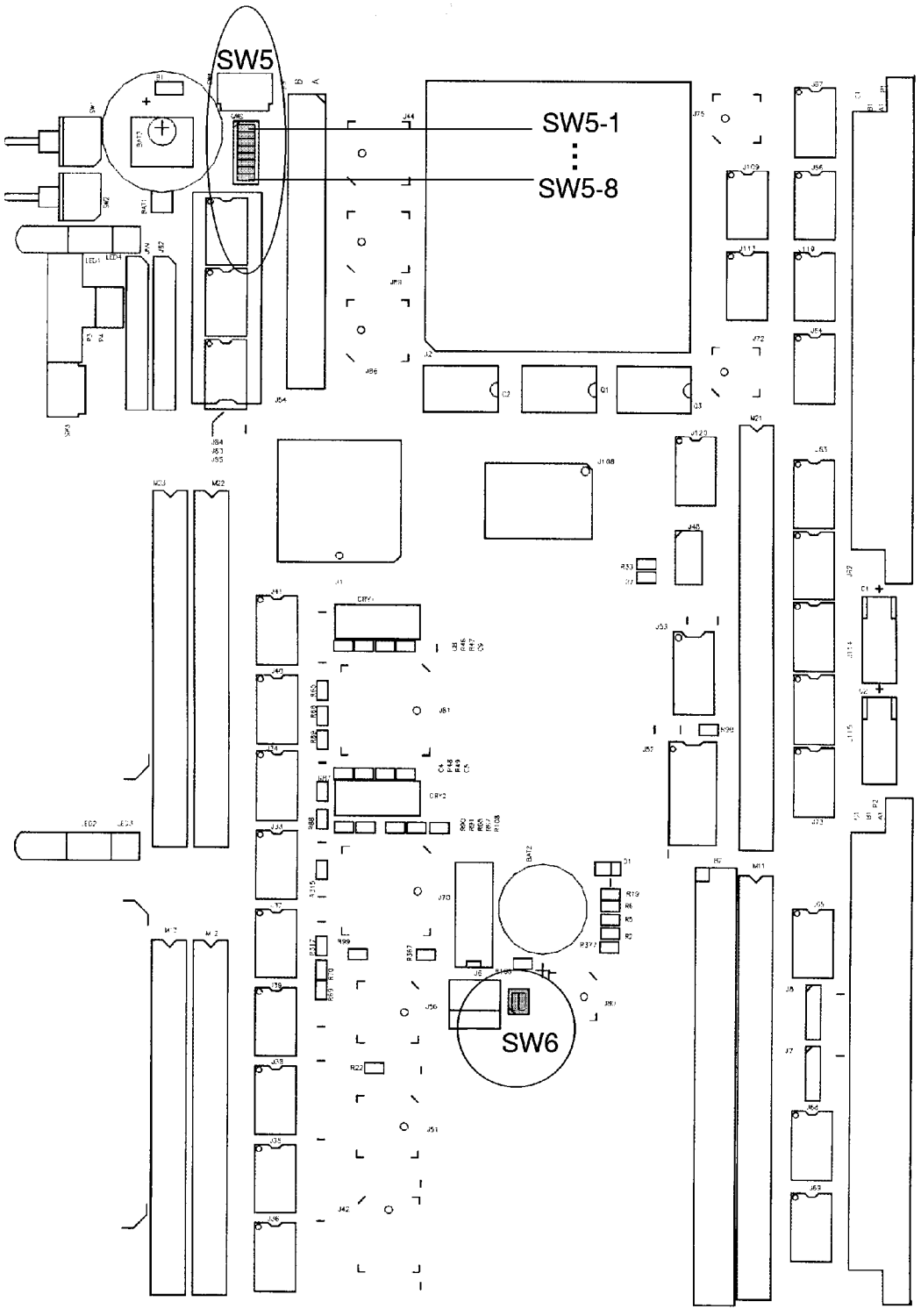
DEFAULT SWITCH SETTING ON THE BOARD

The following tables show the default slide switch settings on the board. The diagram displaying the location of the switches follows the tables.

Switch 5	Default	Name	Selections
SW5-1	ON	IBCFLASH	ON Local Flash EPROM is writable OFF Local Flash EPROM write protected
SW5-2	ON	VMERESOT	ON SYSRESET driven OFF SYSRESET not driven
SW5-3	ON	VMERESIN	ON SYSRESET received OFF SYSRESET not received
SW5-4	ON	MIN4.85V	ON Power-fail reset voltage 4.8V OFF Power-fail reset voltage 4.2V
SW5-5	ON	MODFLASH	ON Module Flash EPROM programmable OFF Module Flash EPROM write protected
SW5-6 SW5-7	ON ON	BRSEL1 BRSEL0	BR0 BR1 BR2 BR3 OFF OFF ON ON OFF ON OFF ON
SW5-8	ON	SLOT 1	ON Slot #1 function enabled OFF Slot #1 function disabled

Switch 6	Default	Selections
SW6-1/2	ON/ON	ON/ON Secondary Battery enabled OFF/OFF Secondary Battery disabled

APPENDIX B1: LOCATION DIAGRAM OF THE SLIDE SWITCHES



APPENDIX C

CONNECTOR PIN ASSIGNMENTS OF THE BOARD

Pinout of the I/O Connector M11

A1: -12V	B1: 5VSTDBY	C1: +12V
A2: -12V	B2: 5VSTDBY	C2: +12V
A3: +5V	B3: +5V	C3: +5V
A4: GND	B4: GND	C4: GND
A5: +5V	B5: P2A1	C5: +5V
A6: P2C1@	B6: P2C2@	C6: P2A2
A7: P2C3@	B7: P2A4	C7: P2A3
A8: P2C5@	B8: P2A5	C8: P2C4@
A9: P2C6@	B9: P2A7	C9: P2A6
A10: P2C7@	B10: GND	C10: P2A8
A11: P2A9	B11: P2C9@	C11: P2C8@
A12: P2C10@	B12: P2A11	C12: P2A10
A13: P2A12	B13: P2C12@	C13: P2C11@
A14: +5V	B14: P2C13@	C14: P2A13
A15: P2C14@	B15: P2A15	C15: P2A14
A16: P2A16	B16: P2C16@	C16: P2C15@
A17: P2C17@	B17: P2A18	C17: P2A17
A18: P2A19	B18: P2C19@	C18: P2C18@
A19: P2C20@	B19: P2A21	C19: P2A20
A20: P2A22	B20: GND	C20: P2C21@
A21: GND	B21: P2C22@	C21: GND
A22: P2C23@	B22: P2A24	C22: P2A23
A23: P2A25	B23: P2C25@	C23: P2C24@
A24: P2C26@	B24: P2A27	C24: P2A26
A25: P2A28	B25: P2C28@	C25: P2C27@
A26: P2C29@	B26: P2A30	C26: P2A29
A27: P2C30@	B27: GND	C27: P2A31
A28: GND	B28: GND	C28: GND
A29: P2C31@	B29: P2A32	C29: P2C32@
A30: +5V	B30: +5V	C30: +5V

@ : These pins are connected via bridges on the I/O selection field B2 to the VME/P2 connector. This default connection is compatible to the IBC-20 Revision 1.

Pinout of the FLXi Connector M12

A6: *	B6: *	C6: *
A7: *	B7: GND	C7: *
A8: BGOUT	B8: BGIN	C8: GND
A9: DFLX1	B9: FC0	C9: -12V
A10: DFLX2	B10: FC1	C10: *
A11: DFLX4	B11: FC2	C11: GND
A12: DFLX5	B12: SIZ0	C12: -12V
A13: DFLX7	B13: AS	C13: +5V
A14: DFLX9	B14: SIZ1	C14: GND
A15: DFLX10	B15: DS	C15: +5VSTDBY
A16: DFLX12	B16: RW	C16: *
A17: DFLX14	B17: *	C17: GND
A18: DFLX15	B18: DSACK0	C18: +5VSTDBY
A19: DFLX17	B19: DSACK1	C19: +5V
A20: DFLX19	B20: *	C20: GND
A21: DFLX20	B21: BERR	C21: +12VSWITCH
A22: DFLX22	B22: RTRY	C22: +5V
A23: DFLX24	B23: *	C23: GND
A24: DFLX25	B24: *	C24: +12V
A25: DFLX27	B25: *	C25: +5V
A26: DFLX29	B26: *	C26: GND
A27: DFLX30	B27: *	C27: +5V
A28: DFLX31	B28: *	C28: *
A29: IACKOUT	B29: IACKIN	C29: GND
A30: *	B30: *	C30: +5V

*** = Reserved pin. Pulled to +5V by 3.3 KOhm resistor.**

Pinout of the FLXi Connector M13

A6: *	B6: *	C6: *
A7: GND	B7: *	C7: GND
A8: CONFIG	B8: POWERUP	C8: RESET
A9: BGACK	B9: BR	C9: GND
A10: AFLX0	B10: AFLX1	C10: DFLX0
A11: AFLX2	B11: AFLX3	C11: DFLX3
A12: AFLX4	B12: AFLX5	C12: GND
A13: AFLX6	B13: AFLX7	C13: DFLX6
A14: AFLX8	B14: AFLX9	C14: DFLX8
A15: AFLX10	B15: AFLX11	C15: GND
A16: AFLX12	B16: AFLX13	C16: DFLX11
A17: AFLX14	B17: AFLX15	C17: DFLX13
A18: AFLX16	B18: AFLX17	C18: GND
A19: AFLX18	B19: AFLX19	C19: DFLX16
A20: AFLX20	B20: AFLX21	C20: DFLX18
A21: AFLX22	B21: AFLX23	C21: GND
A22: AFLX24	B22: AFLX25	C22: DFLX21
A23: AFLX26	B23: AFLX27	C23: DFLX23
A24: AFLX28	B24: AFLX29	C24: GND
A25: AFLX30	B25: AFLX31	C25: DFLX26
A26: reserved	B26: reserved	C26: DFLX28
A27: reserved	B27: reserved	C27: GND
A28: IPLIN0	C28: IPLIN1	C28: IPLIN2
A29: IPLOUT0	B29: IPLOUT1	C29: IPLOUT2
A30: MODINS	B30: RMC	C30: GND

Pinout of Connector M21

A1: -12V	B1: 5VSTDBY	C1: +12V
A2: -12V	B2: 5VSTDBY	C2: +12V
A3: +5V	B3: +5V	C3: +5V
A4: GND	B4: GND	C4: GND
A5: +5V	B5: P2C1@	C5: +5V
A6: %	B6: %	C6: P2C2@
A7: %	B7: P2C4@	C7: P2C3@
A8: %	B8: P2C5@	C8: %
A9: %	B9: P2C7@	C9: P2C6@
A10: %	B10: GND	C10: P2C8@
A11: P2C9@	B11: %	C11: %
A12: %	B12: P2C11@	C12: P2C10@
A13: P2C12@	B13: %	C13: %
A14: +5V	B14: %	C14: P2C13@
A15: %	B15: P2C15@	C15: P2C14@
A16: P2C16@	B16: %	C16: %
A17: %	B17: P2C18@	C17: P2C17@
A18: P2C19@	B18: %	C18: %
A19: %	B19: P2C21@	C19: P2C20@
A20: P2C22@	B20: GND	C20: %
A21: GND	B21: %	C21: GND
A22: %	B22: P2C24@	C22: P2C23@
A23: P2C25@	B23: %	C23: %
A24: %	B24: P2C27@	C24: P2C26@
A25: P2C28@	B25: %	C25: %
A26: %	B26: P2C30@	C26: P2C29@
A27: %	B27: GND	C27: P2C31@
A28: GND	B28: GND	C28: GND
A29: %	B29: P2C32@	C29: %
A30: +5V	B30: +5V	C30: +5V

@ : These pins are used to connect the Eagle module to the VME/P2 connector pins C1-C32. The connection to the VME/P2 connector is done via the I/O selection field B2. By default, these pins are open. This is compatible to the IBC-20 Revision 1.

% : Not connected pin

Pinout of the FLXi Connector M22

A6: *	B6: *	C6: *
A7: *	B7: GND	C7: *
A8: BGOUT	B8: BGIN	C8: GND
A9: DFLX1	B9: FC0	C9: -12V
A10: DFLX2	B10: FC1	C10: *
A11: DFLX4	B11: FC2	C11: GND
A12: DFLX5	B12: SIZ0	C12: -12V
A13: DFLX7	B13: AS	C13: +5V
A14: DFLX9	B14: SIZ1	C14: GND
A15: DFLX10	B15: DS	C15: +5VSTDBY
A16: DFLX12	B16: RW	C16: *
A17: DFLX14	B17: *	C17: GND
A18: DFLX15	B18: DSACK0	C18: +5VSTDBY
A19: DFLX17	B19: DSACK1	C19: +5V
A20: DFLX19	B20: *	C20: GND
A21: DFLX20	B21: BERR	C21: +12VSWITCH
A22: DFLX22	B22: RTRY	C22: +5V
A23: DFLX24	B23: *	C23: GND
A24: DFLX25	B24: *	C24: +12V
A25: DFLX27	B25: *	C25: +5V
A26: DFLX29	B26: *	C26: GND
A27: DFLX30	B27: *	C27: +5V
A28: DFLX31	B28: *	C28: *
A29: IACKOUT	B29: IACKIN	C29: GND
A30: *	B30: *	C30: +5V

*** = Reserved pin. Pulled to +5V by 3.3 KOhm Resistor.**

Pinout of the FLXi Connector M23

A6: *	B6: *	C6: *
A7: GND	B7: *	C7: GND
A8: CONFIG	B8: POWERUP	C8: RESET
A9: BGACK	B9: BR	C9: GND
A10: AFLX0	B10: AFLX1	C10: DFLX0
A11: AFLX2	B11: AFLX3	C11: DFLX3
A12: AFLX4	B12: AFLX5	C12: GND
A13: AFLX6	B13: AFLX7	C13: DFLX6
A14: AFLX8	B14: AFLX9	C14: DFLX8
A15: AFLX10	B15: AFLX11	C15: GND
A16: AFLX12	B16: AFLX13	C16: DFLX11
A17: AFLX14	B17: AFLX15	C17: DFLX13
A18: AFLX16	B18: AFLX17	C18: GND
A19: AFLX18	B19: AFLX19	C19: DFLX16
A20: AFLX20	B20: AFLX21	C20: DFLX18
A21: AFLX22	B21: AFLX23	C21: GND
A22: AFLX24	B22: AFLX25	C22: DFLX21
A23: AFLX26	B23: AFLX27	C23: DFLX23
A24: AFLX28	B24: AFLX29	C24: GND
A25: AFLX30	B25: AFLX31	C25: DFLX26
A26: reserved	B26: reserved	C26: DFLX28
A27: reserved	B27: reserved	C27: GND
A28: IPLIN0	C28: IPLIN1	C28: IPLIN2
A29: IPLOUT0	B29: IPLOUT1	C29: IPLOUT2
A30: MODINS	B30: RMC	C30: GND

APPENDIX D

LITERATURE REFERENCE

Please refer to the following books for further more detailed information.

1) MC 68020 Users Manual.

2) VMEbus Standards:

2618 S Shannon
Tempe Arizona 85282
(602) 966-5936

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APPENDIX E

PRODUCT ERROR REPORT

ALTHOUGH FORCE COMPUTERS HAS ACHIEVED A VERY HIGH STANDARD OF QUALITY IN PRODUCTS AND DOCUMENTATION, SUGGESTIONS FOR IMPROVEMENT ARE ALWAYS WELCOME.

ANY FEEDBACK YOU CARE TO OFFER WOULD BE APPRECIATED.

PLEASE USE ATTACHED "PRODUCT ERROR REPORT" FORM FOR YOUR COMMENTS AND RETURN IT TO ONE OF OUR FORCE COMPUTERS OFFICES.

FORCE COMPUTERS, GmbH

THE IBC MOD-1 MODULE

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1. GENERAL DESCRIPTION

The IBC MOD-1 module is designed for the IBC-20 revision 2 board to allow the user to increase the functionality of the IBC-20 base board. The module provides the MC68882 Floating Point Coprocessor and System EPROM built by Flash memory devices.

The IBC MOD-1 module is available with up to 8 Mbyte of non-volatile Flash System memory. The Flash memory devices are on-board programmable by the microprocessor of the IBC-20 board. The data path of the System EPROM is 32-bit wide.

The IBC MOD-1 module is available with or without a Floating Point Coprocessor.

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2. MODULE ASSEMBLY CODE

The IBC MOD-1 module supplies a 4 bit assembly code to the IBC-20 base board which allows the base board software to identify the memory capacity of the module and the presence of the MC68882 Floating Point Coprocessor.

The assembly code is available at the pins B36..B39 of the module connector. These pins are readable by the local processor via the CIO unit port A signals PA3..PA0.

The assignment of the assembly code to the module connector pins and the CIO unit terminals is shown in the next table:

Table 1: Assembly Code Assignments

Device	Assembly Code Bit			
	3	2	1	0
Module Connector Pin	B39	B38	B37	B36
CIO Unit Terminal	PA3	PA2	PA1	PA0

Bit 3 of the assembly code identifies the presence or absence of the Floating Point Coprocessor. Logical "0" indicates that the FPU is available, logical "1" is read if there is no FPU assembled. The bits 2..0 carry the code of the total memory capacity of the module.

The 4-bit assembly code is read when the port A data register of the CIO device is accessed with the address $FF800C0E.

Please refer to the chapter *"The Counter/Timer I/O Unit CIO Z8536"* of the Hardware User's Manual (Section 3) for more information about the signals connected to port A.

The table on the following page shows the 4-bit assembly code of the IBC MOD-1 module.

Table 2: Assembly Codes of the IBC MOD-1 Module

Assembly Code of the IBC MOD-1 Module			
Floating Point Coprocessor	Memory Capacity	Assembly Code Bit 3 2 1 0	Code (Hex)
present	0.5 MB	0 1 0 1	5H
	1 MB	0 0 0 1	1H
	2 MB	0 0 1 0	2H
	3 MB	0 0 1 1	3H
	4 MB	0 1 0 0	4H
	6 MB	0 1 1 0	6H
	8 MB	0 0 0 0	0H
	No Memory	0 1 1 1	7H
not present	0.5 MB	1 1 0 1	DH
	1 MB	1 0 0 1	9H
	2 MB	1 0 1 0	AH
	3 MB	1 0 1 1	BH
	4 MB	1 1 0 0	CH
	6 MB	1 1 1 0	EH
	8 MB	1 0 0 0	8H
	No Memory	1 1 1 1	FH

3. THE FLOATING POINT UNIT MC68882

The Floating Point Unit (FPU) of the IBC MOD-1 module functions as a coprocessor to the MC68020 microprocessor of the IBC-20 board.

Via the 68020 coprocessor interface, the FPU provides a logical extension to the 68020 microprocessor registers and instruction set. For the programmer, the FPU registers appear transparent, as if the MC68882 is implemented on the microprocessor.

The IBC MOD-1 module uses the 84 pin PLCC packaged Floating Point Coprocessor with 25 MHz speed.

The presence of the Floating Point Unit is indicated to the IBC-20 board by the status of the module connector pin B39. The connector pin B39 is readable via the CIO unit port PA3 and allows the base board software to detect the presence of the Floating Point Unit on the IBC MOD-1 module.

On the module, the connector pin B39 is attached to the "Sense" signal of the FPU device. If there is a FPU device installed, pin B39 will be asserted to low, since the "Sense" signal is internally tied to "ground".

The next table shows the Floating Point Unit coding.

Table 3: Floating Point Unit Coding

IBC MOD-1 Floating Point Unit Coding	
Floating Point Unit	**Assembly Code Bit 0**
not present	1
present	0

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4. THE SYSTEM EPROM MEMORY

The IBC MOD-1 module is available with up to 8 Mbyte of System EPROM memory by using Flash EPROM devices.

The System EPROM is accessible by the microprocessor of the base board in the address range $FF000000 - $FF7FFFFF.

The switch SW5-5 on the base board provides erase/program protection of the System memory.

Depending on the amount of Flash EPROM memory, the System EPROM is present in the address ranges listed in the table below.

Table 4: Addresses of System EPROM Memory

Total Memory Capacity	Address Range
0.5 Mbyte	FF000000 - FF07FFFF
1 Mbyte	FF000000 - FF0FFFFF
2 Mbyte	FF000000 - FF1FFFFF
3 Mbyte	FF000000 - FF2FFFFF
4 Mbyte	FF000000 - FF3FFFFF
6 Mbyte	FF000000 - FF5FFFFF
8 Mbyte	FF000000 - FF7FFFFF

4.1 System EPROM Capacity Code

The IBC MOD-1 module supports System EPROM memory with various capacities. The total capacity of the System memory available on the module is displayed with a 3-bit code. The code is supplied at the module connector pins B36/B37/B38.

The capacity code is provided with the bits 3..0 of the 4-bit module assembly code.

The following table shows the code for the total capacity of the System EPROM memory.

Table 5: System EPROM Coding

IBC MOD-1 Memory Capacity Coding	
System EPROM Capacity	**Assembly Code Bit** 2 1 0
0.5 Mbyte	1 0 1
1 Mbyte	0 0 1
2 Mbyte	0 1 0
3 Mbyte	0 1 1
4 Mbyte	1 0 0
6 Mbyte	1 1 0
8 Mbyte	0 0 0
No Memory	1 1 1

4.2 Flash EPROM Access

The module provides the System EPROM with 32-bit wide data path.

Read accesses to the System memory are allowed with any operand size. Writing to the System memory must be with 32-bit data at long word aligned addresses because the control logic does not support byte or word operands.

The 150ns access time of the Flash memory devices allows the processor to access the System EPROM memory with 3 wait states in read cycles.

Write accesses to the System EPROM memory require 4 wait states with 25 MHz processor speed.

4.3 Program/Erase Protection

The Flash memory devices of the System EPROM are program/erase protectable by switch SW5-5 (named "MODFLASH"), which is located on the IBC-20 board.

If the switch is set "OFF", the System EPROM is protected from being erased/programmed. Setting the switch to "ON" (default) allows the processor to program the Flash EPROM.

A convenient way to program the Flash memory devices is to use the "PROG" command provided by the VMEPROM firmware. This routine supports the special programming algorithm which is demanded by the Flash device.

Details about the programming algorithm can be found in the corresponding data sheet (please see Section 5).

The usage of the "PROG" command is described in the *IBC-20 Firmware User's Manual*.

NOTE

The System memory is arranged with 32-bit wide data path. Therefore, the "Width" parameter of the PROG command must be set to "4" (32 bit) when the System memory is programmed.

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