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FORCE COMPUTERS
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SPARC/IOBP-520

Installation Guide

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1 Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the SPARC/IOBP-520. For your protection, follow all warnings and instructions found in the following text.

General notes

This *Installation Guide* provides the necessary information to install and handle the SPARC/IOBP-520. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. In case you need additional information, ask your Force Computers representative.

The SPARC/IOBP-520 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or qualified persons in electronics or electrical engineering are authorized to install, uninstall or maintain the SPARC/IOBP-520. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Installation

Electrostatic discharge and incorrect board or I/O panel installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing the I/O panel, read this *Installation Guide*.**
- **Verify that the *Installation Guide* of the board under consideration states that the I/O panel under consideration is designed for use with the board.**
- **Only use the I/O panel connectors indicated by the *Installation Guide* of the board under consideration. Note that in general the connectors to be used differ**
  - **between different boards**
  - **and between different main PCBs of the same board installed in different CompactPCI slots (e.g. base board and I/O board).**

    Therefore, in case of boards using several PCBs, check the *Installation Guide* of the board for information additional to the following:



  - **The SPARC/IOBP-520/CPU must be used as I/O panel for the base board of the SPARC/CPCI-52x. The SPARC/IOBP-520/IO must be used as I/O panel for the I/O-board of the SPARC/CPCI-52x.**

    The *Installation Guide* of the board additionally documents which connectors of the I/O panel are to be used together with which PCB.

- **In case of delivery as part of a system, never change the cabling of the I/O panel unless explicitly stated otherwise in the system's *User's Manual*.**
- **Before touching integrated circuits, ensure that you are working in an electrostatic-free environment.**
- **Before installing or uninstalling the board, read the board's *Installation Guide* and ensure that you apply all safety notes given by that guide.**
- **Before installing or uninstalling the board in a CompactPCI rack:**
  - **Check all installed boards for steps that you have to take before turning off the power.**
  - **Take those steps.**
  - **Finally turn off the power.**

Protect your environment

Always dispose used batteries and/or old boards according to your country's legislation.

RJ-45 connector

If an RJ-45 connector is available on the board, take into account that the RJ-45 connector type is used for telephone connectors and for twisted pair Ethernet (TPE) connectors. Note that mismatching these 2 connectors may destroy your telephone as well as your SPARC/IOBP-520. Therefore:

- **Make sure that TPE connectors near your working area are clearly marked as network connectors.**
- **Make sure that TPE bushing of the system is connected only to safety extra low voltage (SELV) circuits.**
- **Verify that the length of the electric cable connected to a TPE bushing does not exceed 1 kilometer outside the building.**
- **If in doubt, ask your system administrator.**



2 Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, welche bei der Installation, dem Betrieb und der Wartung des SPARC/IOBP-520 zu beachten sind. Beachten Sie zu Ihrem Schutz alle folgenden Warnhinweise und Anleitungen.

Dieses Installationshandbuch enthält alle notwendigen Informationen zur Installation und zum Betrieb des SPARC/IOBP-520. Da es sich um ein komplexes Produkt mit einer aufwendigen Bedienung handelt, kann keine Garantie dafür übernommen werden, dass die enthaltenen Informationen vollständig sind. Für weitere Informationen wenden Sie sich bitte an Ihren Vertreter der Firma Force Computers.

Das SPARC/IOBP-520 erfüllt die gültigen industriellen Sicherheitsanforderungen. Dieses Produkt darf ausschließlich für Anwendungen innerhalb der Telekommunikationsindustrie und der industriellen Steuerung verwendet werden.

Lediglich von Force Computers eingewiesene oder im Bereich Elektrotechnik oder Elektronik qualifizierte Personen sind zur Installation, zum Betrieb und zur Wartung dieses Produktes befugt. Die in dieser Dokumentation enthaltenen Informationen sollen lediglich als Hilfestellung für entsprechend qualifiziertes Fachpersonal dienen. Keinesfalls können sie dieses ersetzen.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Lesen Sie vor Einbau oder Ausbau des IOBPs dieses Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das jeweilige IOBP laut Benutzerhandbuch des jeweiligen CPU Boards zu diesem CPU Board passt.**
- **Verwenden Sie nur die IOBP Stecker, die im Benutzerhandbuch des jeweiligen CPU Boards angegeben sind. Im allgemeinen unterscheiden sich die Stecker durch folgendes:**
  - **verschiedene CPU Boards**
  - **verschiedene Platinen desselben CPU Boards, die in verschiedene CompactPCI Steckplätze gesteckt werden (z.B. Basis-Board und I/O-Board)**



- **Überprüfen Sie deshalb im Falle von Boards mit mehreren Platinen das Benutzerhandbuch auf Informationen über folgendes:**
  - **Das SPARC/IOBP-520/CPU muss als IOBP für das Basis-Board des SPARC/CPCI-52x verwendet werden. Das SPARC/IOBP-520/IO muss als IOBP für das I/O-Board des SPARC/CPCI-52x verwendet werden.**
  - **Das Benutzerhandbuch des Boards beschreibt ausserdem, welche Stecker des IOBPs zusammen mit welcher Platine verwendet werden sollen.**
- **Wird das IOBP als Teil eines Systems geliefert, tauschen Sie nie die Verkabelungen des IOBPs, es sei denn, es ist in der Systemdokumentation ausdrücklich erwähnt.**
- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Lesen Sie vor Einbau oder Ausbau des CPU Boards dessen Benutzerhandbuch, und vergewissern Sie sich, dass alle darin enthaltenen Sicherheitshinweise befolgt werden.**
- **Beachten Sie folgendes vor dem Einbau in ein CompactPCI Rack oder vor dem Ausbau daraus:**
  - **Überprüfen Sie alle installierten Boards auf Schritte, die unternommen werden müssen, bevor Sie den Strom abschalten.**
  - **Unternehmen Sie diese Schritte.**
  - **Schalten Sie schließlich den Strom ab.**

Umweltschutz

Alte Batterien und/oder Boards oder Systeme müssen stets gemäß der in Ihrem Land gültigen Gesetzgebung entsorgt werden.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:

- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**

3 How to Install the SPARC/IOBP-520

This manual describes the SPARC/IOBP-520 I/O panel, which is designed to be used together with a SPARC/CPU-52x.

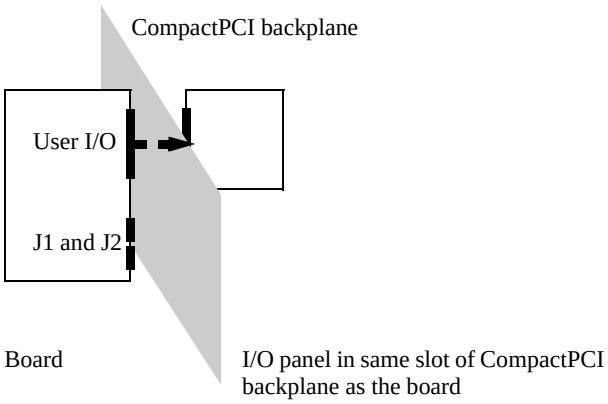
…/CPU, …/IO variants

The SPARC/IOBP-520 I/O panel is available in 2 variants:

- The SPARC/IOBP-520/CPU variant of the SPARC/IOBP-520 is an I/O panel to be used together with the base board of a SPARC/CPCI-52x.
- The SPARC/IOBP-520/IO is an I/O panel to be used together with the I/O-board of a SPARC/CPCI-52x.

I/O panel overview

The SPARC/IOBP-520 I/O panel is plugged into the CompactPCI backplane from its rear. It enables easy connection to the backplane I/O signals of the board plugged into the CompactPCI backplane from the front. The backplane I/O signals are available on the user I/O connectors of the board and depend on the pinout implemented on the board installed in the CompactPCI slot under consideration.



The number of user I/O connectors depends on the board under consideration.

If contained in other products …

The I/O panel variants are also delivered as part of accessory kits compiled for boards and as part of a system design:

…/AccKit…

- If delivered as part of an accessory kit, the accessory kit typically also contains cables to be used with the I/O panel or with connectors on the board's front panel. For information on the accessory kits defined for a board refer to the board's *Installation Guide*.

Systems

- If delivered as part of a system design, the I/O panel is already installed in the system. For information on the system connectors available for user-defined system configuration refer to the system's *User's Manual*. The cabling of all other connectors of the I/O panel must remain as configured at system delivery.

How to begin installation

1. Read the safety notes (see section 1 “Safety Notes” on page 1).
2. Refer to the following section for general information on the I/O panel, for a location diagram and for connector related information like for example the pinouts and cabling or termination considerations in case of SCSI interfaces.

Table 1 History of manual publication

Edition No.	Date	Description
1.0	Feb. 1998	First Print
2.0	Mar. 1998	Editorial Changes
3.0	October 1999	Section “Safety Notes” included
4.0/AA	August 2001	Section “Sicherheitshinweise” included, editorial changes
AB	November 2001	Editorial changes

4 SPARC/IOBP-520 Connectors and Jumpers

The remaining parts of this section document the connector pinouts and other installation information related to the connectors or jumpers such as information on SCSI termination and cabling or information on the Ethernet connectors. See table 2 “SPARC/IOBP-520/CPU connectors” on page 8, table 3 “SPARC/IOBP-520/CPU jumpers” on page 8, and table 5 “SPARC/IOBP-520/IO connectors” on page 12 for an overview for the respective I/O panel.

Note: **Note that some connectors listed in table 2 “SPARC/IOBP-520/CPU connectors” on page 8 and table 5 “SPARC/IOBP-520/IO connectors” on page 12 are not assembled in the numerical sort order on the PCB, for example the following:**

- J6, J7, J9, and J11 for the …/CPU variant of the SPARC/IOBP-520,
- JP5, JP6, JP7, and JP8 for the …/IO variant of the SPARC/IOBP-520.

4.1 …/CPU Variant

Table 2 SPARC/IOBP-520/CPU connectors

Connector and installation restrictions		See …
P5	CompactPCI connector P5	page 9
J6	Serial A+B D-Sub: SerA and SerB	page 10
JP9	Serial A+B header: SerA and SerB	page 10
J7	Headphone: AUD	page 11
J9	Line In: AUD	
J11	Keyboard, mouse	page 10
J12	100BaseT Ethernet – available only if J13 unplugged	page 16
J13	MII Ethernet – available only if J12 unplugged	
JP1	Parallel: LPT	page 11
JP2	Floppy: FDC	page 10
JP3	SCSI (8 bit) out	page 18
JP4	SCSI (8 bit) in	
J14	Ultra/wide SCSI	

Table 3 SPARC/IOBP-520/CPU jumpers

Jumper and installation restrictions		See …
JP10	Ethernet configuration	page 16

Figure 1 **SPARC/IOBP-520/CPU (schematic)**

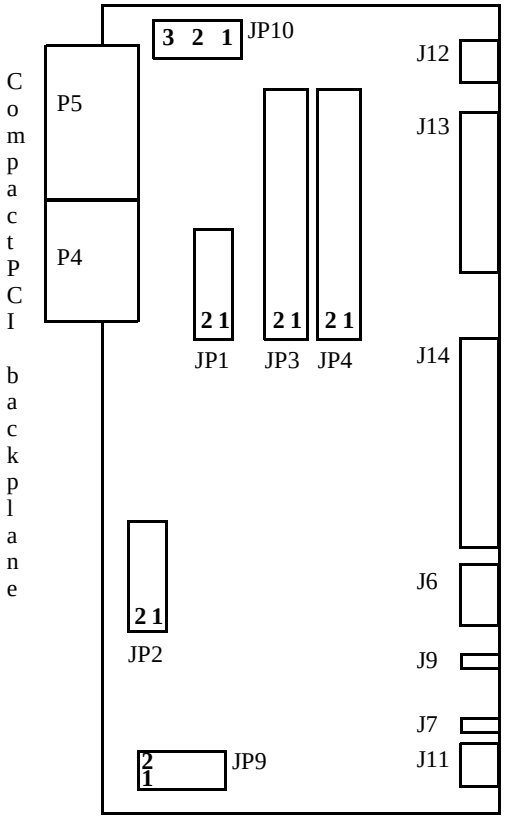
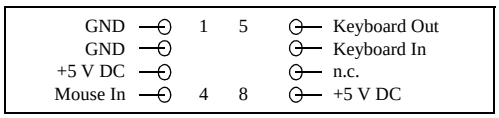


Figure 2 **CompactPCI connector P5 for SPARC/IOBP-520/CPU**

A	B	C		D	E
SCSI D8	SCSI D9	SCSI D10	1	SCSI D11	n.c.
SCSI SEL	SCSI CD	SCSI REQ	2	SCSI IO	SCSI WIDETERMPWR
SCSI ATN	SCSI BSY	SCSI ACK	3	SCSI RST	SCSI MSG
SCSI D4	SCSI D5	SCSI D6	4	SCSI D7	SCSI TERMPWR
SCSI D0	SCSI D1	SCSI D2	5	SCSI D3	SCSI DP0
SCSI D12	SCSI D13	SCSI D14	6	SCSI D15	SCSI DP1
MII RXD3	MII RXD2	MII RXD1	7	MII RXD0	MII RX_CLK
MII RX_DV	MII COL	MII CRS	8	MII RX_ER	MII MGT_DIO
MII TXD3	MII TXD2	MII TXD1	9	MII TXD0	MII TX_CLK
FDC HDSEL	FDC DSKCHG	MII TX_EN	10	MII TX_ER	MII MGT_CLK
FDC WDATA	FDC WGATE	FDC TRK0	11	FDC WP	FDC RDATA
FDC DR0	FDC DR1	FDC MTR0	12	FDC DIR	FDC STEP
FDC EJECT	FDC DENSEL	FDC DSENS	13	FDC INDEX	VP5_IOBP
LPT BSY	LPT ERR	LPT SLIN	14	LPT INIT	n.c.
VP5_IOBP	LPT PE	LPT SLCT	15	LPT AFD	n.c.
LPT D4	LPT D5	LPT D6	16	LPT D7	LPT ACK
LPT D0	LPT D1	LPT D2	17	LPT D3	LPT STB
SerA RXD	SerA CTS	SerB DCD	18	SerB CTS	SerB RXD
SerA TXD	SerA RTS	SerA DCD	19	SerB RTS	SerB TXD
SerA DTR	Keyboard Out	Keyboard In	20	Mouse In	SerB DTR
AUD rLINE IN	AUD rAUX2 IN	AUD rAUX1 IN	21	AUD r OUT	AUD Mono OUT
AUD lLINE IN	AUD lAUX2 IN	AUD lAUX1 IN	22	AUD l OUT	AGND

The actual AUD signals may depend on the factory options chosen for the SPARC/CPCI-52x under consideration. However, the right and left channel of LINE IN and of OUT as well as AGND, which are used for J7 and J9, are not affected.

Figure 3 Keyboard, mouse (J11)



Mini DIN-8

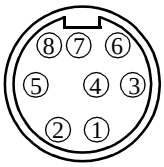


Figure 4 Floppy: FDC (JP2)

EJECT	1	2	DENSEL
n.c.	3	4	DSENS
n.c.	5	6	n.c.
GND	7	8	INDEX
GND	9	10	DR0
GND	11	12	DR1
GND	13	14	n.c.
GND	15	16	MTR0
GND	17	18	DIR
GND	19	20	STEP
GND	21	22	WDATA
GND	23	24	WGATE
GND	25	26	TRK0
GND	27	28	WP
GND	29	30	RDATA
GND	31	32	HDSEL
GND	33	34	DSKCHG

34-pin header

Figure 5 Serial A+B D-Sub: SerA and SerB (J6)

n.c.	1	14	SerB TXD
SerA TxD		15	n.c.
SerA RxD			SerB RXD
SerA RTS			n.c.
SerA CTS	5		n.c.
n.c.			SerB RTS
GND		20	SerA DTR
SerA DCD			n.c.
n.c.			n.c.
n.c.	10		GND
SerB DTR			n.c.
SerB DCD		25	n.c.
SerB CTS	13	26	n.c.

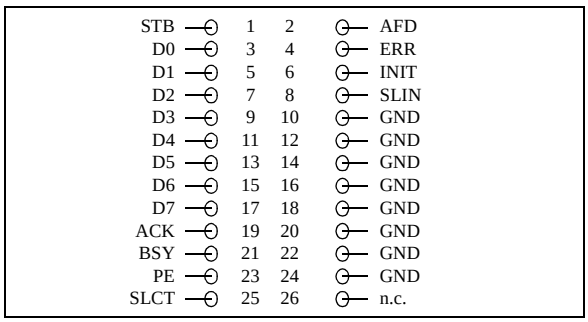
26-pin D-Sub

Figure 6 Serial A+B header: SerA and SerB (JP9)

n.c.	1	2	n.c.
n.c.	3	4	n.c.
SerB TxD	5	6	SerA TxD
SerB RxD	7	8	SerA RxD
SerB RTS	9	10	SerA RTS
SerB CTS	11	12	SerA CTS
GND	13	14	GND

14-pin header:

Figure 7 **Parallel: LPT (JP1)**



26-pin header

Table 4 **Audio connectors (all EIA standard 3.5-mm/0.125-inch jacks)**

Signal	**Location**	**Headphone: AUD** J9	**Line In: AUD** J7
Left channel	Tip	l OUT	lLINE IN
Right channel	Ring	r OUT	rLINE IN
GND	Shield	AGND	

4.2 …/IO Variant

Table 5 SPARC/IOBP-520/IO connectors

Connector and installation restrictions		See …
P5	CompactPCI connector P5	page 13
P4	CompactPCI connector P4	page 14
J12	100BaseT Ethernet – available only if J13 unplugged	page 16
J13	MII Ethernet – available only if J12 unplugged	
JP3	SCSI (8 bit) out	page 18
JP4	SCSI (8 bit) in	
J14	Ultra/wide SCSI	
JP5	PMC #1 user I/O 1…32	page 14
JP6	PMC #1 user I/O 33…64	
JP7	PMC #2 user I/O 1…32	
JP8	PMC #2 user I/O 33…64	

Table 6 SPARC/IOBP-520/IO jumpers

Jumper and installation restrictions		See …
JP10	Ethernet configuration	page 16

Figure 8 **SPARC/IOBP-520/IO (schematic)**

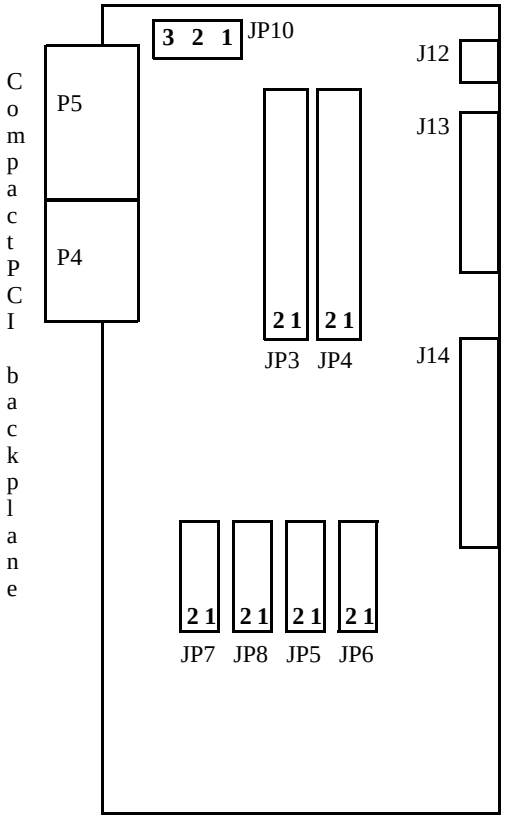


Figure 9 **CompactPCI connector P5 for SPARC/IOBP-520/IO**

A	B	C		D	E
SCSI D8	SCSI D9	SCSI D10	1	SCSI D11	n.c.
SCSI SEL	SCSI CD	SCSI REQ	2	SCSI IO	SCSI WIDETERMPWR
SCSI ATN	SCSI BSY	SCSI ACK	3	SCSI RST	SCSI MSG
SCSI D4	SCSI D5	SCSI D6	4	SCSI D7	SCSI TERMPWR
SCSI D0	SCSI D1	SCSI D2	5	SCSI D3	SCSI DP0
SCSI D12	SCSI D13	SCSI D14	6	SCSI D15	SCSI DP1
MII RXD3	MII RXD2	MII RXD1	7	MII RXD0	MII RX_CLK
MII RX_DV	MII COL	MII CRS	8	MII RX_ER	MII MGT_DIO
MII TXD3	MII TXD2	MII TXD1	9	MII TXD0	MII TX_CLK
PMC #2 I/O 19	PMC #2 I/O 20	MII TX_EN	10	MII TX_ER	MII MGT_CLK
PMC #2 I/O 14	PMC #2 I/O 15	PMC #2 I/O 16	11	PMC #2 I/O 17	PMC #2 I/O 18
PMC #2 I/O 9	PMC #2 I/O 10	PMC #2 I/O 11	12	PMC #2 I/O 12	PMC #2 I/O 13
PMC #2 I/O 5	PMC #2 I/O 6	PMC #2 I/O 7	13	PMC #2 I/O 8	VP5_IOBP
PMC #2 I/O 1	PMC #2 I/O 2	PMC #2 I/O 3	14	PMC #2 I/O 4	n.c.
VP5_IOBP	n.c.	n.c.	15	n.c.	n.c.
n.c.	n.c.	n.c.	16	n.c.	n.c.
n.c.	n.c.	n.c.	17	n.c.	n.c.
n.c.	n.c.	n.c.	18	n.c.	n.c.
n.c.	n.c.	n.c.	19	n.c.	n.c.
n.c.	n.c.	n.c.	20	n.c.	n.c.
n.c.	n.c.	n.c.	21	n.c.	n.c.
n.c.	n.c.	n.c.	22	n.c.	n.c.

Figure 10 CompactPCI connector P4 for SPARC/IOBP-520/IO

A	B	C		D	E
PMC #1 I/O 61	PMC #1 I/O 62	PMC #1 I/O 63	1	PMC #1 I/O 64	n.c.
PMC #1 I/O 56	PMC #1 I/O 57	PMC #1 I/O 58	2	PMC #1 I/O 59	PMC #1 I/O 60
PMC #1 I/O 51	PMC #1 I/O 52	PMC #1 I/O 53	3	PMC #1 I/O 54	PMC #1 I/O 55
PMC #1 I/O 46	PMC #1 I/O 47	PMC #1 I/O 48	4	PMC #1 I/O 49	PMC #1 I/O 50
PMC #1 I/O 41	PMC #1 I/O 42	PMC #1 I/O 43	5	PMC #1 I/O 44	PMC #1 I/O 45
PMC #1 I/O 36	PMC #1 I/O 37	PMC #1 I/O 38	6	PMC #1 I/O 39	PMC #1 I/O 40
PMC #1 I/O 31	PMC #1 I/O 32	PMC #1 I/O 33	7	PMC #1 I/O 34	PMC #1 I/O 35
PMC #1 I/O 26	PMC #1 I/O 27	PMC #1 I/O 28	8	PMC #1 I/O 29	PMC #1 I/O 30
PMC #1 I/O 21	PMC #1 I/O 22	PMC #1 I/O 23	9	PMC #1 I/O 24	PMC #1 I/O 25
PMC #1 I/O 16	PMC #1 I/O 17	PMC #1 I/O 18	10	PMC #1 I/O 19	PMC #1 I/O 20
PMC #1 I/O 11	PMC #1 I/O 12	PMC #1 I/O 13	11	PMC #1 I/O 14	PMC #1 I/O 15
	Coding key area		12		
			13		
			14		
PMC #1 I/O 6	PMC #1 I/O 7	PMC #1 I/O 8	15	PMC #1 I/O 9	PMC #1 I/O 10
PMC #1 I/O 1	PMC #1 I/O 2	PMC #1 I/O 3	16	PMC #1 I/O 4	PMC #1 I/O 5
PMC #2 I/O 61	PMC #2 I/O 62	PMC #2 I/O 63	17	PMC #2 I/O 64	VP5_IOBP
PMC #2 I/O 56	PMC #2 I/O 57	PMC #2 I/O 58	18	PMC #2 I/O 59	PMC #2 I/O 60
PMC #2 I/O 51	PMC #2 I/O 52	PMC #2 I/O 53	19	PMC #2 I/O 54	PMC #2 I/O 55
PMC #2 I/O 46	PMC #2 I/O 47	PMC #2 I/O 48	20	PMC #2 I/O 49	PMC #2 I/O 50
PMC #2 I/O 41	PMC #2 I/O 42	PMC #2 I/O 43	21	PMC #2 I/O 44	PMC #2 I/O 45
PMC #2 I/O 36	PMC #2 I/O 37	PMC #2 I/O 38	22	PMC #2 I/O 39	PMC #2 I/O 40
PMC #2 I/O 31	PMC #2 I/O 32	PMC #2 I/O 33	23	PMC #2 I/O 34	PMC #2 I/O 35
PMC #2 I/O 26	PMC #2 I/O 27	PMC #2 I/O 28	24	PMC #2 I/O 29	PMC #2 I/O 30
PMC #2 I/O 21	PMC #2 I/O 22	PMC #2 I/O 23	25	PMC #2 I/O 24	PMC #2 I/O 25

PMC User I/O Connectors and Installation Restrictions – Connectors Only Available in Case of …/IO variant

Caution



Note that the I/O board of the SPARC/CPCI-52x provides factory options concerning the signal routing of the 2 PMC slots to the CompactPCI backplane. Check the actual signal routing of the SPARC/CPCI-52x under consideration before connecting any cables to the PMC user I/O connectors of the SPARC/IOBP-520/IO.

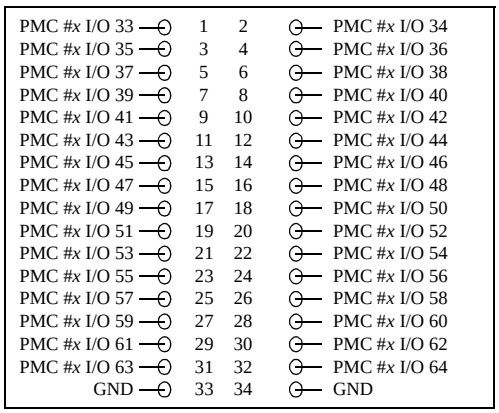
Figure 11 PMC #1 user I/O 1…32 (JP5) and PMC #2 user I/O 1…32 (JP7)

PMC #*x* I/O 1	1	2	PMC #*x* I/O 2
PMC #*x* I/O 3	3	4	PMC #*x* I/O 4
PMC #*x* I/O 5	5	6	PMC #*x* I/O 6
PMC #*x* I/O 7	7	8	PMC #*x* I/O 8
PMC #*x* I/O 9	9	10	PMC #*x* I/O 10
PMC #*x* I/O 11	11	12	PMC #*x* I/O 12
PMC #*x* I/O 13	13	14	PMC #*x* I/O 14
PMC #*x* I/O 15	15	16	PMC #*x* I/O 16
PMC #*x* I/O 17	17	18	PMC #*x* I/O 18
PMC #*x* I/O 19	19	20	PMC #*x* I/O 20
PMC #*x* I/O 21	21	22	PMC #*x* I/O 22
PMC #*x* I/O 23	23	24	PMC #*x* I/O 24
PMC #*x* I/O 25	25	26	PMC #*x* I/O 26
PMC #*x* I/O 27	27	28	PMC #*x* I/O 28
PMC #*x* I/O 29	29	30	PMC #*x* I/O 30
PMC #*x* I/O 31	31	32	PMC #*x* I/O 32
GND	33	34	GND

PMC #*x* = PMC #1 for JP5
PMC #*x* = PMC #2 for JP7

34-pin header

Figure 12 **PMC #1 user I/O 33…64 (JP6) and PMC #2 user I/O 33…64 (JP8)**



4.3 …/CPU and …/IO Variants

This section documents all connectors which provide the same pinout on SPARC/IOBP-520/CPU and …/IO:

- For “Ethernet Connectors and Installation Restrictions” see page 16
- and for “SCSI Connectors, Termination, and Cabling Restrictions” see page 18.

For all other connectors

- see section 4.1 “…/CPU Variant” on page 8
- or section 4.2 “…/IO Variant” on page 12.

Ethernet Connectors and Installation Restrictions

The setting of a jumper on-board the I/O panel controls whether the Ethernet interface is available on the I/O panel or on the board to which the I/O panel is connected. For location information, see JP10 on page 9 for the …/CPU variant of the I/O panel and see JP10 on page 13 for the …/IO variant of the I/O panel. The settings described below apply to the jumper on both variants:

- If pin 2 and 3 of JP10 are jumpered, the front-panel connector of the SPARC/CPCI-52x is operational and the I/O panel connectors are non-operational. In case of the …/CPU variant the operational front-panel connector of the SPARC/CPCI-52x is located on the front panel of the base board. In case of the …/IO variant the operational front-panel connector is located on the front panel of the I/O board of the SPARC/CPCI-52x.



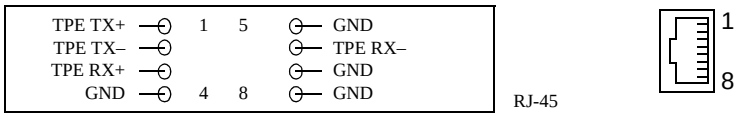
JP10 on SPARC/IOBP-520 (default setting)

- If pin 1 and 2 of JP10 are jumpered, the base board connector of the SPARC/CPCI-52x is non-operational and the I/O panel connectors are operational. However, never operate the SPARC/IOBP-520 with both Ethernet connectors J13 and J12 connected at the same time.



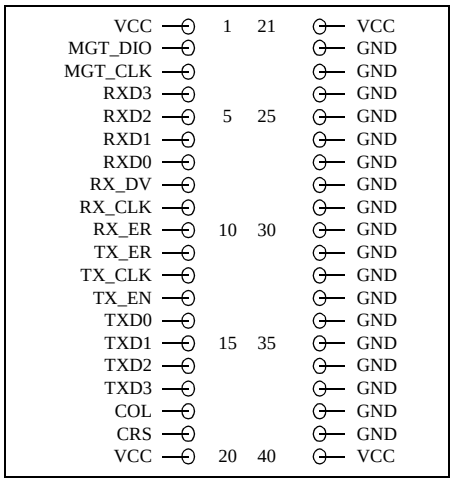
JP10 on SPARC/IOBP-520

Figure 13 **100BaseT Ethernet – available only if J13 unplugged (J12)**



RJ-45

Figure 14 **MII Ethernet – available only if J12 unplugged (J13)**

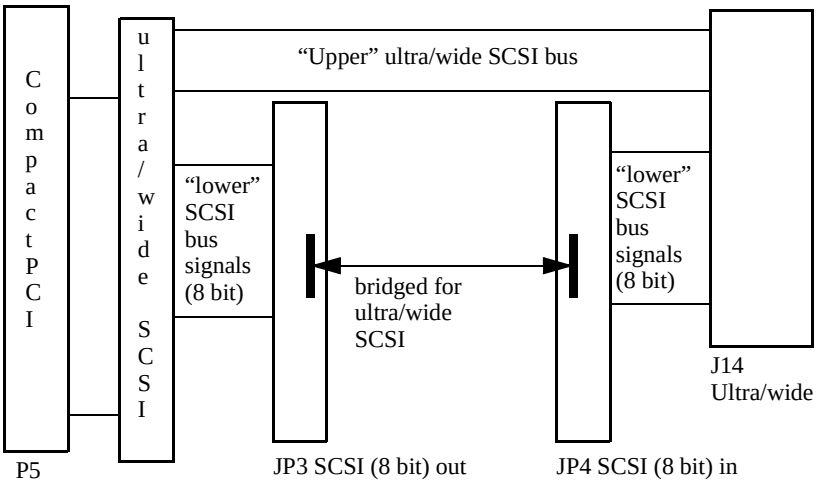


40-pin fine pitch connector

SCSI Connectors, Termination, and Cabling Restrictions

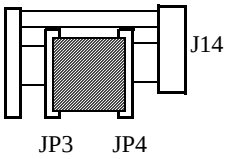
The SPARC/IOBP-520 provides the ultra/wide SCSI interface (16-bit) via J14 and a SCSI interface (8-bit) via JP3. Both interfaces provide automatic termination.

Figure 15 Block diagram of the SCSI interface

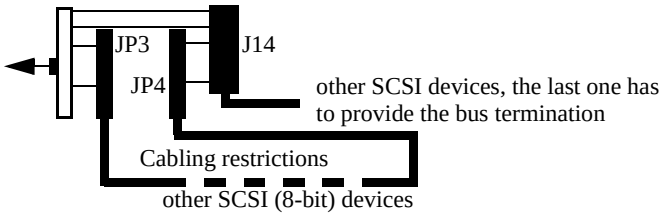


Note: **The SCSI bus available on JP3 is a part of the ultra/wide SCSI bus. The signals of the SCSI bus are connected to the JP3 header. The remaining signals of the ultra/wide SCSI bus are directly connected to the J14 connector, i.e. the upper 8 data bit signals D8, …, D15, and DP1. In this section these remaining signals are called "upper" ultra/wide SCSI bus, in contrast to the "lower" 8-bit SCSI bus.**

- To use the ultra/wide SCSI interface, JP3 and JP4 must be bridged as assembled at delivery of the SPARC/IOBP-520.



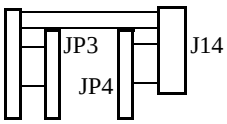
- To use both the ultra/wide SCSI interface and the 8-bit SCSI interface simultaneously, the actual cabling between JP3 and JP4 and the actual SCSI devices must be considered, potentially also resulting in J14 providing a wide instead of an ultra/wide SCSI interface. Therefore, before using such a configuration, please ask your local Force Computers representative for further information.



SCSI configurations

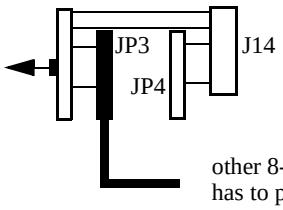
Use one of the following configurations for the SCSI interface of the SPARC/IOBP-520:

1. JP3, JP4, and J14 are not plugged.



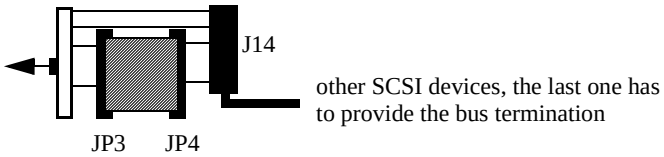
   Both, the “upper” ultra/wide SCSI bus and the 8-bit SCSI bus are terminated.

2. JP3 is plugged, but JP4 and J14 are not plugged.



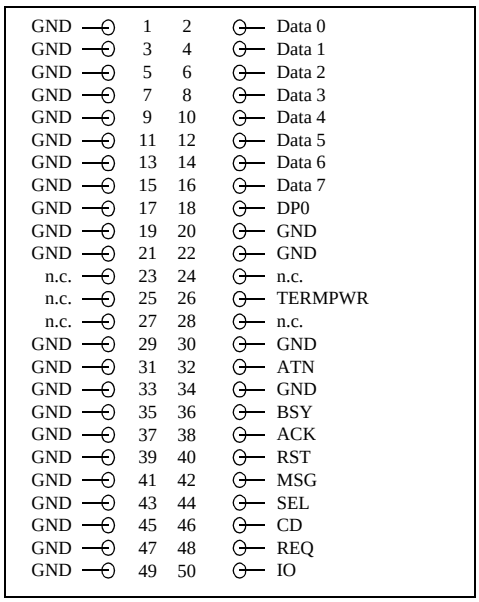
   The “upper” ultra/wide-SCSI bus is terminated. However, the 8-bit SCSI bus has to be terminated by the last device connected to the cable which is plugged in JP3.

3. JP3 and JP4 are bridged, and J14 is plugged.



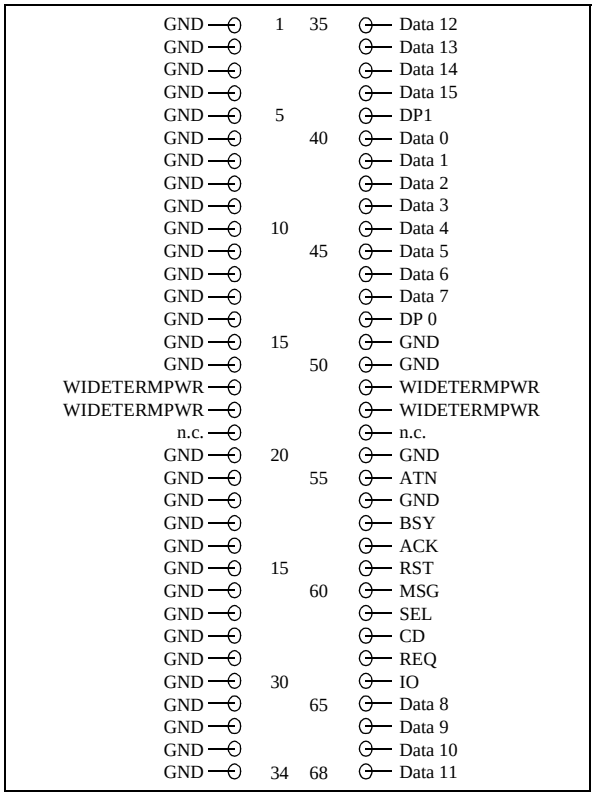
   The ultra/wide-SCSI bus has to be terminated by the last device connected to the cable which is plugged in J14.

Figure 16 SCSI (8 bit) out (JP3) and SCSI (8 bit) in (JP4)



50-pin header

Figure 17 Ultra/wide SCSI (J14)



68-pin fine pitch connector

Product Error Report

PRODUCT:	SERIAL NO.:
DATE OF PURCHASE:	ORIGINATOR:
COMPANY:	POINT OF CONTACT:
TEL.:	EXT.:
ADDRESS: _____ _____ _____	
PRESENT DATE:	
AFFECTED PRODUCT: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS	AFFECTED DOCUMENTATION: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS
ERROR DESCRIPTION: _____ _____ _____ _____ _____ _____ _____ _____ _____ _____	

THIS AREA TO BE COMPLETED BY FORCE COMPUTERS:

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