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PENT/CPCI-735R2/736R2 Family

Reference Guide

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Using This Guide

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), Compact Peripheral Component Interconnect (CPCI), and telecommunications.

Style Conventions

Notation	Description
1234	All numbers are decimal numbers except when used with the notations described below
00000000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal point indicator is signaled
Bold	Character format used to emphasize a word
`Courier`	Character format used for on-screen output
`Courier+Bold`	Character format used to characterize user input
Italics	Character format for references, table, and figure descriptions
<text>	Typical notation used for variables and keys
[text]	Typical notation for buttons
...	Repeated item
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges
:	Extents
|	Logical OR

Notation	Description
Note:	No danger encountered. Pay attention to important information marked using this layout.
Caution 	Possibly dangerous situation: slight injuries to people or damage to objects possible
Danger 	Dangerous situation: injuries to people or severe damage to objects possible

Product Naming Conventions

The following product names are used in this documentation:

Product Name Used	Description
CPCI-735R2	PENT / CPCI-735R2 / 736R2 Family and the standard board variant
CPCI-735AR2	Board variant with Ethernet via front panel
CPCI-736R2	PICMG 2.16 compliant variant with Ethernet via CPCI connector

Abbreviations

BCD	Binary-Coded Decimal
BIB	Board Information Block
BIOS	Basic Input Output System
BMC	Base Board Management Controller
CMOS	Complementary Metal Oxide Semiconductor
CPCI	Compact Peripheral Component Interconnect
CPU	Central Processing Unit
DHC	Dual Host Controller
DRAM	Dynamic Random Access Memory
ESD	Electrostatic Discharge

FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit
GND	Ground
HSC	Hot-Swap Controller
IDE	Integrated Device Electronics
ICMB	Intelligent Chassis Management Bus
IPMB	Intelligent Peripheral Management Bus
IPMI	Intelligent Platform Management Interface
ITE	Informationstechnische Einrichtung
KSC	Keyboard Controller Style
LED	Light Emitting Diode
LFM	Linear Feet per Minute
NMI	Nonmaskable Interrupt
PCI	Peripheral Component Interconnect
PM	Peripheral Management Controller
POST	Power-On Self-Test
PSU	Power Supply Unit
RAM	Random Access Memory
ROM	Read-Only Memory
RTB	Rear Transition Board
SBC	Single-Board Computer
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SEL	System Event Log
SMB	Serial Management Bus
SPP	Standard Parallel Port
SRAM	Static RAM
TPE	Twisted-Pair Ethernet
VGA	Video Graphics Adapter

Revision History

Order No.	Revision	Date	Description
215764	AA	January 2002	Preliminary Installation Guide
215764	AB	May 2002	Removed “Product Naming Conventions” from Preface, modified “EMC” page xxi and “EMV” page xxv, corrected safety note in “Installation in a Powered System” page 2-20, “Hot Swap” page xxiii and page xxvii, replaces NVRAM by SRAM in Figure 1 “Function Blocks” page 1-5, added information on IDE flash disk in “About this Manual” page 1-3, corrected “Standard Compliances” page 1-7, added note to “Standard Compliances” page 1-7 and “Board Installation” page 2-19, modified “Order Numbers” page 1-8, added step to “Action Plan” page 2-3, added safety note to “Environmental Requirements” page 2-5, modified Table 4 “Power Requirements” page 2-7, added information to “Rear Transition Board” page 2-14, modified note in “Connectors” page 3-7 and “J5” page 3-12, corrected list in “J3” page 3-10 and “J4” page 3-11, corrected Figure 21 “IDE Connector Pinout” page3-13, corrected pin 21 row B in Figure 19 “J5 Connector Pinout, Rows A-C” page3-12, added README.1ST to list in “Update Procedure” page 4-11, corrected information on IDE flash disk and CompactPCI bus in “Block Diagram” page 5-3, added information to “IPMI Controller” page 5-15, corrected CIB byte size in Table 18 “Devices on I2C Bus” page 5-21, changed name of Figure “IPMI System Interface for Intelligent Devices” to “Communication with Intelligent Devices” in IPMI chapter,

Order No.	Revision	Date	Description
215764	AB	May 2002	changed name of Figure “IPMI System Interface for Non-Intelligent Devices” to “Communication with Non-Intelligent Devices” in IPMI chapter, corrected Table 25 “SRAM Configuration Register” page 6-9
217572	AA	October 2002	Changed manual type from Installation Guide to Reference Guide, removed IPMI chapter, modified “Other Sources of Information” page xix, modified “Order Numbers” page 1-8, modified “SMB Interface” page 5-9, added information to “IPMI Controller” page 5-15, added information to “Overview” page 6-3, added Table 20 “Overview of IPMI Related Register Signals” page 6-4, added IPMI_CS2 to Table 21 “I/O Address Ranges” page 6-5, added information on “IPMI IRQ Register” page 6 -26, editorial changes
217761	AA	January 2003	Added 1.2 GHz variants to “Order Numbers” page 1-8, added note and updated Temperature in Table 3 “Environmental Requirements” page 2-5, added note that BIOS does not support booting from USB to section “Selecting The Boot Device” page 4-5, added information on keyboard configuration etc. to section “Requirements” page 4-8, added USB version number to section “USB” page 5-9, added note that temperature sensor is not IBMU powered to section “Temperature Sensor” page 5-16, editorial changes
220455	AA	March 2003	Corrected Table 4 “Power Requirements” page 2-7
220455	AB	May 2003	Changed cable name in section “Requirements” page 4-8 of Serial Console Redirection section

Order No.	Revision	Date	Description
221091	AA	June 2003	Removed order numbers of Force documentation from “Other Sources of Information” page xix Modified description of switches SW2-1 and SW2-2 in Table 7 “Default Settings” page 2-16; added null modem adapter to requirement list in “Serial Console Redirection” page 4-8; deleted entry “BIB (MEM-735 I2C memory)” from Table 18 “Devices on I2C Bus” page 5-21; added “I2C Addresses” page 5-20; Corrected Table 14 “System Management I2C Bus” page 5-10
221843	AA	October 2003	Modified Table 1 “Standard Compliance” page 1-7; modified Figure 6 “Location of Switches” page 2-15; modified “Via Setup” page 4-5 and Figure 26 “Boot Device Order” page 4-5
221843	AB	December 2003	Modified description of switch SW3-2 in Table 7 “Default Settings” page 2-16
221843	AC	January 2004	Added section “PMC Connectors” page 3-14
221843	AD	June 2004	Corrected description of bit 7 of the SRAM Configuration Register on page 6-9
221843	AE	November 2004	Modified description of bits 5, 6 and 7 of the Hardware Configuration Register on page 6-15
228499	AA	December 2005	Changed to Motorola-compliant format
6806800B25	A	July 2006	Added section “Comments and Suggestions” page 1-4 Modified section “Standard Compliances” page 1-7

Other Sources of Information

For further information refer to the following documents and data sheets of the mentioned devices. Motorola user manuals can be downloaded from the Motorola literature catalog.

Company/Org.	www.	Document
Motorola	motorola.com/computers	Sentinel Rev. 1 Reference Guide)
		IPMI Reference Guide
		PENT/MEM-735 Installation Guide
		ACC/RTB-735R2/736R2 Installation Guide
		CPCI-735/HD-AccKit Installation Guide
Intel	http://developer.intel.com	Ethernet 82559ER
		Pentium III-M
		User Flash E28F320J3
Micron	micron.com	BIOS Flash 28F800B3
National Semiconductor	national.com	Super I/O PC97317
PCI Industrial Computer Manufacturers Group	picmg.com	System Management Specification PICMG 2.9 R1.0
Samsung	samsung.com	Flash Disc Controller KS32P6632-LC/TX
Server Works	serverworks.com	Northbridge CNB30LE
		Southbridge OSB4
Texas Instruments	ti.com	PC Card Controller PCI1410
		Serial Controller TL16C550C

Company/Org.	www.	Document
XICOR	xicor.com	Serial EEPROM 24C02
		Serial EEPROM 24C04
-	http://developer.intel.com/design/servers/ipmi/spec.htm	IPMI specification V. 1.0.



Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PENT/CPCI-735R2/736R2 Family.

We intend to provide all necessary information to install and handle the PENT/CPCI-735R2/736R2 Family in this Reference Guide. However, as the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Motorola representative.

The PENT/CPCI-735R2/736R2 Family has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Motorola or persons qualified in electronics or electrical engineering are authorized to install, maintain, and operate the PENT/CPCI-735R2/736R2 Family. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a standard Motorola system according to PCI specification and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules respectively EN 55022 Class A and EN 55024. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial, business or industrial environment.

The board generates and uses radio frequency energy and, if not installed properly and used in accordance with this Reference Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If you use the board without a PMC module, cover empty slots with blind panels to ensure proper EMC shielding. If boards are integrated into open systems, always cover empty slots.



Installation

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life. Therefore:

- **Before touching boards or electronic components, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or removing an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the CompactPCI backplane via all assembled connectors and that power is available on all power pins.**

Operation

While operating the board ensure that the environmental and power requirements are met.

Do not operate the board outside the specified environmental limits. High humidity and condensation may cause short circuits. Make sure the board is completely dry and there is no moisture on any surface before applying power. Do not operate the board below 0 °C.

When operating the board in areas of electromagnetic radiation ensure that the board is bolted on the CompactPCI system and the system is shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

To prevent damage to the board, do not change the switch settings while the board is operating but before board installation.



Hot Swap

Never remove the board from a system under hot-swap conditions unless a hot-swap or high-availability platform is used and the documentation of all installed boards and the system documentation explicitly include appropriate guidelines. For the hot-swap support of the board in a system slot, check the system documentation.

Removing the board from a powered system with IDE devices attached to the board's secondary IDE interface may result in data losses.

As long as the hot-swap LED is off, the board is in normal operation and must not be removed.

Replacement/Expansion

Only replace or expand components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMC and the possibly changed functionality of the product.

The total max. power consumption per PMC slot at +/–12V, 5V and 3.3V level must not exceed 7.5W (total overall used voltages).

If the standard CPCI-735/HD-AccKit is installed, the operating and storage temperature of the board is limited by the maximum operating temperature of the hard disk. If the maximum temperature of the hard disk is lower than the one of the board, the maximum temperature specified for the hard disk must not be exceeded.

RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted-pair Ethernet (TPE) connectors. Mismatching the two connectors may destroy your telephone as well as the board. Therefore:

- **TPE connectors near your working area have to be clearly marked as network connectors.**
- **TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The length of the electric cable connected to a TPE bushing must not exceed 100 meters.**

If you have further questions, ask your system administrator.



Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, backup affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is installed.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation, if possible in an environmentally acceptable way.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Einbau, Betrieb und Wartung des PENT/CPCI-735R2/736R2 Family zu beachten sind.

Wir sind darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem PENT/CPCI-735R2/736R2 Family in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem PENT/CPCI-735R2/736R2 Family um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Ihnen Informationen fehlen sollten, wenden Sie sich bitte an Ihren Vertreter von Force Computers.

Das PENT/CPCI-735R2/736R2 Family erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Force Computers ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

EMV

Das Board wurde entsprechend der PCI Spezifikation in einem Force Computers Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A und EN 55024. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Boards in Gewerbe- sowie Industriegebieten gewährleisten.

Das Board arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.



Wenn Sie das Board ohne ein PMC-Modul verwenden, schirmen Sie freie Steckplätze mit einer Blende ab, um einen ausreichenden EMV Schutz zu gewährleisten. Wenn Sie Boards in Systeme einbauen, schirmen Sie freie Steckplätze mit einer Blende ab.

Installation

Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Beachten Sie deshalb die folgenden Punkte:

- **Bevor Sie Boards oder elektronische Komponenten berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie bei Ein- oder Ausbau des Boards nicht auf die Frontblende, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Ein- oder Ausbau von zusätzlichen Geräten oder Modulen das dazugehörige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die CompactPCI Backplane angeschlossen ist und Spannung an allen Versorgungskontakten anliegt.**

Betrieb

Achten Sie darauf, dass die Umgebungs- und die Leistungsanforderungen während des Betriebs eingehalten werden.

Betreiben Sie das Produkt nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur, da durch hohe Luftfeuchtigkeit Kurzschlüsse entstehen können. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Produkt kein Kondensat befindet und betreiben Sie das Produkt nicht unter 0°C.

Wenn Sie das Board in Gebieten mit elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Board mit dem CompactPCI System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Stellen Sie sicher, dass Anschlüsse und Kabel des Boards während des Betriebs nicht berührt werden können.

Um Schäden am Board zu vermeiden, ändern sie die Schaltereinstellungen nicht während des Betriebs sondern vor der Installation.



Hot Swap

Ein- oder Ausbau des Boards in einem System unter Hot-Swap-Bedingungen darf nur dann stattfinden, wenn die Basic Hot Swap Plattform, die Full-Hot-Swap Plattform, oder die High-Availability Hot-Swap-Plattform benutzt wird und die Systembeschreibung dies ausdrücklich erlaubt. In der Systembeschreibung finden Sie die Informationen über die Unterstützung von Hot Swap, wenn sich das Board in einem Systemsteckplatz befindet.

Wenn Sie das Board, an dem an der zweiten IDE Schnittstelle Komponenten angeschlossen sind, aus einem laufenden System entfernen, kann dies zu Datenverlusten führen.

Leuchtet die Hot-Swap-LED nicht, so befindet sich das Board in normalem Betrieb und darf auf keinen Fall entfernt werden.

Austausch/Erweiterung

Verwenden Sie bei Austausch oder Erweiterung nur von Force Computers empfohlene Komponenten und Systemteile. Andernfalls sind Sie für mögliche Auswirkungen auf EMV und geänderte Funktionalität des Produktes voll verantwortlich.

Der Gesamtleistungsverbrauch pro PMC Modul bei +/-12V, 5V und 3,3V darf 7,5W nicht übersteigen (Gesamtheit aller Spannungen).

Ist das Standard CPCI-735/HD-AccKit installiert, wird die Höchsttemperatur des Boards durch die Höchsttemperatur der Festplatte bestimmt. Liegt die Höchsttemperatur der Festplatte unter der des Boards, darf die für die Festplatte festgelegte Höchsttemperatur nicht überschritten werden.



RJ-45 Stecker

Das CPU Board ist mit RJ-45 Steckern ausgestattet. Dieser Stecker wird sowohl für Telefonanschlüsse als auch für Netzwerkkabel (Twisted Pair Ethernet - TPE) verwendet. Die Verwechslung dieser Anschlüsse kann sowohl das Telefon als auch das Board zerstören. Beachten Sie deshalb folgende Punkte:

- **Vergewissern Sie sich, dass Anschlüsse an Ihrem Arbeitsplatz deutlich als Netzwerkanschlüsse gekennzeichnet sind.**
- **Schließen Sie TPE-Stecker/Netzwerkstecker Ihres Systems nur an Sicherheits-Kleinspannungs-Kreise (SELV) an.**
- **Vergewissern Sie sich, dass die an einem TPE-Anschluss angeschlossene Leitung eine Gesamtlänge von 100 Metern nicht überschreitet.**

Falls Sie Fragen haben, wenden Sie sich an Ihren Systemadministrator.

Batterie

Muss eine Lithiumbatterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithiumbatterien kann zu lebensgefährlichen Explosionen führen.**
- **Tauschen Sie die Batterie aus bevor fünf Jahre reine Betriebsdauer vorüber sind.**
- **Der Austausch der Batterie bringt immer einen Datenverlust bei den Komponenten mit sich, die sich durch die Batterie die Stromversorgung sichern. Sichern Sie deshalb vor dem Batteriewechsel Ihre Daten.**
- **Verwenden Sie beim Batteriewechsel immer den selben Batterietyp, der bereits eingesetzt wurde.**

Umweltschutz

Entsorgen Sie alte Boards gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich immer umweltfreundlich.

1

Introduction

About this Manual

This reference Guide provides the information that you need to install, access and operate the board.

Organization of this Manual

The Reference Guide is organized as follows:

Chapter	Description
Using This Guide	Lists all conventions and abbreviations used in this manual and outlines the revision history
Other Sources of Information	Lists related documentation and specifications
Safety Notes	Provides safety relevant information when handling the board
Sicherheitshinweise	German translation of the Safety Notes chapter
Introduction	Provides an overview of the features, the standard compliances, and the order information.
Installation	Outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures
Controls, Indicators, and Connectors	Describes the front panel, the LEDs, keys, and connectors
BIOS	Describes the configuration settings, the boot device selection, booting via network, serial console redirection, updating the BIOS and the BIOS messages.
Buses	Provides detailed information about the buses
Maps and registers	Provides an overview of the I/O and memory maps and describes all board-specific registers.
Battery Exchange (Appendix)	Describes how to exchange the on-board battery
Troubleshooting (Appendix)	Describes how to deal with problems related to the operation of the board

Comments and Suggestions

We welcome and appreciate your comments on our documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

- Motorola GmbH
  Embedded Communications Computing
  Lilienthalstrasse 15
  85579 Neubiberg
  Germany
- ECCRC@motorola.com

In all your correspondence, please list your name, position, and company. Be sure to include the title, part number, and revision of the manual and tell how you used it.

Features

The PENT / CPCI-735R2 / 736R2 Family is a universal board using the Motorola SENTINEL universal bridge technology. As it is based on an Intel Mobile Processor-M of 800 MHz and higher, the PENT / CPCI-735R2 / 736R2 Family offers high performance. Combined with full hot-swap capabilities the PENT / CPCI-735R2 / 736R2 Family is an ideal component for multi-node processor systems.

Other important improvements of the PENT / CPCI-735R2 / 736R2 Family are:

- Assembly variants with either two 100BaseT Ethernet controllers at the front or at the rear or via CompactPCI connector (PICMG 2.16 or RTB)
- More memory: Up to 2 GBytes SDRAM in a single CompactPCI slot
- One 64-bit / 66 MHz PMC interface
- IPMI (Intelligent Platform Management Interface) support
- IDE flash disk (assembly option)

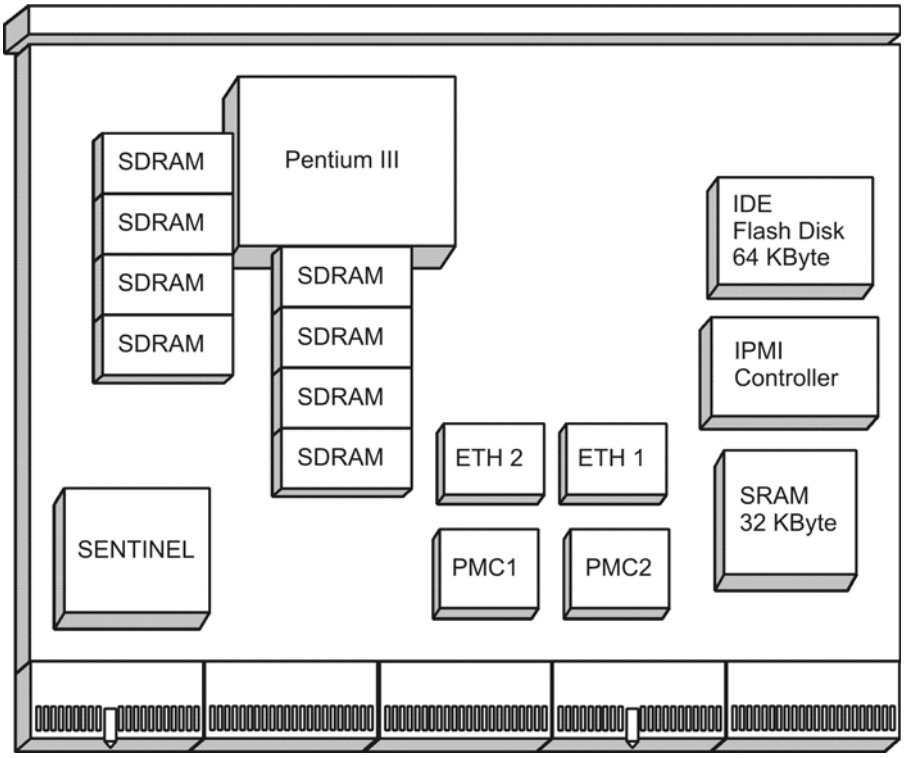


Figure 1: *Function Blocks*

Variants

The PENT/CPCI-735R2/736R2 Family comes in three main assembly variants:

Name	Description
CPCI-735R2	PMC slots 1 (64 bit) and 2 (32 bit) accessible, assembly option for hard disk, RTB required for two Ethernet interfaces at CompactPCI connector J5
CPCI-735AR2	PMC slot 1 (64 bit) accessible, assembly option for hard disk, two Ethernet interfaces at front panel, transformers for Ethernet ports
CPCI-736R2	PMC slots 1 (64 bit) and 2 (32 bit)[1)] accessible, assembly option for hard disk, Ethernet interfaces at CompactPCI connector J3 (PICMG 2.16)

1) PMC slot 2 is not compliant to the PMC Specification since the transformer necessary for PICMG support 2.16 is assembled under the I/O connectors of the PMC module. Only PMC modules where this connector is not assembled and which have front I/O access can be used.

Standard Compliances

The PENT/CPCI-735R2/736R2 Family meets the following standards:

Note: EN 55022 Class A and FCC Part 15 Class A are achieved by using single-point grounding. If you ground the board at multiple points, EMC problems may occur.

Table 1: *Standard Compliance*

Standard	Description
EN 60950-1 IEC 60950-1 CSA 60950-1 UL/cUL 60950-1 (predefined Motorola system)	Legal safety requirements
EN 61000-6-2 EN55022 EN55024 FCC Part 15 Class A	EMC requirements on system level
ANSI/IPC-A610 Rev.C Class 2 ANSI/IPC-7711 ANSI/IPC-7721 ANSI-J-001...003	Manufacturing requirements

Ordering Information

When ordering the PENT/CPCI-735R2/736R2 Family board variants, upgrades and accessories, use the order numbers given below.

Product Nomenclature

In the following you find the key for the product name extensions.

PENT/CPCI-735R2/736R2 Family/xxxx-ccc-Lyyy-zz	
xxxx	DRAM size in MByte
ccc	Processor type and clock frequency in MHz
Lyyy	L2 cache capacity in KByte
zz	Flash disk capacity in MByte

Order Numbers

Depending on the PENT/CPCI-735R2/736R2 Family type, the available upgrades and accessories may differ. Consult your local sales representative to check the possibility of combinations.

Table 2: *Ordering Information Excerpt*

Order No.	PENT/CPCI-...	Description
110714	...735R2/512-800-L512-0	Intel Processor-M, 800 MHz with 512 MByte main memory, 512 KByte 2nd level cache
110715	...735AR2/512-800-L512-0	Intel Processor-M, 800 MHz with 512 MByte main memory, 512 KByte 2nd level cache
110958	...735AR2/1G-800-L512-0	Intel Processor-M, 800 MHz with 1 GByte main memory, 512 KByte 2nd level cache
110712	...736R2/512-800-L512-0	Intel Processor-M, 800 MHz with 512 MByte main memory, 512 KByte 2nd level cache
111035	...735R2/1G-800-L512-0	Intel Processor-M, 800 MHz with 1 GByte main memory, 512 KByte 2nd level cache

Table 2: *Ordering Information Excerpt (cont.)*

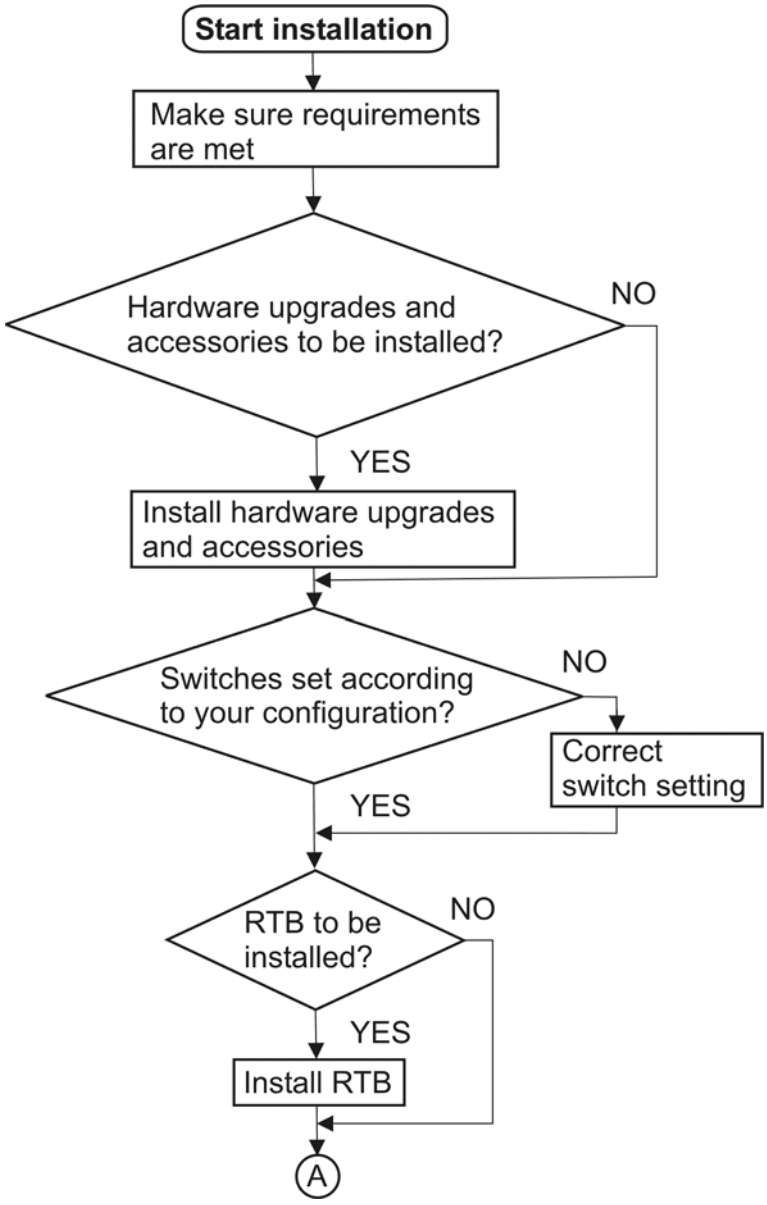
Order No.	PENT/CPCI-...	Description
111335	...735R2 / 512-1200-L512-0	Intel Processor-M, 1.2 GHz with 512 MByte main memory, 512 KByte 2nd level cache
111336	...735AR2 / 512-1200-L512-0	Intel Processor-M, 1.2 GHz with 512 MByte main memory, 512 KByte 2nd level cache
111337	...736R2 / 1G-1200-L512-0	Intel Processor-M, 1.2 GHz with 1 GByte main memory, 512 KByte 2nd level cache
Hardware Accessories		
109895	ACC / RTB-735R2	Rear transition board for CPCI-735R2 and related installation components
109896	ACC / RTB-736R2	Rear transition board for CPCI-736R2 and related installation components
109374	PENT / MEM-735 / 1G-ACC-KIT	Memory module and related installation components
110130	PENT / CPCI-7xx / CABLE-ACCKIT	Split cable for keyboard / mouse, cable for serial interface
Software Accessories		
105757	PENT / NT-Support-Package	Windows NT drivers

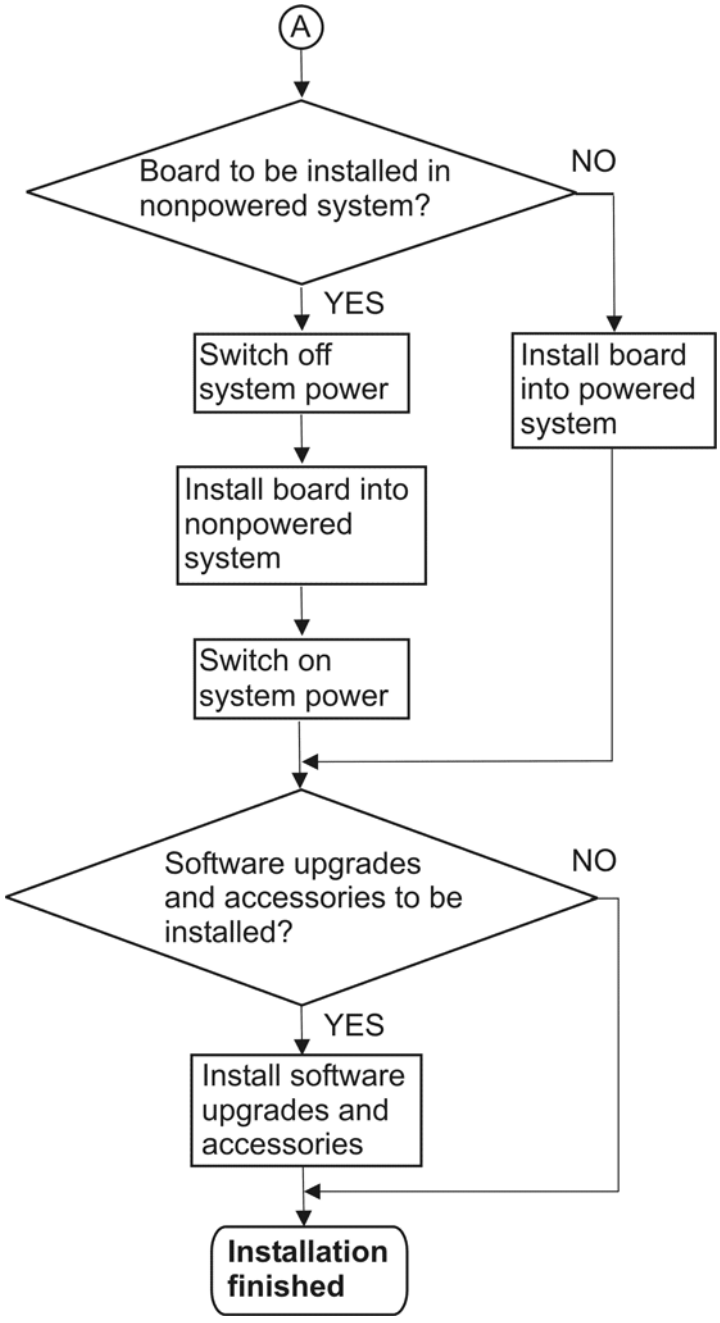
2

Installation

Action Plan

To install the board, the following steps are necessary and described in detail in the following sections of this chapter.




A
Board to be installed in nonpowered system?
NO
YES
Switch off system power
Install board into powered system
Install board into nonpowered system
Switch on system power
Software upgrades and accessories to be installed?
NO
YES
Install software upgrades and accessories
Installation finished

Requirements

To meet the environmental requirements, the board has to be tested in the system where it is to be installed. Before you power up the board, calculate the power needed according to your combination of board upgrades and accessories.

Environmental Requirements

The environmental values must be tested and proven in the used system configuration. The conditions listed below refer to the surroundings of the board within the user environment.

Note:

- **Operating temperatures refer to the temperature of the air circulating around the board and not to the component temperature.**
- **Operating temperatures of the 1.2 GHz board variants are lower than the Motorola standard temperature requirements. They are limited to 50°C.**

Caution



Do not operate the board outside the specified environmental limits. High humidity and condensation may cause short circuits. Make sure the board is completely dry and there is no moisture on any surface before applying power. Do not operate the board below 0°C.

Table 3: *Environmental Requirements*

Requirement	Operating	Non-Operating
Temperature 800 MHz variant: 1.2 GHz variant:	 0°C to +55°C 0°C to +50°C (may be further limited by type of hard disk)	 –40°C to +85°C –40°C to +85°C
Forced air flow	300 LFM	–
Temp. change	+/– 0.5°C / min	+/– 1°C / min
Rel. humidity	5% to 95% non-condensing at +40°C	5% to 95% non-condensing at +40°C

Table 3: *Environmental Requirements*

Requirement	Operating	Non-Operating
Altitude	–300 m to +3,000 m	–300 m to +13,000 m
Vibration 10 to 15 Hz 15 to 150 Hz	 2 mm amplitude 2 g	 5 mm amplitude 5 g
Shock	5 g / 11 ms halfsine	15 g / 11 ms halfsine
Free fall	100 mm / 3 axis	1,200 mm / all edges and corners (packed state)

Power Requirements

The board's power requirements depend on the installed hardware accessories. The following table gives examples of typical power requirements for 5V and 3.3V for a processor running at 800 MHz and 1.2 GHz without any accessories. If you want to install any accessories, the load of the respective accessory has to be added to the load of the used board variant.

For information on the accessories' power requirements, refer to the documentation coming with the respective accessory or ask your local Motorola representative.

Table 4: *Power Requirements*

Variant	**800 MHz**		**1.2 GHz**	
Requirement	**+5V**	**+3.3V**	**+5V**	**+3.3V**
Typical power requirements	16 W	6.9 W	23.5 W	7.3 W
Min. voltage	+4.85V	+3.2V	+4.85V	+3.2V
Max. voltage	+5.25V	+3.46V	+5.25V	+3.46V
Max. current	3.2A	2.1A	4.7A	2.2A
Board in idle state	1.6A	1.4A	1.8A	1.4A

Hardware Upgrades and Accessories

The PENT/CPCI-735R2/736R2 Family itself allows an easy and cost-efficient way to adapt the board to your application needs.

The following table gives an overview on the possible accessories, described in Table 2 “Ordering Information Excerpt” page 1-8. For the respective board variant, x indicates that the accessory can be used, - indicates that the accessory cannot be used and a number indicates the available PMC slot.

Table 5: *Possible On-Board Upgrades and Accessories*

Variant	Mem. Module	PMC	HD	RTB-735R2
CPCI-735R2	x	1+2	x	x
CPCI-735AR2	x	1	x	x
CPCI-736R2	x	1+2[1)]	x	x

1) PMC slot 2 is not compliant to the PMC Specification since the transformer necessary for PIGMIC support 2.16 is assembled under the I/O connectors of the PMC module. Only PMC modules where this connector is not assembled and which have front I/O access can be used.

The following tables gives an overview on the possible combinations of the upgrades and accessories.

Table 6: *Possible On-Board Upgrades and Accessories Combinations*

Option	Mem. Mod.	PMC	HD
Mem. Module	-	Mem.: slot 1 PMC: slot 2	Mem.: slot 1 HD: slot 2
PMC	PMC: slot 2 Mem.: slot 1	1 PMC: slot 1 1 PMC: slot 2	PMC: slot 1 HD: slot 2
HD	HD: slot 2 Mem.: slot 1	HD: slot 2 PMC: slot1	-

Memory Module

The memory module PENT/MEM-735 with SDRAM chips provides additional memory for the board. It is connected to the 133 MHz memory bus. The memory module is available as 1 GByte variant. The maximum possible memory size can be 2 GByte.

For installation information, refer to the *PENT/MEM-735 Installation Guide.*

PMC Module

All three board variants provide PMC slot 1. It supports either a 32- or a 64-bit data bus width with a frequency of either 33 MHz or 66 MHz. PMC Slot 1 provides user I/O signals at connector J3.

The CPCI-735R2 and, with limitation, the CPCI-736R2 additionally provides PMC slot 2. It supports a 32-bit data bus width with a maximum frequency of 33 MHz. PMC Slot 2 provides user I/O signals at connector J4.

Both PMC slots provide +/–12V and can be used to install a standard PMC module.

Note:

- **To ensure proper EMC shielding, either operate the board with the blind panels for the front panel or with the modules installed.**
- **If the board is upgraded, ensure that the blind panels are stored in a safe place in order to be used again when removing the upgrades.**

Voltage Key

PMC slot 1 provides a 3.3V PCI interface. Therefore, a voltage key for 3.3V is assembled at PMC slot 1.

PMC slot 2 provides a 5V-only PCI interface. The voltage key prevents 3.3V PMC modules from being plugged into PMC slot 2.

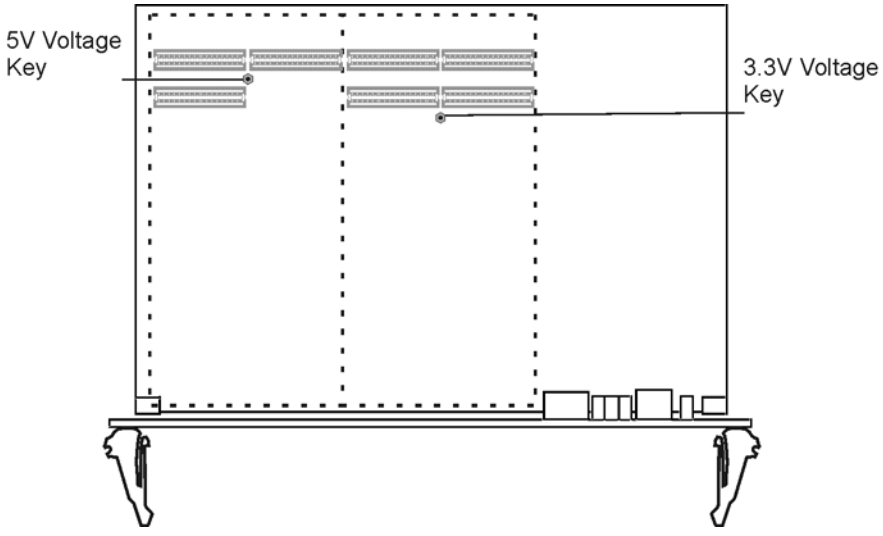


Figure 2: *Voltage Key*

Installation Procedure

1. Remove memory module from PMC slot 1 or remove hard disk from PMC slot 2, if necessary
   For removal information, refer to the *PENT/MEM-735 Installation Guide* and to the *CPCI-735/HD-AccKit Installation Guide.*
2. Remove blind panel of respective PMC slot from front panel
3. Store blind panel in a safe place

Caution



The max. power consumption per PMC slot at +/–12V, 5V and 3.3V level must not exceed 7.5W (total overall used voltages).

4. Plug PMC module into connectors of PMC slot 1 (PN11, 12, 13, 14) or PMC slot 2 (PN21, 22 and 24)

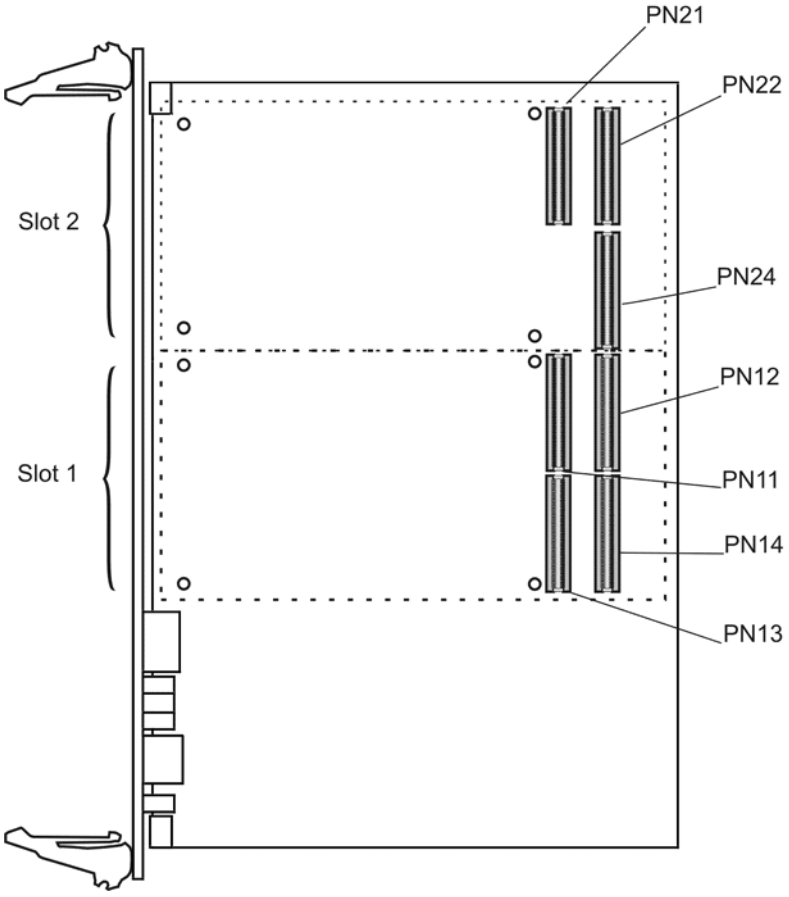


Figure 3: *PMC Connectors and Slots*

5. Check whether the standoffs of the module cover the mounting holes of the board

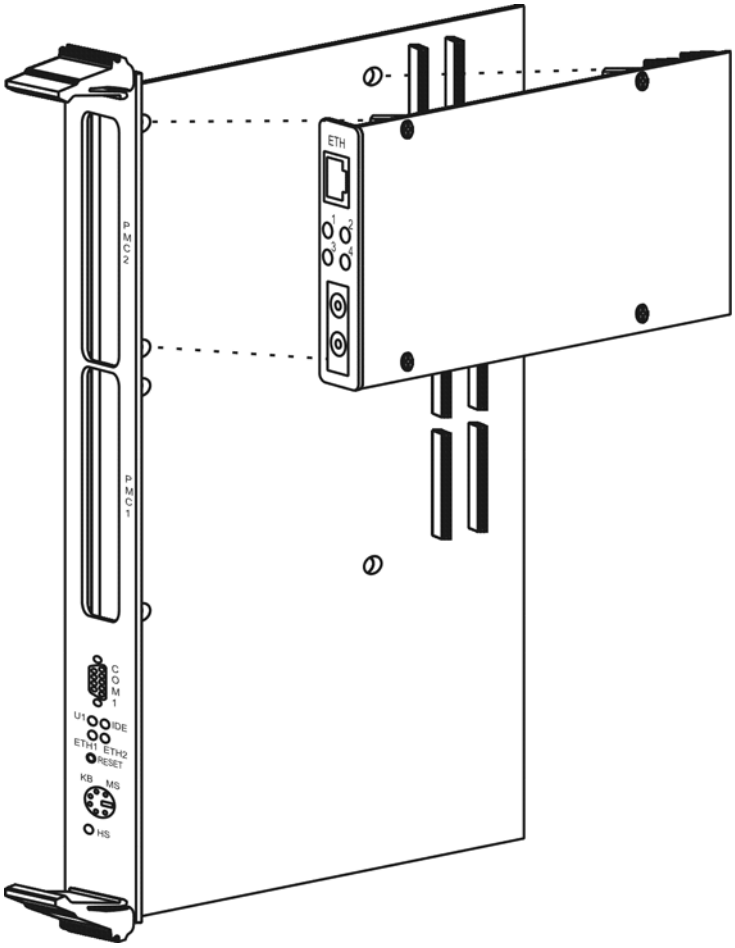


Figure 4: *Position of Mounting Holes*

6. Place screws delivered with PMC module into mounting holes
7. Fasten screws

Removal Procedure

1. Remove screws
2. Disconnect PMC module carefully from slot
3. Close front panel gap at free slot with blind panel

IDE Devices

It is possible to have up to two IDE devices on the board which are connected to the primary IDE interface:

- As assembly option a flash disk can be installed
- A hard disk can be connected via on-board connector

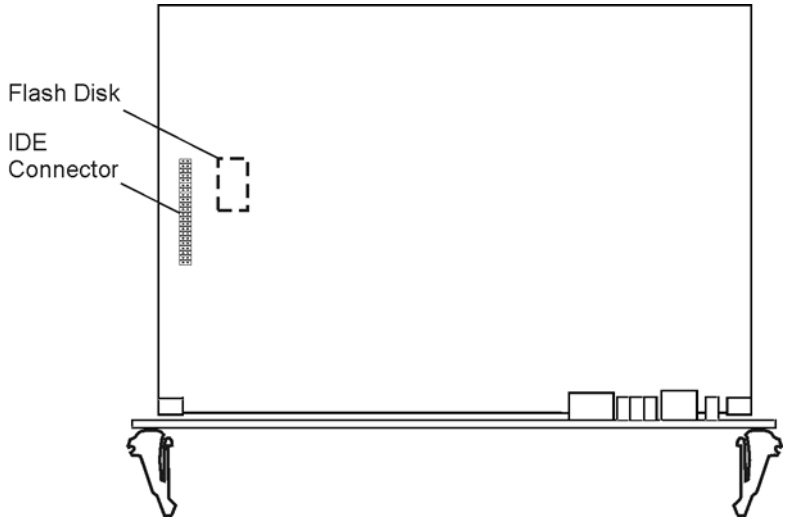


Figure 5: *Flash Disk and IDE Connector*

Note: Never connect more than two devices to the primary IDE interface.

If only one device is connected to the primary IDE interface, it must be the master. If two devices are connected, one must be the master, the other one must be the slave. The flash disk can be configured as IDE master (device 0) or IDE slave (device 1) via switch SW2-2 (see Table 7 “Default Settings” page 2-15).

Further devices can be connected to the secondary IDE interface via a rear transition board. For further information, refer to the *ACC/RTB-735 Installation Guide.*

At the first boot after connecting an IDE device use the appropriate menu in setup to modify the BIOS parameters appropriately (see “Selecting The Boot Device” page 4-5).

Hard-Disk Drive Accessory Kit

The Motorola's hard-disk accessory kit CPCI-735/HD-AccKit provides a local mass storage device. It can be connected to the primary IDE port via the on-board connector.

For installation information, refer to the *CPCI-735/HD-AccKit Installation Guide.*

Caution



If the standard CPCI-735/HD-AccKit is installed, the operating and storage temperature of the board is limited by the maximum operating and storage temperature of the hard disk. If the maximum temperature of the hard disk is lower than the one of the board, the maximum temperature specified for the hard disk must not be exceeded. For information on the allowed hard-disk operating temperature, consult the *CPCI-735/HD-AccKit Installation Guide.*

Rear Transition Board

As a separate price list item, a rear transition board, the ACC/RTB-735R2/736R2, is offered. The RTB provides access to the CPU board's CompactPCI user I/O interfaces via industry standard connectors. In addition to the IPMI specification, IPMB1 and ICMB are available at the CPU board's J5 connector. They can be accessed only via the RTB's IPMB1 and ICMB connectors.

In order to use the ICMB support of IPMI, you need the RTB for connecting the BMCs of two or more chassis.

For further information, refer to *IPMI Reference Guide* or to the *ACC/RTB-735R2/736R2 Installation Guide.*

Note: Only use the ACC/RTB-735R2/736R2 for boards of the PENT/CPCI-735R2/736R2 Family.

Switch Settings

The board provides four configuration switches, SW1,SW2, SW3 and SW4.

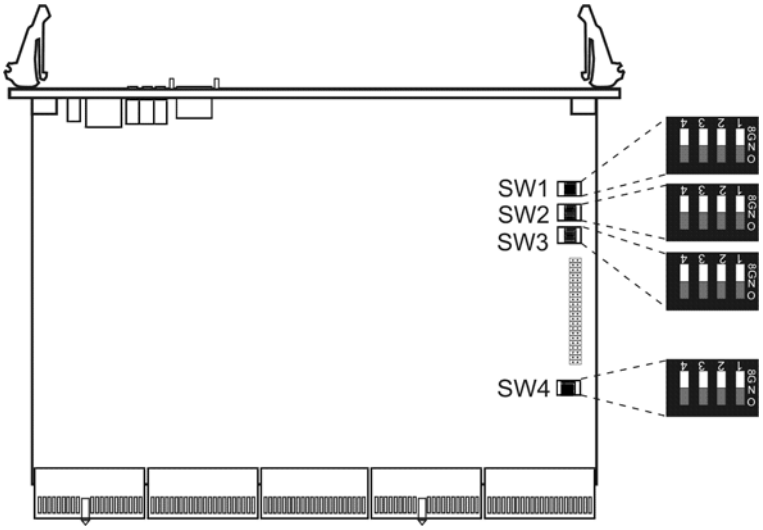


Figure 6: *Location of Switches*

The board is delivered with the white switches set to the default position.

Caution



- **If the board is to be used in a Motorola' system, check whether the System's Guide contains information on system-specific switch settings of the board.**
- **Do not change switch setting of switches marked as 'reserved' for they might carry production-related functions which could cause the board to malfunction.**
- **In order to prevent damage to the boot block do not change the flash memory boot block write protection unless it is explicitly stated.**
- **To prevent damage to the board, do not change switch settings while the board is operating.**

Table 7: *Default Settings*

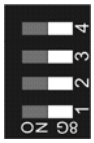
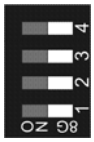
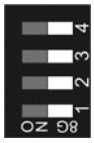
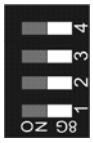
Switch	Number	Description
SW1		
	1	BIOS crisis recovery (BIOS update)[1)] OFF: Normal operation mode (default) ON: BIOS crisis recovery mode
	2	BIOS Flash memory boot block write protection OFF: Write-protected (default) ON: Write enabled
	3	Reserved OFF: Default
	4	Reserved OFF: Default
SW2		
	1	Reserved OFF: Default
	2	Reserved OFF: Default
	3	Reserved OFF: Default
	4	FORCE_PM OFF: IPMI controller in automatic mode (default)[2)] ON: IPMI controller acts as PM
SW3		
	1	Reserved OFF: Default
	2	Reserved OFF: Default
	3	PMC1 frequency OFF: Set by PMC module (default) ON: Set to 33 MHz
	4	Reserved OFF: Default

Table 7: *Default Settings*

Switch	Number	Description
SW4		
	1	Front panel reset key[3)] OFF: Reset key enabled (default) ON: Reset key disabled
	2	RTB reset key[3)] OFF: Reset key enabled (default) ON: Reset key disabled
	3	IPMI reset[3)] OFF: Reset enabled (default) ON: Reset disabled
	4	Watchdog OFF: Enabled (but not started) (default) ON: Disabled (cannot be started)

1) For further information, refer to the README file on the floppy disk for BIOS upgrade
2) The IPMI controller mode depends on whether the board is installed into a CPCI system as a peripheral or a system board:
As system board: BMC
As peripheral board: PM
3) If reset is disabled by switch, register settings have no effect

Board Installation

The board carries Motorola's SENTINEL PCI to CPCI Universal Bridge. With this technology the board is capable to run as System Controller in the CPCI system slot and as an intelligent I/O board in a peripheral slot.

The board provides hot-swap support, i.e it may be installed in or removed from a powered system. This section is divided into two subsections for installing the board in a non-powered system and in a powered system supporting hot swap.

Note: EN 55022 Class A and FCC Part 15 Class A are achieved by using single-point grounding. If you ground the CPCI-735R2 at multiple points, EMC problems may occur.

Installation in a Nonpowered System

Due to the hot-swap capability the board has been designed to run in a 5V Compact PCI System. A 5V key prevents the board from being installed into an otherwise specified CompactPCI rack.

Note:

- **Before installing the board install the upgrades and accessories, if necessary (refer to "Hardware Upgrades and Accessories" page 2-7).**
- **If memory modules have been installed, check that all socket locks of the board are closed before board installation.**

Installation Procedure

1. Turn off system power

Caution



Before touching integrated circuits, make sure that you are working in an ESD-safe environment.

2. Check switch settings for consistency (see "Switch Settings")

3. Plug in board depending on intended function either in system slot marked with a triangle or in peripheral slot marked with a circle
4. Press handles inwards to lock board on CompactPCI rack
5. Fasten board with screws
6. Plug in interface cables into front panel connectors, if applicable
7. Turn on system power

Removal Procedure

1. Turn off system power
2. Unfasten screws of front panel until board is detached from rack frame
3. Press handles outwards to disconnect board from backplane
4. Remove board from rails of slot position

Installation in a Powered System

The PENT / CPCI-735R2 / 736R2 Family supports full hot swap and high availability.

The basic purpose of hot-swap support and high availability is to allow the board to be installed and removed in a powered system without adversely affecting system operation. With hot-swap support, defective boards can be repaired and systems can be reconfigured without stopping system operation and with minimum operator interaction.

Caution



Never remove the board from a system under hot-swap conditions unless a hot-swap or high-availability platform is used and the documentation of all installed boards and the system documentation explicitly include appropriate guidelines. For the system hot-swap support of the board in a system slot, check the system documentation.

The board is fully compliant to CompactPCI Hot Swap Specification PICMG 2.1 R2.0 and can run in a 5V Compact PCI System. A 5V key in connector J1 prevents the board from being installed into an otherwise specified Compact PCI rack.

Signals

For information on board status concerning the hot-swap conditions, the board provides ENUM# and HEALTHY# signals for hot-swap-controller (HSC) notification and SENTINEL's Control and Status registers.

After installing the board into or before removing it from a powered system, the interrupt ENUM# signal is generated and passed to the system board of the CompactPCI system to indicate a service request. The Control and Status registers allow to determine the source of the ENUM# signal and to control the hot-swap LED. The HEALTHY# signal is active whenever all backplane and on-board voltages are within their operating range.

Control Elements

The board provides the following elements as man-machine interface:

- Hot-swap switch
  Integrated in the lower handle of the front panel, it allows the user to indicate the intention to remove the board.
- Blue hot-swap LED
  Indicates that you are allowed to remove the board.

Removal Procedure

Before removing the board, observe the following:

Caution



- **Never remove the board from a system under hot-swap conditions unless a hot-swap or high-availability platform is used and the documentation of all installed boards and the system documentation explicitly include appropriate guidelines. For the system hot-swap support of the board in a system slot, check the system documentation.**
- **Removing the board from a powered system with IDE devices attached to the board's secondary IDE interface may result in data losses.**
- **Before touching integrated circuits, make sure that you are working in an ESD-safe environment.**

The removal procedure depends on the system the board is to be removed from.

From Basic Hot-Swap System

1. Carry out software disconnection
2. Wait until software disconnection process has been completed
3. Open handles
4. Remove board from powered system

From Full Hot-Swap or High-Availability System

1. Press red button to unlock handles



Figure 7: *Button on Handle*

2. Open handles
   The hot-swap switch will be opened automatically.
3. Wait until blue hot-swap LED is illuminated

Caution



As long as the hot-swap LED is off, the board is in normal operation and must not be removed.

4. Remove board from powered system

Installation Procedure

Before installing the PENT / CPCI-735R2 / 736R2 Family, observe the following:

Caution



- **Only install the board under hot-swap conditions if the board is to be operated in slots for which hot swap is explicitly permitted by the system documentation (in most hot-swap systems peripheral slots only).**
- **Installation of the board under hot-swap conditions is only supported without IDE devices attached to the board's secondary IDE interface.**
- **Before touching integrated circuits, make sure that you are working in an ESD-safe environment.**

The installation procedure depends upon the system the board is to be installed in.

Into Basic Hot-Swap System

1. Check board configuration e.g. switch settings, additional memory modules
2. Check that you are using an appropriate rear transition board, if applicable
3. Insert board into powered system
4. Press handles inwards to lock board on CompactPCI rack
5. Carry out software connection according to system documentation

Into Full Hot-Swap or High-Availability System

1. Check board configuration e.g. switch settings, additional memory modules
2. Check that you are using an appropriate rear transition board, if applicable
3. Insert board into powered system
   The hot-swap LED stays blue until the board goes healthy.
4. Press handles inwards to lock board on CompactPCI rack

Software Upgrades and Accessories

The following software upgrades and accessories are offered for the PENT / CPCI-735R2 / 736R2 Family.

BIOS Upgrade

From the S.M.A.R.T. server you can download a zip file to create a floppy disk containing a BIOS upgrade file and upgrade utilities. For information on how to upgrade your BIOS, refer to the README file provided on your created BIOS upgrade disk.

NT-Support-Package

With the Pent / NT-Support-Package comes a CD-ROM with Windows NT drivers e.g. to extend hardware support for Windows NT such as an Ethernet driver.

For information on how to install the NT-Support-Package, refer to the README file on the CD-ROM.

3

Controls, Indicators, and Connectors

Front Panel

Two front panels are available:

- Standard front panel, providing two cutouts for PMC module 1 and 2
- Ethernet front panel, providing:
  - Cutout for PMC module 1
  - Two connectors for Ethernet 1 and 2
  - One USB connector

The standard front panel is used for both, CPCI-735R2 and CPCI-736R2, the Ethernet front panel is used for CPCI-735AR2.

The following figure shows the position of cutouts for PMC modules, connectors, LEDs and keys for the standard front panel (left) and the Ethernet front panel variant (right).

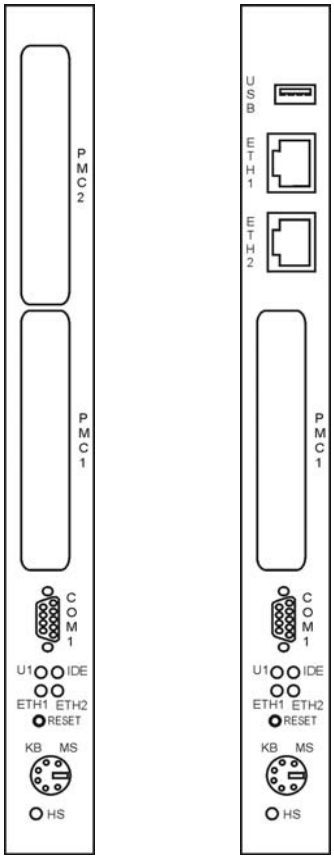


Figure 8: *Standard and Ethernet Front Panel*

PMC Cutouts

The number of PMC cutouts provided depends on the used front panel variant.

The standard front panel provides two cutouts for PMC module 1 and 2. The Ethernet front panel provides only one cutout for PMC module 1.

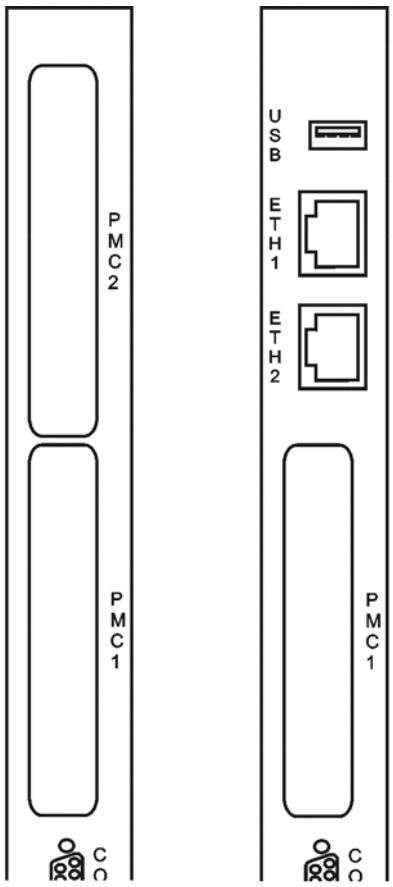


Figure 9: *Cutouts for PMC Modules on Standard and Ethernet Front Panel*

LEDs

The following LEDs are provided on both front panel variants:

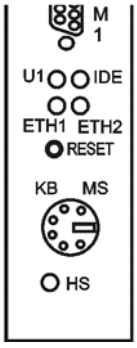


Table 8: *Description of Front Panel LEDs*

LED	Description
U1[1)]	User LED: Indicates POST status (green after POST)
IDE[1)]	User LED: Indicates POST status and IDE activity (green)
ETH1[1)]	User LED: Indicates link / activity of Ethernet controller 1 (green)
ETH2[1)]	User LED: Indicates link / activity of Ethernet controller 2 (green)
HS	Hot Swap LED: Indicates hot swap status (blue)

1) LED can be fully user defined (green, red, off) by setting the LED Control register

During power up, the settings of the LEDs U1 and IDE are as follows:

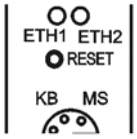
Table 9: *U1 and IDE LEDs During Power Up*

State	LED	Status
Before POST (Initial Register Values)	U1	Red
	IDE	Red
During Boot Block execution	U1	Red
	IDE	OFF
During POST	U1	Red / green[1)]
	IDE	Green / red[1)]
After POST	U1	Green
	IDE	Green (indicating IDE activity)

1) LED's colors change alternately

Keys

The only front panel key available by both front panel variants is the mechanical reset key.



When enabled and toggled, it instantaneously affects the board by generating a main reset. The main reset generates a CompactPCI reset if the board is assembled in a system slot.

A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. Reset is held active until the key is back in the inactive position, however at least 200 ms are guaranteed by a local timer.

For information on how to disable the key, Table 7 “Default Settings” page 2-15.

Connectors

Both, the standard and the Ethernet front panel provide the following connectors:

- COM1
- Keyboard / Mouse

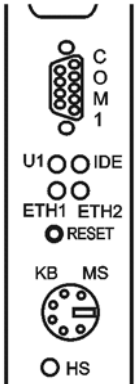


Figure 10: *Connectors of Standard and Ethernet Front Panel*

Additionally, the Ethernet front panel provides two RJ-45 connectors for Ethernet 1 and 2 and one USB connector.

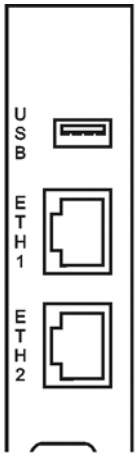


Figure 11: *Additional Connectors of Ethernet Front Panel*

If the board is to be incorporated in larger systems and adapted to specific needs, the following connector pinouts may be useful to give information on which signal is assigned to which pin.

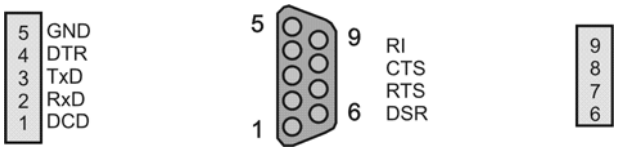


Figure 12: *COM1 Connector Pinout*

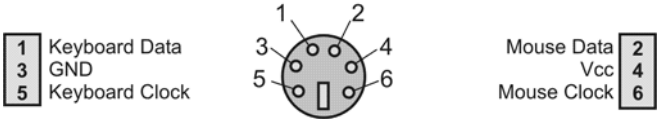


Figure 13: *KBD/MS - Keyboard and Mouse Connector Pinout*

Note: Make sure that the length of keyboard and mouse cables does not exceed three meters.



Figure 14: *Ethernet 1 and 2 Connector Pinout*



Figure 15: *USB Connector Pinout*

On-Board Connectors

The following connectors are on-board:

- CompactPCI connectors
- IDE Connector
- PMC connectors

CompactPCI Connectors

The board provides the CompactPCI connectors J1, J2, J3, J4 and J5. The CompactPCI interface is clocked with 33 MHz and is 32-bit wide.

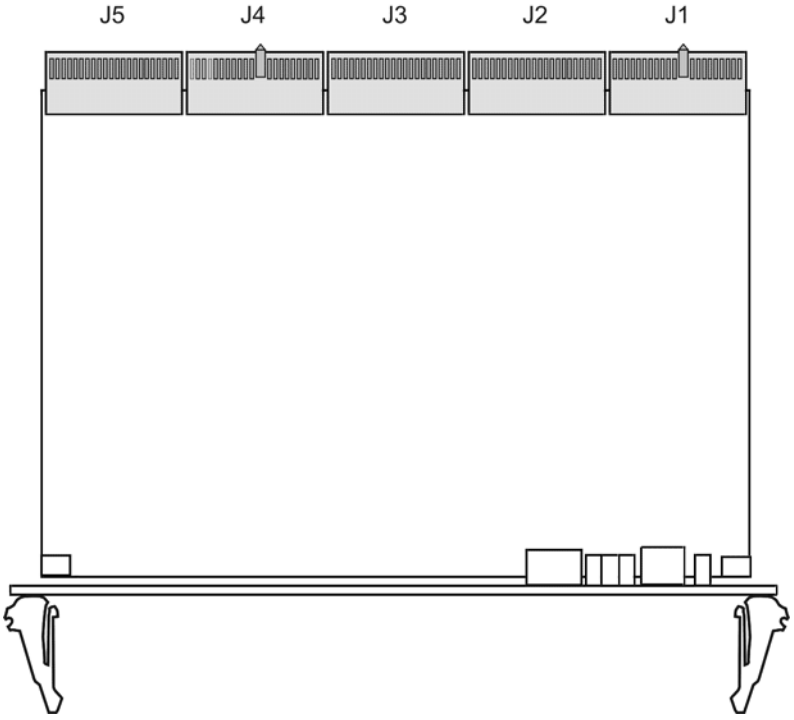


Figure 16: *Location of CompactPCI Connectors (Top View)*

J1 and J2

The J1 and J2 connectors implement the CompactPCI 64-bit connector pinout as specified by the CompactPCI specification PICMG 2.0 R3.0. Therefore, these pinouts are not documented.

J3

Connector J3 provides interfaces to:

- Ethernet signals (ETHx, reserved_2.16) for PICMG 2.16 and RTB
- PMC1 I/O (PMC1IO_*)
- Rear transition board information block (RTB_*)

Note: The interface to PICMG 2.16 Ethernet signals is only available on the CPCI-735R2 and the CPCI-736R2. For CPCI-735AR2 the pins are not connected.

	A	B	C	D	E	
19	GND	GND	GND	GND	GND	19
18	ETH1_TX_P	ETH1_TX_N	GND	Reserved_2.16	Reserved_2.16	18
17	ETH1_RX_P	ETH1_RX_N	GND	Reserved_2.16	Reserved_2.16	17
16	ETH2_TX_P	ETH2_TX_N	GND	Reserved_2.16	Reserved_2.16	16
15	ETH2_RX_P	ETH2_RX_N	GND	Reserved_2.16	Reserved_2.16	15
14	GND	GND	GND	GND	GND	14
13	PMC1IO_5	PMC1IO_4	PMC1IO_3	PMC1IO_2	PMC1IO_1	13
12	PMC1IO_10	PMC1IO_9	PMC1IO_8	PMC1IO_7	PMC1IO_6	12
11	PMC1IO_15	PMC1IO_14	PMC1IO_13	PMC1IO_12	PMC1IO_11	11
10	PMC1IO_20	PMC1IO_19	PMC1IO_18	PMC1IO_17	PMC1IO_16	10
9	PMC1IO_25	PMC1IO_24	PMC1IO_23	PMC1IO_22	PMC1IO_21	9
8	PMC1IO_30	PMC1IO_29	PMC1IO_28	PMC1IO_27	PMC1IO_26	8
7	PMC1IO_35	PMC1IO_34	PMC1IO_33	PMC1IO_32	PMC1IO_31	7
6	PMC1IO_40	PMC1IO_39	PMC1IO_38	PMC1IO_37	PMC1IO_36	6
5	PMC1IO_45	PMC1IO_44	PMC1IO_43	PMC1IO_42	PMC1IO_41	5
4	PMC1IO_50	PMC1IO_49	PMC1IO_48	PMC1IO_47	PMC1IO_46	4
3	PMC1IO_55	PMC1IO_54	PMC1IO_53	PMC1IO_52	PMC1IO_51	3
2	PMC1IO_60	PMC1IO_59	PMC1IO_58	PMC1IO_57	PMC1IO_56	2
1	RTB_VP5	PMC1IO_64	PMC1IO_63	PMC1IO_62	PMC1IO_61	1

Figure 17: *J3 Connector Pinout*

J4

Connector J4 provides interfaces to:

- Parallel (LPT_*)
- PMC 2 I/O (PMC2IO_*)
- COM3 (RS232_3_*)

Note: The connector J4 is only available on CPCI-735R2 and CPCI-735AR2.

	A	B	C	D	E	
25	PMC2IO_5	PMC2IO_4	PMC2IO_3	PMC2IO_2	PMC2IO_1	25
24	PMC2IO_10	PMC2IO_9	PMC2IO_8	PMC2IO_7	PMC2IO_6	24
23	PMC2IO_15	PMC2IO_14	PMC2IO_13	PMC2IO_12	PMC2IO_11	23
22	PMC2IO_20	PMC2IO_19	PMC2IO_18	PMC2IO_17	PMC2IO_16	22
21	PMC2IO_25	PMC2IO_24	PMC2IO_23	PMC2IO_22	PMC2IO_21	21
20	PMC2IO_30	PMC2IO_29	PMC2IO_28	PMC2IO_27	PMC2IO_26	20
19	PMC2IO_35	PMC2IO_34	PMC2IO_33	PMC2IO_32	PMC2IO_31	19
18	PMC2IO_40	PMC2IO_39	PMC2IO_38	PMC2IO_37	PMC2IO_36	18
17	PMC2IO_45	PMC2IO_44	PMC2IO_43	PMC2IO_42	PMC2IO_41	17
16	PMC2IO_50	PMC2IO_49	PMC2IO_48	PMC2IO_47	PMC2IO_46	16
15	PMC2IO_55	PMC2IO_54	PMC2IO_53	PMC2IO_52	PMC2IO_51	15
14	Key	Key	Key	Key	Key	14
13	Key	Key	Key	Key	Key	13
12	Key	Key	Key	Key	Key	12
11	PMC2IO_60	PMC2IO_59	PMC2IO_58	PMC2IO_57	PMC2IO_56	11
10	GND	PMC2IO_64	PMC2IO_63	PMC2IO_62	PMC2IO_61	10
9	LPT_INIT_N	LPT_PD_1	LPT_STB_N	LPT_AFD_N	LPT_PD_2	9
8	LPT_PD_5	LPT_PD_4	LPT_ERR_N	LPT_PD_0	LPT_PD_6	8
7	LPT_PE	LPT_BUSY_N	LPT_PD_3	LPT_SLIN_N	LPT_SLCT	7
6	GND	GND	LPT_ACK_N	LPT__PD_7	GND	6
5	Reserved	Reserved	GND	GND	Reserved	5
4	Reserved	Reserved	GP_RXD	Reserved	Reserved	4
3	Reserved	Reserved	GP_TXD	Reserved	SPKR	3
2	RS232_3_RTS	RS232_3_CTS	RS232_3_RI	GND	GND	2
1	RS232_3_DCD	RS232_3_RXD	RS232_3_TXD	RS232_3_DTR	RS232_3_DSR	1

Figure 18: *J4 Connector Pinout*

J5

Connector J5 provides interfaces to:

- Secondary IDE (IDE_*)
- USB (USB_*)
- Keyboard (KBD)
- PS2 mouse (MS)
- COM1 (RS232_1_*) and COM2 (RS232_2_*)
- Floppy (FD_*)
- IPMB and ICMB

Note: Make sure that the length of keyboard, mouse and USB cables does not exceed three meter.

	A	B	C	
22	Reserved	Reserved	Reserved	22
21	CPCI_IPMB1_DAT	ICMB_RXD	Reserved	21
20	Reserved	Reserved	Reserved	20
19	CPCI_IPMB1_CLK	ICMB_TXD	Reserved	19
18	Reserved	Reserved	Reserved	18
17	RS232_1_CTS	RS232_2_CTS	RS232_1_DTR	17
16	RS232_1_RTS	RS232_2_RTS	RS232_2_DTR	16
15	RS232_1_RXD	RS232_2_RXD	RS232_1_DCD	15
14	RS232_1_TXD	RS232_2_TXD	RS232_2_DCD	14
13	FD_DENSEL	FD_RDATA_N	FD_WDATA_N	13
12	FD_DSKCHG_N	FD_INDEX_N	FD_TRK0_N	12
11	FD_WP_N	FD_MTR1_N	FD_MTR0_N	11
10	RIB_DAT	RIB_CLK	VP5_RTB	10
9	S_IDE_BRSDR_N	S_IDE_IORDY	Reserved	9
8	S_IDE_A_2	S_IDE_IOR_N	S_IDE_IOW_N	8
7	S_IDE_A_1	S_IDE_D_15	S_IDE_D_14	7
6	S_IDE_A_0	S_IDE_D_11	S_IDE_D_10	6
5	S_IDE_D_7	S_IDE_D_6	S_IDE_D_5	5
4	S_IDE_D_2	S_IDE_D_1	S_IDE_D_0	4
3	S_IDE_DASP_N	GND	GND	3
2	USBVCC0	USB_P0_N	USB_P0_P	2
1	EXTSMI_N	VP5_RTB	V3P3_RTB	1

A B C D E

Figure 19: *J5 Connector Pinout, Rows A-C*

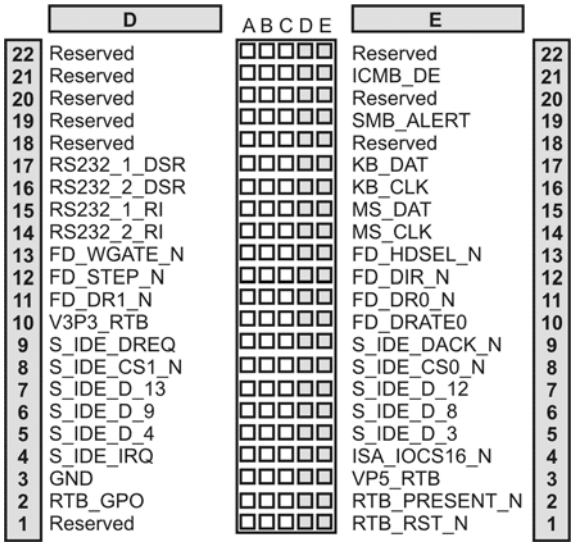


Figure 20: *J5 Connector Pinout, Rows D and E*

IDE Connector

A 2.5” hard disk can be connected to the primary IDE interface of the board. The pinout is given below.

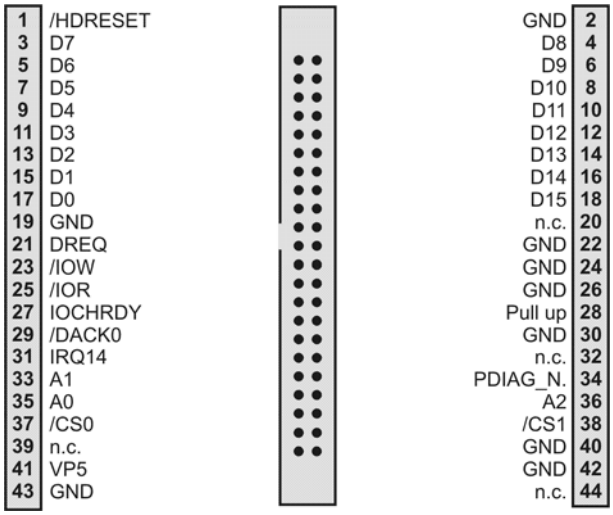


Figure 21: *IDE Connector Pinout*

PMC Connectors

At PMC slot 1, the board provides the connectors PN11-PN14 and at PMC slot 2, the board provides the connectors PN21, PN22 and PN24.

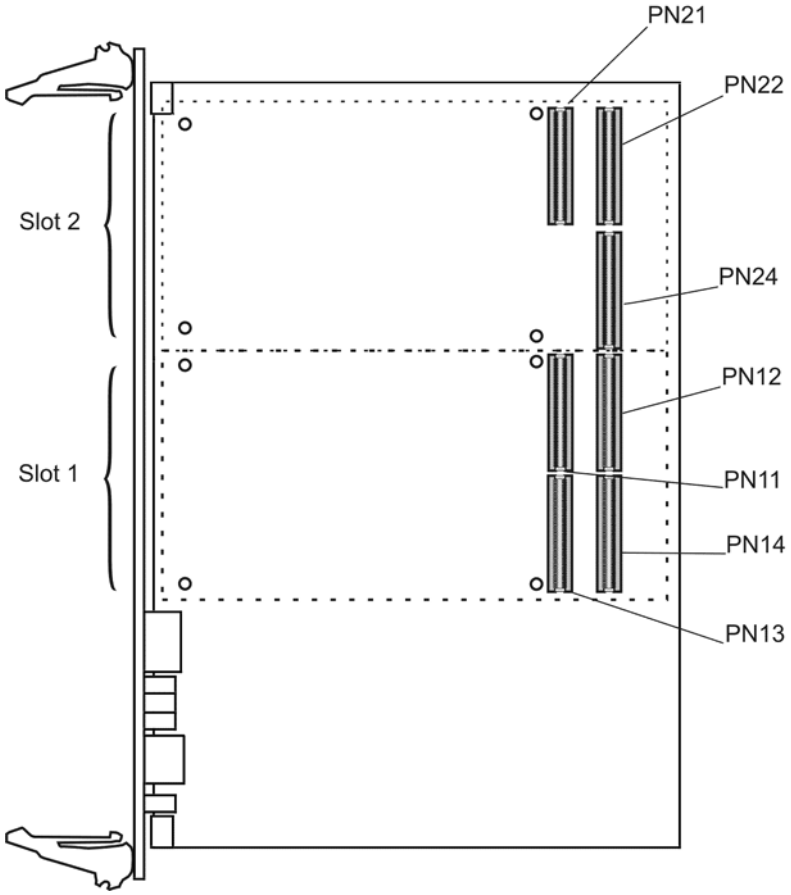


Figure 22: *PMC Connectors and Slots*

The connectors PN11-13 and PN21-22 implement the pinout as specified by the PMC specification IEEE Standard 1386.1-2001. Therefore, these pinouts are not documented. The following figures show the pinouts for PN14 and PN24.

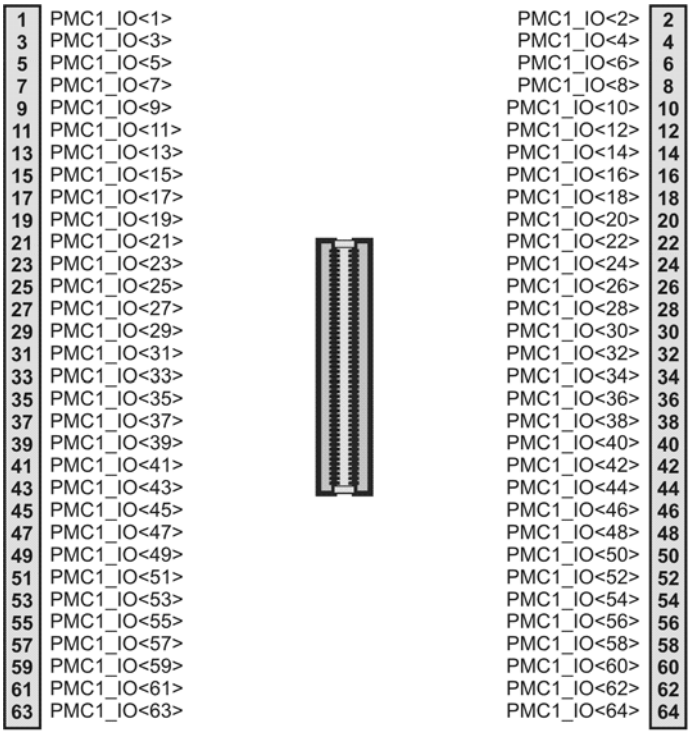


Figure 23: *PN14 Connector Pinout*

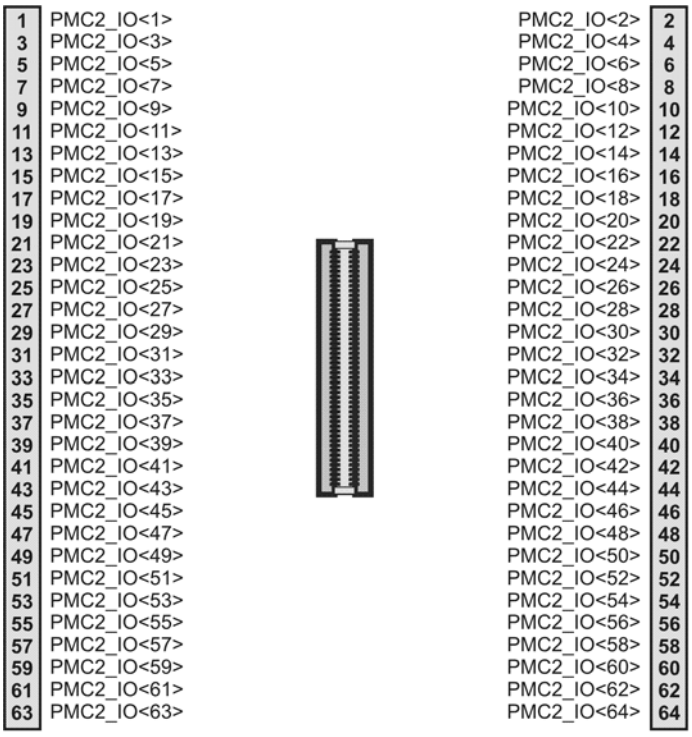


Figure 24: *PN24 Connector Pinout*

For information on the signaling level and data bus width of the PMC slots, refer to section “PMC Module” page 2-9.

4

BIOS

Introduction

BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the board and is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the board for the initial boot-up procedure. BIOS offers the following features:

- Hardware set-up utility for setting configuration data
- Multiboot for a flexible boot order
- Serial Console redirection for remote board configuration
- Software upgrade utility

The BIOS complies to the following specifications:

- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.3
- BIOS Boot Specification 1.01
- PXE 2.0

The BIOS set-up program is required to configure the hardware of the board. This configuration is necessary for operating the board and connected peripherals and is stored in the CMOS memory. A battery preserves configuration data when the board is powered off.

Whenever you are not sure about configuration settings, restore the default values. They are provided in case that a value has been changed and one wishes to reset settings. To restore the default values, press <F9> in setup.

Note:

- **Loading the BIOS default values will affect all setup items and will reset options previously altered.**
- **If you set the default values, the displayed default values are not yet stored to be effective for the next boot. They are just loaded to be displayed. However, they become effective if the BIOS setup is exited after changes have been saved.**

Changing Configuration Settings

When the system is turned on or rebooted, the presence and functionality of the system components is tested by POST (Power-On Self Test). Press <F2> while the message `Press <F2> to enter SETUP` appears on the screen. The main menu appears.

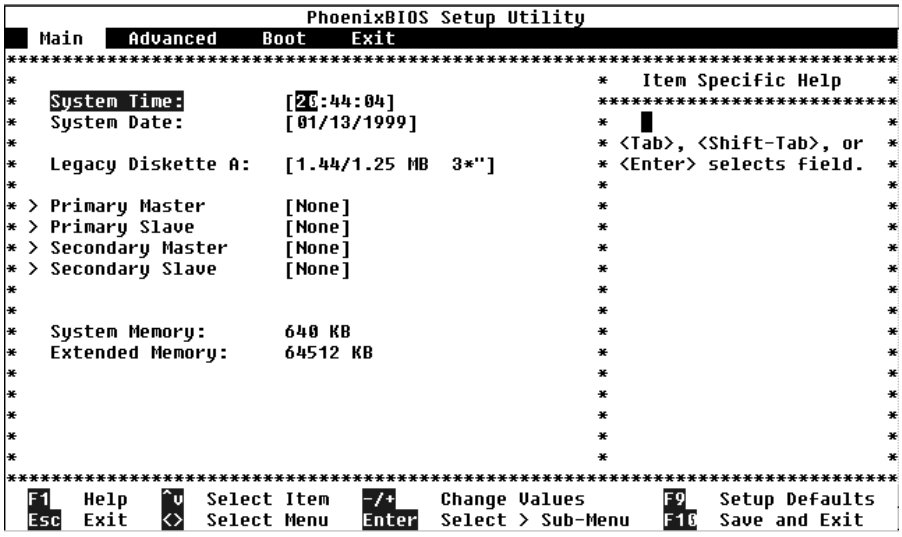


Figure 25: *Main Menu*

Note:

- **Make sure that BIOS is properly configured prior to installing the operating system and its drivers.**
- **If you saved changes in setup, the next time the board boots BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter setup to get the default values or to change the selections that caused the failure. If the boot fails or is interrupted three times in a row, the default values are then loaded automatically.**

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the menu window.

Selecting The Boot Device

There are two possibilities to determine the device from which BIOS attempts to boot:

- Via setup to select a permanent order of boot devices
- Via boot selection menu to select any device for the next boot-up procedure only

Note: BIOS does not support USB, therefore, booting from USB devices is not possible.

Via Setup

To determine the order of boot devices in setup, proceed as follows:

1. In menu line, select [Boot]
2. Select order of devices from which BIOS attempts to boot operating system

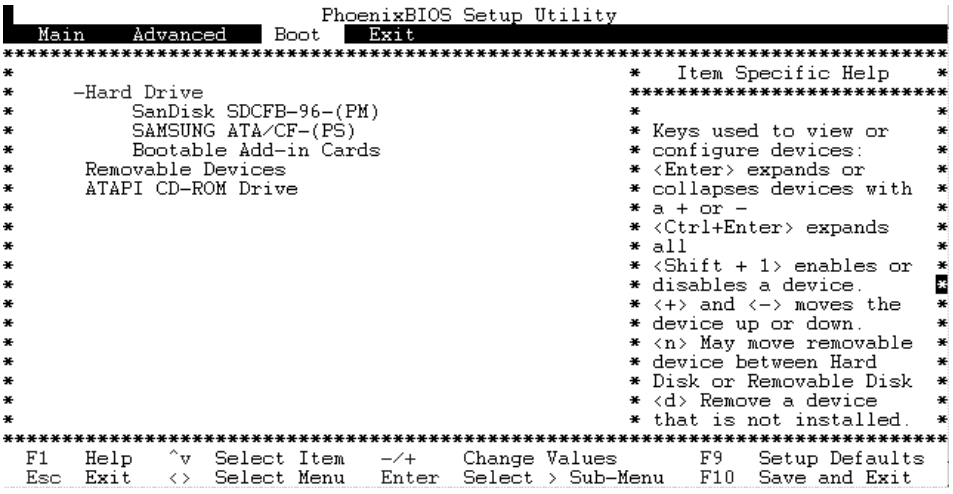


Figure 26: *Boot Device Order*

If BIOS is not successful at booting from a device, it tries to boot from the first device of the next main entry. If, for example, BIOS cannot boot from the SanDisk SDCFB-96-(PM), it does not try to boot from the hard disk

SAMSUNG ATA / CF-(PS) but from the first device listed under “Removable devices”.

The same options determine the order in which POST installs the devices and the operating system assigns device letters. BIOS supports up to two floppy devices to which the operating system may assign, e.g. drive letters A: and B:. The drives C:, D:, E: etc. are reserved for hard-disk drives.

Note: There is not always an exact correspondence between the order specified in setup and the letters assigned by the operating system. Many devices, such as legacy option ROMs, support more than one device that can be assigned to several letters. If the CD-ROM drive should have a letter coming before the one assigned to the hard drive, move it in front of the hard drive. The group of bootable add-in cards refers to devices with non-multiboot-compliant BIOS option ROM from which you can boot the operating system.

Via Boot Selection Menu

To enter the boot menu, press <ESC> during POST.



Figure 27: *Boot Menu*

Continue with one of the following options:

a) Override existing boot sequence by selecting another boot device from the boot order list

Note: If the selected device does not load the operating system, BIOS reverts to the previous boot sequence.

b) Select [Enter Setup] to enter setup utility

c) Press <Esc> to return to POST screen and continue with previous boot sequence

Booting the Board via Network

By default, the possibility to boot the board via network is disabled. This is done because the boot process takes significantly more time if network boot is enabled.

In order to enable the possibility to boot from network, proceed as follows:

1. Turn on board
2. Press <F2> when `Press <F2> to enter SETUP` appears
3. Select [Advanced]
4. Select [POST Options]
5. Set [Network Option ROM] to enabled
6. Save setup
7. Reboot board

Now ETH1 and ETH2 boot devices are displayed in setup and boot selection menu and can be selected.

Serial Console Redirection

The firmware of the board provides a serial console redirection feature. This allows remote board configuration by connecting a terminal to the board via a serial communication link.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC keyboard input. The serial console redirection feature can be configured via setup utility.

Note: If serial console redirection is enabled the terminal represents an option and is not necessarily required for boot-up procedure.

Requirements

For serial console redirection, the following is required:

- Terminal which supports a VT100 or ANSI mode
- Serial interface cable (part of cable accessory kit available from Motorola)
- Null modem adapter

Terminal emulation programs such as TeraTermPro can be used.

Before using TeraTermPro the keyboard configuration of TeraTermPro has to be modified to guarantee that the function keys work properly. The following function key codes have to be entered into the relevant configuration file:

- PF1=59
- PF2=60

The respective key codes can be found with the keycode.exe utility of the TeraTerm software package. The required modifications are described in detail in the TeraTerm help files.

Serial console redirection does not necessarily require a VGA card to be present. If no VGA card is present, on-board SRAM memory is used as video buffer.

Remote Configuration

The procedure to configure the board remotely for boot up depends on the board's configuration. For boards with standard BIOS the following default settings for remote configuration are used.

Table 10: *Default Settings for Remote Configuration*

Parameter	Default Setting
Console type	VT100
COM port	COM1 (on front panel)
Baud rate	9600
Flow control	Xon / Xoff

Remote Configuration Set

If the board is set for remote configuration and if you are familiar with the setting, proceed as follows:

1. Configure terminal to communicate using the same parameters as in BIOS setup
2. Connect terminal to serial interface cable
3. Connect serial interface cable to COM port you have selected in setup
4. Turn on board

Remote Configuration Not Set

If the board is not set for remote configuration, proceed as follows:

1. Connect monitor and keyboard to board
2. Turn on board
3. Press <F2> when `Press <F2> to enter SETUP` appears on screen
4. Select [Advanced]
5. Select [Console Redirection]
6. Select appropriate parameters for communication
7. Save setup

8. Reboot board
9. Configure terminal to communicate using the same parameters as in BIOS setup
10. Connect erial interface cable to COM port you have selected in setup

Updating BIOS

Via the Software Maintenance And Reference Tools (S.M.A.R.T.) you can get help on configuration, installation, usage and functionality issues of Motorola' products. You can download documentation via limited public S.M.A.R.T. access and software via full access after subscribing to a TSA contract.

Downloading Software from S.M.A.R.T.

In order to get access to the S.M.A.R.T. server proceed as follows:

1. Go to Motorola internet site (www.motorola.com)
2. Click on blue button labeled "log on S.M.A.R.T."
3. Follow the instructions on screen

For a limited public S.M.A.R.T. account, enter a User ID. A password will be given to you automatically.

For a full S.M.A.R.T. account, download and subscribe to the TSA contract.

For further information, contact your local sales representative.

Update Procedure

To update BIOS, you first have to create a floppy disk containing a BIOS upgrade file and upgrade utilities. Therefore, download a zip file from the S.M.A.R.T. server that contains the following files:

- rawrite.exe
- bios_upd.img
- README.1ST

Insert a floppy disk into the drive of your computer and execute rawrite.exe to write the bios_upd.img file to the disk. This file contains a README file providing further information for updating your BIOS.

BIOS Messages

The following messages may be displayed, e.g. if your system fails after you made changes in the setup menus. If it is not possible to fix a problem with the help of this section, contact your local sales representative or services for further support.

Message	Explanation	Corrective Action
`nnnn Cache SRAM Passed`	*nnnn* is amount of system cache in KBytes successfully tested	None
`CD-ROM Drive Identified`	Autotyping identified CD-ROM Drive	None
`Diskette drive A error` `Diskette drive B error`	Drive A: or B: fails the BIOS POST disk tests. Drive is selected via setup but either not present or defect.	Check that drive is defined with proper disk type in setup, that disk drive is attached correctly and that controller is enabled.
`Entering SETUP ...`	Starting setup program	None
`Extended RAM Failed at offset: nnnn`	Extended memory not working or not configured properly at offset *nnnn*	Check if memory modules are installed correctly. Otherwise contact your local sales representative or services for further support.
`nnnn Extended RAM Passed`	*nnnn* is amount of RAM in MBytes successfully tested.	None
`Failing Bits: nnnn`	*nnnn* is a map of the bits at the RAM address (in system, extended or shadow memory) which failed the memory test. Each `1` (one) in the map indicates a failed bit.	Check if memory modules are installed correctly. Otherwise contact your local sales representative or services for further support.

Message	Explanation	Corrective Action

`Fixed Disk 0 Failure`
`Fixed Disk 1 Failure`
`Fixed Disk Controller Failure`
	Fixed disk not working or not configured properly	Check if fixed disk is attached properly. Run setup to be sure the fixed-disk type is correctly identified.

`Fixed Disk 0...3 Identified`	Autotyping identified specified fixed disk.	None
`Incorrect Drive A type - run SETUP` `Incorrect Drive B type - run SETUP`	Type of floppy drive not correctly identified in setup	Check for correct floppy drive in setup.
`Keyboard controller error`	Keyboard controller failed test	Replace keyboard
`Keyboard error`	Keyboard not working	Check for correct keyboard connection.
`Keyboard error nnn`	BIOS discovered a stuck key and displays scan code *nn* for stuck key.	Replace keyboard, check for stuck keys.
`Operating system not found`	Operating system cannot be located on either drive A: or drive C:.	Enter setup and check if fixed disk and drive A: are properly identified.
`Parity Check 1 nnnn`	Parity error found in system bus. BIOS attempts to locate address *nnnn* and display it on screen. If it cannot locate the address, it displays `????`.	Check for correct memory module types.
`Parity Check 2 nnnn`	Parity error found in system bus. BIOS attempts to locate address *nnnn* and display it on the screen. If it cannot locate the address, it displays `????`.	Check for correct memory module types.
`Press <F1> to resume, <F2> to Setup`	Displayed after any recoverable error message	Press <F1> to start boot process or <F2> to enter setup and change any settings.

Message	Explanation	Corrective Action
`Previous boot incomplete - Default configuration used`	Previous POST did not complete successfully. POST loads default values and offers to run setup. If failure was caused by incorrect values and they are not corrected, the next boot is likely to fail.	Run setup to restore original configuration. This error is cleared the next time the system is booted.
`Real time clock error`	Real-time clock fails BIOS test	May require board repair
`Resource allocation conflict on motherboard - Run Configuration Utility`	Possible interrupt or interface resource conflict.	Run ISA or EISA Configuration Utility to resolve resource conflict.
`Shadow RAM Failed at offset: nnnn`	Shadow RAM failed at offset *nnnn* of the 64k block at which error was detected.	Contact your local sales representative or services for further support.
`nnnn Shadow RAM Passed`	*nnnn* is amount of shadow RAM in KBytes successfully tested	None
`System battery is dead - Replace and run SETUP`	The SRAM (CMOS) clock battery indicator shows the battery is dead	Replace battery and run Setup to reconfigure system.
`System BIOS shadowed`	System BIOS copied to shadow RAM	None
`System cache error - Cache disabled`	RAM cache failed BIOS test. BIOS disabled cache	Contact your local sales representative or services for further support.
`System CMOS checksum bad - run SETUP`	System SRAM (CMOS) has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in SRAM (CMOS).	Run setup and reconfigure system either by getting default values and / or making your own selections.

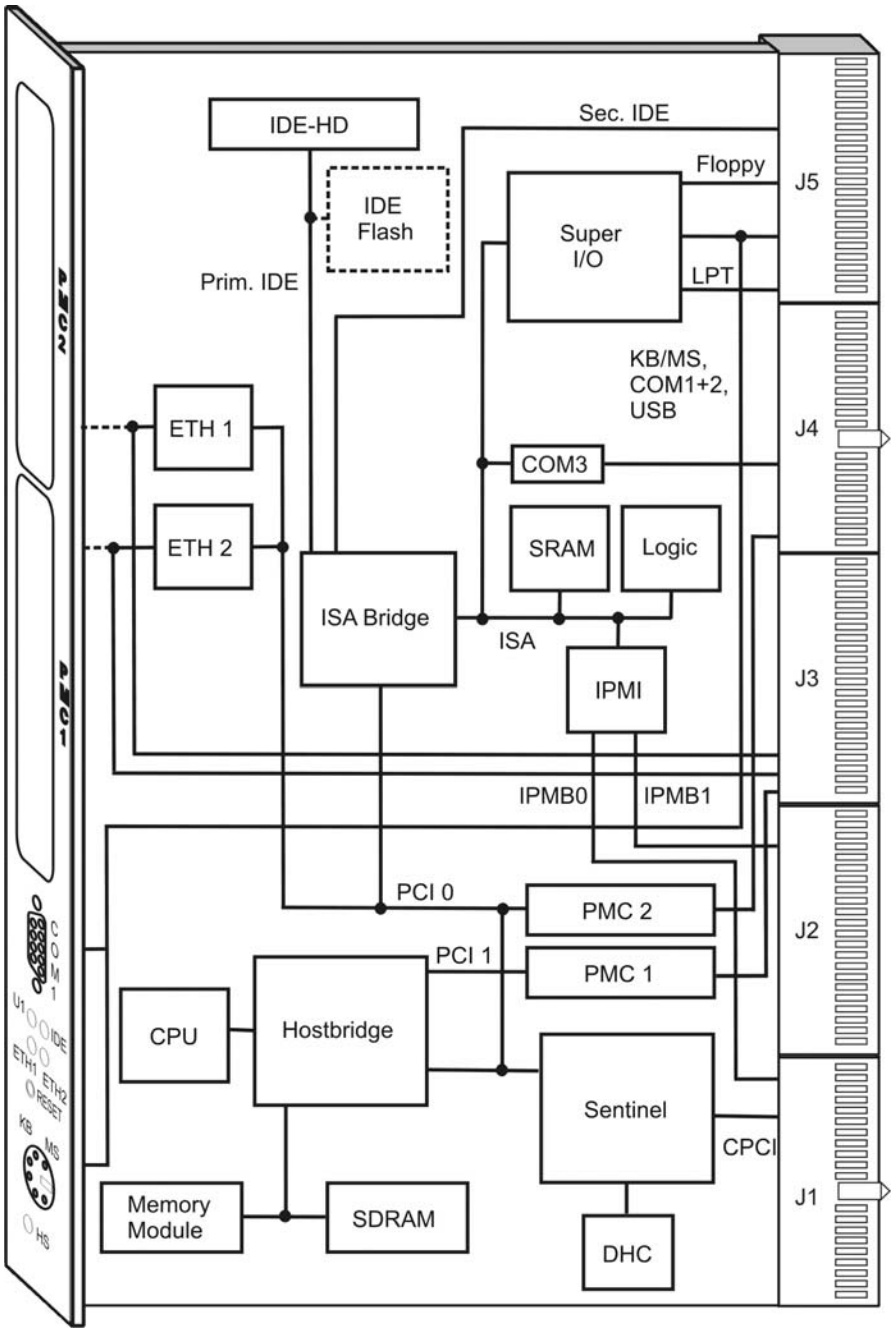
Message	Explanation	Corrective Action
`System RAM Failed at offset: nnnn`	System RAM failed at offset *nnnn* in the 64k block at which the error was detected.	Check for correct memory modules. Otherwise contact your local sales representative or services for further support.
`nnnn System RAM Passed`	*nnnn* is amount of system RAM in KBytes successfully tested	None
`System timer error`	Timer test failed	Requires repair of system board
`UMB upper limit segment address: nnnn`	Address *nnnn* of the upper limit of upper memory blocks indicates released segments of BIOS which may be reclaimed by a virtual memory manager	None
`Video BIOS shadowed`	Video BIOS successfully copied to shadow RAM	None
`Invalid System Configuration Data – run configuration utility`		Enter setup and use advanced configuration option to reset configuration data (due to corrupted ESCD data).

5

Buses

Block Diagram

The block diagram shows how the CPCI-735R2 devices work together and which data paths they use. The broken line marks optional devices or paths.



PCI Local Bus 0

PCI local bus 0 is capable to run at 32 Bit and 33 MHz only.

Table 11: *Devices on PCI Local Bus 0*

PCI Device	Device Type	IDSEL	Dev. No	PCI IRQ	REQ/GNT
LAN #1	Intel 82559ER	AD[17]	1	INTB	0
LAN #2	Intel 82559ER	AD[18]	2	INTC	1
PMC Slot 2 (upper)	PMC2	AD[24]	8	INTA	3
PCI / CPCI-Bridge	Motorola SENTINEL	AD[20]	4	INTA	2
Primary PCI Interface	CNB30LE North Bridge	-	0	-	-
South Bridge	OSB4 Open South Bridge	AD[31]	20	-	-

Ethernet

The PENT / CPCI-735R2 / 736R2 Family is equipped with two Intel 82559ER 10Base-T / 100Base-T Ethernet controllers, LAN#1 and LAN#2, which are able to operate in either full duplex or half duplex mode.

The Ethernet interface is available depending on the variant of the PENT / CPCI-735R2 / 736R2 Family board:

Table 12: *Ethernet Interface*

Board Variant	Ethernet Available
CPCI-735R2	Via CompactPCI connector J5 (transformer on rear transition board)
CPCI-735AR2	Via front panel (transformer on CPCI-735AR2)
CPCI-736R2	Via CompactPCI Connector J3 (PICMG 2.16) (transformer on CPCI-736R2)

Two LEDs at the front panel of the CPCI-735R2, designated as ETH1 and ETH2, indicate Ethernet link and activity.

PMC2

The PMC 2 interface is a 5V compliant PCI interface with its I/O signals routed towards CPCI I/O Connector J4.

Note: The space of the PMC 2 I/O connector is used for the Ethernet transformers to support PICMG 2.16 on CPCI-736R2 boards. Therefore, the PMC 2 Interface on CPCI-736R2 boards does not fully comply to PMC specifications and can only carry PMC modules without PMC I/O connector assembled.

SENTINEL

Motorola SENTINEL is used as PCI-to-CompactPCI universal bridge that enables the board to work as either CompactPCI system (host) or peripheral board.

SENTINEL is capable to run in either 3.3V or 5V VIO environment. However, hot-swap requirements for the 3.3V environment differ from requirements for the 5V environment. The PENT/CPCI-735R2/736R2 Family boards are designed for 5V CompactPCI systems only. For further information, refer to “Installation in a Powered System” page 2-19.

The table below lists all fields in the SPROM of the SENTINEL, the contents loaded into the registers at power up.

Note: Invalid SPROM contents may cause malfunction of the board.

Table 13: *SENTINEL SPROM Contents*

Register Name	Offset	Configurable	Default Value	Comment
Magic word	0_{16}	No	1146_{16}	-
Downstream IR mask	2_{16}	No	$FFFF_{16}$	-
Upstream IR mask	6_{16}	No	$FFFF_{16}$	-

Table 13: *SENTINEL SPROM Contents (cont.)*

Register Name	Offset	Configurable	Default Value	Comment
Downstream BAR 0 DSR setup	8_{16}	Yes	$FFFFF000_{16}$	Maps 4 KByte DSR registers by default. Larger values provide access to on-board resources. A value less than FFFFF000 is not allowed.
Downstream BAR 0 DSR translate	C_{16}	Yes	00000000_{16}	-
Downstream BAR 2 DSR setup	10_{16}	Yes	$FFF00000_{16}$	This defines a default PCI window of 1 MByte.
Downstream BAR 2 DSR translate	14_{16}	Yes	00000000_{16}	-
Downstream BAR 3 DSR setup	18_{16}	Yes	00000000_{16}	-
Downstream BAR 3 DSR translate	$1C_{16}$	Yes	00000000_{16}	-
Downstream BAR 4 DSR setup	20_{16}	Yes	00000000_{16}	-
Downstream BAR 4 DSR translate	24_{16}	Yes	00000000_{16}	-
Upstream BAR 2 DSR setup	28_{16}	Yes	FFF8000016	Defines a default PCI window of 512 KByte.
Upstream BAR 2 DSR translate	$2C_{16}$	Yes	00000000_{16}	-
Memory base preload	30_{16}	No	0001_{16}	These two settings effectively disable the memory window (base>limit).
Memory limit preload	32_{16}	No	0000_{16}	-
I_2O outbound post list interrupt mask	34_{16}	No	$FFFFFFFF_{16}$	-
Subsystem vendor ID preload	38_{16}	No	1146_{16}	-

Table 13: *SENTINEL SPROM Contents (cont.)*

Register Name	Offset	Configurable	Default Value	Comment
Subsystem ID preload	$3A_{16}$	No	$1A_{16}$	Board-specific subsystem ID
I_2O setup mask	$3C_{16}$	No	00000000_{16}	-
Secondary min. grant preload	42_{16}	No	01_{16}	-
Secondary max. latency preload	43_{16}	No	01_{16}	-
Primary min. grant preload	46_{16}	No	01_{16}	-
Primary max. latency preload	47_{16}	No	01_{16}	-
Upstream BAR 3 setup	48_{16}	Yes	00000000_{16}	-
Upstream BAR 3 translate	$4C_{16}$	Yes	00000000_{16}	-
Chip control 0	54_{16}	Yes	0000_{16}	-
Chip control 1	56_{16}	Yes	0000_{16}	-
Arbiter control/status	$5A_{16}$	Yes	8020_{16}	-
Primary SERR# control	$5D_{16}$	Yes	07_{16}	-
Secondary SERR# control	$5F_{16}$	Yes	07_{16}	-
GPIO control	60_{16}	No	$F0_{16}$	-
GPIO write data	61_{16}	No	80_{16}	-
GPIO IR mask	63_{16}	No	FF_{16}	-
User capability ID	68_{16}	Yes	00_{16}	-
MSI next item pointer	71_{16}	Yes	00_{16}	User capability is disabled.
Message control	72_{16}	Yes	0000_{16}	-
Scratchpad	76_{16}	Yes	0000_{16}	-
Primary programming interface	79_{16}	Yes	00_{16}	-

Table 13: *SENTINEL SPROM Contents (cont.)*

Register Name	Offset	Configurable	Default Value	Comment
Primary sub class code	$7A_{16}$	Yes	80_{16}	This field defines “Other Bridge”.
Primary base class code	$7B_{16}$	Yes	06_{16}	This field defines “Bridge Device”.
Secondary programming interface	$7D_{16}$	Yes	00_{16}	-
Secondary sub class code	$7E_{16}$	Yes	80_{16}	This field defines “Other Bridge”.
Secondary base class code	$7F_{16}$	Yes	06_{16}	This field defines “Bridge Device”.

ISA Bridge

The ISA bridge provides the following interfaces:

- IDE
- USB
- SMB

IDE Interfaces

The ISA bridge provides two separate IDE interfaces. Both interfaces support PIO and Ultra DMA 33 mode. A bicolor LED is available at the front panel to indicate IDE traffic.

Primary IDE Interface

The primary IDE interface provides access to two onboard IDE devices. A 2.5” hard disk can be connected to the primary IDE interface via the onboard IDE connector. The hard disk is mounted via four standoffs directly to the board and is connected with a 44-pin flat ribbon cable. For further information, refer to “IDE Devices” page 2-12.

As a second on-board device the CPCI-735R2 provides an IDE flash controller SAMSUNG KS32P6632-TX or compatible (assembly option) with up to 64 MByte of IDE flash memory. The IDE flash controller can be enabled or disabled and configured to be either master or slave via switch setting.

Device Type	I/O Address Space	ISA IRQ
ISA bridge	$1F0_{16}..1F7_{16}$ $3F6_{16}..3F7_{16}$	14

Secondary IDE Interface

The secondary IDE interface is routed to CPCI Connector J5 for up to two additional, external IDE devices which can be connected via RTB.

Device Type	I/O Address Space	ISA IRQ
ISA bridge	$170_{16}..177_{16}$ $376_{16}..377_{16}$	15

USB

The CPCI-735R2 provides up to two USB 1.1 interfaces (assembly option). USB port 0 is available on CPCI connector J5.

Note: USB port 1 is only available on the CPCI-735AR2 front panel.

SMB Interface

The SMB interface of the ISA bridge is connected to the SPD EEPROM of the on-board memory and the SPD EEPROM of the memory module. BIOS reads memory configuration parameters from SPD EEPROMs during power up and after reset.

Furthermore, on boards without IPMI, a temperature sensor measuring CPU and board temperature is connected to the SMB interface.

Table 14: *System Management I^2C Bus*

Device Name	Device Type	Function	Location	Address
SPDEEPROM1	24C02	Memory bank 0, 1 information	Board	$1010000x_2$
SPDEEPROM4	24C02	Memory bank 6, 7 information	Board	$1010011x_2$
SPDEEPROM2	24C02	Memory bank 2, 3 information	Memory module	$1010001x_2$
SPDEEPROM3	24C02	Memory bank 4, 5 information	Memory module	$1010010x_2$
TEMPSENSE1	MAX1617 (or compatible)	Temperature sensor	Board	$0011000x_2$ (assembly option)

PCI Local Bus 1

PCI local bus 1 is capable to run at 64 bit and 66 MHz.

Table 15: *Devices on PCI Local Bus 1*

PCI Device	Device Type	IDSEL	Dev. No	PCI IRQ	REQ/GNT
Secondary PCI Interface	CNB30LE North Bridge	-	17	-	-
PMC Slot 1 (lower)	PMC	AD[19]	3	INTD	0

PMC1

The only device besides the north bridge that is connected to the local PCI bus 1 is the PMC module 1.

The bus speed and width negotiation is controlled by the PCI signals M66EN and REQ64_N / ACK64_N according to the PCI Local Bus Specification Rev.2.1.

M66EN

The bus frequency depends on the PCI signal M66EN. If this signal is not driven low by an attached PMC module, the board assumes an 66 MHz compliant PMC module and drives the clock accordingly.

The PCI local bus 1 can be set to run at 33 MHz by switching SW3-3 to the 'ON' position (refer to Table "Default Settings").

REQ64_N and ACK64_N

64-bit transfers are requested and acknowledged by the PCI signals REQ64_N and ACK64_N. If no 64-bit transfers are requested, 32-bit transfers will be performed instead.

ISA Bus

The local ISA bus is 16-bit wide and is used for connecting flash memory, SRAM, Super I/O, serial ports and user-specific functionality.

Flash Memory

The firmware memory is built with two 8-bit wide flash chips. One is used as the standard 1 MByte boot flash memory, the other can be used as a 4 MByte user flash memory.

The flash memory is visible at the top of the processor memory space. It is either visible as five pages of 1 MByte blocks or as 10 pages of 512 KByte blocks. The default page is 0, so that the boot block flash part is visible. A different page can be selected via register access.

The upper 512 KByte (page 0) within the boot block flash are reserved for BIOS, while the remaining 4.5 MByte are available for applications. Page 0 is always active after reset (depending on bit 7 of the Flash Control register).

The boot block memory range ($FFFFC000_{16}$..$FFFFFFFF_{16}$) is write-protected. Write protection can only be removed via switch setting (refer to Table 7 “Default Settings” page 2-16). The remaining flash region is also write protected. Write protection can be removed via register access (refer to “Flash Control Register” page 6-24).

Device Type	Memory Address Space
Micron MT28F800B3 (or compatible) Intel E28F320J3A (or compatible)	$FFF00000_{16}$..$FFFFFFFF_{16}$

SRAM

The board carries an 8-bit wide SRAM with I^2C backup functionality (SRAM) of up to 32 KByte size (assembly option). The lower 4 KByte of this device are used as the video memory for the BIOS serial redirection feature if no VGA card is installed. The remaining 28 KByte are available for user applications and can be mapped to different memory addresses via SRAM Configuration register (refer to page 6-9).

The chip select signal for the SRAM is generated by the FPGA depending on the actual memory map of this device.

Device Type	Memory Address Space (Serial Redirection)	Memory Address Space (User)
IDT71V256 (or compatible)	$000B8000_{16}$..$000B9FFF_{16}$	$000C8000_{16}$..$000DFFFF_{16}$ (programmable)

.

Serial Port COM3

The CPCI-735R2 has three full-duplex serial interfaces. They are fully compatible to industry standard 16550 asynchronous communication controller.

Serial port 3 is implemented with dedicated TL16C550 devices connected to the on-board ISA bus. The serial port is sourced by a 1,8432 MHz clock and supports baud rates of 600, 1200, 2400, 4800, 9600, 19200, 38400 and 115200. Serial port 3 is equipped with a RS232 line driver and is routed to the CompactPCI connector J4.

Device Type	I/O Address Space	ISA IRQ
TL16C550 (or compatible) Serial Port #3	$2E8_{16}$..$2EF_{16}$, $2F8_{16}$..$2FF_{16}$, $3E8_{16}$..$3EF_{16}$ [1], $3F8_{16}$..$3FF_{16}$	3 [1],4,5

1) Default setting

Super I/O Controller

The National Semiconductor PC97317 Super I/O integrates legacy support features missing in the OSB4 Open South Bridge such as real time clock, serial ports, floppy disk interface, keyboard and mouse controller and a parallel port.

Device Type	I/O Address Space	ISA IRQ
Super I/O	152_{16}	-
Real time clock	$070_{16}..07F_{16}$	8
COM1	$2E8_{16}..2EF_{16}$ $2F8_{16}..2FF_{16}$ $3E8_{16}..3EF_{16}$ $3F8v...3FF_{16}$ [1)]	3 or 4 [1)]
COM2	$2E8_{16}..2EF_{16}$ $2F8_{16}..2FF_{16}$ [1)] $3E8_{16}..3EF_{16}$ $3F8_{16}..3FF_{16}$	3 [1)] or 4
Floppy	$3F0_{16}...3F5_{16}$	IRQ6
Keyboard	$060_{16}...06F_{16}$	IRQ1
Mouse	$060_{16}...06F_{16}$	IRQ12
Parallel Port	$278_{16}...27A_{16}$ / 378h...$37A_{16}$ [1)] $3B0_{16}...3B2_{16}$ / $3BC_{16}...3BE_{16}$	IRQ5 or IRQ7 [1)]

1) Default setting

Real Time Clock

The RTC is fully DS1287, MC14618, PC87911 and Y2K compliant and provides 242 Bytes of battery backed up CMOS RAM. An external +3V lithium battery with a capacity of 200mAh is used for backup during power down. The RTC interrupt is routed to IRQ8 of the ISA bridge.

Serial Ports

The board has three full duplex serial interfaces. They are fully compatible to industry standard 16550 asynchronous communication controller. Serial port 1 and 2 are integrated in the National Semiconductor PC97317 Super I/O device. Both serial ports support baud rates of 600, 1200, 2400, 4800, 9600, 19200, 38400 and 115200. Serial port 1 and 2 are equipped with RS232 line drivers and are routed to the CPCI connector J5. Serial port 1 is also available at the front panel. For the CPCI-736, the serial port 3 is not available via the rear transition board.

Floppy Disk Interface

The integrated floppy disk controller is a superset of uDP8473, uPD765A and the N82077. It supports standard 5.25” and 3.5” floppies. The floppy disk interface is routed to the CPCI connector J5.

Keyboard and Mouse

National Semiconductor PC97317 Super I/O includes a keyboard and mouse controller compliant with 8042H. The keyboard and mouse signals are routed to the CPCI connector J5.

A keyboard/mouse connector is also available at the front panel of the CPCI-735R2.

Parallel Port

The bidirectional parallel port is IEEE1284 compliant and supports Standard Parallel Port (SPP) mode. The parallel port is routed to the CPCI connector J4.

Glue Logic FPGA

Two programmable logic devices connected to the on-board ISA bus are used to implement dedicated board-specific functions and registers.

Device Type	I/O Address Space
Xilinx SpartanXL XCS5XL, XCS10XL	$100_{16}..103_{16}$

IPMI Controller

The IPMI controller unit consists of a MIPS based micro controller Vitesse VSC215, 512 KByte SRAM and 3 MByte flash memory. It can be accessed via the ISA bus (see Table 22 “I/O Address Ranges” page 6-5).

ICMB is connected to the IPMI controller via an RS485 interface. Furthermore, four I2C buses are connected to the IPMI controller with the following buses/devices:

- I2C bus 0: Connected to IPMB0
- I2C bus 1: Connected to IPMB1
- I2C bus 2: Connected to the board information block (BIB) of the PENT/CPCI-735R2/736R2 Family board and of the attached boards/modules and to the power-up controller SMT4004
- I2C bus 3: Connected to on-board temperature sensor

IPMB0 signals are available at CompactPCI connector J1. IPMB1 and ICMB signals are available at CompactPCI connector J4.

Peripheral management functionality can be set manually via switch (see Table 7 “Default Settings” page 2-15). If the manual selection is disabled, automatic selection of PM or Base Board Management Controller (BMC) functionality is activated.

IPMI offers the possibility to explicitly identify the product. This is done by means of the global IPMI command “Get Device ID”. For both, CPCI-735R2 and CPCI-736R2 variants, the product ID is 0804_{16}.

For information on the IPMI firmware and the supported IPMI commands, refer to the IPMI Reference Guide available via SMART.

Temperature Sensor

The board provides temperature sensors measuring CPU and board temperature. The sensor measuring CPU temperature is inside the CPU.

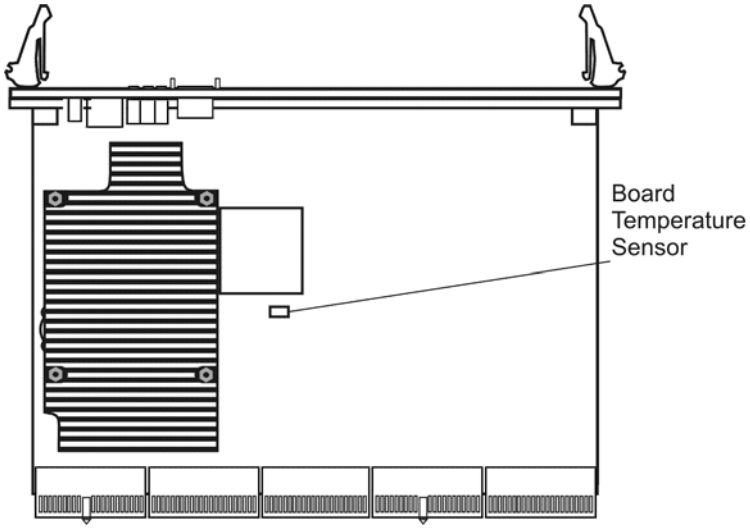


Figure 28: *Location of Board Temperature Sensor*

Note: The temperature sensor is not powered by the IBMU. This means that if the power supply is interrupted, the sensor status at the time of power supply interruption is logged but the current sensor value cannot be read. The current sensor value can be read as soon as the board power is up again.

The temperature sensors are connected to the IPMI controller's I2C bus 3 and can be configured and read via the IPMI controller. The Motorola IPMI firmware already provides sensor data records (SDRs) containing sensor configuration data such as temperature threshold values. For the board temperature, no threshold is defined. For the CPU temperature, a threshold of 110°C is set which cannot be changed. If temperature exceeds this value, the IPMI controller initiates an event which is sent to the system management software and is written into the system event log (SEL).

To check how many SDRs are provided, use the IPMI command "Get Device SDR Info" together with the API of the Motorola VxWorks IPMI driver. To read the SDRs into your system management software, use the IPMI command "Get Device SDR". To add the provided SDRs to the repository, use the IPMI command "Add SDR".

The temperature values can also be read via the Master Write-Read I2C IPMI command and the I2C slave address together with the API of the Motorola VxWorks IPMI driver.

For further information, refer to the *Tornado 2.02 BSP Rel. 1-x for PENT/CPCI-731/735/735R2/736/760/770 Installation Guide* and *Release Notes* and the *IPMI Specification V.1.0.*

Available IPMI Drivers

Motorola provides IPMI drivers to access the IPMI controller for the operating systems VxWorks, Windows 2000 and Linux.

These drivers include an application programming interface (API) to use IPMI commands and the KCS interface. The drivers and respective documentation are available via S.M.A.R.T. Internet Access www.motorola.com/computers.

For further information, refer to the following documentation:

Table 16: *IPMI Driver Documentation*

Driver	Documentation
VxWorks	Tornado 2.02 BSP Rel. 1-x for PENT/CPCI-731/735/735R2/736/760/770 - Installation Guide
	Tornado 2.02 BSP Rel. 2-0 for PENT/CPCI - 735/735R2/736 Release Notes
Windows 2000	PENT/IPMI-Drivers - Installation Guide

I²C Addresses

The following table shows the addresses of devices on the I²C buses attached to the IPMI controller.

Table 17: *I2C Addresses of Devices Attached to IPMI Controller*

Device	I²C Bus	Address
BIB (CPU board)	2	$A0_{16}$
BIB (MEM-735)[1)]	2	$A6_{16}$
BIB (IPMI controller)	2	AE_{16}
Temperature sensor MAX1617	3	30_{16}

1) if assembled

I²C Bus

The local I²C bus is attached to the southbridge.

The I²C interface provides access to board information memory devices such as the board information block (BIB) of the board itself and the RTB (assembly option).

Table 18: *Devices on I²C Bus*

Device	Bus	Address	Size in Byte
Shadow BIB	Connected to south bridge bus #128	$A0_{16}$	512
CIB (Customer I²C memory)	Connected to south bridge bus #128	$A4_{16}$	512
RIB (RTB I²C memory)	Connected to south bridge bus #128	AA_{16}	256

6

Maps and Registers

Overview

This section gives an overview on the I/O and memory maps and describes all board-specific registers.

Table 19: *Register Overview*

Register	Description
BIOS Support register	Page 6-11
COM 3 IRQ register	Page 6-35
Flash Control register	Page 6-24
Hardware Configuration register	Page 6-15
Interrupt Status register	Page 6-36
IPMI IRQ 0 register	Page 6-29
IPMI IRQ 1 register	Page 6-31
IPMI IRQ 2 register	Page 6-32
L_ENUM IRQ register	Page 6-33
LED Control register	Page 6-12
SRAM Configuration register	Page 6-9
PMC 1 IRQ register	Page 6-34
Reset Control register	Page 6-18
Reset Status register	Page 6-19
Software Reset register	Page 6-21
Version register (FPGA 1)	Page 6-13
Version register (FPGA2)	Page 6-27
Watchdog Control register	Page 6-22
Watchdog Retrigger register	Page 6-21

The table below gives an overview of IPMI related register signals. These signals can be used if you wish to use interrupts (e.g. OBF interrupts) in your own IPMI driver. The interrupt status bits may be useful in IPMI watchdog applications, for example, as trigger to back up data before the board is reset.

Table 20: *Overview of IPMI Related Register Signals*

Function	Signal	Description
Indicates whether IPMI controller has been assembled	IPMI_CTRL_ PRESENT	Page 6-15
Masks reset signal driven by IPMI controller	IPMI_RST_ MASK	Page 6-18
Shows occurrence of IPMI reset since last Power-up reset	IPMI_RST_ STATUS	Page 6-19
In order to write your own IPMI driver in interrupt driven mode, the communication with the IPMI controller goes via the interfaces KSC0, KSC1 or KSC2. With IPMI IRQ 0 register you can chose one of eight interrupt levels for the KSC0 interface and with IPMI IRQ 1 register you can chose one of eight interrupt levels for the KSC1 interface. IPMI IRQ 2 register is reserved.	ISA_IRQ_3 ISA_IRQ_5 ISA_IRQ_7 ISA_IRQ_9 ISA_IRQ_10 ISA_IRQ_11 PCI_INT_A PCI_INT_D	Pages 6-29 to 6-32
Indicates occurrence of IPMI IRQ 0, 1 or 2 interrupt	IPMI_IRQ_0 IPMI_IRQ_1 IPMI_IRQ_2	Page 6-36

I/O and Memory Maps

The I/O address ranges of all on-board functional units are shown below.

Table 21: *I/O Address Ranges*

Functionality	Offset
DMA controller 1	$0000_{16}..001F_{16}$
Interrupt controller	$0020_{16}..003F_{16}$
Timer	$0040_{16}..005F_{16}$
Keyboard, mouse	$0060_{16}..006F_{16}$
Real time clock	$0070_{16}..007F_{16}$
Interrupt controller 2	$00A0_{16}..00BF_{16}$
DMA controller 2	$00C0_{16}..00DF_{16}$
Glue logic FPGA	$0100_{16}..0101_{16}$
Secondary IDE	$0170_{16}..0178_{16}$ [1)] or 0376_{16}, 0377_{16}
Primary IDE	$01F0_{16}..01F8_{16}$ [1)] or $03F6_{16}$, $03F7_{16}$
Floppy disk	$03F0_{16}..03F5_{16}$
COM1	$02F8_{16}..02FF_{16}$ or $02E8_{16}..02EF_{16}$ or $03E8_{16}..03EF_{16}$ or $03F8_{16}..03FF_{16}$ [1)]
COM2	$02F8_{16}..02FF_{16}$ [1)] or $02E8_{16}..02EF_{16}$ or $03E8_{16}..03EF_{16}$ or $03F8_{16}..03FF_{16}$
COM3	$02F8_{16}..02FF_{16}$ or $02E8_{16}..02EF_{16}$ or $03E8_{16}..03EF_{16}$ [1)] or $03F8_{16}..03FF_{16}$

Table 21: *I/O Address Ranges (cont.)*

Functionality	Offset
Parallel port SPP mode	$0278_{16}..027A_{16}$ or $0378_{16}..037A_{16}$ or $03B0_{16}..03B2_{16}$ or $03BC_{16}..03BE_{16}$
GPIO	$0C52_{16}$
IPMI_CS0	$0CA2_{16}..0CA5_{16}$
IPMI_CS1	$0CA6_{16}..0CA9_{16}$
IPMI_CS2	0080_{16}
GPCS	$0F50_{16}..0F58_{16}$

1) Default setting

The following table shows the address map of direct addressable on-board nonvolatile memory.

Table 22: *Memory Address Map*

PCI Address Range	Range Size	Device
$FFF00000_{16}..FFFFFFFF_{16}$	1 MByte	On-board flash 5 MByte, pages programmable via register setting (“LED Control Register” page 6-12)
$000C8000_{16}..000CBFFF_{16}$	4 KByte	On-board SRAM
$000C8000_{16}..000CBFFF_{16}$ $000CC000_{16}..000CFFFF_{16}$ or $000D0000_{16}..000D3FFF_{16}$ or $000D4000_{16}..000D7FFF_{16}$ or $000D8000_{16}..000DBFFF_{16}$ or $000DC000_{16}..000DFFFF_{16}$	16 KByte	On-board SRAM (see “FPGA 2” page 6-17)
$000C8000_{16}..000CAFFF_{16}$ or $000CC000_{16}..000CEFFF_{16}$ or $000D0000_{16}..000D2FFF_{16}$ or $000D4000_{16}..000D6FFF_{16}$ or $000D8000_{16}..000DAFFF_{16}$ or $000DC000_{16}..000DEFFF_{16}$	12 KByte	On-board SRAM (see “FPGA 2” page 6-17)

Board-specific registers are realized with two FPGAs. All registers are accessible via Index and Data register of the according FPGA.

The following table gives information on the I/O address of the Index and Data register of FPGA 1 and FPGA 2.

Table 23: *FPGA Address Map*

ISA Bus Address	Register Function
100_{16}	Index register of FPGA 1
101_{16}	Data register of FPGA 1
102_{16}	Index register of FPGA 2
103_{16}	Data register of FPGA 2

FPGA 1

The index address and description of all registers realized within FPGA 1 are shown below.

Table 24: *Index Register FPGA 1*

Index No.	Register Function	Reset/Preset
00_{16}	Reserved	-
01_{16}	SRAM Configuration register	PCI_RST[1)]
02_{16}	BIOS Support register	POWER_UP_RST[2)]
03_{16}	LED Control register	PCI_RST[1)]
04_{16}	Hardware Configuration register	POWER_UP_RST[2)]
05_{16}	Reserved	-
06_{16}	Reserved	-
07_{16}	Reserved	-
08_{16}	Version register	POWER_UP_RST[2)]

1) Any PCI reset causes an initialisation of this register with its default values.
2) Only the power-up reset causes the initialisation of this register with its default values.

SRAM Configuration Register

This register enables / disables the lower 4 KByte of the SRAM (at $B800_{16}$). It maps the remaining 4 KByte of a 8 KByte SRAM in a 4 KByte segment or the remaining 28 KByte of a 32 KByte SRAM in a 16 KByte and 12 KByte segment to base addresses between $C8000_{16}$ an $DC000_{16}$.

Note: If the middle and upper segments of a 32 KByte SRAM are located at the same base address, the middle segment (16 KByte) will be the active segment. The upper segment will be disabled.

Table 25: *SRAM Configuration Register*

Offset: 01_{16}			
Bit	**Signal**	**Description**	**Access**
0	L_SEG	Enables / disables access to lower 4 KByte of SRAM at $B8000_{16}$ 0: Segment disabled (default) 1: Segment enabled	r / w
3..1	M_SEG [2..0]	Locates 4 KByte (if 8 KByte SRAM assembled) or 16 KByte (32 KByte SRAM assembled) to a specified address 000_2: Segment disabled (default) 001_2: Segment located at $C8000_{16}$ 010_2: Segment located at $CC000_{16}$ 011_2: Segment located at $D0000_{16}$ 100_2: Segment located at $D4000_{16}$ 101_2: Segment located at $D8000_{16}$ 110_2: Segment located at $DC000_{16}$	r / w
6..4[1)]	U_SEG [2..0]	Locates upper 12 KByte (if 32 KByte SRAM assembled) to a specified address. 000_2: Segment disabled (default) 001_2: Segment located at $C8000_{16}$ 010_2: Segment located at $CC000_{16}$ 011_2: Segment located at $D0000_{16}$ 100_2: Segment located at $D4000_{16}$ 101_2: Segment located at $D8000_{16}$ 110_2: Segment located at $DC000_{16}$	r / w
7	SRAM_ TYPE	Indicates size of available SRAM. 0: 8 KByte 1: 32 KByte	r / w

1) Not available if 8 KByte SRAM is assembled.

BIOS Support Register

The BIOS Support register is used for BIOS related issues and may not be used.

Caution



Do not write to this register. Writing any values to this register may damage the board or cause it to malfunction.

Table 26: *BIOS Support Register*

Offset: 02_{16}			
Bit	**Signal**	**Description**	**Access**
7..0	Reserved	Reserved	r

LED Control Register

The FPGA controls four bicolored (red / green) LEDs. They can be configured as user LEDs and / or to show the primary and secondary IDE device access and Ethernet 1 and 2 link and activity.

Table 27: *LED Control Register*

Offset: 03_{16}			
Bit	**Signal**	**Description**	**Access**
1..0	1_LEDSTAT	Controls user LED U1. 00_2: OFF 01_2: Red 10_2: Green (default after POST) 11_2: OFF	r / w
3..2	2_LEDSTAT	Controls user LED U2 / IDE. 00_2: OFF 01_2: Red 10_2: Green 11_2: IDE activity - green (default after POST)	r / w
5..4	3_LEDSTAT	Controls user LED U3 / ETH1. 00_2: OFF 01_2: Red 10_2: Green 11_2: Ethernet 1 link / activity - green (default)	r / w
7..6	4_LEDSTAT	Controls user LED U4 / ETH2. 00_2: OFF 01_2: Red 10_2: Green 11_2: Ethernet 2 link / activity - green (default)	r / w

Version Register

The Version register provides the version of the FPGA software in BCD code.

Table 28: *Version Register*

Offset: 08_{16}			
Bit	**Signal**	**Description**	**Access**
3..0	x [3..0]	The most significant four bits specify the first number of the version.	r
7..4	y [3..0]	The least significant four bits specify the second number of the version.	r

Hardware Configuration Register

The Hardware Configuration register provides information about hardware assembly or configuration options. All bits of this register are set once during power up, except bit 5 and 7 which dynamically represent the current state.

Table 29: *Hardware Configuration Register*

Offset: 04_{16}			
Bit	**Signal**	**Description**	**Access**
0	IPMI_CTRL_ PRESENT	Indicates whether IPMI controller has been assembled 0: Not assembled 1: Assembled	r
1	RTB_PRESENT	Indicates whether RTB has been assembled in system 0: Assembled 1: Not assembled	r
3-2	Reserved	Reserved	r
4	IO_736_PRESENT	Indicates whether IO-736 board is assembled or not 0: IO-736 assembled 1: IO-736 not assembled	r
5	EJECT_SWITCH	Shows the state of the board eject handle 0: Handle open 1: Handle closed	r
6	PCI_PRESENT	Shows the status of the PCI_PRESENT signal, identifies whether a CompactPCI bus is available. 0: CompactPCI bus available 1: No CompactPCI bus available	r
7	BLUE_LED_ CONTROL[1)]	Controls the blue HS LED if no CPCI bus is present. 0: Blue LED is not illuminated 1: Blue LED is illuminated	r / w

1) Only available if no CompactPCI bus available, i.e. PCI_PRESENT is 1

FPGA 2

The index address and description of all registers realized within FPGA 2 are shown below.

Table 30: *Index Register FPGA 2*

Index No.	Register Function	Reset/Preset
00_{16}	Reserved	-
01_{16}	Reset Control register	Set through bit '7'[1)]
02_{16}	Reserved	-
03_{16}	Reset Status register	POWER_UP_RST[2)]
04_{16}	Software reset	-
05_{16}	Watchdog Retrigger register	-
06_{16}	Watchdog Control register	Set through bit '7'[1)]
07_{16}	Flash Control register	Set through bit '7'[1)]
08_{16}	Version register	POWER_UP_RST[2)]
09_{16}	IPMI IRQ 0 register	PCI_RST[2)]
$0A_{16}$	IPMI IRQ 1 register	PCI_RST[2)]
$0B_{16}$	IPMI IRQ 2 register	PCI_RST[2)]
$0C_{16}$-10_{16}	Reserved	-
11_{16}	L_ENUM IRQ register	PCI_RST[3)]
12_{16}	PMC 1 IRQ register	PCI_RST[3)]
13_{16}	COM3 IRQ register	PCI_RST[3)]
14_{16}	Reserved	-
15_{16}	IRQ Status register	Set through bit '7'[1)]

1) The value of bit '7' defines whether a reset will cause the initialization of this register with its default values.
2) Only the power-up reset causes the initialization of this register with its default values.
3) Any PCI reset causes the initialization of this register with its default values.

Reset Control Register

The Reset Control register provides the possibility to enable / disable certain reset sources on the board.

Table 31: *Reset Control Register 1*

Offset: 01_{16}			
Bit	**Signal**	**Description**	**Access**
0[1)]	CPCI_RST_MASK	Masks CPCI reset signal. 0: CPCI reset enabled (default) 1: CPCI reset disabled	r / w
1	PB_RST_MASK	Masks CPCI push-button reset (PRST). 0: PRST reset enabled (default) 1: PRST reset disabled	r / w
2[2)]	FP_RST_KEY_MASK	Masks front panel reset key. 0: Reset key enabled (default) 1: Reset key disabled	r / w
3[2)]	RTB_RST_KEY_MASK	Masks RTB reset key. 0: Reset key enabled (default) 1: Reset key disabled	r / w
4[2)]	IPMI_RST_MASK	Masks reset signal driven by IPMI controller. 0: IPMI reset enabled (default) 1: IPMI reset disabled	r / w
5	SOFTWARE_RST_ MASK	Masks reset signal driven by software reset register. 0: Software reset enabled (default) 1: Software reset disabled	r / w
6	Reserved	Reserved 0: default	-
7	RESET_MODE	Indicates whether this register should be initialized with its default values upon reset or not. 0: Register will be set to default values (default). 1: Register keeps its current settings after reset.	r / w

1) The CompactPCI reset is only available if the board is used as peripheral board.
2) This reset key can also be disabled by switch. If it is disabled by switch, this register has no effect.

Reset Status Register

The Reset Status register stores the reset events that occurred since the last power up of the board. The reset events are accumulated and need to be cleared manually. This register will only be reset after power-up reset.

Table 32: *Reset Status Register*

Offset: 03_{16}

Bit	Signal	Description	Access
0[1)]	CPCI_RST_ STATUS	Shows occurrence of CompactPCI-reset since last power-up reset. 0: Reset did not occur 1: Reset did occur	r / w
1	PB_RST_STATUS	Shows occurrence of CPCI push-button reset (PRST) since last power-up reset. 0: Reset did not occur 1: Reset did occur	r / w
2	FP_RST_KEY_ STATUS	Shows occurrence of front panel reset since last power-up reset. 0: Reset did not occur 1: Reset did occur	r / w
3	RTB_RST_KEY_ STATUS	Shows occurrence of RTB reset since last power-up reset. 0: Reset did not occur 1: Reset did occur	r / w
4	IPMI_RST_ STATUS	Shows occurrence of IPMI reset since last Power-Up reset. 0: Reset did not occur 1: Reset did occur	r / w
5	SOFTWARE_RST _MODE	Shows occurrence of software reset since last power-up reset. 0: Reset did not occur 1: Reset did occur	r / w
6	WD_RST_ STATUS	Shows occurrence of watchdog reset since last power-up reset 0: Reset did not occur 1: Reset did occur	r / w
7	PWR_ON	Is set to 1 after power-up reset has occurred. 1: Default	r / w

1) CompactPCI reset status bit is only available if board is running in I/O mode.

Software Reset Register

By writing a magic word (55_{16}) to this register a reset can be performed.

Table 33: *Software Reset Register*

Offset: 04_{16}			
Bit	**Signal**	**Description**	**Access**
7..0	SOFTW_RST	55_{16}: Reset Other than 55_{16}: Normal operation	w

Watchdog Retrigger Register

If the watchdog is enabled, a write access with any value to the Watchdog Retrigger register resets the watchdog timer. To prevent a watchdog time out this must be done at least every time period specified in the Watchdog Control register.

If the watchdog has been configured to cause an NMI that is followed by a reset within one second, the watchdog can also be retriggered within that last second without causing a reset.

Table 34: *Watchdog Retrigger Register*

Offset: 05_{16}			
Bit	**Signal**	**Description**	**Access**
7..0	W_RETRIG	Write access retriggers watchdog.	w

Watchdog Control Register

The watchdog control register controls the functionality of the watchdog.

Note: If bit 7 is set to 1 this register is not reset to its default values upon reset. If the watchdog is enabled and is not handled by the boot software the board gets stuck in a permanent watchdog time-out reset cycle.

Table 35: *Watchdog Control Register*

Offset: 06_{16}			
Bit	**Signal**	**Description**	**Access**
3..0	DIVx	Programs length of watchdog timer (see Table 36 “Watchdog Timer” page 6-23)	r / w
6..4	WDOG_ FUNCTx	Enables watchdog. 000_2: Watchdog disabled (default) 001_2: Reset 010_2: Reserved 011_2: Reserved 100_2: NMI 101_2: NMI followed by a reset after 1s 110_2: Reserved 111_2: Reserved	r / w
7	RESET_MODE	Indicates whether this register should be initialized with its default values upon reset or not. 0: Register will be set to default values (default) 1: Register keeps its current settings after reset	r / w

To implement the watchdog timer the FPGA input clock signal FPGA_CLK14 with a frequency of 14 MHz is used.

Table 36: *Watchdog Timer*

DIVx	FPGA_CLK Divider	Watchdog Timer
00_{16}	2^{19}	37 ms (default)
01_{16}	2^{20}	75 ms
02_{16}	2^{21}	150 ms
03_{16}	2^{22}	300 ms
04_{16}	2^{23}	600 ms
05_{16}	2^{24}	1.2 s
06_{16}	2^{25}	2.4 s
07_{16}	2^{26}	4.8 s
08_{16}	2^{27}	9.6 s
09_{16}	2^{28}	19.2 s
$0A_{16}$	2^{29}	38.3 s
$0B_{16}$	2^{30}	76.7 s (1.2 min)
$0C_{16}$	2^{31}	153.4 s (2.5 min.)
$0D_{16}$	2^{32}	306.8 s (5.1 min.)
$0E_{16}$	2^{33}	613.6 s (10.2 min.)
$0F_{16}$	2^{34}	1227.2 s (20.4 min.)

Flash Control Register

The Flash Control register controls the functionality of the Boot Flash and the User Flash device. It determines the addressing range and which device and page is selected.

Note: If bit 7 is set to 1 this register is not reset to its default values upon reset. If the page is not set to page 0 of the boot flash, BIOS cannot be accessed and the board will not boot after reset.

Table 37: *Flash Control Register*

Offset: 07_{16}			
Bit	**Signal**	**Description**	**Access**
0	FLASH_SEL	Selects which flash device is accessible. 0: Boot flash selected (default) 1: User Flash selected	r / w
1	RANGE	Selects Flash address range between 512KByte and 1 MByte. 0: Address range is 512 KByte (default) A19 bit drives the FLASH_A19 address line. 1: Address range is 1 MByte The ISAbus address line ISA_SA[19] drives the FLASH_A19 address line.	r / w
2[1)]	A19	Drives address line FLASH_A19 of the selected flash device. 0: Address line is driven low. The lowest 512 KByte page of 1 MByte page is selected. 1: Address line is driven high (default). The upper 512 KByte page of 1 MByte page is selected.	r / w
3	A20	Drives address line FLASH_A20 of the selected flash device. 0: Address line is driven low. 1: Address line is driven high (default).	r / w
4	A21	Drives address line FLASH_A21 of the selected flash device. 0: Address line is driven low. 1: Address line is driven high (default).	r / w

Table 37: *Flash Control Register (cont.)*

5[2)]	A22	Drives address line FLASH_A22 of the selected flash device. 0: Address line is driven low. 1: Address line is driven high (default).	r / w
6	WE	Selects between write protect and write enable mode of flash memory. 0: Flash memory write-protected (default) 1: Flash memory enabled for write access	r / w
7	RESET_MODE	Indicates whether this register should be initialized with its default values upon reset or not. 0: Register will be set to default values (default) 1: Register keeps its current settings after reset	r / w

1) If bit 2 of the register (RANGE) is set to 1, bit A19 has no effect.
2) This bit has no function if the board is equipped with 4 MByte User Flash

To access the BIOS on the ISA bus the south bridge provides a 512 KByte or a 1 MByte address window.

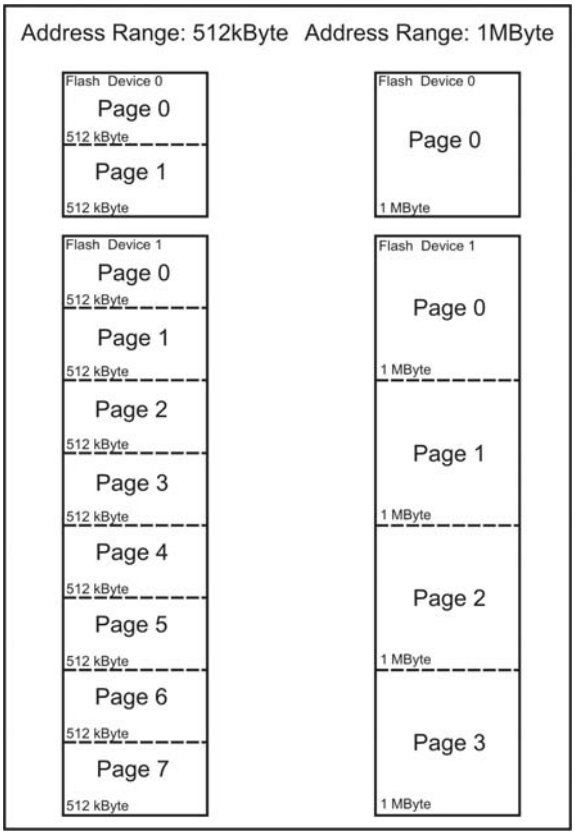


Figure 29: *Flash Device Page Map*

The FPGA allows the mapping of ten pages with a size of 512 KByte or five pages with a size of 1 MByte in the BIOS address range.

Table 38: *Flash Page Addressing*

Device[1)]	Page for 1 MByte Mode (Range 1)	Page for 512 KByte Mode (Range 0)	A19[2)]	A20	A21
0	0	0	0	0	0
0	0	1	1	0	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	2	0	1	0
1	1	3	1	1	0
1	2	4	0	0	1
1	2	5	1	0	1
1	3	6	0	1	1
1	3	7	1	1	1

1) Device 0: Boot Flash, Device 1: User Flash
2) Driven by FPGA (512KByte page mode) or by ISA_SA[19] (1 MByte page mode)

Using 512 KByte BIOS Address Range

The FLASH_A19 address line is provided by the FPGA to the flash memory device to select the lower or the upper 512 KByte block of the 1MByte boot flash device or the lower and upper 512 KByte page in one of the four 1 MByte segments of the user flash device.

The FLASH_A20 and FLASH_A21 address lines can be used to switch to the pages 2-7 in the user flash device. FLASH_A22 is reserved for 8 MBytes user flash devices if required.

Using 1 MByte BIOS Address Range

The 1 MByte address setting is used for programming the flash devices with standard utility software. The software has to be run in protected mode.

The FLASH_A19 address line is directly controlled by the ISAbus address ISA_SA19.

FLASH_A20 and FLASH_A21 are controlled by the Flash Control register bit 3 and bit 4.

Version Register

The Version register provides the version of the FPGA software in BCD code.

Table 39: *Version Register*

Offset: 08_{16}			
Bit	**Signal**	**Description**	**Access**
3..0	x [3..0]	The most significant four bits specify the first number of the version.	r / w
7..4	y [3..0]	The least significant four bits specify the second number of the version.	r / w

IPMI IRQ Register

In order to write your own IPMI driver in interrupt driven mode, the communication with the IPMI controller goes via the interfaces KSC0, KSC1 or KSC2. With the IPMI IRQ 0 register you can chose one of eight interrupts for the KSC0 interface and with the IPMI IRQ 1 register you can chose one of eight interrupts for the KSC1 interface. IPMI IRQ 2 register is reserved.

Caution



Using an interrupt which is already occupied by another device can result in a malfunctioning of the board. Therefore, only use interrupts which are free.

Before choosing an ISA or PCI interrupt, check, e.g. via BIOS, if the interrupt to be used is not occupied by another device.

IPMI IRQ 0

The IPMI IRQ 0 Register provides the possibility to route IPMI IRQ 0 to several ISA IRQs or PCI INT A or INT D.

Table 40: *IPMI IRQ 0 Register*

Offset: 09_{16}			
Bit	**Signal**	**Description**	**Access**
0	ISA_IRQ_3	If this bit is set, the IPMI IRQ 0 is routed to ISA IRQ 3. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
1	ISA_IRQ_5	If this bit is set, the IPMI IRQ 0 is routed to ISA IRQ 5. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
2	ISA_IRQ_7	If this bit is set, the IPMI IRQ 0 is routed to ISA IRQ 7. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
3	ISA_IRQ_9	If this bit is set, the IPMI IRQ 0 is routed to ISA IRQ 9. 0: IRQ not assigned (default) 1: IRQ assigned	r / w

Table 40: *IPMI IRQ 0 Register*

Offset: 09_{16}			
Bit	**Signal**	**Description**	**Access**
4	ISA_IRQ_10	If this bit is set, the IPMI IRQ 0 is routed to ISA IRQ 10. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
5	ISA_IRQ_11	If this bit is set, the IPMI IRQ 0 is routed to ISA IRQ 11. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
6	PCI_INT_A	If this bit is set, the IPMI IRQ 0 is routed to PCI INT A. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
7	PCI_INT_D	If this bit is set, the IPMI IRQ 0 is routed to PCI INT D. 0: IRQ not assigned (default) 1: IRQ assigned	r / w

IPMI IRQ 1

The IPMI IRQ1 Register provides the possibility to route IPMI IRQ 1 to several ISA IRQs or PCI INT A or INT D.

Table 41: *IPMI IRQ 1 Register*

Offset: $0A_{16}$			
Bit	**Signal**	**Description**	**Access**
0	ISA_IRQ_3	If this bit is set, the IPMI IRQ 1is routed to ISA IRQ 3. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
1	ISA_IRQ_5	If this bit is set, the IPMI IRQ 1 is routed to ISA IRQ 5. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
2	ISA_IRQ_7	If this bit is set, the IPMI IRQ 1 is routed to ISA IRQ 7. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
3	ISA_IRQ_9	If this bit is set, the IPMI IRQ 1 is routed to ISA IRQ 9. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
4	ISA_IRQ_10	If this bit is set, the IPMI IRQ 1 is routed to ISA IRQ 10. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
5	ISA_IRQ_11	If this bit is set, the IPMI IRQ 1 is routed to ISA IRQ 11. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
6	PCI_INT_A	If this bit is set, the IPMI IRQ 1 is routed to PCI INT A. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
7	PCI_INT_D	If this bit is set, the IPMI IRQ 1 is routed to PCI INT D. 0: IRQ not assigned (default) 1: IRQ assigned	r / w

IPMI IRQ 2

The IPMI IRQ 2 Register provides the possibility to route IPMI IRQ 2 to several ISA IRQs or PCI INT A or INT D.

Table 42: *IPMI IRQ 2 Register*

Offset: $0B_{16}$			
Bit	**Signal**	**Description**	**Access**
0	ISA_IRQ_3	If this bit is set, the IPMI IRQ 2 is routed to ISA IRQ 3. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
1	ISA_IRQ_5	If this bit is set, the IPMI IRQ 2 is routed to ISA IRQ 5. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
2	ISA_IRQ_7	If this bit is set, the IPMI IRQ 2 is routed to ISA IRQ 7. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
3	ISA_IRQ_9	If this bit is set, the IPMI IRQ 2 is routed to ISA IRQ 9. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
4	ISA_IRQ_10	If this bit is set, the IPMI IRQ 2 is routed to ISA IRQ 10. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
5	ISA_IRQ_11	If this bit is set, the IPMI IRQ 2 is routed to ISA IRQ 11. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
6	PCI_INT_A	If this bit is set, the IPMI IRQ 2 is routed to PCI INT A. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
7	PCI_INT_D	If this bit is set, the IPMI IRQ 2 is routed to PCI INT D. 0: IRQ not assigned (default) 1: IRQ assigned	r / w

L_ENUM IRQ Register

The L_ENUM IRQ register provides the possibility to route SENTINEL's L_ENUM IRQs to several ISA IRQs or PCI INT A or INT D.

Table 43: *L_ENUM Interrupt Register*

Offset: 11_{16}			
Bit	**Signal**	**Description**	**Access**
0	ISA_IRQ_3	If this bit is set, the L_ENUM is routed to ISA IRQ 3. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
1	ISA_IRQ_5	If this bit is set, the L_ENUM is routed to ISA IRQ 5. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
2	ISA_IRQ_7	If this bit is set, the L_ENUM is routed to ISA IRQ 7. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
3	ISA_IRQ_9	If this bit is set, the L_ENUM is routed to ISA IRQ 9. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
4	ISA_IRQ_10	If this bit is set, the L_ENUM is routed to ISA IRQ 10. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
5	ISA_IRQ_11	If this bit is set, the L_ENUM is routed to ISA IRQ 11. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
6	PCI_INT_A	If this bit is set, the L_ENUM is routed to PCI INT A. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
7	PCI_INT_D	If this bit is set, the L_ENUM is routed to PCI INT D. 0: IRQ not assigned (default) 1: IRQ assigned	r / w

PMC 1 IRQ Register

The PMC 1 IRQ register provides the possibility to route the IRQ of PMC slot 1 to several ISA IRQs or PCI INT A or INT D.

Table 44: *PMC 1 IRQ Register*

Offset: 12_{16}			
Bit	**Signal**	**Description**	**Access**
0	ISA_IRQ_3	If this bit is set, the INT signal of PMC 1 is routed to ISA IRQ 3. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
1	ISA_IRQ_5	If this bit is set, the INT signal of PMC 1 is routed to ISA IRQ 5. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
2	ISA_IRQ_7	If this bit is set, the INT signal of PMC 1 is routed to ISA IRQ 7. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
3	ISA_IRQ_9	If this bit is set, the INT signal of PMC 1 is routed to ISA IRQ 9. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
4	ISA_IRQ_10	If this bit is set, the INT signal of PMC 1 is routed to ISA IRQ 10. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
5	ISA_IRQ_11	If this bit is set, the INT signal of PMC 1 is routed to ISA IRQ 11. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
6	PCI_INT_A	If this bit is set, the INT signal of PMC 1 is routed to PCI INT A. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
7	PCI_INT_D	If this bit is set, the INT signal of PMC 1 is routed to PCI INT D. 0: IRQ not assigned (default) 1: IRQ assigned	r / w

COM 3 IRQ Register

The COM 3 IRQ register provides the possibility to route the IRQ of the serial interface COM 3 to several ISA IRQs or PCI INT A or INT D.

Table 45: *COM 3 IRQ Register*

Offset: 13_{16}			
Bit	**Signal**	**Description**	**Access**
0	ISA_IRQ_3	If this bit is set, the INT signal of COM 3 is routed to ISA IRQ 3. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
1	ISA_IRQ_5	If this bit is set, the INT signal of COM 3 is routed to ISA IRQ 5. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
2	ISA_IRQ_7	If this bit is set, the INT signal of COM 3 is routed to ISA IRQ 7. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
3	ISA_IRQ_9	If this bit is set, the INT signal of COM 3 is routed to ISA IRQ 9. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
4	ISA_IRQ_10	If this bit is set, the INT signal of COM 3 is routed to ISA IRQ 10. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
5	ISA_IRQ_11	If this bit is set, the INT signal of COM 3 is routed to ISA IRQ 11. 0: IRQ not assigned (default) 1: IRQ assigned	r / w
7..6	Reserved	-	r / w

Interrupt Status Register

The Interrupt Status register indicates whether one of the following interrupts has occurred even if it is not routed to an external interrupt:

- IPMI IRQ 0
- IPMI IRQ 1
- IPMI IRQ 2
- L_ENUM
- PMC Slot 1
- COM 3

The register can be cleared by writing a '0' to the according register bit.

Table 46: *Interrupt Status Register*

Offset: 15_{16}			
Bit	**Signal**	**Description**	**Access**
0	IPMI_IRQ_0	Indicates occurrence of IPMI IRQ 0 interrupt. 0: Interrupt has not occurred (default) 1: Interrupt has occurred	r / w
1	IPMI_IRQ_1	Indicates occurrence of IPMI IRQ 1 interrupt. 0: Interrupt has not occurred (default) 1: Interrupt has occurred	r / w
2	IPMI_IRQ_2	Indicates occurrence of IPMI IRQ 2 interrupt. 0: Interrupt has not occurred (default) 1: Interrupt has occurred	r / w
3	L_ENUM	Indicates occurrence of L_ENUM interrupt 0: Interrupt has not occurred (default). 1: Interrupt has occurred.	r / w
4	PMC_1_INT	Indicates occurrence of PMC 1 interrupt 0: Interrupt has not occurred (default). 1: Interrupt has occurred.	r / w
5	COM_3_INT	Indicates occurrence of COM 3 interrupt. 0: Interrupt has not occurred (default). 1: Interrupt has occurred.	r / w
6	Reserved	-	r / w
7	RESET_MODE	Indicates whether this register should be initialized with its default values upon reset or not. 0: Register will be set to its default values (default). 1: Register keeps its current settings after reset.	r / w

A

Battery Exchange

Dear Customer,

the battery provides a data retention of five years summing up all periods of actual battery use. Motorola therefore assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.

Caution

- **Incorrect exchange of lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, backup affected data before exchanging the battery.**
- **Always use the same type of lithium battery as is installed.**

The battery is located under the heat sink.

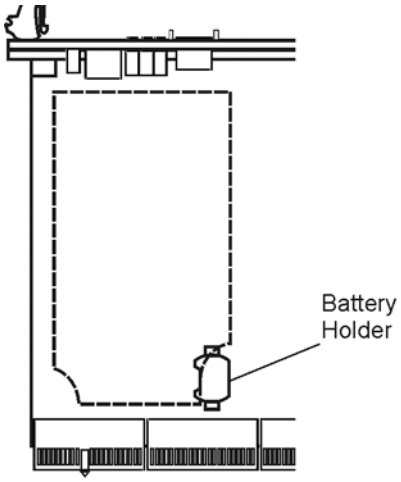


Figure 30: *Battery Location*

In order to exchange the battery, follow the instructions below:

1. Remove board from backplane
   For board removal procedure, see “Board Installation” page 2-18
2. Remove battery

Note: When installing new battery, ensure that the ’+’ on top of battery is face up

3. Press new battery into holder
4. Install board into backplane

B

Troubleshooting

Error List

A typical CompactPCI system is highly sophisticated. This chapter can be taken as a hint list for detecting erroneous system configurations and strange behaviors. It cannot replace a serious and sophisticated pre- and post sales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or services for further support.

Problem	Possible Reason	Solution
Mechanical		
Unable to insert board into backplane	Damaged plugs, bent or broken pins: backplane defect	1. Check CompactPCI slot position to be used for bent or broken pins 2. Replace backplane.
	Board defect	Replace board
	Keying of backplane does not fit to board	1. Check if you use correct board variant and replace board if necessary 2. Replace backplane
During Power-On		
Powering-on the board fails	Backplane voltages for device not within the specified range	1. Check that all backplane voltages are within their specific ranges 2. Check that power supply is capable to drive the respective loads
	Board defect	Replace board
	Damaged plugs, bent or broken pins: backplane defect	1. Check CompactPCI slot position to be used for bent or broken pins 2. Replace backplane.

Problem	Possible Reason	Solution
During Boot-up Procedure		
Board does not boot	Boot device is not partitioned according to used operating system	Check partition according to operating system's needs.
	Boot sequence not correct	Correct boot sequence
	Interrupts are not set correctly	Set interrupts correctly
	Wrong configuration of boot devices	Configure boot devices correctly
During Board Operation		
Application software does not work	Memory ranges of system and peripheral boards do not match	Change application software so that memory ranges match I/O cards and host.
	Not enough disk capacity on mass storage device	Add disk capacity
	Not enough system memory	Add system memory
	Used I/O ranges do not match	Change application software so that I/O ranges match I/O cards and host.
Connected devices do not work	Device defect	Replace device
	Device not connected to power supply	Connect device to power supply
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective device
	Devices are disabled	Configure board correctly
Board runs unstable	Disregard of environmental requirements	1. Check that temperature inside system stays within specified ranges for all system devices 2. Check for hot-spots within system Improve cooling system, if necessary. 3. Check that other environmental values like moisture or altitude are kept within specified ranges

Problem	Possible Reason	Solution
	Drivers are missing, faulty or do not match hardware	1. Check that all used hardware parts have a driver matching the hardware 2. Reinstall hardware drivers
	Board defect	Replace board
Low system performance	Caches are disabled	Enable caches
Memory / PMC module does not work	Module defect	Replace module
	Module not defined for the used board	1. Check if module specification match with interface specification of board. 2. Replace module if specifications do not match
	Module not installed correctly	Check if module fits perfectly in socket.
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective module
RTB does not work	RTB defect	Replace RTB
	RTB installed on wrong slot position	Install RTB on adjacent slot position of the used CPU board.
	RTB not defined for the used peripheral or system board	Install RTB defined for the used peripheral or system board.

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