PPC/PowerCoreCPCI-680

Reference Guide

P / N 214452 Revision AB
September 2001

Copyright

World Wide Web: www.forcecomputers.com
24-hour access to on-line manuals, driver updates, and application notes is provided via SMART, our SolutionsPLUS customer support program that provides current technical and services information.

Headquarters

The Americas

Force Computers Inc.
5799 Fontanoso Way
San Jose, CA 95138-1015
U.S.A.

Tel.: +1 (408) 369-6000
Fax: +1 (408) 371-3382
Email: support@fci.com

Europe

Force Computers GmbH
Prof.-Messerschmitt-Str. 1
D-85579 Neubiberg/München
Germany

Tel.: +49 (89) 608 14-0
Fax: +49 (89) 609 77 93
Email: support@force.de

Asia

Force Computers Japan KK
Shiba Daimon MF Building 4F
2-1-16 Shiba Daimon
Minato-ku, Tokyo 105-0012 Japan

Tel.: +81 (03) 3437 3948
Fax: +81 (03) 3437 3968
Email: smiyagawa@fci.com

214452 420 000 AB

Contents

2 Installation

3 Controls, Indicators and Connectors

8 Maps and Registers

Product Error Report

Tables

Introduction

Installation

Controls, Indicators and Connectors

Devices

PowerBoot for PPC/PowerCoreCPCI-680

Maps and Registers

Figures

Installation

Controls, Indicators and Connectors

Devices

Using This Manual

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), Compact Peripheral Component Interconnect (CPCI), and telecommunications.

Other Sources of Information

For further information refer to:

- *PowerBoot Instruction Set*
  The *PowerBoot Instruction Set* describes the board-independent PowerBoot commands. The *PowerBoot Instruction Set* is packaged separately and shipped with this *Reference Guide*.
- *SENTINEL Reference Guide*
  The *SENTINEL Reference Guide* delivered with this *Reference Guide* describes in detail the SENTINEL universal PCI-to-PCI bridge.

The following data sheets of the board components are relevant to the PPC/PowerCoreCPCI-680. They contain appropriate information on configuring the board and integrating it in systems and can be found on the respective company's webpage.

- PowerPC Microprocessor – Motorola MPC750 or MPC7400 (http://www.motorola.com)
- PPC-to-PCI Bridge – Motorola MPC107 (http://www.motorola.com)
- Ethernet LAN Controller – Intel 82559ER (http://www.intel.com)
- Asynchronous Communication Controller – Texas Instruments TL16C550C (http://www.ti.com)
- PCI-to-ISA Bridge – Winbond W83C553F (http://www.winbond.com)
- CIO – Zilog Z8536 (http://www.zilog.com)

Conventions

Notation	Description
1234	All numbers are decimal numbers except when used with the notations described below
00000000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal point indicator is signalled
Bold	Character format used to emphasize a word
`Courier`	Character format used for on-screen output
`Courier+Bold`	Character format used to characterize user input
Italics	Character format for references, table, and figure descriptions
<text>	Typical notation used for variables and keys
[text]	Typical notation for buttons
...	Repeated item
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges
:	Extents
|	Logical OR
Note:	No danger encountered. Pay attention to important information marked using this layout
Caution 	Possibly dangerous situation: slight injuries to people or damage to objects possible
Danger 	Dangerous situation: injuries to people or severe damage to objects possible

Revision History

SAP No.	Revision	Date	Description
211 718	AA	April 2000	Reference Guide
211 718	AB	July 2000	Added information to SW3-1 and SW3-2 description in Table 4 “Switch Settings” page 2-5; added information to the “PowerBoot for PPC/PowerCoreCPCI-680” chapter; changed CPU clock from E +27 to E +27C in “Example” page 79; added note to “SETBOOT – Editing Auto Boot Parameters” page 712; editorial changes
214 452	AA	January 2001	Modified Table description and changed value of bit 6 and 7 in Table 37 “BSCR Watchdog Control and Status Register” page 8-16 from reserved to WD2_Status and WD2_ACK, modified EMC safety note page xxiii, added copyright page, modified addresses page, editorial changes: modified table layout, replaced Style Conventions and Safety Instructions by “Conventions” page xx,
214452	AB	September 2001	Added “Sicherheitshinweise” page xxvii

Safety Instructions

The following three types of safety instructions appear in this manual. Be sure to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

Danger

Dangerous situation: injuries to people or severe damage to objects possible

Caution

Possibly dangerous situation: no injuries to people but damage to objects possible

Note: No danger encountered. Pay attention to important information marked using this layout.

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the PPC/PowerCoreCPCI-680. For your protection, follow all warnings and instructions found in the following text.

This Reference Guide provides the necessary information to install and handle the PPC/PowerCoreCPCI-680. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The PPC/PowerCoreCPCI-680 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the PPC/PowerCoreCPCI-680. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a Standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules.

Class A is designed to protect against harmful interference when the system is operated in a commercial environment.

The board generates, uses and can radiate radio frequency energy and, if not installed properly and used in accordance with this Reference Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If boards are integrated into open systems, always cover empty slots.

To ensure proper EMC shielding, always operate the PPC/PowerCoreCPCI-680 with the blind panels or with PMC modules installed.

Installation

Electrostatic discharge and incorrect board installation and removing can damage circuits or shorten their life. Therefore:

- **Before installing or removing the board, check the "Requirements" section on page 2-7.**
- **Before touching integrated circuits, ensure that you are working in an ESD-safe environment.**
- **When plugging in the board or removing it, do not press on the front panel but use the handles.**
- **Before installing or removing an additional device or module, read the respective documentation.**
- **Ensure that the board is connected to the CompactPCI backplane via all assembled connectors and that power is available on all power pins.**

Operation

While operating the board ensure that the environmental and power requirements are met.

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the CompactPCI rack and shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Hot Swap

The PPC/PowerCoreCPCI-680 provides hot-swap support, i.e. it may be installed in or removed from a powered system supporting hot swap. Never install or remove the board in a system under hot-swap conditions unless the basic hot-swap, full hot-swap or high-availability platform is used and the system documentation explicitly includes appropriate guidelines. For detailed information on the hot-swap support and the relevant safety notes, see the "Installation in a Powered System Supporting Hot Swap" section on page 2-12. All of the following safety notes refer to the installation and removal of the board in a non-powered system or a system not supporting hot swap.

Expansion

Check the total power consumption of all components installed (see the technical specification of the respective components).

Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Only replace components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMI and the possibly changed functionality of the product.

RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted pair Ethernet (TPE) connectors or for other communication equipment. Mismatching the two connectors may destroy your telephone, your equipment as well as the PPC/PowerCoreCPCI-680. Therefore:

- **TPE connectors near your working area have to be clearly marked as network connectors.**
- **TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The length of the electric cable connected to a TPE bushing must not exceed 100 meters.**

Battery

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**

Environment

Always dispose of used batteries and/or old boards according to your country's legislation.

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Einbau, Betrieb und Wartung des PPC/PowerCoreCPCI-680 zu beachten sind.

Wir sind darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem PPC/PowerCoreCPCI-680 in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem PPC/PowerCoreCPCI-680 um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantiert. Falls Ihnen Informationen fehlen sollten, wenden Sie sich bitte an Ihren Vertreter von Force Computers.

Das PPC/PowerCoreCPCI-680 erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschliesslich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Force Computers ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschliesslich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzewerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Boards in Geschäfts-, Gewerbe- sowie Industriebereichen gewährleisten.

Das Board arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten. Wird das Board in Wohngegenden betrieben, ist der Benutzer verpflichtet, entstehende Störungen auf seine Kosten beheben zu lassen.

Wenn Sie das Board ohne ein PMC Modul verwenden, schirmen Sie freie Steckplätze mit einer Blende ab, um einen ausreichenden EMV Schutz zu gewährleisten. Wenn Sie Boards in Systeme einbauen, schirmen Sie freie Steckplätze mit einer Blende ab.

Installation

Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Beachten Sie deshalb die folgenden Punkte:

- **Bevor Sie Boards oder elektronische Komponenten berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie bei Ein- oder Ausbau des Boards nicht auf die Frontplatte, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Ein- oder Ausbau von zusätzlichen Geräten oder Modulen das dazugehörige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die CompactPCI Backplane angeschlossen ist und Strom an allen Spannungskontakten anliegt.**

Betrieb

Achten Sie darauf, dass die Umgebungs- und die Leistungsanforderungen während des Betriebs eingehalten werden.

Wenn Sie das Board in Gebieten mit elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Board mit dem CompactPCI System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Stellen Sie sicher, dass Anschlüsse und Kabel des Boards während des Betriebs nicht berührt werden können.

Austausch/Erweiterung

Verwenden Sie bei Austausch oder Erweiterung nur von Force Computers empfohlene Komponenten und Systemteile. Andernfalls sind Sie für mögliche Auswirkungen auf EMV und geänderte Funktionalität des Produktes voll verantwortlich.

Überprüfen Sie die gesamte aufgenomme Leistung aller eingebauten Komponenten (siehe die technischen Daten der entsprechenden Komponente). Stellen Sie sicher, dass die Ausgangsströme jedes Verbrauchers innerhalb der zulässigen Grenzwerte liegen (siehe die technischen Daten des entsprechenden Verbrauchers).

Hot Swap

Einbau oder Ausbau des Boards in einem System unter Hot Swap Bedingungen darf nur dann stattfinden, wenn die grundlegende Hot Swap Plattform, die vollständige Hot Swap Plattform, oder die Hochverfügbarkeits Hot Swap Plattform benutzt wird und die Systembeschreibung ausdrücklich die geeigneten Richtlinien vorgibt. Im Abschnitt "Installation in a Powered System Supporting Hot Swap" auf Seite 2-12 finden Sie ausführliche Informationen zur Unterstützung von Hot Swap und die entsprechenden Sicherheitshinweise. Alle folgenden Sicherheitshinweise beziehen sich auf den Ein- und Ausbau des Boards aus einem abgeschalteten System oder aus einem System, das Hot Swap nicht unterstützt.

RJ-45 Stecker

RJ-45 Stecker werden sowohl für Telefonanschlüsse als auch für Twisted-pair-Ethernet (TPE) verwendet. Die Verwechslung solcher Anschlüsse kann sowohl das Telefonsystem als auch das Board zerstören. Daher:

- **TPE-Anschlüsse in der Nähe Ihres Arbeitsplatzes müssen deutlich als Netzwerkanschlüsse gekennzeichnet sein.**
- **An TPE-Buchsen dürfen nur SELV-Kreise angeschlossen werden (Sicherheitskleinspannungsstromkreise).**
- **Die Länge der an einer TPE-Buchse angeschlossenen Leitung darf nicht mehr als 100 Meter betragen.**

Batterie

Muss eine Lithium-Batterie auf dem Board ausgetauscht werden, müssen die folgenden Sicherheitshinweise beachtet werden:

- **Fehlerhafter Austausch von Lithium-Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**
- **Stellen Sie beim Einsetzen der neuen Batterie sicher, daß der Punkt, der sich oben auf der Batterie befindet, den Punkt auf dem Chip abdeckt.**

Umweltschutz

Entsorgen Sie alte Boards gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich umweltfreundlich.

1

Introduction

Overview

The PPC/PowerCoreCPCI-680 is a high-performance universal mode single-board computer providing a peripheral CompactPCI interface. It is based on:

- PowerPC microprocessor
  MPC750 or MPC7400
- Universal PCI-to-PCI bridge SENTINEL
  The universal PCI-to-PCI bridge differentiates between the system slot and any other CompactPCI slot. Consequently, the PPC/PowerCoreCPCI-680 can be used in any CompactPCI slot with the PCI-to-PCI bridge running in the appropriate mode.
- PCI bus

Per default the PPC/PowerCoreCPCI-680 provides one on-board SDRAM memory bank of up to 256 MByte. The memory capacity can optionally be increased up to 1 GByte by installing additional memory modules (see “Power Requirements” page 2-8).

The secondary (L2) cache has a size of up to 1 MByte in case of the MPC750 and up to 2 MByte in case of the MPC7400. The boot flash has a maximum capacity of 1 MByte and the on-board user flash has a maximum capacity of 16 MByte.

The PPC/PowerCoreCPCI-680 includes CompactPCI bus interface, two PMC slots, two Ethernet interfaces, and two serial I/O ports to provide full single-board computer functionality. The serial I/O ports are available at the front panel via 9-pin Micro D-Sub connectors.

The PowerPC CPU runs with a minimum frequency of 400 MHz.
A real-time clock with on-board battery backup is available.
Two independent watchdog timers are available to monitor the CPU activity.

Features

Table 1: *Features of the PPC/PowerCoreCPCI-680*

Feature	Description
Processor	MPC750 or MPC7400 PowerPC microprocessor
Main memory	128-MByte or 256-MByte SDRAM upgradable to max. 1 GByte, 100-MHz operating frequency
PMC slots	Two PMC slots for 32-bit PMC modules, 5V signaling level I/Os for both PMC modules on CompactPCI connectors J3 and J5
CompactPCI bus	SENTINEL universal PCI-to-PCI bridge 32-bit, 33-MHz interface supporting hot swap, 5V signaling level
Local PCI bus	MPC107 PPC-to-PCI bridge 32-bit, 33-MHz interface
Ethernet interface	Two Ethernet controllers 10Base-T or 100Base-TX, one at front panel, one via rear transition board, self-negotiating
Two serial I/O ports	RS-232 compatible I/O at front panel or via rear transition board
Counters/timers	Programmable timers in Zilog Z8536 CIO device, PPC-to-PCI bridge, and PCI-to-ISA bridge
DMA controllers	DMA controllers in PCI-to-ISA bridge, PPC-to-PCI bridge and Ethernet controller
Boot flash	Up to 1 MByte On-board programmable Hardware write protection Two sockets for 512 KByte PLCC flashes each
User flash	Up to 16 MByte On-board programmable Hardware write protection
RTC/SRAM/battery	Real-time clock and NVRAM
Additional features	Reset and abort keys, status/user LEDs, serial PROM for board configuration, one user serial PROM, voltage sensors, watchdog timers
Firmware	PowerBoot

Table 1: *Features of the PPC/PowerCoreCPCI-680*

Feature	Description
Environmental conditions	See "Environmental Requirements" page 2-7
Power consumption	See "Power Requirements" page 2-8
Standards compliance	CompactPCI Specification PICMG 2.0 R2.1 CompactPCI Hot-Swap Specification PICMG 2.1 R1.0 PCI Local Bus Specification Rev. 2.1 IEEE P1386.1 / Draft 2.0 - Layers for PCI Mezzanine Cards: PMC CF+ and CompactFlash Specification Revision 1.4

The PPC / PowerCoreCPCI-680 is available in several memory and speed options. Consult your local Force Computers sales representative to confirm availability of specific combinations.

Product Nomenclature

In the following you find the key for the product name extensions.

Table 2: *Nomenclature of the PPC/PowerCoreCPCI-680*

PPC/PowerCoreCPCI-680/*xxx-ccc*-L*y*-*zz*-(SSIO/CF) (G3)	
xxx	SDRAM size in MByte
ccc	Processor clock frequency in MHz
L*y*	L2 cache capacity in MByte
zz	User flash capacity in MByte
SSIO	Force Computers module with SCSI and serial interfaces
CF	CompactFlash slot
G3	MPC750 PowerPC microprocessor

Ordering Information

The following table is an excerpt from the PPC/PowerCoreCPCI-680 ordering information at the time of print. Contact your local Force Computers representative for current information.

Table 3: *Ordering Information Excerpt*

Product Name	Description
PPC/PowerCoreCPCI-680/…	
...128-450-L1-8 G3	MPC750, 128 MByte SDRAM, 450 MHz processor clock frequency, 1 MByte L2 cache, and 8 MByte user flash
…256-450-L1-8-CF G3	MPC750, 256 MByte SDRAM, 450 MHz processor clock frequency, 1 MByte L2 cache, 8 MByte user flash, and CompactFlash slot
…256-450-L1-16 G3	MPC750, 256 MByte SDRAM, 450 MHz processor clock frequency, 1 MByte L2 cache, and 16 MByte user flash
…256-450-L1-16-SSIO G3	MPC750, 256 MByte SDRAM, 450 MHz processor clock frequency, 1 MByte L2 cache, 16 MByte user flash, and SSIO module
…256-400-L2-16	MPC7400, 256 MByte SDRAM, 400 MHz processor clock frequency, 2MByte L2 cache, and 16 MByte user flash
PPC/PowerCore-SMEM/…	
…256L-100	User upgradable lower SDRAM memory module, 256 MByte, 100-MHz bus frequency
…512U-100	User upgradable upper SDRAM memory module, 512 MByte, 100-MHz bus frequency
Accessories	
ACC/RTB-600	Rear transition board

Factory Options

The following factory options are available:

- Processor type and clock frequency
- Capacity of main memory
- Capacity of user flash
- Capacity of L2 cache
- PN15 connector
- CompactFlash slot for type I or II flash cards

2

Installation

Prerequisites

Before powering up or plugging the board in:

- Read the “Safety Notes” section on page xxiii.
- Check the consistency of the current switch settings (see Figure 1 “Location Diagram (Schematic)” page 2-4).
- Read “Installation” page 2-1 for installation requirements and procedures.

Location Overview

The figure below shows the location of the important PPC / PowerCoreCPCI-680 components. Depending on the board type the board may not include some components shown in the location diagram.

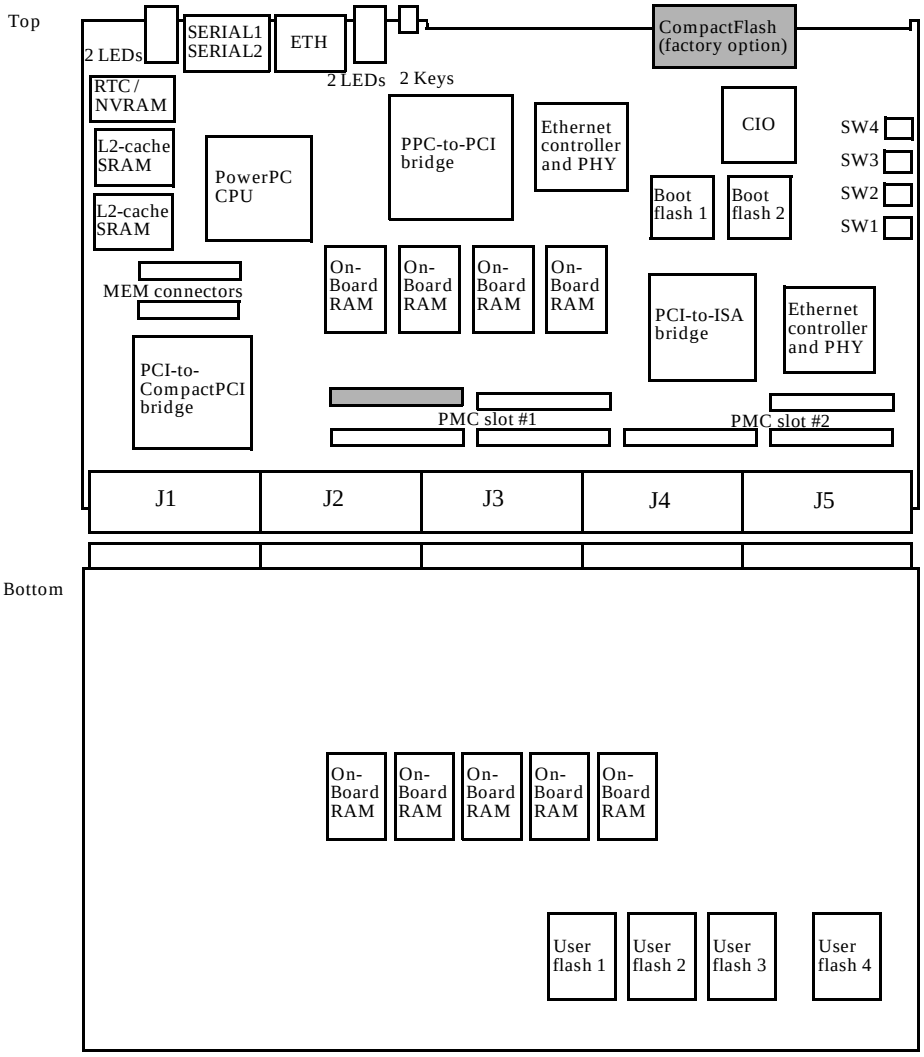


Figure 1: *Location Diagram (Schematic)*

Switch Settings

The following table lists the functions and the default settings of all switches shown in Figure 1 “Location Diagram (Schematic)” page 2-4. The switches are located on the top side of the board and can be switched without removing any module.

Caution

The switch settings have to be checked and changed before the board installation. Do not set/reset the switches during operation.

Table 4: *Switch Settings*

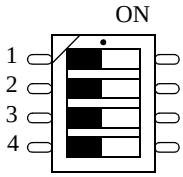
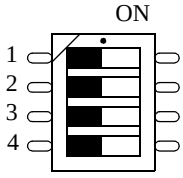
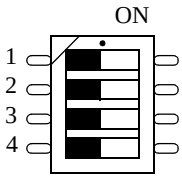
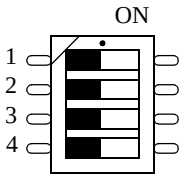
Switch	Setting	Description
SW1		
	SW1-1 OFF	Boot device selection OFF: Booting from boot flash 1 ON: Booting from boot flash 2
	SW1-2 OFF	Enable write access to boot flash OFF: Write-protected ON: Writing enabled
	SW1-3 OFF	User flash write protection OFF: Writing enabled ON: Write-protected
	SW1-4 OFF	General purpose switch (readable by software, no effect to hardware)
SW2		
	SW2-1 OFF	Disable RESET key OFF: Enabled ON: Disabled
	SW2-2 OFF	Disable ABORT key OFF: Enabled ON: Disabled
	SW2-3 OFF	Reserved, must be OFF.
	SW2-4 OFF	Reserved, must be OFF.

Table 4: *Switch Settings (cont.)*

Switch	Setting	Description
SW3		
	SW3-1 OFF	If the signal FAL# is active OFF: No interrupt is generated ON: Interrupt is generated (not available at SSIO variant)
	SW3-2 OFF	If the signal DEG# is active OFF: No interrupt is generated. ON: Interrupt is generated (not available at SSIO variant)
	SW3-3 OFF	Reserved, must be OFF.
	SW3-4 OFF	Reserved, must be OFF.
SW4		
	SW4-1 OFF	Watchdog timer #1 OFF: Disabled ON: Enabled
	SW4-2 OFF	Watchdog timer #2 OFF: Disabled ON: Enabled
	SW4-3 OFF	Watchdog time OFF: NMI: ~32 ms, RESET: ~0.5 s ON: NMI: ~500 ms, RESET: ~2.5 s
	SW4-4 OFF	If SW4-2 is ON OFF: Watchdog timer #2 generates NMI. ON: Watchdog timer #2 generates high-level interrupt.

Requirements

The PPC / PowerCoreCPCI-680 fulfills the standard Force Computers reliability requirements for board products. The power requirements are given below separately because they depend on the product variant.

Environmental Requirements

The environmental conditions must be tested and proven in the used system configuration. These conditions refer to the surroundings of the board within the user environment. Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature. To meet the operating conditions, forced airflow is required at the heat sink of the CPU and at the top side of the board.

Table 5: *Environmental Requirements*

Feature	Operating	Non-operating
Temperature	0°C to +55°C	–40°C to +85°C
Forced airflow	300 LFM (linear feet per minute)	–
Temp. change	±0.5°C / min	±1°C / min
Rel. humidity	5% to 95% non-condensing at +40°C	5% to 95% non-condensing at +40°C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m
Vibration	10 Hz to 15 Hz: 2 mm amplitude 15 Hz to 150 Hz: 2 g	10 Hz to 15 Hz: 5 mm amplitude 15 Hz to 150 Hz: 5 g
Shock	5 g / 11 ms halfsine	15 g / 11 ms halfsine
Free fall	100 mm / 3 axes	1200 mm / all edges and corners (packed state)

Power Requirements

The installation of the PPC/PowerCoreCPCI-680 requires:

- 5V and 3.3V power supply
- ±12V power supply if a PMC module is assembled
- Fan unit providing an airflow meeting the thermal requirements of the board (see Table 5 “Environmental Requirements” page 2-7)
- CompactPCI backplane with P1 and P2 connectors

The 3.3V and 5V voltage levels are watched by voltage sensors to generate a reset of the board if either of the voltage levels drops below the value specified by the *CompactPCI Specification PICMG 2.0 R2.1.* After power up, board operation can be supervised by two watchdog timers. For more information see Figure 6 “PN15 Connector Pinout” page 3-9. The following tables gives examples of typical power requirements for + 5V and +3.3 V without PMC Modules, Memory Modules and CompactFlash Card.

Table 6: *Typical Power Requirements*

Product Variant	+5V	+3.3V
PPC/PowerCoreCPCI-680/128-450-L1-8 G3	1.6A	1.7A
PPC/PowerCoreCPCI-680/256-450-L1-8-CF G3	1.7A	1.8A
PPC/PowerCoreCPCI-680/256-450-L1-16 G3	1.7A	1.8A
PPC/PowerCoreCPCI-680/256-450-L1-16-SSIO G3	2.1A	1.8A
PPC/PowerCoreCPCI-680/256-400-L2-16	1.8A	1.8A

Memory Modules

The available system memory may be increased by one or two additional memory module(s). If your board is equipped with a lower memory module, you may increase the capacity of the memory by installing an additional appropriate (upper) memory module on top of the lower one.
When installing or removing a memory module, observe the following safety notes:

Caution

- **The PPC/PowerCoreCPCI-680 may be equipped only with memory modules qualified by Force Computers. Otherwise the board or connected components may be damaged.**
- **Before installing or removing a memory module turn off power, since the memory modules do not provide hot-swap functionality.**

The following Force Computers memory modules are available:

- PPC / PowerCore-SMEM / 256L-100
- PPC / PowerCore-SMEM / 512U-100

The upgrading instructions are shipped together with the memory modules (see the respective memory module's *Installation Guide*.)

When installing a memory module, you have to consider the overall power consumption. In this case add:

- Power consumption of the CPU board (see Table 6 "Typical Power Requirements" page 2-8)
- Max. power consumption drawn by the memory module(s) (see the table below)

Table 7: *Max. Power Consumption of Memory Modules*

PPC/PowerCore-…	+5V	3.3V
…SMEM / 256L-100	–	0.4A
…SMEM / 512U-100	–	0.6A

PMC Modules

The PPC / PowerCoreCPCI-680 provides two PMC slots which can be used to install PMC modules based on the PCI bus architecture.

Caution

Make sure that the maximum total power consumption of a PMC module at all voltage levels (±12V, +5V, and +3.3V) used does not exceed 7.5W.

Upgrades and Accessories

In this section the installation of additional memory modules and PMC modules available for the PPC/PowerCoreCPCI-680 is described.

Memory Modules

To increase the capacity of the available system memory, one or two memory modules can be installed on the PPC/PowerCoreCPCI-680. For detailed information on the memory modules:

- See "Power Requirements" page 2-8.
- Read the respective memory module's *Installation Guide.*

PMC Modules

Before installing or removing a PMC module:

Caution

- **Read the PMC module's documentation.**
- **Turn off power, since the PMC modules do not provide hot-swap functionality.**

The PPC/PowerCoreCPCI-680 provides two PMC slots for installation of PMC modules. The PCI bus – a high-speed local bus – connects different high-speed I/O cards with the board. The PMC slots are compliant with the *IEEE P1386.1/Draft 2.0 - Layers for PCI Mezzanine Cards: PMC* specification and support 32-bit data bus width with a frequency of 33 MHz.

For information on the power requirements of the PMC modules, see "Power Requirements" page 2-8.
The PCI bus at the PPC/PowerCoreCPCI-680 uses 5V voltage to signal bus levels. The voltage keys prevent 3.3V PMC modules from being plugged into the PMC slots.

Caution

Only the Force Computers PPC/SSIO-6750 PMC module may be installed at the PMC slot #1 of the PPC/PowerCoreCPCI-680/*xxx-ccc*-L*y*-*zz*-SSIO G3 variant and only there.

Installation

In order to install a PMC module, proceed as follows::

1. Remove the PMC blind panel and store it in a safe place to be used again when removing the PMC module.
2. Plug the PMC module on the connectors PN*x*1, PN*x*2, and PN*x*4 at the PMC slot #*x* where *x* = 1 or 2, so that the stand-offs of the module fit on the mounting holes M*x*1, M*x*2, M*x*3, and M*x*4.

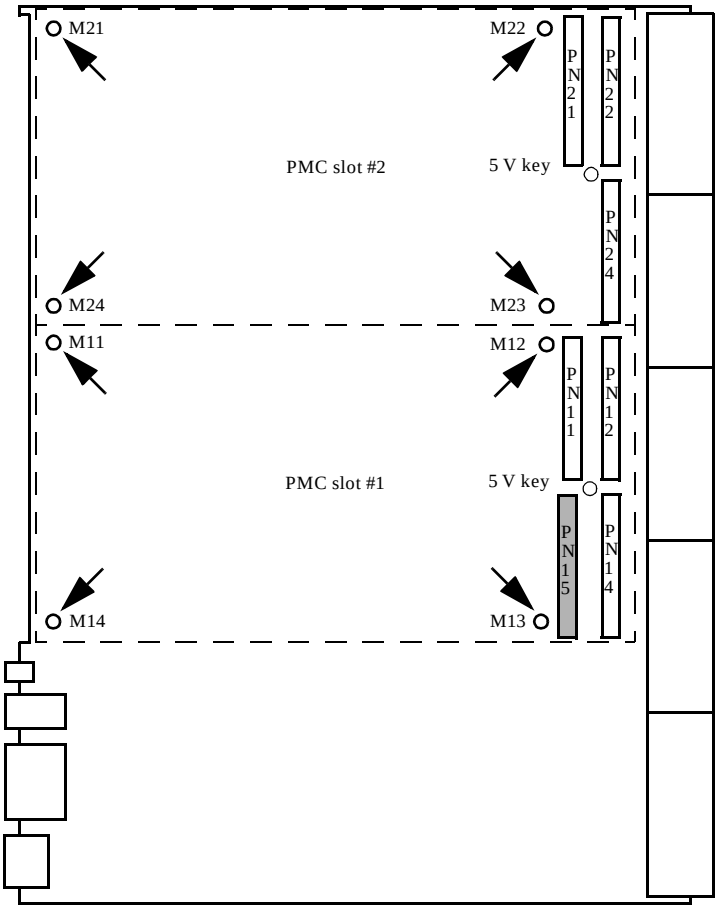


Figure 2: *Mounting Holes of PMC Modules*

Note: Do not remove the 5V key from the board.

3. Fasten the PMC module onto the board with the four screws delivered with the PMC module.

Board Installation

The PPC / PowerCoreCPCI-680 can be used either in a system slot or in a peripheral slot. According to the *CompactPCI Specification PICMG 2.0 R2.1*, the front panel of the PPC / PowerCoreCPCI-680 shows both compatibility glyphs, the triangle and the circle.

The PPC / PowerCoreCPCI-680 provides hot-swap support, i.e. it may be installed in or removed from a powered system supporting hot swap. In this section you will find the instructions for installing the board in a non-powered system and in a powered system supporting hot swap.

Installation in a Non-Powered System

In order to install the PPC / PowerCoreCPCI-680, proceed as follows:

1. Turn power off.
2. Check the switch settings for consistency (see Table 4 “Switch Settings” page 2-5).
3. Plug in the board, depending on its intended function, either in a system slot marked with a triangle or in a peripheral slot marked with a circle.
4. Fasten the board by the handles on the CompactPCI rack.
5. Fasten the board with the screws.
6. Plug in the interface cables in front panel connectors, if applicable.
7. Turn power on.

Installation in a Powered System Supporting Hot Swap

Caution

The PPC/PowerCoreCPCI-680 can be used in non hot-swap platforms, basic hot-swap platforms, full hot-swap platforms, and high-availability platforms. Never install or remove the board under hot-swap conditions unless the basic hot-swap, full hot-swap or high-availability platform is used and the system documentation explicitly includes appropriate guidelines for these tasks. For the system hot-swap support of the board in a system slot, check the system documentation.

The PPC / PowerCoreCPCI-680 is a full hot-swap board. This covers board support in the following situations:

- The basic purpose of the hot-swap support is to allow the board to be installed in and removed from a powered system without adversely affecting system operation. This is done for repairing faulty boards or reconfiguring a system.
- Additionally, the hot-swap support provides programmatic access to hot-swap services allowing system reconfiguration and fault recovery to take place without system downtime and with minimum operator interaction.
- Finally, the hot-swap support allows the system to isolate faulty boards so that the system can continue operating in case of failure – possibly with reduced capability. This is especially useful in the area of high-availability applications, although other typical features may play a prominent role to the user of high-availability systems.

Signals

The PPC / PowerCoreCPCI-680 provides ENUM# and HEALTHY# signals for host or hot-swap-controller (HSC) notification and four control and status bits concerning the hot-swap conditions.

- After installing or before removing the PPC / PowerCoreCPCI-680 in a powered system, the interrupt ENUM# signal is generated and passed to the system host board of the CompactPCI system to indicate a service request.
- The HEALTHY# signal is active whenever all backplane and on-board voltages are within their operating range.
- A set of four control and status bits on each board allows the host software to determine the source of the ENUM# signal and control the blue hot-swap LED.

Control Elements

The PPC / PowerCoreCPCI-680 provides a hot-swap switch (integrated in the lower handle) and a blue LED as an interface with the operator.

- The hot-swap switch allows the operator to indicate the intention to remove the board. The PPC / PowerCoreCPCI-680 implements the hot-swap switch in the lower handle of the front panel.
- The blue hot-swap LED indicates that you are allowed to remove the board.

Caution

- **The removal and installation of the PPC/PowerCoreCPCI-680 under hot-swap conditions described below is allowed only if the board is to be operated in such slots for which hot swap is explicitly permitted by the system documentation (in most hot-swap systems peripheral slots only).**
- **Do not install or remove the board with system power supply turned on when using a non hot-swap platform.**
- **Check what type of system supporting hot swap you are using.**
- **Do not install the board in a system slot and do not remove it from the system slot unless explicitly allowed by the system documentation.**

Removal

The removal procedure depends upon the system the board is to be removed from.

In order to remove the board from a basic hot-swap system, proceed as follows:

1. Start removing the board by disconnecting software manually using the system documentation.
2. Check that the software disconnection process has been completed.
3. Remove the board from the powered system.

In order to remove the board from a full hot-swap or high-availability system, proceed as follows:

1. Open the lower front panel handle.
   The interrupt signal ENUM# is asserted to the CompactPCI backplane to indicate a pending removal.
2. Wait until the hot-swap LED turns blue.
   The hot-swap control and status register bits are appropriately set.

Caution

As long as the blue hot-swap LED is OFF, the board is in normal operation and must not be removed.

3. Remove the board from the powered system.

Installation

The installation procedure depends upon the system the board is to be installed in.

In order to install the board in a basic hot-swap system, proceed as follows:

1. Check the board configuration (switch settings, additional memory modules, PMC modules).
2. Check that you are using an appropriate rear transition board, if applicable.
3. Insert the board into the powered system.
4. Connect software manually according to the system documentation.

Installing the board in the full hot-swap or high-availability system:

1. Check the board configuration (switch settings, additional memory modules, PMC modules).
2. Check that you are using an appropriate rear transition board, if applicable.
3. Insert the board into the powered system.
   The hot-swap LED stays blue until the board software connection process has been completed.

Battery Change

The board is designed to be maintenance-free. However, note that a Lithium battery is installed on the board. The battery provides a data retention of seven years summing up all periods of actual battery use. Therefore, Force Computers assumes that there usually is no need to exchange the Lithium battery except, for example, in the case of long-term spare part handling. Observe the following safety notes:

Caution

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before seven years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is already installed.**
- **When installing the new battery ensure that the dot marked on top of the battery covers the dot marked on the chip.**
- **Used batteries have to be disposed of according to your country's legislation.**

3

Controls, Indicators and Connectors

LEDs, Keys and Interfaces

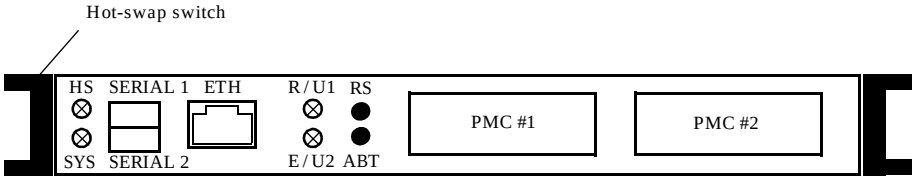


Figure 3: *Front Panel*

Table 8: *LEDs, Keys and Connectors*

Device	Description
HS	Blue hot-swap LED (see also "Installation in a Powered System Supporting Hot Swap" page 2-12): Blue: Board is plugged in or may be removed from the system. OFF: Board must not be removed from the system.
SYS	System controller LED: Yellow: Board is a system controller (plugged into a system slot). OFF: Board is an intelligent I/O board (plugged into a peripheral slot).
SERIAL 1 SERIAL 2	Double 9-pin MicroD-Sub connector for two serial ports (see "Serial I/O Ports" page 3-5)
ETH	8-pin RJ-45 connector for a 100Base-TX or 10Base-T Ethernet interface (see "Ethernet Interface" page 3-6)
R/U1	In Hardware-LED mode (default): RUN/RESET LED indicating the board status: Green: Normal operation Red: Reset is active. In User-LED mode (programmable by software): USER LED 1: Can be programmed to be red, green or OFF.
E/U2	In Hardware-LED mode (default): Ethernet green and red LED indicating the status of the Ethernet #1 and #2 interfaces respectively: ON: Ethernet link is available. Blinking: Data is transferred. In User-LED mode (programmable by software): USER LED 2: Can be programmed to be red, green or OFF.

Table 8: *LEDs, Keys and Connectors (cont.)*

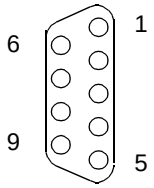
Device	Description
RS	Mechanical RESET key: When toggled it instantaneously affects the board by generating a reset (if not disabled by switch SW2-1). A reset of all on-board I/O devices and the CPU is performed when the reset key is pushed to the active position. To avoid unintentional reset, the reset key is recessed in the front panel. For information on disabling the key see "SW2-1" page 2-5.
ABT	Mechanical ABORT key: When toggled it instantaneously affects the board by generating a non-maskable interrupt (NMI) request via the PCI-to-ISA bridge (if not disabled by switch SW2-2). This allows to implement an abort of the current program, to trigger a self-test, or to start a maintenance program. To avoid unintentional abort, the abort key is recessed in the front panel. For information on enabling the key see "SW2-2" page 2-5.
PMC #1 PMC #2	PMC slots for installation of two PMC modules based on the PCI bus architecture. For the installation instructions see "PMC Modules" page 2-10, for the PMC connector pinouts see "PMC Slots" page 3-6.
Hot-swap switch	Hot-swap switch integrated in the lower handle. When the handle is opened during normal operation the interrupt signal ENUM# is asserted on the CompactPCI backplane. This interrupt indicates insertion of a new board or the pending removal of a board (see also "Installation in a Powered System Supporting Hot Swap" page 2-12).

Serial I/O Ports

The PPC/PowerCoreCPCI-680 provides two serial I/O ports. The RS-232 serial I/O ports #1 and #2 are both available via a double 9-pin MicroD-Sub connector at the front panel. Each serial I/O port is also routed to the CompactPCI connector J3 (see Figure 7 “Pinout of the CompactPCI Connector J3, Rows A…E” page 3-12) and therefore available at a rear transition board.

Note: The serial I/O ports must not be connected simultaneously at the front panel and via the rear transition board. However, it is allowed e.g. to connect the serial I/O port #1 at the front panel and the serial I/O port #2 via the rear transition board at the same time.

Table 9: *Pinout of RS-232 Serial I/O Ports*

Connector	Pin	Signal
9-pin MicroD-Sub 	1	DCD (Data Carrier Detect, input)
	2	RXD (Receive Data, input)
	3	TXD (Transmit Data, output)
	4	DTR (Data Terminal Ready, output)
	5	GND (Ground)
	6	DSR (Data Set Ready, input)
	7	RTS (Request to Send, output)
	8	CTS (Clear to Send, input)
	9	RI (Ring Indicator)

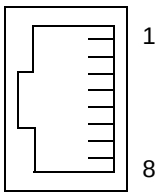
Default port setup:

- RS-232 asynchronous communication
- 9600 baud, eight data bits, one start bit, one stop bit, no parity
- No handshake protocol used per default

Ethernet Interface

The PPC/PowerCoreCPCI-680 provides two 10Base-T or 100Base-TX Ethernet interfaces. The Ethernet interface #1 is available via an 8-pin RJ-45 connector at the front panel. The Ethernet interface #2 is routed via CompactPCI connector J5 (see Figure 8 “Pinout of the CompactPCI Connector J5, Rows A…E” page 3-13) and is available via a rear transition board.

Table 10: *Pinout of the Ethernet Interface #1 Connector*

Connector	Pin	Signal
8-pin RJ-45 	1	TX+
	2	TX–
	3	RX+
	4	n.c.
	5	n.c.
	6	RX–
	7	n.c.
	8	n.c.

PMC Slots

In this section the PMC connectors and the ISA connector PN15 are described. The ISA connector is available as a factory option and makes available a set of ISA bus signals and interrupt request signals.

PMC Connectors

The 32-bit PCI bus requires two PMC connectors for each PMC slot. The third PMC connector PN*x*4, where *x* is 1 and 2 for the PMC slots #1 and #2 respectively, connects additional user I/O signals of the respective PMC slot with the CompactPCI bus J3 and J5 connectors.
PMC slot #1:

- PN11 and PN12 for the PCI bus
- PN14 for 64 user I/O signals

PMC Slot #2:

- PN21 and PN22 for the PCI bus
- PN24 for 64 user I/O signals

Note: The PMC slots #1 and #2 have 64 user I/O signals each. All signals of the PMC slot #1 are available on the connector J3 (see Figure 7 "Pinout of the CompactPCI Connector J3, Rows A…E" page 3-12) and all signals of the PMC slot #2 are available on the connector J5 (see Figure 8 "Pinout of the CompactPCI Connector J5, Rows A…E" page 3-13).

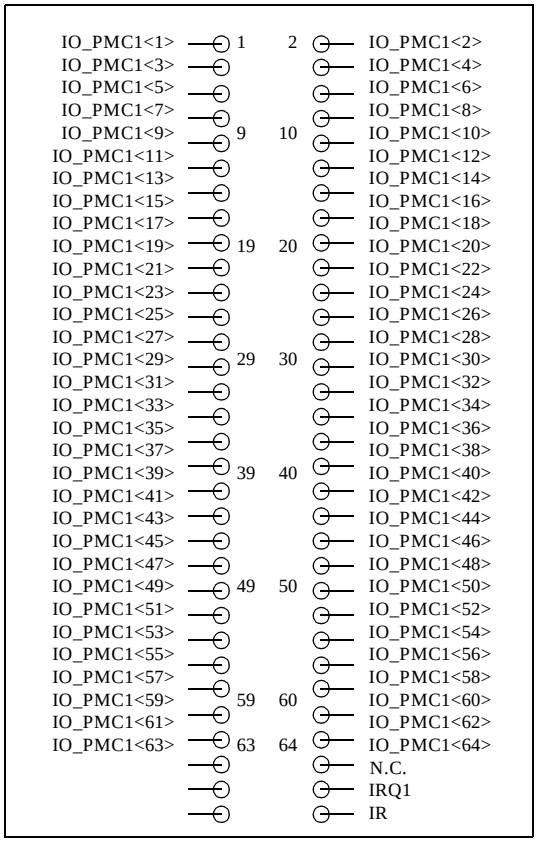


Figure 4: *PN14 Connector Pinout*

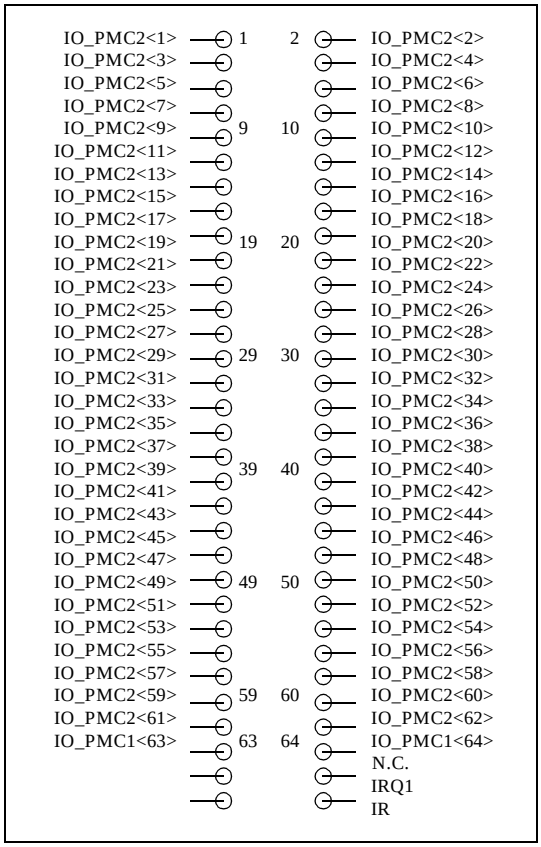


Figure 5: *PN24 Connector Pinout*

ISA Connector

The PN15 connector makes available a set of ISA bus signals and interrupt request signals. The following figure shows the signals available on the ISA connector.

Note: The PN15 connector is only assembled at the PPC/PowerCoreCPCI-680/*xxx-ccc*-L*y-zz*-SSIO G3 variant.

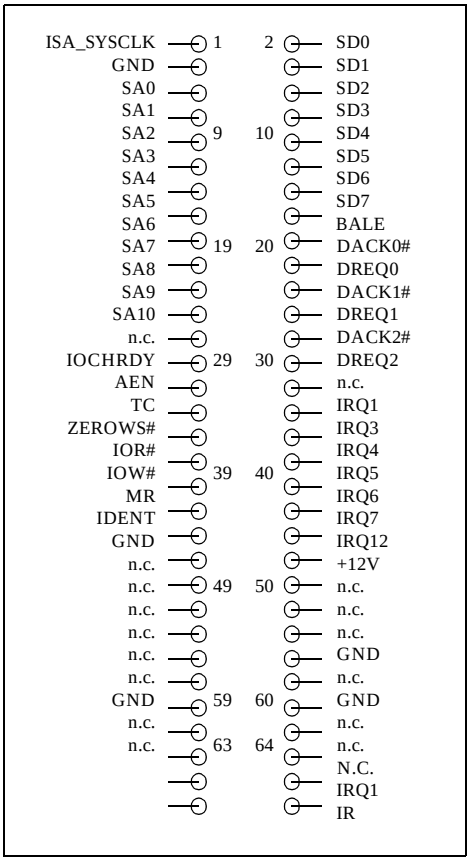


Figure 6: *PN15 Connector Pinout*

Automatic Power Up, Voltage Sensor and Watchdog Timer

The PPC/PowerCoreCPCI-680 implements control logic to automatically power up and reset the board depending on the 3.3V or 5V voltage levels. After power up, board operation can be supervised by two watchdog timers.

Voltage Sensors

If the 3.3V or 5V voltage level drops below the values given by the *CompactPCI Specification PICMG 2.0 R2.1*, the voltage sensors automatically generate a reset of the board and proceed with a normal booting procedure. The +12V and –12V voltage levels are neither observed nor used by the PPC/PowerCoreCPCI-680. If a PMC module uses the +12V or –12V voltage, the voltage must be observed by the PMC module.

Watchdog Timers

Two watchdog timers disabled per default are available on the PPC/PowerCoreCPCI-680:

- Watchdog timer #1

  Watchdog timer #1 can be enabled via the switch SW4-1 (see “SW4-1” page 2-6). The expiry time can be selected by the switch SW4-3 (see “SW4-3” page 2-6). If the watchdog timer #1 is enabled, it generates a reset after the selected time has expired.

- Watchdog timer #2

  Watchdog timer #2 can be enabled via the switch SW4-2 (see “SW4-2” page 2-6). The expiry time can be selected by the switch SW4-3 (see see “SW4-3” page 2-6). Depending on the setting of the switch SW4-4 the enabled watchdog timer #2 generates a non-maskable interrupt (NMI) or a high-level interrupt after the selected time has expired.

CompactPCI Interface

The PPC/PowerCoreCPCI-680 provides a CompactPCI interface capable to be used either in a system slot or in a peripheral slot. The features of the CompactPCI interface are:

- 32-bit width
- 33 MHz bus frequency
- 5V signaling level
- Full hot-swap support
- Working as host board in a system slot or as intelligent I/O board in a peripheral slot

Note: Before installing the board in or removing it from a powered system, check the system documentation (see "Installation in a Powered System Supporting Hot Swap" page 2-12).

J1 and J2 Connectors

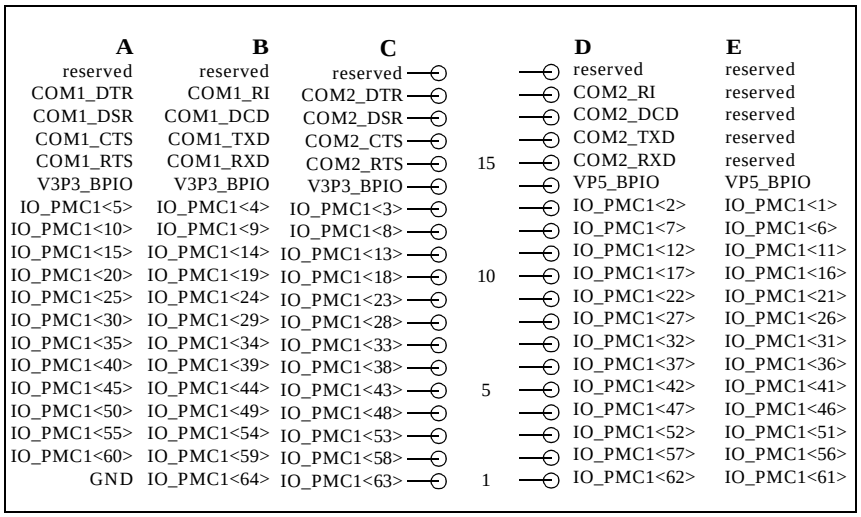
The CompactPCI connectors J1 and J2 implement the CompactPCI 64-bit connector pinout as specified by the *CompactPCI Specification PICMG 2.0 R2.1*.

J3 and J5 Connectors

The following naming conventions for the user I/O signals available on the CompactPCI connectors J3 and J5 are used:

- IO_PMC1<*x*> and IO_PMC2<*x*> are the user defined I/O signals from the PMC I/O connectors PN14 and PN24 respectively, where *x* corresponds to the pin number of the PMC I/O connectors (see Figure 4 "PN14 Connector Pinout" page 3-7 and Figure 5 "PN24 Connector Pinout" page 3-8).
- COM1_ .. and COM2_ .. are the signals of the serial I/O ports #1 and #2 respectively.
- ETH2_ .. are the differential twisted pair signals from the Ethernet interface #2.

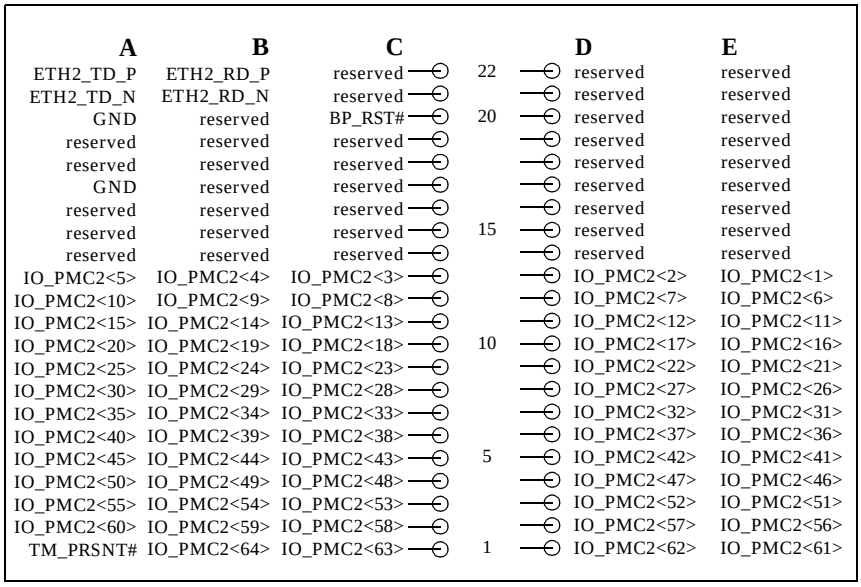
- BP_RST# (backpanel-reset) is an active low reset input that can be connected to a push-button reset (that connects to GND to request a reset).
- TM_PRSNT# (transition module present) is an input that indicates if a rear transition board is connected to the board.
- GND are signal reference ground pins.
- V3P3_BPIO is a 3.3V voltage supply that is fused to about 1.5A on the board (total current through all V3P3_BPIO connector pins).
- VP5_BPIO is a 5V voltage supply that is fused to about 2A on the board (total current through all VP5_BPIO connector pins).



	A	B	C		D	E
	reserved	reserved	reserved		reserved	reserved
	COM1_DTR	COM1_RI	COM2_DTR		COM2_RI	reserved
	COM1_DSR	COM1_DCD	COM2_DSR		COM2_DCD	reserved
	COM1_CTS	COM1_TXD	COM2_CTS		COM2_TXD	reserved
	COM1_RTS	COM1_RXD	COM2_RTS	15	COM2_RXD	reserved
	V3P3_BPIO	V3P3_BPIO	V3P3_BPIO		VP5_BPIO	VP5_BPIO
	IO_PMC1<5>	IO_PMC1<4>	IO_PMC1<3>		IO_PMC1<2>	IO_PMC1<1>
	IO_PMC1<10>	IO_PMC1<9>	IO_PMC1<8>		IO_PMC1<7>	IO_PMC1<6>
	IO_PMC1<15>	IO_PMC1<14>	IO_PMC1<13>		IO_PMC1<12>	IO_PMC1<11>
	IO_PMC1<20>	IO_PMC1<19>	IO_PMC1<18>	10	IO_PMC1<17>	IO_PMC1<16>
	IO_PMC1<25>	IO_PMC1<24>	IO_PMC1<23>		IO_PMC1<22>	IO_PMC1<21>
	IO_PMC1<30>	IO_PMC1<29>	IO_PMC1<28>		IO_PMC1<27>	IO_PMC1<26>
	IO_PMC1<35>	IO_PMC1<34>	IO_PMC1<33>		IO_PMC1<32>	IO_PMC1<31>
	IO_PMC1<40>	IO_PMC1<39>	IO_PMC1<38>		IO_PMC1<37>	IO_PMC1<36>
	IO_PMC1<45>	IO_PMC1<44>	IO_PMC1<43>	5	IO_PMC1<42>	IO_PMC1<41>
	IO_PMC1<50>	IO_PMC1<49>	IO_PMC1<48>		IO_PMC1<47>	IO_PMC1<46>
	IO_PMC1<55>	IO_PMC1<54>	IO_PMC1<53>		IO_PMC1<52>	IO_PMC1<51>
	IO_PMC1<60>	IO_PMC1<59>	IO_PMC1<58>		IO_PMC1<57>	IO_PMC1<56>
	GND	IO_PMC1<64>	IO_PMC1<63>	1	IO_PMC1<62>	IO_PMC1<61>

Figure 7: *Pinout of the CompactPCI Connector J3, Rows A…E*

Note: Reserved pins must not be connected.



A	B	C		D	E
ETH2_TD_P	ETH2_RD_P	reserved	22	reserved	reserved
ETH2_TD_N	ETH2_RD_N	reserved		reserved	reserved
GND	reserved	BP_RST#	20	reserved	reserved
reserved	reserved	reserved		reserved	reserved
reserved	reserved	reserved		reserved	reserved
GND	reserved	reserved		reserved	reserved
reserved	reserved	reserved		reserved	reserved
reserved	reserved	reserved	15	reserved	reserved
reserved	reserved	reserved		reserved	reserved
IO_PMC2<5>	IO_PMC2<4>	IO_PMC2<3>		IO_PMC2<2>	IO_PMC2<1>
IO_PMC2<10>	IO_PMC2<9>	IO_PMC2<8>		IO_PMC2<7>	IO_PMC2<6>
IO_PMC2<15>	IO_PMC2<14>	IO_PMC2<13>		IO_PMC2<12>	IO_PMC2<11>
IO_PMC2<20>	IO_PMC2<19>	IO_PMC2<18>	10	IO_PMC2<17>	IO_PMC2<16>
IO_PMC2<25>	IO_PMC2<24>	IO_PMC2<23>		IO_PMC2<22>	IO_PMC2<21>
IO_PMC2<30>	IO_PMC2<29>	IO_PMC2<28>		IO_PMC2<27>	IO_PMC2<26>
IO_PMC2<35>	IO_PMC2<34>	IO_PMC2<33>		IO_PMC2<32>	IO_PMC2<31>
IO_PMC2<40>	IO_PMC2<39>	IO_PMC2<38>		IO_PMC2<37>	IO_PMC2<36>
IO_PMC2<45>	IO_PMC2<44>	IO_PMC2<43>	5	IO_PMC2<42>	IO_PMC2<41>
IO_PMC2<50>	IO_PMC2<49>	IO_PMC2<48>		IO_PMC2<47>	IO_PMC2<46>
IO_PMC2<55>	IO_PMC2<54>	IO_PMC2<53>		IO_PMC2<52>	IO_PMC2<51>
IO_PMC2<60>	IO_PMC2<59>	IO_PMC2<58>		IO_PMC2<57>	IO_PMC2<56>
TM_PRSNT#	IO_PMC2<64>	IO_PMC2<63>	1	IO_PMC2<62>	IO_PMC2<61>

Figure 8: *Pinout of the CompactPCI Connector J5, Rows A…E*

Note: Reserved pins must not be connected.

4

Testing the Board Using PowerBoot

PowerBoot is firmware providing some basic test and debug commands. It is stored in the on-board Boot PROM. In this section a procedure to test the board using PowerBoot is described.
PowerBoot automatically starts after power up or reset. After the successful pass of the self-initialization routine, the following message or a similar one will appear on the screen:

```
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller 1 at address: 0xFE870000
Init Ethernet Controller 2 at address: 0xFE880000
PMC1/2: no auto mapping setup
Found PCI-to-PCI bridge/device SENTINEL - Host mode
Init PCI-to-PCI Host bridge at address: 0xFE890000
Probelist for CompactPCI I/O slots:  2, 3, 4, 5, 6, 7, 8,
Testing NVRAM.....................done
Testing RAM ......................done
Testing Boot FLASH....CSUM 0xABCD..done
Testing PCI Bus ..................done
Testing ISA ......................done
Testing Ethernet Controller1.......done
Testing Ethernet Controller2.......done
Found CPU7400/G4, PVR=000C0200,
CPU clock: 350MHz, Bus clock: 100MHz, E
SDRAM mode enabled
Onboard DRAM       :  128MB, 0x00000000..0x03FFFFFF
Init SDRAM Module 1:  none
Init SDRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 140MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board
BIB version: 2.0
Ethernet 1: 00:80:42:0E:30:32
Ethernet 2: 00:80:42:0E:30:33

<<PowerBoot V3.30 for PowerCoreCPCI CPU-680>>

PowerBoot> _
```

To test the board for correct operation enter `probepci`. `probepci` does not provide a full-featured power-on self-test. However, it tests some I/O devices and scans the PCI bus for participants. Depending on the board configuration, a message like the following will appear.

```
PowerBoot> probepci
Probing PCIbus at 0x80000000
Device ID = 0x0004; Vendor ID = 0x1057;
Status    = 0x00A0; Command   = 0x0016;
Base Class= 0x06;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x10;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x08;
base addr0= 0x00000008, base addr1= 0x00000000;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x01;   IRQ Line  = 0x00;
Found PCI device: Motorola MPC107 PowerPC PCI bridge

Probing PCIbus at 0x8000C000
Device ID = 0x0001; Vendor ID = 0x1146;
Status    = 0x0210; Command   = 0x0017;
Base Class= 0x06;   Sub Class = 0x80;   Prg. Inter= 0x00;   Rev. ID   = 0x00;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x08;
base addr0= 0xFFFFF000, base addr1= 0x00890001;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x01;   IRQ Line  = 0x00;
Found PCI device: FORCE Computers SENTINEL PCI-to-PCI Bridge

Probing PCIbus at 0x8000C800
Device ID = 0x1229; Vendor ID = 0x8086;
Status    = 0x0290; Command   = 0x0017;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x08;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x08;
base addr0= 0xFFFFF000, base addr1= 0x00870001;
Max Lat   = 0x38;   Min Gnt   = 0x08;   IRQ Pin   = 0x01;   IRQ Line  = 0x00;
Found PCI device: Intel i82559 Ethernet Controller

Probing PCIbus at 0x8000E000
Device ID = 0x1229; Vendor ID = 0x8086;
Status    = 0x0290; Command   = 0x0017;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x08;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x20;   Cache Line= 0x08;
base addr0= 0xFFFFF000, base addr1= 0x00880001;
Max Lat   = 0x38;   Min Gnt   = 0x08;   IRQ Pin   = 0x01;   IRQ Line  = 0x00;
Found PCI device: Intel i82559 Ethernet Controller

Probing PCIbus at 0x8000F000
Device ID = 0x0565; Vendor ID = 0x10AD;
Status    = 0x0200; Command   = 0x0007;
Base Class= 0x06;   Sub Class = 0x01;   Prg. Inter= 0x00;   Rev. ID   = 0x10;
BIST      = 0x00;   Header Typ= 0x80;   Latency Ti= 0x00;   Cache Line= 0x00;
base addr0= 0x00000000, base addr1= 0x00000000;
Max Lat   = 0x00;   Min Gnt   = 0x00;   IRQ Pin   = 0x00;   IRQ Line  = 0x00;
Found PCI device: Winbond W83C553F Sys. I/O Con., function 0
```

```
Probing PCIbus at 0x8000F100
Device ID = 0x0105; Vendor ID = 0x10AD;
Status    = 0x0280; Command   = 0x0000;
Base Class= 0x01;   Sub Class = 0x01;   Prg. Inter= 0x8F;   Rev. ID   = 0x05;
BIST      = 0x00;   Header Typ= 0x80;   Latency Ti= 0x00;   Cache Line= 0x08;
base addr0= 0x000001F1, base addr1= 0x000003F5;
Max Lat   = 0x28;   Min Gnt   = 0x02;   IRQ Pin   = 0x01;   IRQ Line  = 0x0E;
Found PCI device: Winbond W83C553F IDE, function 1

Probing PCIbus at 0x8000F800
PowerBoot>
```

5

Devices

Block Diagram

The block diagram shows how the PPC/PowerCoreCPCI-680 devices work together and which data paths they use.

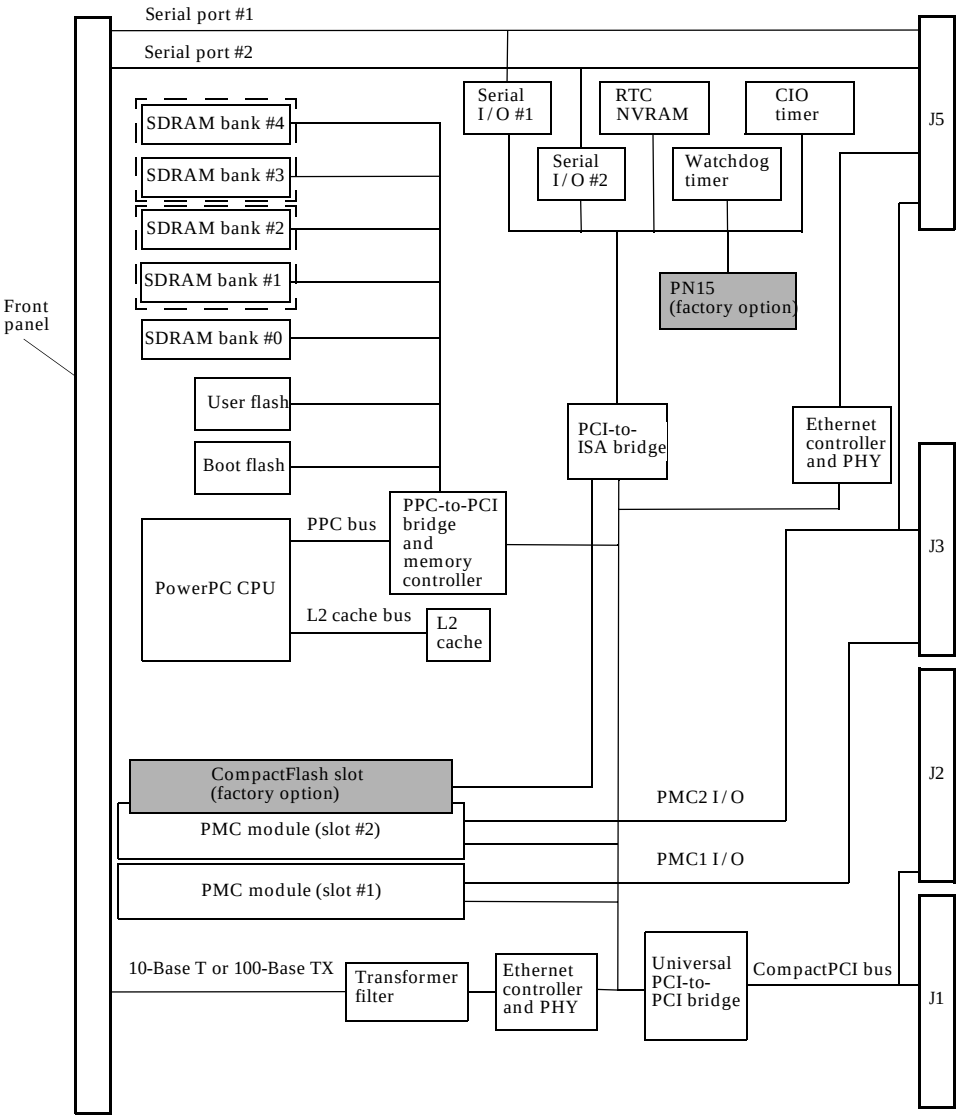


Table 11: *Buses and Connected Devices*

Bus	Clock Frequency	Data Bus Width	Endian Mode	Connected Devices
L2-cache	≤200 MHz	64 bit	Big endian	PowerPC CPU L2-cache memory
PPC	100 MHz	64 bit	Big endian	PowerPC CPU PPC-to-PCI bridge / memory controller
Memory	100 MHz	64 bit	Big endian	PPC-to-PCI bridge / memory controller On-board SDRAM bank 0 SDRAM banks 1 to 4 (memory modules) Boot flash memory User flash memory
Local PCI	33 MHz	32 bit	Little endian	PPC-to-PCI bridge / memory controller PMC slots #1 and #2 Two Ethernet controllers PCI-to-CompactPCI bridge PCI-to-ISA bridge
CompactPCI	33 MHz	32 bit	Little endian	PCI-to-CompactPCI bridge CompactPCI connectors J1 and J2
ISA	8.25 MHz	8 bit	Little endian	PCI-to-ISA bridge Two serial I / O controllers RTC / NVRAM Watchdog timers

PowerPC CPU

The MPC750 or MPC7400 PowerPC microprocessor is one of the basic components of the PPC / PowerCoreCPCI-680.
For detailed information refer to the *PowerPC User's Manual* available from Motorola Semiconductors.
The MPC750 and MPC7400 PowerPC microprocessors consist of a processor core and an internal L2 tag RAM combined with a dedicated L2 cache interface and a PPC bus interface. They provide:

- 32-bit effective addresses
- Integer data types of 8, 16, and 32 bits
- Floating-point data types of 32 and 64 bits

Execution Units

The MPC750 and MPC7400 PowerPC microprocessors are superscalar processors sustaining a peak throughput of three instructions per clock. They include the following independent execution units:

- Floating-point unit
- Two fixed-point units
- Load and store unit
- Cache and memory unit
- AltiVec vector unit (MPC7400 only)

Additional Features

Additional features of the MPC750 and MPC7400 PowerPC microprocessors include:

- 32-KByte L1 data cache (eight-way set-associative)
- 32-KByte L1 instruction cache (eight-way set-associative)
- Support of up to 1 MByte (MPC750) and 2 MByte (MPC7400) L2 cache (two-way set-associative)
- Memory management unit (MMU) with 128 entries, two-way set-associative instruction TLB with 128 entries, two-way set-associative data TLB

L2 Cache

The PPC/PowerCoreCPCI-680 provides an L2 cache of up to 2 MByte. The L2 cache is controlled by the L2 cache controller of the PowerPC CPU. The L2 tag is two-way set-associative with 8K-entry tags per way. For further information on programming the L2 cache controller see the *PowerPC User's Manual* available from Motorola Semiconductors.

The available size of the L2 cache can be read by the software from the DCCR A, bits [7..6] (see Table 30 "DCCR A" page 8-11).

Main Memory

The main memory of the board is provided per default by one on-board SDRAM memory bank of up to 256 MByte. The capacity of the main memory can be increased up to 1 GByte by installing a lower memory module and an upper memory module onto the lower one.

Requirements

For detailed information on the requirements, qualified configurations, and maximum power consumption of the memory modules, see “Requirements” page 2-7.

Installation

For information on installing the memory modules refer to the respective *Memory Module Installation Guide*.

Accessibility

The main memory is accessible from:

- PowerPC CPU
- Other CompactPCI bus masters via the PCI-to-PCI bridge
- Ethernet DMA controllers
- Other PCI DMA controllers on PMC modules
- PCI-to-ISA bridge DMA controller

ECC

ECC is supported. The ECC detects and corrects all single-bit errors. Double-bit errors and errors within a nibble are only detected but not corrected. ECC is disabled per default and can be enabled by software.

Accesses

The following two different types of main memory accesses are possible:

- Main memory access without ECC:
  - In case of main memory read accesses the bytes requested by the master are read from the main memory without additional transfers for ECC. If less than one long-word is read, the extraneous data is ignored by the PPC-to-PCI bridge.
  - In case of main memory write accesses the bytes provided by the master are written into the main memory without additional transfers for ECC. If less than one long-word is written, the extraneous data is masked by control signals. Therefore, only targeted bytes are actually written.
- Main memory accesses with ECC:
  - A main memory read access to less than one long-word is performed by the PPC-to-PCI bridge as a read access to one aligned long-word, so that the ECC byte can be checked. The 8 bytes and the ECC byte are stored in the memory controller.
  - A main memory write access to less than one long-word is performed by the PPC-to-PCI bridge as a read-modify-write access to one aligned long-word. The PPC-to-PCI bridge reads the aligned long-word, checks the ECC byte and merges the written data with the data read from the main memory. Then the PPC-to-PCI bridge generates a new ECC for the merged long-word and writes the long-word and ECC code into the main memory.

Controller

The memory controller is located in the PPC-to-PCI bridge. The memory controller registers of the PPC-to-PCI bridge are accessible via the configuration address register (CAR) and the configuration data register (CDR). For configuring the memory controller the CAR and the CDR must be set appropriately (see “PPC-to-PCI Bridge” page 5-18).

Performance

The main memory control logic is optimized for fast accesses from the PowerPC CPU providing the maximum performance with enabled ECC. Since the PowerPC CPU includes a data and instruction cache, many CPU accesses are cache line “burst fills”. Within four 8-byte cycles these burst fills attempt to read 32 consecutive bytes into the PowerPC CPU. As an example, the main memory performance for a 100-MHz PPC bus is described below.

“4-1-1-1” Burst Transfer

The first read cycle of a burst consists of four PPC bus clock cycles delayed against the activated SDRAM chip select signal (using “registered DIMM” mode and CAS latency 3 memory devices). Owing to the optimized design of the memory control logic, each subsequent cycle requires only one PPC bus clock cycle to complete. This is commonly called a “4-1-1-1” burst transfer. Overall, the total cache line “burst fill” operation requires seven PPC bus clock cycles to transfer 32 bytes providing a maximum memory bandwidth of 457 MByte/s at 100-MHz PPC clock frequency.

Single Read and Write

A single read or write access (1, 2, 4, or 8 bytes) requires three PPC bus-clock cycles. Distributed asynchronous refresh is provided every ~15 µs and an access during a pending refresh cycle may be delayed by a maximum of eight additional clock cycles at 100-MHz PPC clock frequency.

Organization

The SDRAM is arranged in one, two, three, four, or five banks with nine 16M×8 or 32M×8 SDRAM devices in each bank. Each main memory bank is 64-bit wide. The capacity of the on-board main memory is encoded in the DCCR A (see Table 30 “DCCR A” page 8-11). The capacity of the main memory enhanced by memory modules is encoded in the DCCR B (see Table 31 “DCCR B” page 8-12).

Cache Coherency and Snooping

To maintain the cache coherency of the main memory, the PowerPC CPU has the capability of snooping. On a snooped external bus cycle the PowerPC CPU invalidates the cache line that is hit. Snoop hits invalidate the cache line in all cases (also for alternate master read / write cycles).

Access from PowerPC CPU

After initialization the firmware enables the complete main memory at start address 00000000_{16}. The memory address range, which is accessible via the PPC bus, can be programmed in the PPC-to-PCI bridge memory controller. Depending on the main memory capacity, the end address is set to the maximum available memory by the firmware.
For information on the contiguousness of the main memory space, see Table 22 “Memory Map Seen from CPU” page 8-3.

Table 12: *Default Main Memory Access from the PowerPC CPU*

Address Range	On-Board Memory Capacity [MByte]	Lower Memory Module Capacity [MByte]	Upper Memory Module Capacity [MByte]
00000000_{16} .. $07FFFFFF_{16}$	128	0	0
00000000_{16} .. $0FFFFFFF_{16}$	256	0	0
00000000_{16} .. $17FFFFFF_{16}$	128	256	0
00000000_{16} .. $1FFFFFFF_{16}$	256	256	0
00000000_{16} .. $37FFFFFF_{16}$	128	256	512
00000000_{16} .. $3FFFFFFF_{16}$	256	256	512

Access via CompactPCI Bus

Main memory access from the CompactPCI bus is routed by the PCI-to-PCI bridge via the local PCI bus and the PPC-to-PCI bridge. Via the PCI-to-PCI bridge the start access address and the size of the accessible main memory window can be programmed. Via the PPC-to-PCI bridge the start addresses is fixed at 00000000_{16}.

Programmable Access Address Range

The access address of the main memory for other CompactPCI bus masters is programmable via the PCI-to-PCI bridge. The start address of the main memory and its size are programmable in 4 KByte increments via the PCI-to-PCI bridge (see *SENTINEL Reference Guide*). Therefore, the address range used by the CompactPCI bus masters is not necessarily the same as the one used by the PowerPC CPU for local accesses.

PCI Bus Access Cycle

When the PCI-to-PCI bridge detects a CompactPCI bus access cycle to the programmed address range of the main memory window, it requests bus mastership of the local PCI bus via the PCI bus arbiter. After the arbiter has granted the PCI bus mastership to the PCI-to-PCI bridge, the PCI bus access cycle is executed and all data is latched from (read cycles) or stored to (write cycles) the main memory. Afterwards the cycle is terminated and the PCI-to-PCI bridge keeps the PCI bus mastership until another PCI bus master requests it.

Access from Ethernet Controllers

The Ethernet controller uses the PCI bus mastership to transfer commands, data and status information to and from the main memory via the local PCI bus and the PPC-to-PCI bridge.

Access from PMC Modules

The PMC modules may use the PCI bus mastership to transfer commands, data and status information to and from the main memory via the local PCI bus and the PPC-to-PCI bridge.

Access from PCI-to-ISA Bridge

The PCI-to-ISA bridge uses the PCI bus mastership to transfer commands, data and status information to and from the main memory via the local PCI bus and the PPC-to-PCI bridge.

Boot Flash

Since the flash memory area is located on the PPC bus, the reset vector table in the boot flash is visible to the CPU after power-on reset before any initialization by the software. A memory address range of 8 MByte is available for the complete boot flash memory, where the upper 1 MByte range is used, 512 KByte for each of the two boot flash devices.

Address Range

The boot flash memory area is 8-bit wide organized. The boot flash consists of two socketed devices with a capacity of 512 KByte each. The address range of the boot flash devices is $FFF00000_{16}$..$FFFFFFFF_{16}$. The CPU reset vector is located at $FFF00100_{16}$.

Caution

Do not use any other type of flash devices than assembled by default at new boards. Otherwise the devices and/or data could be damaged.

Devices

The board provides two user programmable boot flash devices 29F040:512K * 8 in the PLCC package in sockets at locations J77 and J78. The locations can be logically exchanged by switch SW1-1. The base address is $FFF00000_{16}$. The devices are programmable at VPP = 5V.

Programming the Boot Flash

Caution

Before erasing or programming the boot flash, ensure that you do not destroy the Force Computers PowerBoot boot image and make a copy of the boot flash 1 contents by using a programmer.

Writing to the boot flash is enabled only if the boot flash write protection switch SW1-2 is set to ON (default “OFF”, see page 2-5). When the write protection of the boot flash is disabled, programming is handled by PowerBoot packaged with the PPC/PowerCoreCPCI-680 (see *PowerBoot Instruction Set*, section “FERASE – Erasing Flash Memories” and section “FPROG – Programming Flash Memories”) and by the assembly process.

User Flash

There is a 8 MByte address space used for the user flash. If more than one 8 MByte user flash is installed, the user flash is visible only bank-wise, each bank consisting of 8 MByte. Since only 8 MByte are preserved for the user flash bank, one parallel port pin (see Table 32 “CIO Port A Data Register” page 8-12) provides bank switching techniques to increase the user flash capacity. This pin extends the PPC-to-PCI bridge addressing lines. The assembled type of flash devices used for the user flash can be detected via an additional parallel port pin (see Table 32 “CIO Port A Data Register” page 8-12).

Address Range

The flash memory area is 8-bit wide organized. The PPC-to-PCI bridge provides 23 addressing lines to address the user flash memory. Therefore, 8 MByte of user flash are accessible for 8-bit wide organized flash devices at the address range $FF000000_{16}$ .. $FF7FFFFF_{16}$.

Note: USER_FL_2MB and FLU_BANK are bits 3 and 2 respectively, of the CIO port A data register. For their description see Table 32 “CIO Port A Data Register” page 8-12.

The following table shows the address range of each of the user flash devices if 29F016 flash devices are used (8 MByte user flash maximum).

Table 13: *User Flash Address Map with 29F016 Flash Devices Assembled*

User Flash	USER_FL_2MB (read only)	FLU_BANK	Address Range
1	1_2	Don’t care	$FF000000_{16}$ .. $FF1FFFFF_{16}$
2	1_2	Don’t care	$FF200000_{16}$ .. $FF3FFFFF_{16}$
3	1_2	Don’t care	$FF400000_{16}$ .. $FF5FFFFF_{16}$
4	1_2	Don’t care	$FF600000_{16}$ .. $FF7FFFFF_{16}$

The following table shows the address range of each of the user flash devices provided that 29F032 flash devices are used (16 MByte user flash maximum).

Table 14: *User Flash Address Map with 29F032 Flash Devices Assembled*

User Flash	USER_FL_2MB (read only)	FLU_BANK	Address Range
1	0_2	0_2	$FF000000_{16}$ .. $FF3FFFFF_{16}$
2	0_2	0_2	$FF400000_{16}$ .. $FF7FFFFF_{16}$
3	0_2	1_2	$FF000000_{16}$ .. $FF3FFFFF_{16}$
4	0_2	1_2	$FF400000_{16}$ .. $FF7FFFFF_{16}$

Note: The firmware supports commands to select the device bank to be mapped into the address range (see *PowerBoot Instruction Set*, section "FSELECT – Selecting Flash Memory").

Size

The on-board user flash is accessible according to Table "" page 5-13 or Table 14 "User Flash Address Map with 29F032 Flash Devices Assembled" page 5-14, depending on the device type assembled. The following user flash capacities are available:

- 8 MByte if four 2M * 8 devices (29F016) or two 4M * 8 devices (29F032) are used
- 16 MByte if four 4M * 8 devices (29F032) are used

Devices

The user flash consists of up to four user programmable devices. The base address of the user flash range is $FF000000_{16}$. The available boot flash devices are programmable at VPP = 5V.
The following table shows the factory options available for the user flash using the device types listed (or equivalent).

Table 15: *User Flash Device Types (Factory Options)*

Device Type	Number	Capacity	USER_FL_2MB
29F016:2M * 8	4	8 MB	1_2 (no bank select possible)
29F032:2M * 8	2	8 MB	0_2 (bank select not allowed)
29F032:2M * 8	4	16 MB	0_2 (bank select necessary)

Programming the User Flash

Writing to the user flash is enabled only if SW1-3 is set to OFF (default "OFF", see page 2-5). When the write protection of the user flash is disabled, programming is handled by PowerBoot packaged with the PPC/PowerCoreCPCI-680 (see *PowerBoot Instruction Set*, section "FERASE – Erasing Flash Memories" and section "FPROG – Programming Flash Memories") and by the assembly process.

Watchdog Timers

The PPC/PowerCoreCPCI-680 provides two independent watchdog timers monitoring the CPU activity. If no triggering occurs during the selected time-out periods:

- Watchdog timer #1 generates a reset pulse.
- Watchdog timer #2 generates an NMI or a high-level interrupt (depending on the setting of SW4-4) to the PowerPC CPU.

Enabling

Watchdog timer #1 is enabled by setting SW4-1 to ON (default “OFF”, see page 2-6).
Watchdog timer #2 is enabled by setting SW4-2 to ON (default “OFF”, see page 2-6).

Starting

If SW4-1 and SW4-2 are set appropriately, both watchdog timers will be started via ENA_WD in the CIO port A data register (see Table 32 “CIO Port A Data Register” page 8-12). Once started, the watchdog timers can be stopped only by a reset. After a reset none of the watchdog timers is started.

Triggering

A watchdog timer is triggered when the respective sanity check of this timer is performed. A sanity check includes two write cycles to the appropriate sanity check address with defined data. After the sanity check has been performed, the time-out period for the watchdog timer will be reset.
To trigger the watchdog timer #1, take the following two steps:

1. Write $\mathbf{55_{16}}$ to the ISA I/O address 312_{16}.
2. Write $\mathbf{AA_{16}}$ to the ISA I/O address 312_{16}.

To trigger the watchdog timer #2, take the following two steps:

1. Write $\mathbf{55_{16}}$ to the ISA I/O address 316_{16}.
2. Write $\mathbf{AA_{16}}$ to the ISA I/O address 316_{16}.

Caution

Although the watchdog timers are started synchronously, they may be retriggered independently, hence asynchronously. Consequently, it is possible to get a reset pulse from the watchdog timer #1 without getting an interrupt from the watchdog timer #2 (if both watchdog timers are enabled). In order to avoid this, the sanity checks for both timers should be performed simultaneously.

Timeout

The watchdog time-out period can be selected via SW4-3 (see Table 4 “Switch Settings” page 2-5).

Interrupt

If triggering of the watchdog timer #2 does not occur within the selected watchdog time-out period, the watchdog timer #2 asserts an interrupt to the PCI-to-ISA bridge:

- If SW4-4 is set to ON, an IOCHCK interrupt, which is an NMI, is asserted and routed to the MCP# interrupt pin of the PowerPC CPU.
- If SW4-4 is set to OFF, an IRQ<8># interrupt is asserted which is routed to the main interrupt input of the PowerPC CPU.

Reset

If triggering of the watchdog timer #1 does not occur within the selected watchdog time-out period, the watchdog timer #1 initiates a reset of the board.

Register

The PPC/PowerCoreCPCI-680 provides a BSCR watchdog status register indicating the current watchdog parameters (see Table 37 “BSCR Watchdog Control and Status Register” page 8-16). The register bits [3…0] reflect the settings of switches SW4-4, SW4-3, SW4-2, and SW4-1.

PPC-to-PCI Bridge

The PPC-to-PCI bridge provides an integrated and PowerPC compliant interface between the PowerPC CPU, the main memory, the user and boot flash, and the PCI bus.

Processor Interface

The processor interface provides a 64-bit data bus and a 32-bit address bus. It supports full memory coherency. Furthermore, it pipelines processor accesses.

Memory Interface

Depending on the memory modules installed on the board, the memory interface is programmed to support the main memory. The memory interface provides a 64-bit data bus to the main memory. ECC is per default disabled by software (see “Main Memory” page 5-7). The PPC-to-PCI bridge supports up to 1 GByte main memory. The memory interface supports writing of flash memory and write buffering for PCI and processor accesses.

PCI Interface

The PCI interface implements the following features:

- Operation at 33 MHz
- PCI-interlocked accesses to main memory via lock pin and lock protocol
- Accesses to all PCI address spaces
- Selectable big or little endian operation
- Store gathering of PPC-to-PCI writes and PCI-to-memory writes and memory prefetching of PCI read accesses
- PCI configuration registers
- Data buffering (in / out)
- Parity support
- Error reporting mechanism
- Concurrent transactions on the processor and the PCI bus

Registers

The register set of the PPC-to-PCI bridge is accessible via the configuration address register (CAR) and the configuration data register (CDR). To configure the memory controller, the CAR and the CDR must be set appropriately:

- To access the register set of the PPC-to-PCI bridge with offset xy, the CAR must contain $xy000080_{16}$ (see Table 25 “Configuration Base Addresses” page 8-6). The register offset xy has to be written into the most significant byte of the CAR. The lowest significant byte must be set to 80_{16} (swapped byte).
- The CDR contains the contents of the memory controller registers (R/W) which are to be accessed.

Table 16: *CAR and CDR Address Map*

Register	Address
CAR	$FEC00000_{16}$
CDR	$FEE00000_{16}$

Example

To enable memory bank 1and 2, you have to access the memory bank enable register at offset $A0_{16}$ and write the value 03_{16} into this register:

1. Write the value **$A0000080_{16}$** to the CAR address $FEC00000_{16}$.
2. Write the value **03_{16}** to the CDR address $FEE00000_{16}$.

PCI-to-PCI Bridge

The PPC / PowerCoreCPCI-680 uses the Force Computers SENTINEL universal PCI-to-PCI bridge. The SENTINEL can operate either in transparent or in non-transparent (embedded) mode. If the board is located in the system slot, the bridge operates in transparent mode, in any other CompactPCI slot the bridge operates in non-transparent mode. The automatic switching of the modes is done by evaluating the CompactPCI SYSEN# signal.

Features

The PCI-to-PCI bridge provides:

- 32-bit with 33-MHz PCI bus interface on the CompactPCI bus and the local PCI bus
- 5V or 3.3V signaling level, independent of the primary and secondary side
- Integral buffers for write posting and read buffering to maximize bandwidth utilization
- In transparent mode:
  - Standard type 1 PCI configuration space
  - Set of device specific registers (DSRs)
- In non-transparent mode:
  - Standard type 0 PCI configuration spaces, one set for the CompactPCI bus, one set for the local PCI bus. The register set from the secondary side is shadowed to the primary side and vice versa.
  - Set of device specific registers (DSRs)
- Four programmable interface base address configuration registers for downstream forwarding from CompactPCI bus to local PCI bus and three programmable interface base address configuration registers for upstream forwarding from local PCI bus to CompactPCI bus.

DSR Base Address

For the local PCI interface the DSR base address is set by the user. The default CSR base address set by PowerBoot is $FE890000_{16}$ seen from the CPU.

Hot-Swap Support

The SENTINEL supports hot swap according to the *CompactPCI Hot Swap Specification PICMG 2.1 R1.0*. The basic purpose of the hot swap support is to allow the orderly insertion and extraction of boards without adversely affecting system operation. Hot swap provides programmatic access to hot-swap services allowing system reconfiguration and fault recovery to take place with no system downtime and minimum operator interaction.
There are three hot-swap system types:

- Basic hot-swap systems
- Full hot-swap systems
- High-availability systems

As a hot-swap-friendly silicon, the SENTINEL has the required features to build systems of all three categories.

Hot Swap Control/Status Register

The SENTINEL provides a hot swap control / status register for software connection control and control of the ENUM# signal and the illumination of the blue hot-swap LED (see *SENTINEL Reference Guide*).

Note: The hot-swap control and status register is accessible in the PCI configuration space from both sides of the PCI-to-PCI bridge (CompactPCI and local PCI). The bridge is accessible from the local PCI bus number 00_{16}, device number 18_{16}, function number 00_{16}. The register offset is FE_{16}. The register location from the CompactPCI bus is system dependent and therefore beyond the scope of this manual.

BD_SEL# and HEALTHY#

The SENTINEL is held in power-on reset state while either the CompactPCI signal BD_SEL# or HEALTHY# is driven inactive. This power-on reset effects the whole chip. Additionally, it is ensured that the chip is tri-stated while the board is extracted.

ENUM# in Non-Transparent Mode

When working in non-transparent mode on a peripheral board, the CompactPCI signal ENUM# is an output that can be activated by the SENTINEL. This signal is used in a full hot-swap or high-availability environment to inform the system controller or a hot-swap-controller (HSC) that a hot-swap process takes place and that the system configuration is to be changed.

ENUM# in Transparent Mode

When working in transparent mode on the system controller, the CompactPCI signal ENUM# is an input to the SENTINEL. The SENTINEL device activates its local PCI interrupt output INTA# when ENUM# is activated by any peripheral board.

CompactPCI Bus Interface

The PPC/PowerCoreCPCI-680 provides a complete CompactPCI bus interface compliant with the *CompactPCI Specification PICMG 2.0 R2.1*.

BARs

The PCI-to-PCI bridge includes four base address registers (BARs) to perform downstream transfers from the CompactPCI bus to the local PCI bus:

- BAR 0: used for mapping downstream memory space and the lower 4 KByte of the CompactPCI DSR space
- BAR 1: used for mapping DSRs in I/O space
- BAR 2: used for mapping downstream I/O or memory space
- BAR 3: used for mapping downstream memory space
- BAR4: used for mapping downstream memory space

The size of the BARs can be programmed and may also be disabled. Only BAR 0 is enabled per default, since the DSRs for the CompactPCI bus are always mapped into this area.

Supported Transfers

The CompactPCI bus interface responds to the following transfers:

- All memory commands
- I/O read and write commands
- Type 0 configuration commands (in non-transparent mode)

The CompactPCI bus interface is able to initiate the following transfers:

- All memory commands
- I/O read and write commands
- Type 0 and type 1 configuration commands (in transparent mode only)

Local PCI Bus Interface

The PPC/PowerCoreCPCI-680 provides a complete local PCI bus interface compliant with the *PCI Local Bus Specification Rev. 2.1*.

BARs

In transparent mode the PCI-to-PCI bridge includes three BARs to perform upstream transfers from the local PCI bus to the CompactPCI bus. Two of them are used for mapping upstream memory space. The third BAR may be programmed for I/O or memory space mapping:

- BAR 0: used for mapping DSRs in memory space
- BAR 1: used for mapping DSRs in I/O space
- BAR 2: used for mapping upstream I/O or memory space
- BAR 3: used for mapping upstream memory space

The size of the BARs can be programmed and may also be disabled.

Supported Transfers

The local PCI bus interface responds to the following transfers:

- All memory commands
- I/O read and write commands
- Type 0 configuration commands

The local PCI bus interface is able to initiate the following transfers:

- All memory commands
- I/O read and write commands

Exception Signals

The *PCI Local Bus Specification Rev. 2.1* describes the signals INTA#, INTB#, INTC#, and INTD# for signaling exceptions or status. The usage of the interrupt signals depends on the operating (transparent or non-transparent) mode of the SENTINEL.

Transparent Mode

When operating in the transparent mode, all four CompactPCI interrupt signals are routed through the SENTINEL to the local PCI interrupt signals. Additionally, the bridge may drive INTA# for its own interrupt.

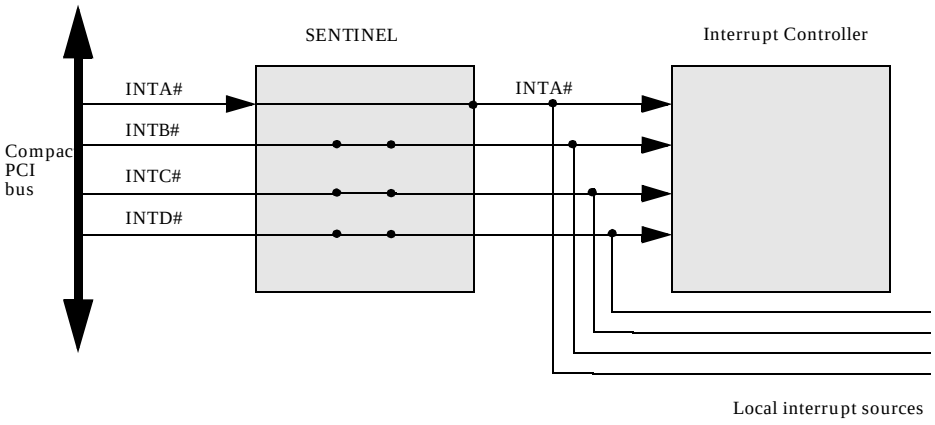


Figure 9: *Interrupt Routing in Transparent Mode*

Non-Transparent Mode

When operating in the non-transparent mode, only the signal INTA# is used to generate a CompactPCI interrupt. The connection of the CompactPCI and local sides of INTB#, INTC#, and INTD# is disabled. Additionally, the SENTINEL may use the local interrupt signal INTA# for its own interrupt.

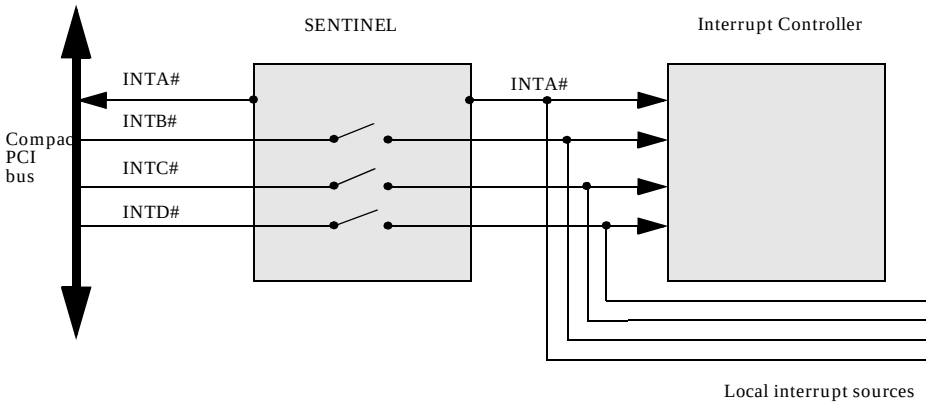


Figure 10: *Interrupt Routing in Non-Transparent Mode*

The SENTINEL generates a CompactPCI or a local PCI interrupt itself under the following conditions.
A CompactPCI interrupt is going to be asserted when one of the following conditions is true:

- The I_2O outbound post list is not empty.
- The I_2O outbound post list falls below half full.
- The I_2O outbound post list falls below quarter full.
- An upstream UCW Write occurs.
- An upstream Local Mailbox Write occurs.

These conditions are individually maskable.

A local PCI interrupt is asserted when one of the following conditions is true:

- The I_2O inbound post list is not empty.
- The I_2O inbound free list falls below half full.
- The I_2O inbound free list falls below quarter full.
- A downstream UCW Write occurs.
- A downstream Local Mailbox Write occurs.
- The CompactPCI ENUM# signal is asserted (transparent mode only).

These conditions are individually maskable.

Ethernet Interface

The PPC/PowerCoreCPCI-680 offers one Local Area Network (LAN) interface (Ethernet #1) at the front panel and one (Ethernet #2) via the rear transition board. This LAN interfaces include:

- 82559ER Ethernet LAN controller with integrated interface adapter (PHY)
- Filter transformer routing two differential receive and two differential transmit lines of the 10Base-T or 100Base-TX interface to the front panel Ethernet interface connector
- (Optional) rear transition board with a filter transformer routing two differential receive and two differential transmit lines of the 10Base-T or 100Base-TX interface to the back panel Ethernet interface connector

Ethernet Address

The unique Ethernet address of each Ethernet interface is permanently stored at the appropriate ID-ROM. After power-on the Ethernet addresses are copied into the NVRAM at offset $1C12_{16}$ (Ethernet #1) and $1C18_{16}$ (Ethernet #2) where they can be read by the software.

Features

The Ethernet interfaces provides the following features:

- Compatibility with IEEE 802.3/Ethernet
- Data rate of 100 Mbit/s
- DMA capability
- Interrupt generation

Ethernet Controller with integrated PHY

The fast Ethernet LAN controller with integrated PHY provides the following features:

- Integration features:
  Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY
- Performance features:
  - Chained memory structure similar to the i82559
  - Improved dynamic transmit chaining with multiple priorities transmit queues
  - Full Duplex support at both 10 and 100 Mbit/s
  - 3 KByte transmit and 3 KByte receive FIFOs
  - Fast back-to-back transmission support with minimum inter-frame spacing
  - IEEE 802.3x 100BASE-TX Flow Control support
  - Direct main memory access (DMA) with programmable burst size provided for low CPU utilization
  - Unlimited PCI burst support
  - Support of early interrupt on receiving
  - Support of address filtering modes
- Device features:
  - Loopback capability
  - LED support for network activity indications
  - Low-power features with efficient dynamic stand-by mode
  - Low-power, 3.3V device
- Automatic detection and sensing feature:
  IEEE 802.3u auto-negotiation support

CSR Base Address

For the local PCI interface the CSR base address is set by the user. The default CSR base address set by PowerBoot is $FE870000_{16}$ (Ethernet #1) and $FE880000_{16}$ (Ethernet #2) seen from the CPU.

Interrupt

The Ethernet #1 and #2 controllers use the signals INTB# and INTA# respectively, for interrupting the CPU (see Table 28 “Interrupt Map” page 8-8).

PCI-to-ISA Bridge

The PCI-to-ISA bridge provides:

- PCI master / slave interface with 33 MHz
- ISA master / slave interface with 8.25 MHz
- Timer / counter with three channels (functionality of one 82C54 timer)
- Two interrupt controllers supporting 15 interrupt channels (functionality of two 82C59A interrupt controllers). The interrupt controllers can be programmed independent of edge or level sensitivity.
- Two DMA controllers (functionality of two 82C37A DMA controllers) and seven independently programmable channels
- Control logic generating NMIs
- Multi-functionality:
  - PCI-to-ISA bridge is function 0.
  - IDE controller (used for the optional CompactFlash slot) is function 1.

Both functions can be configured independently. The IDE interface is disabled per default.

PCI-to-ISA Function

The PCI-to-ISA-bridge prevents the slower I / O devices from slowing down the PCI bus. The following devices / registers are located on the ISA bus:

- Two serial interfaces
- NVRAM and RTC
- CIO for internal control
- DCCRs
- BSCRs
- PN15 connector (factory option) for ISA extension

The ISA base address of the PCI-to-ISA bridge is $FE000000_{16}$.

Interrupt Controller

The following figure shows the default interrupt structure of the CPU board. The interrupt controller of the PCI-to-ISA bridge is used for interrupt routing. The PCI-to-ISA bridge collects the possible interrupts and passes them to the PPC-to-PCI bridge via the INTR line. An NMI is generated only if:

- PCI system error (PCI signal SERR# active) occurs
- Watchdog timeout occurs
- Abort key is pressed

All interrupts can be disabled independently

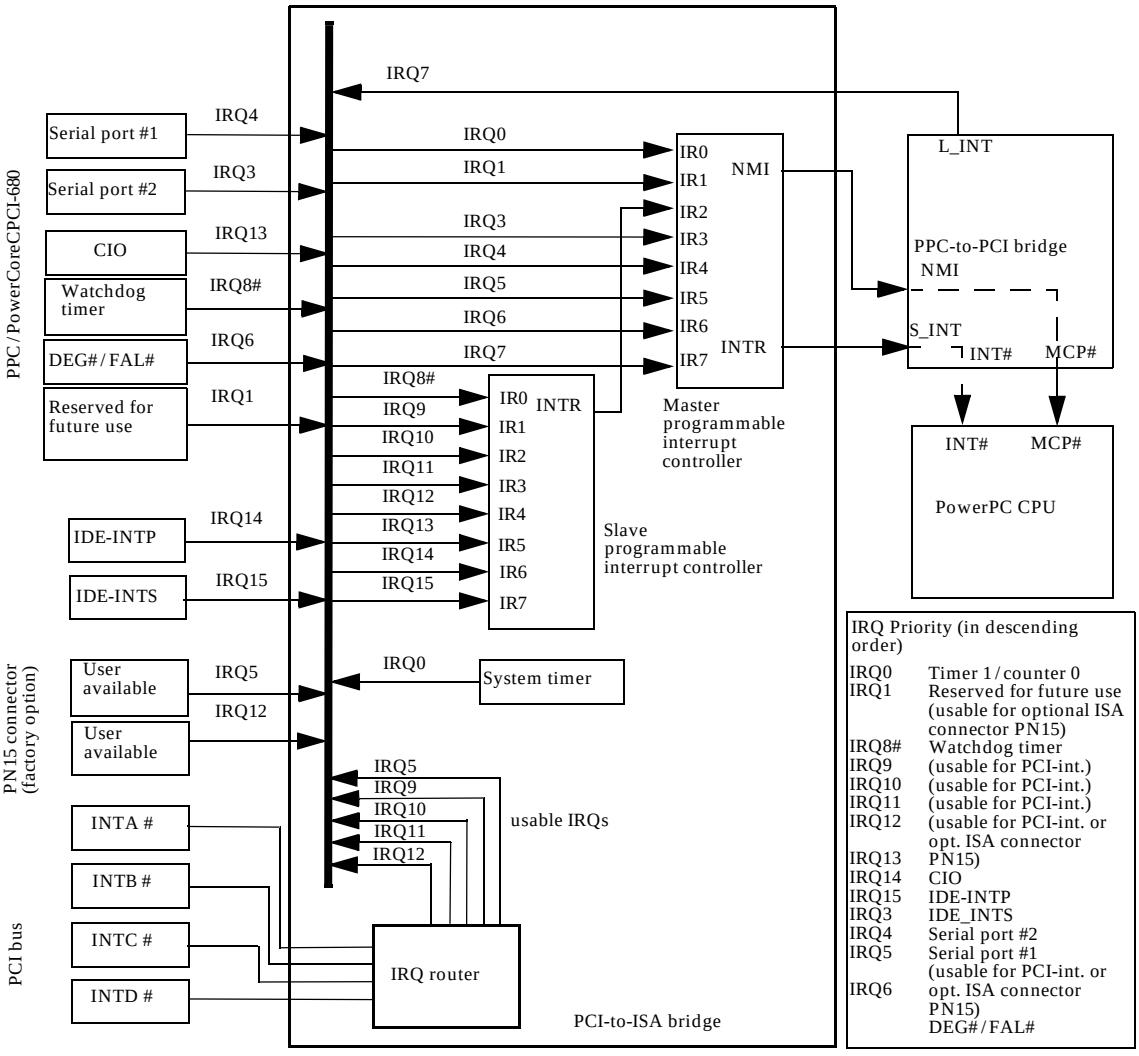


Figure 11: *Default PCI-to-ISA Interrupt Structure*

Real-Time Clock/Non-Volatile RAM

The real-time clock (RTC) and the non-volatile RAM (NVRAM) are housed in one device including a battery backup. The battery is mounted on top of the device with a direct connection to its power supply. For information on exchanging the battery see “Battery Change” page 2-16.
If power fails, the device is automatically deselected and changes into write-protected mode.
The RTC / NVRAM address space is divided into three used parts as shown in table below.

Table 17: *Address Ranges of the RTC/NVRAM*

Address Range	Access
0000_{16} .. $1BFF_{16}$	NVRAM user defined area
$1C00_{16}$ .. $1FF0_{16}$	NVRAM configuration area used by PowerBoot
$1FF1_{16}$ .. $1FF7_{16}$	Unused
$1FF8_{16}$ .. $1FFF_{16}$	RTC registers

Address Access

The access to the RTC / NVRAM is 8-bit wide and indirect. To access a location within the device:

1. Write the lower address byte to $FE000073_{16}$ (write-only).
2. Write the higher address byte to $FE000075_{16}$ (write-only).
3. Read or write data byte sized from or to $FE000077_{16}$.

NVRAM

Since the last 16 bytes are used for the RTC or unused, the NVRAM has a capacity of 8 KByte – 16 bytes. The complete address space of the NVRAM is 0000_{16} .. $1FF0_{16}$. The user may store important data in the user defined area of the NVRAM. The NVRAM configuration area is used for internal configuration data.

Note: Do not change the values stored in the configuration area.

RTC

The on-board RTC maintains accurate time and date based on its own quartz.

PPC/PowerCoreCPCI-680 Parameters, Timers and CIO

The configuration and status information for several PPC/PowerCoreCPCI-680 parameters and timers are accessible via two 8-bit registers, the CIO data and timer registers and the NVRAM configuration area. They are all located on the ISA bus.

Parameters

Some of the following parameters can only be read, others can be read and written:

- Cache
  DCCR A, bits [7..6] and CIO port A data register, bit [4] (read-only)
  For DCCR A and CIO port A register description, see Table 30 “DCCR A” page 8-11 and Table 32 “CIO Port A Data Register” page 8-12 respectively.
- Main memory
  DCCR A, bits [3..0] for on-board RAM and DCCR B, bits [1...0] for memory modules (read-only)
  For DCCR A and DCCR B register description, see Table 30 “DCCR A” page 8-11 and Table 31 “DCCR B” page 8-12 respectively.
- Boot flash
  DCCR A, bit [4] (read-only)
  For DCCR A register description, see Table 30 “DCCR A” page 8-11.
- User flash
  CIO port A data register, bit [3] (read-only) and bit [2] (read/write)
  For CIO port A data register description, see Table 32 “CIO Port A Data Register” page 8-12.
- PPC bus and memory frequency
  DCCR B, bits [7..6] (read-only)
  For DCCR B register description, see Table 31 “DCCR B” page 8-12.

- Boot parameters
  Stored in the NVRAM (see “Real-Time Clock / Non-Volatile RAM” page 5-30)
- ID-ROM
  Various board parameters are stored in the ID-ROM for internal use.
- PMC busmode
  The PMC busmode signals can be set and read via CIO port B (see Table 33 “CIO Port B Data Register” page 8-14).

Timers

The PPC / PowerCoreCPCI-680 provides the following timers:

- One 64-bit timer in the PowerPC CPU (resolution 4 PPC bus clock periods, i.e. 40 ns at 100 MHz PPC bus frequency)
- Four 32-bit timers integrated in the PPC-to-PCI bridge (resolution 8 PPC bus clock periods, i.e. 80 ns at 100 MHz PPC bus frequency)
- Functionality of one 82C54 timer integrated in the PCI-to-ISA bridge (three timers, 16 bit, resolution 838 ns)
- Three independently programmable 16-bit timers provided by the CIO which can also be used as counters (resolution 485 ns)

The peripheral clock of the CIO device is connected to a 4.125 MHz source.

CIO

The PPC / PowerCoreCPCI-680 integrates one CIO device which controls board internal signals and devices. The CIO includes three independently programmable ports A, B, and C.
The CIO contains:

- Two independent 8-bit ports (ports A and B)
- One special-purpose 4-bit port (port C)
- Three independently programmable 16-bit timers which can also be used as counters

The base address is $FE000300_{16}$ seen from the CPU. The interrupt request output of the CIO uses IRQ13. For CIO data register description see Table 32 “CIO Port A Data Register” page 8-12, Table 33 “CIO Port B Data Register” page 8-14, and Table 34 “CIO Port C Data Register” page 8-15.

Board Status and Capability Registers

The PPC/PowerCoreCPCI-680 provides several board status and capability registers (BSCRs). The BSCRs indicate the current status of the board and include features for generating software requested reset conditions. All BSCRs are located on the ISA bus and are accessible in the address range $FE000312_{16}$..$FE000340_{16}$. Unused addresses within this address range are reserved.

For the BSCR description see Table 37 “BSCR Watchdog Control and Status Register” page 8-16, Table 35 “BSCR Watchdog Timer 1 Sanity Check Register” page 8-15, Table 36 “BSCR Watchdog Timer 2 Sanity Check Register” page 8-16, Table 38 “BSCR Last Reset Register” page 8-17, and Table 39 “BSCR Reset Request Register” page 8-19.

Serial I/O Ports – SCCs

The PPC/PowerCoreCPCI-680 provides two serial I/O ports implemented by the serial communication controllers (SCCs).
The SCCs:

- Run with all existing 16C450 software
- Provide programmable baudrate generator
- Provide standard asynchronous communication bits
- Have fully programmable serial interface characteristics

The peripheral clock input of the SCCs is driven by an 1.8432-MHz clock. The interrupt requests of the SCCs are connected to the IRQ4 and IRQ3 input of the PCI-to-ISA-bridge.

Table 18: *SCC Base Addresses*

Serial I/O Port #	SCC Base Address
1	$FE0003F8_{16}$
2	$FE0002F8_{16}$

The RS-232 serial I/O ports are available at the front panel or via the rear transition board. For information on the connector pinout see “Serial I/O Ports” page 3-5.

PMC Slots

The PPC/PowerCoreCPCI-680 provides two PMC slots. For information on the power requirements and installation of the PMC modules see “Power Requirements” page 2-8 and “PMC Modules” page 2-10 respectively.
Via the signals BUSMODE[4..2] and BUSMODE[1..0] the host gets information on the presence of PMC modules (= card) and logical protocol of the PMC modules.
Via the BUSMODE[4..2] signals driven by the host the PMC modules get the information whether a host is present. The answer of the PMC modules is transferred by the signal lines BUSMODE[1..0].

Note: The BUSMODE[4..2] signals must be set accordingly. If the CIO port B data register is not initialized, the PMC modules do not detect the host and do not work. Per default, the firmware initializes the signals BUSMODE[4..2].

For CIO port B data register description, see Table 33 “CIO Port B Data Register” page 8-14.

ISA Devices

The connector PN15 available as a factory option may be used to install ISA devices. For CIO port B data register description, see Table 33 “CIO Port B Data Register” page 8-14.

CompactFlash Slot

As a factory option, a CompactFlash slot can be assembled. If the CompactFlash slot is assembled, only the PMC slot #1 is available. The CompactFlash slot is integrated in the front panel to allow insertion and / or removal of a CompactFlash card without removing the board out of the system.

CompactFlash cards of type I or type II can be plugged into the CompactFlash slot. The CompactFlash cards are accessed in the True-IDE mode via the primary IDE port integrated in the PCI-to-ISA bridge. The (read-only) bit 5 of the CIO Port A data register (see Table 32 “CIO Port A Data Register” page 8-12) can be used by software to determine whether a CompactFlash card is fully inserted in the CompactFlash slot.

Note: Inserting the CompactFlash card while the board’s power is on will configure the CompactFlash card to PC Card ATA mode, which is not supported by the PowerCore CPCI-680 board. In order to configure the CompactFlash card to the supported True-IDE mode the card must already be inserted when the board‘s power is turned on.

6

PowerBoot (= PowerBoot Instruction Set)

Please Note…

The *PowerBoot Instruction Set* is an integral part of the *PPC/PowerCoreCPCI-680 Reference Guide* (P / N 214452), which is packaged separately.
The *PowerBoot Instruction Set* will always be shipped together with the *Reference Guide*.
Please:

☞ **Insert the *PowerBoot Instruction Set* (P/N 204525) now into the *PPC/PowerCoreCPCI-680 Reference Guide* (P/N 214452).**

☞ **Remove this sheet.**

7

PowerBoot for PPC/PowerCoreCPCI-680

This chapter describes the board-specific PowerBoot commands. PowerBoot includes the following board-specific commands:

- Manually map the PCI bus devices at the PMC slot #1 or #2:
  “PMCPCI – Mapping PMC Modules” page 7-7
- Restart the CPU board:
  “RESET – Restarting the Board” page 7-10
- Set and display auto boot after power-on:
  “SETBOOT – Editing Auto Boot Parameters” page 7-12
- Turn the user LED at the front panel ON or OFF:
  “USERLED – Setting User LED” page 7-26
- Access the PCI bus:
  “Accessing the PCI Bus” page 7-27
- Programming the onboard boot and user FLASH memory devices:
  “Flash Memory” page 7-32

Supports and Requirements

PowerBoot supports up to 9 MByte on-board flash memory:

- 2 × 512 KByte boot flash for PowerBoot or other boot software for booting operating systems
- 8 MByte user flash which can be accessed in a memory-mapped flat array of 4 × 2 MByte flash memory devices
- 16 MByte user flash which can be accessed in a banked array of 2× 2×4 MByte flash memory devices

The boot flash memory must be located at the CPU address $FFF00000_{16}$, because the PPC/PowerCoreCPCI-680 CPU vectors to the address $FFF00100_{16}$ after releasing an active /RESET. Additionally, this boot flash memory has to be visible to the CPU at all times (no bank switching). For more information on programming images into user flash memory devices, see “Flash Memory” page 7-32.

PPC/PowerCoreCPCI-680 Address Map

The following table lists the default addresses of the PPC/PowerCoreCPCI-680 board mapped by PowerBoot.

Table 19: *PPC/PowerCoreCPCI-680 Address Map Seen from the CPU*

Address	Device
00000000_{16} .. $3FFFFFFF_{16}$	SDRAM: On-board memory + memory modules
40000000_{16} .. $7FFFFFFF_{16}$	PowerPC-to-PCI bridge internal use
80000000_{16} .. $FDFFFFFF_{16}$	PCI memory
$FE000000_{16}$	PCI-to-ISA bridge: Base address of ISA registers
$FE000073_{16}$	ISA RTC/NVRAM: Low-address byte port
$FE000075_{16}$	ISA RTC/NVRAM: High-address byte port
$FE000077_{16}$	ISA RTC/NVRAM: Data byte port
$FE000170_{16}$ .. $FE000177_{16}$	ATA/IDE Registers ATA/IDE Command Block Registers Secondary drive 0/1
$FE0001F0_{16}$ .. $FE0001F7_{16}$	ATA/IDE Registers ATA/IDE Command Block Registers Primary drive 0/1
$FE0002F8_{16}$ .. $FE0002FF_{16}$	Serial console 2: I/O port
$FE000300_{16}$ .. $FE000303_{16}$	CIO parallel port: addresses
$FE000308_{16}$	DCCR A
$FE000310_{16}$	Chip select signal (PN15 connector)
$FE000348_{16}$	DCCR B
$FE000370_{16}$ .. $FE000377_{16}$	ATA/IDE Registers: ATA/IDE Control Block Registers Secondary drive 0/1
$FE0003F0_{16}$ .. $FE0003F7_{16}$	ATA/IDE Registers: ATA/IDE Control Block Registers Primary drive 0/1

Table 19: *PPC/PowerCoreCPCI-680 Address Map Seen from the CPU (cont.)*

Address	Device
$FE0003F8_{16}$ .. $FE0003FF_{16}$	Serial console 1: I / O port
$FE870000_{16}$	Ethernet controller 1: Base address of CSR registers
$FE880000_{16}$	Ethernet controller 2: Base address of CSR registers
$FE890000_{16}$	PCI-to-PCI bridge / device: Base address of DSR registers (transparent and non-transparent mode)
$FEC00000_{16}$	PCI bus: Configuration address register (CAR)
$FEE00000_{16}$	PCI bus: Configuration data register (CDR)
$FEF00000_{16}$	Interrupt acknowledge cycle
$FF000000_{16}$ .. $FF7FFFFF_{16}$	User flash: User flash devices 1, 2, 3, 4
$FFF00000_{16}$ .. $FFF7FFFF_{16}$	Boot flash 1 (default: 512 KByte):
$FFF80000_{16}$ .. $FFFFFFFF_{16}$	Boot flash 2 (default: 512 KByte):

PMCPCI – Mapping PMC Modules

PMCPCI manually maps a user mounted PMC module to any location in the PCI addressing space by defining its PCI I/O space address and/or its PCI memory space address. The PCI addressing space is divided into two areas as shown in the table below.

Table 20: *PCI Addressing Spaces*

PCI Addressing Space	Address	PCI Addressing Space Seen from:
PCI I/O space	$FE800000_{16}$ .. $FEBFFFFF_{16}$	CPU
	00800000_{16} .. $00BFFFFF_{16}$	PCI bus master
PCI memory space	80000000_{16} .. $FCFFFFFF_{16}$	CPU or PCI bus master

On the PPC/PowerCoreCPCI-680 the CSR registers for the local Ethernet devices and the PCI-to-PCI bridge are already mapped to the PCI I/O space (see Table 19 “PPC/PowerCoreCPCI-680 Address Map Seen from the CPU” page 7-5).

Syntax

PMCPCI *PmcModule PciIOSpaceAddr PciMemSpaceAddr*

PmcModule
defines the PMC module to be mapped:

- 1 = PMC module #1
- 2 = PMC module #2

PciIOSpaceAddr

defines the PCI I/O space address as seen from the PCI bus.

PciMemSpaceAddr
defines the PCI memory space address as seen from the PCI bus.

Description

PMCPCI checks the capabilities of every device as follows:

- PCI bus device registers at offset 10_{16}, 14_{16}, 18_{16}, $1C_{16}$, 20_{16}, 24_{16} are searched to set a base address for devices command / control registers (CSR).
- If a PCI bus device mounted on a PMC module does not support PCI memory and PCI I / O addressing spaces at a time, only the supported one will be used even if both addressing spaces have been user defined.
- If a PCI bus device mounted on a PMC module supports a addressing spaces (e.g. PCI memory space) in more than one register, the first one in descending sequence will be used.
- If a PCI bus device mounted on a PMC module is able to support both addressing spaces, but only one should be used, set the address not to be used to $FFFFFFFF_{16}$.
- If no PCI bus device is installed, one of the following messages will appear:

```
PMC 1/2 modules:
Error: Can’t set base-address of PMC1

PMC 1/2 modules:
Error: Can’t set base-address of PMC2
```

Example

In the following example a PMC module at PMC slot #1 is mapped to the PCI I/O space 00810000_{16} and to the PCI memory space 80000000_{16}. A user application can access the PCI bus device CSR registers via the PowerPC CPU at the PCI I/O space address $FE810000_{16}$ and at the PCI memory space address 80000000_{16}.

```
PowerBoot>
PowerBoot>
PowerBoot> PMCPCI 1 00810000 80000000

PMC1/2 modules:
PMC1, PCI address 0x00810000, Base Reg. 0x10, PCI I/O space, Master enable
PMC1, PCI address 0x80000000, Base Reg. 0x10, PCI MEM space, Master enable
Device ID = 0x0009; Vendor ID = 0x1011;
Status    = 0x0280; Command   = 0x0007;
Base Class= 0x02;   Sub Class = 0x00;   Prg. Inter= 0x00;   Rev. ID   = 0x20;
BIST      = 0x00;   Header Typ= 0x00;   Latency Ti= 0x00;   Cache Line= 0x08;
base addr0= 0x00810001, base addr1= 0x80000000;
base addr2= 0x00000000, base addr3= 0x00000000;
base addr4= 0x00000000, base addr5= 0x00000000;
Max Lat   = 0x28;   Min Gnt   = 0x14;   IRQ Pin   = 0x01;   IRQ Line  = 0xFF;
Found PCI device: DEC Chip 21140A Fast Ethernet LAN


PowerBoot>_
```

RESET – Restarting the Board

The restarting of the CPU board via RESET is not as strong as a power-on reset. RESET incites only a jump to the /HRESET exception vector at $FFF00100_{16}$.

Syntax

RESET

Description

All devices based on the PCI bus will keep their PCI configuration space header region, e.g. the Ethernet controller will keep its default base address. But the main memory, the PCI-to-ISA bridge, the serial console, the CIO parallel port, the Ethernet controller, etc. will be initialized. The L1 and L2 caches will be flushed and invalidated.

Example

```
PowerBoot> RESET
Init serial 1 at address: 0xFE0003F8
Init serial 2 at address: 0xFE0002F8
Init CIO at address: 0xFE000300
Init Ethernet Controller 1 at address: 0xFE870000
Init Ethernet Controller 2 at address: 0xFE880000
PMC1/2: no auto mapping setup
Found PCI-to-PCI bridge/device SENTINEL - Host mode
Init PCI-to-PCI Host bridge at address: 0xFE890000
Probelist for CompactPCI I/O slots:  2, 3, 4, 5, 6, 7, 8,
Testing NVRAM.....................done
Testing RAM ......................done
Testing Boot FLASH....CSUM 0xABCD..done
Testing PCI Bus ..................done
Testing ISA ......................done
Testing Ethernet Controller1.......done
Testing Ethernet Controller2.......done
Found CPU7400/G4, PVR=000C0200,
CPU clock: 350MHz, Bus clock: 100MHz, E +27C
SDRAM mode enabled
Onboard DRAM       :  128MB, 0x00000000..0x03FFFFFF
Init SDRAM Module 1:  none
Init SDRAM Module 2:  none
Init DTLB/ITLB for block translation, enable MMU
Init L1-Icache
Init L1-Dcache
Init L2-Cache, found 1024 kByte cache, 140MHz
Init exception vectors starting at address: 0x00000100
Read NVRAM...identify board
BIB version: 2.0
Ethernet 1: 00:80:42:0E:30:32
Ethernet 2: 00:80:42:0E:30:33

<<PowerBoot V3.33 for PowerCoreCPCI CPU-680>>

PowerBoot> _
```

SETBOOT – Editing Auto Boot Parameters

SETBOOT prompts the user to enter values for the parameters required for the auto booting. The defined parameters become valid after the next power-on or when RESET is entered. The parameters are stored in the on-board NVRAM which keeps its contents during power off and checks them after power on or after RESET has been entered.

Syntax

SETBOOT

Description

After SETBOOT has been entered, the user is prompted to assign a value to each parameter described in the following. The prompt describes briefly the possible values of the respective parameters and the current setting.
The parameters described in the following:

- Define the location of the automatically loaded binary image: boot select defines the location of the automatically loaded binary image:.
- Determine the kind of booting and the location where the binary image is started: auto boot enables or disables the auto booting:, boot address specifies the location in the CPU addressing space where the opcode is started. It is independent of other NVRAM parameters. The binary image always starts at boot address, regardless whether it is downloaded during power on to load address or stored in the user flash. For further information on the address map see “PPC/PowerCoreCPCI-680 Address Map” page 7-5., load address specifies the location in the CPU addressing space where the opcode is downloaded. `load address` does not depend on other NVRAM parameters. The binary image is always downloaded to load address by using the boot select defines the location of the automatically loaded binary image: parameters 0, 2, 6,8,9..
- Select a delay for the auto booting after power-on: auto boot delay selects a delay ranging from 0 to 99 seconds, i.e. this parameter delays the auto booting by a preset period of time. This is useful for example in case of spinning up a ATA/IDE or SCSI hard disk drive for booting. During count down of auto boot delay the autobooting can be stopped by pressing any user key on the serial console line..

- Select a hard disk SCSI ID for booting a boot file: boot disk SCSI ID.
- Select a controller SCSI ID for a mounted PMC module: PMCx controller SCSI ID.
- Define the name and the path of the file loaded during auto boot: TFTP / disk boot file name defines the name and path of the file which will be loaded during auto boot (if boot select = 0, 6, 8,9). The file name including path has 128 characters at the most. If TFTP is used for booting, the host must be set up as TFTP server (boot select = 0 or 8). The host has to be able to provide the desired file via Ethernet (TFTP and front panel connector). If a SCSI hard disk is used for booting (boot select = 6), it must be set to the corresponding parameters defined by boot disk SCSI ID and PMCx controller SCSI ID. If a ATA / IDE hard disk is used for booting (boot select = 9), always ATA / IDE hard disk drive 0 of the Primary ATA / IDE interface is used. At first the hard disk partitions 0 to 3 are scanned in order to find a PREP partition (41_{16}). If no PREP partition is found, a DOS 4.0-compatible hard-disk partition (06_{16}) will be searched. In case of a valid DOS 4.0 partition, TFTP / disk boot file name must be limited to a maximum of 8 characters followed by a dot `.` and an extension consisting of 3 characters (e.g. myfile.bin). All other names are ignored. Do not type a hard disk character like `C:\` in front of TFTP / disk boot file name. The root directory of the hard-disk partition is searched only for TFTP / disk boot file name. Subdirectory levels are not searched and FAT32 systems are not supported. ATA / IDE hard disk drives are supported for DOS 4.0-compatible boot only. In both cases (TFTP and hard disk) the user is fully responsible for upper case letters, lower case letters, and the file name itself..
- Select whether front [1] or rear [2] Ethernet controller / connector will be used for file load during auto boot.
- Select the internet protocol for connecting a server to the board: RARP or ARP protocol selects the internet protocol used for connecting a server to the board..
- Select the protocol numbers for selecting the TFTP file server and for identifying the board: serverIP# defines the internet protocol number which selects the TFTP file server. If the internet protocol RARP is selected, serverIP# will be ignored. serverIP# is stored as string, therefore it has to be written as shown in the following example 123.3.255.255., targetIP# defines the internet protocol number identifying the board at internet layer. If the internet protocol RARP is selected, targetIP# will be ignored. targetIP# is stored as string,

therefore it has to be written as shown in the following example 3.255.37.67..

- Define the I/O or MEM address as seen from the PCI bus which will be written to the PCI bus device of the PMC1 or the PMC2 module: PMC1 PCI bus I/O base address and MEM base address, same applies to PMC2.
- Select the order in which the CompactPCI slots will be scanned for PCI devices if the PPC/PowerCoreCPCI-680 runs in the Compact-PCI system controller mode (slot #1).
- Define the MEM downstream base address and limit which will be written into the PCI-to-PCI bridge if running in transparent mode.
- Define the I/O or MEM upstream and downstream base addresses, translated addresses, and set-up base addresses which will be written into the PCI-to-PCI device for running in non-transparent mode.
- Define whether the PCI-to-PCI device Primary Access Lockout bit is cleared after PowerBoot has initialized the board when running in non-transparent mode.
- Define whether the power on test (POT) should not be executed after next power on or reset.

boot select
defines the location of the automatically loaded binary image:

- 0 = autoloads a binary image to load address via Ethernet (TFTP and front-panel connector). The user must link the download application image to load address. boot address is used for starting the downloaded image.
- 2 = copies the user flash memory contents of user flash 1..4 in case of 4× 2MByte user flash devices (or user flash 1..2 in case of 4× 4MByte user flash devices) to load address and starts executing at boot address. There is always a sum of 8MBytes copied regardless of the type/size of devices assembled and the amount of already programmed/used user flash storage capacity.
- 6 = autoloads a PREP boot image from a SCSI hard disk as described in the PREP specification. If no PREP partition is found, a DOS 4.0 partition will be used. It is assumed that a PMC module is mounted at PMC1 or PMC2, which holds an NCR53C825 or an NCR53C875 SCSI 2 controller. The user has to prepare the hard disk format to be PREP compliant or DOS 4.0 compliant. Furthermore, the application image must be prepared for booting. If the partition format DOS 4.0 is used, the pure binary file to be booted can be copied from PC as normal DOS file to the root partition of the hard disk. The parameter

load address is used for downloading, boot disk SCSI ID for identifying the hard disk, PMCx controller SCSI ID is used for identifying the PMC based SCSI controller and auto boot delay for selecting a delay period after power on. boot address is used for starting the downloaded image.

- 7 = writes all parameters for the upstream and downstream windows to the PCI-to-PCI bridge. The primary lockout bit at the PCI-to-PCI bridge is set before the upstream and downstream parameters will be written. After this, the primary lockout bit will be cleared regardless of its status before autobooting.
- 8 = includes the same procedures as value 7 described above. Additionally, a binary image is autoloaded to load address via Ethernet (TFTP and front-panel connector). The user must link the download application image to load address. boot address is used for starting the downloaded image.
- 9 = autoloads a boot image from a ATA / IDE hard disk. A DOS 4.0 partition will be used. It is assumed that a ATA / IDE controller is accessible at the PCI-to-ISA bridge device. The user has to prepare the ATA / IDE hard disk format to be DOS 4.0 compliant. Furthermore, the application image must be prepared for booting. If the partition format DOS 4.0 is used, the pure binary file to be booted can be copied from PC as normal DOS file to the root partition of the hard disk. Subdirectories are not searched. The parameter load address is used for downloading, boot address is used for starting the downloaded image, TFTP / disk boot file name is used to define the boot file name and auto boot delay for selecting a delay period after power on. Primary ATA / IDE controller interface device 0 (Master) is used

auto boot
enables or disables the auto booting:

- 0 = auto boot disabled. All NVRAM parameters are ignored. The PowerBoot debugger is invoked.
- 1 = auto boot enabled. Auto boot will take place after the next power on or when RESET is used.

auto boot delay
selects a delay ranging from 0 to 99 seconds, i.e. this parameter delays the auto booting by a preset period of time. This is useful for example in case of spinning up a ATA / IDE or SCSI hard disk drive for booting. During count down of auto boot delay the autobooting can be stopped by pressing any user key on the serial console line.

load address
specifies the location in the CPU addressing space where the opcode is downloaded. `load address` does not depend on other NVRAM parameters. The binary image is always downloaded to load address by using the boot select defines the location of the automatically loaded binary image: parameters 0, 2, 6,8,9.

boot address
specifies the location in the CPU addressing space where the opcode is started. It is independent of other NVRAM parameters. The binary image always starts at boot address, regardless whether it is downloaded during power on to load address or stored in the user flash. For further information on the address map see “PPC/PowerCoreCPCI-680 Address Map” page 7-5.

boot disk SCSI ID
selects the hard disk SCSI ID for booting the hard disk. boot disk. SCSI ID is set to:

- 0 for hard disk drive 0
- 1 for hard disk drive 1
- 2 for hard disk drive 2, and so on

boot disk SCSI ID can range between 0 and 15 and supports wide SCSI drives. boot disk SCSI ID is used only for the autoboot functionality. Other drives and their SCSI IDs may also be connected but they will be ignored during autobooting. SCSI parity checking is not supported.

PMCx controller SCSI ID
selects the SCSI controller ID for booting the hard disk. PMCx controller SCSI ID is set to:

- 0 for SCSI ID 0
- 1 for SCSI ID 1
- 2 for SCSI ID 2 and so on

PMCx controller SCSI ID can range between `0` and `15` and supports wide SCSI drives. PMCx controller SCSI ID is used only for the autoboot functionality. It may be changed on demand by an application software. SCSI parity checking is not supported.

PowerBoot checks PMC1 and PMC2 for a mounted PMC module containing either the NCR53C825 or the NCR53C875 SCSI controller. If one of the above SCSI controllers is found, it will be mapped automatically by firmware to the addresses shown in the table below.

Table 21: *PCI I/O Addressing Spaces of the SCSI Controllers*

PCI I/O Addressing Space	NCR53C825	NCR53C875
Seen from the CPU	$FE820000_{16}$	$FE830000_{16}$
Seen from the PCI bus	00820000_{16}	00830000_{16}

Other SCSI controllers are not supported and will therefore be ignored.

Front [1] or rear [2] Ethernet
selects whether the front panel connected Ethernet controller #1 or the rear connector extension Ethernet controller #2 is used for autoboot.

Note: For the rear connector extension the rear transition board ACC/RTB-600 must be plugged into the CompactPCI backplane to provide standard Ethernet RJ-45 cable connector.

RARP or ARP protocol
selects the internet protocol used for connecting a server to the board.

- 1 = selects RARP (Reverse Address Resolution Protocol). In case of RARP the parameters `serverIP#` and `targetIP#` are ignored.
- 2 = selects ARP (Address Resolution Protocol). In case of ARP the values entered for the parameters `serverIP#` and `targetIP#` are valid.

If another value is entered, the default setting `1` will be assigned to the parameter.

serverIP#
defines the internet protocol number which selects the TFTP file server. If the internet protocol RARP is selected, serverIP# will be ignored. serverIP# is stored as string, therefore it has to be written as shown in the following example *123.3.255.255*.

targetIP#
defines the internet protocol number identifying the board at internet layer. If the internet protocol RARP is selected, targetIP# will be ignored. targetIP# is stored as string, therefore it has to be written as shown in the following example *3.255.37.67*.

TFTP / disk boot file name
defines the name and path of the file which will be loaded during auto boot (if boot select = 0, 6, 8,9). The file name including path has 128 characters at the most.

If TFTP is used for booting, the host must be set up as TFTP server (boot select = 0 or 8). The host has to be able to provide the desired file via Ethernet (TFTP and front panel connector).
If a SCSI hard disk is used for booting (boot select = 6), it must be set to the corresponding parameters defined by boot disk SCSI ID and PMCx controller SCSI ID. If a ATA / IDE hard disk is used for booting (boot select = 9), always ATA / IDE hard disk drive 0 of the Primary ATA / IDE interface is used.
At first the hard disk partitions 0 to 3 are scanned in order to find a PREP partition (41_{16}). If no PREP partition is found, a DOS 4.0-compatible hard-disk partition (06_{16}) will be searched. In case of a valid DOS 4.0 partition, TFTP / disk boot file name must be limited to a maximum of 8 characters followed by a dot `.` and an extension consisting of 3 characters (e.g. myfile.bin). All other names are ignored. Do not type a hard disk character like `C:\` in front of TFTP / disk boot file name. The root directory of the hard-disk partition is searched only for TFTP / disk boot file name. Subdirectory levels are not searched and FAT32 systems are not supported. ATA / IDE hard disk drives are supported for DOS 4.0-compatible boot only.
In both cases (TFTP and hard disk) the user is fully responsible for upper case letters, lower case letters, and the file name itself.

PMCx PCI bus I / O or MEM base address
defines the respective I / O or MEM address based on the PCI bus device of the PMC*x* module.

The following description is divided into two parts. The first part is a general description of the PMC modules and their base addresses whereas the second part describes the four parameters.
On the PPC / PowerCoreCPCI-680 up to two PMC modules can be installed. Every PMC module can have two different base addresses: One base address in the PCI bus I / O space and one base address in the PCI bus MEM space.
Depending on the features of the installed PMC modules, the addresses have to be set differently:

- If no PMC module is installed, set both addresses to `0`.
- If the installed PMC modules support only one addressing space, set the address which is not supported to $FFFFFFFF_{16}$ to disable it.
- If the installed PMC modules support both addressing spaces, set both addresses to the desired value.

Note: Do not set a PMC module base address to an address already used by the on-board PCI bus devices (see Table 19 "PPC/PowerCoreCPCI-680 Address Map Seen from the CPU" page 7-5).

The following four parameters are described below:

- PMC1 PCI bus I/O base address
- PMC1 PCI bus MEM base address
- PMC2 PCI bus I/O base address
- PMC2 PCI bus MEM base address

When defining the I/O base address of PMC*x*, the following is done:

- PCI bus master bit (bit 2) is set to 1.
- PCI bus I/O space control bit (bit 0) is set to 1.
- The value of the I/O base address is written to a PCI device header offset $10_{16}..24_{16}$ which supports PCI I/O space. The first I/O base address register in the PCI device header type region is used.

When defining the MEM base address of PMC*x*, the following is done:

- The PCI bus master bit (bit 2) is set to 1.
- The PCI bus MEM space control bit (bit 1) is set to 1.
- The value of the MEM base address is written to a PCI device header offset $10_{16}..24_{16}$ which supports PCI memory space. The first MEM base address register in the PCI device header type region is used.

The SETBOOT parameters shown below are valid for transparent mode of the SENTINEL PCI-to-PCI bridge only. This applies if the PPC/PowerCoreCPCI-680 is mounted as system controller in the CompactPCI I/O slot 1.

Compact PCIbus probe list
determines the order in which the I/O slots at the CompactPCI bus are probed for PCI devices. A configuration cycle of type 1 is generated for every slot in the given order at the local PPC/PowerCoreCPCI-680 PCI bus and converted via the SENTINEL transparent PCI-bridge to a configuration cycle of type 0. This SETBOOT parameter will only be valid if the PPC/PowerCoreCPCI-680 is a CompactPCI system controller and the SENTINEL PCI-to-PCI bridge is running in transparent bridge mode. In the I/O-mode/nontransparent-mode of the SENTINEL device this parameter will be ignored.

Downstream Memory Base/Limit address
defines the memory base addresses written into the PCI-to-PCI base address register for the downstream window if the SENTINEL is configured as transparent PCI-bridge. In the I/O-mode/nontransparent-mode of the SENTINEL device this parameter will be ignored.

The SETBOOT parameters shown below are valid for the nontransparent-mode/I/O-mode of the SENTINEL PCI-to-PCI device only. This applies if the PPC/PowerCoreCPCI-680 is mounted in a CompactPCI I/O slot 2..8.

OVERwrite Upstream/Downstream Setup Regs
defines whether the upstream/downstream setup registers of SENTINEL are patched by NVRAM values. "1" enables the patching of the serial I^2C ROM downloaded set-up register values by autoboot NVRAM based values. The set-up register values given by the user later on are used. "0" disables the patching of the serial I^2C ROM downloaded set-up register values. The string expression "-NA-" will be shown instead of a user input line. No set-up register is changed or patched in that case.

Note: The serial I^2C ROM connected to SENTINEL PCI-to-PCI bridge/device contains a standard register setup image which configures SENTINEL PCI-to-PCI bridge/device immediately after reset. It is recommended that the user checks its setboot parameters compared to the serial I^2C ROM standard register setup to avoid any unwanted interference which may cause unwanted configuration side effects further on. For more information on these registers setup refer to the SENTINEL *Reference Guide*.

Downstream DSR or I/O or MEM 0..4 BAR
defines the base addresses written into the PCI-to-PCI base address register for the downstream windows 0, 2, 3, and 4. If bit 31 of the Downstream I/O or MEM 0..4 Setup Register defines the setup value written into the PCI-to-PCI set-up register for the downstream windows 0, 2, 3, and 4. Downstream I/O or MEM 0..4 Setup Register defines the size of the appropriate window. For further information on these registers refer to the SENTINEL Reference Guide. (see below) is zero, the respective window will be disabled and Downstream DSR I/O or MEM 0..4 BAR value will be ignored. The window 0 contains the DSR register set in the first 4 KByte of the memory space. Therefore, the minimum size of the window 0 is 4 KByte. The remaining address space of the window 0 can be set up into the MEM space. The window 2 can be set up into the

I/O space or MEM space. The window 3 can be set up only into the MEM space. The window 4 can be set up only into the MEM space. For further details on these registers refer to the *SENTINEL Reference Guide.*

Note: At CompactPCI systems Downstream DSR I/O or MEM 0..4 BAR registers are usually initialized by the CompactPCI system controller and not by the PPC/PowerCoreCPCI-680 local CPU if running in nontransparent-mode/I/O-mode. Nevertheless, PowerBoot as a booter/debugger provides the capability to influence these registers. Note that this may interfere with the CompactPCI system controller settings initialized at CompactPCI bus probing. Especially, watch Downstream DSR MEM 0 BAR which holds the 4 KByte DSR register area.

Upstream I/O or MEM 2..3 BAR
defines the base addresses written into the PCI-to-PCI base address register (BAR) for the upstream windows 2 and 3. If bit 31 of the Upstream I/O or MEM 2..3 Setup Register defines the set-up value written into the PCI-to-PCI set-up register for the upstream windows 2 and 3. Upstream I/O or MEM 2..3 Setup Register defines the size of the appropriate window. For further information on these registers refer to the SENTINEL Reference Guide. (see below) is zero, the respective window is disabled. Window 2 can be set up in the I/O space or MEM space, whereas window 3 can be set up only in the MEM space. For further information on these registers refer to the *SENTINEL Reference Guide*.

Downstream I/O or MEM 0..4 Translated BAR
defines the base address written into the PCI-to-PCI translated base address registers 0, 2, 3, and 4. Accesses from the primary to the secondary side of the nontransparent-mode/I/O-mode device are translated into the address ranges in the registers. For further information on these registers refer to the *SENTINEL Reference Guide.*

Upstream I/O or MEM 2..3 Translated BAR
defines the base address written into the PCI-to-PCI translated base address registers 2 and 3. Accesses from the secondary to the primary side of the nontransparent-mode/I/O-mode device are translated into the address ranges in the registers. For further information on these registers refer to the *SENTINEL Reference Guide*.

Downstream I/O or MEM 0..4 Setup Register
defines the setup value written into the PCI-to-PCI set-up register for the downstream windows 0, 2, 3, and 4. Downstream I/O or MEM 0..4

Setup Register defines the size of the appropriate window. For further information on these registers refer to the *SENTINEL Reference Guide.*

Upstream I/O or MEM 2..3 Setup Register
defines the set-up value written into the PCI-to-PCI set-up register for the upstream windows 2 and 3. Upstream I/O or MEM 2..3 Setup Register defines the size of the appropriate window. For further information on these registers refer to the *SENTINEL Reference Guide.*

Clear LOCKOUT bit
defines whether the PCI-to-PCI bridge Primary Access LOCKOUT bit (bit 9) at the Chip Control 1 Register is cleared to 0 after booting procedure, or whether it is left at the default power-on setting. The default power-on LOCKOUT bit setting is defined by hardware as 1. This SETBOOT parameter is independent of all other SETBOOT parameters stored in NVRAM and is checked after every reboot of the PPC/PowerCoreCPCI-680. For further information on this bit refer to the *SENTINEL Reference Guide.*

Note: If the CompactPCI system controller – not being a PPC/PowerCoreCPCI-680 board – in the Compact PCI rack does not seem to boot after power on, the Primary Access Lockout bit of every PCI-to-PCI device SENTINEL running in non-transparent mode located on the PPC/PowerCoreCPCI-680 in every used CompactPCI I/O slot must be cleared. This prevents the CompactPCI system controller board from being stuck on endless PCI bus retry cycles while probing the CompactPCI bus configuration. For further information refer to the *SENTINEL Reference Guide*.

Power On Test POT
is the command to disable the Power On Test (POT) which is executed at boot-up time:

- `1` = disables the Power On Test.
- `0`= enables the Power On Test (default).

The Power On Test results are stored at NVRAM. The results are stored at NVRAM offset `0x1E04` having the bit layout as seen below:

```
DRAM testokaybit0 = 1,DRAM test failbit0 = 0;
PCI testokaybit1 = 1,PCI test fail bit1 = 0;
ISA testokaybit2 = 1,ISA test fail bit2 = 0;
BootFlash CRCokaybit3 = 1,BootFlash CRC failbit3 = 0;
Ethernet1okaybit4 = 1,Ethernet1 fail bit4 = 0;
NVRAM testokaybit5 = 1,NVRAM test fail bit5 = 0;
Ethernet2okaybit6 = 1,Ethernet2 fail bit6 = 0;
```

Therefore a fully functional PPC/PowerCoreCPCI-680 will show the value `0x7F` for all tests okay. A failure will not stop the power-up process of the PPC/PowerCoreCPCI-680, because debug functionality must be provided via console serial interface 1. The Power On Test is shown like this:

```
Testing NVRAM.....................done
Testing RAM ......................done
Testing Boot FLASH....CSUM 0x20A7..done
Testing PCI Bus ..................done
Testing ISA ......................done
Testing Ethernet Controller1.......done
Testing Ethernet Controller2.......done
```

If the Power On Test is disabled, a value of 0x00 will be stored at NVRAM offset 0x1E2C to indicate that no test results are available. It is indicated as follows:

```
Power On Test disabled
```

After the last parameter has been typed in, a checksum is calculated to protect the NVRAM contents from offset $1C00_{16}$ to $1FF0_{16}$ containing all edited parameters.

Example

```
PowerBoot>
PowerBoot> setboot

 -General boot parameters-

Boot select [0=Net,2=Flash+Copy,6=SCSI,7=PCI,8=PCI+Net,9=ATA-
IDE] (0) :
Auto boot   [0=disable, 1=enable], (0)   :
Auto boot delay [0..99s], (0)   :
Load address (00000000) :
Boot address (00000000) :
Boot Disk SCSI-ID [0..15], (0) :
PMCx Controller SCSI-ID [0..15], (0) :

-TFTP/SCSI/ATA-IDE boot file name-

Front [1] or rear [2] Ethernet : (1) :
RARP [1] or ARP [2] protocol : (1) :
Server-IP# [aaa.bbb.ccc.ddd] : :
Target-IP# [aaa.bbb.ccc.ddd] : :
TFTP/SCSI/ATA-IDE Disk Boot file name :
: myfile.bin

 -PMC module mapping parameters-

PMC1 PCIbus I/O base address (00000000) :
PMC1 PCIbus MEM base address (00000000) :
PMC2 PCIbus I/O base address (00000000) :
PMC2 PCIbus MEM base address (00000000) :
```

```
-PCI-to-PCI bridge host-mode parameters-

Compact PCIbus probe list [8,7,6,5,4,3,2] (2,3,4,5,6,7,8) :
Downstream Memory Base address  (81000000) :
Downstream Memory Limit address (8FFFFFFF) :

-PCI-to-PCI device I/O-mode Up-/Downstream window mapping
addresses-

OVERwrite Upstream/Downstream Setup Regs [0=disable, 1=enable],
(0):

Upstream   I/O MEM 2 BAR        (00000000) :
Upstream       MEM 3 BAR        (00000000) :
Downstream DSR MEM 0 BAR        (84000000) :
Downstream I/O MEM 2 BAR        (80000000) :
Downstream     MEM 3 BAR        (00000000) :
Downstream     MEM 4 BAR        (00000000) :
Downstream DSR MEM 0 Trans Base (84000000) : -NA-
Downstream DSR MEM 0 Setup Reg. (FFFF0000) : -NA-
Downstream I/O MEM 2 Trans Base (00200000) : -NA-
Downstream I/O MEM 2 Setup Reg. (FFF00000) : -NA-
Downstream     MEM 3 Trans Base (00000000) : -NA-
Downstream     MEM 3 Setup Reg. (00000000) : -NA-
Downstream     MEM 4 Trans Base (00000000) : -NA-
Downstream     MEM 4 Setup Reg. (00000000) : -NA-
Upstream   I/O MEM 2 Trans Base (00000000) : -NA-
Upstream   I/O MEM 2 Setup Reg. (00000000) : -NA-
Upstream       MEM 3 Trans Base (00000000) : -NA-
Upstream       MEM 3 Setup Base (00000000) : -NA-


 -PCI-to-PCI device I/O-mode LOCKOUT bit setup-

Clear LOCKOUT bit [0=untouched, 1=clear], (0):

-Power On Test (POT) parameters-
Power On Test POT [1=disable, 0=enable], (0) :
.
.
.
CSUM : 0x1800
PowerBoot> _
```

Note: All additional parameters are for internal use only. Do not change default settings.

USERLED – Setting User LED

USERLED defines the color of the user LED at the front panel. The on-board user LED is red, green, or can be turned off.

Syntax

USERLED 1 or 2 *color*

color

defines the color of the user LED1 or 2:

- *red* = user LED U 1 or 2 is red.
- *green* = user LED U 1 or 2 is green.
- *dis* = user LED U 1 or 2 is OFF.
- *hw* = user LED U 1 or 2 prepared for hardware driven mode

Example

In the following example the user LED U is green:

```
PowerBoot> USERLED 1 green
PowerBoot> _
```

Accessing the PCI Bus

PowerBoot provides a set of commands for accessing the PCI bus.

Note: The commands CONFIG_RD, CONFIG_WR, BUSSHOW, AGENTSHOW, and FINDDEVICE are used in SENTINEL transparent mode only. This applies if the PPC/PowerCoreCPCI-680 is mounted as system controller in the CompactPCI I/O slot 1.

CONFIG_RD - PCI Bus Configuration Read Cycles

CONFIG_RD performs a PCI bus configuration read cycle from an address specified by the bus number, the function number, and the slot number.

Syntax

CONFIG_RD *<bus-nr><dev-nr><fun-nr><reg-nr> [B|W|L]*

bus-nr

specifies the PCI bus segment.
dev-nr
specifies the PCI bus device number.
fun-nr
specifies the PCI bus device function number.
reg-nr
specifies the address / register offset.
[B/W/L]
specifies the size of bytes fetched:

- *B* = byte (8bit)
- *W* = word (16bit)
- *L* = long (32bit)

Example

The example below illustrates a PCI bus configuration read cycle of 32 bit of data:

```
PowerBoot> config_rd 0 18 0 4 l
address: 0x8000C004
0x02800007
PowerBoot>
```

CONFIG_WR - PCI Bus Configuration Write Cycles

CONFIG_WR performs a PCI bus configuration write cycle to an address specified by the bus number, the function number, and the slot number.

Syntax

`CONFIG_WR <bus-nr><dev-nr><fun-nr><reg-nr><data> [B|W|L]`

bus-nr

specifies the PCI bus segment.
dev-nr
specifies the PCI bus device number.
fun-nr
specifies the PCI bus device function number.
reg-nr
specifies the address / register offset.
data
specifies the data to be stored.
[B/W/L]
specifies the size of bytes stored:

- *B* = byte (8bit)
- *W* = word (16bit)
- *L* = long (32bit)

Example

The example below illustrates a PCI bus configuration write cycle of 8 bit of data:

```
PowerBoot> config_wr 0 18 0 19 1 b
address: 0x8000C019
PowerBoot>
```

BUSSHOW - Scan All PCI Bus Segments and Print Devices Found

BUSSHOW scans all PCI bus segments printing the vendor and device ID as well as the bus number, device number, and function number of all PCI agents found.

Syntax

```
BUSSHOW
```

Example

The example below illustrates the information printed if executing the command busshow:

```
PowerBoot> busshow
Found PCI device: Vendor/DeviceID: 0x00021057 at bus 0x00, device
0x00, function 0x0
Found PCI device: Vendor/DeviceID: 0x00221011 at bus 0x00, device
0x18, function 0x0
Found PCI device: Vendor/DeviceID: 0x00191011 at bus 0x00, device
0x19, function 0x0
Found PCI device: Vendor/DeviceID: 0x056510ad at bus 0x00, device
0x1e, function 0x0
Found PCI device: Vendor/DeviceID: 0x010510ad at bus 0x00, device
0x1e, function 0x1
Found PCI device: Vendor/DeviceID: 0x00241011 at bus 0x01, device
0x09, function 0x0
Found PCI device: Vendor/DeviceID: 0x908010b5 at bus 0x01, device
0x0d, function 0x0
Found PCI device: Vendor/DeviceID: 0x00031000 at bus 0x02, device
0x05, function 0x0
Found PCI device: Vendor/DeviceID: 0x80789004 at bus 0x02, device
0x06, function 0x0
Found PCI device: Vendor/DeviceID: 0xf0ce11af at bus 0x02, device
0x09, function 0x0
Found PCI device: Vendor/DeviceID: 0x00091011 at bus 0x02, device
0x0b, function 0x0

PowerBoot>
```

AGENTSHOW - Print the Config Register of a Device

The command AGENTSHOW prints the standard PCI configuration register (0x00-0x40) to standard output with respect to whether a PCI device or a PCI bridge has been selected.

Syntax

AGENTSHOW *<bus-nr><dev-nr><fun-nr>*

bus-nr

specifies the PCI bus segment.
dev-nr
specifies the PCI bus device number.
fun-nr
specifies the PCI bus device function number.

Example

The example below illustrates the configuration register of an on-board PCI-to-PCI bridge:

```
PowerBoot> AGENTSHOW 0 18 0
PCI-to-PCI Bridge Configuration Header :
---------------------------------------
(0x00) PPB device and vendor IDs:       0x00221011
(0x04) PPB status and command:          0x02800007
(0x08) PPB revision ID:                 0x03
(0x09) PPB classCode:                   0x000004
(0x0c) PPB cache line Size:             0x00
(0x0d) PPB latency timer:               0x00
(0x0e) PPB header type:                 0x01
(0x0f) PPB BIST:                        0x00
(0x10) PPB base addresse 0:             0x00000000
(0x14) PPB base addresse 1:             0x00000000
(0x18) PPB primary bus:                 0x00
(0x19) PPB secondary bus:               0x01
(0x1a) PPB subordinate bus:             0x02
(0x1b) PPB sec. latency timer:          0x00
(0x1c) PPB I/O base:                    0x01
(0x1d) PPB I/O limit:                   0xf1
(0x1e) PPB secondary status:            0x2280
(0x20) PPB memory base:                 0x8000
(0x22) PPB memory limit:                0x8ff0
(0x24) PPB pref. memory base:           0xfff1
(0x26) PPB pref. memory limit:          0x0001
(0x28) PPB pref. upper memory base:     0xffffffff
(0x2c) PPB pref. upper memory limit:    0x00000000
(0x30) PPB upper I/O base:              0x008a
(0x32) PPB upper I/O limit:             0x008b
```

```
(0x34) PPB reserved:                    0x00000000
(0x38) PPB expansion rom addr:          0x00000000
(0x3c) PPB interrupt line:              0x00
(0x3d) PPB interrupt pin:               0x00
(0x3e) PPB bridge control:              0x0000
```

FINDDEVICE - Scan All PCI Bus Segments for a PCI Device

FINDDEVICE searches for a device in the whole PCI bus structure identified by its vendor and device ID. The bus number, device number, and function number of the devices found will be returned. The instance of the device can be selected, e.g.: Two devices with the same vendor and device ID reside in a PCI bus hierarchy. When the position of the first of the two devices is needed, the instant counter must be initialized to 0. For the second one, the instance counter must be initialized to 1.

Syntax

`FINDDEVICE <id><index>`

id

specifies the device / vendor id.
index
specifies instance.

Example

The example below illustrates the usage of the command FINDDEVICE:

```
PowerBoot> FINDDEVICE 00221011 0
Found PCI device - Vendor/DeviceID: 0x00221011 at bus 0x00,device
0x18,function 0x00
PowerBoot>
```

Flash Memory

PowerBoot enables you to easily program images into user flash memory devices.

Boot Flash 1

The boot flash device 1 acts like a read-only device and cannot be reprogrammed by using a PowerBoot command.

Boot Flash 2

The boot flash device 2 can be reprogrammed by using a PowerBoot command.

User Flash

Since the size of a user flash window is defined as 8 MByte by the PowerPC-to-PCI bridge, every user flash memory device is contiguously memory-mapped accessible from the user flash window in case of 4×2MByte devices being assembled. In case of 4×4MByte user flash devices, the user flash device 1 and 2 are accessible contiguously memory-mapped. User flash devices 3 and 4 are accessible by using a kind of bank switching logic, provided by the PowerBoot fselect command. The base addresses for the user flash device 1, 2, 3, and 4 (in case of 2MByte devices) are always $FF000000_{16}$, $FF200000_{16}$, $FF400000_{16}$, and $FF600000_{16}$ respectively. The base addresses for the user flash device 1 and 2 (in case of 4MByte devices) are always $FF000000_{16}$ and $FF400000_{16}$. The last address to be used for the user flash devices is $FF7FFFFF_{16}$ in every case.

Note: The example below relies on the 4×4MByte user flash devices assembly only. In case of 4×2 MBytes user flash devices assembly the given addresses will vary.

Programming the User Flash Devices

To program the user flash devices, proceed as follows:

1. Start the PPC / PowerCoreCPCI-680 PowerBoot by turning power on.

```
PowerBoot> _
```

2. Erase the user flash that you want to reprogram by using the ferase command. For example, if you want to erase user flash 1 type:

```
PowerBoot> ferase user_flash1
Erasing flash memory ... done.
```

Note: The ferase command erases the whole 4 MByte storage of the 4 MByte user flash device. If you only want to erase smaller parts of the user flash device you need to use certain offset and length parameters. For a list of these parameters refer to the *PowerBoot Instruction Set*.

---

3. In order to reprogram the user flash device you have just erased, you need to load the image into the DRAM memory first by using e.g. the netload command.

   Example:

```
PowerBoot> netload this-is-my-file-name 100000
Init Ethernet Controller MII-Port and PHY-Device
PHY-Device at 10MB/s negotiated
LAN-controller at address FE870000 set to Ethernet
00:80:42:0E:00:69
Transmitting RARP-REQUEST... Reception of RARP-REPLY
Transmitting TFTP-REQUEST to server 02:80:42:0A:0D:79, IP
192.168.41.1
PACKET:307 - loaded $00100000..$001265CF (157136 bytes)
PowerBoot> _
```

   As a second (principle) example, loading the word “FORCE” into user flash 1, you need to type the following:

```
PowerBoot> bf 100000 500000 “FORCE” p
```

4. Verify the DRAM memory contents by using the md command.

   Example:

```
PowerBoot> md 100000
00100000:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
00100010:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
00100020:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
00100030:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
00100040:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
00100050:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
00100060:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
00100070:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
00100080:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
00100090:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
001000a0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
001000b0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
001000c0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
001000d0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
001000e0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
001000f0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
More (cr) ? .
PowerBoot>
```

5. Program the image from the DRAM memory into the user flash device 1 by using the `fprog` command. The DRAM memory contents from 100000_{16}..$4FFFFF_{16}$ will be programmed.

   Example:

```
PowerBoot> fprog user_flash1 100000
Programming flash memory
0 ... 100%
Done.
```

6. To see the contents of the programmed user flash memory 1 use the md command.

   Example:

```
PowerBoot> md ff000000
00100000:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
00100010:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
00100020:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
00100030:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
00100040:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
00100050:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
00100060:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
00100070:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
00100080:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
00100090:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
001000a0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
001000b0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
001000c0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
001000d0:  45 20 46 4f 52 43 45 20  46 4f 52 43 45 20 46 4f
001000e0:  52 43 45 20 46 4f 52 43  45 20 46 4f 52 43 45 20
001000f0:  46 4f 52 43 45 20 46 4f  52 43 45 20 46 4f 52 43
More (cr) ?
PowerBoot>
```

Programming Images of Various Sizes

PowerBoot enables you to program images that are:

- Smaller than 4 MByte
- Larger than 4 MByte
- Larger than 8 MByte

Images Smaller than 4 MByte

To program images smaller than 4 MByte use the following command:

```
PowerBoot> fprog user_flash(x) source
```

Note: Your image is programmed from offset 0 until the end of your image. The remaining parts of the flash memory device storage are programmed with random data from your DRAM memory. In order to program only the image, use the same command and additionally type the length of the specific file in hexadecimal numbers as an add-on parameter.

Images Larger than 4 MByte

To program images larger than 4 MByte use the following commands (Remember: 4MByte user flash assembly!):

```
PowerBoot> fprog user_flash(x) source
```

and

```
PowerBoot> fprog user_flash(x+1) source+40.0000_16
```

Note: Your image is programmed from offset 0 of the first user flash device until the end of the first user flash device. The second command programs your image from offset 0 of the second user flash device until the end of your image. The remaining parts of the second user flash device are programmed with random data from your memory. In order to program only the image, use the same two commands. Since the first user flash device is programmed with 4 MByte you need to type the residual length of the specific file in hexadecimal numbers after the second command. The residual length is the full length minus 4 MByte.

Example:

```
PowerBoot> fprog user_flash1 100000
PowerBoot> fprog user_flash2 500000
```

Images Larger than 8 MByte

To program images larger than 4 MByte use the following commands:

```
PowerBoot> fprog user_flash(x) source
```

and

```
PowerBoot> fprog user_flash(x+1) source+40.0000_16
```

and

```
PowerBoot> fprog user_flash(x+2) source+80.0000_16
```

Note: Your image is programmed from offset 0 of the first user flash device until the end of the first user flash device. The second command programs your image from offset 0 of the second user flash device until the end of the second user flash device. The third command programs your image from offset 0 of the third user flash device until the end of your image. The remaining parts of the third user flash device are programmed with random data from your memory. In order to program only the image, use the same three commands. Since the first and the second user flash devices are programmed with 8 MByte you need to type the residual length of the specific file in hexadecimal numbers after the third command. The residual length is the full length minus 8 MByte.

Example:

```
PowerBoot> fprog user_flash1 100000
PowerBoot> fprog user_flash2 500000
PowerBoot> fprog user_flash3 900000
```

Note: PowerBoot automatically handles all bank switching to access 4 MByte user flash devices 3 and 4 in case of PowerBoot ferase/fprog command. A flash device must be erased prior to reprogramming.

8

Maps and Registers

Address Maps

The PPC/PowerCoreCPCI-680 provides a CHRP compliant address map. The following tables given below show the address maps of the PPC/PowerCoreCPCI-680:

- Memory Map Seen from CPU (addresses on the processor bus)
- Memory Map Seen from PCI Bus (memory space addresses on the PCI bus)
- I/O Map Seen from PCI Bus (I/O space addresses on the PCI bus)
- Configuration Base Addresses (configuration addresses for the on-board PCI devices)
- ISA Bus Ports Seen from CPU (physical addresses for the on-board ISA devices)
- PCI I/O Devices Seen from CPU (physical addresses for the on-board PCI I/O devices)

Table 22: *Memory Map Seen from CPU*

Address on PPC Bus	Device	Accessible Bus		Cache		Bus Width [bit]
		PCI	CPCI	L1	L2	
00000000_{16} .. $3FFFFFFF_{16}$	Main memory space consisting of: On-board memory, Lower memory module. Upper memory module The memory space begins with bank 0 and is contiguous. The end address depends on the memory capacity.	Y	Y	Y	Y	[64]
40000000_{16} .. $7FFFFFFF_{16}$	Reserved	–	–	–	–	–
80000000_{16} .. $FCFFFFFF_{16}$	PCI memory space CPCI memory space	Y	Y	N	N	[32]
$FD000000_{16}$ .. $FDFFFFFF_{16}$	PCI/ISA memory space 00000000_{16} .. $00FFFFFF_{16}$ on PCI memory space	Y	Y	N	N	[8]

Table 22: *Memory Map Seen from CPU (cont.)*

Address on PPC Bus	Device	Accessible Bus		Cache		Bus Width [bit]
		PCI	CPCI	L1	L2	
$FE000000_{16}$ .. $FE00FFFF_{16}$	ISA bus ports (see Table 26 “ISA Bus Ports Seen from CPU” page 8-7)	Y	Y	N	N	[8]
$FE01.0000_{16}$ .. $FE7FFFFF_{16}$	Reserved	–	–	–	–	–
$FE800000_{16}$ .. $FEBFFFFF_{16}$	PCI I/O space 00800000_{16} .. $00BFFFFF_{16}$ on PCI I/O space (see Table 24 “I/O Map Seen from PCI Bus” page 8-6)	Y	Y	N	N	[32]
$FEC00000_{16}$ .. $FEDFFFFF_{16}$	Configuration address register of the PPC-to-PCI bridge (any aligned address)	N	N	N	N	[32]
$FEE00000_{16}$ .. $FEEFFFFF_{16}$	Configuration data register of the PPC-to-PCI bridge (any aligned address)	N	N	N	N	[32]
$FEF00000_{16}$ .. $FEFFFFFF_{16}$	PCI interrupt acknowledge	N	N	N	N	[32]
$FF000000_{16}$ .. $FF7FFFFF_{16}$	User flash space (end address depends on capacity of user flash memory)	Y	Y	Y	Y	[8]
$FF800000_{16}$ .. $FFBFFFFF_{16}$	Diagnostic port	Y	Y	N	N	[8]
$FFC00000_{16}$ .. $FFEFFFFF_{16}$	Reserved	–	–	–	–	–
$FFF00000_{16}$ .. $FFF7FFFF_{16}$	Boot flash device 1	Y	Y	Y	Y	[8]
$FFF80000_{16}$ .. $FFFFFFFF_{16}$	Boot flash device 2	Y	Y	Y	Y	[8]

Table 23: *Memory Map Seen from PCI Bus*

PCI Memory Address	Device	Accessible Bus		Cache		Bus Width [bit]
		PPC	CPCI	L1	L2	
00000000_{16} .. $3FFFFFFF_{16}$	Main memory space consisting of: On-board memory, Lower memory module, Upper memory module The memory space begins with bank 0 and is contiguous. The end address depends on the memory capacity.	Y	Y	Y	Y	[64]
40000000_{16} .. $7FFFFFFF_{16}$	Reserved	–	–	–	–	–
80000000_{16} .. $FCFFFFFF_{16}$	PCI memory space CPCI memory space	Y	Y	N	N	[32]
$FD000000_{16}$ .. $FDFFFFFF_{16}$	Main memory space 00000000_{16} .. $00FFFFFF_{16}$ on PowerPC CPU	Y	Y	N	N	[32]
$FE000000_{16}$ .. $FEFFFFFF_{16}$	Reserved	–	–	–	–	–
$FF000000_{16}$ .. $FF7FFFFF_{16}$	User flash space (end address depends on capacity of user flash memory)	Y	Y	Y	Y	[8]
$FF800000_{16}$ .. $FFBFFFFF_{16}$	Diagnostic port	Y	Y	N	N	[8]
$FFC00000_{16}$ .. $FFEFFFFF_{16}$	Reserved	–	–	–	–	–
$FFF00000_{16}$ .. $FFF7FFFF_{16}$	Boot flash 1	Y	Y	Y	Y	[8]
$FFF80000_{16}$ .. $FFFFFFFF_{16}$	Boot flash 2	Y	Y	Y	Y	[8]

Table 24: *I/O Map Seen from PCI Bus*

PCI I/O Address	Device	Accessible Bus		Cache		Bus Width [bit]
		PPC	CPCI	L1	L2	
00000000_{16} .. $0000FFFF_{16}$	ISA I/O space $FE00.0000_{16}$ … $FE00.FFFF_{16}$ on PowerPC CPU (see Table 22 “Memory Map Seen from CPU” page 8-3)	Y	Y	N	N	[8]
00010000_{16} .. $007FFFFF_{16}$	Reserved	–	–	–	–	–
00800000_{16} .. $00BFFFFF_{16}$	PCI I/O space FE80.000016 … FEBF.FFFF16 on PowerPC CPU (see Table 22 “Memory Map Seen from CPU” page 8-3)	Y	Y	N	N	[32]
$00C00000_{16}$ .. $FFFFFFFF_{16}$	Reserved	–	–	–	–	–

Table 25: *Configuration Base Addresses*

Configuration Base Address	Device
$8000C000_{16}$	Universal PCI-to-PCI bridge
$8000F000_{16}$	PCI-to-ISA bridge
$8000F100_{16}$	PCI-to-ISA bridge IDE interface function (used with optional CompactFlash slot only)
$8000C800_{16}$	Ethernet controller #1 (front panel)
$8000E000_{16}$	Ethernet controller #2 (rear transition board)
$8000D000_{16}$	PMC #1
$8000D800_{16}$	PMC #2

Table 26: *ISA Bus Ports Seen from CPU*

Address	Device
$FE000073_{16}$	NVRAM/RTC address low register
$FE000074_{16}$	Reserved
$FE000075_{16}$	NVRAM/RTC address high register
$FE000077_{16}$	NVRAM/RTC data register
$FE00.02F8_{16}$ .. $FE00.02FF_{16}$	Serial I/O port #2
$FE00.0300_{16}$ .. $FE00.0303_{16}$	CIO registers
$FE000308_{16}$	DRAM and cache configuration register DCCR A
$FE00.0312_{16}$ .. $FE00.0340_{16}$	Board status and capability registers (BSCRs)
$FE000348_{16}$	DRAM and cache configuration register DCCR B
$FE00.03F8_{16}$ .. $FE00.03FF_{16}$	Serial I/O port #1

Note: The following address map is a default address map which can be changed by the user.

Table 27: *PCI I/O Devices Seen from CPU*

(Base) Address	Device
$FE870000_{16}$	Ethernet controller #1
$FE880000_{16}$	Ethernet controller #2
$FE890000_{16}$	PCI-to-PCI bridge (in either non-transparent mode or transparent mode)
User defined	PMC #1
User defined	PMC #2
$FEC0.0000_{16}$ .. $FEDF.FFFF_{16}$	PCI configuration address register
$FEE0.0000_{16}$ .. $FEEF.FFFF_{16}$	PCI configuration data register
$FEF0.0000_{16}$ .. $FEFF.FFFF_{16}$	PCI interrupt acknowledge register

Interrupt Map

The PCI-to-ISA bridge monitors all PPC / PowerCoreCPCI-680 interrupt requests (IRQs):

- Interrupt requests of all four PCI bus interrupt levels
- Interrupt requests from on-board ISA bus devices, e.g. from the serial controller
- Optional interrupt requests (see Figure 6 “PN15 Connector Pinout” page 3-9)
- CompactPCI related interrupt requests (see SW3-1 and SW3-2 in Table 4 “Switch Settings” page 2-5)

The PCI-to-ISA bridge provides an ISA-compatible interrupt controller that incorporates the functionality of two interrupt controllers. The two controllers are cascaded so that 13 chip external and three chip internal interrupts are possible. For information on programming the interrupt controller, see “Interrupt Controller” page 5-29.

Every interrupt source can be enabled and disabled to interrupt the CPU. The PCI-to-ISA bridge supplies the interrupt vectors for all interrupts except the non-maskable interrupt (NMI).
The NMI is routed from the IOCHK interrupt via the PPC-to-PCI bridge to the MCP# signal at the PowerPC CPU. The NMI has the highest priority and is a non-vectored processor exception.
The following table shows the default mapping of the interrupts and their interrupt priority. Interrupt priority level 0 is the highest priority, level 15 is the lowest priority. The mapping of the interrupts and the interrupt priority can also be set by the user.

Table 28: *Interrupt Map*

Function	Device	PCI-to-ISA Bridge IRQ	Interrupt Priority[1)]
Watchdog timer / abort key / SERR#	Dedicated logic (hardware mapped)	IOCHK (MCP#), NMI	0 (highest)
Timer 1 / counter 0[2)]	PCI-to-ISA bridge	IRQ0	1
Reserved for future use[3)]	Dedicated logic, ISA connector PN15 of PMC #1	IRQ1	2
Cascade[2)]	PCI-to-ISA bridge	IRQ2	–
Serial port #2	Serial port #2	IRQ3	11

Table 28: *Interrupt Map (cont.)*

Function	Device	PCI-to-ISA Bridge IRQ	Interrupt Priority[1)]
Serial port #1	Serial port #1	IRQ4	12
Configurable[3)4)]	ISA connector PN15 of PMC #1	IRQ5	13
CompactPCI signals FAL# and DEG#[3)]	Dedicated logic (see SW3-1 and SW3-2 in Table 4 “Switch Settings” page 2-5), ISA connector PN15 of PMC #1	IRQ6	14
DMA-controller, message unit (I_2O), I^2C interface	MPC107 PPC-to-PCI bridge	IRQ7	15 (lowest)
Watchdog timer (optional routing)	Dedicated logic (see SW4-4 in Table 4 “Switch Settings” page 2-5)	IRQ8#	3
Configurable[4)]	Not connected externally	IRQ9	4
Configurable[4)]	Not connected externally	IRQ10	5
Configurable[4)]	Not connected externally	IRQ11	6
Configurable[3)4)]	ISA connector PN15 of PMC #1	IRQ12	7
Timer / CIO ports	CIO	IRQ13	8
CompactPCI signal IDE-INTP or optionally CompactFlash IDE-INT[5)]	Legacy support for primary IDE interface (CompactPCI) or optionally CompactFlash interrupt	IRQ14	9
CompactPCI signal IDE-INTS	Legacy support for secondary IDE interface (CompactPCI)	IRQ15	10

1. Interrupt priority level 0 is the highest priority, level 15 is the lowest priority.
2. The mapping of this IRQ is pre-defined at the interrupt controller.
3. Can be used by ISA devices on PMC1 (if PN15 is assembled)
4. The configurable interrupts can be used for the PCI interrupt signals INTA#, INTB#, INTC# and INTD# (the mapping of PCI interrupts to IRQs is programmable in the interrupt controller).
5. Is connected to CompactFlash interrupt output if CompactFlash slot is assembled.

The following table shows the interrupt routing of the PCI devices and PMC slots. The connection is marked by “x”.

Table 29: *Interrupt Routing of the Local PCI Bus*

PCI Device/PMC Slot	Interrupt	PCI-to-ISA Bridge (Interrupt Controller)			
		INTA#	INTB#	INTC#	INTD#
Universal PCI-to-PCI bridge SENTINEL	INTA#	x	-	-	-
	INTB#	-	x	-	-
	INTC#	-	-	x	-
	INTD#	-	-	-	x
Ethernet controller #1	INTA#	-	x	-	-
Ethernet controller #2	INTA#	x	-	-	-
PMC slot #1	INTA#	-	-	x	-
	INTB#	-	-	-	x
	INTC#	x	-	-	-
	INTD#	-	x	-	-
PMC slot #2	INTA#	-	-	-	x
	INTB#	x	-	-	-
	INTC#	-	x	-	-
	INTD#	-	-	x	-

Registers

Note: Always remember the following access rule for any reserved bits in any PPC/PowerCoreCPCI-680 register: written as 0, read as undefined. All registers must be written or read using the data path width documented for the respective register.

DRAM and Cache Configuration Registers - DCCR A and DCCR B

The DRAM and cache configuration registers (DCCRs) are used to store the available size of the L2 cache, the frequency of the memory bus and the PPC bus, and the available size and type of the on-board memory. Beyond this the status of the boot device selection switch SW1-1 and the general purpose switch SW1-4 can be read via a DCCR

Table 30: *DCCR A*

Address Offset: $FE000308_{16}$			
Bit	**Value**	**Description**	**Access**
3..0	ONBOARD_MEM [3..0]	Indicates configuration set number of on-board memory bank 0_{16}: Reserved 1_{16}: 64 MByte, CAS latency 3 at 100 MHz 2_{16}: 128 MByte, CAS latency 3 at 100 MHz 3_{16}: 256 MByte, CAS latency 3 at 100 MHz $4...F_{16}$: Reserved	r
4	BOOT-XCHG-SW	Indicates whether board booted out of flash 1 or 2 (set by switch SW1-1) 0_2: Board booted out of boot flash 2. 1_2: Board booted out of boot flash 1 (default)	r
5	GP-SW	Indicates status of general purpose switch SW1-4 0_2: General purpose switch ON 1_2: General purpose switch OFF	r
7..6	L2_SIZE	Indicates L2 cache size 00_2: 2 MByte 01_2: Reserved 10_2: 1 MByte 11_2: 512 KByte	r

Table 31: *DCCR B*

Address Offset: $FE000348_{16}$			
Bit	**Value**	**Description**	**Access**
1..0	MODULE_CODE [1..0]	Indicates type of installed memory module(s) 00_2: PPC/PowerCoreSMEM/256L-100 lower and PPC/PowerCoreSMEM/512U-100 upper modules installed 01_2: PPC/PowerCoreSMEM/256L-100 lower module installed 10_2: Reserved 11_2: No memory module is installed (only on-board memory available)	r
2	REGMODE	Always set to 1	r
3	FASTBUS	Always set to 1	r
5..4	SLOW-BUS-FREQ [1..0]	Not used.	r
7..6	FAST-BUSFREQ [1..0]	If value is 1, it indicates front-side bus frequency (memory bus and PPC bus) 00_2: Reserved 01_2: 99 MHz 10_2: 82.5 MHz 11_2: 66 MHz	r

CIO Ports

The ports A, B, and C of the CIO counter/timer and parallel I/O element are used for local control such as LED control, watchdog control and reading the board configuration.

Table 32: *CIO Port A Data Register*

Address Offset: $FE000302_{16}$			
Bit	**Value**	**Description**	**Access**
0	TM_PRSNT	Indicates whether a rear transition board is connected. 0: Rear transition board present 1: Rear transition board not present	r
1	PROBE_TM	Must be set to 1 to ensure proper detection of rear transition board	r/w

Table 32: *CIO Port A Data Register*

Address Offset: $FE000302_{16}$			
Bit	**Value**	**Description**	**Access**
2	FLU_BANK	Selects area of user flash to be paged into user flash address range 0: Lower 8 MByte paged into user flash address range 1: Upper 8 MByte paged into user flash address range	r / w
3	USER_FL_2MB	Indicates type of user flash devices 0: 4MByte (32Mbit) devices assembled (for the device type, see “User Flash” page 5-13) 1: 2MByte (16Mbit) devices assembled (for the device type, see “User Flash” page 5-13)	r
4	L2_SPEED	Indicates maximum frequency of L2 cache memory devices 0: Slow cache memory devices (133 MHz if 1 MByte L2 cache memory assembled, 150 MHz if 2 MByte L2 cache memory assembled) 1: Fast cache memory devices (200MHz)	r
5	CF_PRSNT_N	Indicates whether a CompactFlash card is fully inserted into the optional CompactFlash slot. 0: CompactFlash card inserted 1: CompactFlash card not inserted	r
6	Reserved	-	-
7	ENA_WD	Starts watchdog timers 1 and 2 0: Watchdog timers 1 and 2 are started if low level is held for more than 8 ms 1: No change	r / w

Table 33: *CIO Port B Data Register*

Address Offset: FE000301$_{16}$			
Bit	**Value**	**Description**	**Access**
0	ISA_IDENT	Indicates whether ISA devices are installed at connector PN15 0: ISA devices installed 1: No ISA devices installed	r
2..1	BUSMODE [1..0]	PMC cards indicate their presence to the given protocol (e.g. PCI protocol, SBus protocol) by the message “Card present”. BUSMODE[1] is connected to PMC slot 2, BUSMODE[0] to PMC slot 1. 0: Card present 1: CArd not present	r
5..3	BUSMODE [4..2]	Indicates meaning of the three output signals routed to both PMC slots. 000_2: Card Present Test: The cards at PMC slots 1 and 2 return “Card Present” if they are plugged into the slot and no bus protocol is used. 001_2: Card Present Test: The cards at PMC slots 1 and 2 return “Card Present” if they are PCI capable and PCI protocol is used (default). 010_2: Card Present Test: The cards at PMC slots 1 and 2 return “Card Present” if they are SBus capable and SBus protocol is used. 011_2: Reserved 100_2: Reserved 101_2: Reserved 110_2: Reserved 111_2: No host present	r / w
6	ID_SDA	Controls and indicates status of ID_ROM serial data signal (I^2C bus)	r / w
7	ID_SCL	Controls ID-ROM SCL signal (I^2C bus)	w

Table 34: *CIO Port C Data Register*

Address Offset: $FE000300_{16}$			
Bit	**Value**	**Description**	**Access**
1..0	LED_1 [1..0]	Control user LED 1 at front panel 00_2: User LED 1 OFF 01_2: User LED 1 green 10_2: User LED 1 red 11_2: User LED 1 used for reset / power (hardware mode, default setting)	r / w
3..2	LED_2 [1..0]	Control user LED 2 at front panel 00_2: User LED 2 OFF 01_2: User LED 2 green 10_2: User LED 2 red 11_2: User LED 2 used for Ethernet read / write (hardware mode, default setting)	r / w
7..4	-	Used as masking bits for write accesses to bit 3..0 (e.g., if bit 4 is 1, bit 0 cannot be written)	r / w

Board Status and Capability Registers - BSCRs

The BSCRs indicate the current status of the board and include features for generating software-requested reset conditions.

Table 35: *BSCR Watchdog Timer 1 Sanity Check Register*

Address Offset: $FE000312_{16}$			
Bit	**Value**	**Description**	**Access**
7..0	WD1_SANITY [7..0]	Correspond to the part of the performed sanity check. To retrigger the watchdog timer 1 two write accesses are required. 55_{16}: First part of sanity check is performed. AA_{16}: Second part of sanity check is performed. All others: No effect	w

Table 36: *BSCR Watchdog Timer 2 Sanity Check Register*

Address Offset: $FE000316_{16}$			
Bit	**Value**	**Description**	**Access**
7..0	WD2_SANITY [7..0]	Correspond to the part of the performed sanity check. To retrigger the watchdog timer 2 two write accesses are required. 55_{16}: First part of sanity check is performed. AA_{16}: Second part of sanity check is performed. All others: No effect	w

Table 37: *BSCR Watchdog Control and Status Register*

Address Offset: $FE000320_{16}$			
Bit	**Value**	**Description**	**Access**
0	WD1_ENABLE	Indicates whether watchdog timer 1 is enabled 0: Watchdog timer 1 disabled 1: Watchdog timer 1 enabled	r
1	WD2_ENABLE	Indicates whether watchdog timer 2 is enabled 0: Watchdog timer 2 disabled 1: Watchdog timer 2 enabled	r
2	WD_TIMEOUT	Indicates period of time after which watchdog timers 1 and 2 expire (set by SW4-3). When the selected time has expired, a reset of the board and an NMI respectively, will be generated. 0: Watchdog timer 1 expires after ~2,5 s and watchdog timer 2 expires after ~500 ms. 1: Watchdog timer 1 expires after ~0,5 s and watchdog timer 2 expires after ~ 32 ms.	r
3	WD2_ROUTING	Indicates interrupt type generated by watchdog timer 2 (set by SW4-4). 0: Watchdog timer 2 generates high-level interrupt 1: Watchdog timer 2 generates NMI	r
4	WD_STARTED	Indicates whether watchdog timers 1 and 2 have been started 0: Watchdog timers 1 and 2 have not been started. 1: Watchdog timers 1 and 2 have been started.	r

Table 37: *BSCR Watchdog Control and Status Register (cont.)*

Address Offset: $FE000320_{16}$			
Bit	**Value**	**Description**	**Access**
5	Reserved	-	-
6	WD2_STATUS	Indicates an interrupt (NMI or high level) generated by watchdog timer 2 time-out. 0: Interrupt not pending 1: Interrupt pending	r
7	WD2_ACK	Control bit to clear interrupt (NMI or high level) generated by watchdog timer 2 time-out. 0: Interrupt will not be acknowledged 1: Interrupt will be acknowledged	w

In the last reset register only one bit is set at time. This bit indicates the last reset source. The bits have different priorities: If more than one reset source is active, bit 0 has the highest, bit 7 the lowest priority.

Note: Only the reset sources described in the following are indicated by the last reset register. If the reset is generated by another source, the last reset register does not indicate this source and keeps its current value.

Table 38: *BSCR Last Reset Register*

Address Offset: $FE000324_{16}$			
Bit	**Value**	**Description**	**Access**
0	POWER_UP	Indicates whether the last reset has been generated via a power-up of the board. 0: Last reset has not been generated by powering up the board. 1: Last reset has been generated by powering up the board.	r
1	RST_KEY	Indicates whether the last reset has been generated via the front-panel reset key. 0: Last reset has not been generated via front-panel reset key. 1: Last reset has been generated via front-panel reset key.	r

Table 38: *BSCR Last Reset Register (cont.)*

Address Offset: FE000324$_{16}$			
Bit	**Value**	**Description**	**Access**
2	PBRST	Indicates whether the last reset has been generated by the CompactPCI push-button reset input. 0: Last reset has not been generated via CompactPCI push-button reset input. 1: Last reset has been generated via CompactPCI push-button reset input.	r
3	CPCI_RST	Indicates whether the last reset has been generated by the CompactPCI reset input. 0: Last reset has not been generated via CompactPCI reset input. 1: Last reset has been generated via CompactPCI reset input.	r
4	WD_EXPIRED	Indicates whether the last reset has been generated due to the expired time-out period of the watchdog timer 1. 0: Last reset has not been caused by the expired time-out of watchdog timer 1. 1: Last reset has been generated due to the expired time-out of watchdog timer 1.	r
5	HARDRST_REQ	Indicates whether the last reset has been generated via a hard reset request to the reset request register (see Table 39 “BSCR Reset Request Register” page 8-19). 0: Last reset has not been generated by software via hard reset request. 1: Last reset has been generated by software via hard reset request.	r
6	SOFTRST_REQ	Indicates whether the last reset has been generated via a soft reset request to the reset request register (see Table 39 “BSCR Reset Request Register” page 8-19) 0: Last reset has not been generated by software via soft reset request. 1: Last reset has been generated by software via soft reset request.	r
7	Reserved	-	-

Table 39: *BSCR Reset Request Register*

Address Offset: FE000332$_{16}$			
Bit	**Value**	**Description**	**Access**
7..0	RSR_REQ [7..0]	Correspond to the kind of reset requested by the software. 11_{16}: Hard reset of the board is requested. 22_{16}: Soft reset of the processor is requested. All others: Reserved	w

Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

☞ Send this report to the nearest Force Computers headquarter listed on the back of the title page.