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SPARC/CPU-54

Reference Guide

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Using This Guide

This Reference Guide is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), VMEbus, and telecommunications.

Conventions

Notation	Description
1234	All numbers are decimal numbers except when used with the notations described below
00000000_{16}	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets
0000_2	Same for binary numbers (digits are 0 and 1)
x	Generic use of a letter
n	Generic use of numbers
n.nn	Decimal point indicator is signaled
Bold	Character format used to emphasize a word
`Courier`	Character format used for on-screen output
`Courier+Bold`	Character format used to characterize user input
Italics	Character format for references, table, and figure descriptions
<text>	Typical notation used for variables and keys
[text]	Typical notation for optional parameters
...	Repeated item
..	Ranges
Note:	No danger encountered. Pay attention to important information marked using this layout
Caution 	Possibly dangerous situation: slight injuries to people or damage to objects possible

Revision History

Order No.	Revision	Date	Description
212466	AA	February 2001	Preliminary Installation Guide
21466	AB	May 2001	Corrected "Expansion" page -xxi; Removed interfaces section in chapter 1; Removed block diagram of I/O board, information on I/O-board installation, connector pinouts of I/O-board and created separate Installation Guide for I/O-board; Corrected Eth 1 and Eth 2 in Figure 1 "Function Blocks" page 1-3; Removed table "Interfaces on the CPU Board" on page 1-4; Corrected Figure 2 "Block Diagram of the CPU Board" page 1-5; Corrected power consumption of SMEM board in Table 7 "SPARC/CPU-54 Maximum Power Consumption" page 2-6; Added "Software Requirements" page 2-7; Corrected safety note in "SPARC/IOBP-54" page 2-9; Corrected switch settings of SW4-1, SW4-2, SW5-2, and SW5-4 in Table 10 "Switch Settings" page 2-11; Added "Solaris Driver Package" page 2-10; Corrected boot flash writing information in "Booting" page 2-16; Corrected "Installing Solaris" page 2-17; Corrected "Setting the SCSI Termination" page 2-22; Corrected Figure 6 "SCSI Termination Concept of SPARC/CPU-54 and IOBP-54" page 2-24; Corrected pinout of Figure 11 "26-Pin Serial A+B Connector Pinout RS422" page 3-8;

Order No.	Revision	Date	Description
212466	AB	May 2001	Corrected pinout 19 and 62 in Figure 14 “68-Pin Ultra-Wide SCSI Connector Pinout” page 3-10; Corrected Table 18 “On-Board Connectors” page 3-11 and Table 19 “P2 Backplane Connector Signals” page 3-11; Corrected pinout row Z in Figure 15 “P2 VMEbus Connector Pinout Rows Z-B” page 3-12 and row D in Figure 16 “P2 VMEbus Connector Pinout Continued Rows C+D” page 3-13; Corrected “CORE” page 4-3; Corrected introduction to CORE commands in “CORE Commands” page 4-6; Corrected screen shot in “Boot Devices” page 4-7; Added “POST” page 4-6; Added the “OBDIAG” page 4-10; Corrected “Diagnostics” page 4-15; Editorial changes
212466	AC	June 2001	Corrected SW4-3 and SW4-4 in Table 10 “Switch Settings” page 2-11;
212466	AD	July 2001	Added information on VxWorks in “VxWorks Support” page 4-13; Added information on PCI Control Register on page 4-18;
212466	AE	August 2001	Added the “Sicherheitshinweise” chapter
212466	AF	September 2001	Revised “Safety Notes” page xix and “Sicherheitshinweise” page xxiii; Added information on the execution of the CORE firmware in “POST” page 4-6;

Order No.	Revision	Date	Description
216116	AA	June 2002	Modified "Safety Notes" page xxi and "Sicherheitshinweise" page xxv; modified Figure 2 "Block Diagram of the CPU Board" page 1-5; replaced EN 50081/2 with EN 55022/4 in Table 1 "Standard Compliance" page 1-8; modified and updated section "Ordering Information" page 1-9; removed table "Qualified Memory Modules" and accompanying safety note in section "Memory Modules" page 2-8; modified section "Setting the SCSI Termination" page 2-10; corrected description of switch SW5-4 in Figure 5 "SCSI Termination Concept of SPARC/CPU-54 and IOBP-54" page 2-11; modified description of switches 4-3, 4-4, 5-4, 7-1 and 7-2 in Table 9 "Switch Settings" page 2-13; added Figure 7 "Location of Switches on Board's Bottom Side" page 2-13; modified sections "Boot Devices OTP PROM and Flash EPROM" page 2-18 and "User Application" page 2-18; added information on problem with VMEbus read errors and Solaris 8 version 4/01 to "Installing Solaris" page 2-19 and the "Troubleshooting" chapter; moved section "Battery Exchange" to Appendix B; changed Table 15 "Flash Segmentation and Write Protection" page 2-23; added description of Ethernet LEDs in Table 16 "Description of Front Panel LEDs" page 3-4; modified section "Serial I/O" page 3-7; deleted section "PCI Control Register"; modified section "OBDIAG" page 4-10; added chapter "Maps and Registers" page 5-1 from Reference Guide with following modifications: corrected description of signal ID[3..0] in "System Configuration Identification Register" page 5-14; modified description of the Serial Protocol Status register page 5-16; changed description of bits 0-4 in Table 42 "Switch 4 and 5 Status Register" page 5-17; modified description of the RS-422 Control and Status register page 5-21
220063	AA	January 2003	Changed document type to "Reference Guide"; added note on EN 55022 non-compliance to sections "EMC" page xxi, "EMV" page xxv, "Standard Compliance" page 1-8, and "SCSI" page 3-9

Order No.	Revision	Date	Description
220991	AA	May 2003	Corrected pinout of RS-422 interface Added information on termination when using RS-422 interfaces

Other Sources of Information

For further information refer to the following documents:

Company	www.	Document
Force Computers	forcecomputers.com	SPARC / CPU-54 OpenBoot Enhancements Programmer's Guide (P / N 216134)[1)]
		SPARC / IO-54 Installation Guide (P / N 214901)
		SPARC / IOBP-54 Installation Guide (P / N 213170)
		SPARC / MEM-54 Installation Guide (P / N 214000)
IEEE Standards Department	ieee.com	IEEE P1386 Standard Mechanics for a Common Mezzanine Card Family: CMC
National Semiconductor	national.com	PC87307 / PC97307 Plug and Play Compatible Super I / O, Preliminary Specification, March 1998
PCI Special Interest Group	pcisig.com	PCI Local Bus Specification Rev2.1
PICMG PCI Special Interest Group	picmg.org pcisig.com	PCI Local Bus Specification Rev2.2
SUN Microsystems	sun.com	UltraSPARC-IIE, Draft Datasheet, Aug 25 1999
		PCIO (Cheerio, STP2003) Preliminary Datasheet, March 1997
		Cheerio Specification, May 1996
Tundra	tundra.com	Universe II User's Guide 1997
		Universe II Manual Addendum, Rev2, Jun 21, 1999
VITA	vita.com	VME64 Standard ANSI / VITA 1-1994
VITA	vita.com	VME64 Extensions Draft Standard, Draft 1.8, Jun 13, 1997

1) Only available via SMART. If you do not have a S.M.A.R.T. account, you can download the PDF file via a Public S.M.A.R.T. Access Account from Force Compters Internet Site. To get an account, click on the blue button labeled "log on S.M.A.R.T." and sign up by entering the form.



Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the SPARC/CPU-54.

We intend to provide all necessary information to install and handle the SPARC/CPU-54 in this Reference Guide. However, as the product is complex and its usage manifold, we do not guarantee that the given information is complete. If you need additional information, ask your Force Computers representative.

The SPARC/CPU-54 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or persons qualified in electronics or electrical engineering are authorized to install, maintain, and operate the SPARC/CPU-54. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

EMC

The board has been tested in a standard Force Computers system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial, business or industrial environment.

Note: The board is not compliant to EN 55022 if you connect a SCSI device to the SCSI connector on the front panel.

The board generates and uses radio frequency energy and, if not installed properly and used in accordance with this Reference Guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

If you use the board without a PMC module, cover empty slots with blind panels to ensure proper EMC shielding. If boards are integrated into open systems, always cover empty slots.



Installation

Electrostatic discharge and incorrect board installation and removal can damage circuits or shorten their life. Therefore:

- **Before installing or removing the board, read the “Action Plan” section page 2-3.**
- **Before touching boards or electronic components, make sure that you are working in an ESD-safe environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or removing an additional device or module, read the respective documentation.**
- **Make sure that the board is connected to the VME backplane via all assembled connectors and that power is available on all power pins.**

Power Up

If an unformatted floppy disk resides in a floppy drive connected to the SPARC/CPU-54 during power up, the SPARC/CPU-54 does not boot and the OpenBoot prompt does not appear. Therefore, never boot the SPARC/CPU-54 with an unformatted floppy disk residing in a floppy drive connected to the SPARC/CPU-54.

Operation

While operating the board ensure that the environmental and power requirements are met.

Do not operate the SPARC/CPU-54 outside the specified environmental limits. High humidity and condensation may cause short circuits. Make sure the product is completely dry and there is no moisture on any surface before applying power. Do not operate the product below 0°C.

When operating the board in areas of electromagnetic radiation ensure that the board is bolted on the VME system and the system is shielded by enclosure.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

The switch settings have to be checked and changed before the board installation. Do not set/reset the switches during operation. Otherwise, the board is damaged.



Replacement/Expansion

Only replace or expand components or system parts with those recommended by Force Computers. Otherwise, you are fully responsible for the impact on EMC and the possibly changed functionality of the product.

Check the total power consumption of all components installed (see the technical specification of the respective components). Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

System Controller

If more than one system controller is active in the VMEbus system, the board or other VMEbus participants can be damaged. Therefore, always ensure that only one CPU board is configured as system controller in the VMEbus system.

RJ-45 Connector

An RJ-45 connector is used for both telephone and twisted pair Ethernet (TPE) connectors. Mismatching the two connectors may destroy your telephone as well as your SPARC/CPU-54. Therefore:

- **TPE connectors have to be clearly marked as network connectors.**
- **The TPE bushing of the system has to be connected only to safety extra low voltages (SELV) circuits.**
- **The total length of the electric cable connected to a TPE bushing must not exceed 100 meters.**



Battery

If a lithium battery on the board has to be exchanged, observe the following safety notes:

- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, backup affected data before exchanging the battery.**
- **Incorrect exchange of lithium batteries can result in a hazardous explosion.**
- **Exchange the battery before seven years of actual battery use have elapsed.**
- **Always use the same type of lithium battery as is already installed.**
- **Use appropriate tools to remove the battery.**
- **When installing the new battery, ensure that the dot marked on top of the battery covers the dot marked on the chip.**

Environment

Always dispose of old boards according to your country's legislation, if possible in an environmentally acceptable way.



Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Einbau, Betrieb und Wartung des SPARC/CPU-54 zu beachten sind.

Wir sind darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem SPARC/CPU-54 in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem SPARC/CPU-54 um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Ihnen Informationen fehlen sollten, wenden Sie sich bitte an Ihren Vertreter von Force Computers.

Das SPARC/CPU-54 erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Force Computers ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

EMV

Das Board wurde in einem Force Computers Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Boards in Geschäfts-, Gewerbe- sowie Industriebereichen gewährleisten.

Anmerkung: Das Board erfüllt den Standard EN 55022 nicht, wenn Sie ein SCSI-Gerät am SCSI-Stecker der Frontblende anschließen.

Das Board arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten. Wird das Board in Wohngegenden betrieben, ist der Benutzer verpflichtet, entstehende Störungen auf seine Kosten beheben zu lassen.



Wenn Sie das Board ohne ein PMC Modul verwenden, schirmen Sie freie Steckplätze mit einer Blende ab, um einen ausreichenden EMV Schutz zu gewährleisten. Wenn Sie Boards in Systeme einbauen, schirmen Sie freie Steckplätze mit einer Blende ab.

Installation

Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Beachten Sie deshalb die folgenden Punkte:

- **Bevor Sie Boards oder elektronische Komponenten berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Lesen Sie vor Ein- oder Ausbau des Boards den Abschnitt “Action Plan” auf Seite 2-3.**
- **Drücken Sie bei Ein- oder Ausbau des Boards nicht auf die Frontblende, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor dem Ein- oder Ausbau von zusätzlichen Geräten oder Modulen das dazugehörige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über alle Stecker an die VME Backplane angeschlossen ist und alle Spannungskontakte mit Strom versorgt werden.**

Booten

Befindet sich während des Bootens eine unformatierte Diskette in einem mit dem SPARC/CPU-54 verbundenen Diskettenlaufwerk, bootet das SPARC/CPU-54 nicht, und die OpenBoot-Eingabeaufforderung erscheint nicht. Booten Sie deshalb niemals das SPARC/CPU-54, wenn sich eine unformatierte Diskette in einem mit dem SPARC/CPU-54 verbundenen Diskettenlaufwerk befindet.



Betrieb

Achten Sie darauf, dass die Umgebungs- und die Leistungsanforderungen während des Betriebs eingehalten werden.

Betreiben Sie das SPARC/CPU-54 nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur, da durch hohe Luftfeuchtigkeit und Kondensation Kurzschlüsse entstehen können. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem SPARC/CPU-54 kein Kondensat befindet, und betreiben Sie das SPARC/CPU-54 nicht unter 0°C.

Wenn Sie das Board in Gebieten mit elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Board mit dem VME System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Stellen Sie sicher, dass Anschlüsse und Kabel des Boards während des Betriebs nicht berührt werden können.

Prüfen und ändern Sie die Schalterstellungen bevor Sie das Board installieren. Ändern Sie die Stellungen während des Betriebs, kann das Board beschädigt werden.

Austausch/Erweiterung

Verwenden Sie bei Austausch oder Erweiterung ausschließlich von Force Computers empfohlene Komponenten und Systemteile. Andernfalls sind Sie für mögliche Auswirkungen auf EMV und geänderte Funktionalität des Produktes voll verantwortlich.

Überprüfen Sie die gesamte aufgenomme Leistung aller eingebauten Komponenten (siehe die technischen Daten der entsprechenden Komponente). Stellen Sie sicher, dass die Ausgangsströme jedes Verbrauchers innerhalb der zulässigen Grenzwerte liegen (siehe die technischen Daten des entsprechenden Verbrauchers).

System Controller

Bei mehr als einem aktiven System Controller im VMEbus System kann das SPARC/CPU-54 oder andere VMEbus Boards beschädigt werden. Vergewissern Sie sich deshalb, dass nur ein CPU Board im VMEbus System als System Controller konfiguriert ist.



RJ-45 Stecker

Das CPU Board ist mit RJ-45 Steckern ausgestattet. Dieser Stecker wird sowohl für Telefonanschlüsse als auch für Netzwerkkabel (Twisted Pair Ethernet - TPE) verwendet. Die Verwechslung dieser Anschlüsse kann sowohl das Telefon als auch das Board zerstören. Beachten Sie deshalb die folgenden Punkte:

- **Vergewissern Sie sich, dass Anschlüsse deutlich als Netzwerkanschlüsse gekennzeichnet sind.**
- **Schließen Sie TPE-Stecker/Netzwerkstecker Ihres Systems nur an Sicherheitskleinspannungskreise (SELV) an.**
- **Vergewissern Sie sich, dass die an einem TPE-Anschluss angeschlossene Leitung eine Gesamtlänge von 100 Metern nicht überschreitet.**

Falls Sie Fragen haben, wenden Sie sich an Ihren Systemadministrator.

Batterie

Achten Sie beim Austausch der Batterie auf folgende Hinweise:

- **Fehlerhafter Austausch von Lithium-Batterien kann zu lebensgefährlichen Explosionen führen.**
- **Der Austausch der Batterie bringt immer einen Datenverlust bei den batteriegepufferten Komponenten mit sich. Sichern Sie deshalb vor dem Batteriewechsel die betroffenen Daten.**
- **Tauschen Sie die Batterie aus, bevor sieben Jahre reiner Betriebsdauer verstrichen sind.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**
- **Verwenden Sie zum Batteriewechsel geeignetes Werkzeug.**
- **Installieren Sie die Batterie so, dass der Punkt auf der Batterie den Punkt auf dem Chip bedeckt.**

Umweltschutz

Entsorgen Sie alte Boards gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich umweltfreundlich.

1

Introduction

Features

The SPARC / CPU-54 is the successor of the SPARC / CPU-50. It is a single-board computer with a processor frequency of 500 MHz and is designed in the 6U VMEbus form factor. It includes a PCI bus subsystem with 32-bit / 33 MHz. On-board are:

- Hardware monitor for observing board temperature
- OpenBoot diagnostics
- Universe II PCI-to-VMEbus
- PCIO chip with interfaces to the Ebus
- Ethernet “Cheerio” controller
- Program-readable registers for board information block (BIB)
- System configuration registers

The figure shows the major function blocks of the SPARC / CPU-54.

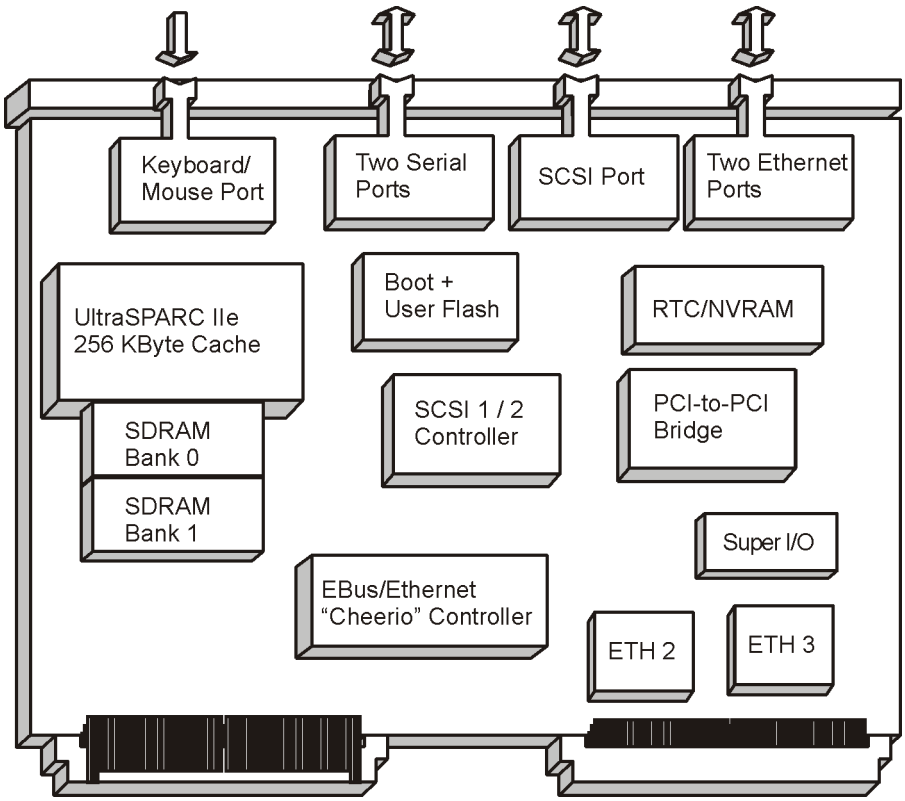


Figure 1: *Function Blocks*

CPU

The UltraSPARC-IIe CPU with 500 MHz has sensors for observing the CPU on-die temperature and provides the following features:

- Four-way superscalar processor
- SPARC V9 Architecture with the VIS instruction set
- 64-bit data path and 44-bit address pointers
- 16 KByte instruction cache
- 16 KByte non-blocking primary data cache
- 256 KByte L2-Cache memory

Memory

Memory features include:

- 128 to 512 MByte on-board SDRAM
- 128 to 1536 MByte SDRAM memory module
- 1 MByte boot PROM
- Internal memory controller support of up to 2 GB SDRAM
- Supports up to 4 MByte user flash

OpenBoot

OpenBoot serves as a boot device and provides the setup for the VME-bus interface. For further details, refer to the “OpenBoot Firmware” section on page 4-1.

Block Diagram

The block diagram shows how the devices of the SPARC/CPU-54 work together and which data paths they use.

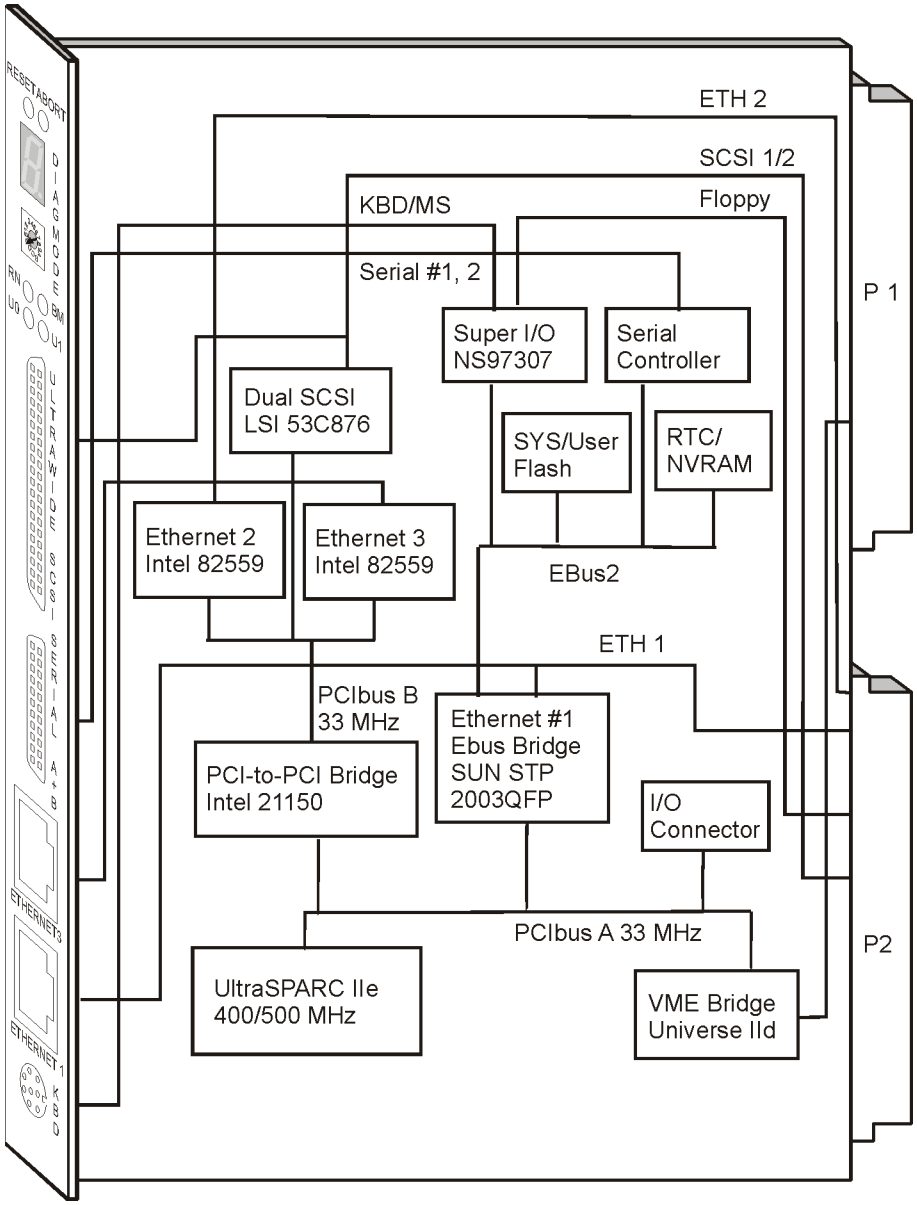


Figure 2: *Block Diagram of the CPU Board*

CPU Board Variants

The SPARC / CPU-54 is available as CPU board and also in combination with the I / O-54. If combined with the I / O-54, the SPARC / CPU-54 is called SPARC / CPU-54T and allows the installation of PMC modules.

SPARC/CPU-54

The SPARC / CPU-54 consists of a single-slot CPU board.

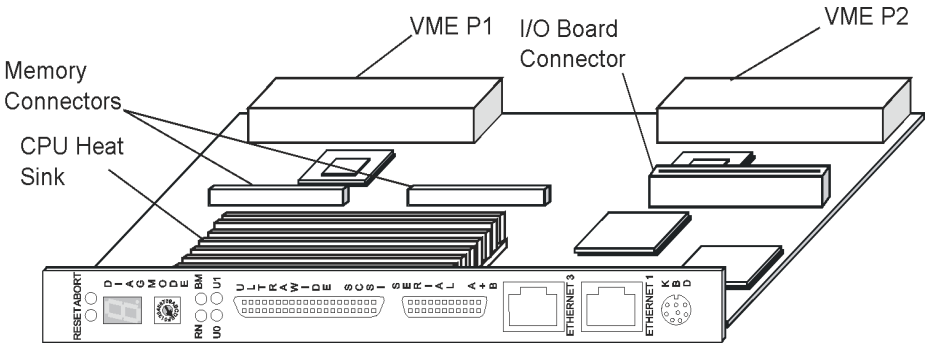


Figure 3: *SPARC/CPU-54*

SPARC/CPU-54T

The SPARC/CPU-54T consists of a single-slot CPU board and a single-slot I/O-54, which allows to mount two PMC modules. For further information on the I/O board, refer to the *IO-54 Installation Guide.*

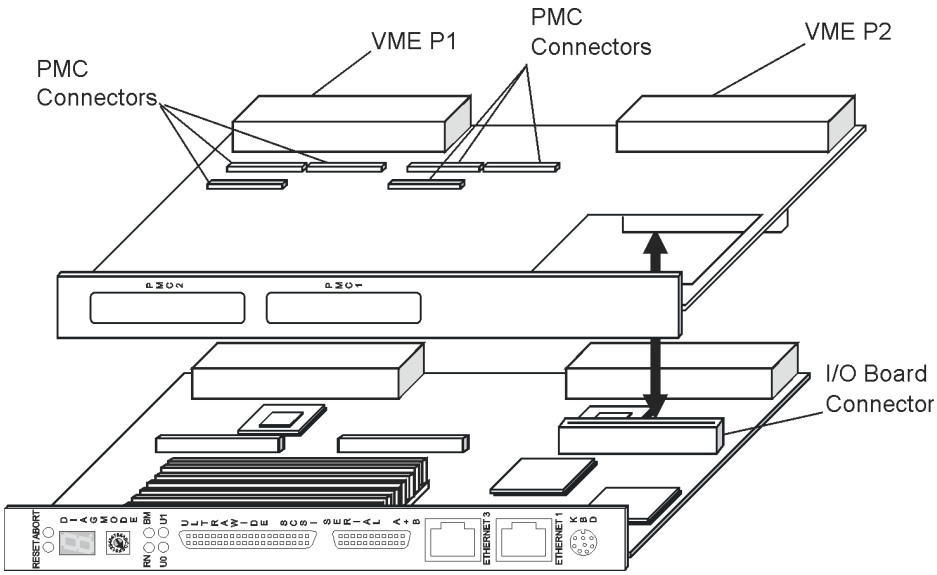


Figure 4: *SPARC/CPU-54T*

Standard Compliance

The CPU board was designed to comply with the standards listed below.

Note: The board is not compliant to EN 55022 if you connect a SCSI device to the SCSI connector on the front panel.

Table 1: *Standard Compliance*

Standard	Description
IEC 68-2-1 / 2 / 3 / 13 / 14	Climatic environmental requirements.The SPARC / CPU-54 can only be used in an restricted temperature range (see Table 6 “Environmental Requirements” on page 2-4) for details.
IEC 68-2-6 / 27 / 32	Mechanical environmental requirements
EN 609 50 / UL 1950 (predefined Force system); UL 94V-0 / 1	Legal safety requirements
EN 55022, EN 55024, FCC Part 15 Class A	EMC requirements on system level
ANSI / IPC_A-610 Rev. C ANSI / IPC-7711 ANSI / IPC-7721 ANSI-J-001...003	Manufacturing requirements
ISO 8601	Y2K compliance

Ordering Information

When ordering board variants, upgrades, and accessories, use the order numbers given below.

Product Nomenclature

In the following table you find the key for the product name extensions.

Table 2: *Product Nomenclature*

SPARC/CPU-54(T)/mmm-sss-c-uu	
mmm	SDRAM capacity in MByte
sss	CPU speed in MHz
c	L2-cache
uu	User flash EPROM size in MByte

Order Numbers

The table below is an excerpt from the board's ordering information. Ask your local Force Computers representative for the current SPARC/CPU-54 ordering information.

Table 3: *Excerpt from the SPARC/CPU-54 Ordering Information for CPU Boards*[1)]

Order No.	SPARC/CPU-54...	Description
110540	.../128-500-1-4/R2	128 MByte CPU board memory (2 banks, 64 MBit devices); 500 MHz CPU with 256 KByte Cache; 4 MByte user flash
110541	.../512-500-1-4/R2	512 MByte CPU board memory (2 banks, 256 MBit devices); 500 MHz CPU with 256 KByte Cache; 4 MByte user flash
110542	...T/128-500-1-4/R2	128 MByte CPU board memory (2 banks, 256 MBit devices); 500 MHz CPU with 256 KByte cache; 4 MByte user flash and I/O-54 (two PMC slots)
110543	...T/512-500-1-4/R2	512 MByte CPU board memory (2 banks, 256 MBit devices); 500 MHz CPU with 256 KByte cache; 4 MByte user flash and I/O-54 (two PMC slots)

1) Status: May 2003

Table 4: *Excerpt from the SPARC/CPU-54 Ordering Information for Memory Modules* [1)]

Order No.	SPARC/...	Description
107463	.../MEM-54/128	128 MByte memory (2 banks, 64 MBit devices)
107464	.../MEM-54/512	512 MByte memory (2 banks, 256 MBit devices)
107465	.../MEM-54/1024	1024 MByte memory (4 banks, 256 MBit devices)
107466	.../MEM-54/1536	1536 MByte memory (6 banks, 256 MBit devices)

1) Status: May 2003

Table 5: *Excerpt from the SPARC/CPU-54 Ordering Information for Accessories* [1)]

Order No.	SPARC/...	Description
108771	IOBP-54/3	3-row I/O panel for the CPU-54 and I/O-54 with 3-row P2 connector pinout
108772	IOBP-54/5	5-row I/O panel for the CPU-54 and I/O-54 with 5-row P2 connector pinout
108773	.../CPU-54/AccKit/3	IOBP-54/3 with cables
108774	.../CPU-54/AccKit/5	IOBP-54/5 with cables
105608	.../Sol/Drv/Rel.2.x	Solaris driver package
107470	Tornado 2.0 BSP for CPU-54	Tornado 2.0 board support package

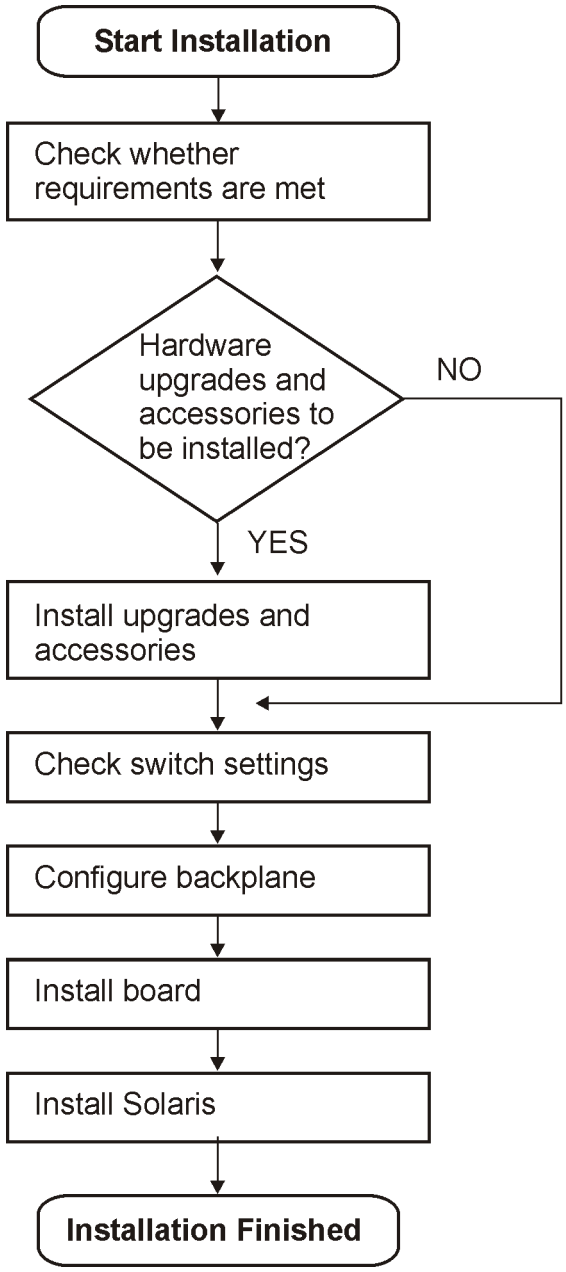
1) Status: May 2003

2

Installation

Action Plan

In order to install the board, the following steps are necessary and will be described in further detail in the sections of this chapter.



Requirements

In order to meet the environmental requirements, the CPU board has to be tested in the system in which it is to be installed.

Before you power up the board, calculate the power needed according to your combination of board upgrades and accessories.

Environmental Requirements

The environmental conditions must be tested and proven in the used system configuration. The conditions refer to the surrounding of the board within the user environment.

Note: Operating temperatures refer to the temperature of the air circulating around the board and not to the actual component temperature.

Caution



- **To ensure that the operating conditions are met, forced air cooling is required within the chassis environment.**
- **Do not operate the SPARC/CPU-54 outside the specified environmental limits. High humidity and condensation may cause short circuits. Make sure the product is completely dry and there is no moisture on any surface before applying power. Do not operate the product below 0°C.**

Table 6: *Environmental Requirements*

Feature	Operating	Non-Operating
Temperature	0°C to +55°C	-40°C to +85°C
Forced airflow	300 LFM (linear feet per minute)	-
Temp. change	+/- 0.5°C/min	+/- 1.0°C/min
Rel. humidity	5% to 95% non-condensating at +40°C	5% to 95% non-condensating at +40°C
Altitude	-300 m to + 3,000 m	-300 m to +13,000 m

Table 6: *Environmental Requirements (cont.)*

Feature	Operating	Non-Operating
Vibration		
10 to 15 Hz	2 mm amplitude	5 mm amplitude
15 to 150 Hz	2 g	5 g
Shock	5g / 11 ms halfsine	15g / 11 ms halfsine
Free fall	100 mm / 3 axes	1200 mm / all edges and corners (packed state)

Power Consumption

The SPARC / CPU-54 power consumption depends on the installed hardware accessories. In the following table you will find typical examples of power consumption without any accessories installed. If you want to install accessories on the SPARC / CPU-54, the load of the respective accessory has to be added to the used SPARC / CPU-54 variant. For information on the accessories' power consumption, refer to the documentation delivered together with the respective accessory or consult your local Force Computers representative for further details.

The installation of the SPARC / CPU-54 requires:

- +5V power supply
- Minimum airflow meeting the thermal requirements (see Table 6 "Environmental Requirements" on page 2-4)
- One slot of a VMEbus backplane with P1 and P2 connectors

The installation of the SPARC / CPU-54T requires:

- +5V and +12V power supply
- Minimum airflow meeting the thermal requirements (see Table 6 "Environmental Requirements" on page 2-4)
- Two slots of a VMEbus backplane with P1 and P2 connectors

The power supply has to meet the requirements given in the tables below.

Table 7: *Maximum Power Consumption*

CPU Board	+5V	+12V	Major Components
SPARC/CPU-54/ 128-400-1-4	4.5A	n.a.	CPU-54 400 MHz, 128 MByte SDRAM
SPARC/CPU-54/ 512-500-1-4	5.0A	n.a.	CPU-54 500 MHz, 512 MByte SDRAM
SPARC/CPU-54T/ 128-400-1-4	6.0A	500mA	CPU-54 400 MHz, 128 MByte SDRAM, including I/O-54
SPARC/CPU-54T/ 512-500-1-4	7.5A	500mA	CPU-54 500 MHz, 512 MByte SDRAM, including I/O-54

Table 8: *Maximum Power Consumption with SPARC/MEM-54 Installed*

MEM Board	+5V	+12V	Major Components
SPARC/MEM-54/128	1A	n.a.	128 MByte, SDRAM
SPARC/MEM-54/1536	1.3A	n.a.	1536 MByte, SDRAM

Caution



In order to protect its components, the SPARC/CPU-54 only powers up if the 5V supply voltage is stable and within its limits. The SPARC/CPU-54T only powers up if the 5V and 12V supply voltages are stable and within their limits. This is in compliance with the VMEbus specification. However, there are systems which are not fully VMEbus-compliant. The power supplies of these systems do not turn on the 12V supply if the 5V supply has not been loaded before. Use a VMEbus board in the system which loads the 5V to prevent such systems from running into a power-up deadlock.

Software Requirements

If you wish to use one of the SPARC/CPU-54 devices listed below you need to install the Force Computers Solaris Driver Package Version 2.11 or higher:

- Intel 82559 Ethernet device
- Universe II PCI-to-VMEbus bridge
- On-board Flash memory
- Temperature sensors, LEDs, seven-segment display, watchdog and floppy ejection

For information on which drivers have to be installed and on the driver package itself, refer to the “Installing Solaris” section on page 2-19 and to the *Solaris Driver Package Installation Guide*.

Hardware and Software Upgrades and Accessories

The following upgrades and accessories are available for the SPARC/CPU-54:

- SPARC/MEM-54 memory module
- IO-54
- IOBP-54
- Solaris Driver Package

Memory Modules

The main memory capacity is adjustable via installation of the Force Computers memory module SPARC/MEM-54. The following memory module variants are available:

- SPARC/MEM-54/128 with 128 MByte additional memory
- SPARC/MEM-54/512 with 512 MByte additional memory
- SPARC/MEM-54/1024 with 1024 MByte additional memory
- SPARC/MEM-54/1536 with 1536 MByte additional memory

For installation information, see the *SPARC/MEM-54 Installation Guide.*

IO-54

The SPARC/CPU-54T includes an I/O board, the SPARC/IO-54, which can be plugged onto the CPU board. The SPARC/IO-54 serves as a carrier board and provides connectors for two PMC modules

Note: The I/O board has to be mounted on the CPU board before the CPU board is installed into the system.

For further information, refer to the *IO-54 Installation Guide.*

SPARC/IOBP-54

As a separate price list item an I/O back panel is available for the CPU board, the SPARC/IOBP-54. It is part of the SPARC/CPU-54/AccKit3/5 Accessory Kit. The SPARC/IOBP-54 provides access to the CPU board's user I/O interfaces via industry standard connectors.

Note: The IOBP has to be connected to the CPU board after it has been installed in the system.

For further information, refer to the *IOBP-54 Installation Guide*.

Caution



- **The SPARC/IOBP-54 is especially designed for the SPARC/CPU-54. Do not use any other I/O back panels on the SPARC/CPU-54. Otherwise, the board may be damaged.**
- **The IOBP-54 provides automatic SCSI termination. Therefore, SW5-2 on the CPU board must be configured appropriately to disable the corresponding backplane SCSI termination.**

Solaris Driver Package

Force Computers provides a Solaris driver package which supports the following devices and features of the SPARC/CPU-54:

- Intel 82559 Ethernet device
- Universe II PCI-to-VMEbus bridge
- On-board flash memory
- Temperature sensors, LEDs, seven-segment display, watchdog and floppy ejection

If you wish to use one of these devices you need to install the Force Computers Solaris Driver Package Version 2.11 or higher.

For information on which drivers have to be installed and on the driver package itself, refer to the "Installing Solaris" section on page 2-19 and to the *Solaris Driver Package Installation Guide*.

Setting the SCSI Termination

The SPARC/CPU-54 provides two Ultra Wide SCSI buses. SCSI 1 is accessible via the front panel and the backplane via the IOBP-54. SCSI 2 is available via the backplane via the IOBP-54. The SPARC/CPU-54 enables and disables the SCSI termination automatically according to the board's position in the SCSI bus, if switch SW5 is set to the respective default settings.

SCSI 1 Termination

The SCSI 1 bus is available via the front panel connector and via the VMEbus P2 connector and the IOBP-54. By default, switch SW5-2 is set to OFF and switch SW5-3 is set to ON to enable automatic termination of the SCSI bus 1. To guarantee proper termination, leave switches in the mentioned position.

Caution



Only connect the SCSI cable at its end connectors and never at its middle connectors. Otherwise, data may be lost.

SCSI 2 Termination

Caution



If you use a flat ribbon T-cable at the SCSI 2 bus, the termination of SCSI 2 has to be set manually to prevent data transmission errors. Before installing the board, check Figure 5 "SCSI Termination Concept of SPARC/CPU-54 and IOBP-54" on page 2-11 whether this applies to your planned configuration.

The SCSI 2 bus is only available via the VMEbus P2 connector and can only be terminated manually. The following options apply:

- The SCSI 2 connector on the IOBP is connected to SCSI devices. The switch SW5-4 must be set to the OFF position which enables the termination on the CPU board.
- The SCSI 2 connector on the IOBP is connected to SCSI devices, but a flat ribbon T-cable is used. The switch SW5-4 must be set to the ON position which disables the termination on the CPU board.

The figure below shows the SCSI bus termination concept on the SPARC / CPU-54 and the IOBP-54.

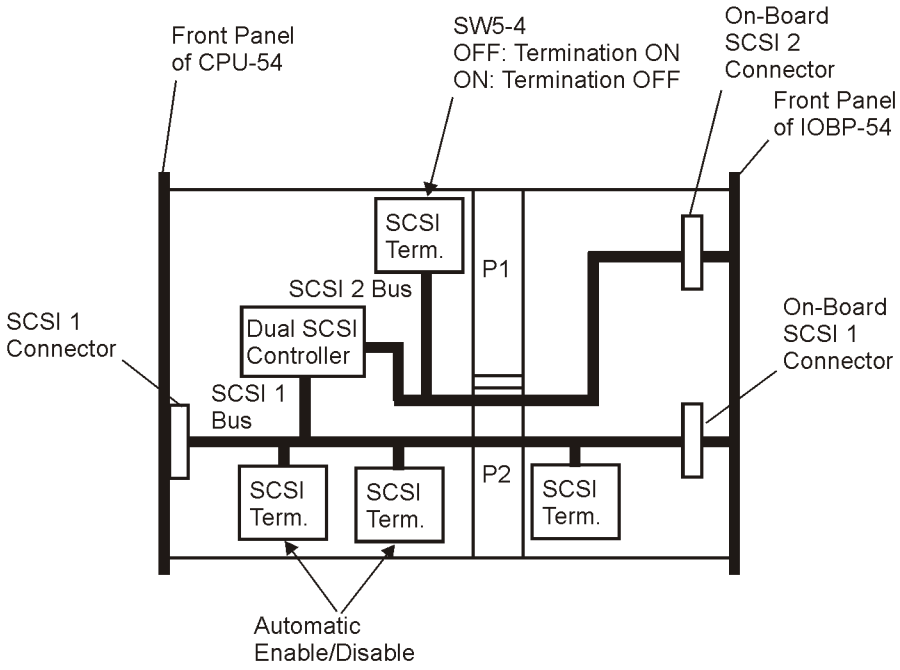


Figure 5: *SCSI Termination Concept of SPARC/CPU-54 and IOBP-54*

Switch Settings

Caution



The switch settings have to be checked and changed before the board installation. Do not set/reset the switches during operation. Otherwise, the board is damaged.

The SPARC/CPU-54 provides five configuration switches: SW4, SW5, SW6, SW7, and SW800. Switches SW4, SW6 and SW7 are located on the top side (see figure below).

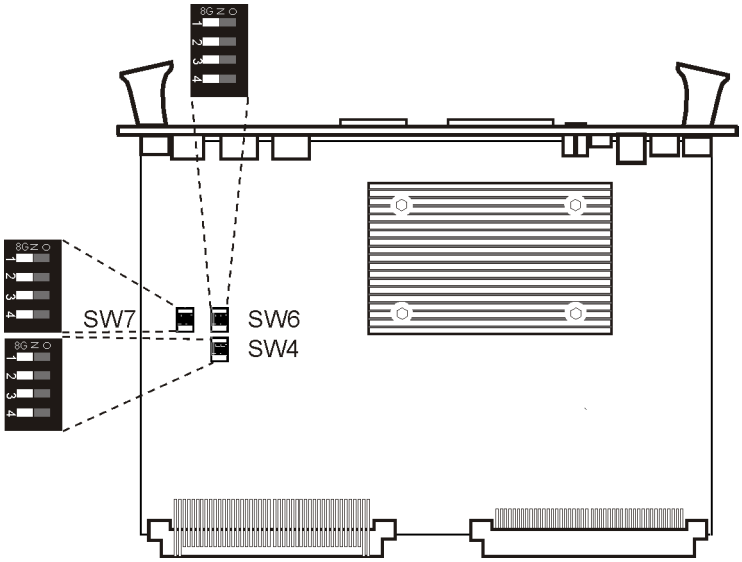


Figure 6: *Location of Switches on Board's Top Side*

The switches SW5 and SW800 are located on the bottom side of the board.

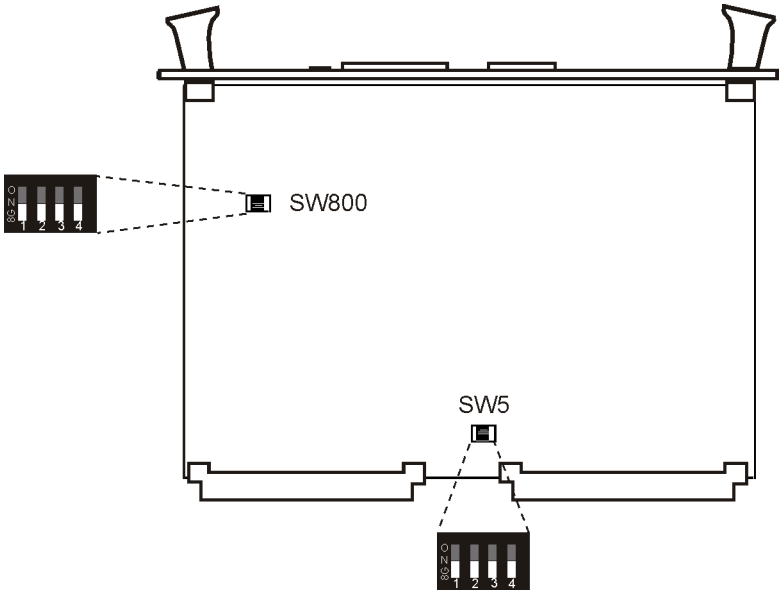


Figure 7: *Location of Switches on Board's Bottom Side*

Table 9: *Switch Settings*

Switch	No.	Description
SW4 	1	Abort key control OFF (default): ABORT key enabled ON: ABORT key disabled
	2	Reset key on front panel control OFF (default): RESET key enabled ON: RESET key disabled
	3	Flash EPROM write protection OFF (default): Flash EPROM write protected ON: Flash EPROM write enabled
	4	Reserved

Table 9: *Switch Settings (cont.)*

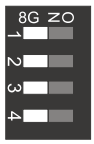
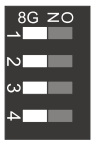
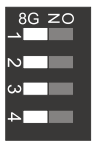
Switch	No.	Description
SW5 	1	Termination for SCSI 1 on front panel OFF (default): Front panel termination automatic ON: Front panel termination disabled
	2	Termination for SCSI 1 on P2 OFF (default): Manual termination enabled ON: Manual termination disabled
	3	Automatic termination for SCSI 1 on P2 OFF: Automatic termination disabled ON (default): Automatic termination enabled
	4	Manual SCSI termination for SCSI 2 on P2 OFF (default): Termination enabled ON: Termination disabled
SW6 	1	**Reserved, must be OFF**
	2	Boot device selection OFF (default): Boot from OTP PROM ON: Boot from flash EPROM
	3	VMEbus SYSRESET on power-up OFF (default): Enabled ON: Disabled
	4	Watchdog enable switch OFF (default): Disabled ON: Enabled
SW7 	1	Serial interface A control selection OFF (default): RS-232 ON: RS-422 (factory option)
	2	Serial interface B control selection OFF (default): RS-232 ON: RS-422 (factory option)
	3	**Reserved, must be OFF**
	4	**Reserved, must be OFF**

Table 9: *Switch Settings (cont.)*

Switch	No.	Description
SW800 	1	Automatic VMEbus slot-1 detection OFF (default): Automatic detection of VMEbus slot-1 function ON: Automatic detection of VMEbus slot-1 function disabled. Set SW800-2 appropriately.
	2	Manual VMEbus slot-1 selection - only relevant if SW800-1 is ON OFF (default): VMEbus slot-1 function enabled ON: VMEbus slot-1 function disabled
	3	External VMEbus SYSRESET OFF (default): VMEbus SYSRESET generates on-board RESET ON: VMEbus SYSRESET does not generate on-board RESET
	4	VMEbus SYSRESET generation OFF (default): SYSRESET is driven to VMEbus ON: SYSRESET is not driven to VMEbus

Board Installation

The SPARC/CPU-54 can be installed in a system with or without the IO-54.

Caution



The SPARC/CPU-54 has to be installed in a non-powered system. If you install the SPARC/CPU-54 in or remove it from a powered system, the system board and other cards installed may be damaged.

Backplane Configuration

If the CPU board is plugged into slot 1 and configured accordingly with switches SW800-1 and SW800-2 (see Table 9 “Switch Settings” on page 2-13), the board acts as IACK daisy-chain driver. Plugged in any other slot, the board closes the IACKIN-IACKOUT path.

If one board is missing in this daisy chain, an active backplane will be able to automatically transfer the signals to the next board in the chain. If the board is not plugged into an active backplane, jumpers on the backplane will transmit the signals. The jumpers have to be set manually. In order to do so, proceed as follows:

1. Remove jumpers connecting BG3IN* and BG3OUT* signals from empty slot on backplane where SPARC/CPU-54 is to be plugged into backplane
2. Assemble jumpers for BG3IN* and BG3OUT* signals on lower and higher slots on backplane where no board is plugged to ensure that daisy chain is not interrupted

If configured appropriately, the SPARC/CPU-54 recognizes automatically whether it is plugged into slot 1 of the VMEbus backplane or in any other slot. This auto-configuration feature requires SW800-1 to be set to the OFF position. The VMEbus system controller is enabled via auto-configuration if the CPU board is plugged into slot 1. Otherwise, it is disabled.

Caution



If more than one system controller is active in the VMEbus system, the board or other VMEbus participants can be damaged. Therefore, always ensure that only one CPU board is configured to be system controller in the VMEbus system.

Installing the CPU Board

1. Check system documentation for all important steps to be taken before switching off power
2. Take those steps
3. Switch off power

Caution



Before installing the board, check switch settings for consistency (see Table 9 “Switch Settings” on page 2-13).

4. Plug board into system slot on left-hand side

Note: Make sure all other boards which are plugged into the system are to the right of the system board.

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5. Fasten board with screws
6. Plug interface cables into front panel connectors, if applicable
7. Switch on power

Removing the CPU Board

1. Check system documentation for all important steps to be taken before switching off power
2. Take those steps
3. Switch off power
4. Remove interface cables, if applicable
5. Unfasten screws
6. Remove board

Powering Up

We recommend to use a terminal when powering up the SPARC/CPU-54. The advantage of using a terminal is that you do not need any frame buffer, monitor, or keyboard for initial powering up.

Note:

- **Before powering up, check the "Requirements" section on page 2-4 for installation prerequisites and requirements.**
- **If an unformatted floppy disk resides in a floppy drive connected to the SPARC/CPU-54 during power up, the SPARC/CPU-54 does not boot and the OpenBoot prompt does not appear.**
- **Check the consistency of the switch settings (Table 9 "Switch Settings" on page 2-13).**

In order to power up the CPU board, proceed as follows:

1. Connect terminal to front panel serial I/O interface A
   For information on the serial interface connector pinout, see the "On-Board Connectors of the SPARC/CPU-54" section on page 3-10.
2. Switch on system
   The monitor will display information about the OpenBoot booting process.
3. Enter OpenBoot commands, if applicable

Boot Devices OTP PROM and Flash EPROM

By default, the SPARC/CPU-54 boots from the 1 MByte OTP PROM (PLCC socket device) which is not writeable and contains the OpenBoot firmware. Alternatively, a 4 MByte flash EPROM device can be enabled with SW6-2. This flash EPROM device is rewriteable if enabled by SW4-3.

User Application

The SPARC/CPU-54 provides a flash EPROM to store user applications. For write-protection of the flash EPROM, see SW4-3 in the "Switch Settings" section on page 2-12. The commands needed to program the flash EPROM are described in the *SPARC/CPU-54 OpenBoot Enhancements Reference Guide*.

Installing Solaris

The SPARC/CPU-54 is designed to run with Solaris Version 8 10/00 or higher with the 64-bit kernel. Pay attention to the guidelines in this section before and during Solaris installation.

Note:

- **Solaris versions prior to version 8 10/00 are not supported. SPARC/CPU-54 runs with 64-bit kernel only.**
- **If a VME bus read error (e.g. bus time-out) occurs and Solaris 8 version 4/01 is used, Solaris sometimes shuts down the system unexpectedly. To avoid this problem, install Solaris 8 kernel patch 108528-12 or higher. For information on how to install it, refer to the README file contained in the zip file.**

The following devices of the SPARC/CPU-54 are not supported by the Solaris operating system:

- Intel 82559 Ethernet device
- Universe II PCI-to-VMEbus bridge
- On-board flash memory
- Temperature sensors, LEDs, seven-segment display, watchdog, and floppy ejection

If you wish to use one of these devices, you need to install the Force Computers Solaris Driver Package Version 2.11 or higher. For information on which driver must be installed for a particular device, see the “Solaris Driver Package” section on page 2-9.

Solaris 8

When setting up Solaris interactively, these packages can be installed by selecting / deselecting the proper software group in the software dialog window. If applicable, customize the software group as shown in the following table.

Table 10: *Customizing Solaris 8*

Software Group	Customizing
Entire distribution plus OEM support	No customizing required
Entire distribution	No customizing required
Developer system support	If a PS / 2 keyboard / mouse is used, proceed as follows: Under “drivers for SME support (64 Bit)”, select “PS / 2 keyboard and mouse device drivers (Root, 64 Bit).
End user system support	
Core system support	

Note: During installation, make sure that the 64-bit support is enabled.

If a PS / 2 keyboard and mouse is used, the package shown in the table below is available.

Table 11: *Required Solaris Package for Solaris 8*

Package	Description
SUNWCsmex for 64-bit	Drivers for SME systems (64-bit)

Note: During the boot process, the following warning may appear: `WARNING: i2c_client_register_failed`. If this should be the case, the warning can be ignored as it has no impact on the boot process.

Solaris Driver Package

The following table shows which driver has to be installed for a particular device.

Table 12: *Devices and Their Appropriate Drivers*

Device	Driver Name
Intel 82559 Ethernet controller	FRCiprb
Universe II PCI-to-VMEbus bridge	FRCvme
On-board flash memory	FRCflash
Temperature sensors, LEDs, seven-segment display, watchdog, floppy ejection	FRCctrl

For further information on the Solaris Driver Packages Release 2.11, refer to the following sections and to the documentation delivered together with the package. For information on how to install the respective driver, see the Solaris Driver Packages Release 2.11 Installation Guide.

FRCiprb

The assignment of the driver's instance number to an Intel 82559 Ethernet device can be viewed by booting with the OpenBoot command boot -rv. Each device is shown with the driver name and instance number during the Solaris boot up.

The other way to obtain the instance number of the Ethernet devices is to look into the file /etc/path_to_inst. In order to do so, type the command:

```
grep fciprb /etc/path_to_inst
```

Typical output:

```
“/pci@1f,0/pci@3/ethernet@2” 1 “fciprb”
“/pci@1f,0/pci@3/ethernet@1” 0 “fciprb”
```

The first part (in quotation marks) specifies the hardware node name in the device tree. The number specifies the instance number and the third part (also in quotation marks) specifies the driver name.

The following table shows how the hardware node names are assigned to a label on the front panel and the IOBP.

Table 13: *Hardware Node Assignment*

Label	Location	Hardware Node
ETHERNET1	CPU front panel	/pci@1f,0/network@1,1 (standard Solaris hme Ethernet device)
ETHERNET2	CPU IOBP	/pci@1f,0/pci@3/ethernet@1
ETHERNET3	CPU front panel	/pci@1f,0/pci@3/ethernet@2

The following table shows how the driver instance numbers are typically assigned to Ethernet devices on the SPARC/CPU-54 (without IO-54) and the SPARC/CPU-54T (with IO-54).

Table 14: *Instance Number Assignment for SPARC/CPU-54*

Label	Location	Driver Instance Number
ETHERNET1	CPU front panel	hme0
ETHERNET2	CPU IOBP	fciprb0
ETHERNET3	CPU front panel	fciprb1

FRCvme

The FRCvme is a set of drivers which handles the Universe II device. The following functions are supported:

- Master windows
- Slave windows
- Interrupts
- DMA controller
- VME arbiter
- Mailboxes

Additionally, the FRCvme package provides a common programming interface for application and driver development to the FRCvme package and a detailed description of the software interface and sample programs.

For more detailed information and board-specific notes, refer to the Solaris Driver Package Installation Guide.

FRCflash

The Solaris 2.x flash memory driver provides access to the flash EPROM device. According to the SPARC / CPU-54(T) switch settings, the flash EPROM is accessible as one user flash or is divided into a boot and a user section.

The following table shows the effects the different CPU board switch settings have on the flash segmentation and the flash write protection.

Table 15: *Flash Segmentation and Write Protection*

SW4-3	SW6-2	Flash Segmentation and Write-Protection	Boot from
OFF	OFF	4 MByte user section, write-protected	Boot PROM
ON	OFF	4 MByte user section, not write-protected	Boot PROM
OFF	ON	1 MByte boot section, write-protected 3 MByte user section, write-protected	Flash PROM
ON	ON	1 MByte boot section, not write-protected 3 MByte user section, not write-protected	Flash PROM

FRCctrl

The FRCctrl driver contains the sysconfig device driver which offers the following features:

- Sets all user LEDs.
- Sets the seven-segment display.
- Accesses the temperature sensor devices.
  To enable the temperature sensors, set the OpenBoot environment variable env-monitor before booting. To do so, enter at the prompt:

  ```
  setenv env-monitor enabled
  ```
- Handles the floppy disk eject pin.
- Enables and triggers watchdog functions.
  To enable the watchdog, set switch SW6-4 to ON.

3

Controls, Indicators, and Connectors

Front Panel of the SPARC/CPU-54

The following figure shows the connectors, keys and LEDs available on the front panel of the SPARC / CPU-54. For the front panel features of the IO-54, see the *IO-54 Installation Guide.*

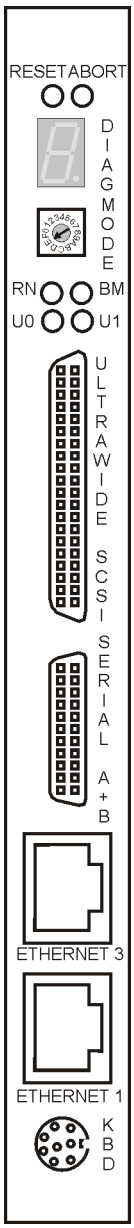


Figure 8: *SPARC/CPU-54 Front Panel*

LEDs

The figure below shows the LEDs available on the SPARC / CPU-54.

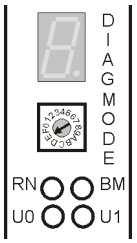


Figure 9: *Front Panel LEDs*

Table 16: *Description of Front Panel LEDs*

LED	Description
DIAG	Software-programmable hexadecimal display for diagnostics
RN	CPU status LED Green: Normal operation Red: Processor halted or reset is active; starts flashing at hung signal of SPARC / CPU-54
BM	VMEbus busmaster and SYSFAIL LED Green: If CPU board accesses VMEbus bus as master Red: If SYSFAIL is asserted from Universerve II to VMEbus Off: Otherwise
U0 and U1	Software-programmable user LEDs Possible status: Off, red, yellow, or green; all colors are either permanently lit up or flash with a frequency of approximately 0.5, 1, or 2 Hz
Ethernet 1, 3	Activity and link LEDs Upper green LED: On: Ethernet link is up Off: Ethernet link is down Lower orange LED: Flashing: Ethernet link activity Off: No link activity

Keys

The front panel of the SPARC/CPU-54 provides two mechanical keys and a hexadecimal rotary switch (front panel shows MODE).

Reset

When enabled and toggled, it instantaneously affects the CPU board by generating a push-button Power On Reset (POR) to the UltraSPARC-IIe. Push-button Power On Reset has the same effect as a Power On Reset from the power supply, with the only difference, that the corresponding status bit (B_POR) in the UltraSPARC-IIe Reset_Control Register is set and the DRAM refresh is not influenced.

Abort

When enabled and toggled, it instantaneously affects the CPU board by generating a push-button external initiated reset (XIR). Push-button external initiated reset allows a user-reset (abort) of part of the processor without resetting the whole system. UltraSPARC-IIe sets the B_XIR bit in the Reset_Control Register when a push-button external initiated reset is detected.

Mode

The mode key is a hexadecimal rotary switch which is decoded with 4 bit. Its functions are user-defined. The default setting is F_{16}.

Connectors

By means of the front panel connectors, the peripherals can be connected to the SPARC / CPU-54.

Ethernet

Two full duplex Ethernet interfaces are available at the front panel via the 10BaseT / 100BaseTx Twisted-Pair-Ethernet (TPE) connectors.

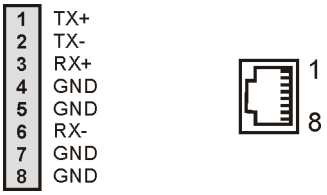


Figure 10: *Twisted-Pair Ethernet Connector Pinout*

The Ethernet #1 interface is also accessible at the 5-row P2 back panel connector. For the connector pinout see Figure 17 “P2 VMEbus Connector Pinout Continued Rows C+D” on page 3-12.

Note: If Ethernet #1 is accessed via the IOBP, the front panel connector is disabled automatically.

Serial I/O

The serial interface on the CPU board's front panel holds the signals for the two serial interfaces A and B. If you want to use both interfaces you need a splitter cable.

Both serial I/O interfaces of the CPU board are independent full-duplex channels. For each of them, the four signals RXD, TXD, RTS, and CTS are also provided via the respective VMEbus P2 connector.

Both I/O interfaces can be configured as RS-232 and RS-422. The selection is made via the switches SW7-1 and SW7-2.

Note: When configuring the serial interfaces as RS-422 and you want to terminate the signals RxD+/- and CTS+/-, you have to mount termination resistors into the serial cable you use. These resistors are not assembled on the CPU board.

The following figures show the pinout of the 26-pin connector in RS-232 and RS-422 mode (factory option).

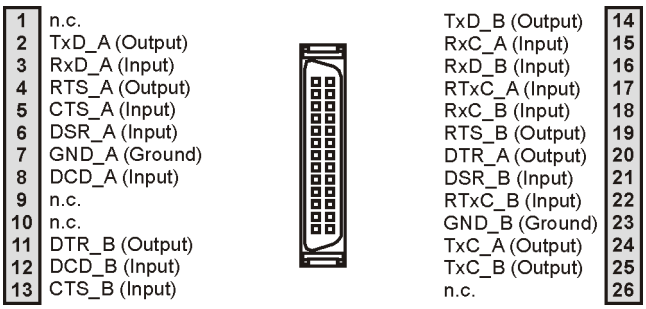


Figure 11: *Serial A+B Connector Pinout RS-232*

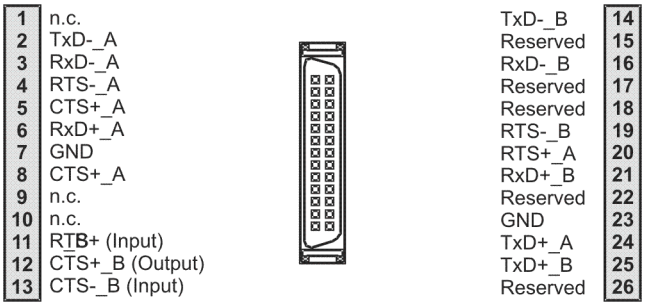


Figure 12: *26-Pin Serial A+B Connector Pinout RS-422*

Keyboard/Mouse

A SUN-type keyboard / mouse is available at the front panel via an 8-pin mini-DIN connector. The pinout can be seen in the following figure.

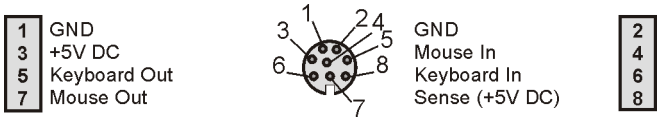


Figure 13: *Keyboard/Mouse Connector Pinout SUN-Type Function*

If using an adapter a PS/2-type interface is also available. The pinout of the PS/2-type interface can be seen in the following figure.

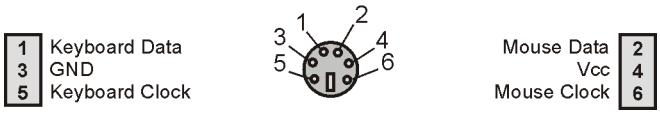


Figure 14: *Keyboard/Mouse Connector Pinout PS/2-Type Function*

SCSI

The following connector pinout shows the signals of the ultra-wide SCSI connector.

Note: The board is not compliant to EN 55022 if you connect a SCSI device to the SCSI connector on the front panel.

1	GND	D12	35
2	GND	D13	36
3	GND	D14	37
4	GND	D15	38
5	GND	DP1	39
6	GND	D0	40
7	GND	D1	41
8	GND	D2	42
9	GND	D3	43
10	GND	D4	44
11	GND	D5	45
12	GND	D6	46
13	GND	D7	47
14	GND	DP0	48
15	GND	GND	49
16	GND	AUTOTERM	50
17	TERMPWR	TERMPWR	51
18	TERMPWR	TERMPWR	52
19	n.c.	n.c.	53
20	GND	GND	54
21	GND	ATN	55
22	GND	GND	56
23	GND	BSY	57
24	GND	ACK	58
25	GND	RST	59
26	GND	MSG	60
27	GND	SEL	61
28	GND	CD	62
29	GND	REQ	63
30	GND	IO	64
31	GND	D8	65
32	GND	D9	66
33	GND	D10	67
34	GND	D11	68

Figure 15: *68-Pin Ultra-Wide SCSI Connector Pinout*

On-Board Connectors of the SPARC/CPU-54

In addition to the front panel connectors, the CPU board provides backplane connectors and on-board connectors for memory modules and for the IO-54.

Table 17: *On-Board Connectors*

Connector Description and Location	Connector Type
VMEbus backplane connector P1	VG 96-pin connector male
VMEbus backplane connector P2	VG 160-pin connector male (in case of three-row factory option VG 96-pin connector male)
IO-54 connector P6	100-pin MBus connector male
Memory module connectors P5, P7	100-pin SMD connector

Table 18: *P2 Backplane Connector Signals*

Interface	Backplane Connector
Ultra-wide SCSI #1	P2 row A+C
Ethernet #1 interface	P2 row Z
Ethernet #2 interface	P2 row Z
Floppy interface	P2 row C
Parallel interface	P2 row C
Serial interface A	P2 row A
Serial interface B	P2 row C
Keyboard and mouse	P2 row A + D

The signal names used in the following pinouts are given in brackets:

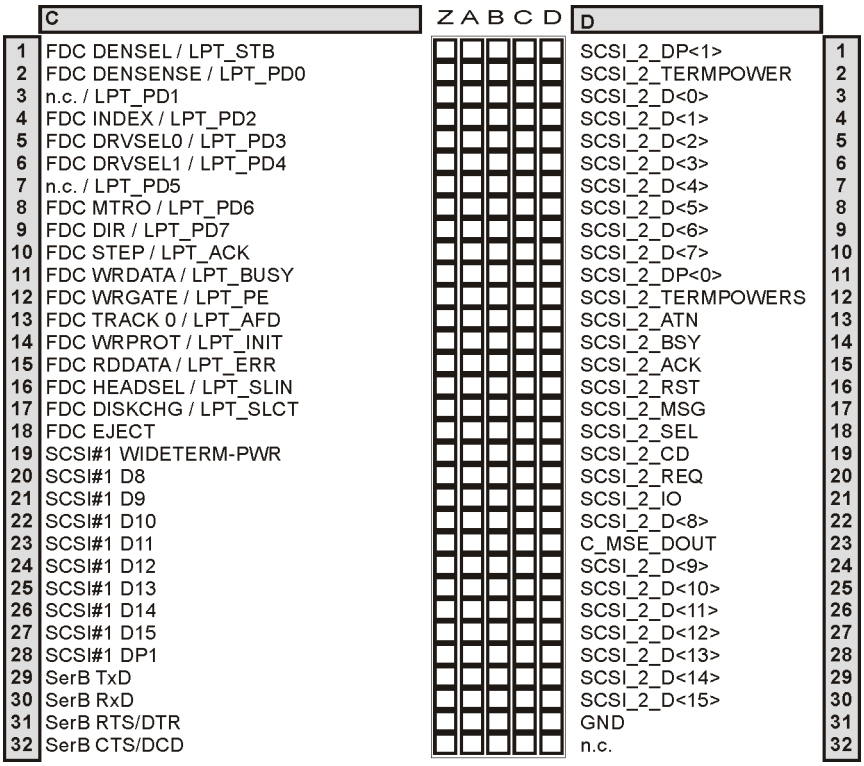
- Floppy (FDC)
- Fused 5V power (VP5)
- Keyboard (KBD) and mouse (MSE)
- Ethernet 1 (TP1R)
- Ethernet 2 (TP2R)
- Parallel (LPT)
- SCSI (SCSI)
- Serial interface A (SerA) and serial interface B (SerB)

The standard CPU board is delivered with a five-row P2 VMEbus connector. However, a three-row P2 connector variant is also available as factory option.

Note: If the three-row P2 VMEbus connector is used, the rows Z and D are not active.

	Z	A	B
1	TP1R_RXD_P	SCSI #1 D0	+5V
2	GND	SCSI #1 D1	GND
3	TP1R_RXD_N	SCSI #1 D2	VME RETRY_N
4	GND	SCSI #1 D3	VME A24
5	TP1R_TXD_P	SCSI #1 D4	VME A25
6	GND	SCSI #1 D5	VME A26
7	TP1R_TXD_N	SCSI #1 D6	VME A27
8	GND	SCSI #1 D7	VME A28
9	TP1R_TREF	SCSI #1 DP0	VME A29
10	GND	SLCT_FDC_LPT	VME A30
11	n.c.	GND	VME A31
12	GND	GND	GND
13	n.c.	SCSI #1 TERMPWR	+5V
14	GND	RTB_PRES	VME D16
15	n.c.	GND	VME D17
16	GND	SCSI #1 ATN	VME D18
17	n.c.	GND	VME D19
18	GND	SCSI #1 BSY	VME D20
19	n.c.	SCSI #1 ACK	VME D21
20	GND	SCSI #1 RST	VME D22
21	n.c.	SCSI #1 MSG	VME D23
22	GND	SCSI #1 SEL	GND
23	n.c.	SCSI #1 CD	VME D24
24	GND	SCSI #1 REQ	VME D25
25	TP2R_RXD_N	SCSI #1 IO	VME D26
26	GND	MSE DIN	VME D27
27	TP2R_RXD_P	KBD DOUT	VME D28
28	GND	KBD DIN	VME D29
29	TP2R_TXD_P	SerA TxD	VME D30
30	GND	SerA RxD	VME D31
31	TP2R_TXD_N	SerA RTS/DTR	GND
32	GND	SerA CTS/DCD	+5V

Figure 16: *P2 VMEbus Connector Pinout Rows Z-B*



	C	Z A B C D	D	
1	FDC DENSEL / LPT_STB		SCSI_2_DP<1>	1
2	FDC DENSENSE / LPT_PD0		SCSI_2_TERMPOWER	2
3	n.c. / LPT_PD1		SCSI_2_D<0>	3
4	FDC INDEX / LPT_PD2		SCSI_2_D<1>	4
5	FDC DRVSEL0 / LPT_PD3		SCSI_2_D<2>	5
6	FDC DRVSEL1 / LPT_PD4		SCSI_2_D<3>	6
7	n.c. / LPT_PD5		SCSI_2_D<4>	7
8	FDC MTR0 / LPT_PD6		SCSI_2_D<5>	8
9	FDC DIR / LPT_PD7		SCSI_2_D<6>	9
10	FDC STEP / LPT_ACK		SCSI_2_D<7>	10
11	FDC WRDATA / LPT_BUSY		SCSI_2_DP<0>	11
12	FDC WRGATE / LPT_PE		SCSI_2_TERMPOWERS	12
13	FDC TRACK 0 / LPT_AFD		SCSI_2_ATN	13
14	FDC WRPROT / LPT_INIT		SCSI_2_BSY	14
15	FDC RDDATA / LPT_ERR		SCSI_2_ACK	15
16	FDC HEADSEL / LPT_SLIN		SCSI_2_RST	16
17	FDC DISKCHG / LPT_SLCT		SCSI_2_MSG	17
18	FDC EJECT		SCSI_2_SEL	18
19	SCSI#1 WIDETERM-PWR		SCSI_2_CD	19
20	SCSI#1 D8		SCSI_2_REQ	20
21	SCSI#1 D9		SCSI_2_IO	21
22	SCSI#1 D10		SCSI_2_D<8>	22
23	SCSI#1 D11		C_MSE_DOUT	23
24	SCSI#1 D12		SCSI_2_D<9>	24
25	SCSI#1 D13		SCSI_2_D<10>	25
26	SCSI#1 D14		SCSI_2_D<11>	26
27	SCSI#1 D15		SCSI_2_D<12>	27
28	SCSI#1 DP1		SCSI_2_D<13>	28
29	SerB TxD		SCSI_2_D<14>	29
30	SerB RxD		SCSI_2_D<15>	30
31	SerB RTS/DTR		GND	31
32	SerB CTS/DCD		n.c.	32

Figure 17: *P2 VMEbus Connector Pinout Continued Rows C+D*

4

OpenBoot Firmware

Introduction

The OpenBoot firmware consists of the Common Operations and Reset Environment (CORE), the POST, the OpenBoot Diagnostics (OBDIAG), and the OpenBoot itself as well as support for the VxWorks RTOS.

The OpenBoot firmware is subject to changes. For the newest version and how to upgrade refer to the SMART service accessible via the Force Computers World Wide Web site (www.forcecomputers.com).

Note: The appearance of the on-screen output shown in the examples can differ from the appearance of the output on your monitor according to your device tree (CPU architecture).

For more information on the OpenBoot firmware, see the OpenBoot 4.x Manual Set.

CORE

CORE is responsible for setting up proper environments for booting purposes. It first initializes the system to a status where different firmware can be loaded from.

CORE automatically transfers control to its clients (such as OpenBoot, VxWorks, Chorus Booter...) during power up.

Furthermore, it provides a unified interface for using public CORE functions. Thus the CORE unifies system initialization and minimizes modifications within the upper level firmware.

The following figure gives a system overview of which systems are initialized by CORE.

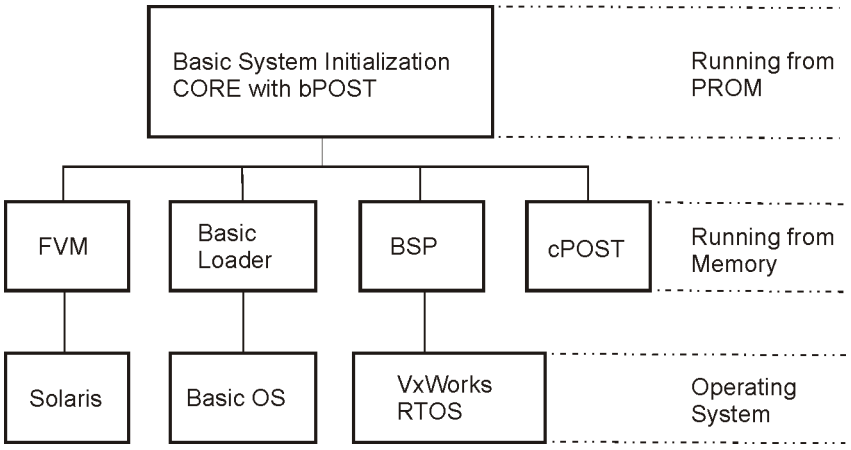


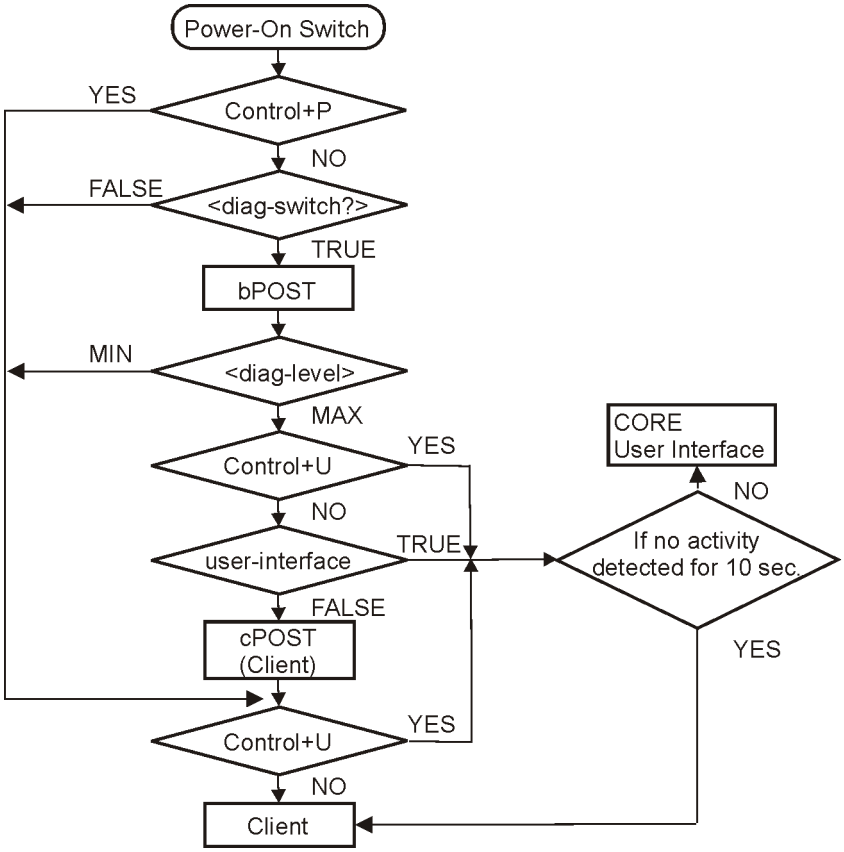
Figure 18: *System Overview*

Additionally, CORE is designed to reach the following goals:

- Ability to use I/O devices including serial port, flash, floppy, and net early on the cold boot sequence of a firmware client.
- Basic system tests that can replace existing POST in min. mode.
- System testing may be done using the POST drop-in in max. mode.
- Error recovery from exceptions which currently do not exist in OpenBoot and from any fatal conditions during flash update
- Developing standard validation test suites that could prevent major bugs in CORE and clients
- Sample client codes that could facilitate any client porting

CORE Workflow

The following figure describes the workflow of CORE.



CORE Commands

In order to change or interrupt the boot process in CORE, the following commands can be executed:

- Skip POST: <Control>+<P>
- Enter user interface: <Control>+<U>
- User default NVRAM variables for this run: <Control>+<N>
- Turn-on messages (if <diag-switch> is set to true): <Control>+<M>

POST

At hardware power-on or button power-on, the CORE firmware executes power-on selftest (POST) if the NVRAM configuration parameter <diag-switch?> was set to true beforehand. The extents of certain tests executed within in the POST depend on the state of the configuration parameter <diag-level>.

You choose between minimal or maximal testing by setting this configuration parameter to min or max. If the NVRAM configuration parameter <diag-switch?> is true for each test, a message is displayed on a terminal connected to the serial I/O interface A.

If the system does not work correctly, error messages will be displayed which indicate the problem. After POST, the OpenBoot firmware boots an operating system or enters the Forth monitor, if the NVRAM configuration parameter <auto-boot?> is false.

OpenBoot

Booting the system is the most important function of the OpenBoot firmware.

Booting is the process of loading and executing a stand-alone program such as the operating system. After the system is powered on, it usually boots automatically after it has passed POST (power-on self-test) which occurs without user intervention.

If necessary, you can explicitly initiate the boot process from the OpenBoot command interpreter. Automatic booting uses the default boot device specified in the nonvolatile RAM (NVRAM). User-initiated booting either uses the default boot device or one specified by the user.

In order to boot the system from the default boot device, enter the following command at the Forth monitor prompt ok:

```
ok boot
```

The boot command has the following format:
boot <device-specifier> <filename> <-bootoption>

Optional Boot Parameters

Table 19: *Boot Parameters*

Parameter	Description	
<device-specifier>	Name (full path or alias) of the boot device Typical values are cdrom, disk, floppy, net or tape.	
<filename>	Name of program to be booted The filename parameter is relative to the root of the selected device. If no filename is specified, the boot command uses the value of the boot file NVRAM parameter. The NVRAM parameters used for booting are described in the following section.	
<-bootoption>	Bootoption may be one of the following:	
	Option	**Description**
	-a	Prompts interactively for device and name of boot file.
	-h	Halts after loading program.
	-r	Reconfigures Solaris device drivers after changing hardware configuration.
	-v	Prints verbose information during boot procedure.

Boot Devices

To explicitly boot from the internal disks using the Forth Monitor, enter:

```
ok boot disk
or
ok boot disk-2
```

To retrieve a list of all device alias definitions, enter at the Forth Monitor command prompt:
devalias

The following tables list some typical device aliases.

Table 20: *Device Alias Definitions for SCSI#1*

Alias	Description
scsi	SCSI
disk	Disk SCSI-target-ID 0
diskf	Disk SCSI-target-ID f
diske	Disk SCSI-target-ID e
diskd	Disk SCSI-target-ID d
diskc	Disk SCSI-target-ID c
diskb	Disk SCSI-target-ID b
diska	Disk SCSI-target-ID a
disk9	Disk SCSI-target-ID 9
disk8	Disk SCSI-target-ID 8
disk7	Disk SCSI-target-ID 7
disk6	Disk SCSI-target-ID 6
disk5	Disk SCSI-target-ID 5
disk4	Disk SCSI-target-ID 4
disk3	Disk SCSI-target-ID 3
disk2	Disk SCSI-target-ID 2
disk1	Disk SCSI-target-ID 1
disk0	Disk SCSI-target-ID 0
tape (or tape0)	First tape drive SCSI-target-ID 4
tape1	Second tape drive SCSI-target-ID 5
cdrom	CD-ROM partition f, SCSI-target-ID 6

Table 21: *Device Alias Definitions for SCSI#2*

Alias	Description
scsi-2	SCSI 2
disk-2	Default disk SCSI-target-ID 0
disk2f	Disk SCSI-target-ID f
disk2e	Disk SCSI-target-ID e
disk2d	Disk SCSI-target-ID d
disk2c	Disk SCSI-target-ID c
disk2b	Disk SCSI-target-ID b
disk2a	Disk SCSI-target-ID a
disk29	Disk SCSI-target-ID 9
disk28	Disk SCSI-target-ID 8
disk27	Disk SCSI-target-ID 7
disk26	Disk SCSI-target-ID 6
disk25	Disk SCSI-target-ID 5
disk24	Disk SCSI-target-ID 4
disk23	Disk SCSI-target-ID 3
disk22	Disk SCSI-target-ID 2
disk21	Disk SCSI-target-ID 1
disk20	Disk SCSI-target-ID 0
tape-2 (or tape20)	First tape drive SCSI-target-ID 4
tape21	Second tape drive SCSI-target-ID 5
cdrom-2	CD-ROM partition f, SCSI-target-ID 6

Table 22: *Other Device Alias Definitions*

Alias	Description
ebus	EBus
flash	Flash EPROM
flash-prog	Flash EPROM programming mode
floppy	Floppy disk
keyboard	Keyboard
mouse	Mouse
net	Ethernet
pci	Primary PCI bus
ttya	Serial interface A
ttyb	Serial interface B
vme	VME

OBDIAG

OBDIAG stands for OpenBoot Diagnostics and is an additional diagnostics drop-in driver program which serves as an NVRAM configuration feature.

It allows to test the hardware by calling OBDIAG when the OpenBoot firmware is present and the <ok> prompt has appeared. During the start-up sequence of the CPU, OpenBoot searches for the presence of devices on all expansion buses and evaluates their characteristics such as device-ID, device-type, vendor-ID, and revision-ID. In order to test the hardware, OBDIAG requires selftest methods for the discovered devices. If OBDIAG does not find any selftest methods in the device nodes, it looks for its own selftest methods.

There are two different methods to execute OBDIAG:

a) Set the configuration variable mfg-mode to chamber and set the variable diag-switch? to true. To set the variable mfg-mode to chamber, enter:
`setenv mfg-mode chamber`
When setting the variable mfg-mode to chamber a script of additional diagnostic tests is executed automatically after each POST from OBDIAG provided the POST has been running without failure during hardware power on.

b) Open OBDIAG by entering the following command at the ok prompt:
`obdiag`

After entering the command obdiag at the ok prompt, the OBDIAG main menu mask appears. The following figure shows the main menu mask if the SPARC / CPU-54 is used and if the standard probe lists have not been changed.

```
o b d i a g

  1 busnet@2d,0          2 ebus@1              3 ecpp@14,340278
  4 eeprom@14,0          5 ethernet@1          6 ethernet@2
  7 fdthree@14,3203f0    8 flashprom@10,0      9 network@1,1
 10 scsi@4              11 scsi@4,1           12 serial@14,400000
 13 sysconfig@14,600000 14 vme@5

   Commands: test test-all except help what printenvs setenv versions exit

obdiag>
```

Figure 19: *OBDIAG Main Menu*

When OBDIAG is called, the <obdiag> test prompt appears and you can now choose the required test. You can run single tests, a number of tests, all tests, or all tests with exceptions. If the test has passed successfully, a short test comment will appear on screen. In order to return to the main menu, hit the enter key.

In order to terminate OBDIAG and return to OpenBoot, enter

`exit`

The OpenBoot prompt will then reappear.

Apart from testing the hardware, you can also call several commands which can be seen in the ODBIAG main menu. The following table provides an overview of these commands.

Table 23: *OBDIAG Commands*

Command	Description
exit	Exits obdiag tool
help	Prints this help information
setenv	Sets diagnostic configuration variable to new value
printenvs	Prints values for diagnostic configuration variables
versions	Prints selftests, library, and obdiag tool versions
test-all	Tests all devices displayed in the main menu
test 1,2,5	Tests devices 1, 2, and 5
except 2,5	Tests all devices except for devices 2 and 5
what 1,2,5	Prints some selected properties for devices 1, 2, and 5

OBDIAG provides a brief excerpt of the OpenBoot configuration variables. The values of the variables are displayed after entering the following command:

`printenvs`

You can decide whether the chosen test will either stop at the occurrence of the first error or continue to test the hardware. It is also possible to run the test more than once or produce a detailed print-out of the test.

The example below shows the detailed print-out of an OBDIAG test.

Example:

```
obdiag> setenv diag-verbosity 2
diag-verbosity =      2

Hit any key to return to the main menu <cr>

obdiag> setenv diag-continue? 0
diag-continue? =      0

Hit any key to return to the main menu <cr>

obdiag> test 2
Hit the spacebar to interrupt testing
Testing /pci@1f,0/ebus@1
SUBTEST: vendor-id-test
SUBTEST: device-id-test
SUBTEST: mixmode-read
SUBTEST: e2-class-test
SUBTEST: status-reg-walk1
SUBTEST: line-size-walk1
SUBTEST: latency-walk1
SUBTEST: line-walk1
SUBTEST: pin-test
SUBTEST: dma-reg-test
SUBTEST: dma-func-test
Selftest at /pci@1f,0/ebus@1
..................................... passed

Hit any key to return to the main menu  <cr>
obdiag> exit <cr>
ok
```

VxWorks Support

The boot PROM delivered together with the CPU board contains support for the real-time operating system VxWorks 5.4 from WindRiver Systems. A VxWorks booter, “bootrom.hex” image, is provided as dropin named “bootrom”. In order to execute it, enter at the CORE command prompt;

```
execute bootrom
```

To automatically start the VxWorks booter at power-up, enter:

```
set kernel bootrom
```

NVRAM Boot Parameters

The OpenBoot firmware holds its configuration parameters in NVRAM. To see a list of all available configuration parameters, enter at the Forth Monitor prompt:

```
printenv
```

Note: By default the SPARC/CPU-54 boots the operating system automatically. If this is not the case, ensure that the <auto-boot?> parameter is set to true.

To set specific parameters, use the setenv command as shown below:
setenv <configuration_parameter> <value>

The configuration parameters in the following table are involved in the boot process.

Table 24: *Setting Configuration Parameters*

Parameter	Default Value	Description
auto-boot?	true	If true, automatic booting after power on or reset
boot-device	disk	Device from which to boot
boot-file	empty string	File to boot
diag-switch?	false	If true, run in diagnostic mode
diag-device	net	Device from which to boot in diagnostic mode
diag-file	empty string	File to boot in diagnostic mode

When booting an operating system or another stand-alone program, and neither a boot device nor a filename is supplied, the boot command of the Forth monitor takes the omitted values from the NVRAM configuration parameters. If the parameter <diag-switch?> is false, the parameters <boot-device> and <boot-file> are used. Otherwise, the OpenBoot firmware uses the parameters <diag-device> and <diag-file> for booting.

Diagnostics

The Forth Monitor includes several diagnostic routines. These on-board tests let you check devices such as network controller, SCSI devices, floppy disk system, memory, clock, keyboard and audio. User-installed devices can be tested if their firmware includes a self-test routine.

The table below lists several diagnostic routines.

Table 25: *Diagnostic Routines*

Command	Description
probe-scsi	Identifies devices connected to the primary SCSI bus.
probe-scsi-all [device-path]	Performs probe-SCSI on all SCSI buses installed in the system below the specified device tree node. If device-path is omitted, the root node is used.
test [device-specifier]	Executes the specified device's self-test method. <device-specifier> may be a device path name or a device alias. Example: test net - test network connection
test-all [device-specifier]	Tests all devices that have a built-in self-test method and that reside below the specified device tree node. If device-path is omitted, the root node is used.
watch-clock	Monitors the clock function.
watch-net	Monitors network connection via primary Ethernet.

SCSI Bus

To check the on-board SCSI#1 or SCSI#2 for connected devices, enter:

`probe-scsi`

```
ok probe-scsi
Primary Ultra SCSI bus
Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
Secondary Ultra SCSI bus
ok
```

All SCSI Buses

To check all SCSI buses installed in the system, enter the following:

probe-scsi-all

The actual response depends on the devices on the SCSI buses.

Note: A terminal message as answer to the command probe-scsi-all can take up to two minutes.

```
ok probe-scsi-all
/pci@1f,0/scsi@2

Target 6
Unit 0 Disk Removable Read Only Device SONY CD-ROM CDU-8012 3.1a

/pci@1f/pci@4,1/scsi@2

Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
ok
```

Single Device

To test a single installed device, enter:

`test <device-specifier>`

This executes the selftest device method of the specified device node.

<Device-specifier> may be a device path name or a device alias as described in Table 20 “Device Alias Definitions for SCSI#1” on page 4-8 and in Table 21 “Device Alias Definitions for SCSI#2” on page 4-9. The response depends on the selftest of the device node.

Group of Devices

To test a group of installed devices, enter:

`test-all`

All devices below the root node of the device tree are tested. The response depends on the devices having a selftest method. If a device specifier option is supplied at the command line, all devices below the specified device tree node are tested.

Clock

To test the clock function enter:

`watch-clock`

```
ok watch-clock
Watching the ‘seconds’ register of the real time clock chip.
It should be ‘ticking’ once a second.
Type any key to stop.
22
ok
```

The system responds by incrementing a number every second. Press any key to stop the test.

Network

To monitor the network connection enter:

`watch-net`

```
ok watch-net
Internal loopback test -- succeeded.
Transceiver check -- Using Onboard transceiver -- Link Up.
passed
Using Onboard transceiver -- Link Up.
Looking for Ethernet packets.
‘.’ is a good packet. ‘X’ is a bad packet.
Type any key to stop.
...........X.........................X.............
ok
```

The system monitors the network traffic. It displays a dot (.) each time it receives a valid packet and displays an X each time it receives a packet with an error which can be detected by the network hardware interface.

Displaying System Information

The Forth Monitor provides several commands to display system information such as the system banner, the Ethernet address for the Ethernet controller, the contents of the ID PROM, and the version number of the OpenBoot firmware.

Ethernet Address and Host ID

In order to see the Ethernet address and host ID, enter the following command at the OpenBoot prompt:

```
ok banner
```

The figures below explain how the SPARC/CPU-54 Ethernet address and the host ID are determined.

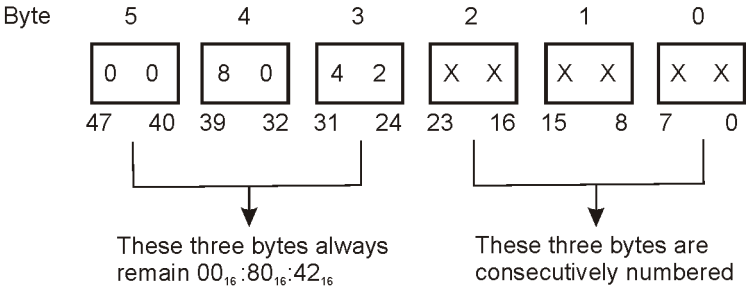


Figure 20: *48-bit (6-byte) Ethernet Address*

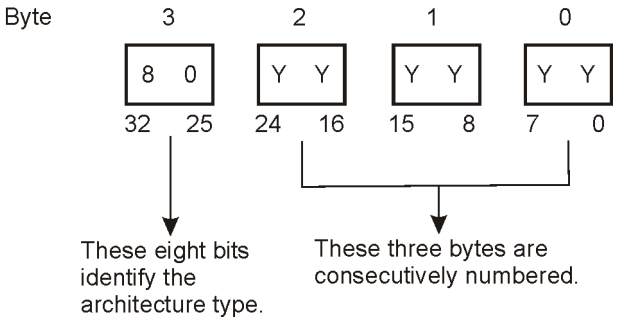


Figure 21: *32-bit (4-byte) Host ID*

ID PROM

The ID PROM contains specific information on the individual machine including the serial number, date of manufacture, and assigned Ethernet address. The following table lists these commands.

Table 26: *Commands to Display System Information*

Command	Description
banner	Displays system banner.
.enet-addr	Displays the Ethernet address.
.idprom	Displays ID PROM contents, formatted.
.traps	Displays a list of SPARC trap types.
.version	Displays version and date of the boot PROM.
show-devs	Displays a list of all device tree nodes.
devalias	Displays a list of all device aliases.

Resetting the System

If your system needs to be reset, there are two possibilities:

- Software reset
  For this type of reset, use the command reset at the Forth command line.
- Button power-on reset

In both cases the system begins with the initialization procedures. If the system is reset via a button power-on reset, the power-on self-test is executed before the initialization if the NVRAM configuration variable <diag-switch?> is set true.

Activating OpenBoot Help

The Forth Monitor contains an online help which can be activated by entering the command help. Entering help creates the following screen output.

```
ok help
Enter ‘help command-name’ or ‘help category-name’ for more help
(Use ONLY the first word of a category description)
Examples: help select -or- help line
Main categories are:
Numeric output
Radix (number base conversions)
Arithmetic
Memory access
Line editor
System and boot configuration parameters
Select I/O devices
Floppy eject
Power-on reset
Diag (diagnostic routines)
Resume execution
File download and boot
Nvramrc (making new commands permanent)
ok
```

A list of all available help categories is displayed. These categories may also contain subcategories. To get help for special Forth words or subcategories, enter

`help <name>`

The online help shows you the Forth word, the parameter stack before and after execution of the Forth word (before -- after), and a short description.

The online help of the Forth monitor is located in the boot PROM. This means that an online help is not available for all Forth words.

Typical examples for how to get help for special Forth words or subcategories are given below.

```
ok help power
reset-all         reset-machine, (simulates power cycling )
power-off         Power Off
ok
```

```
ok help memory
dump ( addr length -- ) display memory at addr for length bytes
fill ( addr length byte -- ) fill memory starting at addr with
byte
move ( src dest length -- ) copy length bytes from src to dest
address
map? ( vaddr -- ) show memory map information for the virtual
address
x? ( addr -- ) display the 64-bit number from location addr
l? ( addr -- ) display the 32-bit number from location addr
w? ( addr -- ) display the 16-bit number from location addr
c? ( addr -- ) display the 8-bit number from location addr
x@ ( addr -- n ) place on the stack the 64-bit data at location
addr
l@ ( addr -- n ) place on the stack the 32-bit data at location
addr
w@ ( addr -- n ) place on the stack the 16-bit data at location
addr
c@ ( addr -- n ) place on the stack the 8-bit data at location addr
x! ( n addr -- ) store the 64-bit value n at location addr
l! ( n addr -- ) store the 32-bit value n at location addr
w! ( n addr -- ) store the 16-bit value n at location addr
c! ( n addr -- ) store the 8-bit value n at location addr
ok
```

5

Maps and Registers

Address Map

The main address map gives an overview of the whole address space of the UltraSPARC-II CPU. This address range is among others used for the main memory and the system configuration registers. Each defined address space is divided into subspaces which are described in the following chapter.

Table 27: *PCI Addresses Considered by the PCI-to-EBus2 Controller*

PCI Address	Description	EBUS CS#
$F0000000_{16}$ - $F0FFFFFF_{16}$	Up to 16 MByte of boot and user flash	0
$F1000000_{16}$ - $F10FFFFF_{16}$	TOD / NVRAM M48T58	1
$F1100000_{16}$ - $F11FFFFF_{16}$	Boot FLASH PLCC	2
$F1200000_{16}$ - $F12FFFFF_{16}$	Reserved	3
$F1300000_{16}$ - $F13FFFFF_{16}$	Super-I / O PC97307	4
$F1400000_{16}$ - $F14FFFFF_{16}$	Serial communication controller SAB82532	5
$F1500000_{16}$ - $F15FFFFF_{16}$	I^2C controller	6
$F1600000_{16}$ - $F16FFFFF_{16}$	System Configuration registers (EBUS-LCA XCS20XL)	7
$F1700000_{16}$ - $F17FFFFF_{16}$	Ebus2 Controller Configuration registers	n.a.

Status and Control Register

The following table provides an overview of the system configuration registers which are described in this chapter.

Table 28: *System Configuration Register Overview*

Offset	Reset Value	Size in Byte	Description
60.0000_{16}	$F0_{16}$	8	USER LED1 Control register
60.0001_{16}	$F0_{16}$	8	USER LED 2 Control register
60.0002_{16}	$F3_{16}$	8	Reserved
60.0003_{16}	$F0_{16}$	8	Reserved
60.0004_{16}	$F0_{16}$	8	Miscellaneous Control register
60.0005_{16}	$F0_{16}$	8	Miscellaneous Control- and Status register
60.0006_{16}	$F0_{16}$	8	Watchdog Timer and Temperature Control Interrupt Control- and Status register
60.0007_{16}	$F0_{16}$	8	Watchdog Timer Trigger register
60.0008_{16}	$F0_{16}$	8	Reserved
60.0009_{16}	$F0_{16}$	8	Reserved
$60.000A_{16}$	$F0_{16}$	8	SYSFAIL, ACFAIL Interrupt Control register
$60.000B_{16}$	FF_{16}	8	Reserved
$60.000C_{16}$	FF_{16}	8	Reserved
$60.000D_{16}$	FF_{16}	8	Switch 7 Status register
$60.000E_{16}$	FX_{16}	8	Reset Status register
$60.000F_{16}$	FX_{16}	8	System Configuration Identification register
60.0010_{16}	00_{16}	8	Seven Segment LED Display Control register
60.0011_{16}	XX_{16}	8	Rotary Switch Status register
60.0012_{16}	XX_{16}	8	Switch 4 and 5 Status register
60.0013_{16}	XF_{16}	8	Switch 800 Status register
60.0020_{16}	XF_{16}	8	Timer Control register
60.0024_{16}	XF_{16}	8	Timer Initial Control register L
60.0025_{16}	XF_{16}	8	Timer Initial Control register U

Table 28: *System Configuration Register Overview (cont.)*

Offset	Reset Value	Size in Byte	Description
60.0026_{16}	XF_{16}	8	Timer Counter Status register L
60.0027_{16}	XF_{16}	8	Timer Counter Status register U
60.0028_{16}	FX_{16}	8	RTB Status register
60.0029_{16}	$F0_{16}$	8	Reserved
$60.002A_{16}$	$F0_{16}$	8	RS-422 Control and Status register
$60.002B_{16}$	$F0_{16}$	8	Ethernet Configuration register

User LED Control Registers

The following registers control front panel LED related features.

User LED 1 Control Register

Table 29: *User LED 1 Control Register*

Address: F1600000$_{16}$			
Bit	**Signal**	**Description**	**Access**
1...0	COLOR	Turns user LED on or off and controls color of LED. 00_2: User LED turned off 01_2: User LED turned on and shines green 10_2: User LED turned on and shines red 11_2: User LED turned on and shines yellow	r / w
3...2	BLINK_FREQ	Controls frequency at which user LED blinks. 00_2: User LED not flashing 01_2: User LED flashing at 0.5 Hz (slow) 10_2: User LED flashing at 1.0 Hz (moderate) 11_2: User LED flashing at 2.0 Hz (fast)	r / w
7...4	Reserved	Reserved	r

User LED 2 Control Register

Table 30: *User LED 2 Control Register*

Address: F1600001$_{16}$			
Bit	**Signal**	**Description**	**Access**
1...0	COLOR	Turns user LED on or off and controls color of LED. 00_2: User LED turned off 01_2: User LED turned on and shines green 10_2: User LED turned on and shines red 11_2: User LED turned on and shines yellow	r / w
3...2	BLINK_FREQ	Controls frequency at which user LED flashes. 00_2: User LED not flashing 01_2: User LED flashing at 0.5 Hz (slow) 10_2: User LED flashing at 1.0 Hz (moderate) 11_2: User LED flashing at 2.0 Hz (fast)	r / w
7...4	Reserved	Reserved	r

Control Register

The following register serves to control and monitor various conditions of the SPARC/CPU-54.

Table 31: *Control Register*

Address: F1600004$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	Reserved	Reserved	r
1	Reserved	Reserved	r
2	EJECT_FD	Ejects floppy disk in floppy disk drive. 0 (default): Bit is cleared 1: Bit is set, floppy disk ejected.	r/w
3	RESET_STAT_CLR	Clears status bits in Reset Status register after reset occurred and software has determined reason for reset. 0: Bit is cleared. 1: Bit is set (1), all status bits are cleared.	r/w
4...7	Reserved	Reserved	r

Control and Status Register

Table 32: *Control and Status Register*

Address: F1600005$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	SW_PLCC_ TSOP	Simulates SW6-2 by software. 0: Bit is cleared after reset. 1: Bit is set by Software, then BOOT-PLCC device is switched off and TSOP BOOT Flash device is selected in corresponding BOOT memory area.	r / w
1	PS / 2_KBD_ MSE	Reflects whether there is a PS / 2 adapter cable plugged to front panel keyboard / mouse connector or not. 0: No PS / 2 adapter cable 1: PS / 2 adapter cable plugged to front panel keyboard / mouse connector.	r
2	IS_TEMP1	Reflects state of output signal O.S. of first LM75 digital temperature sensor. 0: Bit is cleared, state of signal is low. 1: State of temperature sensor's output signal is high.	r
3	IS_TEMP2	Reflects state of output signal O.S. of second LM75 digital temperature sensor. 0: Bit is cleared, state of signal is low. 1: State of signal is high.	r
4...7	Reserved	Reserved	r

The temperature sensors may be programmed in such a way that either the O.S. output is operating in the Comparator Mode or the Interrupt Mode.

In the comparator mode the O.S output is cleared (0) when the current temperature exceeds an upper temperature limit (T_{OS}); and the O.S. output is set (1) only when the current temperature falls below a lower limit (T_{HYST}).

In the interrupt mode the O.S output is cleared (0) whenever the current temperature exceeds an upper temperature limit (T_{OS}), or falls below a lower limit (T_{HYST}). The O.S. output is set (1) only upon reading one of the temperature sensor's internal registers across the I^2C Bus.

Watchdog Timer and Temperature Control Register

The registers described in this section serve to control and monitor the watchdog and temperature sensors of the SPARC/CPU-54.

Watchdog Timer and Temperature Control Status Register

For temperature control, two temperature sensors connected to the I^2C-based temperature controller LM75 are used. The watchdog time-out is three seconds.

Table 33: *Watchdog Timer and Temperature Control Status Register*

Address: F1600006$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	IE_WDT	Enables Watchdog Timer Interrupt. 0: Watchdog Timer interrupt is disabled 1: Watchdog Timer interrupt is enabled.	r/w
1	IS_WDT	1: Watchdog timer interval still does not expire. Watchdog logic designed within LCA is fully compatible with Watchdog Timer device MAX815.	r
2	IE_TEMP	Enables Temperature Control Interrupt. 0: Temperature Control interrupt is disabled. 1: Temperature Control interrupt is enabled.	r/w
3	IP_TEMP	Reflects if one of two temperature sensors has its O.S. output active and signals an alarm condition. 0: No temperature Control Interrupt is pending. 1: Temperature Control Interrupt is pending.	r
4...7	Reserved	Reserved	r

Watchdog Timer Trigger Register

Table 34: *Watchdog Timer Trigger Register*

Address: F1600007$_{16}$			
Bit	**Signal**	**Description**	**Access**
0...2	Reserved	Reserved	r
3	WDI	Triggers Watchdog Timer. 0: Default 1: To start Watchdog timer (must be enabled by hardware-switch SW6-4 in ON position), it is necessary to trigger WDI once.	r / w
4...7	Reserved	Reserved	r

SYSFAIL and ACFAIL Interrupt Control Register

Note: SYSFAIL/ACFAIL are rising edge sensitive.

Table 35: *SYSFAIL and ACFAIL Interrupt Control Register*

Address: F160000A$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	IE_SYSF	Enables SYSFAIL interrupt. 0: SYSFAIL interrupt enabled 1: SYSFAIL interrupt disabled	r / w
1	IP_SYSF	Reflects if SYSFAIL interrupt is pending. 0: No SYSFAIL interrupt is pending. 1: SYSFAIL interrupt is pending.	r / w
2	IE_ACFAIL	Enables ACFAIL interrupt. 0: ACFAIL interrupt disabled 1: ACFAIL interrupt enabled	r / w
3	IP_ACFAIL	Reflects if ACFAIL interrupt is pending due to a low to high transition of signal SYSFAIL. 0: No ACFAIL interrupt pending 1: ACFAIL interrupt pending	r / w
4...7	Reserved	Reserved	r

Reset Status Register

Once one of the bits listed below has been set (1), it can be cleared (0) by setting the RESET_STAT_CLR bit in the Miscellaneous Control Register.

Table 36: *Reset Status Register*

Address: F160000E$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	KEY_RESET	Reflects whether a reset has been generated. 0: No reset 1: Reset has been generated	r
1	BUS_RESET	Reflects whether a reset has been generated. 0: No reset 1: Reset has been generated	r
2	WDT_RESET	Reflects whether a reset has been generated. 0: No reset 1: Reset has been generated	r
3...7	Reserved	Reserved	r

Note: When all status bits in this register are cleared (0) after a reset, then the reset has been generated due to a power on reset. A power on reset occurs when the power supply unit is turned on, or the power supply sensor detects that one of the available power supply voltages falls below a tolerable limit.

System Configuration Identification Register

Table 37: *System Configuration Register*

Address: F160000F$_{16}$			
Bit	**Signal**	**Description**	**Access**
3...0	ID[3...0]	Reads the version of LCA logic Current revision is F1$_{16}$	r
7...4	Reserved	Reserved	r

Seven-Segment LED Display Control Register

Table 38: *Seven-Segment LED Display Control Register*

Address: F1600010$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	SEG_A	Turns seven-segment LED display's segment A on or off. 0: Segment turned off 1: Segment turned on	w
1	SEG_B	Turns seven-segment LED display's segment B on or off. 0: Segment turned off 1: Segment turned on	w
2	SEG_C	Turns seven-segment LED display's segment C on or off. 0: Segment turned off 1: Segment turned on	w
3	SEG_D	Turns seven-segment LED display's segment D on or off. 0: Segment turned off 1: Segment turned on	w
4	SEG_E	Turns seven-segment LED display's segment E on or off. 0: Segment turned off 1: Segment turned on	w

Table 38: *Seven-Segment LED Display Control Register (cont.)*

Address: F1600010$_{16}$			
Bit	**Signal**	**Description**	**Access**
5	SEG_F	Turns seven-segment LED display's segment F on or off. 0: Segment turned off 1: Segment turned on	w
6	SEG_G	Turns seven-segment LED display's segment G on or off. 0: Segment turned off 1: Segment turned on	w
7	SEG_DP	Turns seven-segment LED display's segment DP on or off. 0: Segment turned off 1: Segment turned on	w

Switch Status Register

The registers described in this section serve to monitor the condition of the various switches on the SPARC/CPU-54.

Serial Protocol Status Register

Table 39: *Serial Protocol Status Register*

Address: F160000D$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	SW7_1	Reflects state of switch SW7-1. 0: RS-422 enabled (factory option) 1 (default): RS-232 enabled	r
1	SW7_2	Reflects state of switch SW7-2. 0: RS-422 enabled (factory option) 1 (default): RS-232 enabled	r
2	SW7_3	Reflects state of reserved switch SW7_3. 1 (default)	r
3	SW7_4	Reflects state of reserved switch SW7_4. 1 (default)	r
4...7	Reserved	Reserved	r

Rotary Switch Status Register

Table 40: *Rotary Switch Status Register*

Address: F1600011$_{16}$			
Bit	**Signal**	**Description**	**Access**
3...0	ROTARY_ SWITCH	Reflects current state of rotary switch. For the values, see Table 41 “Rotary Switch Settings” page 5-17.	r
4...7	Reserved	Reserved	r

The following table provides an overview of the rotary switch settings.

Table 41: *Rotary Switch Settings*

Register Contents	Rotary Switch	Register Contents	Rotary Switch
0_{16}	0000_2	8_{16}	1000_2
1_{16}	0001_2	9_{16}	1001_2
2_{16}	0010_2	A_{16}	1010_2
3_{16}	0011_2	B_{16}	1011_2
4_{16}	0100_2	C_{16}	1100_2
5_{16}	0101_2	D_{16}	1101_2
6_{16}	0110_2	E_{16}	1110_2
7_{16}	0111_2	F_{16}	1111_2

Switch 4 and 5 Status Register

Table 42: *Switch 4 and 5 Status Register*

Address: F1600012$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	SW_4_4	Reflects state of switch SW4-4 which is reserved. 0: Switch SW4-4 is set to ON. 1 (default): Switch SW4-4 is set to OFF.	r
1	SW_4_3	Reflects state of user flash write protection switch SW4-3. 0 (default): Flash write-protected 1: Flash not write-protected	r
2	TERM_SCSI1_ FRONT	Reflects state of SCSI 1 front panel termination 0: SCSI 1 front panel termination disabled 1 (default): SCSI 1 front panel termination enabled	r
3	IOBP_PRESENT#	Reflects whether an IOBP is present 0: IOBP is present 1 (default): IOBP is not present	r
4	Reserved	-	r

Table 42: *Switch 4 and 5 Status Register (cont.)*

Address: $F1600012_{16}$			
Bit	**Signal**	**Description**	**Access**
5	SW_6_2	Reflects state of Switch SW6-2 0 (ON): Board boots from TSOP PROM 1 (OFF): Board boots from PLCC PROM	r
6	SW_5_4	Reflects state of SCSI #2 manual termination switch. 0: SCSI termination disabled 1 (default): SCSI termination enabled	r
7	Reserved	Reserved	r

Switch 800 Status Register

Table 43: *Switch 800 Status Register*

Address: $F1600013_{16}$			
Bit	**Signal**	**Description**	**Access**
3...0	Reserved	Reserved	r
4	VSYS_ RESOUT	Reflects state of VMEbus SYSRESET output enable switch SW800-4. 0: VMEbus SYSRESET output disabled 1 (default): VMEbus SYSRESET output enabled	r
5	VSYS_RESIN	Reflects state of VMEbus SYSRESET input enable switch SW800-3. 0: VMEbus SYSRESET input disabled 1 (default): VMEbus SYSRESET input enabled	r
6	MAN_SLOT1	Reflects state of manual SLOT1 enable switch SW800-2. 0: Manual SLOT1 enable switch in ON position 1 (default): Manual SLOT1 enable switch in OFF position	r
7	AUTO_SLOT1	Reflects state of AUTO-SLOT1 enable Switch SW800-1. 0: AUTO-SLOT1 enable Switch in ON position 1 (default): AUTO-SLOT1 enable Switch in OFF position	r

Timer Register

In order to set a new initial timer value, the timer must be disabled. The registers described in the following section serve to control and monitor the timer and the timer status.

Timer Control Register

The SPARC / CPU-54 contains an interruptible timer used for real time operating systems.

The timer is implemented within the LCA and consists of five registers. The first register is used to control the timer status. Two additional registers are used for setting the initial timer value, and the last two registers are used to read the current value of the count down timer.

The timer counts down from its initial value to zero in steps of 10us. The initial value can be set by software from 1 to 65535 which results in a timer period of 10us to 655.35 ms. If the timer has reached zero, an interrupt is generated, if enabled, and the timer loads his initial value to count down again.

The following register is used to set up the timer.

Table 44: *Timer Control Register*

Address: F1600020$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	EN_TIM	Controls timer status. 1: Timer enabled 0: Timer disabled	r / w
1	IE_TIM	Enables interrupt timer. 1: Timer interrupt enabled 0: Timer interrupt disabled	r / w
2	IP_TIM	Reflects if timer interrupt occurred. 0: No timer interrupt pending 1: Timer interrupt pending	r
3	IC_TIM	Clears pending timer interrupt. 0: No function 1: Interrupt cleared	w
4...7	Reserved	Reserved	r

Timer Initial Control Register L

Table 45: *Timer Initial Control Register L*

Address: F1600024$_{16}$			
Bit	**Signal**	**Description**	**Access**
7...0	TINITL	Set lower byte of timer initial value	w

Timer Initial Control Register U

Table 46: *Timer Initial Control Register U*

Address: F1600025$_{16}$			
Bit	**Signal**	**Description**	**Access**
7...0	TINITU	Set upper byte of timer initial value TINITU_TINITL=0001$_{16}$ - timer period of 10µs TINITU_TINITL=FFFF$_{16}$ - timer period of 655.35µs	w

Timer Counter Status Register L

Table 47: *Timer Counter Control Register L*

Address: F1600026$_{16}$			
Bit	**Signal**	**Description**	**Access**
7...0	TCOUNTL	Provides lower byte of current timer value	r

Timer Counter Status Register U

Table 48: *Timer Counter Control Register L*

Address: F1600027$_{16}$			
Bit	**Signal**	**Description**	**Access**
7...0	TCOUNTU	Provides upper byte of current timer value	r

RS-422 Control and Status Register

The serial interfaces can be configured as RS-232 or RS-422 (factory option). The following register controls and monitors the interface mode.

Table 49: *RS-422 Control and Status Register*

Address: F160002A$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	REG_TTYA	Selects protocol of serial transceiver for TTYA. 0: RS-232 enabled 1: RS-422 enabled (factory option)	r / w
1	REG_TTYB	Selects protocol of serial transceiver for TTYB. 0: RS-232 enabled 1: RS-422 enabled (factory option)	r / w
2	SW_ OVERRIDE	Enables settings of bits 0 and 1 of the RS-422 Control and Status register. 0: Bit settings disabled 1: Value of bits 0 and 1 of RS-422 Control and Status register overrides value of hardware switches SW7-1 and SW7-2.	r / w
3...7	Reserved	Reserved	r

Ethernet Control and Status Register

This register is used to select the Ethernet connection for Ethernet interface 1. It is possible to make a connection to Ethernet interface 1 via the front panel or the backplane.

Table 50: *Ethernet Control and Status Register*

Address: F160002B$_{16}$			
Bit	**Signal**	**Description**	**Access**
0	ETH_CTRL0	Selects condition of Ethernet routing. ETH_CTRL0 is LSB	r / w
1	ETH_CTRL1	Selects condition of Ethernet routing. ETH_CTRL1 is MSB	r / w
2...7	Reserved	Reserved	r

The table below shows the selection for autodetect or fixed routing.

Bit (ETH_CTRL1, ETH_CTRL0)	**Description**
0 0	Autodetect
0 1	Fixed to front panel
1 0	Autodetect
1 1	Fixed to backplane

A

Troubleshooting

Dear Customer,

a typical VMEbus system is highly sophisticated. This chapter can be taken as a hint list for detecting erroneous system configurations and strange behaviors. It cannot replace a serious and sophisticated presales and postsales support during application development.

If it is not possible to fix a problem with the help of this chapter, contact your local sales representative or FAE for further support.

Problem	Possible Reason	Solution
Application software does not work	Memory ranges of system and peripheral boards do not match	Change application software so that memory ranges match I/O cards and host.
	Not enough disk capacity on mass storage device	Add disk capacity.
	Not enough system memory	Add system memory.
	Used I/O ranges do not match	Change application software so that I/O ranges match I/O cards and host.
Board does not boot	Boot device not partitioned according to used operating system	Check partition according to the operating system's needs.
	Boot sequence not correct	Correct the boot sequence.
	Interrupts not set correctly	Set interrupts correctly.
	Memory's timing parameters in firmware are outside specified ranges of used memory type	Set timing parameters correctly if configurable.
	Wrong configuration of boot devices	Configure boot devices correctly.
Board does not work	Backplane defect	1. Check VME slot position to be used for bent or broken pins. 2. Replace damaged backplane.
	Backplane voltages wrong or missing	1. Check that all backplane voltages are within their specific ranges. 2. Check that power supply is capable to drive the respective loads.
	Board defect	Replace board.
	Cables not connected	Connect all cables.
	Cables connected to wrong connector	Check if plug fits into connector. Reconnect all cables to right connectors.

Problem	Possible Reason	Solution
	Damaged plugs, bent or broken pins	Replace board.
Board functions do not work	Functions are disabled	Configure board correctly.
Board runs unstable	Disregard of environmental requirements	1. Check that temperature inside system stays within specified ranges for all system devices. 2. Check for hot spots within system. Improve cooling system if necessary. 3. Check that other environmental values like moisture or altitude are kept within specified ranges.
Connected devices do not work	Backplane voltages for device not within the specified range	1. Check that all backplane voltages are within their specific ranges. 2. Check that power supply is capable to drive the respective loads.
	Device defect	Replace device.
	Device not connected to power supply	Connect device to power supply.
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective device.
Devices collide with each other	Devices might have been moved to wrong address location.	Configure board / devices correctly.
Low system performance	Caches disabled	Enable caches.
Memory / PMC Module does not work	Module defect	Replace module.
	Module not defined for the used board	1. Check if module specification matches interface specification of board. 2. Replace module if specifications do not match.
	Module not installed correctly	Check if module fits perfectly in socket.
	Wrong board configuration, faulty switch setting	Configure the board correctly for the respective module.
Operating system runs unstable.	Drivers are missing, faulty or do not match hardware.	1. Check that all used hardware parts have a driver matching the hardware. 2. Reinstall hardware drivers.

Problem	Possible Reason	Solution
IOBP does not work.	IOBP defect	Replace IOBP.
	IOBP installed on wrong slot position	Install IOBP on adjacent slot position of the used board.
	IOBP not defined for the used peripheral or system board	Install IOBP defined for the used peripheral or system board.
System shuts down unexpectedly	Solaris 8 version 4/01 and later performs a regular and automatic shutdown if a VME read error (e.g. bus time-out) occured.	Install Solaris 8 kernel patch 108528-12 or higher available from SUN Microsystems. For installation instructions, refer to the README file contained in the zipped file.

B

Battery Exchange

Dear Customer,

the battery provides data retention of five years summing up all periods of actual data use. Force Computers therefore assumes that there usually is no need to exchange the battery except for example in case of long-term spare part handling.

Caution



- **Incorrect exchange of lithium batteries can result in a hazardous explosion.**
- **Exchange battery before five years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of lithium battery as is already installed.**

In order to exchange the battery, follow the instructions below:

1. If battery is covered by PMC module or memory module, remove module first

Caution



In order to prevent the PCB or the battery holder from being damaged, do not use a screw driver to remove the battery from its holder.

2. Exchange battery
3. When installing new battery, ensure that battery connectors fit sockets on CPU board
4. Install battery in such a way that the dot marked on top of battery covers dot marked on chip.
5. If necessary, reinstall PMC module or memory module in correct position

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Product Error Report

Product:	Serial No.:
Date Of Purchase:	Originator:
Company:	Point Of Contact:
Tel.:	Ext.:
Address:	
Present Date:	
Affected Product: ❑ Hardware ❑ Software ❑ Systems	Affected Documentation: ❑ Hardware ❑ Software ❑ Systems
Error Description:	

This Area to Be Completed by Force Computers:

Date:

PR#:

Responsible Dept.: ❑ Marketing ❑ Production

Engineering ➠ ❑ Board ❑ Systems

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