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Datasheet

June 2000

MB86060

Version 1.1

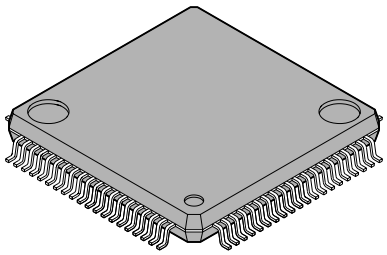
16-Bit Interpolating Digital to Analog Converter

FME/MS/SFDAC1/DS/4250

The Fujitsu MB86060 is a high performance 12-bit, 400MSa/s digital to analog converter (DAC) enhanced with a 16-bit interpolation filtering front-end. Use of novel techniques for the converter architecture delivers high speed operation consistent with BiCMOS or bipolar devices but at the low power of CMOS. Fujitsu's proprietary architecture is the subject of several patent applications. Additional versatility is provided by selectable input interpolation filters, programmable dither and noise shaping facilities. Excellent SFDR performance coupled with high speed conversion rate and low power make this device particularly suitable for high performance communication systems, in particular direct IF synthesis applications.

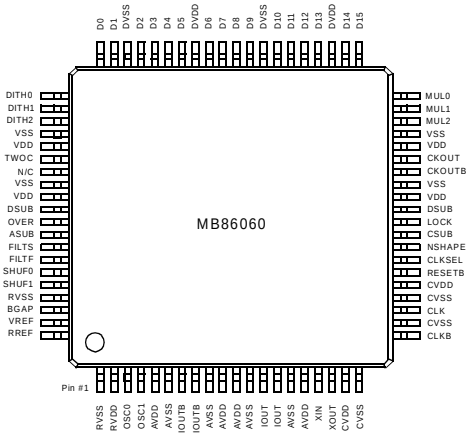
PLASTIC PACKAGE

LQFP-80



(FPT-80P-M05)

PIN ASSIGNMENT



Features

- 16-bit Interpolating Digital to Analog conversion
- x2 or x4 interpolation filtering
- 100MSa/s input, with x4 interpolation enabled
- Programmable highpass filtered dither
- Selectable 2nd order noise shaping
- Versatile CMOS digital interface
- Internal programmable clock multiplier
- Low power, 3.3V operation (343mW @32MSa/s input, x4)
- Performance enhanced pinout with on-chip decoupling
- 0.35µm CMOS technology with Triple Well
- Industrial temperature range (-40°C to +85°C)

Applications

- Direct IF Synthesis
- Cellular basestations
- Wide-band communication systems

This product has Patents applied for in the US and elsewhere including GB2333191A, EP0935345A, JP11-274934A, GB2333171A, EP0930717A, JP11-274935A, GB2333190A, EP0929158A, JP11-243339A, GB2335097A, EP0940923A, JP11-317667A, GB2335076A, EP0940852A, JP11-251530A.

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1 Functional Description

The MB86060 integrates a 12-bit 400MSa/s DAC core with selectable front end processing to provide input interpolation filtering, dither and noise shaping. Versatile interfacing via the 16-bit parallel CMOS data input allows different system requirements to be accommodated, with either offset binary or 2's complement data formats selected by an input format control.

The device is manufactured in a 0.35µm advanced CMOS process with Triple Well extension giving improved isolation between analog blocks and digital-analog.

A functional block diagram is shown in Figure 1.

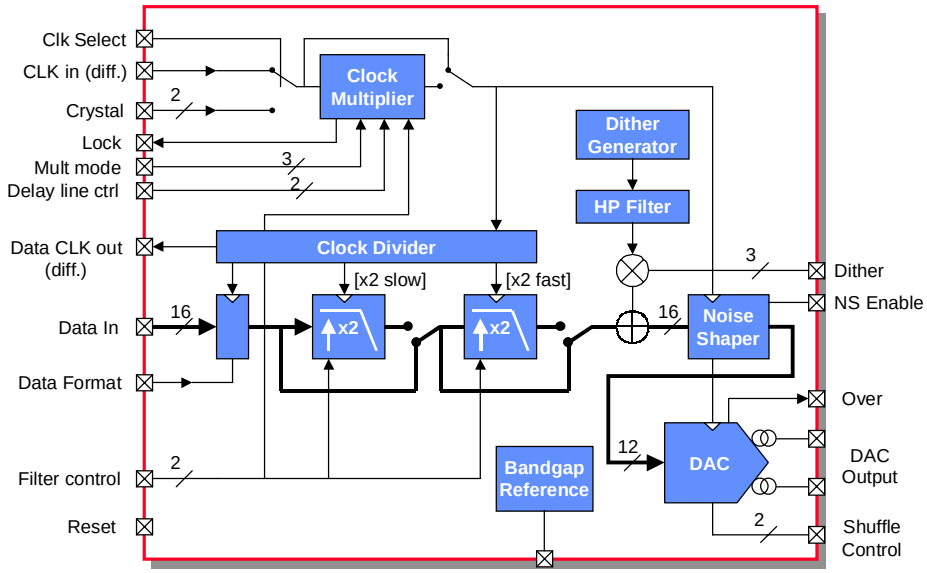


Figure 1 MB86060 Functional Block Diagram

1.1 Operating Modes

The device can be configured into a number of different operating modes, depending on which clock source and interpolation filtering mode is selected. The tables below summarise the MB86060 operating modes according to clock multiplier and interpolation filtering configuration.

- x1 Interpolating filters disabled, effectively a conventional 12-bit DAC for up to 200MSa/s
- x2 [slow] First interpolating filter only, used for generating 0~43MHz, assuming 100MSa/s data
- x2 [fast] Second interpolating filter only, used for generating 0~74MHz, assuming 200MSa/s data
- x4 Full interpolation, for generating 0~43MHz with 100MSa/s data & maximum DAC rate

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1.2 Clock

The MB86060 incorporates a clock multiplier to generate the required internal x1, x2 and x4 clock signals from an external reference. The clock multiplier is based on a delay-lock-loop whose delay is adjusted by a charge pump controlled by a phase detector. A 'Lock' indicator is provided so that the a system can monitor the multiplier's condition. For systems where a high frequency clock is available, or the lowest possible jitter is required, then the clock multiplier may be disabled and the external clock used directly.

The input clock is selectable between either a differential system clock, typically a sine wave source of amplitude 0dBm, or an external crystal using the internal oscillator circuit. A CMOS single ended clock can also be connected to XIN. See Table 1.

Table 1 Input Clock Source Selection

CLKSEL	Clock multiplier mode	Clock source	Function
0	x1 (Either filter enabled) or x2 to x8	Crystal oscillator	Connect crystal between XIN and XOUT, or connect CMOS clock to XIN
1	Any	Differential clock	Connect differential clock source to CLK and CLKB

When using the internal oscillator with an external crystal, or connecting a single-ended CMOS clock to XIN, the clock multiplier must be set to multiply modes x2 to x8 so that XIN is enabled. The operating speed of the internal crystal oscillator is limited. See section 5.5.

If minimum jitter is required, then the differential clock should be used, with an amplitude sufficient to ensure that the specification for minimum slew rate is met. For a 250MHz clock this represents 0dBm, with higher amplitudes required for lower clock rates. A sine signal is recommended over a square wave to avoid unwanted harmonics.

1.2.1 Clock Multiplier Modes

The clock multiplier can be set in one of eight modes. These take the form of two basic groups, either multiplier functioning or bypassed.

With the multiplier in bypass mode, MUL[2:0] = 000, then the clock frequency applied at CLK in, (F_{IN}), will be the update frequency used by the DAC core, (F_{DAC}). The frequency available at Data CLK out, (F_{DATA}), will be dependant on the interpolation filter settings. If no filters are selected, then $F_{DATA} = F_{DAC}$. If the x2 filter, slow or fast, is selected, then $F_{DATA} = F_{DAC}/2$. If x4 filtering is selected, then $F_{DATA} = F_{DAC}/4$.

With the multiplier modes x1 to x8, MUL[2:0] = 001 to 111, then the clock frequency applied at CLK in, (F_{IN}), will be multiplied by the chosen clock multiplier setting, and this will be the frequency available at Data CLK out, (F_{DATA}). The update frequency used by the DAC core, (F_{DAC}) will then depend on the interpolation filter settings. If no filters are selected, $F_{DAC} = F_{DATA}$. If the x2 filter, slow or fast, is selected, then $F_{DAC} = 2.F_{DATA}$. If x4 filtering is selected, then $F_{DAC} = 4.F_{DATA}$. Hence the DAC core sampling rate will be between $1xF_{IN}$ and $32xF_{IN}$.

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The OSC[1:0] setting controls the delay response within the delay-lock-loop. Different settings are required to enable best jitter performance to be achieved and should be set according to the DAC clock rate being used.

Table 2 Clock Multiplier Configuration

Data CLK out (F_{DATA})†	MUL[2:0]	Clock multiplier	CLK in (F_{IN})
F_{DATA} MHz	000	Bypass	F_{DAC}‡
F_{DATA} MHz	001	x1	F_{DATA}
F_{DATA} MHz	010	x2	F_{DATA} / 2
F_{DATA} MHz	011	x3*	F_{DATA} / 3
F_{DATA} MHz	100	x4	F_{DATA} / 4
F_{DATA} MHz	101	x5*	F_{DATA} / 5
F_{DATA} MHz	110	x6	F_{DATA} / 6
F_{DATA} MHz	111	x8	F_{DATA} / 8

OSC[1:0]	Mode	DAC Clk (F_{DAC}) (min)	DAC Clk (F_{DAC}) (max)
00	Fastest	250 MHz	
01		150 MHz	250 MHz
10		80 MHz	150 MHz
11	Slowest		80 MHz

† Limits on Data CLK out apply. Refer to Interpolation Filter configuration table

‡ See Table 3

*Note: Clock Multiplier modes x3 and x5 are implemented with a multiply by 6 and divide by 2, and a multiply by 10 and divide by 2, respectively. Ensure that OSC[1:0] is set for the clock frequency produced by the x6 or x10 multiplication. F_{DAC} (max) will apply to the multiplication frequency.

Table 3 DAC Core Clock Configuration

Data CLK out†	FILTF	FILTS	Filter mode	DAC Clk‡ (F_{DAC})
F_{DATA} MHz	0	0	Disabled	F_{DATA} MHz
	0	1	x2 slow	2.F_{DATA} MHz
	1	0	x2 fast	2.F_{DATA} MHz
	1	1	x4	4.F_{DATA} MHz

† Data CLK should not exceed limits for F_{DATA}

‡ DAC Clk should not exceed limits for F_{DAC}

F_{DATA} Frequency of Data presented to the device. Available at Data CLK out.
F_{DAC} Frequency that the DAC core is updating at. Not available externally.
F_{IN} Frequency of the reference source applied to CLK.

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1.2.2 Multiple Device Clock Synchronisation

To allow multiple devices to be used with a common clock source, a clock synchronization function is included. This will ensure that the clock out to clock in phase relationship is maintained.

With the clock multiplier disabled, the clock in (CLK in) signal bypasses the clock multiplier block and is connected directly to the clock divider. The divider generates clock out (Data CLK) depending upon the interpolation filter settings. The phase relationship between clock out and clock in will be maintained by the simultaneous release of a *FULL-RESET* on all devices. See section 1.11.

With the clock multiplier enabled, the clock in (CLK In) signal is routed through the multiplier block before connecting to the clock divider. The multiplier block maintains the phase relationship between clock in and clock out by producing a re-synchronization pulse which locks clock out to clock in.

1.2.3 Clock Out

A differential clock out (Data CLK) signal is available to act as a reference to clock data into the device. Data CLK is available on CKOUT and CKOUTB. These pins have a nominal output resistance of 25Ω each, and are designed to drive a bridged load to reduce the effect of package inductance. The output waveform will be a square wave.

1.3 Interpolating Filters

The interpolating filters are configured as two cascaded, independently selectable low-pass stages. The first filter being slower with sharp roll-off, and the second faster but with relaxed roll-off. It is important to note that when the interpolation stages are not selected they are not clocked, significantly reducing the power consumption for either x2 or x1 modes, compared to x4.

Table 4 Interpolating Filters

Slow Filter	Fast Filter	Reduction in Q noise Noise Shaping disabled	Reduction in Q noise Noise Shaping enabled
Disabled	Disabled	N/A	N/A
Enabled	Disabled	3dB	5dB
Disabled	Enabled	3dB	5dB
Enabled	Enabled	6dB	22dB

Further information on the interpolating filters, including frequency response, is given in Section 2.

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1.4 Programmable Dither

Dither can be added to improve low-level performance and reduce effects due to nonlinearities within the DAC, and reducing DNL and glitch energy. The dither has programmable amplitude, see Table 5, and is high pass filtered to fall out of the pass band.

Table 5 Programmable Dither

Dither Setting			Dither Amplitude	
DITH2	DITH1	DITH0	rms	peak
0	0	0	Disabled - no dither added	
0	0	1	-33.6 dBFS (480 $LSBs_{16}$)	-27.0 dBFS (1458 $LSBs_{16}$)
0	1	0	-27.6 dBFS (960 $LSBs_{16}$)	-21.0 dBFS (2916 $LSBs_{16}$)
0	1	1	-21.6 dBFS (1920 $LSBs_{16}$)	-15.0 dBFS (5832 $LSBs_{16}$)
1	0	0	-15.6 dBFS (3840 $LSBs_{16}$)	-9.0 dBFS (11664 $LSBs_{16}$)
1	0	1	-9.6 dBFS (7680 $LSBs_{16}$)	-3.0 dBFS (23328 $LSBs_{16}$)
1	1	0	Reserved for factory use only	
1	1	1	Reserved for factory use only	

The frequency characteristics of the added dither is illustrated in Section 3.

1.5 Noise Shaping

Second order noise shaping can be applied to interpolated data prior to being passed to the DAC core. When enabled this provides an additional reduction in quantisation noise to that gained through the use of interpolation filtering. For the x4 interpolation mode this improvement will be 16dB, equivalent to 2.7 bits.

1.6 Converter Architecture

The MB86060 interpolating DAC incorporates a number of novel design aspects that are subject to patent applications. Key to its operation are the current sources where segmented, common centroid, interleaved techniques for the most significant bits, as well as load matching ensure good linearity and low distortion to at least the 12-bit level. In the switch elements tracking capacitance is minimised to improve settling, while controlled rise and fall times improve SFDR performance. Finally the digital decoding uses a 3-dimensional addressing approach to minimise propagation delays from latch to element.

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1.6.1 Segment Shuffling

The DAC core incorporates a proprietary segment shuffling capability which is provided to further improve linearity, and hence improve SFDR. This feature reduces any signal level dependent effects on linearity as the same code can be generated by the same number of MSB cells but taken from any quarter of the MSB segments. Segment shuffling can be selected to operate every 4, 8 or 16 updates of the DAC output using a random shuffle sequence between the four segments A, B, C and D. See Figure 2. Most performance improvement will be observed when the device is used in one of the interpolating modes. The effect of segment shuffling is to produce a spread noise spectrum, raising the overall noise floor, but reducing the distortion. For minimum distortion when generating low frequency signals, it is recommended that the shuffling clock rate is no more than 25MHz (F_{DAC} / Segment Shuffling setting). See Table 5. However, low shuffle clock rates give reduced spreading out of distortion components.

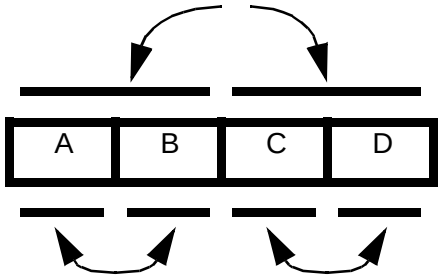


Figure 2 Segment Shuffling

Table 6 Segment Shuffling Control

Mode	SHUF1	SHUF0	Segment Shuffling	Note
0	0	0	Segment Shuffling disabled	Lowest noise
1	0	1	Random - every 4 cycles	$F_{DAC} \leq 100$ MSa/s
2	1	0	Random - every 8 cycles	$100 \leq F_{DAC} \leq 200$ MSa/s
3	1	1	Random - every 16 cycles	$200 \leq F_{DAC}$ MSa/s

1.6.2 Converter Overload

Within the front end digital processing there is no automatic protection against converter overload except for clipping at 12-bit FSD. Warning of 12-bit overload at the input to the DAC is provided by the ‘OVER’ status pin. Conditions where care must be taken to avoid problems due to overload would include input signal level when high levels of dither is selected, and fast edge input data where inevitable overshoot in the digital filters occurs.

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1.7 Voltage Reference

A 1.25V bandgap reference is provided on-chip, although this may be bypassed where an external reference is to be used. To use the internal bandgap reference pins BGAP and VREF should be linked via a 50Ω resistor, or smaller if better rejection of reference noise at low frequencies is required. VREF should be decoupled to Reference Ground (RVSS) with a 100nF capacitor. For maximum accuracy an external voltage reference is recommended

1.8 Analog Output

The DAC output is a differential current type. A termination resistor should be used appropriate for the maximum allowable output swing. A power down control places the analog circuitry in a low power state, switching off the current output drive and reference circuitry. When power down mode is selected the device enters its reset state setting the input data code to +1/2 in 2's complement or 0 in unsigned binary.

Table 7 Full Scale Code Representation

2's Complement				Unsigned Binary			
Code		IOUT	IOUTB	Code		IOUT	IOUTB
+32767	0111111111111111	$^{65}/_{64}.I_{FS}$	$^{1}/_{64}.I_{FS}$	65535	1111111111111111	$^{65}/_{64}.I_{FS}$	$^{1}/_{64}.I_{FS}$
:	:	:	:	:	:	:	:
0	0000000000000000	$^{33}/_{64}.I_{FS}$	$^{33}/_{64}.I_{FS}$	32768	1000000000000000	$^{33}/_{64}.I_{FS}$	$^{33}/_{64}.I_{FS}$
:	:	:	:	:	:	:	:
-32768	1000000000000000	$^{1}/_{64}.I_{FS}$	$^{65}/_{64}.I_{FS}$	0	0000000000000000	$^{1}/_{64}.I_{FS}$	$^{65}/_{64}.I_{FS}$

1.8.1 Analog Output Reference Resistor

From the voltage reference a control loop defines the current through an external resistor, Rref, where the current in the reference resistor is 4 times the internal segment current, and the full scale output current is defined as,

$$I_{OP} = \left(63\frac{63}{64}\right) \times \left(\frac{Vref}{4 \times Rref}\right) \approx 16 \cdot I_{ref}$$

therefore,

$$R_{ref} = \frac{16 \times V_{ref}}{I_{OP}}$$

e.g. Using a 1.25V $V_{ref.}$, to give a 20mA full scale output => R_{ref} = 1kΩ

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1.8.2 Analog Output Scaling

Power savings can be made by reducing the full scale analog output current (I_{OP}) by increasing R_{ref}. However, to maintain the specified performance, I_{OP} should be programmed to 20mA, and the digital data should be pre-scaled to achieve full scale deflection at an output current lower than full scale (I_{OP}).

1.8.3 Analog Output Pins

The analog outputs, IOUT and IOUTB, are each connected to two pins to reduce output inductance. These pins should be directly connected together on the PCB.

1.9 Digital Data Interface

16-bit digital data is input through pins D[15:0]. D15 is the MSB. Data may be presented in either Unsigned Binary or 2's Complement format, depending upon the setting of the TWOC pin. See Table 8.

Table 8 Digital Data Format Control Pin Function

TWOC	Digital Data Format
0	Unsigned Binary
1	2's Complement

Note: The Digital Data interface has CMOS inputs. The voltage levels of the input data must not exceed the specifications in section 5.2. Data from a 5V source must not be presented directly to the Digital Data Interface.

1.9.1 Data Timing

Data should be clocked into the device with the rising edge of the Data CLK signal. The timing relationship between the rising edge of Data CLK and the setup and hold times for Data In, forms an 'eye' opening, within which data may be presented to the Digital Data Interface. If data is presented outside of this 'eye', significant distortion will occur. See Figure 9.

1.10 Power Supplies

Separate power and ground supplies are used for both digital data and digital control, analog, reference and clock circuits. A low jitter supply, free from data dependent signals is required by the clock domain. A supply with low clock and data noise is required for the analog domain. The clock, digital interface, analog and reference circuitry are all implemented using Fujitsu's Triple-Well extension to the standard CMOS process to provide the necessary electrical isolation. Individual substrate connections are provided to analog, digital and clock domains.

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1.10.1 Substrate Connections

Connections to the analog, digital interface, and clock section substrates are provided. These pins would typically be directly connected to the main digital ground (VSS), so as to direct any noise that has been collected by the substrates away from the analog blocks.

1.10.2 Power Dissipation

The power dissipation, P_D, is dependant on specific operating conditions: supply voltage (V_{DD}), full scale output current (I_{OP}), DAC output update rate (F_{DAC}) and input data waveform. Equations for calculating power dissipation in certain conditions are given in section 5.3.

Depending on these factors, applications requiring high F_{DAC} frequencies and/or extended lifetime at ambient temperatures >70^{0}C may need additional cooling.

1.10.3 Pinout

The MB86060 features a performance enhanced pinout to gain the maximum performance from the PCB. Ground connection pins are provided adjacent to clock in, clock out and analog out pins to minimise the loop inductance of the return current path. All critical power supplies are paired on adjacent pins to minimise the decoupling loop inductance, and small value decoupling is provided on-chip. Discrete decoupling, typically 100nF, must be provided for each power supply pin pair. See Section 6.

1.11 Reset

A RESETB pin is provided, which when taken low allows the device to be reset and placed in a low power state. There is a two cycle latency requiring the device to be clocked in order to reset the device. On power up the device must be reset before it is operational. Multiple device clock synchronization (see section 1.2.2), and configuration changes require a device reset to be performed.

There are two reset modes available determined by the state of the TWOC pin. If TWOC is held low while RESETB is taken low then a *PARTIAL-RESET* is performed. This will reset and place in a low power state all sections of the device except the Clock Multiplier and Voltage Reference sections. If TWOC is held high while RESETB is taken low, a *FULL-RESET* is performed. This will reset and place in a low power state all sections of the device.

Table 9 Reset Modes

TWOC	RESETB	Function	Sections Reset
0	1 > 0	*PARTIAL-RESET*	All sections except Clock Multiplier and Voltage Reference
1	1 > 0	*FULL-RESET*	All sections

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2 Interpolating Filters

The integration of interpolating filters provides a number of benefits to the system implementation. In general, improved performance can be gained by using a higher DAC conversion rate effectively providing a higher level of oversampling from the generated signal. For the designer, the problem with this approach is generating the required high speed digital data, especially when considering high performance wide-band designs with up to 50MHz of signal. Integrating this processing on-chip with the DAC alleviates this problem for the designer.

Other benefits include a reduced effect due to the sinx/x roll-off due to the DAC S&H output stage, which for a conventional DAC represents -4dB at Nyquist, compared to only -0.22dB when operating in the x4 interpolating mode. Also the digital interpolation filters sharp cutoff and effective stop-band attentuation improves both in and out-of-band SFDR. This is illustrated in Figure 3.

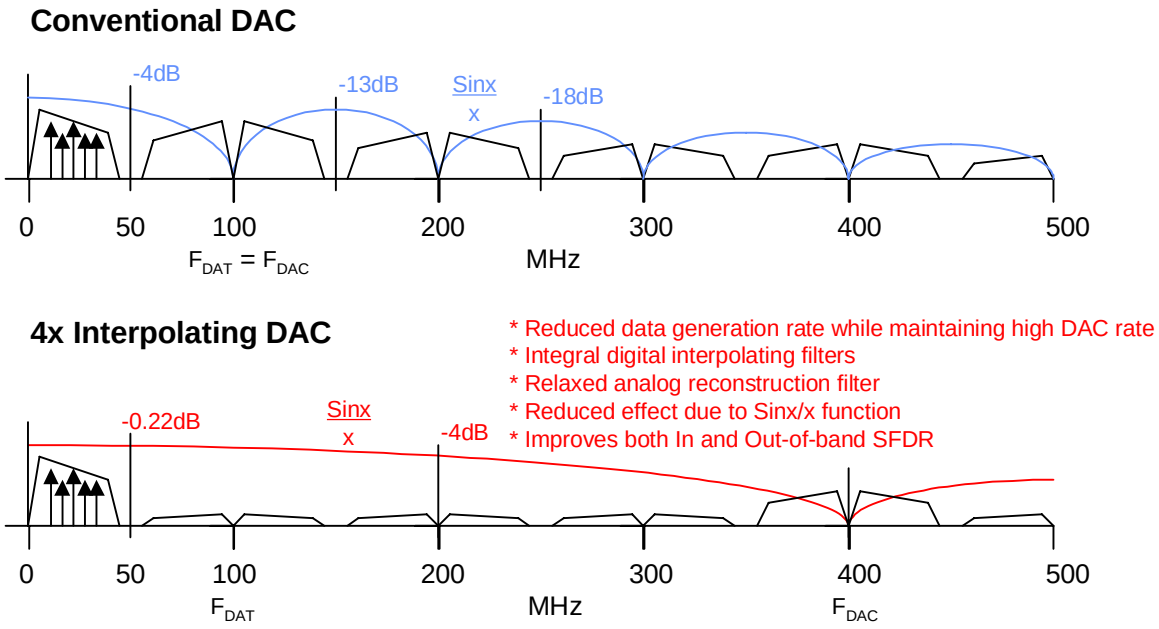


Figure 3 Benefits of Interpolating Filters

The MB86060 features four interpolation filter modes x1, x2(slow), x2(fast) and x4. x1 is as per a conventional DAC, and choosing between the remaining three modes would depend on the system requirements. x2(slow) may be advantageous to a system requiring the benefits of interpolation filtering but saving some power by not running the DAC core at full rate. x2(fast) gives access to the wider band, slower

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roll-off interpolation filter allowing wider band signals to be generated compared to the other modes, for example 74MHz (-0.1dB) for 200MSa/s data rate. x4 for the complete interpolation filter operation. These different modes are illustrated in Figure 4.

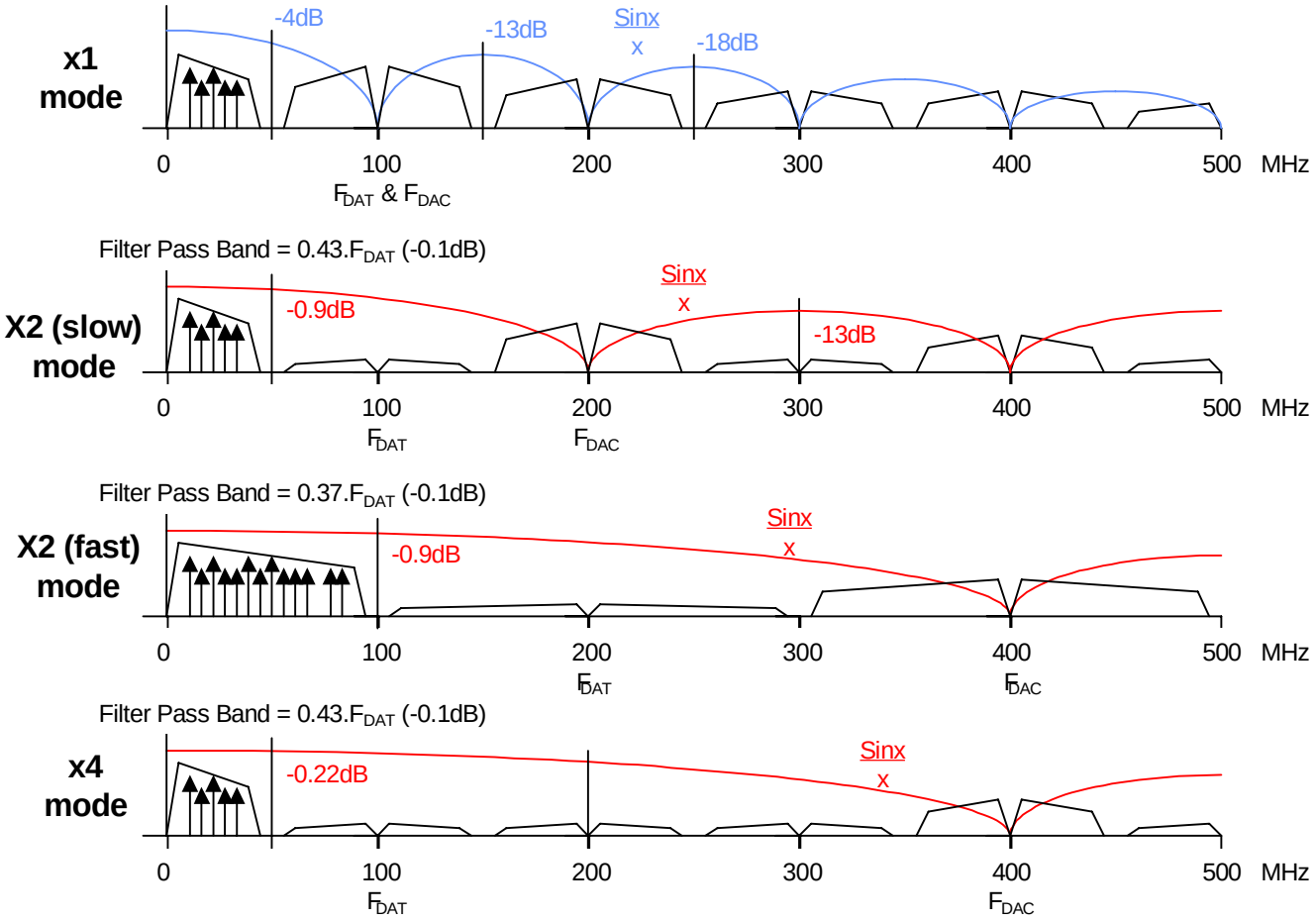


Figure 4 Interpolating Filter Modes

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x2 Slow Filter

Pass Band 0.43fs (-0.1dB)
Stop Band -75dBFS from 0.59fs
[note: Frequency axis normalised to input data rate]

x2 Fast Filter

Pass Band 0.74fs (-0.1dB)
Stop Band -83dBFS from 1.54fs
[note: Frequency axis normalised to input data rate for x4 interpolation mode. With only x2 Fast selected then the input data rate is normalised to 2.0 Frequency]

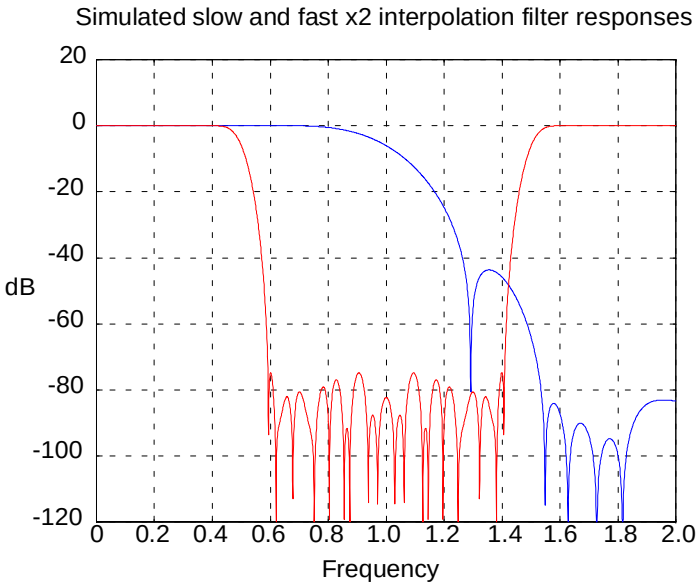


Figure 5 Slow & Fast Filter Characteristics

Combined Filters, x4 Mode

Pass Band 0.43fs (-0.1dB)
Stop Band -75dBFS from 0.59fs -
(excluding transition band at around 1.5fs)

[note: Frequency axis normalised to input data rate]

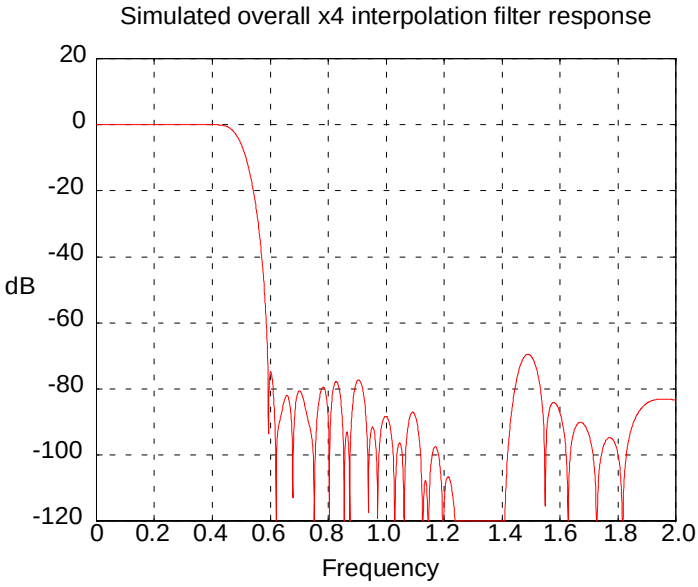


Figure 6 Combined Filter Characteristics

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3 Dither Frequency Spectrum

The use of dither in data converter applications is not uncommon, where improvements in low-level performance and reduced effects due to nonlinearities can be achieved. For dither to be used effectively both amplitude and frequency characteristics must be carefully considered. Obviously the dither amplitude should be larger than the nonlinearities to be masked, but levels significantly larger than this will ultimately limit available dynamic range for the wanted signal. Similar considerations should be made for the frequency characteristics, which in the MB86060 the dither is highpass filtered such that the majority of the energy is concentrated at Nyquist of the DAC output rate.

In many systems a simple calculation can be used to determine the maximum input signal level for a given dither amplitude, and in most applications this applies. However, in multi-tone systems such as discrete multi-tone (DMT) or multi-channel communication systems a more statistical approach may be adopted where the probability of converter overloads occurring is considered.

The frequency characteristics of the highpass filtered dither is shown in Figure 6.

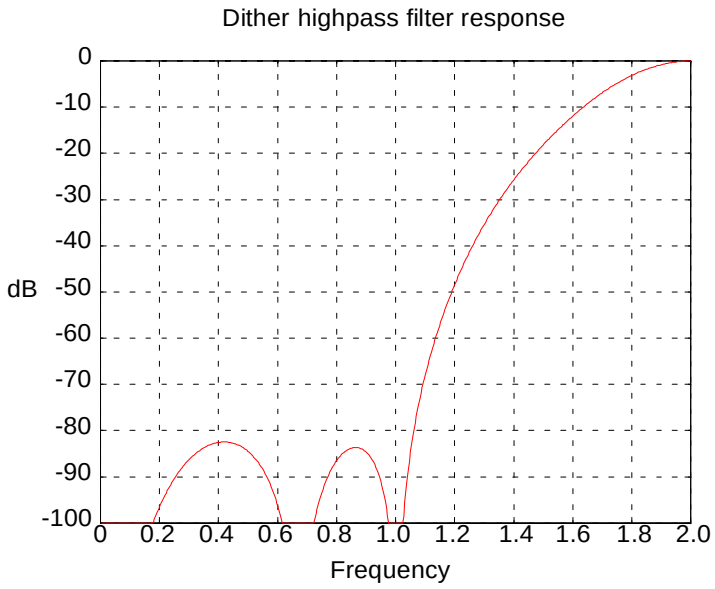


Figure 7 Dither Frequency Characteristics

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4 Timing Diagrams

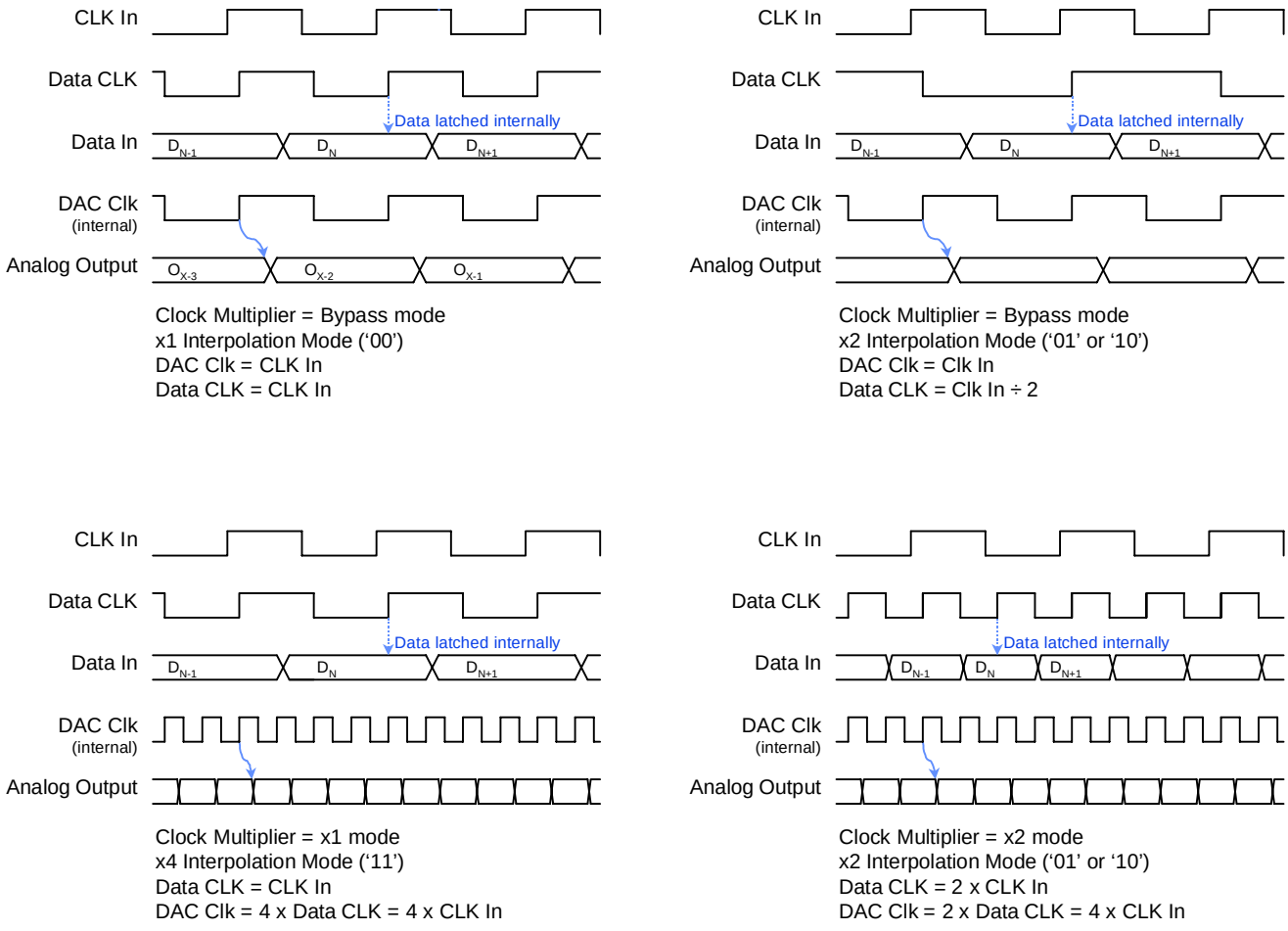
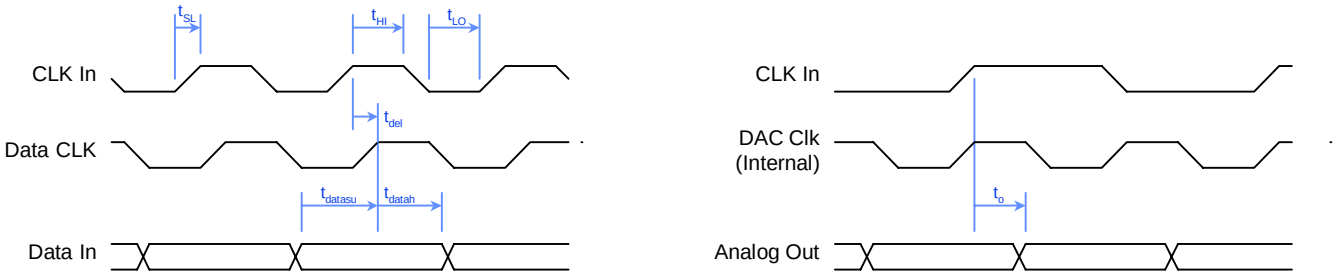


Figure 8 Functional Timing of the DAC in Relation to CLK In

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Clock Multiplier = Bypass mode
x1 Interpolation Mode ('00')
CLK In = Data CLK

Clock Multiplier = x2 mode
x1 Interpolation Mode ('00')
DAC Clk = 2 x CLK In

Figure 9 CLK In to Analog Out, Data CLK and Data In Timing

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5 Electrical Specifications

5.1 Absolute Maximum Ratings

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Supply voltage		V_{DD}	-0.5	3.3	3.6	V
Input voltage	1	V_{IL}	-0.5		V_{DD}+0.5	V
Output current	2	I_O		+20	+21	mA
Storage temperature		T_{ST}	-40	25	+125	^oC
T_{OP}(min) to T_{OP}(max), VDD = RVDD = AVDD = CVDD = +3.3V, VSS = RVSS = AVSS = CVSS = 0V, I_{FS}=20mA, Differential Transformer coupled output, 50Ω doubly terminated, unless otherwise specified. 1. IOUT & IOUTB VSS - 1.0 to VDD + 0.5 2. For 1 second per pin						

CAUTION
ELECTROSTATIC DISCHARGE SENSITIVE DEVICE

High electrostatic charges can accumulate in the human body and discharge without detection. Ensure proper ESD procedures are followed when handling this device.

5.2 Digital Interface Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
CMOS inputs						
High-level input voltage		V_{IH}	2.3		V_{DD}	V
Low-level input voltage		V_{IL}	V_{SS}		1.0	V
High-level input current		I_{IH}	-10		+10	µA
Low-level input current		I_{IL}	-10		+10	µA
Input capacitance				5		pF
Data inputs						
Setup time		t_{datasu}		1.0		ns
Hold time		t_{datah}		1.2		ns
CMOS outputs						
High-level output voltage		V_{OH}	2.9		V_{DD}	V
Low-level input voltage		V_{OL}	V_{SS}		0.4	V
T_{OP}(min) to T_{OP}(max), VDD = RVDD = AVDD = CVDD = +3.3V, VSS = RVSS = AVSS = CVSS = 0V, I_{FS}=20mA, Differential Transformer coupled output, 50Ω doubly terminated, unless otherwise specified.						

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5.3 DC Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
DC Accuracy						
Integral Non Linearity (Shuffle Off)		INL		10	20	LSB_{16}
Differential Non Linearity (Dither Off)		DNL		5	10	LSB_{16}
Analog output						
Full scale output current		I_{OP}		20		mA
Output resistance				100		kΩ
Output capacitance				15		pF
Gain error			-1		+1	%FS
Output voltage (compliance)			-1		1	V
CLK In to Analog Out delay						
x1 Interpolation		t_o		6		ns
x2 Interpolation		t_o		6		ns
x4 Interpolation		t_o		6		ns
Bandgap Reference						
Reference voltage		V_{BG}	1.19	1.25	1.31	V
Reference output current		I_{BG}	5		20	mA
Reference Input						
Reference voltage		V_{REF}	1.19	1.25	1.31	V
Reference input current		I_{BG}	-1		+1	µA
Power Dissipation	1, 2, 3	P_D				
32MSa/s input, x1 interpolation				131		mW
100MSa/s input, x1 interpolation				201		mW
32MSa/s input, x4 interpolation				343		mW
100MSa/s input, x4 interpolation				863		mW
Maximum power dissipation				1079		mW
Power down current				<1		mA
Ambient Temperature		T_A	-40	25	+85	°C
Junction Temperature		T_J			+110	°C

T_{OP}(min) to T_{OP}(max), VDD = RVDD = AVDD = CVDD = +3.3V, VSS = RVSS = AVSS = CVSS = 0V, I_{FS}=20mA, Differential Transformer coupled output, 50Ω doubly terminated, unless otherwise specified

1. Nominal power dissipation (with no filters enabled) P_D = 99 + (102 per 100MSa/s) (mW) approx.
2. Nominal power dissipation (with both filters enabled, clock multiplier bypassed) P_D = 99 + (191 per 100MHz(F_{DAC})) (mW) typ.
3. Nominal power dissipation (with both filters and ditherer enabled, clock multiplier bypassed) P_D = 99 + (245 per 100MHz(F_{DAC})) (mW) typ.

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5.4 AC Specifications

Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Signal to Noise Ratio	1	SNR				
Range DC to 50MHz, F_{DAC} = 400 MSa/s, x4 Interpolation mode, Noise Shaping enabled, Dither disabled						
2MHz tone, Segment Shuffling - Off				90		dB
2MHz tone, Segment Shuffling - On				80		dB
Total Harmonic Distortion	1	THD				
Range DC to 50MHz, F_{DAC} = 400 MSa/s, x4 Interpolation mode, Noise Shaping enabled, Dither disabled						
2MHz tone, Segment Shuffling - Off				80		dB
2MHz tone, Segment Shuffling - On				90		dB
20MHz tone, Segment Shuffling - Off				65		dB
20MHz tone, Segment Shuffling - On				76		dB
Spurious Free Dynamic Range	1	SFDR				
Single tone at -1dBFS, F_{DAC} = 200MSa/s, range DC to 100MHz						
2MHz tone, Segment Shuffling - Off				83		dBc
2MHz tone, Segment Shuffling - On				93		dBc
15MHz tone, Segment Shuffling - Off			65	70		dBc
15MHz tone, Segment Shuffling - On				83		dBc
4-tones at -15dBFS, F_{DAC} = 200MSa/s, x4, range DC to 100MHz						
19.1, 19.3, 19.7, & 19.9MHz tones, missing centre tone						
Spurious tone @ 19.5MHz, Segment Shuffling - Off				88		dBFS
Spurious tone @ 19.5MHz, Segment Shuffling - On				95		dBFS
17.5 - 21.5MHz, Segment Shuffling - Off				89		dBFS
17.5 - 21.5MHz, Segment Shuffling - On				97		dBFS
Adjacent Channel Power Ratio	1	ACPR				
4MHz BW, 5MHz ch spacing,						
16MHz centre frequency, 64MSa/s, F_{DAC}=256MSa/s				80		dBc
32MHz centre frequency, 128MSa/s, F_{DAC}=256MSa/s				74		dBc

T_{OP}(min) to T_{OP}(max), VDD = RVDD = AVDD = CVDD = +3.3V, VSS = RVSS = AVSS = CVSS = 0V, I_{FS}=20mA, Differential Transformer coupled output, 50Ω doubly terminated, unless otherwise specified

1. Clock mode = '000' (Clock multiplier bypassed)

Spurious Free Dynamic Range (SFDR) is defined as the highest spurious product (harmonic or non-harmonically related) within a defined bandwidth while generating a test tone or tones (multi-tone test). SFDR varies with amplitude and frequency of the test tone(s) and should either be quoted as the difference between the tone and highest spurious component (dBc) or referenced to full scale (dBFS). In both cases the test tone amplitude and frequency should be quoted as well as the measurement bandwidth. The measurement bandwidth is typically regarded as DC to Nyquist (of the input data rate where interpolating modes are selected) but occasionally systems will specify an appropriate narrow band.

Adjacent Channel Power Ratio (ACPR) relates to the ratio of power in an adjacent band compared to that in a wanted transmit band, where channel bandwidth and channel spacing should be quoted.

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5.5 Clock Specifications

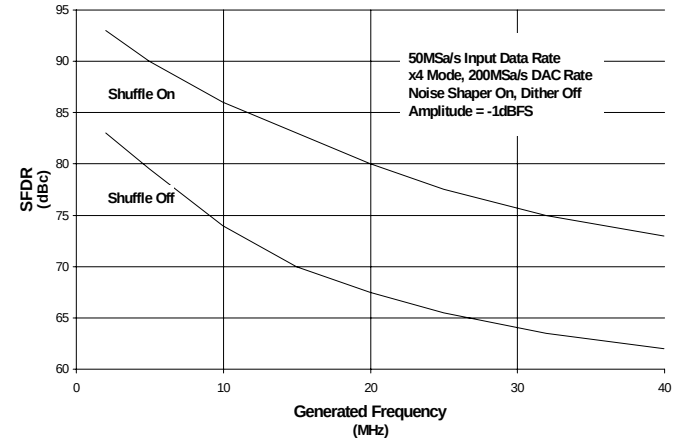
Parameter	Notes	Symbol	Ratings			Units
			Min.	Typ.	Max.	
Maximum DAC Conversion rate						
VDD <3.3V	1	F_{DAC}	350	380		MSa/s
VDD ≥3.3V			400	416		MSa/s
Maximum input data rate, interpolation modes						
x4		F_{DATA}	100	104		MSa/s
x2 [slow]			100	104		MSa/s
x2 [fast]			200	208		MSa/s
x1	2		200	208		MSa/s
Clock in						
Low time		t_{lo}	1			ns
High time		t_{hi}	1			ns
Slew rate for minimum wide-band jitter		t_{sl}	0.5			V/ns
Common mode input voltage		V_{cm}	0		V_{DD} - 1.25	V
Signal level (differential)	3		100			mV
Clock out				7		
CLK In to Data CLK delay		t_{del}				ns
Crystal oscillator maximum speed		F_{XTAL}			40	MHz

T_{OP}(min) to T_{OP}(max), VDD = RVDD = AVDD = CVDD = +3.3V, VSS = RVSS = AVSS = CVSS = 0V, I_{FS}=20mA, Differential Transformer coupled output, 50Ω doubly terminated, unless otherwise specified

1. Assumes x2[fast] or x4 Interpolation mode selected
2. Limited by CMOS digital I/O speed
3. Ensure that slew rate specifications are observed

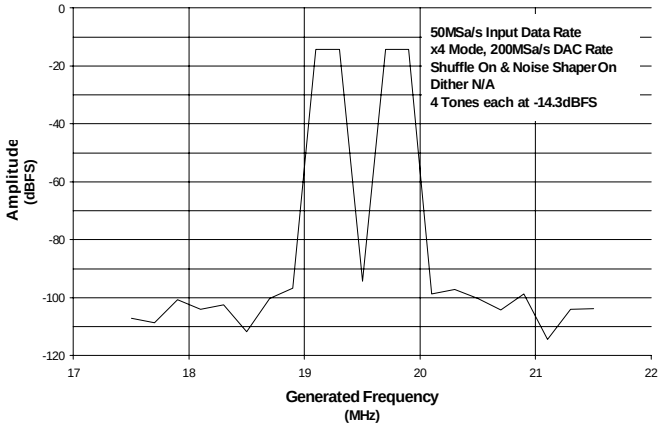
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5.6 Typical Performance Characterisation Graphs



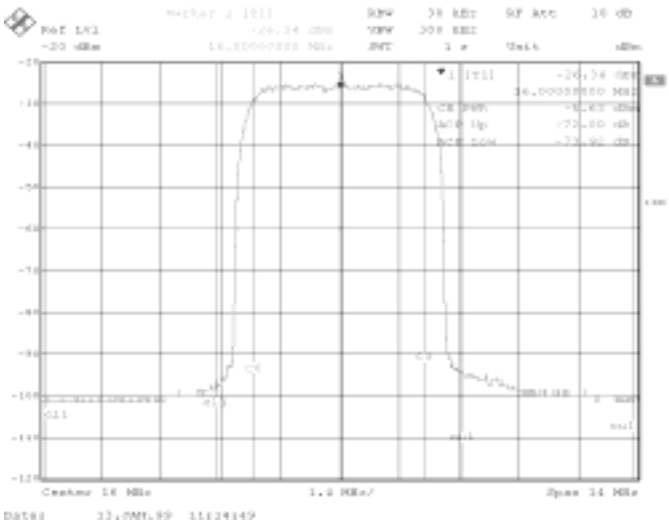
Single Tone Spurious Free Dynamic Range

Figure 10 Single Tone SFDR Performance



Multi-tone test, 4 tones, 200kHz channel spacing, missing centre tone

Figure 11 Multi-tone Performance



W-CDMA direct-IF channel generation example
4MHz channel, 5MHz channel spacing
16MHz channel centre frequency
F_{DATA} = 64MSa/s, x4 Interpolation
F_{DAC} = 256MSa/s

Figure 12 W-CDMA Carrier Direct-IF Generation

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6 Application Notes

6.1 Power & Ground Plane Regions

The following guidelines are suggested to obtain the specified performance. Any departure from these recommendations should be investigated to confirm that performance in the application is acceptable.

The device should be used with an epoxy-glass PCB, utilizing a minimum of four layers for separate power and ground planes, manufactured with tolerances capable of producing exact impedance tracking. When using a four layer board critical analog signals should be routed on the external layer adjacent to the ground plane (typically layer 1). The power and ground planes should be split to isolate digital, clock and analog regions of the circuitry to prevent supply noise coupling from one to another. These separated regions should only be connected together at one place, a star point located underneath the device, which should also be used as a connection point to the PSU. These isolated regions should only extend across the PCB as far as necessary, and avoid other sections of the application circuit that could introduce noise. Signal regions such as the Analog Out and Clock In/Out can be separated from the remainder of the application circuit by introducing a transformer as an isolator.

The connection to the PSU should also be arranged as a star point, with all other sections of the application circuit joined at this point. Tracks to this point should be made as wide as possible, and if they are located in the ground plane layer, should be positioned under static pins. No connection to the supply tracks should be made midway. See Figure 13.

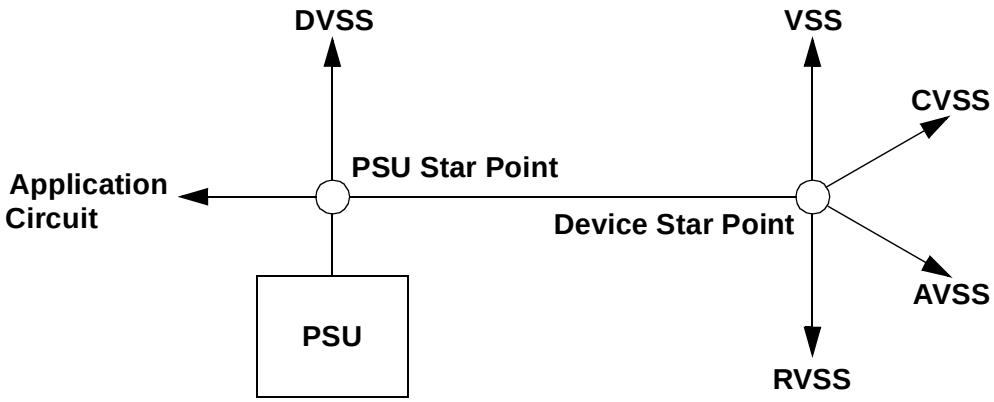


Figure 13 Power Supply Distribution Through Star Points

The DVDD and VDD, and DVSS and VSS pins can be connected to the same region, but normally the Digital supply and ground plane regions should be split further to isolate the Digital control and Digital data blocks. The Digital data region will normally extend into the application circuit, and as such will be subject to significant noise.

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Another significant reason for splitting the digital data ground plane from the main digital ground is that when using a remote data generator (e.g. a benchtop pattern or data generator) there is a tendency for noise to be injected on the data ground by the equipment. This is significant because the data rate is high, the data bus is wide, and it's correlation with the signal can cause spurious tones which degrade SFDR. The coupling mechanism is from the fast-slewing data inputs via the capacitance of the input pins/pads/ protection diodes into the internal circuits. The transient currents through these parasitics can be several hundred milliamps. For this reason, it is recommended that this region is not connected to the device star point but to the PSU star point directly.

The data supplies are only used for the input section of the device, so noise in this region cannot couple into the DAC core. The digital supplies connect to the digital circuits (filters, noise shaper and ditherer) inside the DAC, including those inside the DAC core. The control inputs can use this supply because they toggle more slowly (if at all) and aren't correlated with the data. The analog sections (Analog, Clock and Reference) have separate supply connections as transition dependant currents from the digital sections will cause delay modulation in the clock path, and amplitude modulation in the analog output section.

Each supply should be decoupled, producing a low impedance shunt at high frequency. The Digital, Analog, Clock and Reference sections can be connected directly to the device star point, but preferably through a small inductor. If a fully split power (VDD) plane is not desired, then as a minimum only the ground plane need be split as described. However it is very important to isolate the I/O supply (DVDD) from all other supplies in some way, possibly feeding the supply through a low-R resistor or ferrite bead. This will help to filter out noise.

If the data (signal) and control lines are connected to the same device (e.g. an ASIC), then generally this should have been designed to support separate supply and ground pins for the digital data bus. The ground plane at the generating device (ASIC) then becomes the star point for the data, requiring cuts in the ground/ supply planes on either side of the data bus, and looping under the DAC. The digital data decoupling at the DAC should also be inside this loop. This gives a "U" shaped cut in the planes with the open end at the data source (with decoupling) and the closed end at the DAC (with decoupling). All the data return currents will then be confined inside this "U", and so none of them can couple into the analog ground planes to degrade SFDR. It may be advisable to bury the digital data bus tracks on an internal layer, with data ground planes above, below and either side of the tracks (the ground layers connected together with a row of vias) to shield against RF radiation.

Figure 14 shows these principles applied to the ground plane of an application board. The pad on the left represents the PSU star point, and the pad in the center represents the device star point. These points could be realized with a via, so that the connection from the PSU out to other star points could be made on another layer if necessary. The positioning of the plane breaks are also shown. The breaks in the planes between each section should mark the boundary of that section. It is very important to ensure that there are no tracks crossing these boundaries, or any splits in the planes that tracks must cross, as this will create current loops within the plane itself.

The power supply track region is shown extending to the side of the device for reference purposes. If the PSU region is not required, then the region should be merged with the Digital region.

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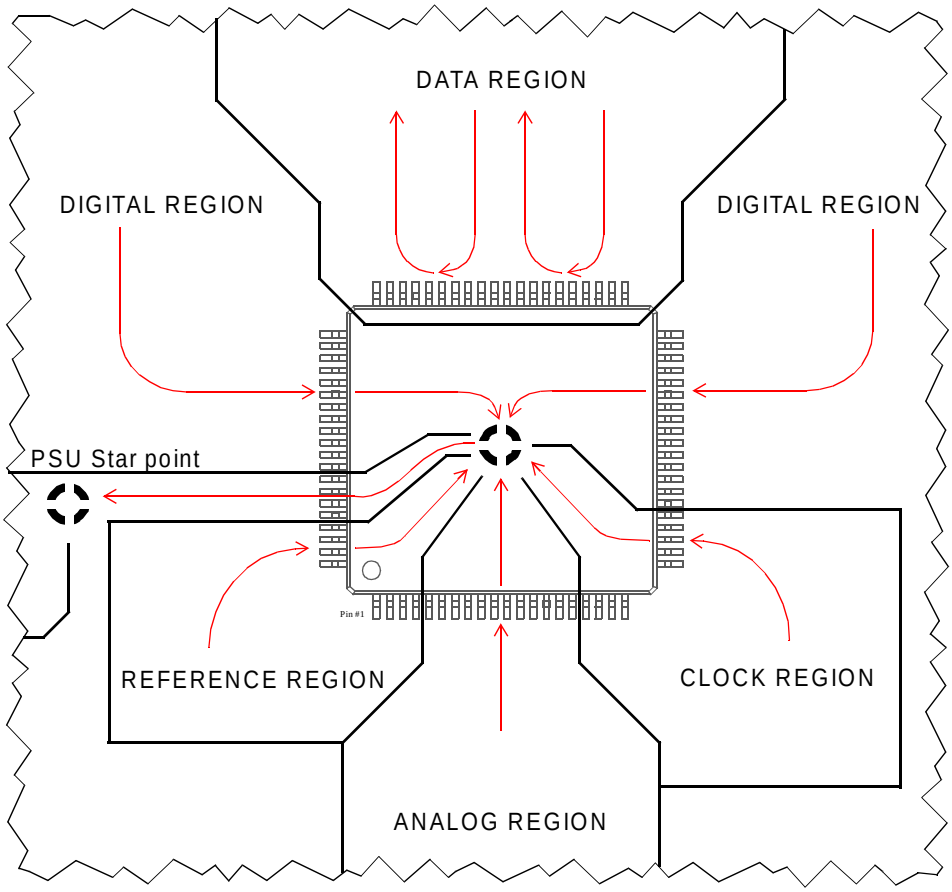


Figure 14 Recommended Ground Plane Splits

6.2 Power Supplies

Only one clean low-impedance power supply is required. Power distribution should be organized as shown in Figure 13, with a main star point at the PSU supplying the data (DVDD/DVSS) block, with a secondary device star point supplying the Digital, Analog, Clock and Reference blocks. If this supply is used to supply any other circuits, they must not introduce any modulation onto the supply, or SFDR will be degraded.

If the impedance of the supply is not low enough to prevent modulation by the currents drawn by the data source, then a separate supply for the Data source should be used. If the Digital, Analog, Clock and Reference block supply is still not low enough impedance to prevent power supply modulation being introduced by the Digital block, then a further supply for the Analog block alone must be introduced.

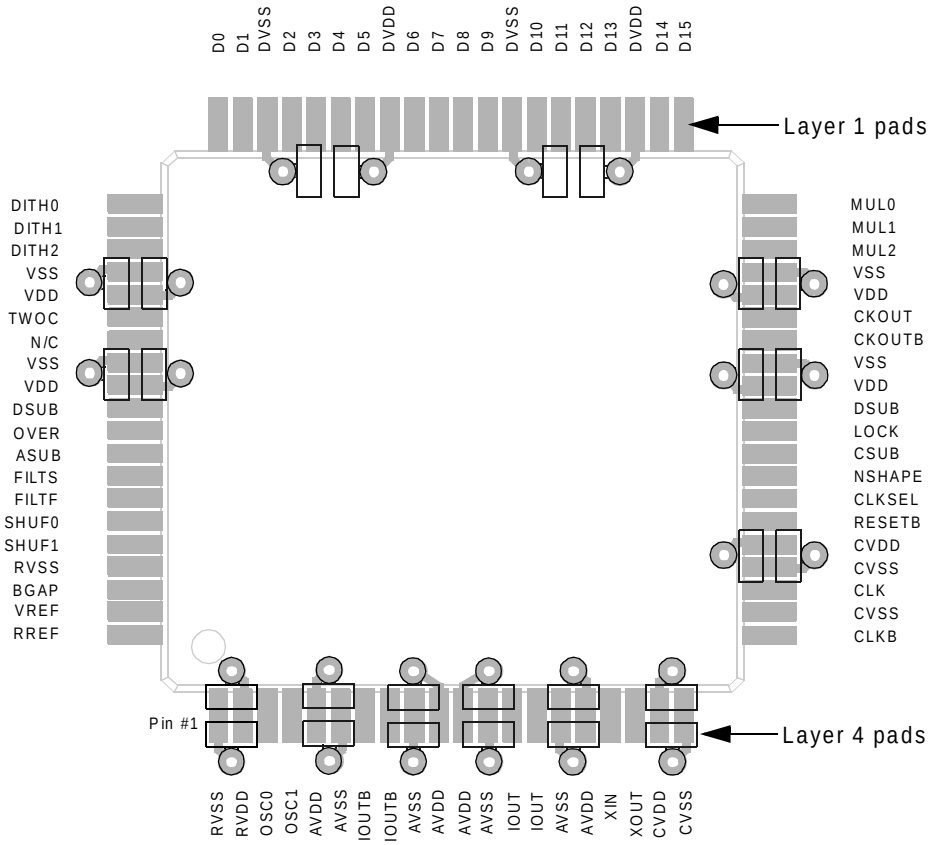
Bulk decoupling of around 100uF at the power supply star point is recommended to remove any low frequency ripple. Smaller value decoupling of 1 to 10uF at the device star point is recommended to apply a low impedance shunt at high frequency.

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Power supply tracks should be kept as short and wide as possible. The ground and supply tracks should run adjacent to each other for as far as possible, whilst avoiding all signal tracks that may couple noise into the supply.

6.3 Decoupling

All supplies and references should be decoupled to the appropriate ground plane using surface mount 100nF capacitors, placed as close as possible to the device. For each pair of VDD/VSS pins it is recommended that the capacitor is located on the reverse of the PCB, immediately under the device, with vias to the supply and ground planes as close as physically possible to the device and capacitor. This layout minimizes the total length of track, including the plated through hole, and hence keeps loop inductance to a minimum. An example of the recommended layout, using 0603 format surface mount capacitors and a four layer PCB is illustrated in Figure 15.



N.B. Not to scale. All vias connect to the appropriate Ground or Power plane.

Figure 15 Recommended Supply Decoupling Layout

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6.4 Analog Output

To provide a differential analog output which is both isolated form the analog ground plane, and which gives good common mode rejection, a two stage transformer circuit can be used. The recommended devices are Mini-Circuits (http://www.minicircuits.com) ADTT1-1, 1:1 transformer, and ADTL1-12 transmission line transformer. The primary of the ADTL1-12 is connected to IOUT and IOUTB, (terminated as shown in Figure 16) and the secondary is connected to the ends of the secondary of the ADTT1-1. The center tapping of the secondary of the ADTT1-1 will be linked to the analog ground plane. The primary of the ADTT1-1 will be terminated as required by the application circuit. See Figure 16.

For optimum performance the transformer should be positioned as close to the device as physically possible, and should be connected to the analog output pins IOUT and IOUTB with 50Ω tracks. The connections to the analog ground plane should be made through the same vias as the decoupling capacitors, which are shown in Figure 15 as being on the outside of the device pad pattern, so that the track length and hence loop inductance can be kept to a minimum.

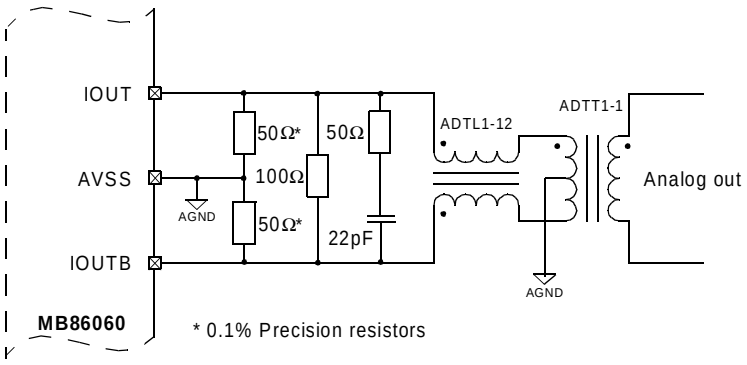


Figure 16 Analog Out Transformer Coupling

6.5 Clock Input

The reference clock input can be connected in a number of ways, depending on the clock source used. For optimum performance the MB86060 should have ground plane isolation from the source by the use of a coupling transformer.

The simplest method is to use the internal oscillator, with a crystal connected across XIN and XOUT. A 1MΩ resistor should be connected in parallel with the crystal, and capacitors (typically 22pF, depending on crystal used) should be connected from both XIN and XOUT to the clock ground plane region. See Figure 17a.

A single ended CMOS crystal oscillator can be used, connected to XIN. This source can be connected to

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the clock ground plane region as long as there are no other devices connected to the clock signal, i.e. the oscillator has a fan-out of one. See Figure 17b.

If a common, system wide logic level clock source is to be used, this should be transformer coupled to remove common mode noise and isolate the clock ground plane region. The recommended 1:1 impedance transformer is a Mini-Circuits, ADT1-1. The secondary will be connected to the differential clock inputs CLK and CLKB, and terminated with a 100Ω resistor. The PCB tracks to the device should be 50Ω tracks. The primary of the transformer will be connected between the digital clock source and the digital clock source ground. A 100Ω source resistor is used, and the PCB tracks to the clock source should be 100Ω. See Figure 17c.

For connection to a low noise RF source, a Balun transformer should be used. The recommended transformer is a Mini-Circuits ADTL1-12. The secondary terminals should be connected through a 100nF capacitor to the differential clock inputs CLK and CLKB. The clock inputs should be terminated with a 50Ω resistor. The primary dot should be connected to the RF signal with a 50Ω PCB track, and the other primary connection should be connected to RF ground. The primary ground may be connected to clock ground if necessary. See Figure 17d. This configuration would allow for a RF signal level of between -6dBm and +24dBm, giving a differential signal level of up to 5V pk-pk at CLK and CLKB.

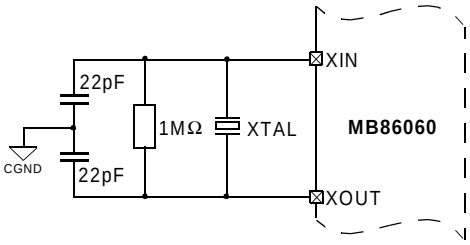
6.6 Clock Output

The data clock output is required as a reference to clock the data into the device. As with the analog output and the reference input it is recommended that the data clock is isolated from the application circuit to remove common mode noise in the digital ground plane.

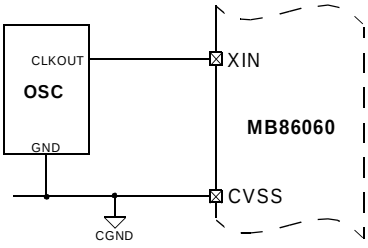
The output pins CKOUT and CKOUTB are designed to drive a bridged load to reduce the effect of package inductance, and each pin has a nominal output resistance of 25Ω.

A transformer can again be used, the recommended device being a Mini-Circuits ADT4-1WT. The ends of the secondary should be connected to CKOUT and CKOUTB through series 75Ω resistors, and 100Ω PCB tracks, and the centre tapping should be left not connected. The primary dot end should be connected to the wiper of a 100Ω variable resistor to provide an adjustable bias point for the output signal. The variable resistor should be placed across the supply and ground rails of the application circuit, and a 100nF capacitor placed from the wiper to application ground. (If the biasing is not required connect the primary dot to ground). The data clock is then present at the other end of the primary. A 50Ω PCB track should be used here. See Figure 18.

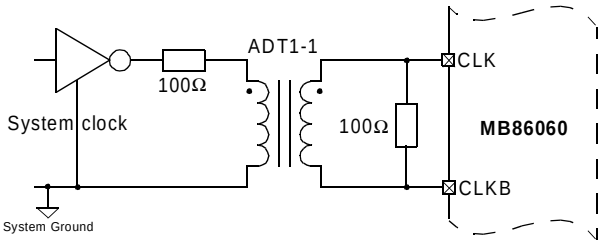
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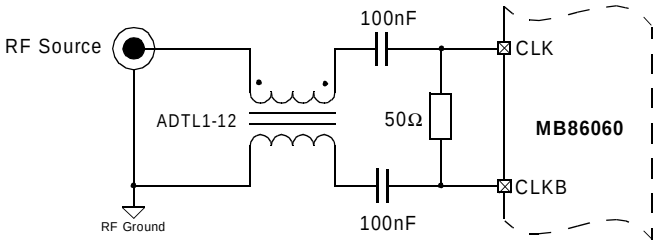
A: Using the internal crystal oscillator



B: Using a dedicated CMOS oscillator



C: Using a common system clock source



D: Using an RF source

Figure 17 Clock Input Configurations

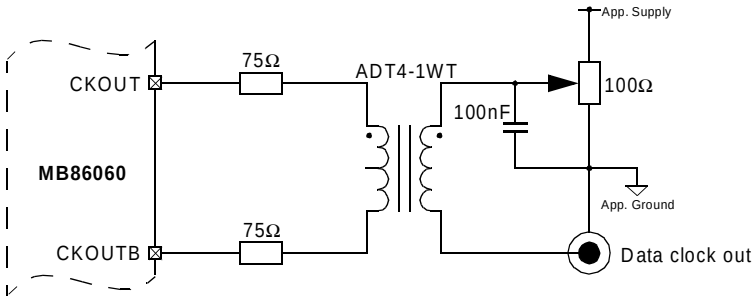
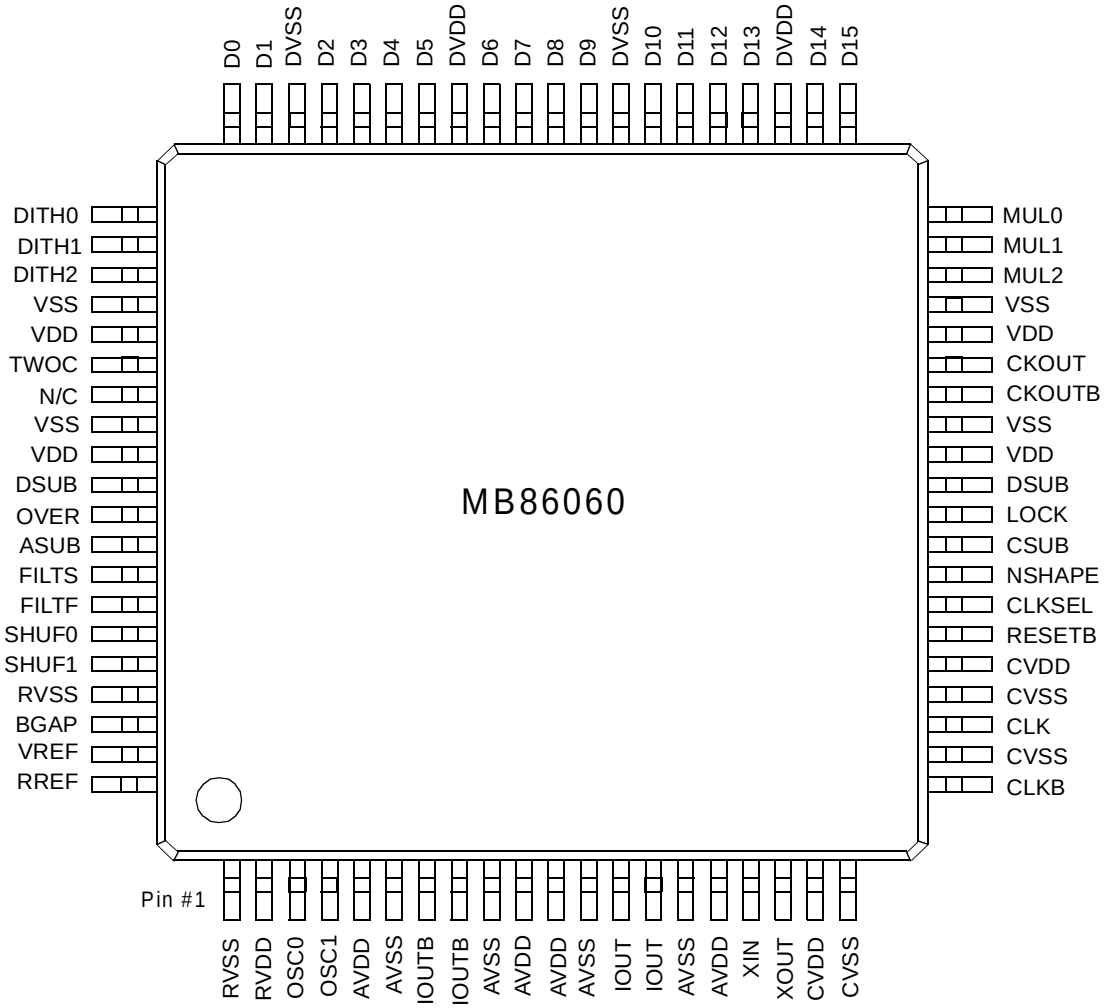


Figure 18 Data Clock Out Transformer Coupling

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7 Pin Description

7.1 Pin Assignment



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7.2 Pin Definition

Digital Interface

Pin No.	Pin Name	Input/ Output	Description
41, 42, 44, 45, 46, 47, 49, 50, 51, 52, 54, 55, 56, 57, 59, 60	D[15:0]	I	Input data [MSB = D15] Connect unused inputs to DVSS, e.g. D0 & D1 for 14-bit source data
43, 53	DVDD	-	Data interface supply, +3.3V
48, 58	DVSS	-	Data interface ground, 0V
31, 70	DSUB	-	Data interface substrate. Link to VSS

Digital & Control

Pin No.	Pin Name	Input/ Output	Description
61, 62, 63	DITH[0:2]	I	Programmable Dither control. See Table 5
73, 74	FILTS, FILTF	I	Interpolation Filters control. See Table 2
28	NSHAPE	I	Noise shaper, enabled ='1', disabled ='0'. See section 1.5
75, 76	SHUF[1:0]	I	Segment Shuffling control. See Table 6.
66	TWOC	I	Input data format selection, '1' = 2's Complement
71	OVER	O	Digital overflow warning
27	CLKSEL	I	Differential clock ='1', Crystal clock via XIN = '0'
38, 39, 40	MUL[2:0]	I	Clock multiplier mode control. See Table 2
30	LOCK	O	DLL locked indicator ='1'
26	RESETB	I	Device reset ='0'
67	N/C	-	No connection
32, 36, 65, 69	VDD	-	Digital supply, +3.3V
33, 37, 64, 68	VSS	-	Digital ground, 0V
Control lines should be linked to VDD or VSS according to the function setting required			

Clock

Pin No.	Pin Name	Input/ Output	Description
21, 23	CLKB, CLK	I	Differential input clock
34, 35	CKOUTB, CKOUT	O	Data clock
17	XIN	I	Crystal / clock input. Connect to CVSS when not used
18	XOUT	O	Crystal oscillator circuit output
19, 25	CVDD	-	Clock supply, +3.3V
20, 22, 24	CVSS	-	Clock ground, 0V
29	CSUB	-	Clock substrate. Link to VSS

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Analog

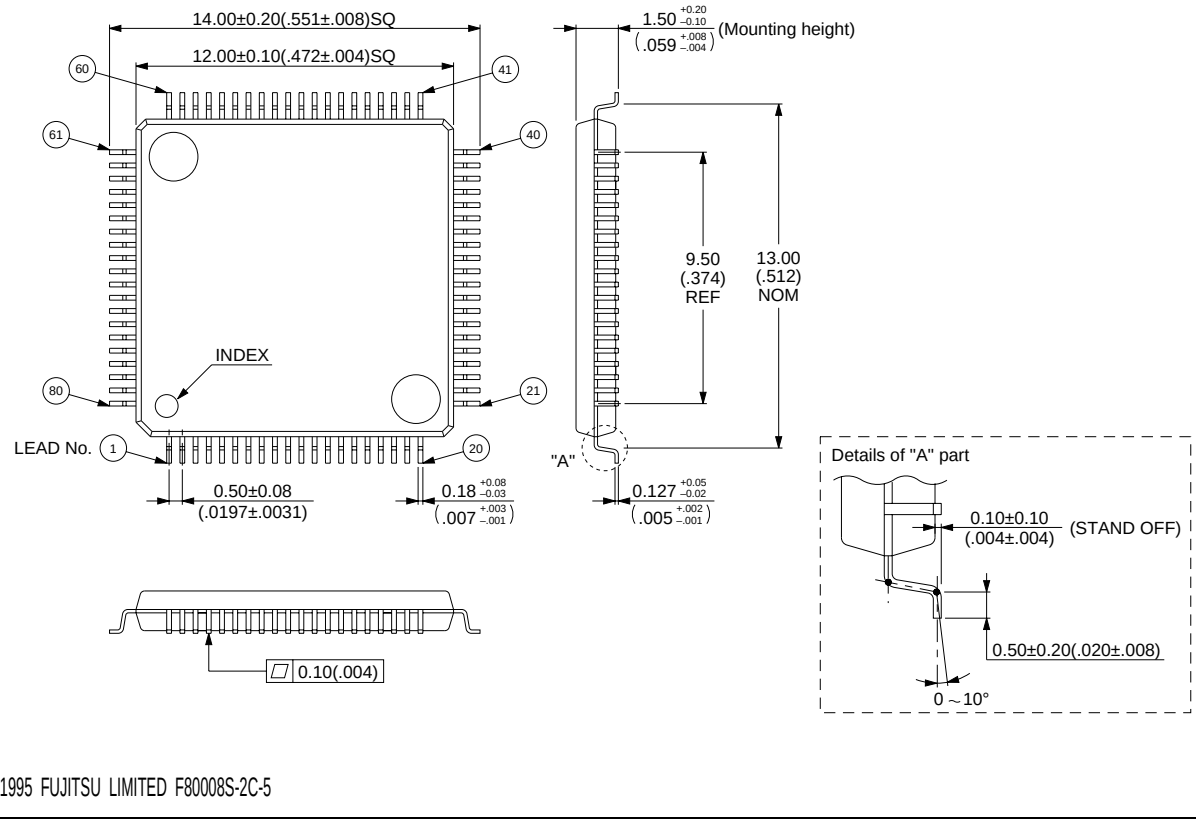
Pin No.	Pin Name	Input/ Output	Description
7,8	IOUTB	O	DAC output (inverting). Connect together.
13,14	IOUT	O	DAC output (non-inverting). Connect together.
5, 10, 11, 16	AVDD	-	Analog supply, +3.3V
6, 9, 12, 15	AVSS	-	Analog ground, 0V
72	ASUB	-	Analog substrate. Link to VSS

Reference

Pin No.	Pin Name	Input/ Output	Description
3, 4	OSC[0:1]	I	Delay line control. Internal pull-down, N/C when not used
78	BGAP	O	Bandgap reference
79	VREF	I	Voltage reference input
80	RREF	O	Output reference resistor. See section
2	RVDD	-	Reference supply, +3.3V
1, 77	RVSS	-	Reference ground, 0V
Bits OSC[0:1] should be linked to RVDD or RVSS according to the Delay Line control setting required			

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7.3 Package Data



All dimensions in millimetres (inches)

7.3.1 Thermal Characteristics

- θ_{JA} = 40.4°C/W, θ_{JC} = 8°C/W

Figures assume mounting on a 4-layer pcb mounted in free air.

7.4 Ordering Information

The following reference should be used when ordering devices,

- MB86060PFV

For further assistance please contact your sales representative.

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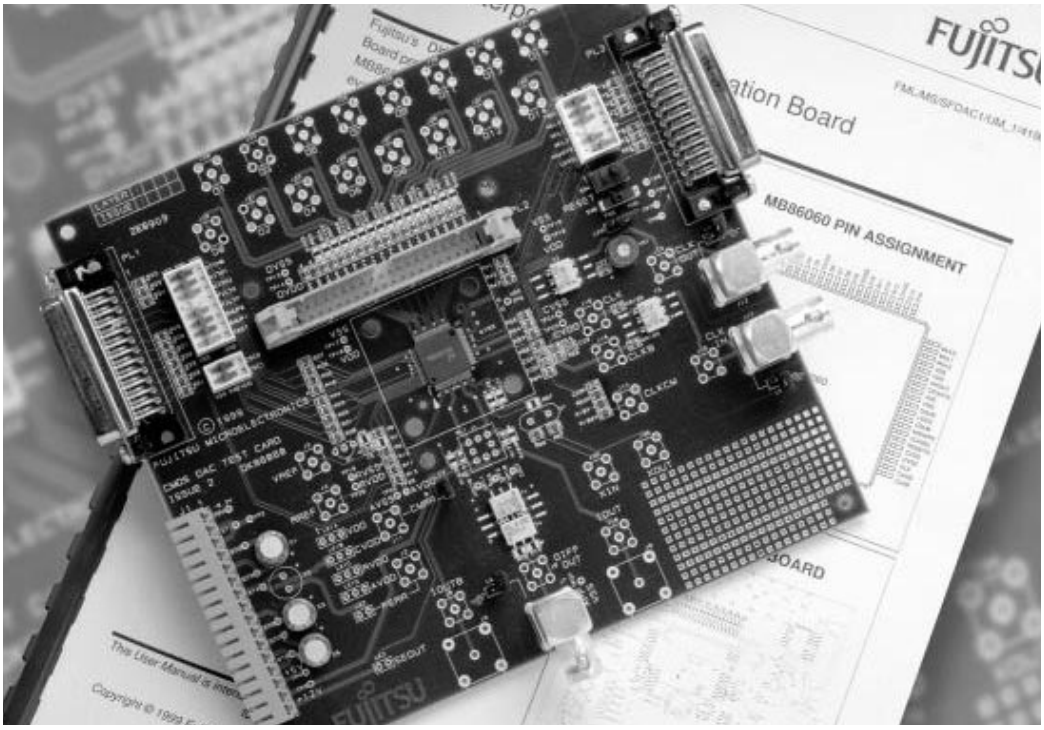
8 Development Kit

A development kit, reference DK86060, is available for the MB86060 16-bit Interpolating DAC. The kit includes an evaluation board that enables simple and effective evaluation of the device.

The board provides a complete evaluation environment for the DAC. A transformer coupled differential output interface is provided to simplify integration into target applications and development environments. An RF clock source can be connected via the transformer coupled input, and 16-bit data via a 40-way IDC header.

The development kit includes,

- Evaluation board with MB86060 device fitted
- Spare MB86060 for customer development
- User Manual



For further assistance, including price and delivery of the development kit, please contact your sales representative.

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MB86060 16-Bit Interpolating Digital to Analog Converter

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