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October 1991
Edition 2.0

FUJITSU

DATA SHEET

MB98A9060x-20/9070x-20/9080x-20/9090x-20
SRAM MEMORY CARD

STATIC RANDOM ACCESS MEMORY CARD
64K / 128K / 256K / 512K-BYTE

The Fujitsu MB98A9060x, MB98A9070x, MB98A9080x and MB98A9090x are Static Random Access Memory (SRAM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by two metal panels, one at the top and the bottom of the card, that help to reduce chip damage from electrostatic discharge.

When the SRAM card is not powered by its system, an on-board, replaceable lithium battery (coin-type) is used to retain data. When the lithium battery must be replaced, two rechargeable batteries that are built into the SRAM card, maintain data. (See the BLOCK DIAGRAM for location of batteries.)

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card Internal Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, SRAM cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is an SRAM memory card option. (See page 2 for a description of the three available options.)



CRD-68P-M04

- PCMCIA and JEIDA industry standard for 68-pin memory card
- Credit card size dimensions: 85.6mm (length) x 54.0mm (width) x 3.3mm (thick).
- PCMCIA / JEIDA industry standard, two-piece 68-pin connector (with a two-row built-in 68-pin replaceable)
- Replaceable lithium battery
- Built-in, rechargeable batteries for data retention during lithium battery replacement
- Battery voltage detect and write protect function

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	−0.5 to +6.0	V
Input Voltage	VIN	−0.5 to VCC +0.5	V
Output Voltage	VOUT	−0.5 to VCC +0.5	V
Temperature under Bias	TBIAS	−10 to +60 *1	°C
Storage Temperature	TSTG	−20 to +65 *2	°C

Note: *1 This value does not apply to the replaceable battery.
*2 This value does not apply to the replaceable battery and data retention.

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the REG pin on the card interface. Option descriptions as follows:

OPTION 1: Attribute memory is not supported. $\overline{\text{REG}}$ Pin : Not Contacted

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90601	MB84256A x 2 pcs	200 ns	N / A	N / A	64K x 8 bits/32K x 16 bits
MB98A90701	MB84256A x 4 pcs	200 ns	N / A	N / A	128K x 8 bits/64K x 16 bits
MB98A90801	MB84256A x 8 pcs	200 ns	N / A	N / A	256K x 8 bits/128K x 16 bits
MB98A90901	MB84256A x 16 pcs	200 ns	N / A	N / A	512K x 8 bits/256K x 16 bits

OPTION 2: Attribute memory in a separate location is not supported.

When the $\overline{\text{REG}}$ line is asserted, "FF" is output to the data bus to indicate that attribute memory may be stored in main memory.

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90602	MB84256A x 2 pcs	200 ns	N / A	N / A	64K x 8 bits/32K x 16 bits
MB98A90702	MB84256A x 4 pcs	200 ns	N / A	N / A	128K x 8 bits/64K x 16 bits
MB98A90802	MB84256A x 8 pcs	200 ns	N / A	N / A	256K x 8 bits/128K x 16 bits
MB98A90902	MB84256A x 16 pcs	200 ns	N / A	N / A	512K x 8 bits/256K x 16 bits

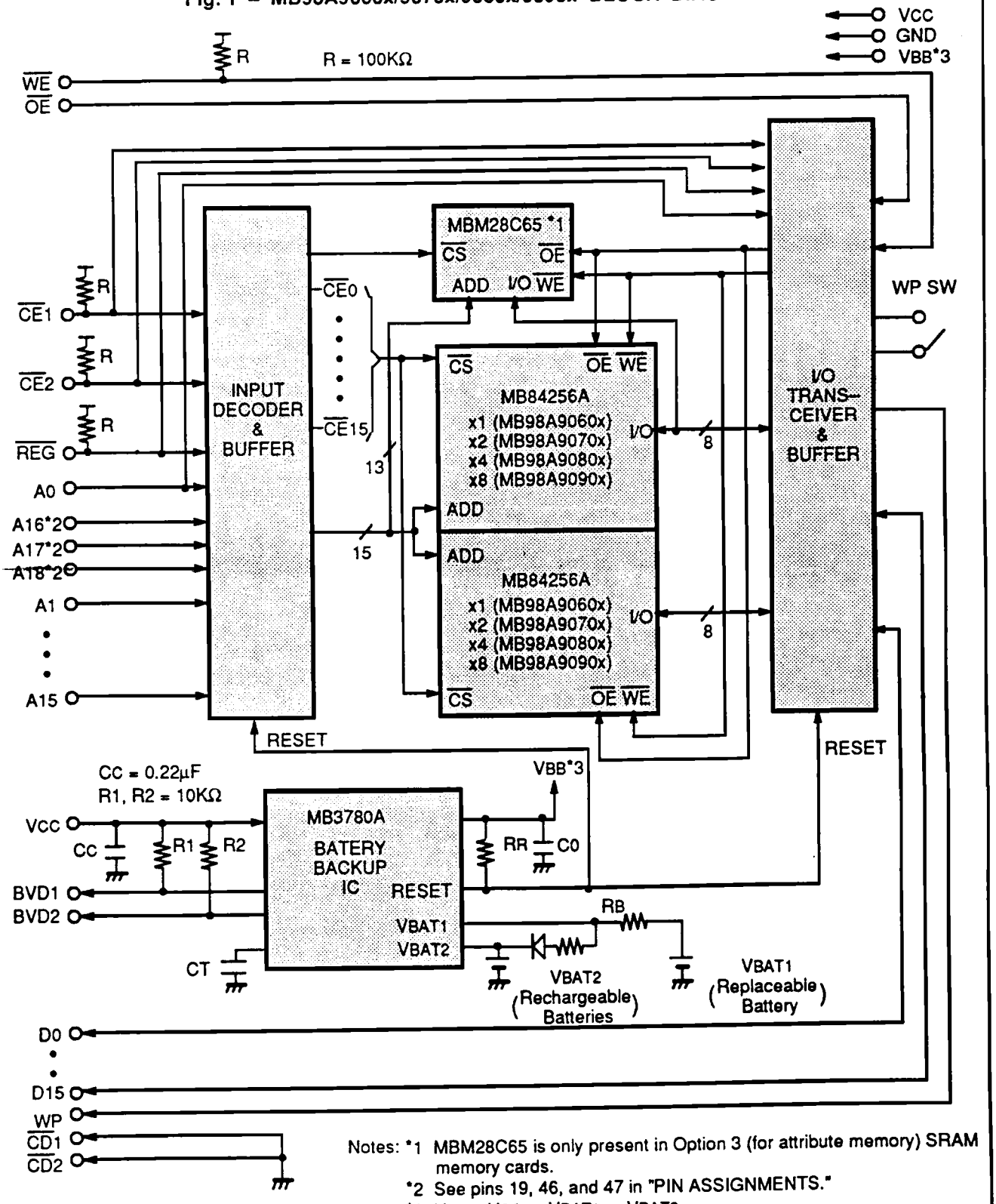
OPTION 3: Attribute memory is supported. The data is stored in an 8K-bit EEPROM.

When the $\overline{\text{REG}}$ line is asserted, data stored in EEPROM is output to the data bus.

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A90603	MB84256A x 2 pcs	200 ns	MBM28C65 x 1 pc	300 ns	64K x 8 bits/32K x 16 bits
MB98A90703	MB84256A x 4 pcs	200 ns	MBM28C65 x 1 pc	300 ns	128K x 8 bits/64K x 16 bits
MB98A90803	MB84256A x 8 pcs	200 ns	MBM28C65 x 1 pc	300 ns	256K x 8 bits/128K x 16 bits
MB98A90903	MB84256A x 16 pcs	200 ns	MBM28C65 x 1 pc	300 ns	512K x 8 bits/256K x 16 bits

Note: * To be configured by user.

Fig. 1 – MB98A9060x/9070x/9080x/9090x BLOCK DIAGRAM



Notes: *1 MBM28C65 is only present in Option 3 (for attribute memory) SRAM memory cards.
*2 See pins 19, 46, and 47 in "PIN ASSIGNMENTS."
*3 VBB = VCC or VBAT1 or VBAT2.

PIN ASSIGNMENTS

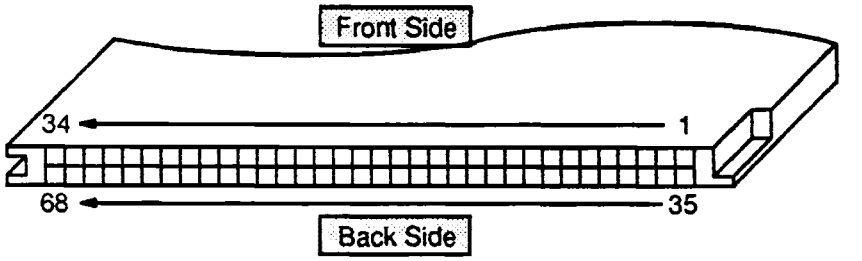
MB98A9060x	MB98A9070x	MB98A9080x	MB98A9090x	Pin No.		MB98A9060x	MB98A9070x	MB98A9080x	MB98A9090x
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC	NC
A11	A11	A11	A11	10	44	NC	NC	NC	NC
A9	A9	A9	A9	11	45	NC	NC	NC	NC
A8	A8	A8	A8	12	46	NC	NC	A17	A17
A13	A13	A13	A13	13	47	NC	NC	NC	A18
A14	A14	A14	A14	14	48	NC	NC	NC	NC
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	15	49	NC	NC	NC	NC
NC	NC	NC	NC	16	50	NC	NC	NC	NC
VCC	VCC	VCC	VCC	17	51	VCC	VCC	VCC	VCC
NC	NC	NC	NC	18	52	NC	NC	NC	NC
NC	A16	A16	A16	19	53	NC	NC	NC	NC
A15	A15	A15	A15	20	54	NC	NC	NC	NC
A12	A12	A12	A12	21	55	NC	NC	NC	NC
A7	A7	A7	A7	22	56	NC	NC	NC	NC
A6	A6	A6	A6	23	57	NC	NC	NC	NC
A5	A5	A5	A5	24	58	NC	NC	NC	NC
A4	A4	A4	A4	25	59	NC	NC	NC	NC
A3	A3	A3	A3	26	60	NC	NC	NC	NC
A2	A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	A1	28	62	BVD2	BVD2	BVD2	BVD2
A0	A0	A0	A0	29	63	BVD1	BVD1	BVD1	BVD1
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A0 to A18	Address Input	Input	Address Inputs, A0–A18.
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs. The data bus size (8-bit or 16-bit) selected with CE1 and CE2.
$\overline{CE1}$	Card Enable for Lower Byte	Input	Active Low. –Lower byte (D0–D7) is selected for read/write function of SRAM cards.
$\overline{CE2}$	Card Enable for Upper Byte	Input	Active Low. –Upper byte (D8–D15) is selected for read/write function of SRAM cards.
$\overline{REG}$	Attribute Memory Select	Input	Active Low. –Attribute memory is selected for read/write function of identification data of SRAM cards. (NC or "FF" data or attribute data.
$\overline{OE}$	Output Enable	Input	Active Low. –Output enable for SRAM cards.
$\overline{WE}$	Write Enable	Input	Active Low. –Write enable for SRAM cards.
$\overline{CD1}$, $\overline{CD2}$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	Write controller for SRAM cards. This pin outputs the On/Off status of "WP Switch".
BVD1	Battery Voltage Detect 1	Output	These pins indicate the battery condition of the SRAM cards. a) BVD1 = BVD2 = VOH –Battery voltage is a safe level. b) BVD2 = VOL, BVD1 = VOH –Battery voltage is lower than 2.65V. Battery should be replaced. c) BVD1 = BVD2 = VOL –Battery voltage is lower than 2.37V.
BVD2	Battery Voltage Detect 2	Output	
VCC	Power Supply	–	Power Supply Voltage. (+5.0V ±5%)
GND	Ground	–	System Ground.
NC	No Connection	–	

PIN LOCATIONS

Fig. 2 – BOTTOM VIEW (CONNECTOR SIDE)



FUNCTION TRUTH TABLE

MAIN MEMORY FUNCTION *1 ($\overline{REG}$=VIH)

$\overline{CE2}$	$\overline{CE1}$	A0 (Byte)	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW.
							D15–D8	D7–D0	
H	H	X	X	X	L	Standby	High–Z		NP
H	L	L	L	H	L	Read (x8)	High–Z	DOUT (Lower Byte)	NP
H	L	H	L	H	L	Read (x8)	High–Z	DOUT (Upper Byte)	NP
H	L	L	H *2	L	L	Write (x8)	High–Z	DIN (Lower Byte)	NP
H	L	H	H *2	L	L	Write (x8)	High–Z	DIN (Upper Byte)	NP
L	H	X	L	H	L	Read (x8)	DOUT (Upper Byte)	High–Z	NP
L	H	X	H *2	L	L	Write (x8)	DIN (Upper Byte)	High–Z	NP
L	L	X	L	H	L	Read (x16)	DOUT		NP
L	L	X	H	L	L	Write (x16)	DIN		NP
X	X	X	H	H	L	Output Disable	High–Z		NP
H	H	X	X	X	H	Standby	High–Z		P
H	L	L	L	H	H	Read (x8)	High–Z	DOUT (Lower Byte)	P
H	L	H	L	H	H	Read (x8)	High–Z	DOUT (Upper Byte)	P
H	L	L	H *2	L	H	Output Disable	High–Z		P
H	L	H	H *2	L	H	Output Disable	High–Z		P
L	H	X	L	H	H	Read (x8)	DOUT (Upper Byte)	High–Z	P
L	H	X	H *2	L	H	Output Disable	High–Z		P
L	L	X	L	H	H	Read (x16)	DOUT		P
L	L	X	H	L	H	Output Disable	High–Z		P
X	X	X	H	H	H	Output Disable	High–Z		P

Notes: *1 H = VIH, L = VIL, X = Either VIL or VIH, WP SW = Write Protect Switch, NP = Non Protect, P = Protect
*2 H-level is recommended though it is functionable at L-level.

FUNCTION TRUTH TABLE (Continued)

ATTRIBUTE MEMORY FUNCTION *1 ($\overline{REG}$=VIL) *2

$\overline{CE2}$	$\overline{CE1}$	A0 (Byte)	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW.
							D15–D8	D7–D0	
H	H	X	X	X	L	Standby	High–Z		NP
H	L	L	L	H	L	Read (x8)	High–Z	DOUT *3 (Lower Byte)	NP
H	L	H	L	H	L	Read (x8)	High–Z	H	NP
H	L	L	H	L	L	Write (x8)	High–Z	DIN (Lower Byte)	NP
H	L	H	H	L	L	Write (x8)	High–Z	X	NP
L	H	X	L	H	L	Read (x8)	H	High–Z	NP
L	H	X	H	L	L	Write (x8)	High–Z	High–Z	NP
L	L	X	L	H	L	Read (x16)	H	DOUT *3 (Lower Byte)	NP
L	L	X	H	L	L	Write (x16)	X	DIN (Lower Byte)	NP
X	X	X	H	H	L	Output Disable	High–Z		NP
H	H	X	X	X	H	Standby	High–Z		P
H	L	L	L	H	H	Read (x8)	High–Z	DOUT *3 (Lower Byte)	P
H	L	H	L	H	H	Read (x8)	High–Z	H	P
H	L	L	H	L	H	Output Disable	High–Z		P
H	L	H	H	L	H	Output Disable	High–Z		P
L	H	X	L	H	H	Read (x8)	H	High–Z	P
L	H	X	H	L	H	Output Disable	High–Z		P
L	L	X	L	H	H	Read (x16)		DOUT *3 (Lower Byte)	P
L	L	X	H	L	H	Output Disable	High–Z		P
X	X	X	H	H	H	Output Disable	High–Z		P

Notes: *1 H = VIH, L = VIL, X = Either VIL or VIH. WP SW = Write Protect Switch, NP = Non Protect, P = Protect
*2 NC for MB98A90601, 90701, 90801, and 90901.
*3 H-level is output for MB98A90602, 90702, 90802, and 90902.

ADDRESS CONFIGURATIONS *1 (MAIN MEMORY)

8-BIT BUS ORGANIZATION ($\overline{CE1}$ = VIL, $\overline{CE2}$ = VIH)

A18 to A0	$\overline{CE2}$	$\overline{CE1}$	D15–D8	D7–D0
000 0000 0000 0000 0000	H	L	------	0 Add.
000 0000 0000 0000 0001	H	L	------	1 Add.
000 0000 0000 0000 0010	H	L	------	2 Add.
000 0000 0000 0000 0011	H	L	------	3 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 1100	H	L	------	524284 Add.
111 1111 1111 1111 1101	H	L	------	524285 Add.
111 1111 1111 1111 1110	H	L	------	524286 Add.
111 1111 1111 1111 1111	H	L	------	524287 Add.

8-BIT BUS ORGANIZATION ($\overline{CE1}$ = VIH, $\overline{CE2}$ = VIL) *2

A18 to A0	$\overline{CE2}$	$\overline{CE1}$	D15–D8	D7–D0
000 0000 0000 0000 000X	L	H	1 Add.	------
000 0000 0000 0000 001X	L	H	3 Add.	------
000 0000 0000 0000 010X	L	H	5 Add.	------
000 0000 0000 0000 011X	L	H	7 Add.	------
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 100X	L	H	524281 Add.	------
111 1111 1111 1111 101X	L	H	524283 Add.	------
111 1111 1111 1111 110X	L	H	524285 Add.	------
111 1111 1111 1111 111X	L	H	524287 Add.	------

16-BIT BUS ORGANIZATION ($\overline{CE1}$ = VIL, $\overline{CE2}$ = VIL)

A18 to A0	$\overline{CE2}$	$\overline{CE1}$	D15–D8	D7–D0
000 0000 0000 0000 000X	L	L	1 Add.	0 Add.
000 0000 0000 0000 001X	L	L	3 Add.	2 Add.
000 0000 0000 0000 010X	L	L	5 Add.	4 Add.
000 0000 0000 0000 011X	L	L	7 Add.	6 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 100X	L	L	524281 Add.	524280 Add.
111 1111 1111 1111 101X	L	L	524283 Add.	524282 Add.
111 1111 1111 1111 110X	L	L	524285 Add.	524284 Add.
111 1111 1111 1111 111X	L	L	524287 Add.	524286 Add.

Notes: *1 H = VIH, L = VIL, X = Either 0 or 1.
*2 Even addresses are not available in this mode.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	V
Ground	GND		0		V
Input High Voltage	VIH	2.4		VCC+0.3	V
Input Low Voltage	VIL	–0.3		0.8	V
Ambient Temperature *	TA	0		55	°C

Note: * This value does not apply to the replaceable lithium battery. See VBAT1 in Fig.1.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Standby Supply Current	$\overline{CE}1$, $\overline{CE}2 \geq$ VCC –0.2V	ISB1			8.0	mA
	$\overline{CE}1$, $\overline{CE}2$ = VIH	ISB2			15.0	mA
Active Supply Current	VIN = VIH or VIL $\overline{CE}1$, $\overline{CE}2$ = VIL, IOUT = 0mA	ICC1			110	mA
Operating Supply Current	VIN = VIH or VIL, Cycle = Min. Duty = 100%, IOUT = 0mA $\overline{OE}$ = VIH during Write Cycle	ICC2			190	mA
Input Leakage Current *1	VIN = 0V to VCC	ILI	–10		10	µA
Output Leakage Current *2	VOUT = 0V to VCC, $\overline{CE}1$, CE2=VIH or $\overline{OE}$ = VIH or $\overline{WE}$ = VIL	ILI/O	–10		10	µA
Output High Voltage *3	IOH = –1.0mA	VOH	2.4			V
Output Low Voltage	IOL = 2.1mA	VOL			0.4	V

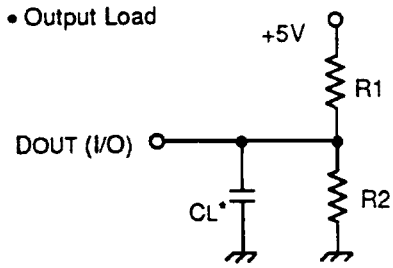
Notes: *1 This value does not apply to $\overline{CE}1$, $\overline{CE}2$, $\overline{REG}$ and $\overline{WE}$.
*2 This value does not apply to BVD1, BVD2, $\overline{CD}1$, $\overline{CD}2$ and WP.
*3 This value does not apply to BVD1, BVD2. $\overline{CD}1$ and $\overline{CD}2$.

CAPACITANCE (TA=25°C, f=1MHz, VIN=VI/O=GND)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance *1	CIN			50	pF
I/O Capacitance *2	COUT			50	pF

Notes: *1 This value does not apply to $\overline{CE}1$, $\overline{CE}2$, $\overline{REG}$ and $\overline{WE}$.
*2 This value does not apply to BVD1, BVD2, $\overline{CD}1$ and $\overline{CD}2$.

Fig. 3 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.6V
- Input Pulse Rise and Fall Times: 5ns (Transition between 0.8V and 2.4V)
- Timing Reference Levels
  Input: VIL = 0.8V, VIH = 2.4V
  Output: VOL = 0.8V, VOH = 2.0V

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8kΩ	990Ω	100pF	All parameters except tCLZ, tOLZ, tCHZ, tOHZ, tRCLZ, tROLZ, tRCHZ, tROHZ, tWLZ and tWHZ
Load II	1.8kΩ	990Ω	5pF	tCLZ, tOLZ, tCHZ, tOHZ, tRCLZ, tROLZ, tRCHZ, tROHZ, tWLZ and tWHZ

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRC	200		ns
Address Access Time	tAA		200	ns
Card Enable Access Time	tCE		200	ns
Output Enable Access Time	tOE		100	ns
Output Hold from Address Change	tOH	5		ns
Card Enable to Output Low-Z *1*2	tCLZ	5		ns
Output Enable to Output Low-Z *1*2	tOLZ	5		ns
Card Enable to Output High-Z *1*2	tCHZ		50	ns
Output Enable to Output High-Z *1*2	tOHZ		50	ns

ATTRIBUTE MEMORY READ CYCLE *3

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRRC	300		ns
Address Access Time	tRAA		300	ns
Card Enable Access Time	tRCE		300	ns
Output Enable Access Time	tROE		150	ns
Output Hold from Address Change	tROH	5		ns
Card Enable to Output Low-Z *1*2	tRCLZ	5		ns
Output Enable to Output Low-Z *1*2	tROLZ	5		ns
Card Enable to Output High-Z *1*2	tRCHZ		60	ns
Output Enable to Output High-Z *1*2	tROHZ		60	ns

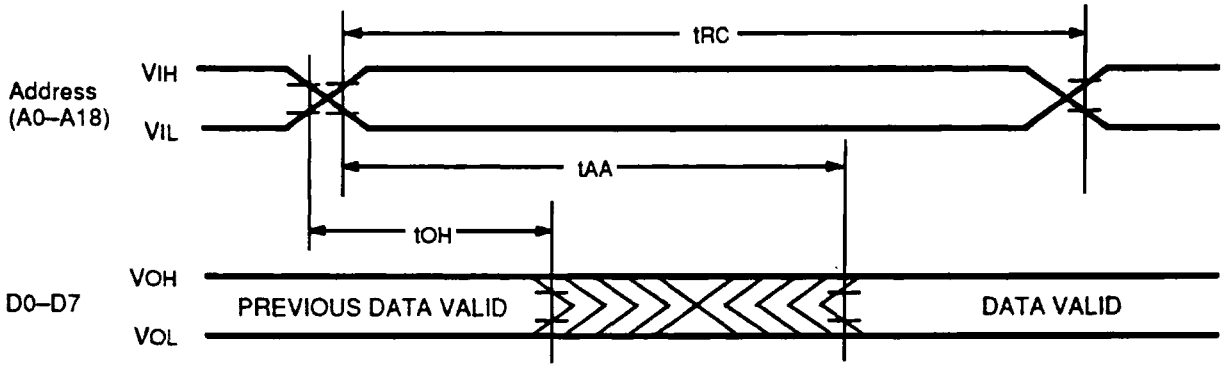
Notes: *1 Transition is measured at the point of ±500mV from steady state voltage.
*2 This parameter is specified using Load II in Fig.2.
*3 This parameter is for MB98A90603, 90703, 90803, and 90903.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

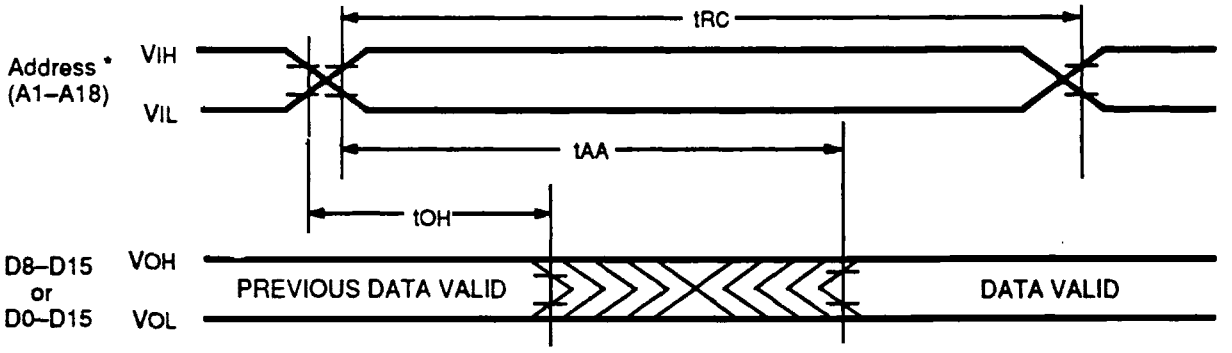
MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIH)

READ CYCLE 1: $\overline{CE1}$ = $\overline{OE}$ = VIL, $\overline{CE2}$ = VIH : x 8-bit Bus Organization



READ CYCLE 2: $\overline{CE1}$ = VIH, $\overline{CE2}$ = $\overline{OE}$ = VIL: x 8-bit Bus Organization

$\overline{CE1}$ = $\overline{CE2}$ = $\overline{OE}$ = VIL: x 16-bit Bus Organization



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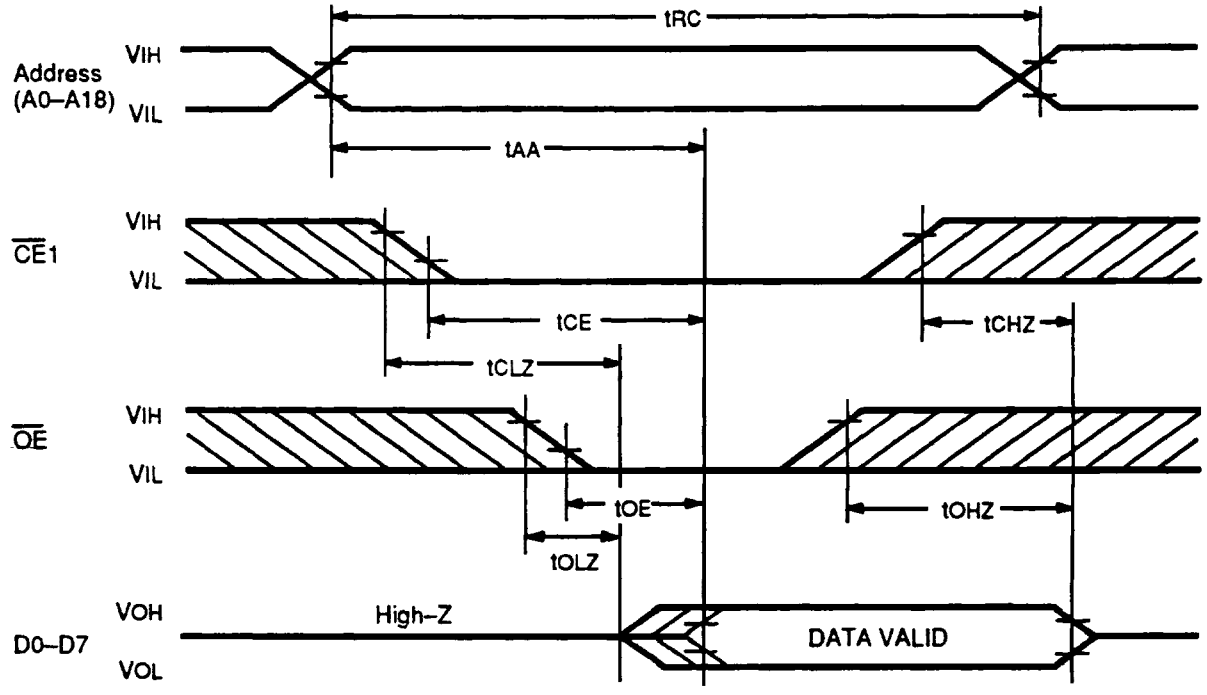
Note: * A0 = Either VIH or VIL.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIH)

READ CYCLE 3: $\overline{CE2}$ = VIH: x 8-bit Bus Organization

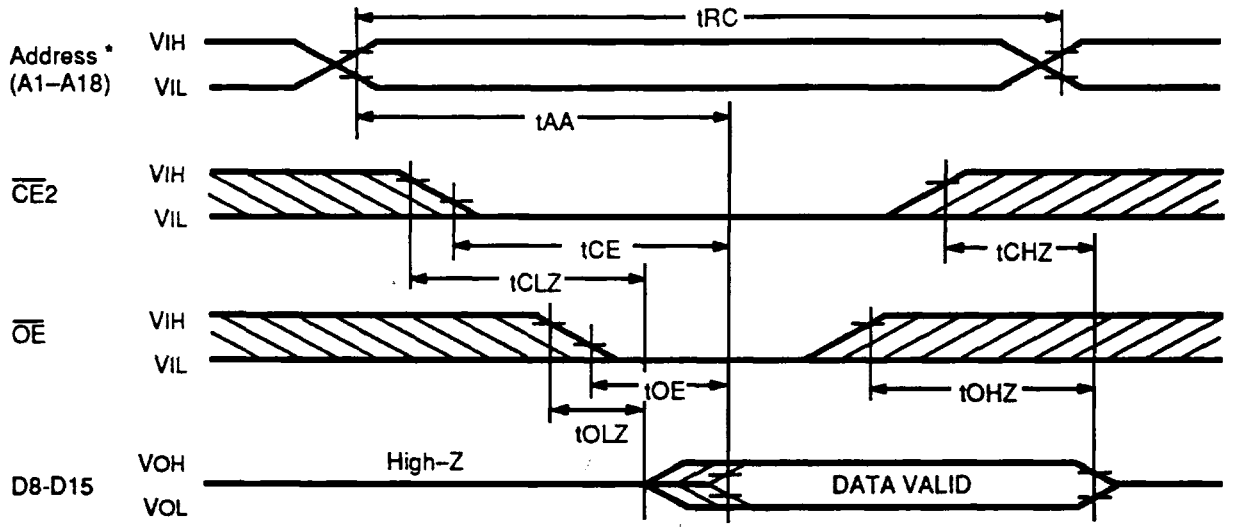


AC CHARACTERISTICS (Continued)

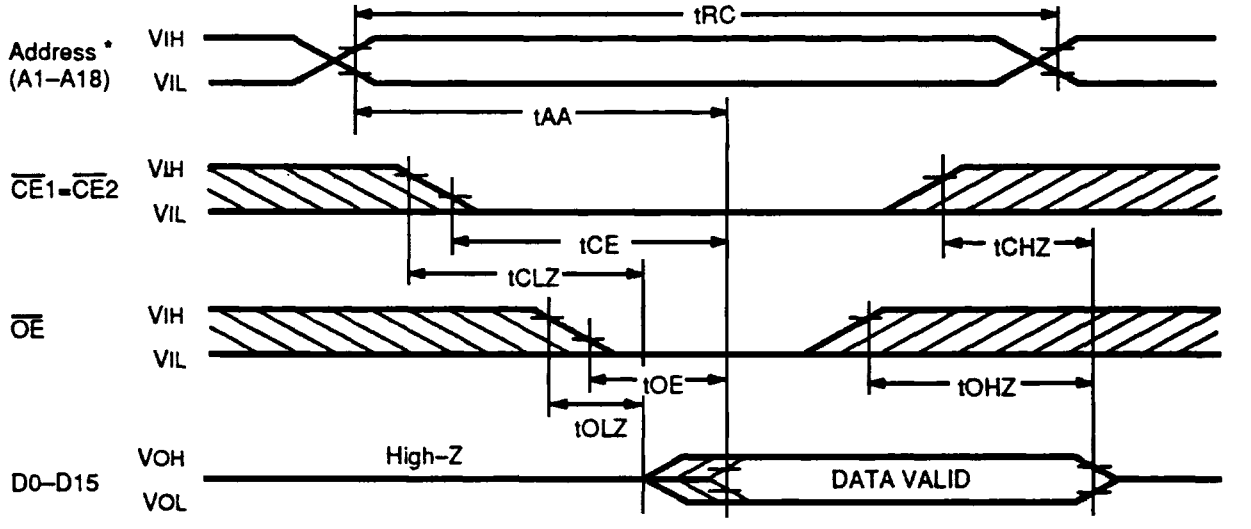
(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIH)

READ CYCLE 4: $\overline{CE1}$ = VIH: x 8-bit Bus Organization



READ CYCLE 5: $\overline{CE1}$ = $\overline{CE2}$: x 16-bit Bus Organization



:Undefined

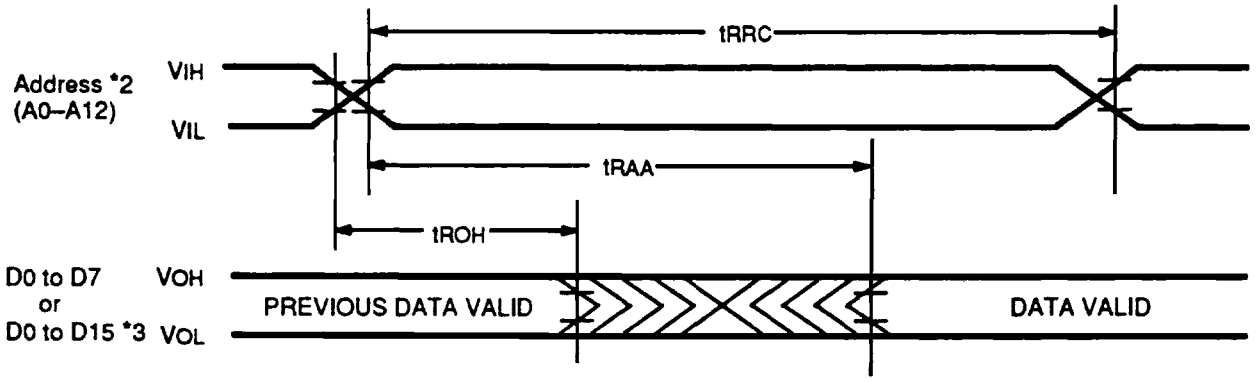
Note: * A0 = Either VIH or VIL.

AC CHARACTERISTICS (Continued)

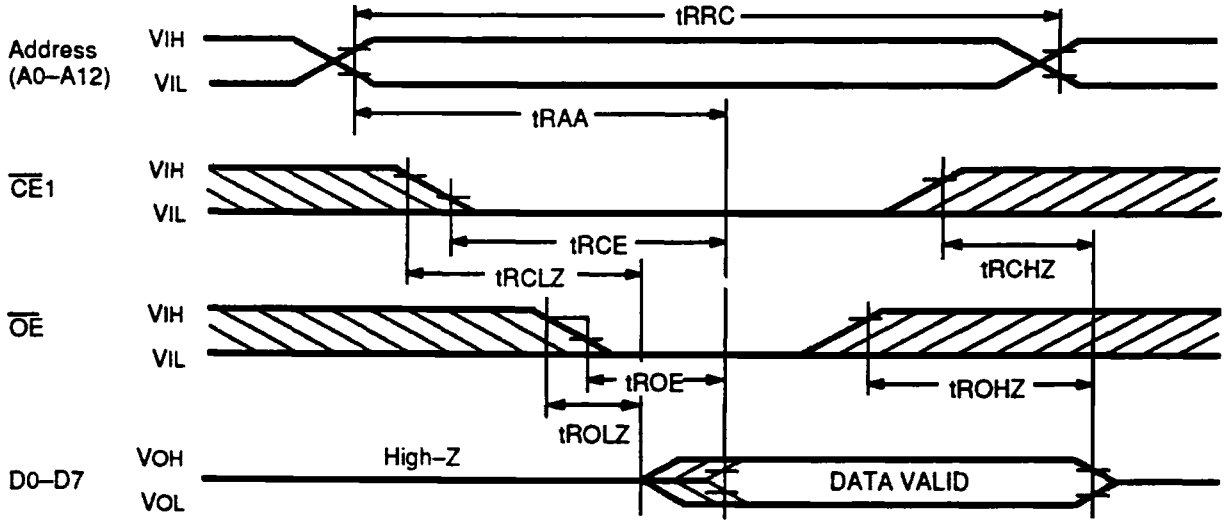
(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIL) *1

READ CYCLE 1: $\overline{CE1}$ = $\overline{OE}$ = VIL, $\overline{CE2}$ = VIH : x 8–bit Bus Organization
$\overline{CE1}$ = $\overline{CE2}$ = $\overline{OE}$ = VIL : x 16–bit Bus Organization



READ CYCLE 2: $\overline{CE2}$ = VIH: x 8–bit Bus Organization

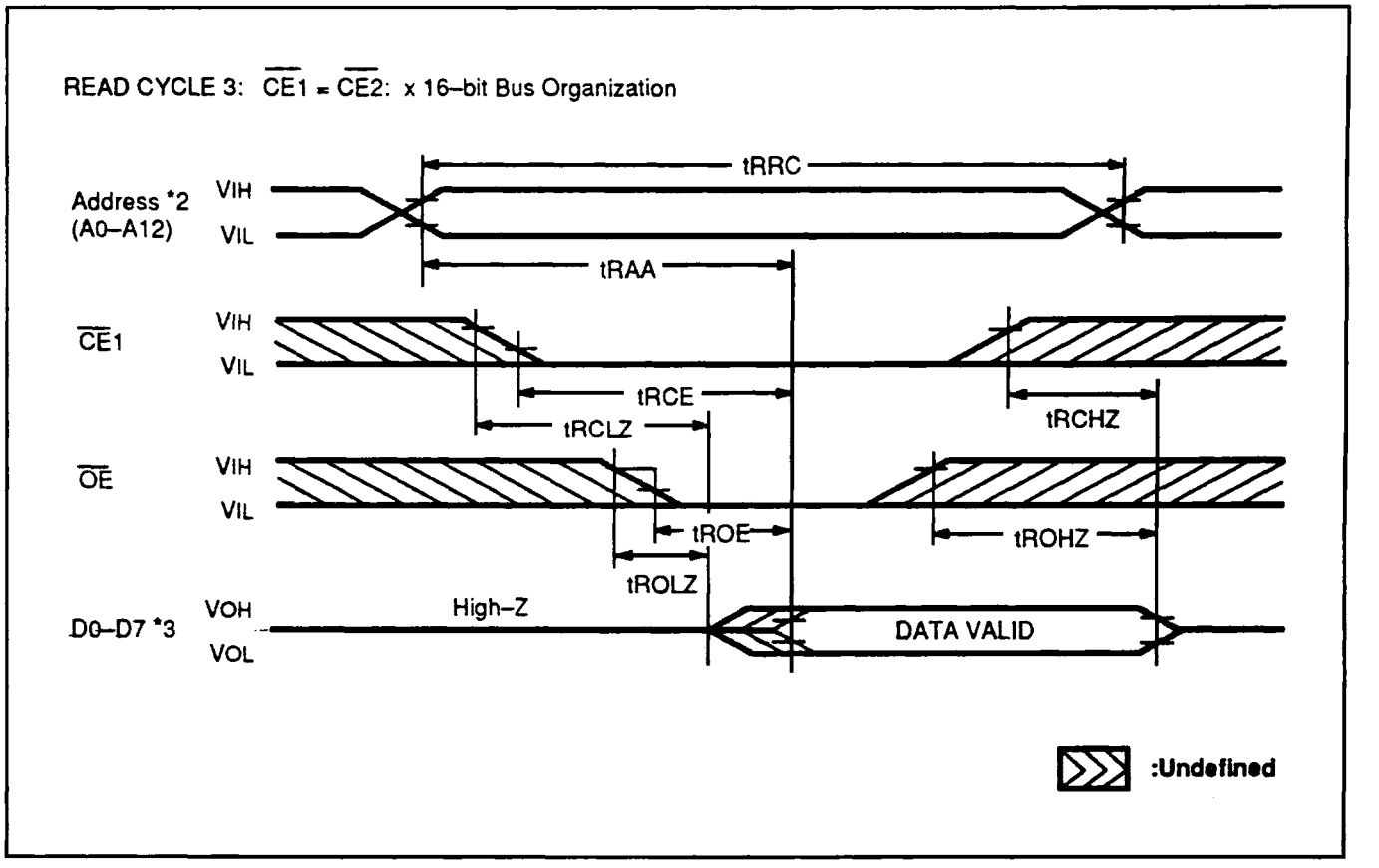


Notes: *1 This timing diagram is for MB98A90603, 90703, 90803, and 90903. "FF" data is available on MB98A90602, 90702, 90802, and 90902 only
*2 A0 = Either VIH or VIL for a 16-bit bus organization.
*3 H-level is output from D8 to D15.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH, $\overline{REG}$ = VIL) *1



Notes: *1 This timing diagram is for MB98A90603, 90703, 90803, and 90903. "FF" data is available on MB98A90602, 90702, 90802, and 90902 only.
*2 A0 = Either VIH or VIL.
*3 H-level is output from D8 to D15.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE *1

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	tWC	200		ns
Address Valid to End of Write	tAW	140		ns
Chip Select to End of Write	tCW	140		ns
Data Valid to End of Write	tDW	60		ns
Data Hold Time	tDH	30		ns
Write Pulse Width	tWP	120		ns
Address Setup Time	tAS	20		ns
Write Recovery Time	tWR	30		ns
Output Enable to Output Low-Z *2	tOLZ	5		ns
Output Enable to Output High-Z *2	tOHZ		50	ns
Write Enable to Output Low-Z *2*3	tWLZ	5		ns
Write Enable to Output High-Z *2*3	tWHZ		50	ns
Output Enable Setup Time	tOES	10		ns
Output Enable Hold Time	tOEH	10		ns

ATTRIBUTE MEMORY WRITE CYCLE *4

Parameter	Symbol	Min	Max	Unit
Byte Write Cycle Time	tRWR		10	ms
Address Setup Time	tRAS	20		ns
Chip Enable Setup Time	tRCS	0		ns
Output Enable Setup Time	tROES	20		ns
Write Pulse Width	tRWP	100		ns
Address Hold Time	tRAH	50		ns
Data Setup Time	tRDS	50		ns
Data Hold Time	tRDH	20		ns
Chip Enable Hold Time	tRCH	0		ns
Output Enable Hold Time	tROEH	20		ns
Write Recovery Time	tRRE	50		ns
End of Write to Output Time	tRRBO		100	ns
Number of Write per Byte	N	10000		Times
Write Enable Hold Time	tRWEH	10		ns

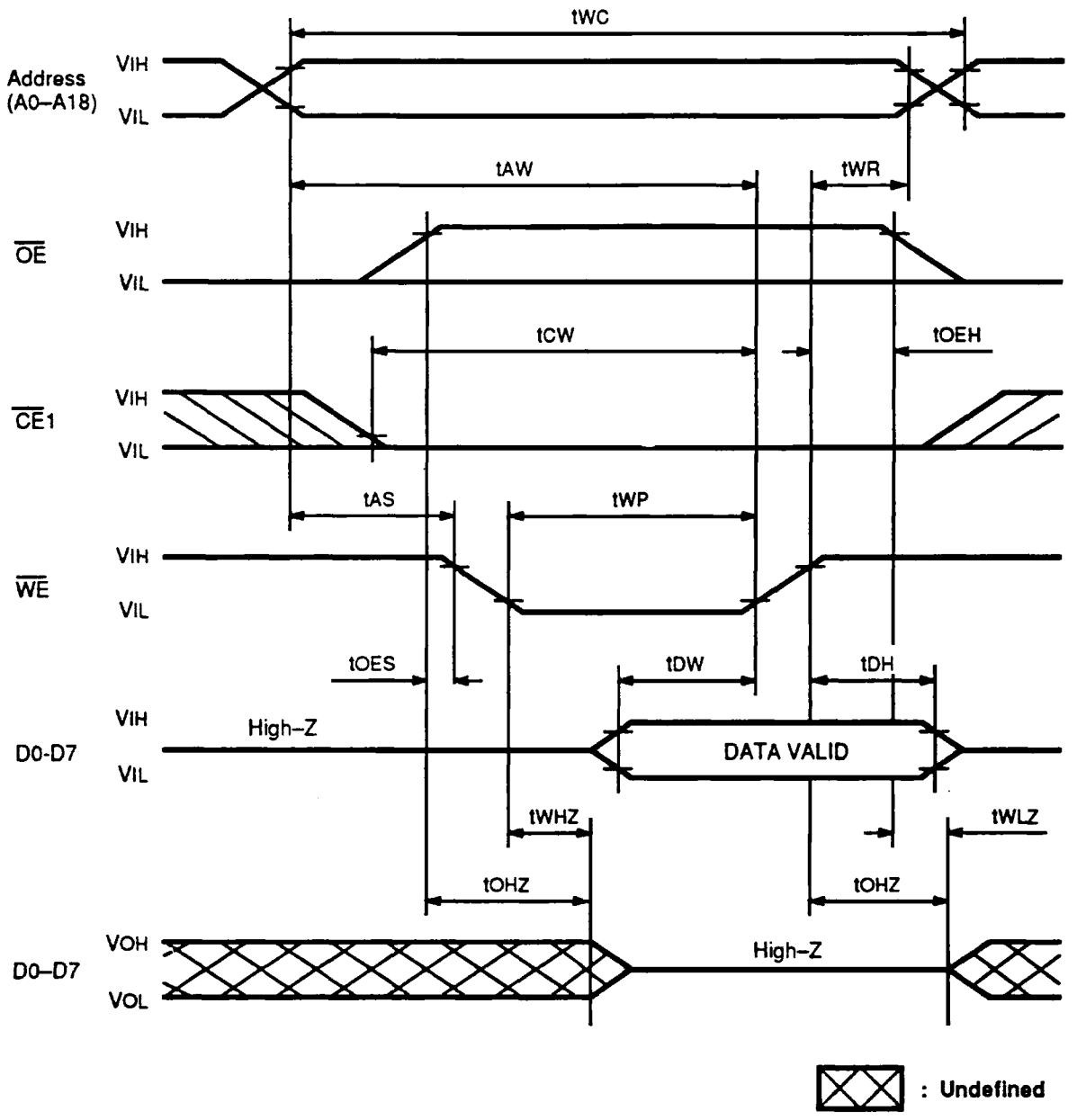
Notes: *1 If $\overline{OE}$, $\overline{CE1}$, and $\overline{CE2}$ are in the Read Mode during this period, then the I/O pins are in the output state and the input signals of the phase opposite to the outputs must be applied.
*2 Transition is measured at the point of ±500mV from steady state voltage.
*3 This parameter is specified only during write cycle with $\overline{OE}$ = VIL and specified using Load II in Fig.2.
*4 This parameter is for MB98A90603, 90703, 90803, and 90903.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = VIH)

WRITE CYCLE 1: $\overline{CE2}$ = VIH : x 8-bit Bus Organization

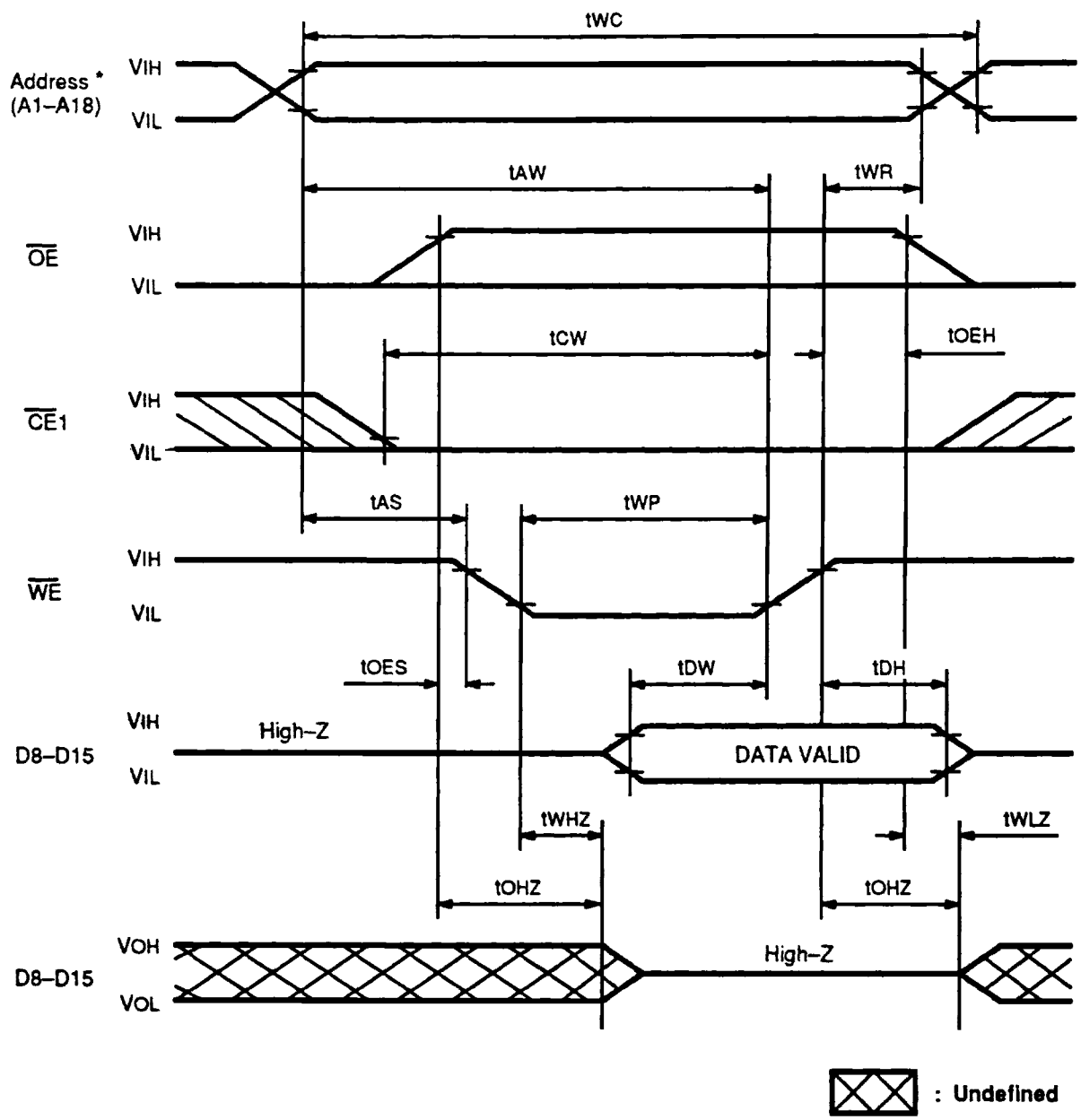


AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = VIH)

WRITE CYCLE 2: $\overline{CE1}$ = VIH : x 8-bit Bus Organization



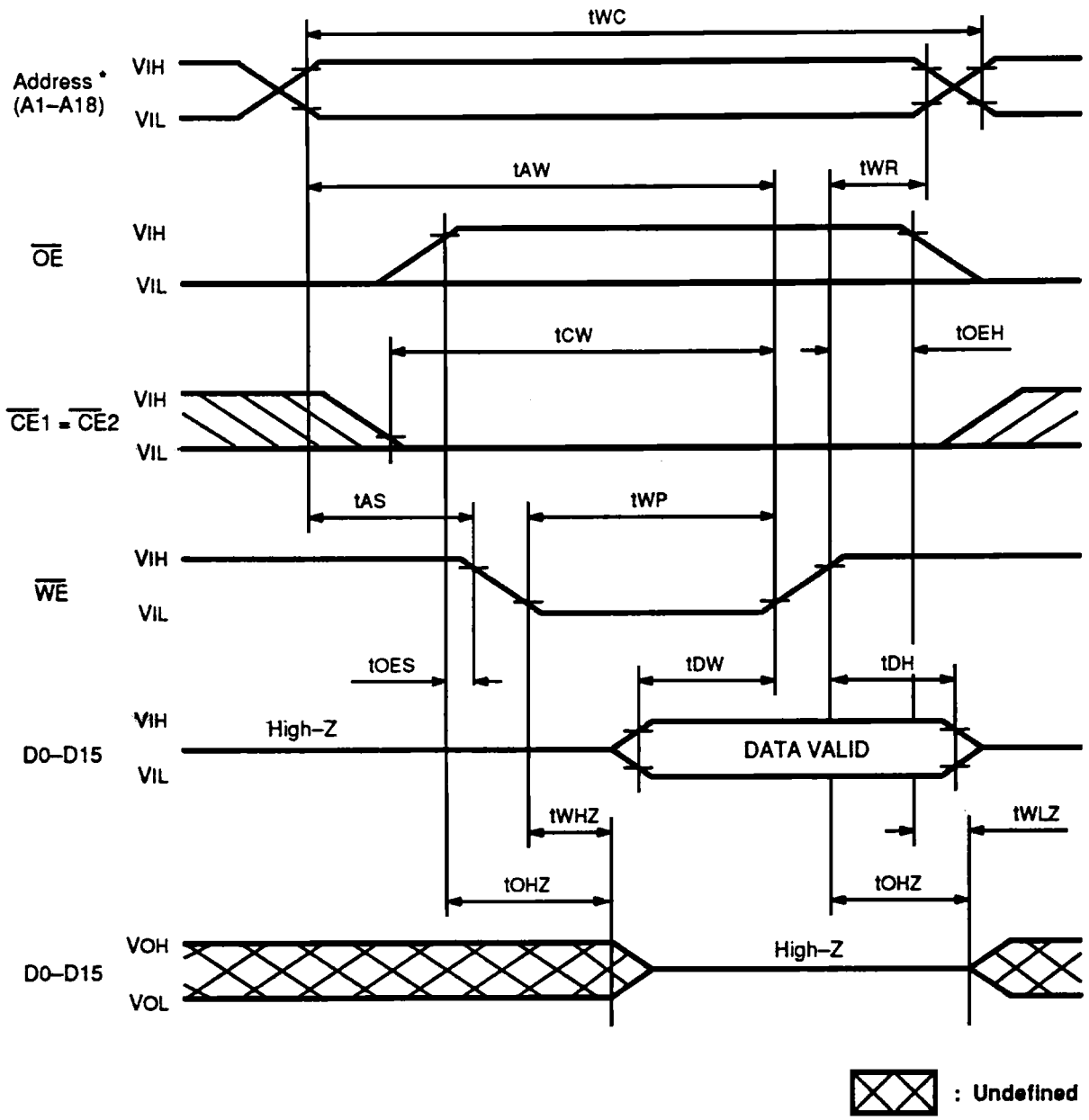
Note: * A0 = Either VIH or VIL.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED, $\overline{REG}$ = VIH)

WRITE CYCLE 3: $\overline{CE1}$ = $\overline{CE2}$: x 16–bit Bus Organization



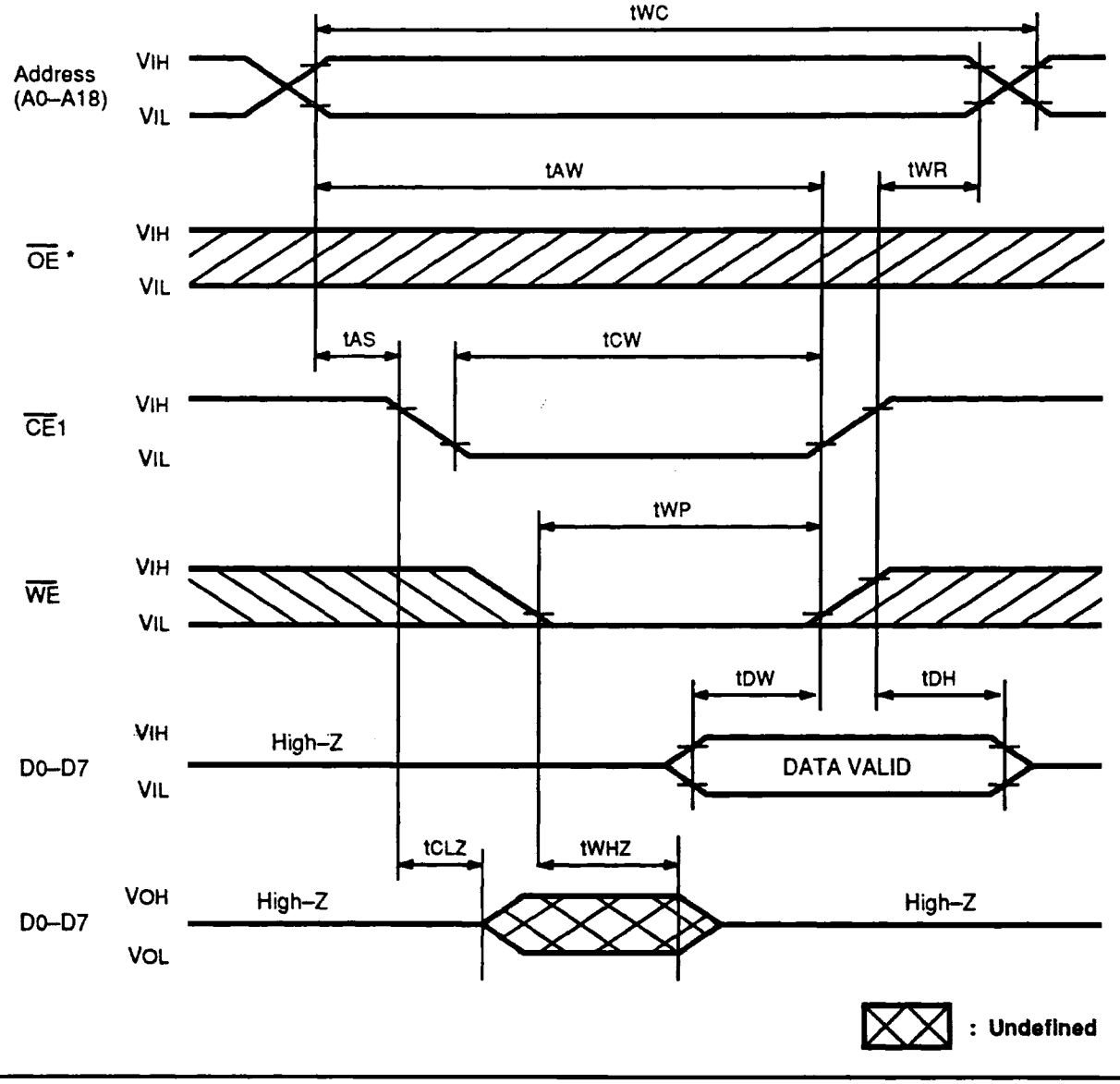
. Note: * A0 = Either VIH or VIL.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = VIH)

WRITE CYCLE 4: $\overline{CE2}$ = VIL : x 8–bit Bus Organization



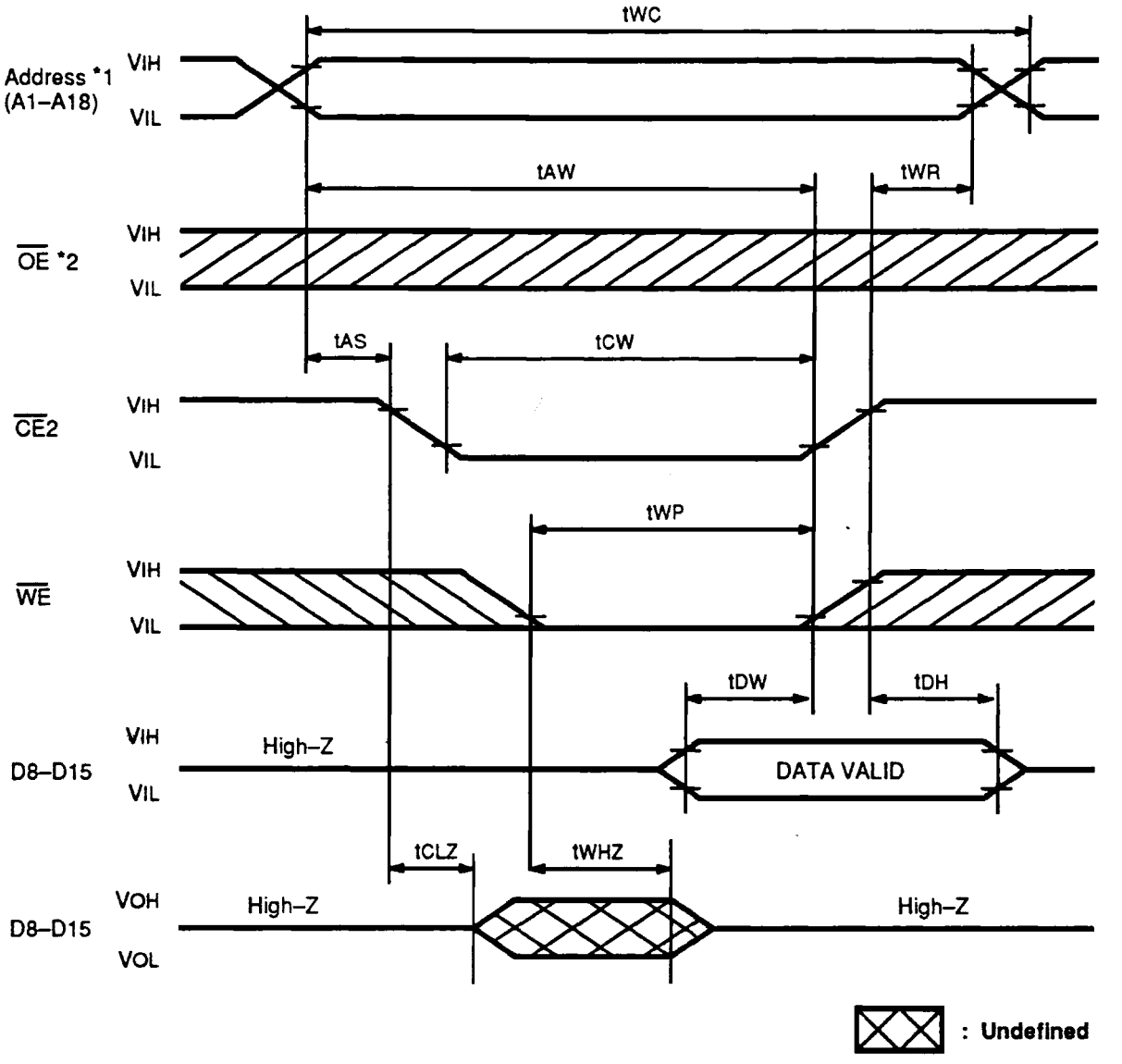
Note: * H-level is recommended for stable operation though the card is operable at L-level.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = VIH)

WRITE CYCLE 5: $\overline{CE1}$ = VIL : x 8-bit Bus Organization



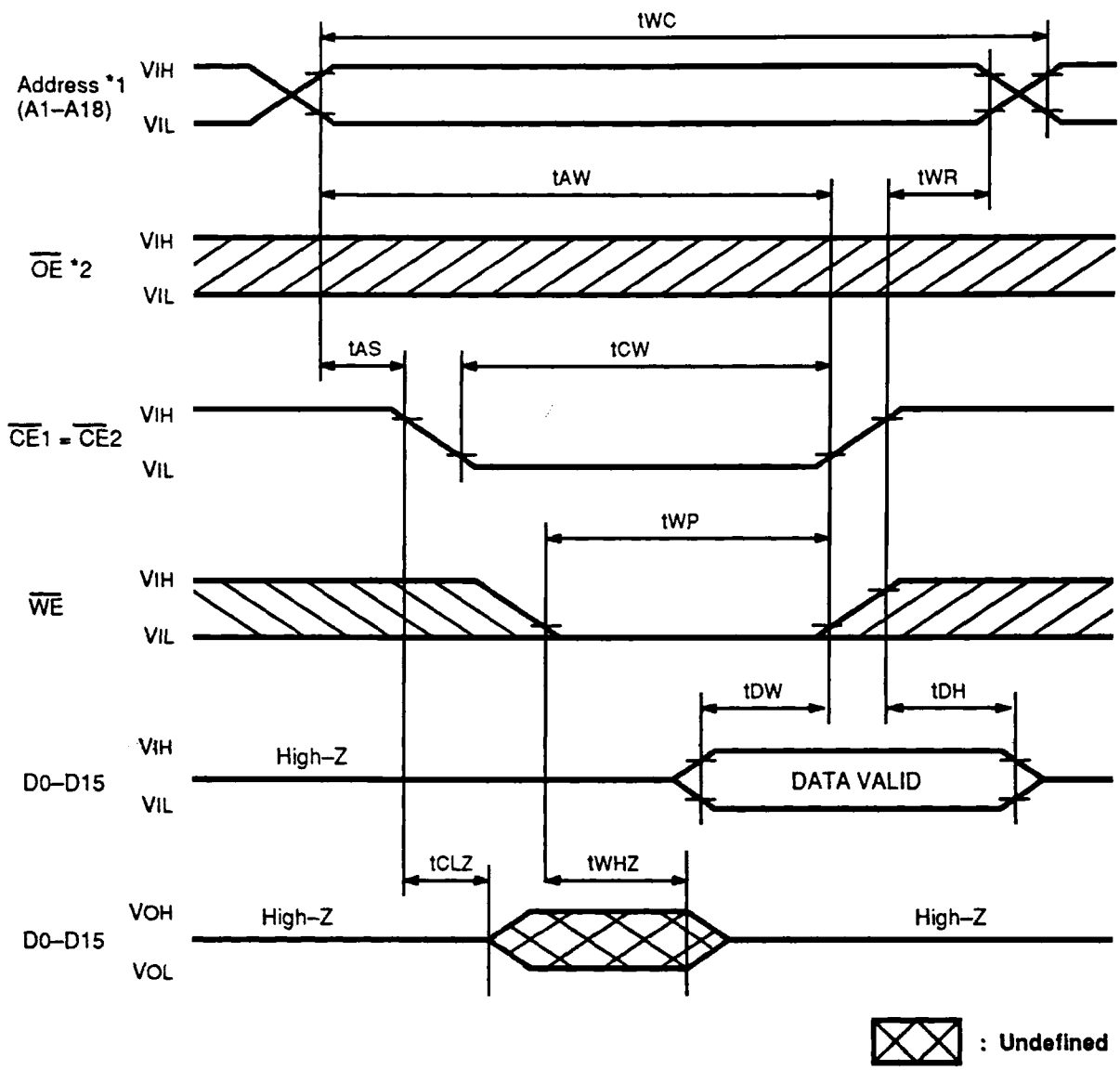
Notes: *1 A0 = Either VIH or VIL.
*2 H-level is recommended for stable operation though the card is operable at L-level.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$ = CONTROLLED, $\overline{REG}$ = VIH)

WRITE CYCLE 6: $\overline{CE1}$ = $\overline{CE2}$: x 16-bit Bus Organization



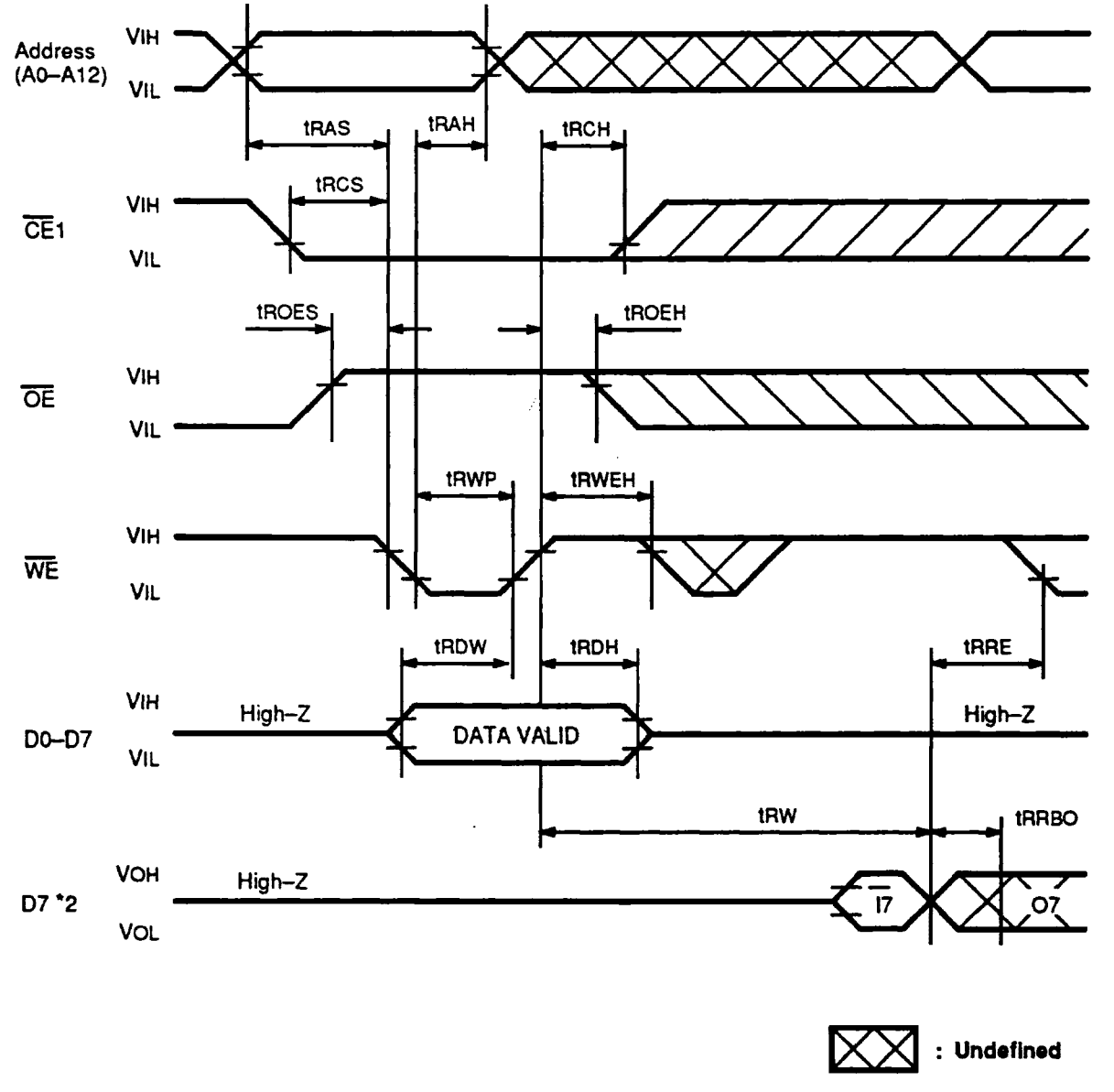
Notes: *1 A0 = Either VIH or VIL.
*2 H-level is recommended for stable operation though the card is operatable at L-level.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$=CONTROLLED, $\overline{REG}$ = VIL) *1

WRITE CYCLE 1: $\overline{CE2}$ = VIH : x 8-bit Bus Organization



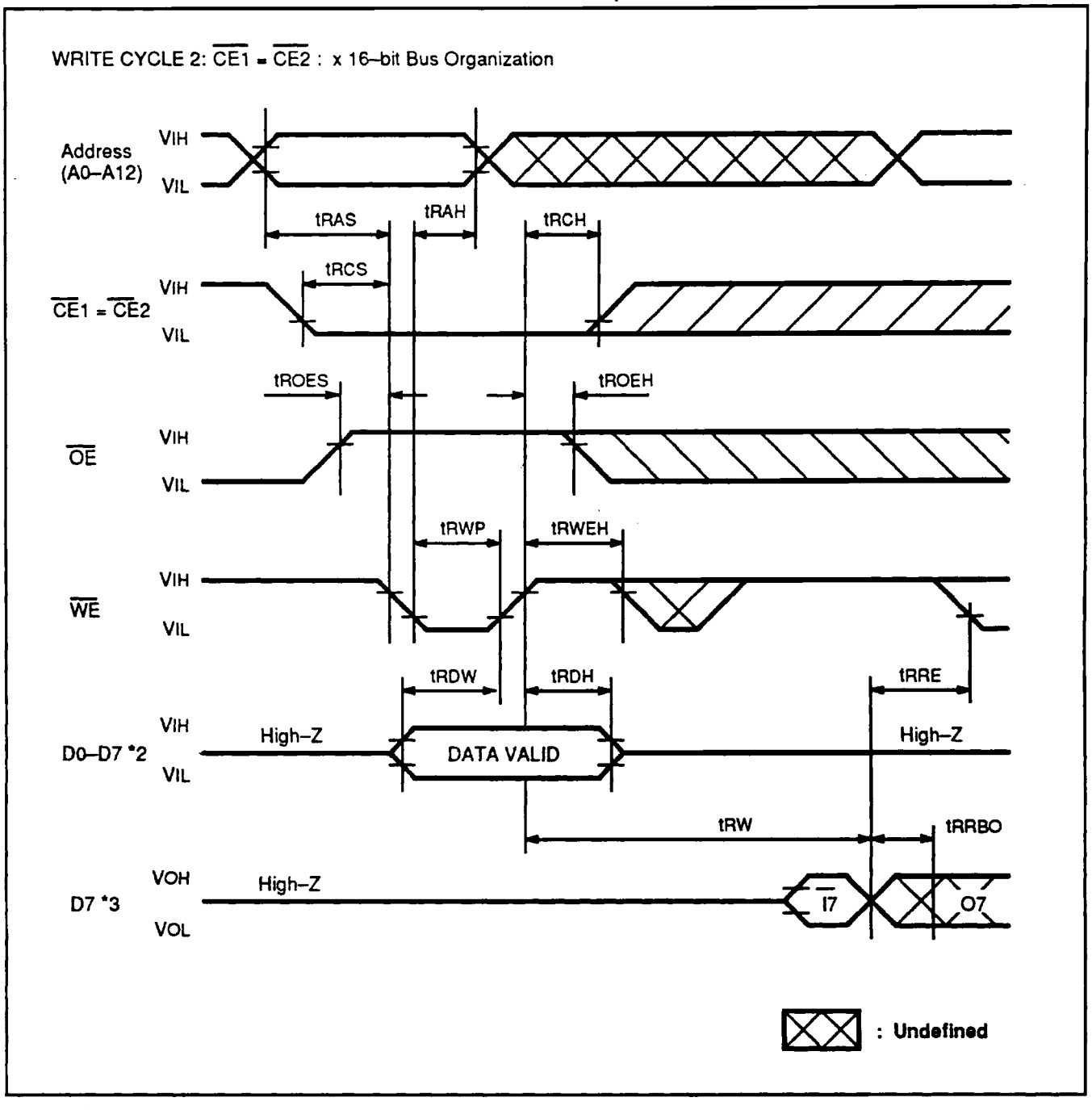
Notes: *1 This timing diagram is for MB98A90603, 90703, 90803, and 90903. "FF" data is available on MB98A90602, 90702, 90802, and 90902 only.

*2 Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$=CONTROLLED, $\overline{REG}$ = VIL) *1



Notes: *1 This timing diagram is for MB98A90603, 90703, 90803, and 90903. "FF" data is available on MB98A90602, 90702, 90802, and 90902 only.

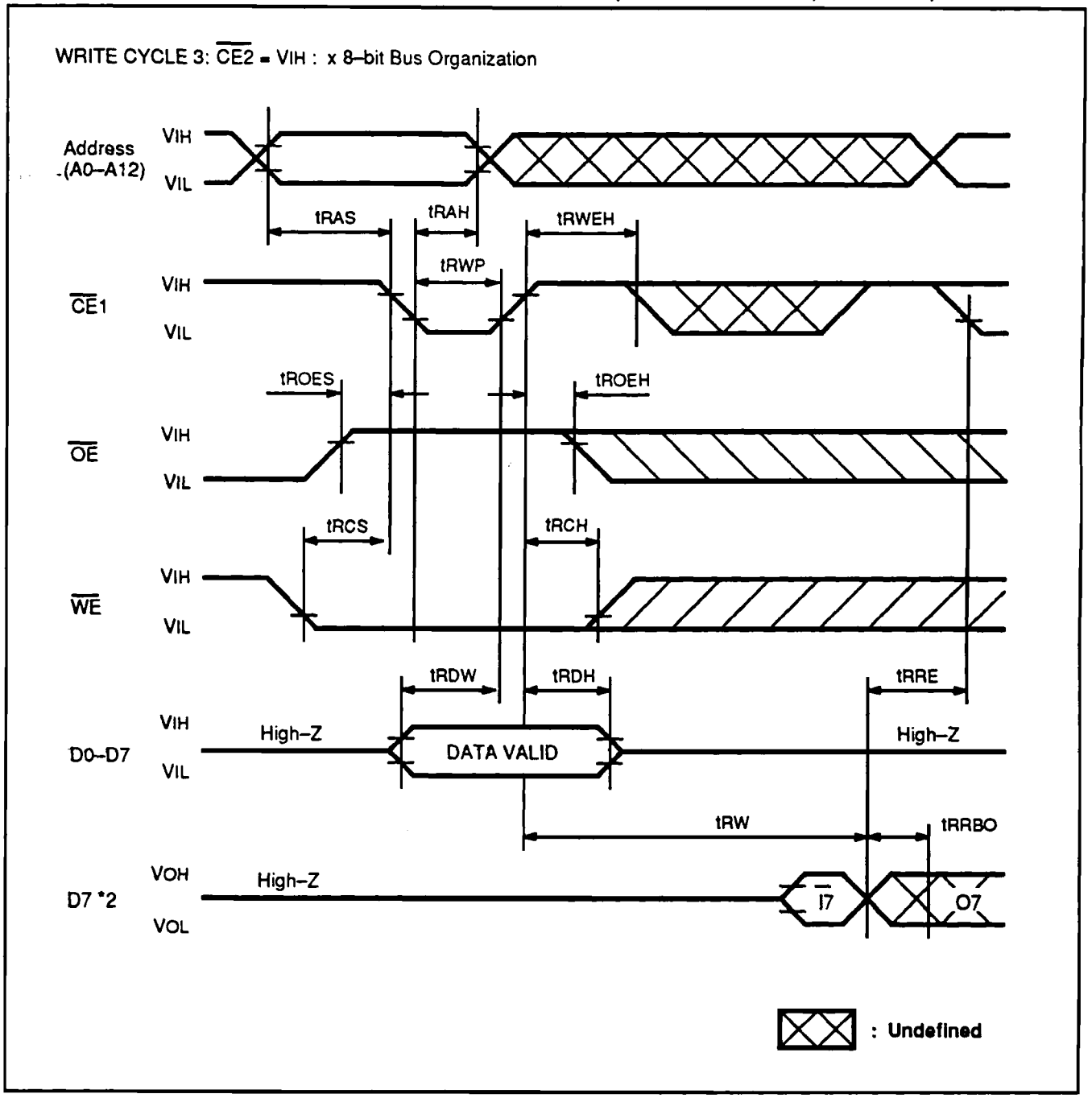
*2 H-level or L-level is output from D8 to D15.

*3 Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$=CONTROLLED, $\overline{REG}$ = VIL) *1



Notes: *1 This timing diagram is for MB98A90603, 90703, 90803, and 90903. "FF" data is available on MB98A90602, 90702, 90802, and 90902 only.

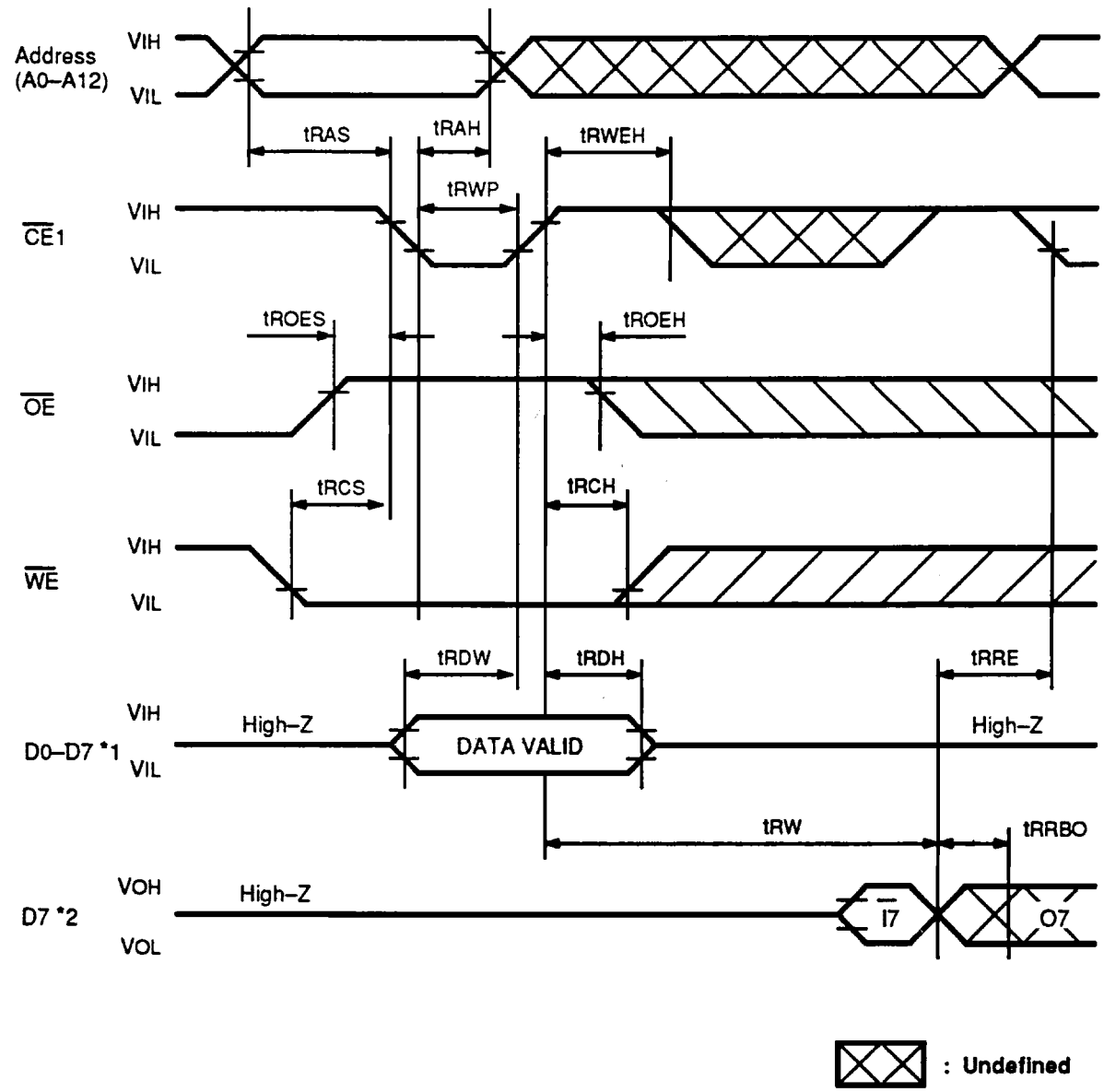
*2 Data polling operation.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ($\overline{CE}$=CONTROLLED, $\overline{REG}$ = VIL) *1

WRITE CYCLE 4: $\overline{CE1}$ = $\overline{CE2}$: x 16-bit Bus Organization

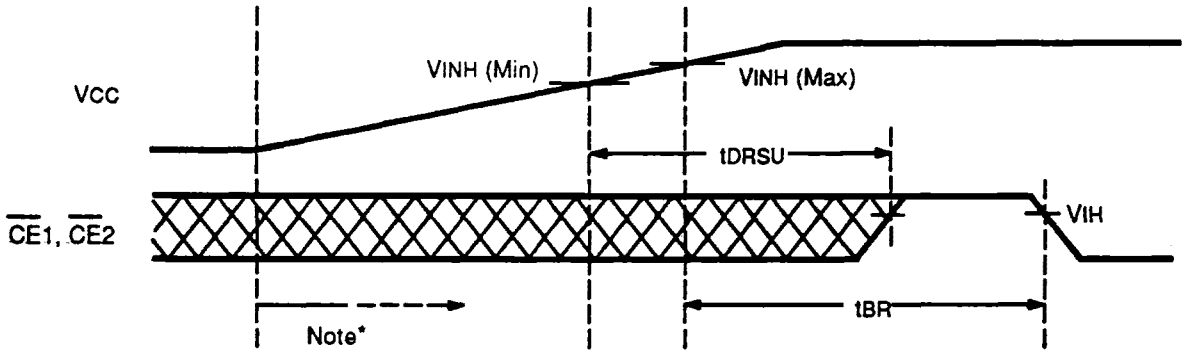


Notes: *1 This timing diagram is for MB98A90603, 90703, 90803, and 90903. "FF" data is available on MB98A90602, 90702, 90802, and 90902 only.
*2 H-level or L-level is output from O8 to O15.
*3 Data polling operation.

POWER SUPPLY SEQUENCE CHARACTERISTICS

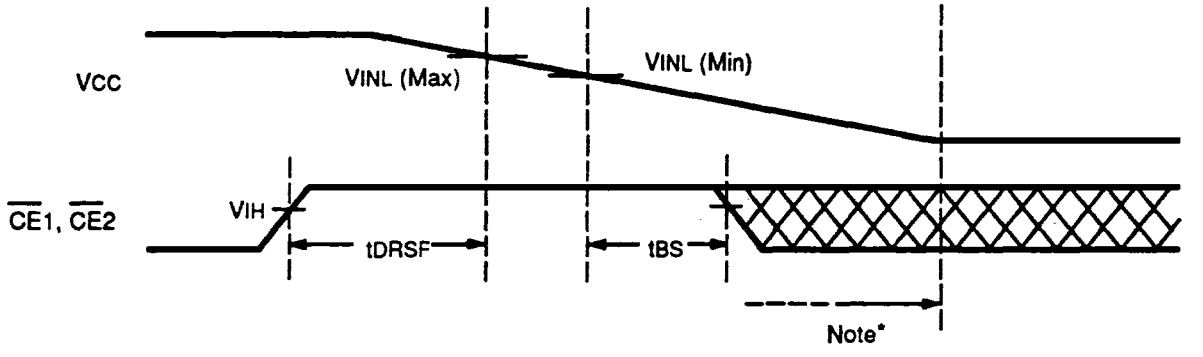
Parameter	Symbol	Min	Typ	Max	Unit
Detection Rising Voltage	VINH	4.2	4.3	4.4	V
Detection Falling Voltage	VINL	4.1	4.2	4.3	V
Battery Backup Recovery Time	tBR	3.0			ms
Data Retention Rising Time	tDRSU			0.5	ms
Battery Backup Setup Time	tBS	10			µs
Data Retention Falling Time	tDRSF	0			ns

POWER -ON TIMING DIAGRAM



Note: * Insertion or removal of the card is not recommended when VCC is greater than 0V.

POWER -OFF TIMING DIAGRAM



Note: * Insertion or removal of the card is not recommended when VCC is greater than 0V.

UNIQUE FEATURES FOR SRAM CARD

1. REPLACEABLE BATTERIES FOR THE SRAM MEMORY CARD

The battery used in the SRAM Memory Card is a 3V Lithium battery (coin type) with the following specifications:

Diameter : 23.0 (mm)
Thickness : 2.5 (mm)
Weight : 3.2 (g) Approx.
Type : CR2325, or equivalent

2. APPROXIMATE DATA RETENTION TIME WITH BATTERY SUPPORT ONLY

Part Number	Approx. Data Retention Time * (TA=20°C)
MB98A9060x	4 years min.
MB98A9070x	2 years min.
MB98A9080x	1 year min.
MB98A9090x	6 months min.

* Determined by the memory density of the card;
i.e., greater card density means less battery time.

3. REPLACING THE BATTERY IN THE SRAM MEMORY CARD

a. Insert a slender pointed object, such as the end of a paper clip, into the hole on the upper side of the card. (See Fig. 3.)

b. Release the battery holder by pressing the paper clip against the catch and pulling the battery holder straight out from the card. (The battery cavity is located at the top of the card. See Fig. 4.) When the battery holder is free from the card the battery will fall out.

c. Replace the old battery with a fresh one. Be certain to match battery polarity to the + and – shown on the holder.

d. Place the new battery into the holder, squeeze the holder containing the new battery tightly, and reinsert it into the battery cavity.

WARNING
Battery MUST be replaced within 30 minutes* or data will be lost.

Note: *With condition that the SRAM card had been inserted into application system more than 10 minutes.

Fig. 3 – SRAM CARD DRAWING (TOP VIEW)

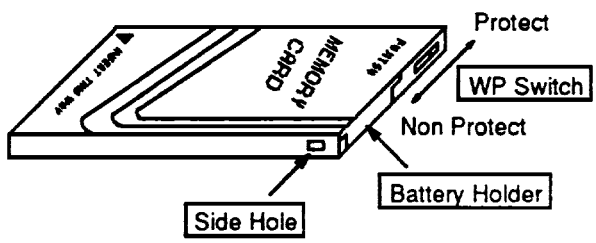
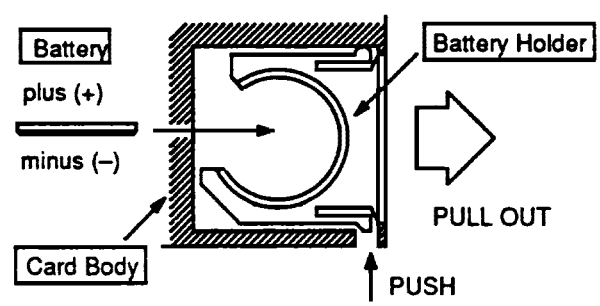


Fig.4 – BATTERY CASE DRAWING (TOP VIEW)



UNIQUE FEATURES FOR SRAM CARD (Continued)

4. SPECIAL MONITORING PINS

4.1 BVD1, BVD2: Voltage Monitoring Pins

These pins monitor the voltage of the battery which must be maintained at 2.65V or greater for data retention. The condition of the battery is determined by reading the output signals on BVD1 and BVD2.

1. When *BVD1=BVD2=VOH*
   Battery voltage is sufficient to guarantee data retention; i.e., ≥2.65V.

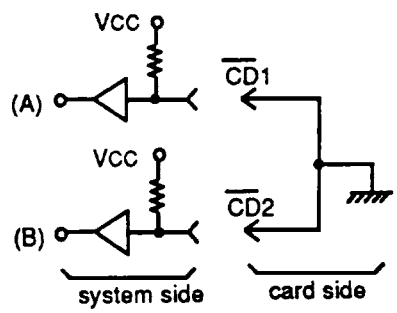
2. When *BVD2=VOL, BVD1=VOH*
   Battery voltage is lower than 2.65V and should be replaced to safeguard data.

3. When *BVD1=BVD2=VOL*
   Battery voltage is less than 2.37V: the level is dangerous. There is a possibility that data has not retained.

* If the battery is removed, BVD1, BVD2 will not function.

4.2 $\overline{CD1}$, $\overline{CD2}$: Card Detection Pins

These pins detect the insertion of the card into the system. (See Fig. 5.)
When the memory card has been correctly inserted, $\overline{CD1}$ and $\overline{CD2}$ are detected by the system. $\overline{CD1}$, $\overline{CD2}$ are tied to ground on the card side as shown in Fig. 5.



– Fig. 5 –

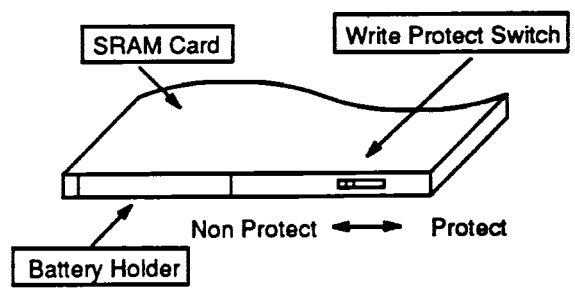
4.3 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 6, the SRAM card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the WE pin low. L–level is output on the WP pin.

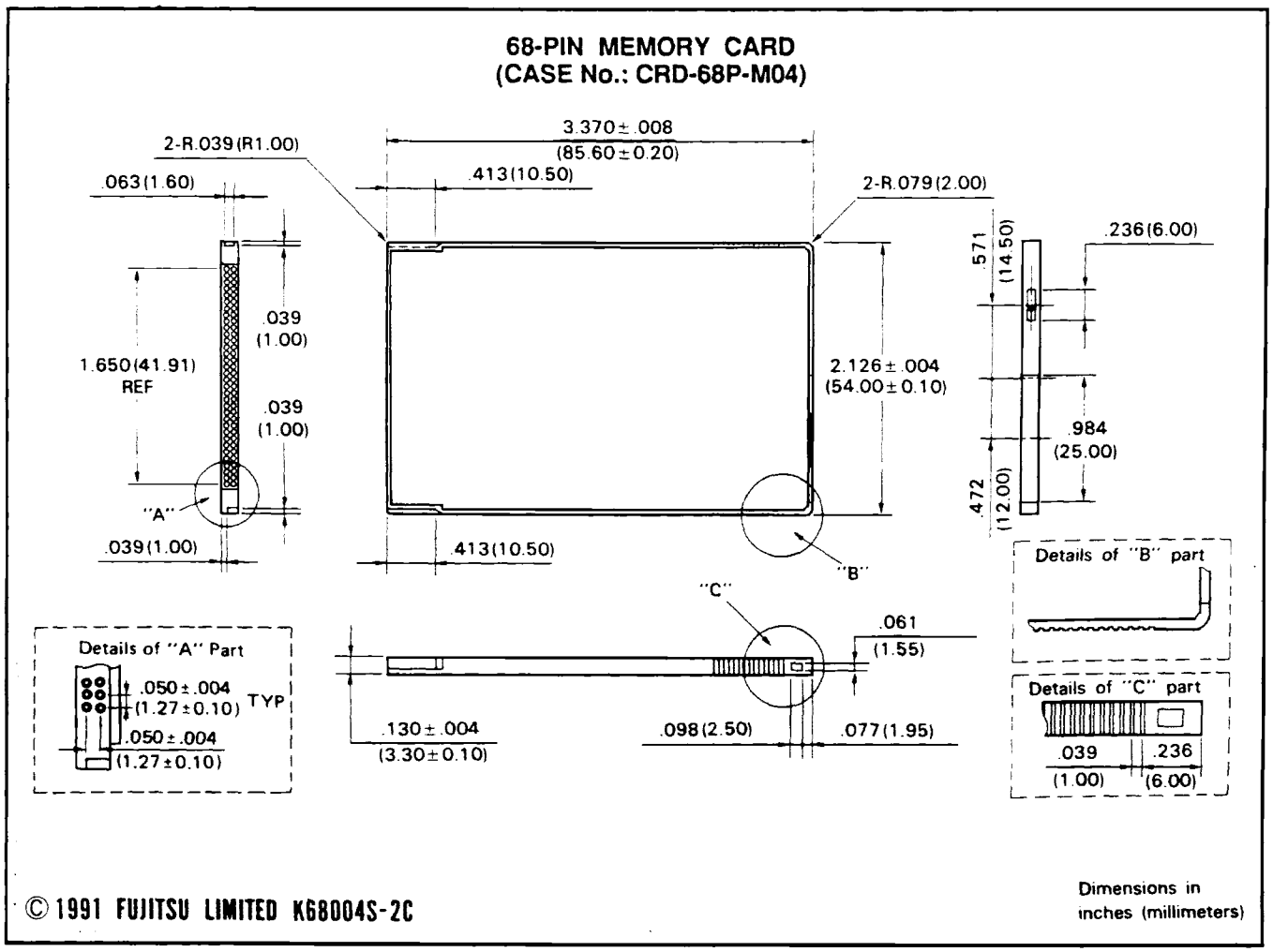
To prevent writing to the card, the switch must be turned to the "Protect" position. H–level is output on the WP pin.

WP Switch	WP
Protect	H
Non Protect	L



– Fig. 6 –

PACKAGE DIMENSIONS



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