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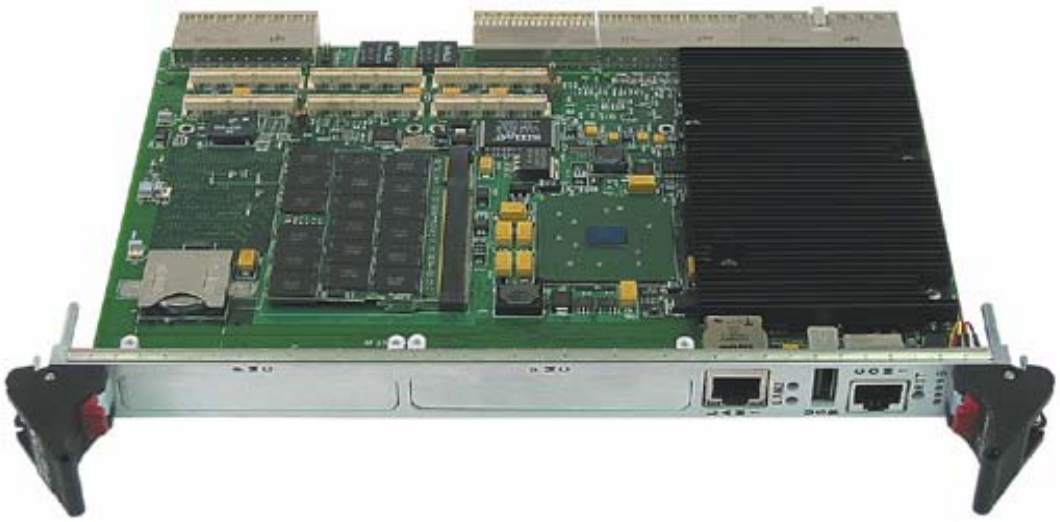
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GE Fanuc Automation



VMICPCI-7808

Intel® Pentium®/Celeron® M Universal CompactPCI® Single Board Computer

PRODUCT MANUAL
500-657808-000 REV. C

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Overview

Introduction

GE Fanuc Embedded Systems' VMICPCI-7808 is a full featured Pentium® M or Celeron® M based, single board computer (SBC) in a single-slot, passively cooled, Eurocard form factor. This product utilizes the advanced technology of Intel®'s 855GME chipset. The VMICPCI-7808 is compliant with the CompactPCI® Specification PICMG® 2.0, Rev. 3.0 and features a universal PCI-to-PCI bridge. This allows the board to function as a system controller or peripheral CPU in multi-CPU systems.

The VMICPCI-7808 provides features typically found on desktop systems:

- Up to 2GB DDR SDRAM
- Built-in SVGA support (requires VMIACC-0591)
- Built-in Dual Gigabit Ethernet controller
- Ultra IDE drive support (requires VMIACC-0591)
- Serial ATA (requires VMIACC-0591)
- Floppy drive support (requires VMIACC-0591)
- USB 2.0 (one located on the front panel and two routed to the rear using the VMIACC-0591)
- Two RS232 serial ports (COM1 via front panel, COM2 via VMIACC-0591)
- Real-Time clock/calendar
- Front panel reset switch
- Miniature speaker
- Keyboard/Mouse port (requires VMIACC-0591)

The 855GME chipset allows the VMICPCI-7808 to provide enhanced features such as integrated video and Ultra ATA/100 IDE support. The VMICPCI-7808 is capable of executing many of today's desktop operating systems such as Microsoft®'s Windows® XP, Windows 2000 and a wide variety of Linux® based operating systems. The standard desktop features of the VMICPCI-7808 are described in Chapter 2 of this manual.

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The VMICPCI-7808 provides features useful to embedded applications such as:

- PICMG 2.16 support
- Universal CompactPCI support (system controller or peripheral)
- Remote Ethernet booting
- Up to 1GB of bootable CompactFlash (requires VMIACC-0591)
- Software-selectable Watchdog Timer with reset
- LVDS Flat Panel Video (requires VMIACC-0591)
- PICMG 2.9 support

Additionally, the VMICPCI-7808 offers two PMC expansion sites with front panel access and I/O routing to the J5 connector of the CompactPCI bus. The VMICPCI-7808 is capable of executing many of today's embedded operating systems such as VxWorks® or QNX®. The embedded features of the VMICPCI-7808 are described in Chapter 3 of this manual.

The VMICPCI-7808 is suitable for use in applications ranging from telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance processing power in a single CompactPCI slot is desired.

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Intel 855GME Chipset

The VMICPCI-7808 incorporates the latest Intel chipset technology, the 855GME. This chipset utilizes Advanced Hub Architecture (AHA). The AHA allows for increased system performance by separating many high-bandwidth I/O accesses from PCI accesses, relieving bottlenecks on the PCI bus. Furthermore, the 855GME chipset brings new levels of integration to motherboard chipsets and provides additional features such as Ultra ATA/100, Intergrated LVDS and Serial ATA (SATA).

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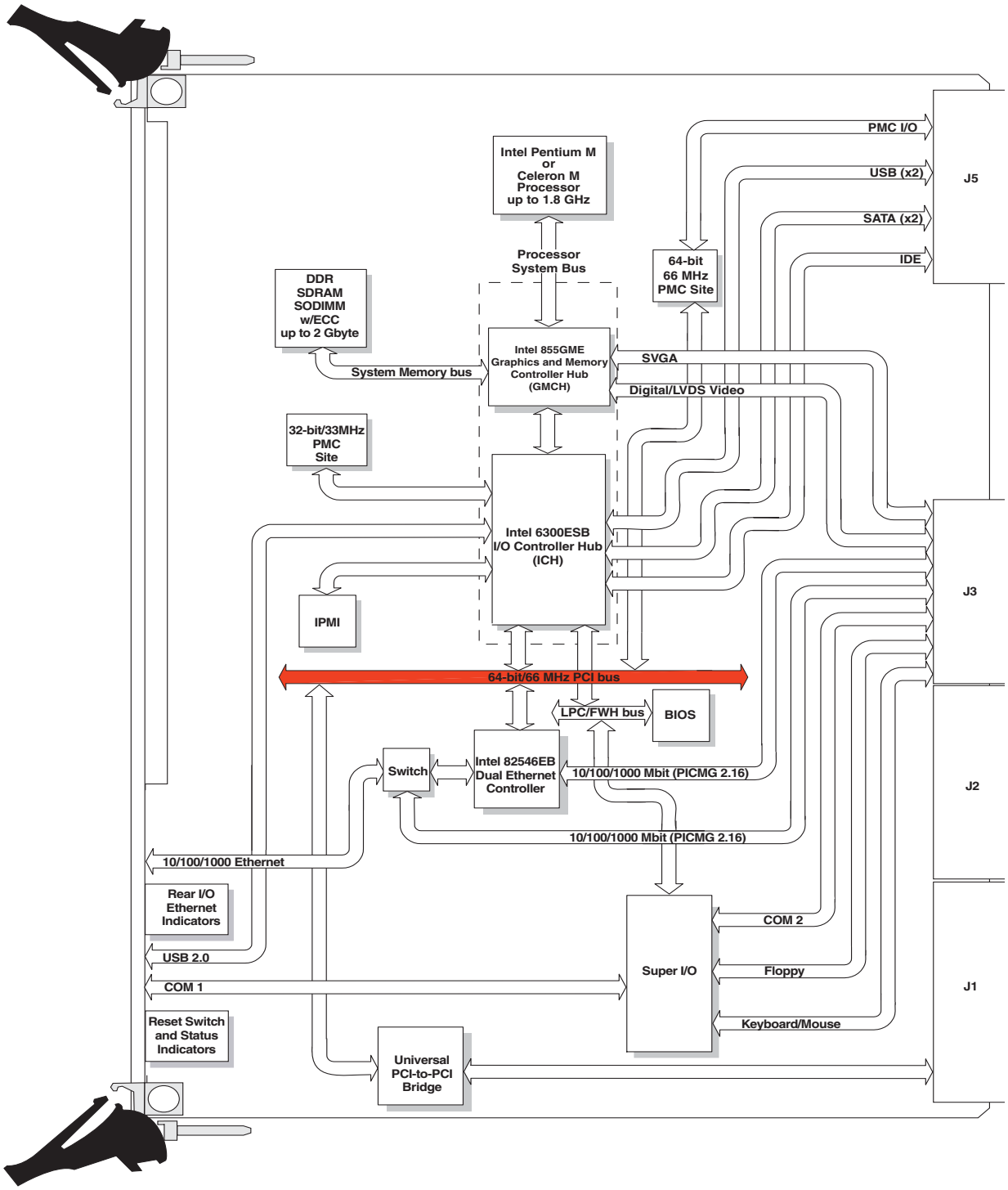


Figure 1 VMICPCI-7808 Block Diagram

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Organization of the Manual

This manual is composed of the following chapters and appendices:

Chapter 1 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup and operation of the VMICPCI-7808.

Chapter 2 - Standard Features describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 3 - Embedded PC/RTOS Features describes the unit features that are beyond standard functions.

Maintenance - provides information relative to the care and maintenance of the unit.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - BIOS Setup Utility describes the menus and options associated with the AMI (system) BIOS.

Appendix C - Argon BIOS describes the menus and options associated with the LAN Boot BIOS.

Appendix D - System Driver Software describes the steps required to load system drivers.

Appendix E - IPMI Firmware and OEM Extensions describes the function and commands of the IPMI firmware.

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References

Intel Pentium M Processor Datasheet
June 2003, Order Number 252612-002

Intel Celeron M Processor Datasheet
January 2004, Order Number 300302-001

Intel 855GME Chipset Graphics and Memory Controller Hub (GMCH)
March 2003, Order Number 252615-001

Intel 6300ESB I/O Controller Hub
February 2004, Order Number 300641-001

PCI Local Bus Specification, Rev. 2.2
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

LPC47M107 100-Pin Enhanced Super I/O with LPC Interface for Consumer Applications
Standard Microsystems Corp.
80 Askay Dr.
Hauppauge, NY 11788-8847
www.smsc.com

CMC Specification, P1386/Draft 2.0 from:
IEEE Standards Department
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445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331

PMC Specification, P1386.1/Draft 2.0 from:
IEEE Standards Department
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445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

PLX PCI-6254 (HB6) Dual Mode Universal PCI-to-PCI Bridge Datasheet
PLX Technology Inc.
870 Maude Ave.
Sunnyvale, CA 94085
www.plxtech.com

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For a detailed description and specification of the CompactPCI bus, please refer to:

CompactPCI Specification PICMG 2.0 R3.0
PCI Industrial Computer Manufacturers' Group
301 Edgewater Place
Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 (FAX)
www.picmg.org

Packet Switching Backplane Specification PICMG 2.16 R1.0
PCI Industrial Computer Manufacturers' Group
301 Edgewater Place
Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 (FAX)
www.picmg.org

The following is useful information related to the operation of the I^2C controllers:

The I^2C Specification version 2.0
Philips Semiconductor
811 East Arques Ave.
Sunnyvale, CA 94088-3409
(800) 234-7381
www.semiconductors.philips.com

Zircon PM Peripheral Management Controller Data Sheet
Order Number 36000-580-03 A
QLogic Management Products Group
804 Las Cimas Pkwy, Suite 100
Austin, TX 78746
USA 512-330-9920
www.qlogic.com

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

GE Fanuc Embedded Systems assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE Fanuc Embedded Systems for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice, or condition which is essential to highlight.

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CHAPTER

1

Installation and Setup

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Hardware Setup 25
Installation 29
Front Panel and Rear Transition Module Connections 32

Introduction

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the VMICPCI-7808.

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Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Fanuc Embedded Systems Customer Care along with a request for advice concerning the disposition of the damaged item(s).

CAUTION: Some of the components assembled on GE Fanuc Embedded Systems' products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that nonconductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

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Hardware Setup

The VMICPCI-7808 is factory populated with user-specified options as part of the VMICPCI-7808 ordering information. The RAM size is not user-upgradable. To change RAM size, contact customer service to receive a Return Material Authorization (RMA) at rma@gefanuc.com.

GE Fanuc Embedded Systems Customer Care is available at: 1-800-GEFANUC (1-800-433-2682) or 1-780-401-7700.

Or E-mail us at support.embeddedsystems@gefanuc.com

The VMICPCI-7808 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the single board CPU are illustrated in Figure 1-1 on page 26. The definitions of the CPU board jumpers and connectors are included in Table 1-1 through Table 1-5. Please note that the VMICPCI-7808 offers two PMC sites designated PMC #1 and PMC #2 as shown in Figure 1-1 on page 26.

CAUTION: All jumpers marked *User Configurable* in the following tables may be changed or modified by the user. All jumpers marked *Factory Configured* should not be modified by the user.

Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper not marked *User Configurable* will void the Warranty and may damage the unit.

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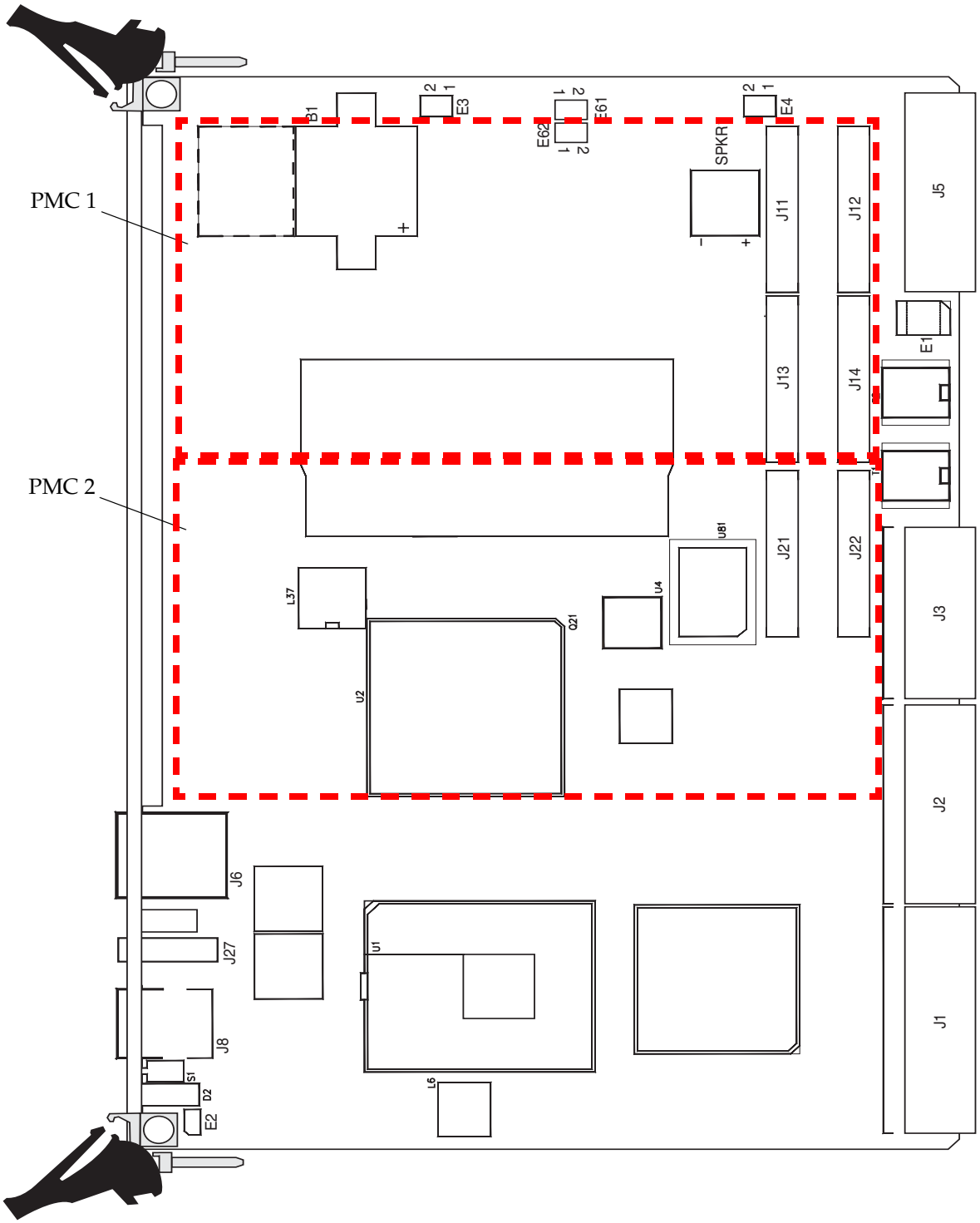


Figure 1-1 VMICPCI-7808 PMC Sites and Jumper Locations

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Table 1-1 CPU Board Connectors and Jumpers

Connector	Function
J1, J2, J3 and J5	CompactPCI Backplane Connectors
J3	COM2, Floppy
J5	USB, IDE, SATA, PMC I/O
J6	Ethernet 1
J8	COM 1
J11, J12, J13, J14	PMC Slot 1
J21, J22	PMC Slot 2
J25	ITP
E2	Hotswap Switch
E3	Battery
E4	CMOS Clear
E61	Blade Mode Jumper
E62	Reset Ignore Jumper

Table 1-2 Battery Enable (**User Configurable**) - Jumper (E3)

Select	Jumper Position
Battery Enabled	**1-3**
Battery Reserved	2-4

NOTE: The BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper allows the user to clear the CMOS and password in the case of a system BIOS malfunction or forgotten password.

Table 1-3 Password Clear (**User Configurable**) - Jumper (E4)

	Jumper Position
Normal	**2-4**
Clear CMOS/Password	1-2

To clear the CMOS password:

1. Turn off power to the unit.
2. Move the jumper on E4 from pins 2-4 to pins 1-2.
3. Wait approximately 5 seconds.
4. Move jumper on E4 back to pins 2-4.
5. Power up the unit.

When power is reapplied to the unit, the CMOS password will have been cleared, and the CMOS will be set to its defaults.

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Table 1-4 CompactPCI Bridge Mode (**User Configurable**) - Jumper (E61)

	Jumper Position
CompactPCI Mode Enable	**1-3 (Default)**
CompactPCI Mode Enable	**2-4 (Default)**

CompactPCI Bridge Mode Default: Normal operation mode.

Blade Mode: In this mode the VMICPCI-7808 will turn off the bridge to the backplane. This allows the SBC to be inserted into any slot on the backplane, with or without a system controller. If the SBC is inserted in a chassis with a system controller the CPCI_RESET# will be ignored. PIGMG 2.16 will still be available on the backplane.

Table 1-5 CompactPCI Reset (**User Configurable**) - Jumper (E62)

	Jumper Position
Reset Active	**1-2 (Default)**
Reset Ignore	3-4

CompactPCI Reset (Default): Resets from the system controller will always be accepted.

Reset Ignore: With the jumper installed on pins 3 and 4, a reset from the system controller will only be accepted until the boot done LED is turned off. When the boot done LED is turned on, resets will be ignored.

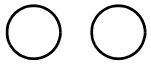
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Installation

The VMICPCI-7808 conforms to the CompactPCI physical specification for a 6U board. The VMICPCI-7808 can be used for system control or as a peripheral board. It can be plugged directly into any standard chassis accepting either type of board. The following pictures illustrate the symbols used to identify the slots in a standard CompactPCI chassis.



This symbol identifies the System Controller slot



This symbol identifies Dual LAN Node slots



This symbol identifies peripheral slots

The following steps describe the recommended method for installation and powerup of the VMICPCI-7808:

1. If a PMC module is to be used, connect it to the VMICPCI-7808 prior to board installation (as shown in Figure 1-2 on page 31). Refer to the Product Manual for the PMC module for configuration and setup.
2. The VMICPCI-7808 must be installed in a designated slot of the CompactPCI backplane (see symbols above for selection of the correct slot).

NOTE: Air flow requirement, as measured at the output side of heatsink, is to be greater than 400LFM.

3. Insert the VMICPCI-7808 into a CompactPCI chassis system controller or peripheral slot. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector. Use the ejector handles to firmly seat the board.
4. All needed peripherals can be accessed from the front panel or the rear I/O VMIACC-0591 Rear Transition Module (RTM). Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A.
5. Connect the keyboard and mouse if the system has not been previously configured.
6. If an external drive module is installed, the BIOS Setup program must be used to configure the drive types. See Appendix B to properly configure the system.
7. If a drive module is present, install the operating system according to the manufacturer's instructions.

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BIOS Setup

The VMICPCI-7808 has an onboard BIOS Setup program that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's 'CMOS Configuration'. The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

Details of the VMICPCI-7808 BIOS setup program are included in Appendix B.

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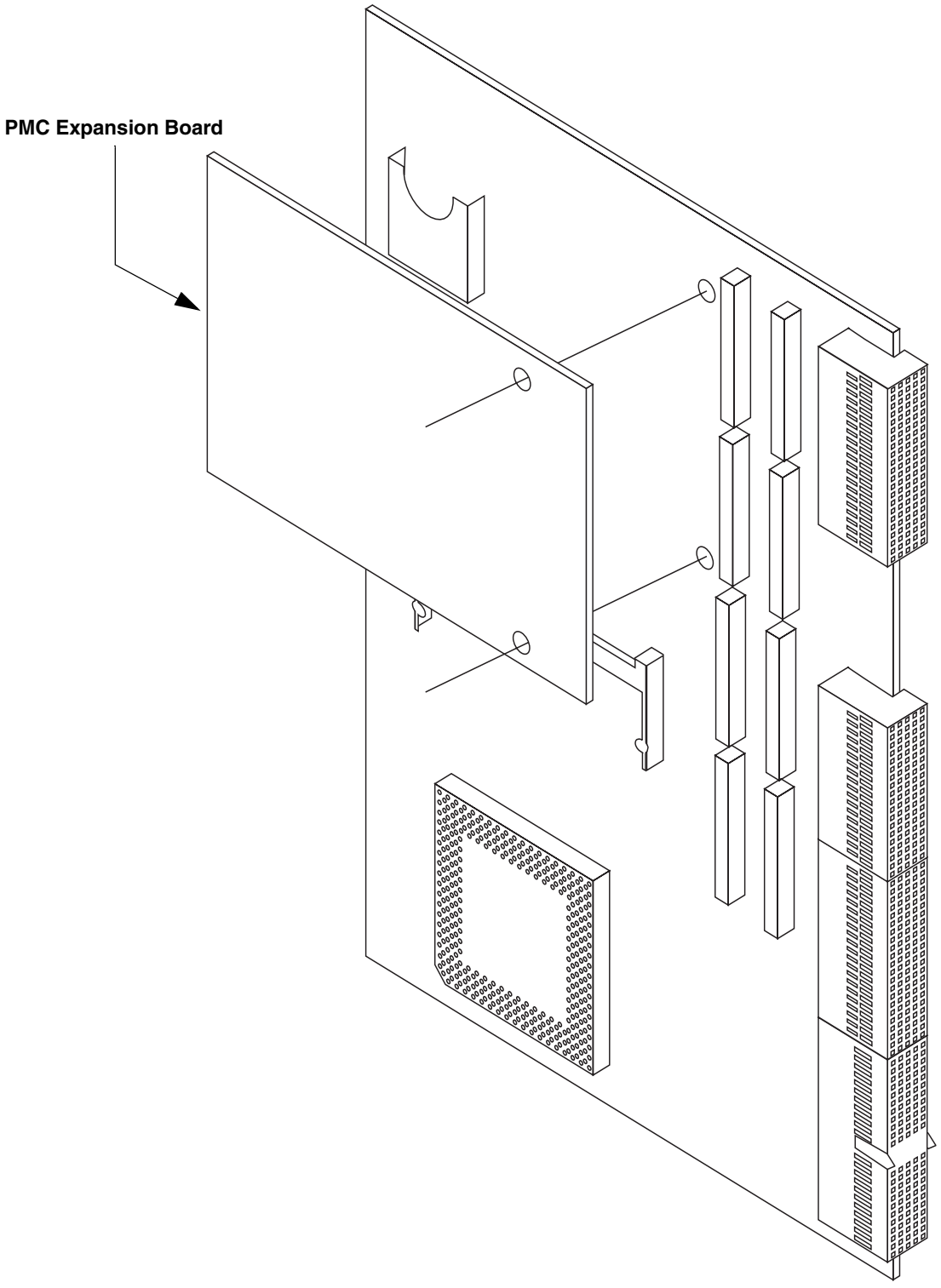


Figure 1-2 Installing a PMC Card on the VMICPCI-7808

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Front Panel and Rear Transition Module Connections

The VMICPCI-7808 provides front panel access for both PMC expansion sites, one 10/100/1000Mbit Ethernet port, one USB, one serial port, the manual reset switch and the status LEDs. A drawing of the VMICPCI-7808 front panel is shown in Figure 1-3. The front panel connectors and indicators are labeled as follows:

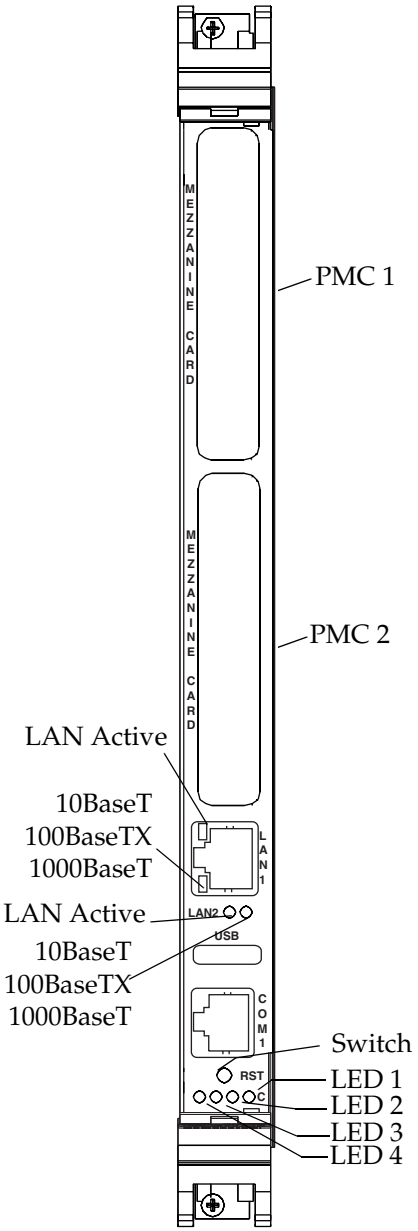
- LAN1 10/100/1000Mbit Ethernet connector 1
- USB USB Port
- COM1 Serial Port
- RST Manual reset switch
- S Status LEDs

The VMICPCI-7808 provides rear I/O support for the following: SVGA, Serial ATA port, Digital/LVDS, COM2, Keyboard/Mouse, PMC I/O for one expansion site, CompactFlash, IDE drive, floppy drive and two USB ports. These signals are accessed using the VMIACC-0591, which terminates into industry standard connectors.

The front panel connectors, including connector pinouts and orientation, for the VMICPCI-7808 are defined in Appendix A. RTM connections are defined in the appropiate RTM Installation Guide. See the VMICPCI-7808 product specification for compatible RTMs offered by GE Fanuc Embedded Systems.

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LED Definition



Switch	*Reset* - Allows the system to be reset from the front panel.
LED 1	*System* - Indicates BIOS Boot is in progress. When LED is off, CPU has finished POST and is ready, (Red LED).
LED 2	*IDE Indicator* - Indicates when IDE or serial ATA activity is occurring, (Yellow LED).
LED 3	*Power* - Indicates when power is applied to the board, (Green LED).
LED 4	*Hot Swap*- Lights during Hot Swap condition, (Blue LED).
LAN 1/2Active/Link	Indicates the Ethernet is active, (Blinking Yellow LED).
LAN Speed 1/2	Indicates Link Speed. LED off, indicates 10BaseT, Yellow LED, indicates 100BaseTX, Green LED, indicates 1000BaseT.

Figure 1-3 Front Panel LED Positions

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CHAPTER 2

Standard Features

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Introduction

The VMICPCI-7808 is a Pentium M or Celeron M processor-based single board computer compatible with modern industry standard desktop systems. The VMICPCI-7808 therefore retains industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB ports, IDE drives, floppy drives, video controller and Ethernet controller) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the VMICPCI-7808.

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CPU

The VMICPCI-7808 SBC is factory populated with a Pentium M or Celeron M processor. The CPU speed and RAM size are user specified as part of the VMICPCI-7808 ordering information.

To change RAM size contact Customer Care to receive a Return Material Authorization (RMA) at rma@gefanuc.com.

GE Fanuc Embedded Systems Customer Care is available at: 1-800-GEFANUC (1-800-433-2682), 1-780-401-7700, or
E-mail us at support.embeddedsystems@gefanuc.com .

Physical Memory

The VMICPCI-7808 provides DDR Synchronous DRAM (SDRAM) as onboard system memory. Memory can be accessed as bytes, words or longwords.

The VMICPCI-7808 accepts one 200-pin DDR SDRAM SODIMM for a maximum capacity of 2GB.

NOTE: Memory capacity may change due to part availability.

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I/O Port Map

Like a desktop system, the VMICPCI-7808 includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64KB I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 2-1.

Table 2-1 VMICPCI-7808 I/O Address Map

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$000 - $00F	16		DMA Controller 1 (Intel 8237A Compatible)
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller (Intel 8259A Compatible)
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer (Intel 8254 Compatible)
$044 - $05F	28		Reserved
$060 - $064	5		Keyboard, Speaker, System Configuration (Intel 8042 Compatible)
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093 - $09F	11		Reserved

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Table 2-1 VMICPCI-7808 I/O Address Map (Continued)

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$0A0 - $0A1	2		Slave Interrupt Controller (Intel 8259A Compatible)
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2 (Intel 8237A Compatible)
$0E0 - $16F	142		Reserved
$170 - $177	8	6300ESB	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	6300ESB	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip*	LPT2 Parallel I/O*
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	6300ESB	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super-I/O Chip	Secondary Floppy Disk Controller
$378 - $37F	8	Super-I/O Chip*	LPT1 Parallel I/O*
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	6300ESB	COM3 Serial I/O (Used for IPMI)
$3F0 - $3F7	8	Super-I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF	256		Reserved
$500 - CFF	2048		Reserved

** While these I/O ports are reserved for the listed functions, they are not implemented on the VMICPCI-7808. They are listed here to make the user aware of the standard PC usage of these ports.*

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Interrupts

System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-2 along with their functions. Table 2-3 on page 40 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 2-3 on page 40.

The interrupt hardware implementation on the VMICPCI-7808 is standard for computers built around the PC architecture, which evolved from the PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 2-1 on page 44.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 2-2 PC Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by VMICPCI-7808 PCIbus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2	
4	COM1	
5	IPMI	Reserved for IPMI Serial Port
6	Floppy Controller	
7	Not Assigned	Determined by BIOS
8	Real-Time Clock	
9	Old IRQ2	Determined by BIOS
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS

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Table 2-2 PC Hardware Interrupt Line Assignments (Continued)

IRQ	AT FUNCTION	COMMENTS
12	Mouse	
13	Math Coprocessor	
14	AT Hard Drive	Primary IDE
15	CompactFlash	Secondary IDE

Table 2-3 PC Interrupt Vector Table

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, CompactPCI Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Unassigned	Unassigned
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	Unassigned	Unassigned
10	16		BIOS Video I/O	Coprocessor Error
11	17		System Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode

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Table 2-3 PC Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26		Time of Day	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode

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Table 2-3 PC Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
67-6F	103-111		Reserved by DOS	Same as Real Mode
70	112	IRQ8	Real Time Clock	
71	113	IRQ9	Redirect to IRQ2	
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	AT Hard Drive	
77	119	IRQ15	CompactFlash	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 2-1 on page 44 depicts the VMICPCI-7808 interrupt logic pertaining to CompactPCI operations and the PMC site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the CompactPCI interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

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PCI Device Interrupt Map

The PCI bus-based external devices include the PMC sites, Ethernet controller and the PCI-to-PCI bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the ICH2. This mapping is illustrated in Figure 2-1 on page 44 and is defined in Table 2-4.

The device PCI interrupt lines (INTA through INTH) that are present on each device *cannot* be modified.

Table 2-4 PCI Device Interrupt Mapping by the BIOS

DEVICE	COMPONENT	VENDOR ID	DEVICE ID	CPU ADDRESS MAP ID SELECT	PCI IRQ	Arbitration Request Line	BUS
PCI-to-PCI Bridge	Hint HB6	0x3388	0x0020/21*	AD19	INTE, F, G, H	REQ2	2
PMC1	N/A	N/A	N/A	AD17	INTD, A, B, C	REQ1	2
PMC2	N/A	N/A	N/A	AD30	INTC, D, A, B	REQ0	1
Ethernet Controller	Intel 82546EB	0x8086	0x1010	AD21	INTA, B	REQ0	2
Host-Hub Interface Bridge	GMCH	0x8086	0x3580	N/A	N/A	N/A	0
System Peripheral	GMCH	0x8086	0x3584	N/A	N/A	N/A	0
System Peripheral	GMCH	0x8086	0x3585	N/A	N/A	N/A	0
Graphics Controller	GMCH	0x8086	0x3582	N/A	INTA	N/A	0
PCI-LPC Bridge	ICH	0x8086	0x25A1	N/A	N/A	N/A	0
SATA Controller	ICH	0x8086	0x25A3	N/A	INTC	N/A	0
SMBus Controller	ICH	0x8086	0x25A4	N/A	INTB	N/A	0
PCI-to-Hub Bridge	ICH	0x8086	0x244E	N/A	N/A	N/A	0
PCI Bridge	ICH	0x8086	0x25AE	N/A	N/A	N/A	0
USB UHCI 1	ICH	0x8086	0x25A9	N/A	INTA	N/A	0
USB UHCI 2	ICH	0x8086	0x25AA	N/A	INTD	N/A	0
WDT	ICH	0x8086	0x25AB	N/A	ISA INT9	N/A	0
USB EHCI	ICH	0x8086	0x25AD	N/A	INTH	N/A	0

**Device 20 = INTs E, F, G, H*
Device 21 = INT E

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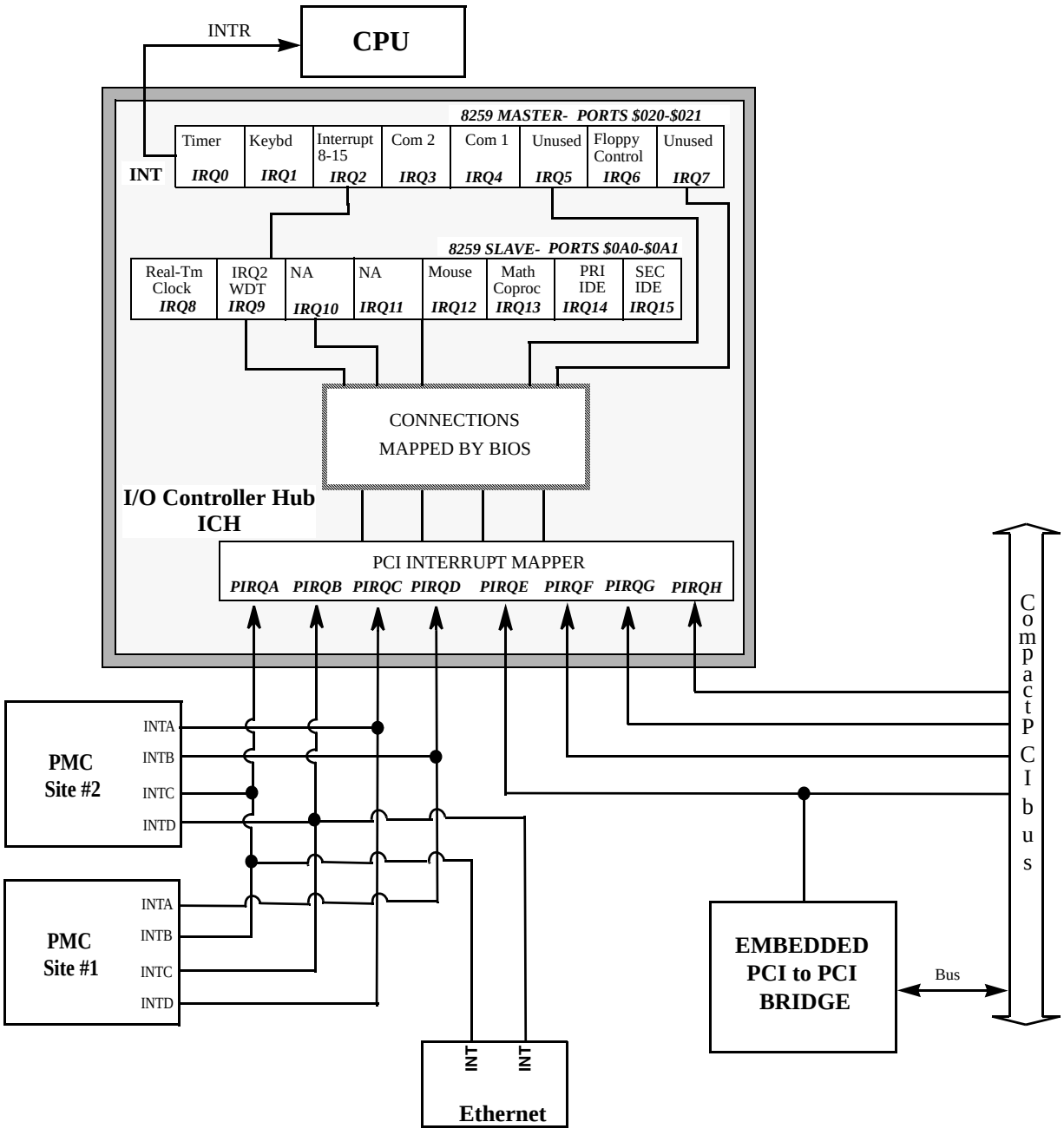


Figure 2-1 Connections for the PC Interrupt Logic Controller

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The PCI-to-PCI Bridge has the capability of generating an NMI via the PCI SERR# line. Table 2-5 describes the register bits that are used by the NMI. The SERR interrupt is routed through logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable/disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable/enable all NMI sources.

Table 2-5 NMI Register Bit Descriptions

Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set Bit 2 to 0 and then set it to 1. When writing to port $061, Bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read/Write) - 1 = Clear and Disable, 0 = Enable
Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

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Integrated Peripherals

The VMICPCI-7808 incorporates an SMSC Super I/O (SIO) chip. The SIO provides the VMICPCI-7808 with a standard floppy drive controller, two 16550 UART-compatible serial ports, keyboard and mouse ports, and general purpose I/O for system functions. The floppy, keyboard and mouse ports are available via the CompactPCI backplane connectors and can be accessed with the appropriate transition utility board. The serial port is accessed via the front panel. The second serial port is routed to the CompactPCI J3 connector for use with the rear transition utility board (VMIACC-0591).

The IDE interface is provided by the Intel I/O Controller Hub chip. The primary channel is routed to the CompactPCI backplane rear I/O for use with a rear transition utility board. The rear transition utility board terminates the signals into a standard 40-pin header and the optional CompactFlash. This channel can support two drives, a master and slave. The IDE interface on the VMICPCI-7808 supports Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100 drives and automatically determines the proper operating mode based on the type of drive used. In order to properly function in the Ultra ATA/100 mode, a special 80-conductor cable must be used instead of the standard 40 conductor cable. This cable is typically available from the Ultra ATA/100 drive manufacturer.

A dual Serial ATA Interface is also provided by the I/O Controller Hub. Both channels for the Serial ATA are routed to the CompactPCI backplane rear I/O. The Serial ATA ports can be used alone or in limited conjunction with the parallel IDE interface. A single Serial ATA drive can be connected to each port.

NOTE: Selection of drive type (parallel or serial), along with detailed IDE/ATA selections is available in the CMOS Advanced BIOS Setup Menu.

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Ethernet Controller

Network capability is provided by the Intel 82546EB dual Ethernet Controller for the VMICPCI-7808. This Ethernet controller is PCI bus based and is software configurable. The VMICPCI-7808 supports 10BaseT, 100BaseTX and 1000BaseT Dual Channel Ethernet. A front panel RJ45 connector is provided with two network status indicators, supporting PICMG 2.16 Rev 1.0. The front panel Ethernet interface can be switched from front to rear using the CMOS LAN selections.

10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters.

100BaseTX

The VMICPCI-7808 also supports the 100BaseTX Ethernet. A network based on a 100BaseTX standard uses unshielded twisted-pair cables and an RJ45 connector. 100BaseTX has a maximum length of 100 meters.

1000BaseT

The VMICPCI-7808 also supports 1000BaseT Ethernet. This standard uses shielded cables with four pairs of conductors, along with RJ45 connectors.

NOTE: Selection of Ethernet routing to the front panel RJ45 connector or switched to the CompactPCI J3 per PICMG 2.16 is in the BIOS CMOS chipset selection.

NOTE: Ethernet activity is monitored using LEDs on the front panel for both the rear I/O and the front panel mounted RJ45 connector by a blinking yellow LED. The yellow LED will be on continuously when the Ethernet port is linked but with no activity.

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Video Graphics Adapter

The SVGA port on the VMICPCI-7808 is controlled by the Intel Graphic and Memory Controller Hub (GMCH) chip. The GMCH is hardware and BIOS compatible with the industry EGA and SVGA standards supporting both VESA high-resolution and extended video modes. Table 2-6 shows the graphics video modes supported by the GMCH video controller.

Table 2-6 Supported Graphics Video Resolutions for Windows 2000

Screen Resolution	Maximum Colors	Maximum Refresh Rates (Hz)
640 x 480	256, High and True are supported at all resolutions.	85
768 x 1024		85
800 x 600		85
1024 x 768		85
1024 x 1280		85
1200 x 1600		85
1280 x 1024		85
1600 x 1200		85

Table 2-7 Supported Graphics Video Resolutions for Windows XP

Screen Resolution	Maximum Colors	Maximum Refresh Rates (Hz)
640 x 480	High and True are supported at all resolutions.	85
800 x 600		85
1024 x 768		85
1080 x 1280		85
1600 x 1200		85

Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 85Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

NOTES: The VMIACC-0591 is required for graphics operation. The default setup in the BIOS for LVDS Video Output is 800x600.

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CHAPTER 3

Embedded PC/RTOS Features

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Introduction

The VMICPCI-7808 features additional capabilities beyond those of a typical desktop computer system. The unit provides standard general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The VMICPCI-7808 also provides support for a bootable CompactFlash system or PICMG 2.16 Ethernet over the CompactPCI backplane rear I/O using the VMIACC-0591 RTM. PICMG 2.9 support is available, which allows for compatibility with the most demanding CompactPCI applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used.

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CompactPCI Bus Bridge

The VMICPCI-7808 incorporates a PLX PCI-6254 (Hint HB6) Universal Bridge device that performs universal PCI bridging functions for embedded and intelligent I/O applications. The PCI device acts as a gateway to an intelligent subsystem. As a peripheral controller it allows the local VMICPCI-7808 processor to configure and control the onboard local subsystem independent from the CompactPCI bus host processor. The VMICPCI-7808 local PCI subsystem is presented to the CompactPCI bus host as a single CompactPCI device. As a system controller, the bridge acts as a standard transparent PCI-to-PCI bridge. For detailed information concerning the embedded PCI bus bridge, consult the PLX PCI-6254 (Hint HB6) datasheet.

The VMICPCI-7808 PCI bridge device provides the following features:

PCI Interface

- Full compliance with the PCI Local Bus Specification, Revision 2.2
- Supports 3.3V or 5V VIO operation
- Concurrent local (secondary) and CompactPCI (primary) bus operation

Buffer Architecture

- Queuing of multiple transactions in either direction
- 256 byte of posted write (data and address) buffering in each direction
- 256 byte of read data buffering in each direction
- Four delayed transaction entries in each direction

Configuration Register and Control/Status Registers (CSRs)

- Two sets of standard PCI configuration registers corresponding to the local and CompactPCI interfaces: accessible from either the local or CompactPCI interface
- Three 32-bit base address configuration registers mapping the CSRs

Transaction Forwarding

- Three primary interface base address configuration registers for downstream forwarding with size and prefetchable programming for all three address ranges
- Direct offset address translation for downstream memory and I/O transactions
- Three secondary interface address ranges for upstream forwarding, with size and prefetchable programming for all three address ranges

NOTE: Configuration of the Universal Bridge memory and I/O register space is selected via the CMOS Setup Chipset section.

Blade Mode

This mode disables the bridge to the backplane. This results in the ability to be inserted into any slot on the backplane, with or without a system controller. All PCI signals from the chassis will be ignored. PIGMG 2.16 will still be available on the backplane.

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Watchdog Timer

General

The Watchdog Timer (WDT) supports the following features and functions:

- Selectable prescaler - approximately 1MHz (1µs to 1s) and approximately 1KHz (1ms to 10min)
- 33MHz clock (30ns clock ticks)
- Multiple modes (WDT and free-running)

Free-running mode:

- One stage timer
- Toggles WDT_OUT# after programmable time

WDT Mode:

- Two stage timer (first stage generates interrupt, second stage drives WDT_OUT# low)

  First stage generates IRQ, SMI or SCI interrupt after programmable time

  Second stage drives WDT_OUT# low or inverts the previous value

  Used only after first timeout occurs

  Status bit preserved in RTC well for possible error detection and correction

  Drives WDT_TOUT# when OUTPUT is enabled

- Timer may be disabled (default state) or locked (hard reset required to disable WDT)
- WDT automatic reload of preload value when WDT reload sequence is performed

Function

The Watchdog Timer provides a resolution that ranges from 1µs to 10 minutes. The timer uses a 35-bit Down-Counter. The counter is loaded with the value from the first Preload register. The timer is then enabled and starts counting down. The time at which the WDT first starts counting down is called the first stage. When the host fails to reload the WDT before the 35-bit down counter reaches zero, the WDT generates an internal interrupt. After the interrupt is generated, the WDT loads the value from the second Preload register into the WDT's 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host fails to reload the WDT before the second timeout, the WDT drives the WDT_TOUT# pin low and sets the timeout bit (WDT_TIMEOUT). This bit indicates that the system has become unstable. The WDT_TOUT# pin is held low until the system is reset or the WDT times out again (depends on TOUT_CNF). The process of reloading the WDT involves the following sequence of writes:

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1. Write 80 to offset BAR1 + 0C.
2. Write 86 to offset BAR1 + 0C.
3. Write 1 to WDT_RELOAD in Reload Register.

The same process is used for setting the values in the preload registers. The only difference exists in step 3. Instead of writing a 1 to the WDT_RELOAD, write the desired preload value into the corresponding Preload register. This value is not loaded into the 35-bit down counter until the next time the WDT re-enters the stage. For example, when Preload Value 2 is changed, it is not loaded into the 35-bit down counter until the next time the WDT enters the second stage.

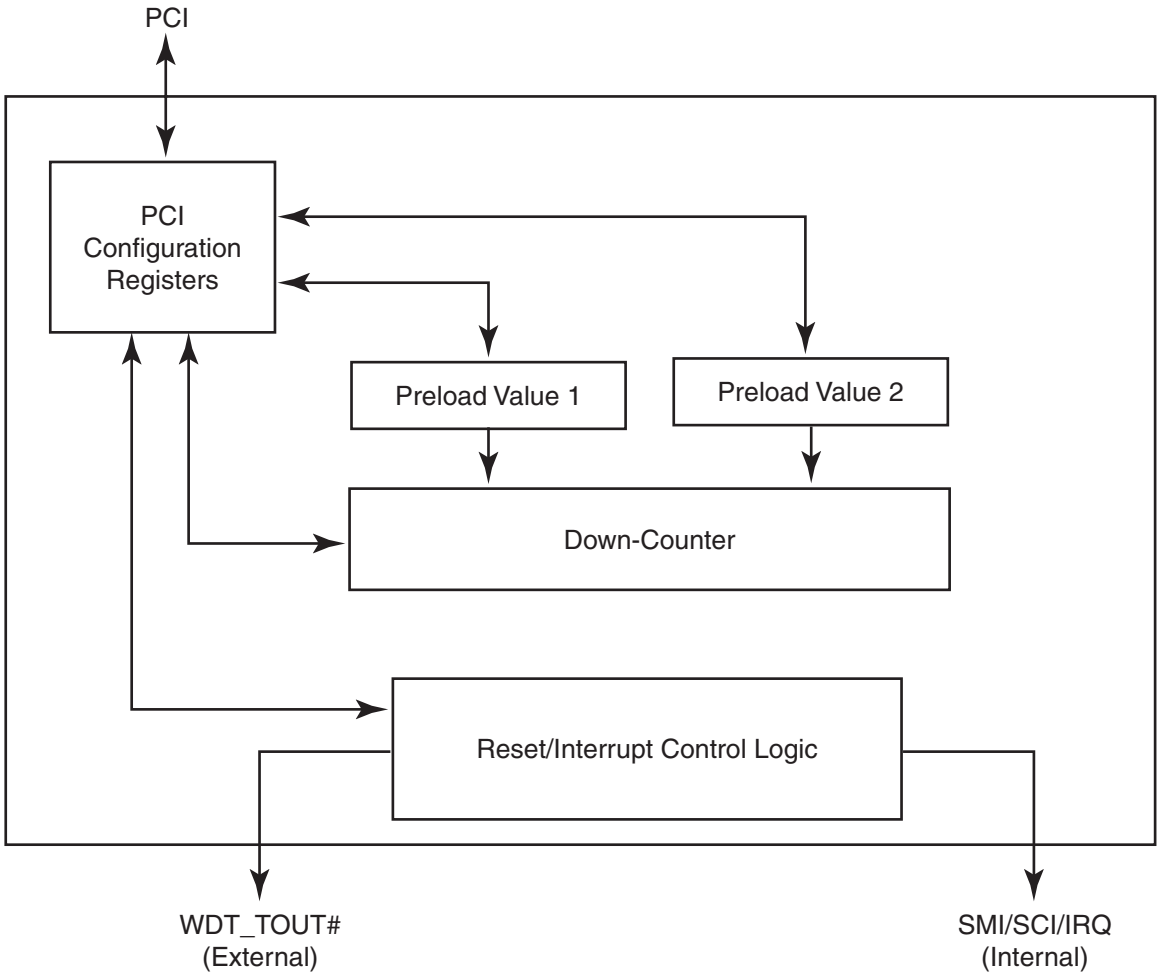


Figure 3-1 Watchdog Timer Block Diagram

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Registers

Table 3-1 Configuration Registers

Offset	Register	Default	Type
00-01h	Vendor ID	8086h	Read Only
02-03h	Device ID	25ABh	Read Only
04-05h	Command Register (COM)	0000h	Read/Write
06-07h	Device Status Register (DS)	0280h	Read/Write Clear
08h	Revision ID Register (RID)	00h	Read Only
09h	Programming Interface register (PI)	00h	Read Only
0Ah	Sub Class Code Register (SCC)	80h	Read Only
0Bh	Base Class Code Register (BCC)	08h	Read Only
0Eh	Header Type Register (HEDT)	00h	Read Only
10-13h	Base Address Register	00000000h	Read/Write
14-2Bh	Reserved	00h	
2C-2Dh	Subsystem Vendor ID	00h	Read/Write Once
2E-2F	Subsystem ID	00h	Read/Write Once
30-5F	Reserved	00h	
60-61h	WDT Configuration	00h	Read/Write
64-67h	Reserved	0000h	
68h	WDT Lock Register	00h	Read/Write
6C-F7	Reserved	00h	
F8-FBh	Manufacturer's ID	00000F66h	Read Only
FC-FFh	Reserved	00h	

Table 3-2 Memory Mapped Registers

Offset	Register	Default	Type
Base + 00h	Preload Value 1	FFFFFh	Read/Write
Base + 04h	Preload Value 2	FFFFFh	Read/Write
Base + 08h	General Interrupt Status	00h	Read/Write/Clear
Base + 0C	Reload Register	0000h	Write

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Table 3-3 Vendor Identification Register (VID)

Offset	00h	**Attribute**	Read Only
Default Value	8086h	**Size**	16-bit
Lockable	No	**Power Well**	Core

Table 3-4 Device Identification Register (DID)

Offset	02h	**Attribute**	Read Only
Default Value	25ABh	**Size**	16-bit
Lockable	No	**Power Well**	Core

Table 3-5 Command Register (COM)

Offset	04-05h	**Attribute**	Read/Write
Default Value	000Ah	**Size**	16-bit
Lockable	No	**Power Well**	Core

Table 3-6 Details of Command Register (COM)

Bit	Attribute	Description
15:10	N/A	Reserved
9	RO	FBE - Fast Back to Back Enable: Reserved as zero ‘0’. Read Only
8	RO	SERR# Enable: Reserved as zero ‘0’. Read Only
7	RO	Wait Cycle Control: Reserved as zero ‘0’. Read Only
6	RO	Parity error response: Reserved as ‘0’. Read Only
5	RO	VGA Palette Snoop: Reserved as ‘0’. Read Only
4	RO	PMWE - Postable Memory Write Enable: Reserved as zero ‘0’. Read Only
3	RO	SCE - Special Cycle Enable: Reserved as zero ‘0’. Read Only
2	RO	BME - Bus Master Enable: Reserved as zero ‘0’. Read Only
1	R/W	MSE - Memory Space Enable: This bit controls access to the WDT’s Memory Mapped registers. If this bit is set, accesses to the WDT’s Memory Mapped registers are enabled. The Base Address register for WDT should be programmed before this bit is set.

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Table 3-6 Details of Command Register (COM)

Bit	Attribute	Description
0	RO	IOSE - I/O Space Enable: Reserved as zero ‘0’. Read Only

Table 3-7 Device Status Register (DS)

Offset	06h - 07h	**Attribute**	Read/Write Clear
Default Value	0280h	**Size**	16-bit
Lockable	No	**Power Well**	Core

Table 3-8 Details of Device Status Register (DS)

Bit	Attribute	Description
15	RO	DPE - Detected Parity Error: Reserved as zero ‘0’. Read Only
14	RO	SSE - Signaled System Error: Reserved as zero ‘0’. Read Only
13	RO	RMA - Received Master Abort: Reserved as zero ‘0’. Read Only
12	RO	RTA - Received Target Abort: Reserved as zero ‘0’. Read Only
11	R/WC	STA - Signaled Target-Abort Status: This bit is set when the function is targeted with a transaction that Hance Rapids ICH terminates with a target abort. Software resets STA to zero ‘0’ by writing a 1 to this bit location.
10:9	RO	DEVT - DEVSEL# Timing Status: This 2-bit field defines the timing for DEVSEL# assertion. These read only bits indicate Hance Rapids ICH’s DEVSEL# timing when performing a positive decode. Note: Hance Rapids ICH generates DEVSEL# with medium time.
8	RO	Data Parity error Detected: Reserved as zero ‘0’. Read Only
7	RO	Fast Back-to-Back Capable: Reserved as zero ‘1’. Read Only
6	RO	UDF - User Definable Features: Reserved as zero ‘0’. Read Only
5	RO	66MHz Capable: Reserved as zero ‘0’. Read Only
4:0	RO	Reserved. Read Only

Table 3-9 Revision Identification Register (RID)

Offset	08h	**Attribute**	Read Only
Default Value	00h	**Size**	8-bit
Lockable	No	**Power Well**	Core

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Table 3-10 Programming Interface Register (PI)

Offset	09h	**Attribute**	Read Only
Default Value	00h	**Size**	8-bit
Lockable	No	**Power Well**	Core

Table 3-11 Sub Class Code Register (SCC)

Offset	0Ah	**Attribute**	Read Only
Default Value	80h	**Size**	8-bit
Lockable	No	**Power Well**	Core

Table 3-12 Base Code Class Register (BCC)

Offset	0Bh	**Attribute**	Read Only
Default Value	08h	**Size**	8-bit
Lockable	No	**Power Well**	Core

Table 3-13 Header Type Register (HEDT)

Offset	0Eh	**Attribute**	Read Only
Default Value	00h	**Size**	8-bit
Lockable	No	**Power Well**	Core

The Base Address Register points to several memory mapped registers for the WDT. It decodes the smallest possible region of 16 byte.

Table 3-14 Base Address Register 1 (BAR1)

Offset	10h	**Attribute**	Read-Write
Default Value	00000000h	**Size**	32-bit
Lockable	No	**Power Well**	Core

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Table 3-15 Details of Base Address Register 1 (BAR1)

Bit	Attribute	Description
31:4	R/W	Base Address: These bits are used to determine the size of the memory-mapped region being requested.
3	RO	Prefetchable: Hard-wired to zero '0', indicating that this range is not prefetchable. Read Only
2:1	RO	Type: Hard-wired to '00', indicating that this range can be mapped anywhere in 32-bit address space. Read Only
0	RO	RTE - Resource Type Indicator: This bit is hard-wired to zero '0', indicating a request for memory space. Read Only

Table 3-16 Subsystem Vendor ID (SVID)

Offset	2Ch-2Dh	**Attribute**	Read, Write Once
Default Value	00h	**Size**	16-bit
Lockable	No	**Power Well**	Core

Software (BIOS) will write the value to this register. After that, the value may be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write.

Table 3-17 Subsystem ID (SID)

Offset	2Eh-2Fh	**Attribute**	Read, Write Once
Default Value	00h	**Size**	16-bit
Lockable	No	**Power Well**	Core

Software (BIOS) will write the value to this register. After that, the value may be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write.

Table 3-18 WDT Configuration Register

Offset	60-61h	**Attribute**	Read-Write
Default Value	00h	**Size**	16-bit
Lockable	No	**Power Well**	Core

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Table 3-19 Details of WDT Configuration Register

Bit	Attribute	Description
15:6	RO	Reserved
5	R/W	WDT_OUTPUT: Out Enable: This bit indicates whether or not the WDT will toggle the external WDT_TOUT# pin when the WDT times out. 0 - Enabled (Default) 1 - Disabled
4:3	RO	Reserved
2	R/W	WDT_PRE_SEL: Prescaler Select: The WDT provides two options for prescaling the main Down Counter. The preload values are loaded into the main down counter right justified. The prescaler adjusts the starting point of the 35-bit down counter. 0 - The 20-bit Preload Value is loaded into bits 34:15 of the main down counter. The resulting timer clock is the PCI Clock (33MHz) divided by 2^{15}. The approximate clock generated is 1KHz, (1ms to 10 min). (Default) 1 - The 20-bit Preload Value is loaded into bits 24:5 of the main down counter. The resulting timer clock is the PCI Clock (33MHz) divided by 2^{5}. The approximate clock generated is 1MHz, (1µs to 1 sec).
1:0	R/W	WDT_INT_TYPE: The WDT timer supports programmable routing of interrupts. The set of bits allows the user to choose the type of interrupt desired when the WDT reached the end of the first stage without being reset. 00 = IRQ* (APIC 1, INT 10**) (Default) 01 = Reserved 10 = SMI 11 = Disabled

**IRQ is Active low.*

*****For operating systems that do not support APIC 1 - the Watchdog Timer Interrupt will be mapped to PIC Interrupt 9.***

Table 3-20 WDT Lock Register

Offset	68h	**Attribute**	Read-Write/Write Once
Default Value	00h	**Size**	8 bit
Lockable	No	**Power Well**	Core

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Table 3-21 Details of WDT Lock Register

Bit	Attribute	Description
7:3	RO	Reserved
2	R/W	WDT_TOUT_CNF: Timeout Configuration: This register is used to choose the functionality of the timer. 0 - Watchdog Timer Mode: When enabled (i.e. WDT_ENABLE goes from 0 to 1) the timer will reload Preload Value 1 and start decrementing (Default). Upon reaching the second stage timeout the WDT_TOU# is driven low once and will not change again until Power is cycled or a hard reset occurs. 1 - Free Running Mode: WDT_TOUT# will change from previous state when the next timeout occurs. The timer ignores the first stage. The timer only uses Preload Value 2. In this mode the timer is restarted whenever WDT_Enable goes from 0 to a 1. This means that the timer will reload Preload Value 2 and start decrementing every time it is enabled. **Note:** In free running mode it is not necessary to reload the timer as it is done automatically every time the decrementer reaches zero.
1	R/W	WDT_ENABLE: The following bit enables or disables the WDT. 0 - Disabled (Default) 1 - Enabled **Note:** This bit cannot be modified if WDT_LOCK has been set. **Note:** In free-running mode Preload Value 2 is reloaded into the down counter every time WDT_ENABLE goes from 0 to 1. In WDT mode Preload Value 1 is reloaded every time WDT_ENABLE goes from 0 to 1 or the WDT_RELOAD bit is written using the proper sequence of writes (See Register Unlocking Sequence). **Warning:** Software should guarantee that a timeout is not about to occur before disabling the timer. A reload sequence is suggested.
0	R/W0	WDT_LOCK: Setting this bit will lock the values of this register until a hard-reset occurs or power is cycled. 0 - Unlocked (Default) 1 - Locked **Note:** This is a Write-Once bit. It cannot be changed until either power is cycled or a hard-reset occurs.

Table 3-22 Manufacturer's ID

Offset	F8-FBh	**Attribute**	Read Only
Default Value	00000F66h	**Size**	32-bit
Lockable	No	**Power Well**	Core

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Table 3-23 Details of Manufacturer's ID

Bit	Attribute	Description
31:16	RO	Reserved
15:8	RO	Manufactory: 0Fh = Intel
7:0	R0	Process/Dot: 66h

Table 3-24 Preload Value 1 Register

Offset	Base + 00h	**Attribute**	Read-Write
Default Value	FFFFFh	**Size**	32-bit
Lockable	No	**Power Well**	Core

Table 3-25 Details of Preload Value 1 Register

Bit	Attribute	Description
31:20	RO	Reserved
19:0	R/W	Preload_Value_1 [19:0]: Use this register to hold the preload value for the WDT Timer. The value in the Preload register is automatically transferred into the 35-bit down counter every time the WDT enters the first stage. **Note:** The value loaded into the preload register needs to be one less than the intended period, as the timer makes use of zero based counting (zero is counted as part of the decrement). **Note:** Please refer to the Register Unlocking Sequence section for details on how to change the value of this register.

Table 3-26 Preload Value 2 Register

Offset	Base + 04h	**Attribute**	Read-Write
Default Value	FFFFFh	**Size**	32-bit
Lockable	No	**Power Well**	Core

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Table 3-27 Details of Preload Value 2 Register

Bit	Attribute	Description
31:20	RO	Reserved
19:0	R/W	Preload_Value_2 [19:0]: Use this register to hold the preload value for the WDT Timer. The value in the Preload register is automatically transferred into the 35-bit down counter every time the WDT enters the first stage. **Note:** The value loaded into the preload register needs to be one less than the intended period, as the timer makes use of zero based counting (zero is counted as part of the decrement). **Note:** Please refer to the Register Unlocking Sequence section for details on how to change the value of this register.

Table 3-28 General Interrupt Status Register

Offset	Base + 08h	**Attribute**	Read-Write Clear
Default Value	00h	**Size**	8-bit
Lockable	No	**Power Well**	Core

Table 3-29 Details of General Interrupt Status Register

Bit	Attribute	Description
7:1	RO	Reserved
0	R/WC	Watchdog Timer Interrupt Active: (1st Stage) this bit is set when the first stage of the 35-bit Down Counter reaches 0. An interrupt will be generated if WDT_INT_TYPE is configured to do so. See WDT Configuration register. This is a sticky bit and is only cleared by writing a one '1'. 0 - No Interrupt 1 - Interrupt Active **Note:** This bit is not set in free running mode. Use Unlock to access.

Table 3-30 Reload Register

Offset	Base + 0Ch	**Attribute**	Read-Write
Default Value	0000h	**Size**	16-bit
Lockable	No	**Power Well**	Core

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Table 3-31 Details of Reload Register

Bit	Attribute	Description
15:10	RO	Reserved
9	R/WC	WDT_TIMEOUT: This bit is in the RTC Well and its value is not lost when the host resets the system. It is set to one when the host fails to reset the WDT before the 35-bit Down Counter reaches zero for the second time in a row. This bit is cleared by performing the Register Unlocking Sequence followed by a 1 to this bit. 0 - Normal (Default) 1 - System has become unstable **Note:** In free running mode this bit is set every time the down counter reaches zero.
8	R/W	WDT_RELOAD: To prevent a timeout the host must perform the Register Unlocking Sequence followed by a one '1' to this bit. **Note:** Refer to Register Unlocking Sequence for details on how to write to this bit.
7:0	W	Reserved **Note:** The reload sequence is only necessary for the Reload register and Preload_Value registers and is not used in Free Running mode.

Register Unlocking Sequence

The register unlocking sequence is necessary whenever writing to the RELOAD register or either PRELOAD_VALUE registers. The host must write a sequence of two writes to offset BAR1 + 0Ch before attempting to write to either the WDT_RELOAD and WDT_TIMEOUT bits of the RELOAD register or the PRELOAD_VALUE registers. The first writes are 80 and 86 (in that order) to offset BAR1 + 0Ch. The next write will be to the proper register (e.g. RELOAD, PRELOAD_VALUE_1, PRELOAD_VALUE_2).

The following is an example of how to prevent a timeout:

1. Write 80 to offset BAR1 + 0Ch
2. Write 86 to offset BAR1 + 0Ch
3. Write a one '1' to RELOAD [8] (WDT_RELOAD) of the Reload register.

NOTE: Any subsequent writes require that this sequence be performed again.

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Reload Sequence

To keep the timer from causing an interrupt or driving WDT_TOUT#, the timer must be updated periodically. The frequency of updates required is dependant on the value of the Preload values. To update the timer the register Unlocking Sequence must be performed followed by writing a 1 to bit 8 at offset BAR + 0Ch within the watchdog timer memory mapped space. This sequence of events is referred to as the Reload Sequence.

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Remote Ethernet Booting

The VMICPCI-7808 is capable of booting from a server over a network utilizing the Argon LAN BIOS. The BIOS gives you the ability to remotely boot the VMICPCI-7808 using a variety of network protocols. The Ethernet must be connected through the LAN front panel (RJ45) or CompactPCI back panel connector to boot remotely. This feature allows users to create systems without the worry of disk drive reliability, or the extra cost of adding CompactFlash drives. Refer to Appendix C for details on Remote Ethernet BIOS selections.

Features

- Netware (802.1, 802.3 or EthII), TCP/IP (DHCP or BootP), RPL and PXE boot support
- Boot sector virus protection
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

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PICMG 2.16 Ethernet

The VMICPCI-7808 support Dual Gigabit Ethernet ports that are routed per the PICMG 2.16 Switching Backplane Specification. To enable Ethernet to support the PIMG 2.16 routing, the user must select the 'Rear Port' (Port 1) PICMG 2.16 routing in the Chipset 'LAN Routing' option of the CMOS BIOS set up program.

NOTE: The system backplane must support the PICMG 2.16 specification, and a PICMG 2.16 compatible switch is required for each Ethernet channel. Only one (1) of the ports can be switched from the front to the rear (Port 1).

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PICMG 2.9 Support

The VMICPCI-7808 provides a Zircon PM peripheral management controller that supports a subset of IPMI 1.5 commands via PICMG 2.9. Refer to Appendix E for details of the IPMI capabilities of the onboard peripheral management controller.

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Maintenance

This section provides information relative to the care and maintenance of GE Fanuc Embedded Systems' products. If the product malfunctions, verify the following:

1. System power
2. Software
3. System configuration
4. Electrical connections
5. Jumper or configuration options
6. Boards are fully inserted into their proper connector location
7. Connector pins are clean and free from contamination
8. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
9. Quality of cables and I/O connections

If products must be returned, contact GE Fanuc Embedded Systems for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**. RMAs are available at rma@gefanuc.com.

Contact GE Fanuc Embedded Systems Customer Care at 1-800-GEFANUC
(or 1-800-240-7782) or 1-780-401-7700, or
E-mail: support.embeddedsystem@gefanuc.com

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Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

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Compliance Information

This chapter provides the applicable information regarding regulatory compliance for the VMICPCI-7808.

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CE

GE Fanuc Embedded Systems VMICPCI-7808 has been evaluated to and has met the requirements for compliance to the following standards:

- EN55024
- EN55022, Class A
- EN61000-4-2
- EN61000-4-3
- EN61000-4-4
- EN61000-4-5
- EN61000-4-6

International Compliance

It has also met the following international levels.

European Union

- EN55024 (1998 w A1:01 & A2: 03)
- CISPR22, EN55022 (Class A)
- CISPR11, EN55011(Class A, Group 1)

United States

- FCC Part 15, Subpart B, Section 109, Class A
- CISPR 22 (1997), Class A
- ANSI C63.4 (2003) method

Australia/New Zealand

- AS/NZS CISPR 22 (2002) Class A using:
- EN55022 (1998) Class A

Japan

- VCCI (April 2005) Class A using:
- CISPR 22 (1997) Class A
- ANSI C63.4 (2003) method

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Canada

- ICES-003 Class A using:
- CISPR 22 (1997) Class A
- ANSI C63.4 (2003) Method

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class A

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

NOTICE: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canadian Regulations

The VMICPCI-7808 Class A digital apparatus complies with Canadian ICES-003.

NOTE: Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfies ICES-003.

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Appendix

A

Connector Pinouts

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Introduction

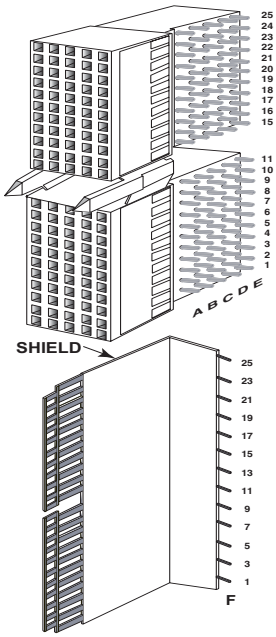
The VMICPCI-7808 CompactPCI Universal SBC has several connectors for its I/O ports. Wherever possible, the VMICPCI-7808 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a CompactPCI bus chassis.

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J1 Connector Pinout

The VMICPCI-7808 utilitizes a high-density 110-pin, low inductance, and controlled impedance connector. This connector meets the IEC-1076 international standard for CompactPCI connectors. An additional external metal shield is required. The large number of ground pins ensures adequate shielding and grounding for low ground bounce and reliable operation in noisy environments. The key prevents misalignment of the board when installing in the chassis. Figure A-1 below depicts the J1 connector and the connector pinout.



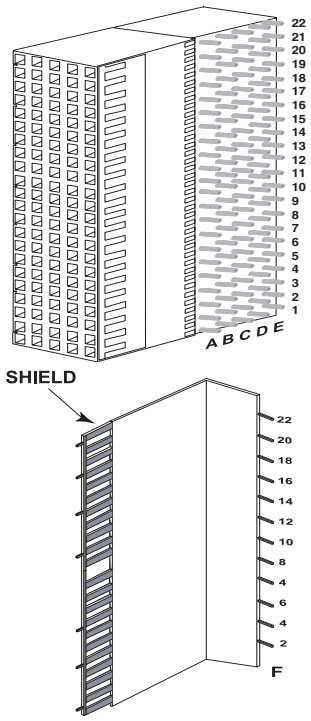
Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
25	VCC_5.0E	CPCI_REQ64#	CPCI_ENUM#	VCC_3.3E	VCC_5.0E	GND
24	CPCI_AD[1]	VCC_5.0E	CPCI_VIO_C24	CPCI_AD[0]	CPCI_ACK64#	GND
23	VCC_3.3E	CPCI_AD[4]	CPCI_AD[3]	CPCI_5V_D23	CPCI_AD[2]	GND
22	CPCI_AD[7]	GND	CPCI_3V_C22	CPCI_AD[6]	CPCI_AD[5]	GND
21	VCC_3.3E	CPCI_AD[9]	CPCI_AD[8]	CPCI_M66EN	CPCI_CBE[0]#	GND
20	CPCI_AD[12]	GND	VCC_VIO	CPCI_AD[11]	CPCI_AD[10]	GND
19	VCC_3.3E	CPCI_AD[15]	CPCI_AD[14]	GND	CPCI_AD[13]	GND
18	CPCI_SERR#	GND	VCC_3.3E	CPCI_PAR	CPCI_CBE[1]#	GND
17	VCC_3.3E	CPCI_IPMB_SCLH	CPCI_IPMB_SDAH	GND	CPCI_PERR#	GND
16	CPCI_DEVSEL#	CPCI_PCIXCAP	VCC_VIO	CPCI_STOP#	CPCI_LOCK#	GND
15	VCC_3.3E	CPCI_FRAME#	CPCI_IRDY#	CPCI_BDSEL#	CPCI_TRDY#	GND
12 through 14 are lost to the keying area						
11	CPCI_AD[18]	CPCI_AD[17]	CPCI_AD[16]	GND	CPCI_CBE[2]#	GND
10	CPCI_AD[21]	GND	VCC_3.3E	CPCI_AD[20]	CPCI_AD[19]	GND
9	CPCI_CBE[3#]	CPCI_IDSEL	CPCI_AD[23]	GND	CPCI_AD[22]	GND
8	CPCI_AD[26]	GND	VCC_VIO	CPCI_AD[25]	CPCI_AD[24]	GND
7	CPCI_AD[30]	CPCI_AD[29]	CPCI_AD[28]	GND	CPCI_AD[27]	GND
6	CPCI_REQ#	CPCI_PCI_PRESENT#	VCC_3.3E	CPCI_CLK	CPCI_AD[31]	GND
5	N/C	N/C	CPCI_RST#	GND	CPCI_GNT#	GND
4	CPCI_IPMB_PWR	CPCI_HEALTHY#	CPCI_VIO_C4	N/C	N/C	GND
3	CPCI_INTAR#	CPCI_INTBR#	CPCI_INTCR#	CPCI_5V_D3	CPCI_INTDR#	GND
2	CPCI_TCK	VCC_5.0E	CPCI_TMS	N/C	CPCI_TDI	GND
1	VCC_5.0E	VCC_-12.0E	CPCI_TRST#	VCC_12.0E	VCC_5.0E	GND

Figure A-1 J1 Connector and Pinout

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J2 Connector Pinout

The VMICPCI-7808 J2 connector is a 2mm “Hard Metric” CompactPCI connector, with 5 rows of 22 pins each. J2 is required for system slot CPUs. An additional external metal shield, labeled row F, is also used. This connector’s controlled impedance minimizes unwanted signal reflections. Figure A-2 illustrates the J2 connector and the connector pinout.



Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
22	VCC_3.3E	VCC_3.3E	VCC_3.3E	VCC_3.3E	VCC_3.3E	GND
21	CPCI_CLK6	GND	N/C	N/C	N/C	GND
20	CPCI_CLK5	GND	N/C	GND	N/C	GND
19	GND	GND	CPCI_SMB1_SDA	CPCI_SMB1_SCL	CPCI_SMB1_ALERT#	GND
18	N/C	N/C	N/C	GND	N/C	GND
17	N/C	GND	BP_RST#	CPCI_REQ6#	CPCI_GNT6#	GND
16	N/C	N/C	CPCI_DEG#	GND	N/C	GND
15	N/C	GND	CPCI_FAL#	CPCI_REQ5#	CPCI_GNT5#	GND
14	CPCI_AD[35]	CPCI_AD[34]	CPCI_AD[33]	GND	CPCI_AD[32]	GND
13	CPCI_AD[38]	GND	VCC_VIO*	CPCI_AD[37]	CPCI_AD[36]	GND
12	CPCI_AD[42]	CPCI_AD[41]	CPCI_AD[40]	GND	CPCI_AD[39]	GND
11	CPCI_AD[45]	GND	VCC_VIO*	CPCI_AD[44]	CPCI_AD[43]	GND
10	CPCI_AD[49]	CPCI_AD[48]	CPCI_AD[47]	GND	CPCI_AD[46]	GND
9	CPCI_AD[52]	GND	VCC_VIO*	CPCI_AD[51]	CPCI_AD[50]	GND
8	CPCI_AD[56]	CPCI_AD[55]	CPCI_AD[54]	GND	CPCI_AD[53]	GND
7	CPCI_AD[59]	GND	VCC_VIO*	CPCI_AD[58]	CPCI_AD[57]	GND
6	CPCI_AD[63]	CPCI_AD[62]	CPCI_AD[61]	GND	CPCI_AD[60]	GND
5	CPCI_CBE[5]#	CPCI_64EN#	VCC_VIO*	CPCI_CBE[4]#	CPCI_PAR64	GND
4	VCC_VIO*	N/C	CPCI_CBE[7]#	GND	CPCI_CBE[6]#	GND
3	CPCI_CLK4	GND	CPCI_GNT3#	CPCI_REQ4#	CPCI_GNT4#	GND
2	CPCI_CLK2	CPCI_CLK3	SYSEN#	CPCI_GNT2#	CPCI_REQ3#	GND
1	CPCI_CLK1	GND	CPCI_REQ1#	CPCI_GNT1#	CPCI_REQ2#	GND

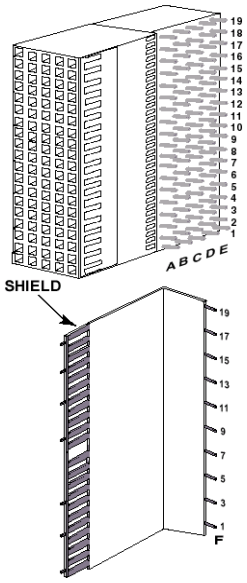
** VCC_VIO - The VMICPCI-7808 is a universal VIO design.*
The VMICPCI-7808 supports a 64-bit CompactPCI bus.

Figure A-2 J2 Connector and Pinout

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J3 Connector Pinout

The J3 connector is a 5 row, 19 pins each, 2mm “Hard Metric” CompactPCI connector. An additional external metal shield is also used, labeled row F. Figure A-3 illustrates the J3 connector and the connector pinout. This connector is used to route the I/O signals of the PMC Site #2 and the serial and floppy drive signals to the backplane I/O.



Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	GND	GND	GND	GND	GND
18	LPA_BI_DA+	LPA_BI_DA-	GND	LPA_BI_DC+	LPA_BI_DC-	GND
17	LPA_BI_DB+	LPA_BI_DB-	GND	LPA_BI_DD+	LPA_BI_DD-	GND
16	LPB_BI_DA+	LPB_BI_DA-	GND	LPB_BI_DC+	LPB_BI_DC-	GND
15	LPB_BI_DB+	LPB_BI_DB-	GND	LPB_BI_DD+	LPB_BI_DD-	GND
14	GND	GND	GND	GND	GND	GND
13	SP2_RTS#B	SP1_RI#B	SP2_DSR#B	SP2_DCD#B	SP2_CTS#B	GND
12	SP1_RTS#B	SP2_DTR#B	VCC_5.0	SP1_CTS#B	LVDS_BKLTEN	GND
11	SP2_TXB	SP2_RXB	SP1_DTR#B	SP1_DCD#B	LVDS_CLKAM	GND
10	SP1_TXB	SP1_RXB	SP1_DSR#B	SP2_RI#B	LVDS_CLKAP	GND
9	FDC_INDEX#	FDC_REDWC#	USB_OC1#	USB_OC0#	LVDS_VDDEN	GND
8	FDC_DIR#	KBCLK_C	AVIDEO_HSYNC	AVIDEO_DDCCLK	LVDS_YAM[1]	GND
7	FDC_HDSEL#	KEYDAT_C	AVIDEO_VSYNC	AVIDEO_DDCDATA	LVDS_YAP[1]	GND
6	FDC_RDATA#	FDC_TRK0#	SW_ON#	LVDS_BKLTCTL	GND	GND
5	FDC_DRATE0	FDC_WDATA#	SLP_S3#	LVDS_DDCPDATA	LVDS_YAM[2]	GND
4	MSCLK_C	FDC_STEP#	VCC_5.0	LVDS_DDCPCLK	LVDS_YAP[2]	GND
3	FDC_DSKCHG#	MSDAT_C	AVIDEO_GREEN	GND	GND	GND
2	FDC_WP#	FDC_DRVSA#	AVIDEO_BLUE	LVDS_YAM[0]	LVDS_YAM[3]	GND
1	FDC_WGATE#	FDC_MTR0#	AVIDEO_RED	LVDS_YAP[0]	LVDS_YAP[3]	GND

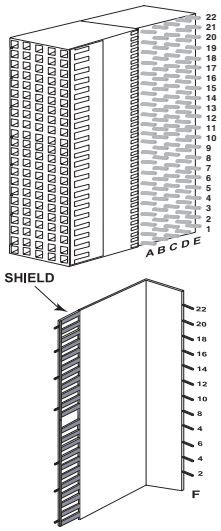
Figure A-3 J3 Connector and Pinout

NOTE: Backplane designs should route P3 signals straight through to rear J3. The VMIACC-0591 board can then be utilized.

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J5 Connector Pinout

The VMICPCI-7808 J5 connector is a 2mm “Hard Metric” CompactPCI connector, with 5 rows of 22 pins each. An additional external metal shield is also used, labeled row F. This connector is used to route the I/O signals of PMC Site #1, and the IDE, serial and USB signals to the backplane I/O. This connector’s controlled impedance minimizes unwanted signal reflections. Figure A-4 illustrates the J5 connector and the connector pinout.



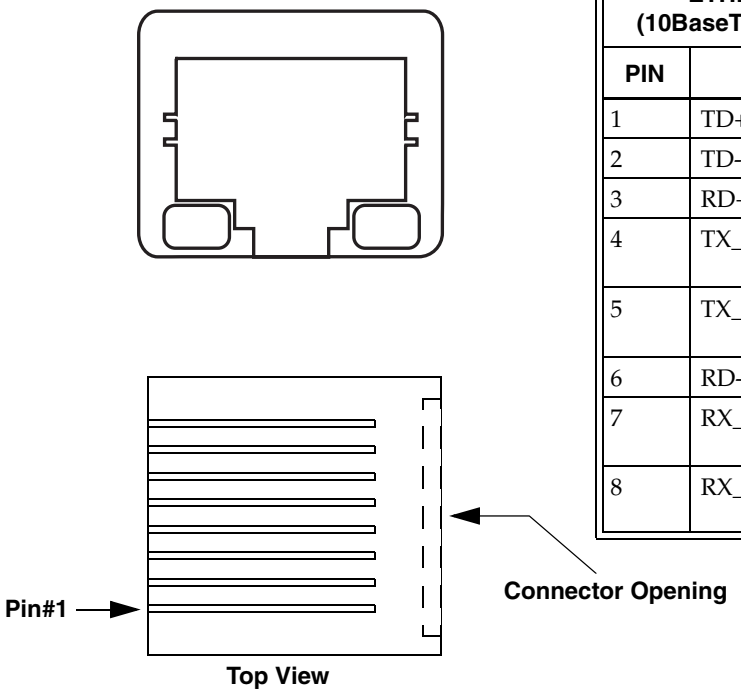
Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
22	PMC1_IO[5]	PMC1_IO[4]	PMC1_IO[3]	PMC1_IO[2]	PMC1_IO[1]	GND
21	PMC1_IO[10]	PMC1_IO[9]	PMC1_IO[8]	PMC1_IO[7]	PMC1_IO[6]	GND
20	PMC1_IO[15]	PMC1_IO[14]	PMC1_IO[13]	PMC1_IO[12]	PMC1_IO[11]	GND
19	PMC1_IO[20]	PMC1_IO[19]	PMC1_IO[18]	PMC1_IO[17]	PMC1_IO[16]	GND
18	PMC1_IO[25]	PMC1_IO[24]	PMC1_IO[23]	PMC1_IO[22]	PMC1_IO[21]	GND
17	PMC1_IO[30]	PMC1_IO[29]	PMC1_IO[28]	PMC1_IO[27]	PMC1_IO[26]	GND
16	PMC1_IO[35]	PMC1_IO[34]	PMC1_IO[33]	PMC1_IO[32]	PMC1_IO[31]	GND
15	PMC1_IO[40]	PMC1_IO[39]	PMC1_IO[38]	PMC1_IO[37]	PMC1_IO[36]	GND
14	PMC_IO[45]	PMC1_IO[44]	PMC1_IO[43]	PMC1_IO[42]	PMC1_IO[41]	GND
13	PMC1_IO[50]	PMC1_IO[49]	PMC1_IO[48]	PMC1_IO[47]	PMC1_IO[46]	GND
12	PMC1_IO[55]	PMC1_IO[54]	PMC1_IO[53]	PMC1_IO[52]	PMC1_IO[51]	GND
11	PMC1_IO[60]	PMC1_IO[59]	PMC1_IO[58]	PMC1_IO[57]	PMC1_IO[56]	GND
10	VCC_VIO_J5	PMC1_IO[64]	PMC1_IO[63]	PMC1_IO[62]	PMC1_IO[61]	GND
9	IDE_PDA[0]	GND	GND	IDE_PDA[2]	ICH_SATA_TXN1	GND
8	IDE_PDA[1]	IDE_PDD[8]	IDE_PIORDY#	IDE_PDD[0]	ICH_SATA_TXP1	GND
7	IDE_PDIOR#	IDE_PDD[9]	IDE_PDCS1#	IDE_PDD[1]	ICH_SATA_RXP1	GND
6	IDE_PDIOW#	IDE_PDD[10]	HD_ACTA#	IDE_PDD[2]	ICH_SATA_RXN1	GND
5	UDMA_PRI_DETECT	IDE_PDD[11]	IDE_PDCS3#	IDE_PDD[3]	GND	GND
4	USB_P1N	IDE_PDD[12]	IDE_IRQ14	IDE_PDD[7]	ICH_SATA_TXN0	GND
3	USB_P1P	IDE_PDD[13]	IDE_PDACK#	IDE_PDD[6]	ICH_SATA_TXP0	GND
2	USB_P0P	IDE_PDD[14]	IDE_PDRQ	IDE_PDD[5]	ICH_SATA_RXP0	GND
1	USB_P0N	IDE_PDD[15]	BRSTDRV#	IDE_PDD[4]	ICH_SATA_RXN0	GND

Figure A-4 J5 Connector and Pinout

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Ethernet Connector Pinout

The pinout diagram for the Ethernet 10BaseT, 100BaseTX and 1000BaseT connector (J6) is shown in Figure A-5.



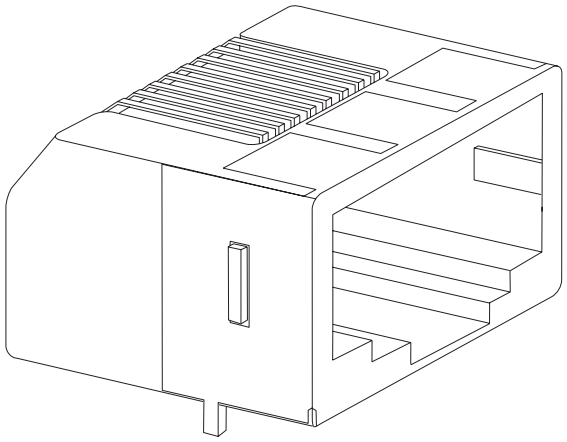
ETHERNET CONNECTOR (10BaseT, 100BaseTX, 1000BaseT)		
PIN	**Signal Name**	
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	TX_CT_OUT	Transmit Center Tap Out
5	TX_CT_OUT	Transmit Center Tap Out
6	RD-	Receive Data
7	RX_CT_OUT	Receive Center Tap Out
8	RX_CT_OUT	Receive Center Tap Out

Figure A-5 Ethernet Connector and Pinout

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Serial Connector Pinout (COM1) J8

The COM1 serial port connector is a RJ45 connector as shown in the drawing in Figure A-6.



COM 1 SERIAL PORT CONNECTOR J8	
PIN	**Assignment**
1	DCD
2	RTS
3	GND
4	TXD
5	RXD
6	GND
7	CTS
8	DTR

Figure A-6 Serial Connector and Pinout

NOTE: An RJ45 to DB9 adapter cable (360-010030-001) is shipped with the VMICPCI-7808.

Table A-1 RJ45 -DB9 Adapter Pinout

DB9	Assignment
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	NC
7	RTS
8	CTS
9	NC

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PMC Connector Pinout

PMC #1 (J11)/PMC #2 (J21) Connector and Pinout

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-2 through A-5 are the pinouts for the PMC connectors.

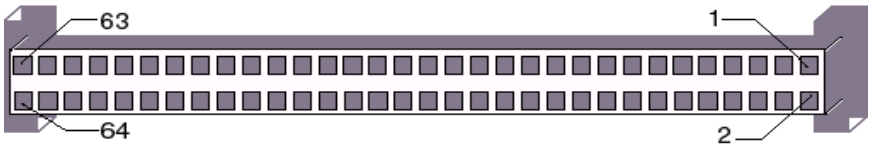


Table A-2 PMC #1 (J11)/PMC #2 (J21) Connector Pinout

PMC Connector (J11/J21)				PMC Connector (J11/J21)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12V	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5 V
7	BMODE1A	8	+5 V	39	PCIXCAP	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	NC
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	VCC_3.3	46	AD[15]
15	GND	16	GNT[1]#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	VCC_3.3	20	AD[31]	51	GND	52	C/BE#[0]
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE#[3]	57	VCC_3.3	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	VCC_3.3	32	AD[17]	63	GND	64	REQ64#

Signal names are generic labels. J11 signals are for the PCI1 bus and J21 signals are for the PCI0 bus.

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PMC #1 (J12)/PMC #2 (J22) Connector and Pinout

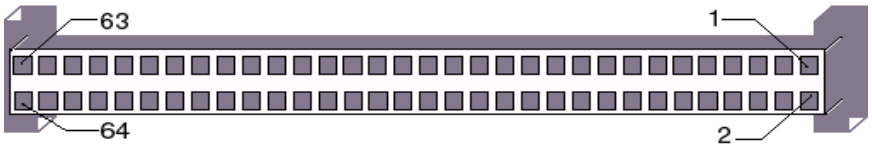


Table A-3 PMC #1 (J12)/PMC #2 (J22) Connector Pinout

PMC Connector (J12/J22)				PMC Connector (J12/J22)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	+5 V	33	GND	34	NC
3	GND	4	NC	35	TRDY#	36	+3.3 V
5	+5 V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3 V	42	SERR#
11	BMODE2#	12	+3.3 V	43	C/BE#[1]	44	GND
13	RESET#	14	GND	45	AD[14]	46	AD[13]
15	+3.3 V	16	GND	47	M66EN	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3 V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3 V	54	NC
23	AD[24]	24	+3.3 V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3 V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3 V
31	AD[16]	32	C/BE#[2]	63	GND	64	NC

Signal names are generic labels. J12 signals are for the PCI1 bus and J22 signals are for the PCI0 bus.

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PMC #1 (J13) Connector and Pinout

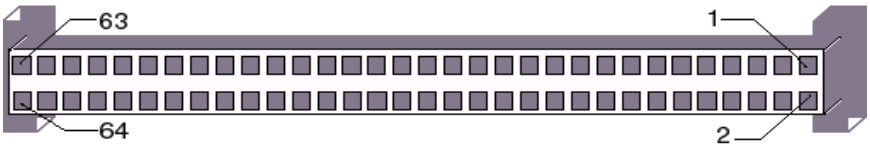


Table A-4 PMC #1 J13 Connector Pinout

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	PCI1_AD[48]
3	GND	4	PCI1_C/BE#[7]	35	PCI1_AD[47]	36	PCI1_AD[46]
5	PCI1_C/BE#[6]	6	PCI1_C/BE#[5]	37	PCI1_AD[45]	38	GND
7	PCI1_C/BE#[4]	8	GND	39	VCC_3.3	40	PCI1_AD[44]
9	VCC_3.3	10	PCI1_PAR64	41	PCI1_AD[43]	42	PCI1_AD[42]
11	PCI1_AD[63]	12	PCI1_AD[62]	43	PCI1_AD[41]	44	GND
13	PCI1_AD[61]	14	GND	45	GND	46	PCI1_AD[40]
15	GND	16	PCI1_AD[60]	47	PCI1_AD[39]	48	PCI1_AD[38]
17	PCI1_AD[59]	18	PCI1_AD[58]	49	PCI1_AD[37]	50	GND
19	PCI1_AD[57]	20	GND	51	GND	52	PCI1_AD[36]
21	VCC_3.3	22	PCI1_AD[56]	53	PCI1_AD[35]	54	PCI1_AD[34]
23	PCI1_AD[55]	24	PCI1_AD[54]	55	PCI1_AD[33]	56	GND
25	PCI1_AD[53]	26	GND	57	VCC_3.3	58	PCI1_AD[32]
27	GND	28	PCI1_AD[52]	59	N/C	60	N/C
29	PCI1_AD[51]	30	PCI1_AD[50]	61	N/C	62	GND
31	PCI1_AD[49]	32	GND	63	GND	64	N/C

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PMC #1 (J14) Connector and Pinout

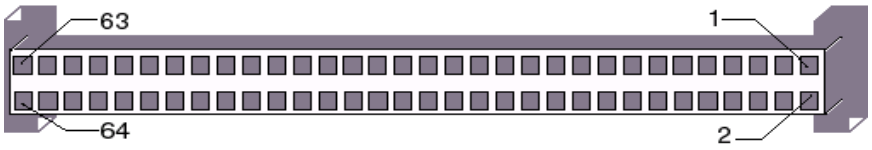


Table A-5 PMC #1 J14 Connector Pinout

PMC Connector (J14)						PMC Connector (J14)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	J14-1	J5 pin E22	2	J14-2	J5 pin D22	33	J14-33	J5 pin C16	34	J14-34	J5 pin B16
3	J14-3	J5 pin C22	4	J14-4	J5 pin B22	35	J14-35	J5 pin A16	36	J14-36	J5 pin E15
5	J14-5	J5 pin A22	6	J14-6	J5 pin E21	37	J14-37	J5 pin D15	38	J14-38	J5 pin C15
7	J14-7	J5 pin D21	8	J14-8	J5 pin C21	39	J14-39	J5 pin B15	40	J14-40	J5 pin A15
9	J14-9	J5 pin B21	10	J14-10	J5 pin A21	41	J14-41	J5 pin E14	42	J14-42	J5 pin D14
11	J14-11	J5 pin E20	12	J14-12	J5 pin D20	43	J14-43	J5 pin C14	44	J14-44	J5 pin B14
13	J14-13	J5 pin C20	14	J14-14	J5 pin B20	45	J14-45	J5 pin A14	46	J14-46	J5 pin E13
15	J14-15	J5 pin A20	16	J14-16	J5 pin E19	47	J14-47	J5 pin D13	48	J14-48	J5 pin C13
17	J14-17	J5 pin D19	18	J14-18	J5 pin C19	49	J14-49	J5 pin B13	50	J14-50	J5 pin A13
19	J14-19	J5 pin B19	20	J14-20	J5 pin A19	51	J14-51	J5 pin E12	52	J14-52	J5 pin D12
21	J14-21	J5 pin E18	22	J14-22	J5 pin D18	53	J14-53	J5 pin C12	54	J14-54	J5 pin B12
23	J14-23	J5 pin C18	24	J14-24	J5 pin B18	55	J14-55	J5 pin A12	56	J14-56	J5 pin E11
25	J14-25	J5 pin A18	26	J14-26	J5 pin E17	57	J14-57	J5 pin D11	58	J14-58	J5 pin C11
27	J14-27	J5 pin D17	28	J14-28	J5 pin C17	59	J14-59	J5 pin B11	60	J14-60	J5 pin A11
29	J14-29	J5 pin B17	30	J14-30	J5 pin A17	61	J14-61	J5 pin E10	62	J14-62	J5 pin D10
31	J14-31	J5 pin E16	32	J14-32	J5 pin D16	63	J14-63	J5 pin C10	64	J14-64	J5 pin B10

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USB Connector (J27)

The Universal Serial Bus (USB) port uses an industry standard, four position (conductors) shielded connector. Figure A-7 illustrates the connector, while Table A-6 shows the pinout of the USB connectors.

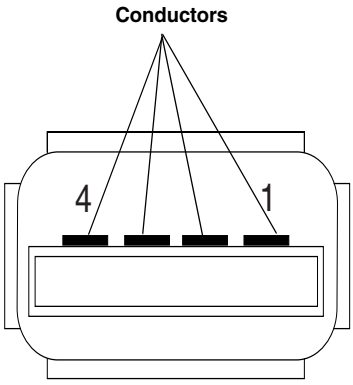


Figure A-7 USB J27 Connector

Table A-6 USB J27 Connector Pinout

Pin	Signal	Function
1	USBV	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

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Appendix

B

BIOS Setup Utility

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VMICPCI-7808 Main 87
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Introduction

This appendix gives a brief description of the setup options in the system BIOS. Due to the custom nature of GE Fanuc Embedded Systems' Single Board Computers, your BIOS options may vary from the options discussed in this appendix.

AMI refers to their BIOS setup screens as ezPORT. For a complete description of all the options available with the AMI BIOS, please visit www.ami.com and download their ezPORT PDF file. The options listed on AMI's web site may not be available on your system.

To Access the First Boot setup screen press the F11 key at the beginning of boot.

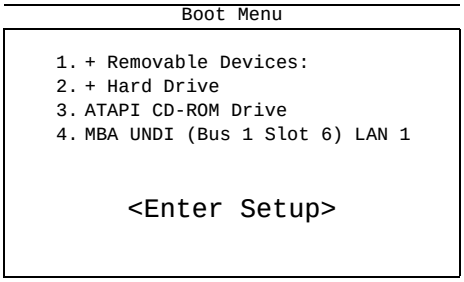
To access the ezPORT setup screens, press the DEL key at the beginning of boot.

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First Boot

The VMICPCI-7808 has a First Boot menu enabling the user to, on a one time basis, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing Windows from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by typing F11 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only and will not be used during the next boot-up of the system. If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.



NOTE: The graphics shown in this section are examples only, view the actual setup screens on your SBC for details.

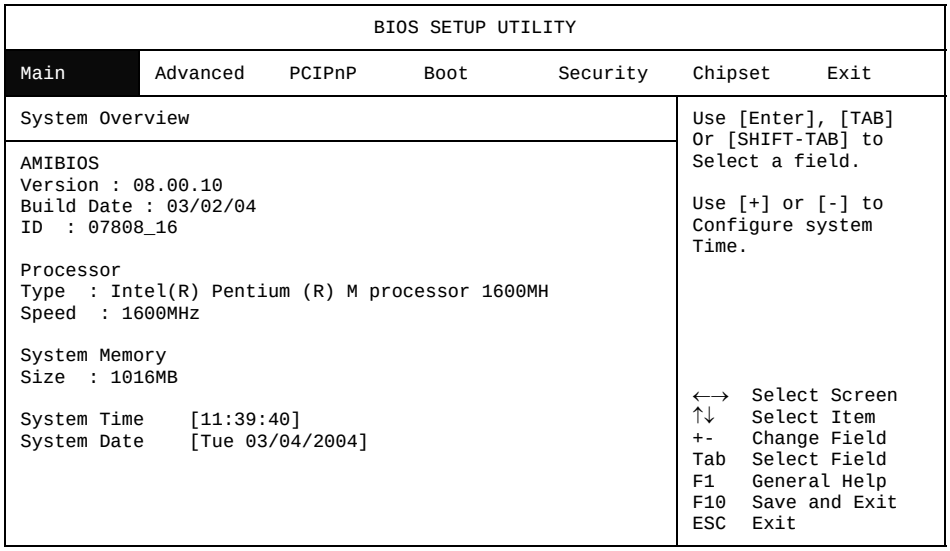
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VMICPCI-7808 Main

The Main BIOS setup menu screen has two main areas. The left frame displays all the options that can be configured. “Grayed-out” options cannot be configured. Options in blue can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white and a text message in the right frame gives a brief description of the option.

The Main menu reports the BIOS revision, processor type and clock speed, and allows the user to set the system’s clock and calendar. Use the left and right arrow keys to select other screens.

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.



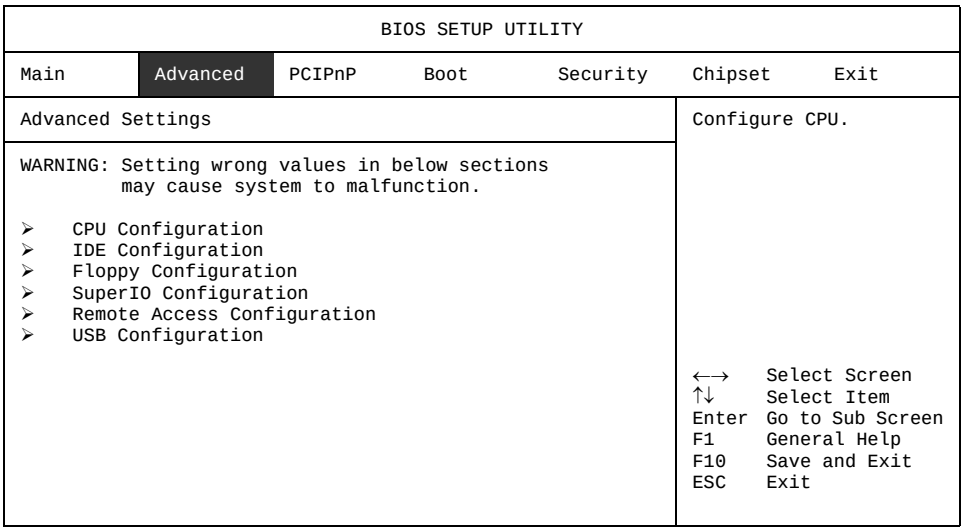
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Advanced BIOS Setup

The Advanced BIOS Setup menu allows the user to configure some CPU settings, the IDE bus, other external devices and internal drives.

Select the *Advanced* tab from the ezPORT setup screen to enter the Advanced BIOS Setup screen. You can select the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. A sample of the Advanced BIOS Setup screen is shown below.

NOTE: Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select 'Load Failsafe Defaults' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Chapter One for instructions on clearing the CMOS.



NOTE: Options shown may not be available on your system.

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PCI/PnP Setup

Included in this screen is the control of internal peripheral cards, as well as various interrupts. From this menu, the user can also determine if the system's plug-and-play is enabled or disabled.

NOTE: Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Chapter One for instructions on clearing the CMOS.

Below is a sample screen of the PCI/PnP menu; options in your system may be different from those shown.

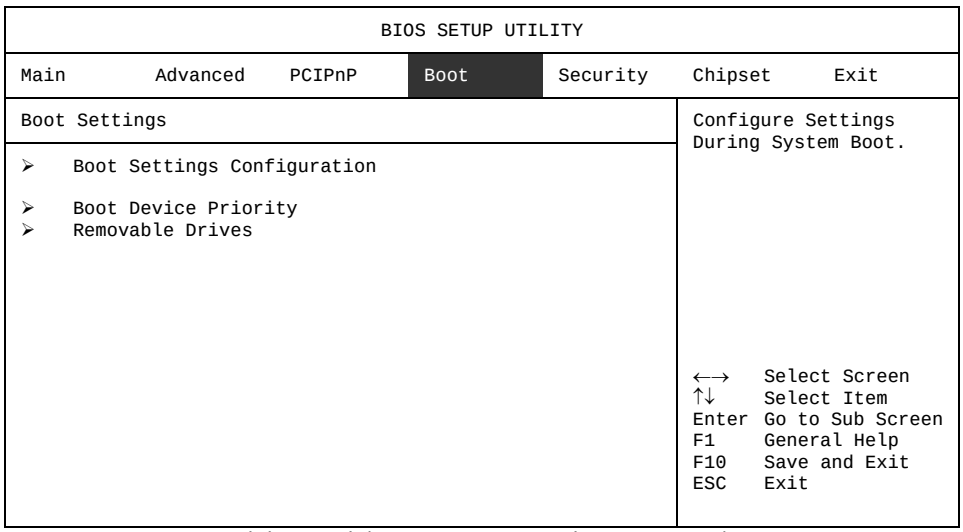
```
                        BIOS SETUP UTILITY
Main      Advanced   PCIPnP   Boot      Security   Chipset   Exit

Advanced PCI/PnP Settings                    | NO: lets the BIOS
                                             | configure all the
WARNING: Setting wrong values in below sections | devices in the system.
         may cause system to malfunction.    | YES: lets the
                                             | operating system
Plug & Play O/S                    [No]      | configure Plug and
PCI Latency Timer                  [64]      | Play (PnP) devices not
Allocate IRQ to PCI VGA            [Yes]     | required for boot if
Palette Snooping                   [Disabled]| your system has a Plug
PCI IDE BusMaster                  [Disabled]| and Play operating
OffBoard PCI/ISA IDE Card          [Auto]    | system.
                                             |
IRQ3                               [Available]|
IRQ4                               [Available]|
IRQ5                               [Available]| ←→  Select Screen
IRQ7                               [Available]| ↑↓  Select Item
IRQ9                               [Available]| +-  Change Option
IRQ10                              [Available]| F1  General Help
IRQ11                              [Available]| F10 Save and Exit
IRQ14                              [Available]| ESC Exit
                  002.53 (C) Copyright 1985-2002, American Megatrends, Inc.
```


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Boot Setup

Use the Boot Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation. Also available in this screen are 'Boot Settings' which allow the user to set how the basic system will act, for example, support for PS/2 mouse and whether to use 'Quick Boot' or not.

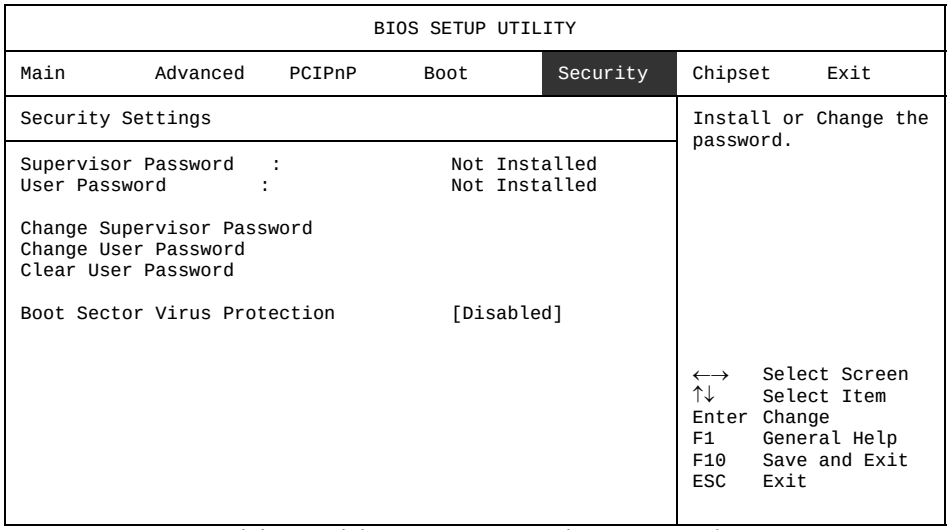


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Security Setup

The ezPORT setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when ezPORT setup is executed, using either the Supervisor password or User password.



To reset the security in the case of a forgotten password you must drain the NVRAM and reconfigure.

To clear the CMOS password:

- Turn off power to the unit.
- Momentarily short pins 1-2 of E4 for approximately five seconds.
- Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared.

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Chipset Setup

Select the various options for chipsets located in the system (for example, the CPU configuration and configurations for the North and South Bridge). The settings for the chipsets are processor dependent and care must be used when changing settings from the defaults set at the factory. Below is a sample of the Chipset Setup screen; the actual options on your system may vary.

NOTE: Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Chapter One for instructions on clearing the CMOS.

```
                              BIOS SETUP UTILITY
Main      Advanced   PCIPnP    Boot      Security  Chipset   Exit

Advanced Chipset Settings                    Intel Montara GML
                                             NorthBridge chipset
WARNING: Setting wrong values in below section Configuration options.
         may cause system to malfunction.

➢  Intel Montara NorthBridge Configuration
➢  Hance Rapids SouthBridge Configuration
➢  CPCI (HINT HB6) Bridge Configuration
➢  Lan (8254EB) Port Routing Options

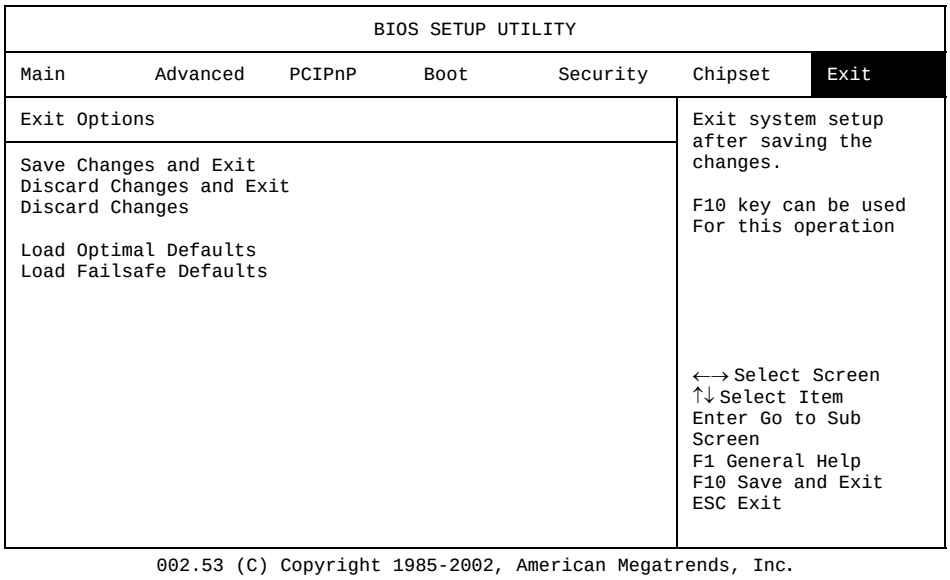
                                             ←→   Select Screen
                                             ↑↓   Select Item
                                             Enter Go to Sub Screen
                                             F1   General Help
                                             F10  Save and Exit
                                             ESC  Exit

                  002.53 (C) Copyright 1985-2002, American Megatrends, Inc.
```


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Exit Menu

Select the *Exit* tab from the ezPORT setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. The Exit BIOS Setup screen is shown below.



If changes have previously been made in the BIOS and the system malfunctions, reboot the system and access this screen. Select 'Load Failsafe Defaults' and continue the reboot.

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Appendix

C

Argon BIOS

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Introduction

The VMICPCI-7808 includes an Argon BIOS option which allows the VMICPCI-7808 to be booted from a network. This appendix describes the procedures to enable this option and the Argon BIOS Setup screens. To access the Argon BIOS setup screen press CTRL+ALT+B when the screen displays the message *'Initializing MBA. Press Ctrl+Alt+B to Configure'*.

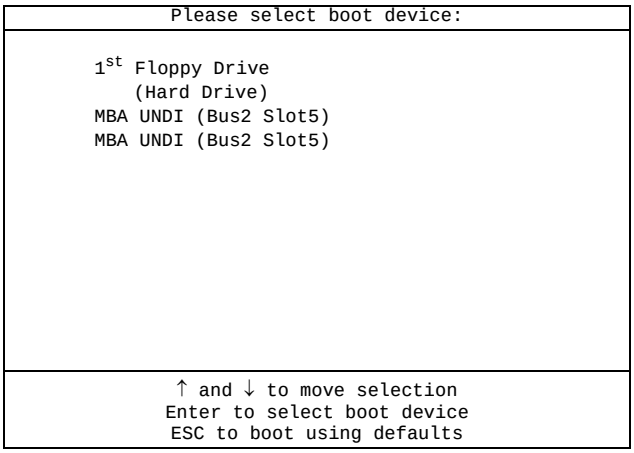
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Boot Menus

There are two methods of enabling the Argon BIOS option. The first method is the *First Boot* menu. The second is the *Boot* menu from the BIOS Setup Utility.

First Boot Menu

Press F11 at the very beginning of the boot cycle, which will access the *First Boot* menu. Selecting "Managed PC Boot Agent (MBA)" to boot from the LAN in this screen applies to the current boot only. At the next reboot the VMICPCI-7808 will revert back to the setting in the Boot menu.



Using the arrow keys, highlight *Managed PC Boot Agent (MBA)* and press the ENTER key to continue with the system boot.

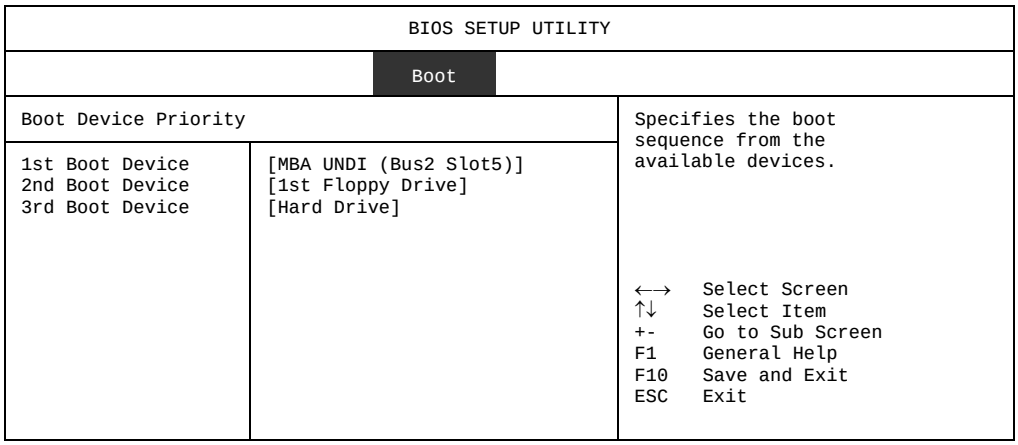
Boot Menu

The second method of enabling the Argon BIOS option is to press the DEL key during system boot. This will access the BIOS Setup Utility. Advance to the Boot menu and then to the Boot Device Priority sub-menu. Use the arrow keys to highlight the Managed PC Boot Agent (MBA) option. Repeat entering <+> until the desired MBA is at the top of the list.

Advance to the Exit menu, select "Exit Saving Changes" and press ENTER. When the system prompts for confirmation, press "Yes". The computer will then restart the system boot-up.

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VMICPCI-7808 BIOS Features Setup

After the Managed PC Boot Agent has been enabled, there are several boot options available to the user. These options are RPL (default), TCP/IP, Netware and PXE. The screens below show the defaults for each boot method.

RPL

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
(c) Copyright 2000 3COM Corporation
All rights reserved
```

```
                              Configuration

     Boot Method:             RPL

     Config Message:          Enabled
     Message Timeout:         3 Seconds
     Boot failure Prompt:     Wait for timeout
     Boot Failure:            Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

TCP/IP

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
(c) Copyright 2000 3COM Corporation
All rights reserved
```

```
                              Configuration

     Boot Method:             TCP/IP

     Protocol                 DHCP
     Config Message:          Enabled
     Message Timeout:         3 Seconds
     Boot failure Prompt:     Wait for timeout
     Boot Failure:            Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```


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Netware

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
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All rights reserved
```

```
                                Configuration

     Boot Method:               Netware

     Protocol                   802.3
     Config Message:            Enabled
     Message Timeout:           3 Seconds
     Boot failure Prompt:       Wait for timeout
     Boot Failure:              Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

PXE

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
(c) Copyright 2000 3COM Corporation
All rights reserved
```

```
                                Configuration

     Boot Method:               PXE

     Config Message:            Enabled
     Message Timeout:           3 Seconds
     Boot Failure Prompt:       Wait for timeout
     Boot Failure:              Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```


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Appendix

D

System Driver Software

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Microsoft Windows XP Professional Software Driver Installation 104

Introduction

The VMICPCI-7808 provides high-performance video, Ethernet access and associated software drivers. High-performance video is provided by the Intel 855GME chipset. High performance LAN operation is provided by a dual-port Intel FW82546EB Gigabit Ethernet adapter. The two Ethernet ports can be configured to allow access to two separate, physical networks. Each Ethernet port is capable of running 10BaseT, 100BaseTX and 1000BaseT.

To optimize performance of each of these PCI-based subsystems, the user must install the driver software located on the distribution CD-ROM provided with the unit. Detailed instructions for the installation of the drivers under Microsoft Windows 2000 Professional and XP Professional are provided in the following section.

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Microsoft Windows 2000 Professional Software Driver Installation

NOTE: Prior to installing device drivers, Windows 2000 should be updated to Service Pack 4 or later. Visit http://support.microsoft.com and search for the latest Service Pack information.

Video Driver Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', 'Run', 'Browse'. In the 'Look in' pull-down selection menu, select the CD-ROM drive. Double-click on the 'Video' folder. Double-click on 'win2k_xp1411'. Click 'OK'.
3. At the 'Intel(R) Extreme Chipset Graphics Driver Software' window, click 'Next'.
4. At the 'Intel(R) Extreme Graphics 2' window, click 'Next'.
5. Click 'Yes' to agree to the software license agreement.
6. Ensure 'Yes, I want to restart my computer now' is selected and click 'Finish'. The computer will restart. The video resolution settings may be changed as desired.

NOTE: If only analog video is being used, ensure that '*Monitor*' is selected as the default video device in the driver.

Hance Rapids Chipset Software Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', 'Run', 'Browse'. In the 'Look in' pull-down selection menu, select the CD-ROM drive. Double-click on the 'Hance Rapids' folder. Double-click on the 'Applications' folder. Double-click on 'infinst_enu'. Click 'OK'.
3. At the 'Intel Chipset Software Installation Utility' window, click 'Next'. Click 'Yes' to agree to the software license agreement. Click 'Next'. At each of the following 'Hardware Installation' windows, click 'Continue Anyway'.
4. Ensure 'Yes, I want to restart my computer now' is selected and click 'Finish'. The computer will restart.

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USB 2.0 EHCI Host Controller

Depending on how the operating system and the latest service pack were installed, the USB 2.0 controller driver may or may not be running. Visit http://support.microsoft.com and search for ***Availability of USB 2.0 Support in Windows 2000 SP1***, for more information on this topic.

To determine whether the driver for the USB 2.0 controller is running, right-click on 'My Computer', and select 'Manage'. In the left pane of the 'Computer Management' window, click on 'Device Manager'. In the right pane, click on the '+' next to 'Universal Serial Bus controllers' to expand the group. If there is a 'Standard Enhanced PCI to USB Host Controller' listed in the group, the USB 2.0 EHCI Host Controller driver is already running, and no further configuration is necessary for the device.

If there is a device labeled 'Universal Serial Bus (USB) controller' under the 'Other devices' section in the right pane of the 'Computer Management' window, the driver has not been installed. To install the driver, right-click on the 'Universal Serial Bus (USB) controller' and select 'Properties' from the drop-down menu, select the 'Driver' tab and select 'Update Driver'. When the wizard starts choose 'Next' and 'Search for a suitable driver' and 'Next again'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. Click 'Next' as necessary then click 'Finish' and 'Close' to close the drivers properties dialog box. Device Manager will relocate the device to the 'Universal Serial Bus controllers' section in the right pane.

Ethernet Adapter Drivers Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Right-click on 'My Computer', and select 'Manage'. In the left pane of the 'Computer Management' window, click on 'Device Manager'.
3. **Intel(R) PRO/1000 MT Dual Port Server Adapter.** Perform this step for each of the Ethernet controllers under the 'Other devices' section in the right pane of the 'Computer Management' window. Right-click on the 'Ethernet Controller' and select 'Properties' from the drop-down menu. Select the 'Driver' tab and select 'Update Driver'. When the wizard starts ensure 'Install the software automatically' is selected and click 'Next'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. Click 'Finish'. Device Manager will relocate the devices to the 'Network adapters' section in the right pane.
4. Click 'X' to close the 'Computer Management' window.
5. Changes may be made to the network configuration as desired.

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Microsoft Windows XP Professional Software Driver Installation

NOTE: Prior to installing device drivers, Windows XP should be updated to Service Pack 1a or later. Visit http://support.microsoft.com and search for the latest Service Pack information.

Video Driver Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', 'Run', 'Browse'. In the 'Look in' pull-down selection menu, select the CD-ROM drive. Double-click on the 'Video' folder. Double-click on 'win2k_xp1411'. Click 'OK'.
3. At the 'Intel(R) Extreme Chipset Graphics Driver Software' window, click 'Next'.
4. At the 'Intel(R) Extreme Graphics 2' window, click 'Next'.
5. Click 'Yes' to agree to the software license agreement.
6. Ensure 'Yes, I want to restart my computer now' is selected and click 'Finish'. The computer will restart. The video resolution settings may be changed as desired.

NOTE: If only analog video is being used, ensure that '*Monitor*' is selected as the default video device in the driver.

Hance Rapids Chipset Software Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', 'Run', 'Browse'. In the 'Look in' pull-down selection menu, select the CD-ROM drive. Double-click on the 'Hance Rapids' folder. Double-click on the 'Applications' folder. Double-click on 'infinst_enu'. Click 'OK'.
3. At the 'Intel Chipset Software Installation Utility' window, click 'Next'. Click 'Yes' to agree to the software license agreement. Click 'Next'. At each of the following 'Hardware Installation' windows, click 'Continue Anyway'.
4. Ensure 'Yes, I want to restart my computer now' is selected and click 'Finish'. The computer will restart.

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USB 2.0 EHCI Host Controller

Depending on how the operating system and the latest service pack were installed, the USB 2.0 controller driver may or may not be running. Visit http://support.microsoft.com and search for ***Availability of USB 2.0 Support in Windows XP SP1***, for more information on this topic.

To determine whether the driver for the USB 2.0 controller is running, click 'Start', right-click on 'My Computer', and select 'Manage'. In the left pane of the 'Computer Management' window, click on 'Device Manager'. In the right pane, click on the '+' next to 'Universal Serial Bus controllers' to expand the group. If there is a 'Standard Enhanced PCI to USB Host Controller' listed in the group, the USB 2.0 EHCI Host Controller driver is already running, and no further configuration is necessary for the device.

If there is a device labeled 'Universal Serial Bus (USB) controller' under the 'Other devices' section in the right pane of the 'Computer Management' window, the driver has not been installed. To install the driver, right-click on the 'Universal Serial Bus (USB) controller' and select 'Update Driver'. Ensure 'Install the software automatically' is selected and click 'Next'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. Click 'Finish'. Device Manager will relocate the device to the 'Universal Serial Bus controllers' section in the right pane.

Ethernet Adapter Drivers Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', right-click on 'My Computer', and select 'Manage'. In the left pane of the 'Computer Management' window, click on 'Device Manager'.
3. **Intel(R) PRO/1000 MT Dual Port Server Adapter.** Perform this step for each of the Ethernet controllers under the 'Other devices' section in the right pane of the 'Computer Management' window. Right-click on the 'Ethernet Controller' and select 'Update Driver'. Ensure 'Install the software automatically' is selected and click 'Next'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. Click 'Finish'. Device Manager will relocate the devices to the 'Network adapters' section in the right pane.
4. Click 'X' to close the 'Computer Management' window.
5. Changes may be made to the network configuration as desired.

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Appendix

E

IPMI Firmware and OEM Extensions

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BMC Functions 123

Introduction

The IPMI firmware provides all the mandatory standard commands specified in the IPMI 1.5 framework. The firmware also provides functionality beyond that of a normal Peripheral Manager, by implementing several commands in the OEM range (per IPMI spec).

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Standard IPMI Commands

The GE Fanuc Embedded Systems' IPMI firmware implements all "Required" commands for a Peripheral Manager per the IPMI 1.5 spec, as well as some of the "Optional" commands.

Get Device ID

This command is used to retrieve the Intelligent device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.

NetFn 0x06, Cmd 0x01

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	
	2	00	Device ID	Unspecified
	3	00	Device Revision	Unspecified
	4	02[1]	Firmware Revision byte 1	Firmware revision 1.08
	5	11[1]	Firmware Revision byte 2	
	6	51	IPMI Version	IPMI version 1.5
	7	2b	Additional device support	The following bits are set: [5] IPMB Event Generator [3] FRU Inventory Device [1] SDR Repository Device [0] Sensor Device
	8:10	CO 33 00	Manufacturer ID	
	11:12[2]	0878	Product ID	

1. Depends on the version of firmware installed on the board.
2. Depends on the type of device.

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Cold Reset

This command performs a "Cold Reset" of the IPMI subsystem. This causes default setting of interrupt enables, event message generation, sensor scanning, threshold values and other "power up default" states to be restored.

NetFn 0x06, Cmd 0x02

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	

Warm Reset

While there are two commands, one for a cold reset, and one for a warm reset, the firmware does not distinguish between them and always performs a cold reset.

NetFn 0x06, Cmd 0x03

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	

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Get Self-Test Results

This command returns the results of the Power-On Self Test.

NetFn 0x06, Cmd 0x04

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	
	2	55h 56h 57h 58h FFh All other	No error. All Self-Tests Passed. Self-Test not implemented in this controller. Corrupted or inaccessible data or devices. Fatal hardware error. Reserved. Device-specific 'internal' failure.	
	3	XXh	If byte 2 is 55h, 56h or FFh, then 00h. If byte 2 is 58h or All other, then device specific. If byte 2 is 57h, then Self-test error bit field. 1b means 'failed', 0b means 'unknown'. [7] 1b = cannot access SEL device [6] 1b = cannot access SDR repository [5] 1b = cannot access FRU device [4] 1b = IPMB signal lines do not respond [3] 1b = SDR repository empty [2] 1b = Internal use area of FRU corrupted [1] 1b = controller update 'boot block' firmware corrupted [0] 1b = controller operational firmware corrupted	

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Set ACPI Power State

This command is used to set the platform management subsystem to a particular power state. The firmware does not support the ACPI power state, instead it can be used to turn off/on power to the board.

NetFn 0x06, Cmd 0x06

	Byte	Value	Data Field	Comments
Request-data	1	XXh	ACPI System power state	The GE Fanuc Embedded Systems IPMI does not have control over the system power state. Therefore, this byte is ignored.
	2	XXh	ACPI Device power state [7] – 1b = set device power state 0b = don't change device power state [6:0] – device power state 00h – Fully on 03h – Power off	
Response-data	1	XXh	Completion Code	

Get ACPI Power State

This command is used to get the platform management subsystem's power state. The firmware does not support the ACPI power state, instead it only returns whether the board has its power turned off/on.

NetFn 0x06, Cmd 0x07

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	
	2	2Ah	ACPI System Power State [7] – reserved [6:0] – System power state 2Ah – unknown	The GE Fanuc Embedded Systems IPMI subsystem does not have control over the system power.
	3	XXh	ACPI Device Power State 00h – Fully on 03h – Power off 2Ah – unknown, power state has not been initialized or device lost track of power state.	

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Get Device GUID command

This command returns a Globally Unique ID (GUID) for the management controller. The format of the ID follows that specified in Attachment A of the *Wired for Management Baseline, Version 2.0 specification*. The ID can be used to uniquely identify an instance of a management controller. This information can be used in conjunction with the SDR information to verify that a particular controller is still present in the system.

NetFn 0x06, Cmd 0x08

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00h	Completion code	
	2	XXh	node	
	3	XXh	node	
	4	XXh	node	
	5	XXh	node	
	6	XXh	node	
	7	XXh	node	MS byte
	8	XXh	clock seq low	
	9	XXh	clock seq high and reserved	MS byte
	10	XXh	time high and version	
	11	XXh	time high and version	MS byte
	12	XXh	time mid	
	13	XXh	time mid	MS byte
	14	XXh	time low	
	15	XXh	time low	
	16	XXh	time low	
	17	XXh	time low	MS byte

Broadcast Get Device ID

This is a broadcast version of the "Get Device ID" command that is provided for the discovery of Intelligent Devices on the IPMB. It is only specified for use on the IPMB.

The response for a *Broadcast 'Get Device ID'* is the same as that returned for a *'Get Device ID'* command.

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Master-Write-Read

This command can be used for low-level I^2C/SMBus write, read, or write-read accesses to the IPMB or private buses behind the management controller.

NetFn 0x06, Cmd 0x52

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Bus ID: [7:4] channel number [3:1] bus ID, 0-based [0] bus type 0 = public (IPMB) 1 = private bus	This byte can take one of following three values, depending on which bus will be used: 0x0 = I2C0 (IPMB 0x3 = I2C1 (CPCI-SMB) 0xf = I2C2 Local 1^2C
	2	XXh	Slave Address [0] - reserved	
	3	XXh	Read count – number of bytes to read 1 based, 0 = no bytes to read.	
	4:N		Data to write	
Response-data	1	XXh	Completion code 00h – if successful 81h – Lost Arbitration 82h – Bus Error 83h – NAK on Write 84h – Truncated Read	
	2:M		Bytes read from the specified slave address.	

Set Event Receiver

This command sets the slave address and the LUN of the Event Receiver, which will receive the Event Messages generated by the GE Fanuc Embedded Systems IPMI subsystem.

NetFn 0x04, Cmd 0x00

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Event Receiver Slave Address. 0FFh disables Event message generation [7:1] - IPMB (I^2C) slave address [0] - 0	
	2	XXh	[7:2] – reserved [1:0] – Event receiver LUN	
Response-data	1	00	Completion code	

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For a list of platform events generated by the GE Fanuc Embedded Systems IPMI subsystem see *Platform Events* on page 121.

Get Event Receiver

This command gets the current setting for the Event Receiver slave address and LUN.

NetFn 0x04, Cmd 0x01

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	XXh	Completion code	
	2	XXh	Event Receiver Slave Address. 0FFh disables Event message generation [7:1] - IPMB (I^2C) slave address [0] - 0	
	3	XXh	[7:2] – reserved [1:0] – Event receiver LUN	

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Get Sensor Reading

This command returns the present reading for the sensor. Sensors are periodically scanned, and the last reading will be immediately returned in response to this command.

NetFn 0x04, Cmd 0x2D

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Sensor Number (FFh reserved)	
Response-data	1	00h	Completion code	
	2	XXh	Sensor reading	
	3	XXh	[7] – 0b = All event messages disabled for this sensor [6] - 0b = Sensor scanning disabled [5] – 1b = Initial update in progress. [4-0] – reserved	
	4	XXh	For threshold-based sensors, Present threshold comparison status. For discrete reading sensors, State 0-7 assert condition.	
	5	XXh	State 8-14 assert condition	Optional for discrete reading sensors

The GE Fanuc Embedded Systems IPMI subsystem contains several sensors. They provide the voltages and temperature reading of the system. The various sensor settings like threshold, hysteresis, event enable, etc., are statically configured in the Sensor Data Records.

Sensor No	Type	Comments
0x41	3.3V	Switched on/off by hotswap controller, *BDSEL etc.
0x42	5V	Switched on/off by hotswap controller, *BDSEL etc.
0x43	3.3V IN backplane	
0x44	5V IN backplane	
0x60	Temp Sensor	
0x61	Temp Sensor	

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The sensor readings returned are in their "raw" values; to convert them to actual values use the following formulas below.

a. For 3.3V sensors

$V_a = (V_r / 256) * (3.3 / 2.5) * 3.3$

Where V_a = actual voltage

V_r = "raw" sensor reading

e.g.: if sensor 0x41 says 0xC0 (192 decimal), the actual voltage is (192/256) * 3.3/2.5 * 3.3 = 3.267 V.

b. For 5V sensors

$V_a = (V_r / 256) * 3.3 * 2$

Where V_a = actual voltage

V_r = "raw" sensor reading

e.g.: if sensor 0x44 says 0xC3 (195 decimal), the actual voltage is (195/256) * 3.3 * 2 = 5.027 V.

c. For Temp sensors

$T_a = T_r$

Where T_a = actual temperature in ^oC

T_r = "raw" sensor reading

e.g.: if sensor 0x61 says 0x1f (31 decimal), the actual temperature is 31^o C.

FRU Inventory Area Info

This command is used to obtain information about the size and access method of the FRU Inventory data in the device.

NetFn 0x0A, Cmd 0x10

	Byte	Value	Data Field	Comments
Request-data	1	XXh	FRU device ID. FFh reserved.	
Response-data	1	00h	Completion code	
	2	XXh	FRU inventory area size in bytes, LS Byte.	
	3	XXh	FRU inventory area size in bytes, MS Byte.	
	4	XXh	[7:1] – reserved [0] – 0b = accessed by bytes 1b = accessed by words	

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Read FRU Data

This command returns the specified data from the FRU Inventory Info area. No parsing of the FRU data is performed by the IPMI subsystem; system management software is responsible for interpreting the FRU data.

NetFn 0x0A, Cmd 0x11

	Byte	Value	Data Field	Comments
Request-data	1	XXh	FRU device ID. FFh reserved.	
	2	XXh	FRU Inventory offset to read. LS Byte.	
	3	XXh	FRU Inventory offset to read. MS Byte.	Offset is in words or bytes per device access type returned in the FRU Inventory Area Info command.
	4	XXh	Count to read – 1 based	
Response-data	1	00	Completion code	
	2	XXh	Count returned – 1 based	
	3:2+N		Requested data	

The FRU data conforms to the *IPMI FRU Information Storage Definition v 1.0* specification. All GE Fanuc Embedded Systems IPMI-enabled boards come with the FRU data preloaded; the specific data is documented in *FRU Data Specification* on page 120.

Write FRU Data

This command writes the specified byte or word to the FRU Inventory Info area. No parsing of the FRU data is performed by the IPMI subsystem; system management software is responsible for creating valid FRU data structures and writing the data to the FRU area.

NetFn 0x0A, Cmd 0x12

	Byte	Value	Data Field	Comments
Request-data	1	XXh	FRU device ID. FFh reserved.	
	2	XXh	FRU Inventory offset to write. LS Byte.	
	3	XXh	FRU Inventory offset to write. MS Byte.	
	4:3+N		Data to write	
Response-data	1	XXh	Completion code 00h – successful 80h – Write protected	
	2	XXh	Count written – 1 based	

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Get SDR Repository Info

This command returns the SDR command version for the SDR Repository.

NetFn 0x0A, Cmd 0x20

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00h	Completion code	
	2	51h	SDR Version.	
	3	XXh	Record count LS Byte.	
	4	XXh	Record count MS Byte.	
	5:6	XXXXh	Free space in bytes. LS Byte first. 000h indicates 'full' FFFEh indicates 64KB-2 or more, FFFFh indicates 'unspecified'.	
	7:10	00000000h	Most recent addition timestamp. LS Byte first.	Add SDR or Partial-Add SDR command not supported, always returns 00000000.
	11:14	00000000h	Most recent erase (delete or clear) timestamp. LS Byte first.	Delete SDR or Clear SDR command not supported, always returns 00000000.
	15	02h	Operation Support [7] – Overflow flag =1	Only Reserve SDR Repository command supported.

Reserve SDR Repository Command

This command is used to set the present 'owner' of the repository, as identified by the 'Software ID' or by the Requester's Slave Address from the command. The reservation process provides a limited amount of protection on repository access from the IPMB when records are being incrementally read.

NetFn 0x0A, Cmd 0x22

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00h	Completion Code.	
	2	XXh	Reservation ID, LS Byte.	
	3	XXh	Reservation ID, MS Byte.	

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Get SDR Command

This command returns the sensor record specified by 'Record ID'. The command also accepts a 'byte range' specification that allows just a selected portion of the record to be retrieved. The Requester must first reserve the SDR Repository using the "Reserver SDR Repository' command in order for an incremental read to an offset other than 0000h to be accepted.

If 'Record ID' is specified as 0000h, this command returns the Record Header for the 'first' SDR in the repository. FFFFh specifies that the 'last' SDR in the repository should be listed. If 'Record ID' is non-zero, the command returns the information from the matching record, and the Record ID for the *next* SDR in the repository.

NetFn 0x0A, Cmd 0x23

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Reservation ID, LS Byte.	Only required for partial reads with a non-zero 'Offset into record' field. Use 0000h otherwise.
	2	XXh	Reservation ID, MS Byte.	
	3	XXh	Record ID of record to Get, LS Byte.	
	4	XXh	Record ID of record to Get, MS Byte.	
	5	XXh	Offset into record.	
	6	XXh	Bytes to read, FFh means read entire record.	
Response-data	1	XXh	Completion Code	
	2	XXh	Record ID for next record, LS Byte.	
	3	XXh	Record ID for next record, MS Byte.	
	4:3+N	XXh	Record Data	

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FRU Data Specification

GE Fanuc Embedded Systems boards have data pre-loaded into the FRU area to provide basic information about the board. The FRU data conforms to the '*Platform Management FRU Information Storage Definition*', Revision 1.1. Please refer to this document, available from Intel, for the exact meaning of the various fields.

Only the Board Info and Product Info areas are utilized. An example of the entire contents of the FRU EEPROM is given below:

```
0000  01 00 00 01 00 00 00 FE-01 09 00 E8 44 41 D9 47   ............DA.G
0010  45 20 46 41 4E 55 43 20-45 6D 62 65 64 64 65 64   E FANUC Embedded
0020  20 53 79 73 74 65 6D 73-CC 56 4D 49 43 50 43 49    Systems.VMICPCI
0030  2D 37 38 30 36 C5 31 30-30 30 31 CE 33 35 30 2D   -7808.10001.350-
0040  36 35 37 38 30 36 2D 32-31 30 C0 C1 00 00 00 B1   657808-210......
0050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0070  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0080  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0090  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00A0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00B0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00C0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00D0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00E0  CA 45 54 F3 90 B6 80 49-94 B0 0B F8 C2 78 47 FD   .ET....I.....xG.
00F0  C0 33 00 06 78 00 00 00-00 00 00 00 00 00 00 00   .3..x...........
```


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Platform Events

The GE Fanuc Embedded Systems IPMI subsystem contains several sensors for reading the voltages and temperature of the system. Each sensor is configured with a threshold, hysteresis, and nominal value. When the value of a sensor crosses a threshold, a platform event is sent to the "Event Receiver".

The following events are generated by the GE Fanuc Embedded Systems IPMI Subsystem:

- Threshold Events – Events of this type are generated if the sensors exceed their threshold settings. Threshold events are either an Assertion Event or a De-Assertion Event.

  NetFn 0x04, Cmd 0x02

	Byte	Value	Data Field	Comments
Request-data	-	-	Generator ID (RqSA, RqLun)	
	1	03h	EvMRev	IPMB v 1.0 message
	2	XXh	Sensor Type	02h = voltage sensors 01h = temperature sensors
	3	XXh	Sensor #	Sensor numbers will be one of 41h, 42h, 43h, 44h, 60h or 61h
	4	XXh	[7] - Event Dir 0b = Assertion Event 1b = De-assertion Event [6:0] - Event Type	Event Type indicates the type of threshold crossing that produced the event.
	5	XXh	Event Data 1 [7:6] – 01b = trigger reading in byte2 [5:4] – 01b = trigger threshold value in byte3 [3:0] - offset from Event/Reading code for threshold event	
	6	XXh	Event Data 2	Sensor reading
	7	XXh	Event Data 3	Threshold value that triggered event.
Response-data	1	XXh	Completion Code	

The Generator ID field is a required element of an Event Request Message. For IPMB messages, this field is equated to the Requestor's Slave Address and LUN fields. Thus, the Generator ID information is not carried in the data field of an IPMB request message.

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Chassis Control

All GE Fanuc Embedded Systems IPMI-enabled boards include extra circuitry to enable the IPMI controller to monitor and control certain CompactPCI signals. These functions are controlled by sending IPMI packets from the VMICPCI-7808 processor card to the controller.

Get Geographical Address

This command returns the Slave Address based on the Geographical Slot the board is inserted into.

NetFn 0x30, Cmd 0x01

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	XXh	Completion code	
	2	XXh	Geographical address	

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BMC Functions

The GE Fanuc Embedded Systems IPMI firmware can perform some of the functions of a Baseboard Management Controller. The firmware can send IPMI commands to other targets on the IPMB on behalf of the VMICPCI-7808, and return the responses to the VMICPCI-7808. It can also forward any platform events it receives to the VMICPCI-7808.

IPMB Relay

This command allows the VMICPCI-7808, connected to the Zircon's I^2C1 bus, to have the Zircon send a command on its I^2C0 bus (which is connected to the IPMB pins on the backplane), and for the Zircon to send the response to that command back to the VMICPCI-7808 on I^2C1.

NOTE: The Zircon will accept an IPMB Relay request on its I^2C0 bus, but it will always send the response to the I^2C1 bus. Therefore, any device on the IPMB that sends an IPMB Relay request to the Zircon will not receive a response.

If the request is successfully sent, then the response will be the actual response from the target system, with only a few header bytes changed to have it sent back to the VMICPCI-7808.

If the request cannot be relayed (due to a device not responding, or the Zircon is temporarily out of memory), the response to this command will use the NetFn and Cmd for IPMB Relay, and a completion code only.

NetFn 0x32, Cmd 0x00

	Byte	Value	Data Field	Comments
Request-Data	1	XXh	[7:1] – Target slave address [0] – 0	
	2	XXh	[7:6] – 0 [5:0] – NetFn	
	3	XXh	[7:2] – 0 [1:0] – LUN	
	4	XXh	Command	
	5:N	XXh	Optional Data	
Response-data	1	XXh	Completion code	
	2:N	XXh	Optional response data	See examples below

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Forwarding of Platform Events

A chassis may contain other IPMI devices, such as an alarm card, which will generate Platform Events. The alarm card would send the event to the I^2C slave address that was provided by a "Set Event Receiver" command. The GE Fanuc Embedded Systems IPMI firmware will immediately acknowledge any Platform Event it receives then forward the packet to the slave address provided by a "Set Platform Event Forwarding Address" command.

The VMICPCI-7808 should not send a response for the Platform Event to the Zircon nor to the originating device, as the Zircon has already responded.

Software on the VMICPCI-7808 should set the forwarding address first then use IPMB relay to send a "Set Event Receiver" command to the alarm cards or other IPMI devices in the chassis.

Set Platform Event Forwarding Address

This command sets the slave address and the LUN of the Event Receiver to which the Platform Events are forwarded.

NetFn 0x32, Cmd 0x80

	Byte	Value	Data Field	Comments
Request-data	1	XXh	[7:1] – I2C slave address [0] – always 0	
	2	XXh	[7:2] – 0 [1:0] – LUN	
Response-data	1	XXh	Completion code	

If the forwarding address is 0 (by default, or deliberately set), events will not be forwarded.

In all cases, any Platform Events will be acknowledged back to the original sender. The VMICPCI-7808 should not acknowledge the forwarded event back to the IPMI controller.

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Additional Resources

For more information, please visit the GE Fanuc Embedded Systems web site at:

www.gefanucembedded.com

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