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ICS-554

OPERATING MANUAL

Interactive Circuits and Systems Ltd.

October 2006

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1 INTRODUCTION

The ICS-554 is a four channel, 14-bit A/D module in a PCI Mezzanine Card (PMC) format. The ICS-554 product is available in several versions. Each version has a nominal signal input impedance of 50 Ohms, and conforms to the PCI 2.2 (64-bit, 66 MHz) standard, with Master Burst Mode (DMA) capability. Each version has a different sampling frequency range, and is optionally available with Graychip DDC modules (-MN option).

All versions include a user programmable FPGA that provides flexible digital signal processing capability for software digital radio and radar applications. The FPGA has connections to the Pn4 User I/O connector (see Reference [7]) to allow high speed serial and parallel data to be passed via this port, and to enable customer specific signals to be connected to the FPGA.

The ICS-554A is a four channel, 14-bit PMC Module data acquisition card, with a maximum sampling rate of 80 MHz per channel. The internal sample clock oscillator is an 80 MHz fixed frequency crystal. The design includes a one million gate FPGA. The FPGA connections to the Pn4 connector provide LVTTL compatible signaling.

The ICS-554B version has a 105 MHz maximum sample rate per channel (also ICS-554C, ICS-554D and ICS-554E versions) and has a one million gate FPGA. The internal sample clock oscillator is a 100 MHz fixed frequency crystal. The Pn4 signaling is LVTTL compatible.

The ICS-554C version of the product includes a three million gate FPGA and provides sampling frequencies in the range of 80 – 105 MHz. Other aspects of this product are the same as the ICS-554B version.

The ICS-554D version includes four op-amp DC-coupled signal inputs for baseband sampling. As an ordering option, the signal input impedance may be selected as 1 MOhm. It provides sampling frequencies in the range of 30 – 105 MHz, as for the ICS-554B version. The FPGA has three million gates. The Pn4 signaling is LVTTL compatible, but has the ordering option of LVDS compatible Pn4 connections.

The ICS-554E version provides the same features as the ICS-554C version, but has the ordering option of LVDS compatible Pn4 connections.

For more information concerning LVTTL and LVDS signaling for the different versions of the ICS-554 board, refer to Section 2 of this document, APPENDIX C and Reference [7].

These products offer a wide range of operating modes and features; their design has been optimized for applications that demand high speed, precision and ease of integration.

ICS offers software drivers for the ICS-554 for a number of platforms, including Windows, VxWorks, and Linux. These drivers greatly simplify control and operation of the ICS-554, and are strongly recommended. Using one of these drivers will generally save the programmer a significant amount of time since they are relieved of the requirement of understanding the complexities of the ICS-554 board.

All references to ICS-554 in this manual apply to all models, except where stated.

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2 GENERAL DESCRIPTION

Figure 1 shows a simplified block diagram of the ICS-554 board (A, B, C and E versions). Figure 2 shows a simplified block diagram of the ICS-554 board (D version) showing the four op-amp DC-coupled signal inputs. The board uses four 14-bit ADCs (Analog Devices AD6645). The maximum sampling rate is 80 MHz for the A version of the product, and 105 MHz for the B, C, D and E versions (100 MHz maximum sampling rate with the optional use of the DDCs).

The ICS-554 includes a 66 MHz/64-bit PCI bus interface conforming to the PCI 2.2 specification. The PCI interface uses the QuickLogic QL5064 chip to support a master burst transfer (DMA) interface. The ICS-554 can generate PCI bus interrupts at any user-programmed interval (number of samples acquired).

The sampling clock and the trigger can be either internal or external. The internal ADC clock is a crystal oscillator with a fixed frequency of 80 MHz on the ICS-554A-w-x Rev.z version, and 100 MHz for the ICS-554B-w-x Rev.z, ICS-554C-w-x Rev.z, ICS-554D-w-xy Rev.z and ICS-554E-w-xy Rev.z versions (see version number description in Sections 2.1 to 2.4). The external clock signal may be either a TTL level or sinewave signal with a frequency in the range 30 – 80 MHz for the ICS-554A-w-x Rev.z version, and 100 MHz for the ICS-554B-w-x Rev.z, ICS-554C-w-x Rev.z, ICS-554D-w-xy Rev.z and ICS-554E-w-xy Rev.z versions (see specifications for the model name definitions).

The ADCs can be operated in a number of different modes. In the continuous mode, data is continuously converted on all selected channels and supplied to the PCI Bus interface upon application of a trigger signal, until the acquisition is disabled. In capture mode, a fixed number of samples are acquired upon each application of the trigger. The number of samples acquired at each application of the trigger is programmable with a resolution of four samples per channel or less, up to the maximum capacity of the buffer. The programmable ADC output decimator can reduce the output data rate by a factor of up to thirty-two.

The outputs of the ADCs are applied to a bank of four quad digital down-converter (DDC) modules on product versions with this option, which are Graychip GC4016 devices. Note that the ADC outputs are also connected to a Xilinx FPGA for direct processing of the ADC data. A crossbar switch is supplied as standard firmware in the FPGA to enable the user to select either the ADC output or the DDC output, under program control. Please refer to Section 4.1 for more information on DDC output.

The output of the FPGA is buffered in two 64K x 72 FIFO memories. PCI Bus interrupts are available for a user programmed threshold level and overflow conditions of the FIFO. The FIFO outputs are applied to the PCI Bus interface, which is implemented using a QuickLogic QL5064 part. This provides a PCI 2.2 compliant 64-bit, 66 MHz PCI interface with Master/Target DMA supporting chain-mode (scatter-gather) DMA.

All power requirements of the ICS-554 are satisfied with PCI Bus or PMC standard voltages.

The ICS-554A, B and C versions support LVTTL signaling for +3.3 V. As shipped from the factory, the standard boards include pads at the Pn4 connector to allow resistors to be installed to connect the signals to ground, for cases in which signals must be terminated (such as the use of FPDP output). When signals are terminated, 110 Ohm resistors are used. If suitable resistors are installed, pins 63 and 64 of Pn4 can be driven from a PECL buffer which is driven from the FPGA pin E13 for versions A and B and pin G15 for version C. The factory defaults can be changed to provide other configurations by means of custom product numbers at the customer's request.

The ICS-554D and ICS-554E are the only versions of the ICS-554 product that support LVDS signaling (they have signal routing that is paired and matched in length for LVDS differential signals). As shipped from the factory, the standard boards up to and including ICS-554D Rev.A (assembly drawing up to and including B11945E or B12048Bx) include 100 Ohm resistors installed between each LVDS signal pair, except for the signals attached to Pn4 pins 63 and 64. All other ICS-554D boards do not include 100 Ohm resistors installed between each LVDS signal pair and between Pn4 pins 63 and 64. As shipped from the

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factory, the standard boards up to and including ICS-554E Rev.A (assembly drawing up to and including B11821C or B12047Bx) include 100 Ohm resistors installed between each LVDS signal pair, except for the signals attached to Pn4 pins 63 and 64. All other ICS-554E boards do not include 100 Ohm resistors installed between each LVDS signal pair and between Pn4 pins 63 and 64.

For ICS-554D and ICS-554E, there are also pads at the Pn4 connector to allow resistors to be installed to connect the signals to ground, for cases in which signals must be terminated (such as the use of FPDP output). If suitable resistors are installed, pins 63 and 64 of Pn4 can be driven from a PECL buffer which is driven from the FPGA pin A21. The factory defaults can be changed to provide other configurations by means of custom product numbers at the customer's request.

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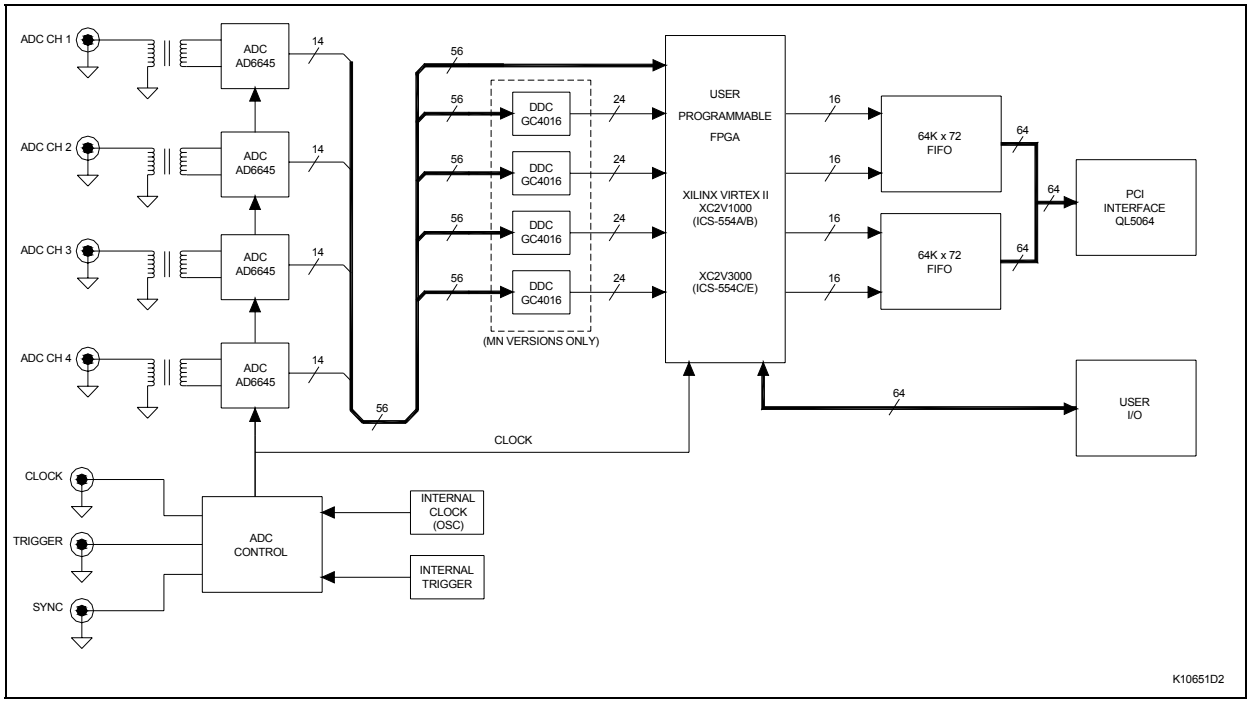


Figure 1 – ICS-554 Block Diagram (A, B, C and E Versions)

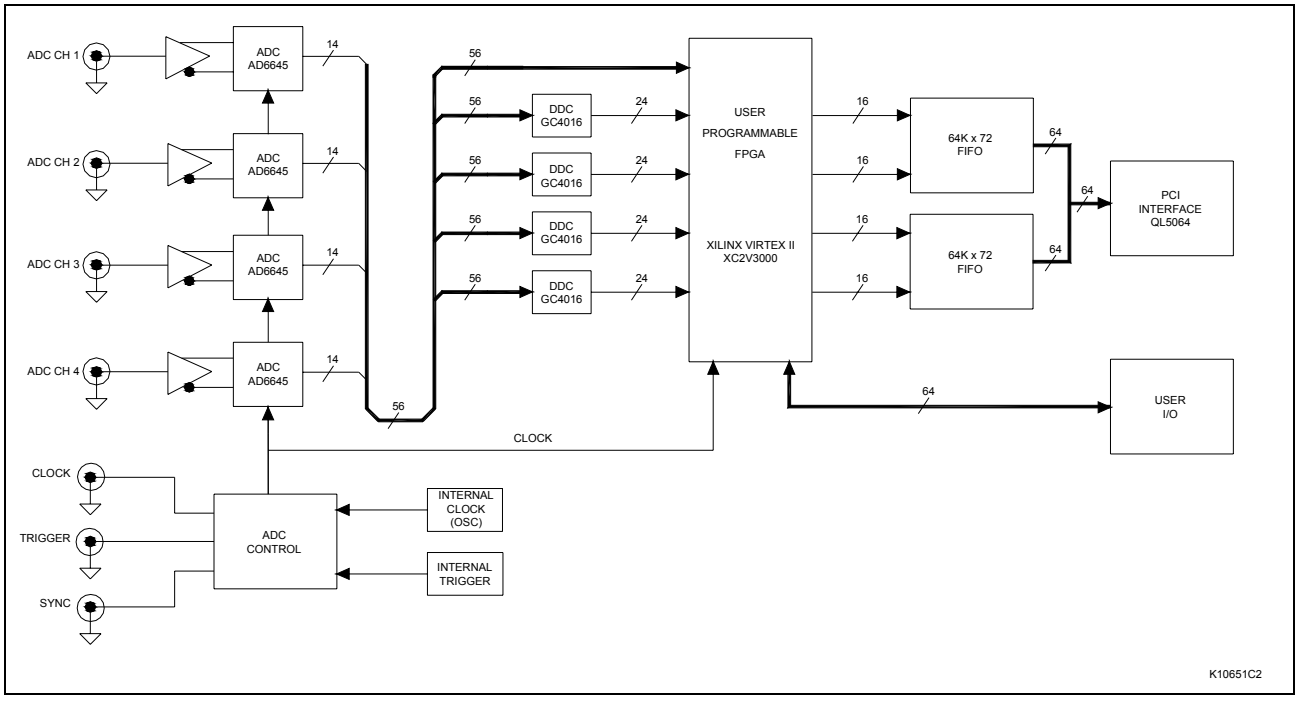


Figure 2 - ICS-554 Block Diagram (D Version)

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2.1 ICS-554A Specifications

Versions: ICS-554A-**w**-**x** Rev.**z**

–	= Board Revision
A (and up)	= Board Revision

1, 2 or 4	= # of ADC Channels

	= no DDCs
MN	= 4 DDCs

ANALOG INPUT	
Number of Analog Input Channels:	4
Analog Connector Type:	SMA Coaxial
Input Impedance:	50 Ohm
Full Scale Input:	1.2 Volts peak-to-peak (+5.5 dBm) into 50 Ohms
Maximum Safe Input Voltage	± 2.5 Volts into 50 Ohms
Input Signal Bandwidth:	2 MHz – 200 MHz (-3 dB point)
Max. Sampling Rate:	80 MHz/ch. for 4 channels, simultaneous
Min. Sampling Rate:	30 MHz/ch. for 4 channels, simultaneous [1]
Internal Sample Clock Oscillator:	80 MHz fixed frequency crystal
ADC Resolution:	14 bits
Sampling:	Rising edge of internal or external sample clock
External trigger:	Sampling occurs on rising edge of clock following rising or falling edge of external trigger (programmable). Trigger must remain high for at least one clock cycle.
Spurious Free Dynamic Range (SFDR):	>85 dB (at 100 MHz sampling, ignoring signal harmonics) [2]
Signal-to-Noise Ratio (S/(N+D)):	> 71 dB @ 80 MHz [2]
On-board Storage:	1 MByte total
GENERAL	
PCI bus Interface:	PCI 2.2 64-bit 66 MHz, Master Burst Mode (DMA) capable Keyed for universal signaling
Optional Digital Downconverter (model ICS-554A-w-MN Rev.z):	Up to 4 wide band channels or 16 narrow band channels using 4 x Graychip GC4016
User I/O:	64 I/Os connected to User programmable FPGA
User Programmable FPGA:	1M gates Xilinx XC2V1000
Board Size	CMC single width form factor (see Reference [2])
Board Weight	140 g
Environmental:	
Operating Temp:	0°- 50°C (at entry point of forced air)
Storage Temp:	-40° - +85°C
Humidity:	95% non-condensing
Cooling:	Approximately 200 LFM
Power:	+5 V @ 1.5 A (model ICS-554A-w-MN Rev.z) +5 V @ 1.0 A (model ICS-554A-w Rev.z) +3.3 V @ 0.8 A

Specifications subject to change without notice

[1] The specified minimum sample rate is 30 MHz. The product can be operated at sample rates down to 5 MHz, but the performance is not guaranteed in this case.

[2] The SFDR & SNR specification is set-up dependent. Please see Reference [9]. For best results ICS recommends the use of external clock.

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2.2 ICS-554B Specifications

Versions: ICS-554B-**w**-**x** Rev.**z**

–	= Board Revision
A (and up)	= Board Revision

1, 2 or 4	= # of ADC Channels

	= no DDCs
MN	= 4 DDCs

ANALOG INPUT	
Number of Analog Input Channels:	4
Analog Connector Type:	SMA Coaxial
Input Impedance:	50 Ohm
Full Scale Input:	1.2 Volts peak-to-peak (+5.5 dBm) into 50 Ohms
Maximum Safe Input Voltage	± 2.5 Volts into 50 Ohms
Input Signal Bandwidth:	2 MHz – 200 MHz (-3 dB point)
Max. Sampling Rate:	105 MHz/ch. for 4 channels, simultaneous 100 MHz/ch. for 4 channels, simultaneous, when using DDCs
Min. Sampling Rate:	30 MHz/ch. for 4 channels, simultaneous [1]
Internal Sample Clock Oscillator:	100 MHz fixed frequency crystal
ADC Resolution:	14 bits
Sampling:	Rising edge of internal or external sample clock
External trigger:	Sampling occurs on rising edge of clock following rising or falling edge of external trigger (programmable). Trigger must remain high for at least one clock cycle.
Spurious Free Dynamic Range (SFDR):	>85 dB (at 100 MHz sampling, ignoring signal harmonics) [2]
Signal-to-Noise Ratio (S/(N+D)):	> 71 dB @ 105 MHz [2]
On-board Storage:	1 MByte total
GENERAL	
PCI bus Interface:	PCI 2.2 64-bit 66 MHz, Master Burst Mode (DMA) capable Keyed for universal signaling
Optional Digital Downconverter (model ICS-554B-w-MN Rev.z):	Up to 4 wide band channels or 16 narrow band channels using 4 x Graychip GC4016
User I/O:	64 I/Os connected to User programmable FPGA
User Programmable FPGA:	1 M gates Xilinx XC2V1000
Board Size	CMC single width form factor (see Reference [2])
Board Weight	140 g
Environmental:	
Operating Temp:	0°- 50°C (at entry point of forced air)
Storage Temp:	-40° - +85°C
Humidity:	95% non-condensing
Cooling:	Approximately 200 LFM
Power consumption at 20 deg. C:	+5 V @ 1.7 A (model ICS-554B-w-MN Rev.z) +5 V @ 1.0 A (model ICS-554B-w Rev.z) +3.3 V @ 0.8 A

Specifications subject to change without notice

[1] The specified minimum sample rate is 30 MHz. The product can be operated at sample rates down to 5 MHz, but the performance is not guaranteed in this case.

[2] The SFDR & SNR specification is set-up dependent. Please see Reference [9]. For best results ICS recommends the use of external clock.

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2.3 ICS-554C/E Specifications

ICS-554C/E Versions: ICS-554**v-w-xy** Rev.**z**

–	= Board Revision
A (and up)	= Board Revision

C or E	= Board Version

1, 2 or 4	= # of ADC Channels

	= LVTTL
L	= LVDS

	= no DDCs
MN	= 4 DDCs

ANALOG INPUT	
Number of Analog Input Channels:	4
Analog Connector Type:	SMA Coaxial
Input Impedance:	50 Ohm
Full Scale Input:	1.2 Volts peak-to-peak (+5.5 dBm) into 50 Ohms
Maximum Safe Input Voltage	± 2.5 Volts into 50 Ohms
Input Signal Bandwidth:	2 MHz – 200 MHz (-3 dB point)
Max. Sampling Rate:	105 MHz/ch. for 4 channels, simultaneous 100 MHz/ch. for 4 channels, simultaneous, when using DDCs
Min. Sampling Rate:	80 MHz/ch. for 4 channels, simultaneous
Internal Sample Clock Oscillator:	100 MHz fixed frequency crystal
ADC Resolution:	14 bits
Sampling:	Rising edge of internal or external sample clock
External trigger:	Sampling occurs on rising edge of clock following rising or falling edge of external trigger (programmable). Trigger must remain high for at least one clock cycle.
Spurious Free Dynamic Range (SFDR):	>85 dB (at 100 MHz sampling, ignoring signal harmonics) [1]
Signal-to-Noise Ratio (S/(N+D)):	> 71.5 dB @ 105 MHz [1]
On-board Storage:	1 MByte total
GENERAL	
PCI bus Interface:	PCI 2.2 64-bit 66 MHz, Master Burst Mode (DMA) capable
Optional Digital Downconverter (model ICS-554C/E-w-MN Rev.z):	Up to 4 wide band channels or 16 narrow band channels
User I/O:	64 I/Os connected to User programmable FPGA
User Programmable FPGA:	3 M gates Xilinx XC2V3000
Board Size	CMC single width form factor (see Reference [2])
Board Weight	140 g
Environmental:	
Operating Temp:	0°- 50°C (at entry point of forced air)
Storage Temp:	-40° - +85°C
Humidity:	95% non-condensing
Cooling:	Approximately 200 LFM
Power consumption at 20 deg. C:	+5 V @ 2.5 A (model ICS-554C/E-w-MN(y) Rev.z) +5 V @ 1.8 A (model ICS-554C/E-w Rev.z) +3.3 V @ 1.1 A

Specifications subject to change without notice

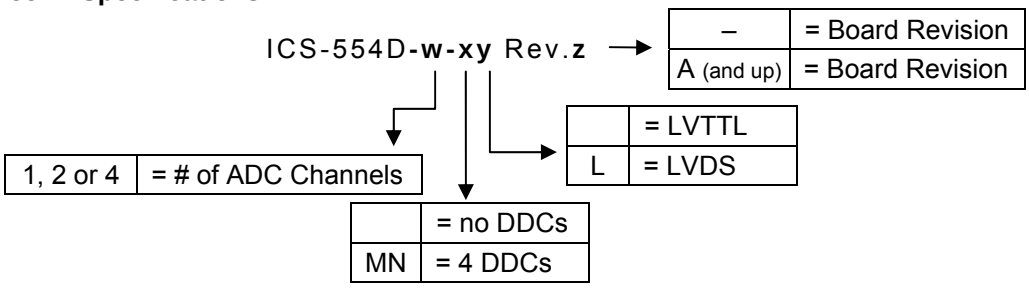
[1] The SFDR & SNR specification is set-up dependent. Please see Reference [9]. For best results ICS recommends the use of external clock.

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2.4 ICS-554D Specifications

Versions:



ANALOG INPUT	
Number of Analog Input Channels:	4 (Op-amp Coupled)
Analog Connector Type:	SMA Coaxial
Input Impedance:	50 Ohm
Full Scale Input:	Approx. 0.9 Volts peak-to-peak (+3 dBm) into 50 Ohms
Maximum Safe Input Voltage	± 5 Volts into 50 Ohms
Input Signal Bandwidth:	0 MHz – 50 MHz (-3 dB point)
Max. Sampling Rate:	105 MHz/ch. for 4 channels, simultaneous 100 MHz/ch. for 4 channels, simultaneous, when using DDCs
Min. Sample Rate:	30 MHz/ch. for 4 channels, simultaneous [1]
Internal Sampling Clock Oscillator	100 MHz fixed frequency
ADC Resolution:	14 bits
Sampling:	Rising edge of internal or external sample clock
External trigger:	Sampling occurs on rising edge of clock following rising or falling edge of external trigger (programmable). Trigger must remain high for at least one clock cycle.
Spurious Free Dynamic Range (SFDR):	>80 dB (at 100 MHz sampling, ignoring signal harmonics) [2]
Signal-to-Noise Ratio	> 67 dB (at 100 MHz sampling) [2]
Harmonic Distortion	<-72 dBc (single tone 1 dB below Full Scale)
On-board Storage:	1 MByte total
GENERAL	
PCI bus Interface:	PCI 2.2 64-bit 66 MHz, Master Burst Mode (DMA) capable Keyed for universal signaling
Optional Digital Downconverter (model ICS-554D-w-MN Rev.z):	Up to 4 wide band channels or 16 narrow band channels using 4 x Graychip GC4016
User I/O:	64 I/Os connected to User programmable FPGA
User Programmable FPGA:	3M gates Xilinx XC2V3000
Board Size	CMC single width form factor (see Reference [2])
Board Weight	140 g
Environmental:	
Operating Temp:	-0 to +50ºC
Storage Temp:	-40 to +85ºC
Humidity:	95% non-condensing
Cooling:	Approximately 200 LFM
Power:	+3.3 V @ 1.5 A +5 V @ 1.8 A (version ICS-554D-wy Rev.z) +5V @ 2.5 A (version ICS-554D-w-MNy Rev.z) +12 V @ 0.3 A , -12 V @ 0.3 A

Specifications subject to change without notice

[1] The specified minimum sample rate is 30 MHz. The product can be operated at sample rates down to 5 MHz, but the performance is not guaranteed in this case.

[2] The SFDR & SNR specification is set-up dependent. Please see Reference [9]. For best results ICS recommends the use of external clock.

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2.5 Cooling

It is essential that the user provides adequate cooling air to the ICS-554 when it is installed in the target system. It is not possible to design high performance, high density A/D and D/A converter products with very low power consumption requirements. Higher power requirements translate to a greater requirement for heat dissipation. Many PCI backplane/enclosure systems are not designed to provide a flow of cooling air to the boards. In some cases, a flow of air is provided through the case, but this may not directly cool the boards. In other situations, no cooling arrangements exist, apart from a fan in the power supply unit and a separate one for the CPU. The ideal cooling arrangement consists of a laminar flow of cooling air over each surface of the board, with the warm air being removed to the external environment. However, this may not be possible to achieve at all times. We recommend that the user consider the following approaches:

1. If using a PCI backplane/enclosure system, select one that has been designed to provide a laminar flow of cooling air to the boards.
2. If using a PCI backplane/enclosure system, use a "fan card" in a slot adjacent to the component side of the ICS-554.
3. If using a VME or cPCI backplane/enclosure system, use one that is generously designed with regard to the flow of cooling air, and use blanking plates in unused slots in order to ensure adequate flow of air to the ICS-554.

Examples of such products may be found at the websites listed in Reference [10] and [11].

2.6 Power

It is not possible to design high performance, high density A/D and D/A converter products with very low power consumption requirements. Many backplane/enclosure products do not measure or limit the power consumption of each PCI slot. However, some products are now taking this approach. When using a PCI backplane/enclosure/system, we therefore recommend that the user should verify that the selected product will supply adequate power to the ICS-554, with a generous margin to allow for a surge when power is applied, and for variation with temperature.

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3 FUNCTIONAL DESCRIPTION

3.1 ADC Section

The ICS-554 uses four 14-bit ADCs (AD6645), which sample synchronously at frequencies of up to 80/105 MHz using either a 80/100 MHz fixed frequency on-board oscillator or an external frequency source. The specified minimum sampling rate for the converters is 30 MHz, except for the ICS-554C and ICS-554E for which the minimum sampling frequency is 80 MHz. The ICS-554A, ICS-554B and ICS-554D will operate at sampling rates as low as 5 MHz, however, the signal/noise performance is not guaranteed in this case. The ICS-554 also provides programmable decimation of the ADC data stream by a factor of up to 32, making the effective minimum sampling rate 937.5 kHz. Decimation is accomplished by storing 1 out of every N samples where N is programmable from 1 to 32. Note that no filtering is performed prior to decimation when the optional DDC is bypassed. The full-scale input signal level is approximately 1.2 V peak-to-peak (+5.5 dBm) into 50 Ohms for the ICS-554A, ICS-554B, ICS-554C and ICS-554E. The full-scale input signal level is approximately 0.9 Vpp (+3 dBm) into 50 Ohms for the ICS-554D. The inputs to the converters are transformer coupled, except for the ICS-554D which is op-amp coupled. The transformers have a lower cut-off frequency of approximately 2 MHz and an upper cut-off frequency that exceeds the bandwidth of the converter part. Four SMA coaxial connectors (marked CH1, CH2, CH3, CH4) are provided on the front panel for connecting the single-ended analog input signals.

The outputs of the four ADCs are passed to the FPGA and to the digital demodulators (models ICS-554v-w-MN(y) Rev.z only). The selection of whether data is taken from the converters or from the DDC outputs is made within the FPGA. When ADC output is selected, the 14-bit converter samples are stored as 16-bit words within the 64Kx72-bit FIFO memories. On output, the data is presented as 2's complement (signed) 14-bit or 16-bit samples; these are justified to the most significant 14 bits of each 16-bit word, in the case of the 14-bit converter data. The standard FPGA firmware also stores the DDC output data as 32-bit values in the FIFO, when DDC output is selected, the data coming from DDC is presented as 2's complement (signed) 24-bit samples; these are justified to the most significant 24 bits of each 32-bit word.

The module may be configured to store data from a single ADC channel, from two channels or from all four channels. In any of these cases, the 14/16-bit data is packed so that the full capacity of the FIFO memories is used. The FIFO provides a bus matching feature so that data can be read out as 64-bit values at the maximum PCI 2.2 bus clock speed of 66 MHz regardless of the number of channels enabled. Thus, the ICS-554 can be operated continuously without data loss when one channel is enabled.

3.2 Clock, Trigger and Sync Options

The ICS-554 offers a number of options for selection of the clock, trigger and DDC synchronization signals.

The sampling clock may be either internal or external. The card has an internal crystal oscillator that provides a sample clock with a fixed frequency of 80 MHz for the ICS-554A-w-x Rev.z version, and 100 MHz for the ICS-554B-w-x Rev.z, ICS-554C-w-x Rev.z, ICS-554D-w-xy Rev.z and ICS-554E-w-xy Rev.z versions.

Both board jumper block J5 (see Section 5) and Control register 1 bit CR1<00> must be configured to select internal or external clock. When internal clock is selected, the clock signal is output to the front panel CLK connector. This enables it to be used to drive one or more other ICS-554 boards for synchronous sampling.

The internal sampling clock has sufficient power to drive a total of four boards.

When using an external clock, a signal of the desired frequency must be applied before configuring the board. The signal is connected via the front panel SMA connector marked CLK and is terminated on the board with a 50 Ohm resistive termination. When driving multiple boards, a power splitter should be used in order to maintain 50 Ohm characteristic impedance of all paths. The external clock signal must have a

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frequency that is within the operating range for that board type (see the Specifications in Section 2 above), and must be a continuous signal. It may be either a sinusoidal waveform with a level in the range –3 dBm to +6 dBm into 50 Ohms, or a signal with TTL levels and drive capability. The drive should not exceed +13 dBm (2.85 Vpp) to avoid possible damage to the board. Sampling occurs on the rising edge of the external clock.

Due to the nature of the PLL clock generation circuitry used for generation of clocks for some parts of the digital circuitry, care should be taken to ensure that the PLL is locked before the module is used. The user should therefore allow a delay of at least 10 microseconds after a stable clock signal has been supplied to the external clock input.

The trigger can also be programmed to be internal or external. Board jumper block J3 (see Section 5) must be configured to select internal or external trigger. Internal triggering is effected by writing to the Trigger register. The internal trigger signal is output to the front panel TRIG connector to allow triggering of one or more other ICS-554 boards.

The external trigger signal is connected at the front panel SMA TRIG connector, and may be programmed to be active on either the rising edge or falling edge using CR1<02>. Sampling starts on the first rising edge of clock following the active transition of the trigger signal. The signal must remain in the state following the active edge for at least one clock cycle. The external trigger signal input will accept a low voltage TTL input (3.3 V), but is tolerant of 5 V TTL signals. The signal must conform to standard TTL drive capability.

The trigger signal is not terminated on the board. It is recommended that a source series termination of 50 Ohms be used.

Synchronization of the Digital Downconverters (DDCs), if installed, can also be programmed to be internal or external. In multiple board configurations, one module must be configured as the master, the other module/s are slaves. The master module generates the DDC Sync signal and supplies it to the slave module/s by means of cables connected to the SYNC connectors. Board jumper block J4 (see Section 5) must be configured to select internal sync output on the master board and external sync input on the slave/s. For a single module, it must be configured for internal sync. The GC4016 Sync Mode registers must be programmed to generate Sync on the master module, and to receive it on the slave modules.

3.3 Channel Allocation

The ICS-554 provides the ability to select the number of channels to be used, under software control. From one to four channels may be selected. Table 3.1summarizes the operation of the module with different numbers of channels enabled. This includes the Control register bits that must be set to enable the channels, and the determination of which interrupts must be checked.

When one ADC channel is enabled, the ICS-554 stores the data from ADC channel 1 into FIFO 1. The maximum acquisition count is 256K samples. The other three channels are unused. When data is read over PCI Bus, only the data for channel 1 will be read.

When two ADC channels are enabled, the ICS-554 stores the data from ADC channel 1 into FIFO 1, and the data from ADC channel 3 into FIFO 2. The maximum acquisition count for either channel is 256K samples. The other two channels are unused. When data is read over PCI Bus, only the data for channels 1 and 3 will be read.

When three ADC channels are enabled, the ICS-554 stores the data from ADC channel 1 into FIFO 1, and the data from ADC channels 3 and 4 into FIFO 2. The maximum acquisition count for channel 1 is 256K samples, and for channels 3 and 4 is 128K samples each. Channel 2 is unused. When data is read over PCI Bus, only the data for channels 1, 3 and 4 will be read.

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When four ADC channels are enabled, the ICS-554 stores the data from ADC channels 1 and 2 into FIFO 1, and the data from ADC channels 3 and 4 into FIFO 2. The maximum acquisition count for each channel is 128K samples. When data is read over PCI Bus, data for all four channels will be read.

Table 3.1– ICS-554 ADC Channel Configuration Without DDCs

No. of Chans Enabled	ADCs Used	FIFO1 No. of Chans	FIFO2 No. of Chans	ADC1&2 Acq. Count	ADC3&4 Acq. Count	CR1<06> Enable12	CR1<07> Enable34	Check ADC1&2 Interrupt	Check ADC3&4 Interrupt
1	1	ONE	TWO	16 - 262143	0	Enable	Disable	YES	NO
2	1, 3	ONE	ONE	16 - 262143	16 - 262143	Enable	Enable	YES	YES
3	1, 3, 4	ONE	TWO	16 - 262143	16 - 131071	Enable	Enable	YES	YES
4	1, 2, 3, 4	TWO	TWO	16 - 131071	16 - 131071	Enable	Enable	YES	YES

Table 3.2– Data Output Format in FIFO1 (1 Channel Enabled Without DDCs)

Bit 63 48	Bit 47 32	Bit 31 16	Bit 15 0	Sequence
ADC1 Sample 1	ADC1 Sample 2	ADC1 Sample 3	ADC1 Sample 4	1
ADC1 Sample 5	ADC1 Sample 6	ADC1 Sample 7	ADC1 Sample 8	2
ADC1 Sample 9	ADC1 Sample 10	ADC1 Sample 11	ADC1 Sample 12	3
ADC1 Sample 13	ADC1 Sample 14	ADC1 Sample 15	ADC1 Sample 16	4
…	…	…	…	…
ADC1 Sample (AcqCount12 –3)	ADC1 Sample (AcqCount12 –2)	ADC1 Sample (AcqCount12 –1)	ADC1 Sample AcqCount12	AcqCount12/4

Table 3.3 – Data Output Format in FIFO2 (2 Channels Enabled Without DDCs)

Bit 63 48	Bit 47 32	Bit 31 16	Bit 15 0	Sequence
ADC3 Sample 1	ADC3 Sample 2	ADC3 Sample 3	ADC3 Sample 4	1
ADC3 Sample 5	ADC3 Sample 6	ADC3 Sample 7	ADC3 Sample 8	2
ADC3 Sample 9	ADC3 Sample 10	ADC3 Sample 11	ADC3 Sample 12	3
ADC3 Sample 13	ADC3 Sample 14	ADC3 Sample 15	ADC3 Sample 16	4
…	…	…	…	…
ADC3 Sample (AcqCount34 –3)	ADC3 Sample (AcqCount34 –2)	ADC3 Sample (AcqCount34 –1)	ADC3 Sample AcqCount34	AcqCount34/4

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Table 3.4 – Data Output Format in FIFO1 (4 Channels Enabled Without DDCs)

Bit 63 48	Bit 47 32	Bit 31 16	Bit 15 0	Sequence
ADC2 Sample 1	ADC1 Sample 1	ADC2 Sample 2	ADC1 Sample 2	1
ADC2 Sample 3	ADC1 Sample 3	ADC2 Sample 4	ADC1 Sample 4	2
ADC2 Sample 5	ADC1 Sample 5	ADC2 Sample 6	ADC1 Sample 6	3
ADC2 Sample 7	ADC1 Sample 7	ADC2 Sample 8	ADC1 Sample 8	4
…	…	…	…	…
ADC2 Sample (AcqCount12 –1)	ADC1 Sample (AcqCount12 –1)	ADC2 Sample AcqCount12	ADC1 Sample AcqCount12	AcqCount12/2

Table 3.5 – Data Output Format in FIFO2 (3 or 4 Channels Enabled Without DDCs)

Bit 63 48	Bit 47 32	Bit 31 16	Bit 15 0	Sequence
ADC4 Sample 1	ADC3 Sample 1	ADC4 Sample 2	ADC3 Sample 2	1
ADC4 Sample 3	ADC3 Sample 3	ADC4 Sample 4	ADC3 Sample 4	2
ADC4 Sample 5	ADC3 Sample 5	ADC4 Sample 6	ADC3 Sample 6	3
ADC4 Sample 7	ADC3 Sample 7	ADC4 Sample 8	ADC3 Sample 8	4
…	…	…	…	…
ADC4 Sample (AcqCount34 –1)	ADC3 Sample (AcqCount34 –1)	ADC4 Sample AcqCount34	ADC3 Sample AcqCount34	AcqCount34/2

The format of the output data varies depending on which of the optional Digital Downconverters (DDCs) is used, if any. The data, whether 14-bit or greater resolution, is provided as a 2's complement signed value justified to the most significant bits of each 16-bit part of the 64-bit word. For more information on DDC data Output Format, refer to Section 4.15.

3.4 Modes of Operation

Two modes of operation are provided by the ICS-554:

- Capture mode;
- Continuous mode.

In the Capture mode, data is acquired for a programmable number of samples following each application of the trigger. Because the size of the memory buffer and the count of samples acquired are both programmable, multiple capture acquisitions may be stored in the ICS-554 memory before data is read from the board. Note that when using Capture mode, the memory buffer length programmed must always be an integral number of acquisition counts. If enabled, an interrupt (ADC interrupt) will occur after the number of samples acquired is equal to the programmed buffer length. See Figure 3 below for more information.

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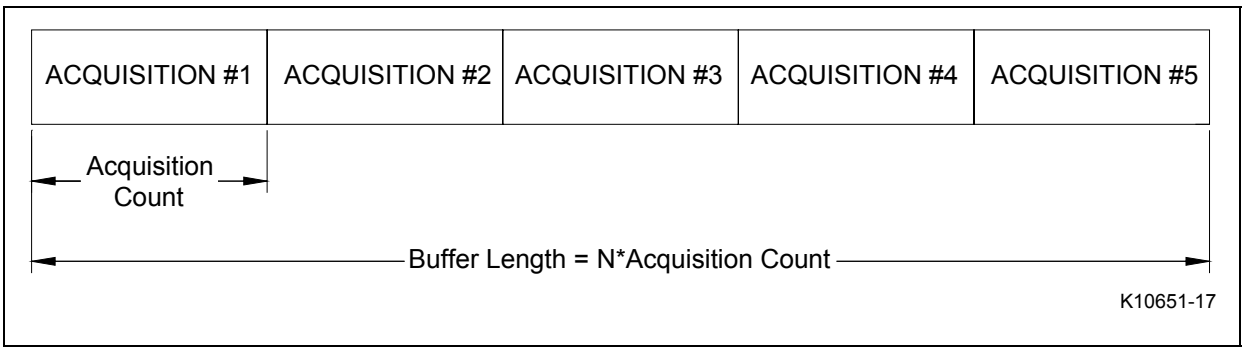


Figure 3 – Buffer Length as a Function of Acquisition Count

In the Continuous mode of operation, acquisition begins upon application of the trigger and continues until the board is disabled. If enabled, an interrupt (ADC interrupt) will occur each time the number of samples acquired since the trigger or since the last interrupt is equal to the programmed buffer length. The host processor must be capable of transferring data at a rate greater than or equal to the rate at which it is generated by the ADCs, or else data received by the host will not be continuous (see Table 3.6). The use of large programmed buffer lengths will help to ensure that data loss does not occur.

Table 3.6 – Data Transfer Speed in Continuous Mode (DDCs Disabled)

	ADCs Enabled	**FIFO1 Channel Mode**	**FIFO2 Channel Mode**	**Required Data Transfer Speed @ 80 MHz Sample Rate**	**Required Data Transfer Speed @ 105 MHz Sample Rate**	**PCI Mode**	**Theoretical Maximum PCI Burst Data Transfer Speed**
1 Channel Mode	1	ONE	TWO (disable)	160 MBytes/s	210 MBytes/s		
2 Channel Mode	1 and 3	ONE	ONE	320 MBytes/s	420 MBytes/s	32 bit/ 33 MHz	132 MBytes/s
3 Channel Mode	1, 3 and 4	ONE	TWO	480 MBytes/s	630 MBytes/s	64 bit/ 33 MHz	264 MBytes/s
4 Channel Mode	1, 2, 3 and 4	TWO	TWO	640 MBytes/s	840 MBytes/s	64 bit/ 66 MHz	528 MBytes/s

3.5 Digital Downconverters and FPGA

The ICS-554v-w-MN(y) Rev.z versions of the product include four Graychip GC4016 digital downconverter chips (DDCs). All versions of the product include a user-programmable Field Programmable Gate Array (FPGA). On the ICS-554A and ICS-554B, this is a Xilinx Virtex II XC2V1000, containing one million system gates. On the ICS-554C, ICS-554D and ICS-554E, the FPGA is a 3 million gate XC2V3000 part. Figure 1 illustrates how these parts are connected.

A description of the functionality of the DDCs is given in Section 4. Programming details are given in Section 6 and in the Graychip data sheet, Reference [5].

The ICS-554 is shipped with a data crossbar switch loaded in the FPGA. This enables the data input source for the FIFO memories to be selected as either the converter outputs or the GC4016 outputs, if installed. It also provides control over the data output format. It can be reprogrammed for other functions

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by the user. 95% of the logic slices of the one or three million gate part are still available for use by the user. Thirty-two 8-bit PCI Bus registers are allocated within the ICS-554 address map for access to the FPGA in the case that programmable functions need to be implemented.

In order to program the FPGA for user-defined functions, the user will need to purchase the ICS-554 Hardware Development Kit (HDK) and the necessary Xilinx tools. The ICS-554 HDK contains details of the FPGA connections, signal functions and timing diagrams as well as the VHDL source code design file and Constraints file for the default code included in the FPGA. A good understanding of the capabilities of the FPGA is required in order to be able to successfully reprogram the device. The required functionality will need to be coded in VHDL, simulated, compiled and loaded to the board by means of the JTAG port (P6) or via PCI bus.

3.6 Buffer Length

The buffer almost full length (number of samples acquired) at which an ADC interrupt will occur is independently programmable for each of the two FIFO memories. In Capture mode, an interrupt will occur when the programmed almost full level has been acquired; this may be as a result of more than one trigger, if the Acquisition Count has been programmed to be a sub-multiple of the buffer length. In Continuous mode, an interrupt will occur every time the total number of samples in the buffer reaches the programmed almost full level. The relationship between the programmed acquisition count and buffer length depends on the output data format, which depends on the operating mode used. This relationship is described in Section 6.10 below. The buffer length is programmed using the FIFO Level Control register. The value must be programmed serially, one bit at a time (see Section 6.14).

3.7 PCI Bus Interface

The ICS-554 implements a 64-bit, 66 MHz PCI bus Master/Slave interface compliant with the PCI 2.2 specification. It uses the QuickLogic QuickPCI™ QL5064 PCI Bus interface chip. The QL5064 includes a PCI core and a field-programmable gate array (FPGA). The PCI core implements the PCI protocol while the FPGA contains a controller for the ICS-554 local bus. This implementation enables the PCI bus and the internal local bus to operate at rates up to the full PCI bandwidth (528 MBytes/s). The ICS-554 uses the chain mode DMA channel in the QL5064 to read data from the ICS-554 memory.

At power on, the operating system must set the PCI base addresses for the board using the standard PCI configuration procedure.

The ICS-554 will operate in 64-bit mode and at 66 MHz clock speed on busses that support these options.

The ICS-554 accepts either 3.3 V or 5 V signaling, and is keyed in accordance with Reference [3].

The ICS-554 uses PCI interrupts to indicate buffer almost full (i.e. data available to be read), ADC over range, and DMA transfer completion. Three bits in the ICS-554 Interrupt Mask register allow the user to enable the interrupts for buffer almost full (ADC Interrupt) and ADC over range (Over range Interrupt). Corresponding bits in the Status register indicate the status of these conditions. A PCI interrupt will occur when one of the IMR bits is set and the condition occurs. The interrupt handler must then clear the corresponding IMR bit to prevent a further interrupt occurring. The ADC interrupt will occur, if enabled, when the number of samples acquired is equivalent to the value programmed to the Buffer Length register. In Continuous mode, the user must read data from the buffer in order to avoid data loss.

Target mode access to the ICS-554 Bus interface for transfer of data is not supported – the DMA engine on the board should always be used for data transfers.

Important note: The ICS-554 orders data in "little-endian" format, i.e. ascending byte address read from LSB to MSB of the data. For big-endian host systems, endian conversion can be enabled within the QL5064 chip.

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The programmable feature allows the user to select the type of endian conversion to be applied to data transferred from the ICS-554 to the PCI Bus. This conversion is applied to data transferred by single cycle bus transfers and by DMA transfers. However, when using the linked-list (chain memory, scatter-gather) DMA capability of the QL5064, the chain memory data is located on host memory and must be reordered by the user using the appropriate endian conversion when it is written. ICS-supplied software device drivers provide this conversion, except for that for Windows operating systems.

3.8 Cascading Multiple Boards

In common with other ICS products, the ICS-554 design provides simultaneous sampling not only on four channels on one board, but also on all channels across multiple boards. In order to achieve multiple board synchronization, one board is designated as the sampling master, while the other board/s is/are configured as slave board/s. An external sample clock must be used when simultaneous sampling is required across multiple boards; the user must supply the same clock signal to master and slave boards. The master board provides a trigger and timing signals to the slaves. All boards to be synchronized must be located in the same chassis in order not to violate signal timing requirements.

The ICS-554's clock circuitry allows multiple board systems to have simultaneous triggering (+/- 0 samples) and less than 1.5 ns board to board sampling skew.

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3.9 Light-Emitting Diodes

The ICS-554 is fitted with a set of light-emitting diodes (LEDs) which indicate board operation and error conditions. The diodes are located as shown in Figure 4 and Figure 5 for the B11608 board layout. The layout is indicated by a label on the board, and is also indicated by the positions of jumpers on the board (see Figure 8 and Figure 9 in Section 5). There are four LEDs installed in a line. Table 3.7 describes the ICS-554 LEDs.

Table 3.7 - Light Emitting Diodes

	LED Function	Color	Description
1.	PCI Access	Green	Illuminated at each valid PCI Bus access to ICS-554
2.	ADC Running	Green	Illuminated for each ADC sample acquired
3.	ADC Over Range	Red	Illuminated when a ADC over range condition occurs (resulting in over range analog input)
4.	FIFO Overflow	Red	Illuminates when the FIFO overflow condition occurs (resulting in lost data)

Note: The LED state is not latched, except for the ADC Over Range LED. Therefore, the illumination level may not be sufficient to be visible for intermittent events.

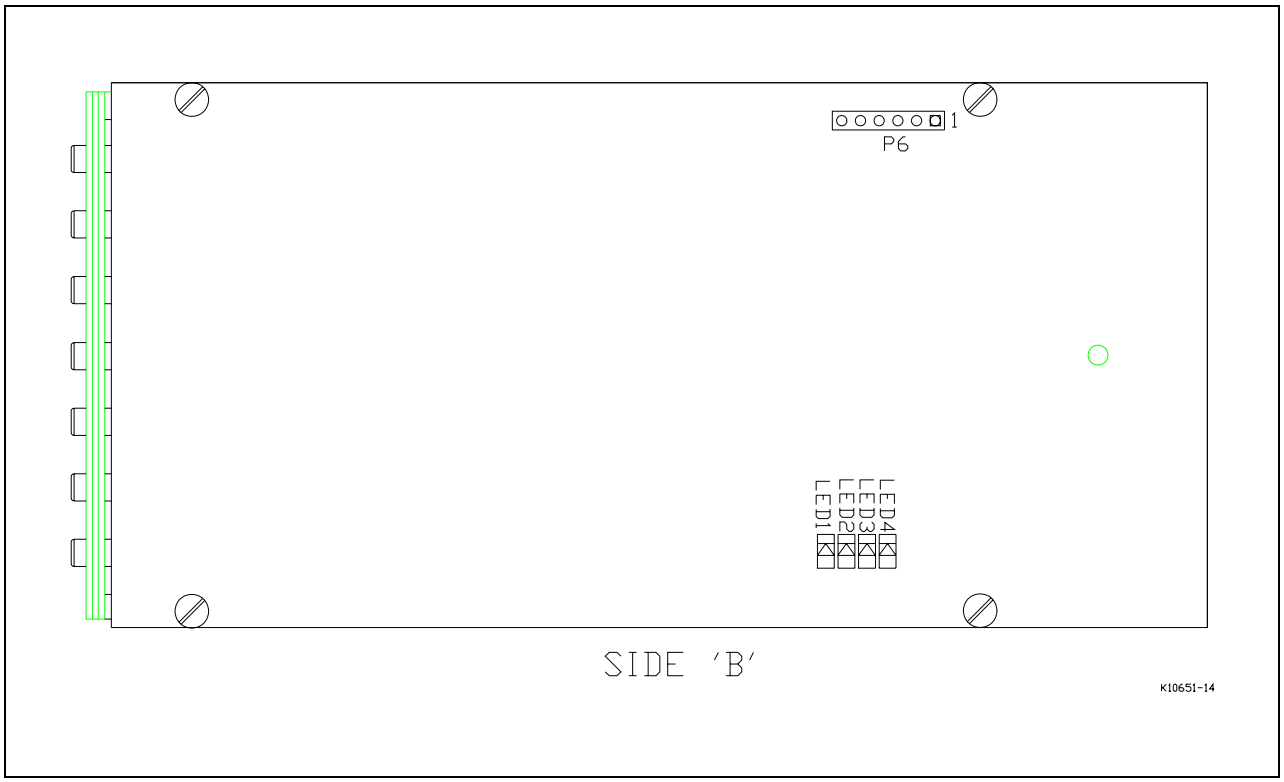


Figure 4 - Position of LEDs and JTAG Port (P6) on ICS-554 (All Board Layouts Other Than B11608)

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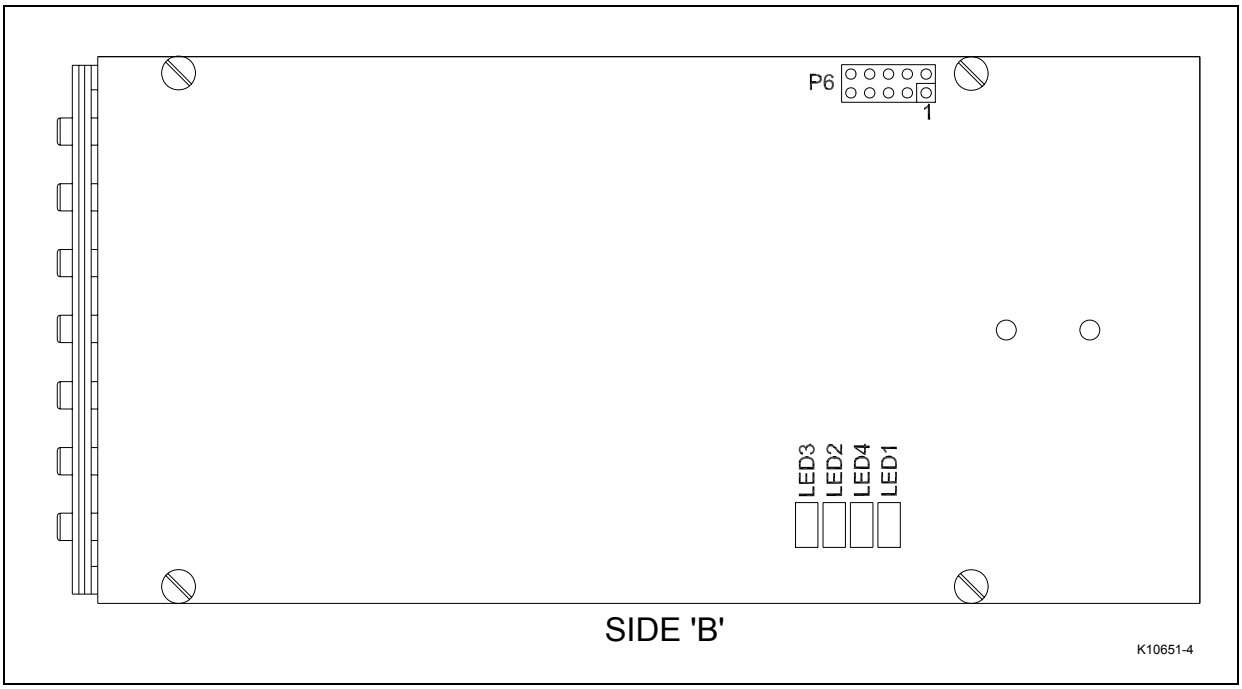


Figure 5- Position of LED Indicators and JTAG Port (P6) on ICS-554 (Board Layout B11608 Only)

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4 OPTIONAL DDC FUNCTIONAL DESCRIPTION

4.1 General Description

The user should consult the Graychip documentation for a complete description of the GC4016 product (see Reference [5]). This section provides an overview of the chip functionality and describes the data output formats available from the ICS-554.

The ICS-554v-w-MN(y) Rev.z versions of the product include up to four Graychip GC4016 Digital Down Converter (DDC) chips, each containing four identical down-conversion circuits, giving a total of up to 16 individual output channels. A block diagram of a single GC4016 device is shown in Figure 6.

The data inputs to each of the GC4016 chips consist of four independent 14-bit data buses from the ADC outputs, so that any of the output channels may use any of the A/D input channels as its data source. Each GC4016 output channel can be configured to select and downconvert a signal band from the input data stream centred on a specific input frequency (the IF or tuning frequency).

Each of the four identical down-converters on the DDC chip accepts a real sample rate up to 100 MHz, down-converts a selected IF frequency to zero, filters the signal, decimates the signal rate by a programmable factor ranging from 32 to 16,384 and then resamples the channel to adjust the sample rate up or down by an arbitrary factor. In the real output mode the output sample rate is doubled and the signal is output as a real signal centered at frequency Fout /4. The channels on a DDC may be combined to produce wider band and/or oversampled outputs or to process complex input data. The chip contains two user programmable output filters per path which can be used to arbitrarily shape the received data spectrum. These filters can be used as Nyquist receive filters for digital data transmission. The chip also contains a resampling filter to provide additional filtering and to allow the user complete flexibility in the selection of input and output sample rates.

Two downconverter paths can be merged to be used as a single complex input down-conversion circuit. Two paths may also be combined to support wider band output rates or oversampled outputs. Four paths may be combined to support both wider band output and oversampling. The downconverters are designed to maintain over 115 dB of spur free dynamic range and over 100 dB of out of band rejection. A five stage CIC and 20 bit internal data paths support this high dynamic range digital signal processing requirement. Each downconvert circuit accepts 14-bit inputs and produces 24-bit outputs. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the decimation and filter parameters of each circuit.

Groups of DDC output channels that feed into the same FIFO memory, i.e. the upper or lower 8 downconverter channels must use the same bandwidth (i.e. same decimation factor). Thus the upper 8 downconverter channels may use a different bandwidth than the lower 8 downconvertor channels. Each channel can be programmed independently for filter coefficients and input selection, centre (IF) frequency, phase and gain. Each downconverter channel contains three filters in sequence to lowpass filter and isolate the downconverted signal(s). Users have the option to download filter coefficient sets provided by ICS with the software device drivers for the ICS-554, or to use their own custom filter coefficients.

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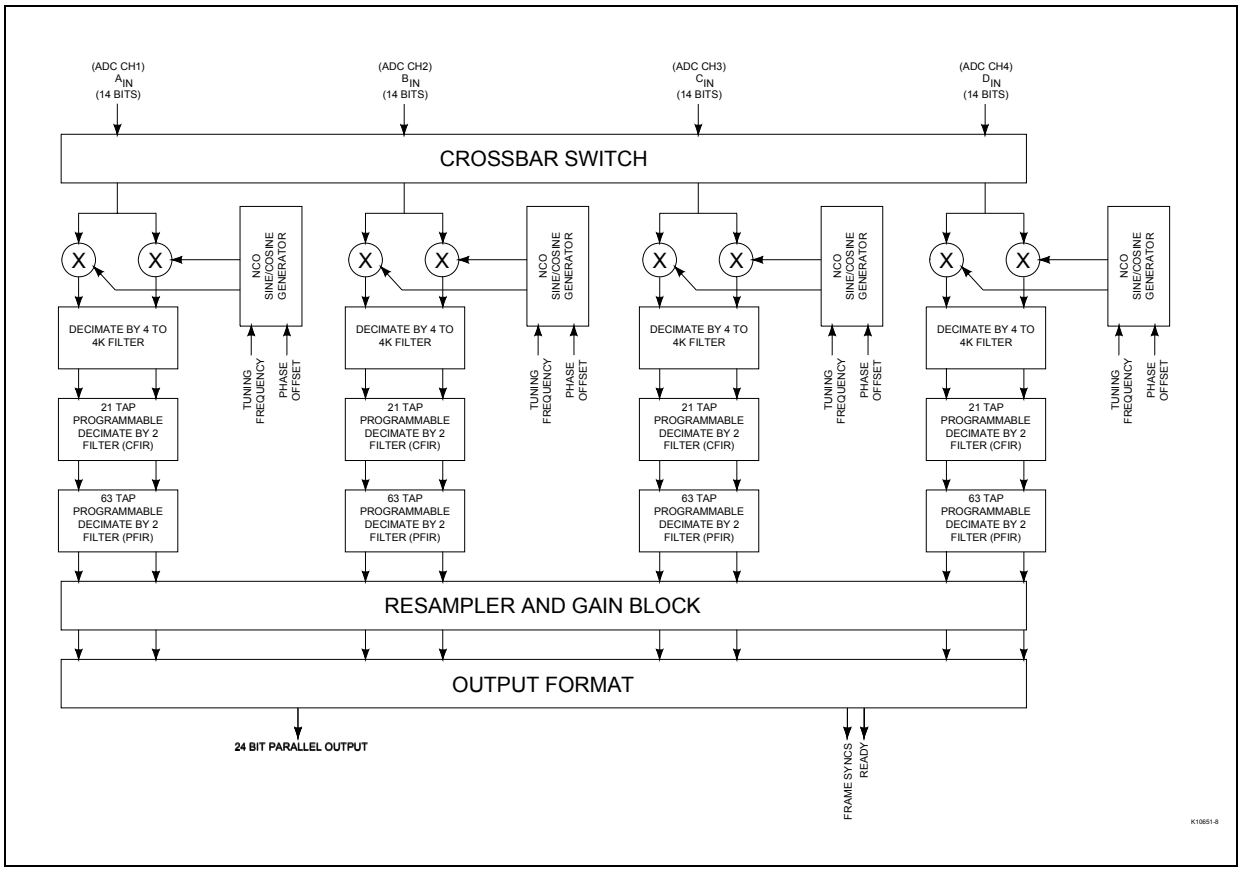


Figure 6 – GC4016 Block Diagram

4.2 Channel Configuration

The maximum signal bandwidth that can be processed by a single channel is dependant upon the clock frequency, the decimation ratio and the type of filter, or the filter coefficients. By combining channels, the signal bandwidth can be increased, as described below. The GC4016 provides a number of options for combining channels and converting the standard complex data output format to real data.

The DDCs in the Graychips contain multichannel mode functionality. The maximum single channel output bandwidth is approximately 2.5 MHz. This output bandwidth can be doubled by combining two channels using the Split-I/Q mode. Four channels may be combined to provide three to four times the single channel output bandwidth. Two channels can be combined to process complex input data, doubling the input bandwidth. Four channels can be combined to both process complex input data and to double the output bandwidth of the chip. Two or four multichannel modes may also be used in the complex to real mode.

Table 4.1 gives a summary of the channel output formats for each GC4016 mode. DDC output data formats are given in Section 4.15. A detailed description of the Channel Count register programming is given in Section 6.18. Please see Reference [5] for more information on GC4016 functionality.

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Table 4.1 – Number of Channels for Each FIFO

DDC Mode	Number of Channels in each FIFO
Narrowband complex output	1,2,3,4,5,6,7,8
Narrowband real output	2,4,6,8
Split-I/Q complex output	2,4
Split-I/Q real output	2,4
Wideband complex output	1,2
Wideband real output	1,2
Narrowband pairs of complex input & complex output	2,4
Narrowband pairs of complex input & real output	2,4
Split-I/Q complex input & complex output	1,2
Split-I/Q complex input & real output	1,2

4.3 Detailed Description

Figure 7 illustrates the structure of a single downconverter channel; there are four such downconverters in each of the four DDC chips. A Numerically Controlled Oscillator (NCO) and mixer are used to quadrature downconvert a signal from the tuning frequency to baseband. The tuning frequency is specified as a 32-bit word and the phase as a 16-bit word. The tuning word TW is based on the formula $TW=2^{32} \times F/Fck$ where F is the desired tuning frequency and Fck is the input data rate (programmed ADC sampling frequency).

A positive tuning frequency is normally used to downconvert the signal; however, a negative tuning frequency can be used to invert the output spectrum. Phase is set according to the following formula: $PH=2^{16} \times P/(2\pi)$, where P specifies the desired phase in radians between 0 and 2π. The spur level of the NCO can be reduced when dithering is turned on, resulting in a significant improvement in SFDR of the output.

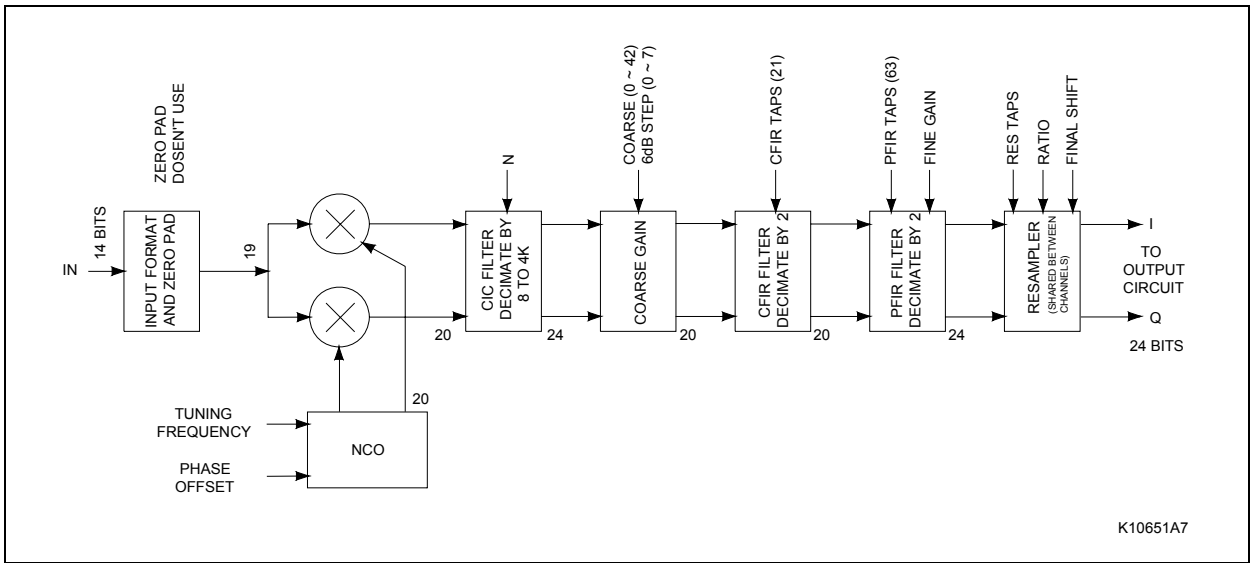


Figure 7 – GC4016 Block Diagram (Single Channel)

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4.4 Input CrossBar

The crossbar switch allows the user to route any input source to any downconverter channel.

4.5 Input Scaling and CIC Filter

The CIC filter decimates the inputs from the NCO by a factor of N, where N is from 8 to 4K, and has a gain equal to N^5. The inputs have to be scaled before this filter to prevent overflow. This scaling is done in the shift down block indicated in Figure 7.

The shift down circuit has a gain equal to:

$$2^{(SHIFT+SCALE+6xBIG_SCALE-62)},$$

where the values for SHIFT, SCALE and BIG_SCALE are set in the Channel Reset and CIC Scale register and are common for all channels of the module. The overall gain of the shift down and CIC filter is given by the following formula:

$$GAIN = N^5 * 2^{(SHIFT+SCALE+6xBIG_SCALE-62)}$$

The user must select the values for SHIFT, SCALE and BIG_SCALE such that the overall gain (GAIN) is less than or equal one. Therefore (SHIFT+SCALE+6xBIG_SCALE) has to be less than or equal to (62-5xlog2(N)) otherwise the resulting overflow will go undetected.

4.6 Coarse Gain

Coarse gain is set for each channel in the CFIR register (bits 4-6) and it can be used to boost the channel's gain by up to 42 dB. This is accomplished by shifting up the output of the CIC filter by 0 to 7 bits before rounding to 24 bits. The coarse gain is equal to 2^{COARSE}, where COARSE is the 3 register bits mentioned above. It is not recommended to change the coarse gain. See Section 4.10 for a description of the effect of this register on the overall gain of the chip.

4.7 Compensating FIR Filter

The output of the coarse gain circuit is filtered in the CFIR filter stage. This stage is a 21-tap decimate by 2 filter with programmable 16-bit coefficients. Since this filter decimates by two, a stopband must be created in that portion of the spectrum that would alias into the signal of interest. This filter has very lax transition band specifications, therefore, 21 taps is sufficient to both provide the required anti-aliasing stopband, and to provide compensation for the droop in the CIC filter's passband. The CFIR is also used, in some cases, to provide additional stopband rejection for the second stage PFIR filter.

The user downloaded filter coefficients are 16-bit 2's complement numbers. Unity gain will be achieved through the filter if the sum of the 21 coefficients is equal to 65536. If the sum is not 65536, then CFIR will introduce a gain equal to: CFIR_GAIN = CFIR_SUM/65536, where CFIR_SUM is the sum of the 21 coefficients.

The 21 coefficients are identified as coefficients h0 through h20, where h10 is the center tap. The coefficients are assumed to be symmetric, so only the first 11 coefficients (h0 through h10) are loaded into the chip. A non-symmetric mode (NO_SYM_CFIR) allows the user to download an 21-tap non-symmetric filter as taps h0 through h20. The newest sample is multiplied by h0 and the oldest is multiplied by h10. NOTE: Filters normally multiply h0 by the oldest data, hence one may wish to reverse the tap order in the non-symmetric mode.

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The CFIR has a programmable delay of one CFIR input sample. This delay is used in a multichannel mode to alter the decimation-by-two phasing in order to generate oversampled or wider bandwidth output data. This delay is independently programmable for each channel and is also independent for I and Q (QDLY_CFIR and IDLY_CFIR). A special mode (Split-I/Q) is also available where the CFIR generates two I outputs rather than one I and one Q.

Table 4.2 describes the CFIR coefficient sets included with ICS software device drivers. Users can also design their own CFIR coefficient sets and download them to the GC4016 chips. Note that ICS supplied device drivers compensate for the varying CFIR gain in the final gain stage to within ±0.5 dB.

Table 4.2 - CFIR Coefficient Sets Included with ICS Device Drivers

Filter type	Descriptions	CFIR_GAIN (dB)
CFIR_80	80% usable output bandwidth (default setting)	-0.0882
CFIR_17	17% usable output bandwidth	6.1981
CFIR_34	34% usable output bandwidth	3.7668
CFIR_68	68% usable output bandwidth	2.0521
CFIR_100	100% usable output bandwidth	-0.8106
CFIR_150	150% usable output bandwidth (used for Wideband converter mode)	-0.7679
CFIR_GSM	GSM usable output bandwidth	-0.0001
CFIR_is95	IS-95 (NB-CDMA) usable output bandwidth	5.4309
CFIR_UMTS	UMTS (WB-CDMA) usable output bandwidth	-0.9381
CFIR_4014	GC4014 usable output bandwidth	-0.0012

4.8 Programmable FIR Filter

The second stage decimate by two filter is a 63-tap decimate-by-2 filter with programmable 16-bit coefficients. Fine gain is applied at the output of the PFIR and rounded to 24 bits. Overflows are detected and hard limited. Overflows can be directed to the channel overflow detection block. The PFIR filter passband must be flat in the region of the signal of interest, and have the desired out of band rejection in the region that will alias into the signal's bandwidth after decimation. The externally downloaded coefficients can be used to tailor the spectral response to the user's needs. For example, it can be programmed as a Nyquist (typically a root-raised-cosine) filter for matched filtering of digital data. The user downloaded filter coefficients are 16 bit 2's complement numbers. Unity gain will be achieved through the filter if the sum of the 63 coefficients is equal to 65536. If the sum is not 65536, then PFIR will introduce a gain equal to: PFIR_GAIN = PFIR_SUM/65536, where PFIR_SUM is the sum of the 63 coefficients.

The 63 coefficients are identified as coefficients h0 through h62, where h31 is the center tap. The coefficients are assumed to be symmetric, so only the first 32 coefficients (h0 through h31) are loaded into the chip. A non-symmetric mode (NO_SYM_PFIR) allows the user to download a 63 tap non-symmetric filter as taps h0 through h62. The newest sample is multiplied by h0 and the oldest is multiplied by h31. NOTE: Filters normally multiply h0 by the oldest data; hence one may wish to reverse the tap order in the non-symmetric mode.

PFIR also contains a one PFIR sample input delay that is independently programmable for the I and Q paths and for the four channels (QDLY_PFIR and IDLY_PFIR). The delay is used when combining channels to allow wider output bandwidth and/or more oversampling. It is also used for complex to real conversion in PFIR.

A fine gain is applied to the data after filtering and negation. The fine gain is a positive 14-bit integer (FINE) ranging from 0 to 16383. Fine gain is equal to: FINE_GAIN = FINE/1024. Setting FINE to zero will clear the channel.

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Table 4.3 describes the PFIR coefficient sets included with ICS software device drivers. Users can also design their own PFIR coefficient sets and download them to the GC4016 chips. Note that ICS supplied device drivers compensate for the varying PFIR gain in the final gain stage to within ±0.5 dB.

Table 4.3 - PFIR Coefficient Sets included with ICS Device Drivers

Filter type	Description	PFIR_GAIN (dB)
PFIR_80	80% usable output bandwidth (default setting)	1.2094
PFIR_17	17% usable output bandwidth	9.9003
PFIR_34	34% usable output bandwidth	6.9933
PFIR_68	68% usable output bandwidth	1.6844
PFIR_100	100% usable output bandwidth	-0.7346
PFIR_150	150% usable output bandwidth (used for Wideband converter mode)	-3.9857
PFIR_GSM	GSM usable output bandwidth	3.3409
PFIR_is95	IS-95 (NB-CDMA) usable output bandwidth	2.6945
PFIR_UMTS	UMTS (WB-CDMA) usable output bandwidth	-0.5069
PFIR_UMTS_24x	UMTS (WB-CDMA) usable output bandwidth	3.0149
PFIR_DAMPS	IS-136 DAMPS usable output bandwidth	5.2095

4.9 Resampler

The resampler will independently filter and change the data rate of each channel. The most common application of the resampler is to increase the sample rate of the data so that it will match a desired symbol or bit rate. Demodulators for digital modulation schemes, such as GMSK, QPSK, QAM or CDMA, for example, require sample rates which are 1X, 2X, 4X or 8X times the bit or symbol rate of the modulation. In these cases, the maximum down converter filter performance is achieved when the PFIR output rate is around 1.5 to 2 times the signal's bandwidth. The resampler is then used to increase the sample rate up to the required 2X, 4X or 8X rate. The resampler can also be used as an additional filter to optimize the passband or stopband response of the channel.

An application example that uses the resampler is included with those supplied with ICS software drivers. For more information about resampler functionality, see the GC4016 datasheet, Reference [5].

4.10 Optimal Gain Settings

The overall gain of each downconverter chip consists of the product of the CIC gain, coarse gain, CFIR gain, PFIR gain, final gain, resampler gain and final shift gain. The following is a summary of the contributions to the overall gain of each channel:

$$GAIN = \{N^{5}2^{(SHIFT+SCALE+6*BIG_SCALE-62)}\}(2^{COARSE})(\frac{CFIR_SUM}{65536})(\frac{PFIR_SUM}{65536})(\frac{FINE_GAIN}{65536})(\frac{RES_SUM}{32768*NDELAY})(2^{FINAL_SHIFT})$$

or

$$GAIN(dB) = 20*\lg(N^{5}2^{(SHIFT+SCALE+6*BIG_SCALE-62)}) +$$
$$20*\lg(2^{COARSE}) + 20*\lg(\frac{CFIR_SUM}{65536}) + 20*\lg(\frac{PFIR_SUM}{65536}) + 20*\lg(\frac{RES_SUM}{32768*NDELAY}) + 20*\lg(2^{FINAL_SHIFT});$$

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CIC gain = $N^5 \times 2^{(SHIFT+SCALE+6*BIG_SCALE-62)}$
This is the gain up to and including the CIC filter and is described in Section 4.5 above. This gain setting can be different to all 16 channels of the DDC chip.
Coarse Gain = 2^{COARSE}
This component is unique to each channel; it is described in Section 4.6 above.

CFIR Gain = CFIR_SUM/65536
This is the gain introduced by the user-downloadable filter taps if their sum is not 65536.

PFIR Gain = PFIR_SUM/65536
This is the gain introduced by the user-downloadable filter taps if their sum is not 65536.

Fine Gain = FINE_GAIN/1024
The default setting of FINE_GAIN is Fine_Gain = 1024 which gives a gain of 0.0 dB. The adjustable range of Fine Gain is from -60.206 dB to 24.0819 dB (from 1 to 16384). It is recommended to change this value to match input and output gain.

Resampler Gain = RES_SUM/(32768*NDELAY)
Final Shift Gain = 2^{FINAL_SHIFT}
If bypassing the resampler and if Final Shift = 5, (resampler gain + Final Shift gain) should be set to unity in the gain equation. For more information, refer to the GC4016 datasheet, Reference [5].

The signal data flows through these gain sections in the order given above. To optimize the dynamic range of the chip, each of these gain stages should be sest so as to maximize the signal amplitude without clipping. Another factor that has to be taken into consideration is the tuning loss; this effectively halves the input amplitude. The tuning loss occurs after the CIC filter. To compensate for this loss, the product of the individual gain stages after the CIC filter should equal 2 for optimal performance.

4.11 DDC Module Configurations

Each GC4016 chip contains four independent channels and each channel can output complex data at sample rates up to Fck/32. Depending on the filter coefficients and the clock rate, the maximum single channel output bandwidth is just under 2 MHz. This output bandwidth can be doubled by combining two channels using the Split-I/Q mode. Four channels may be combined to provide 3 to 4 times the single channel output bandwidth (with reduced out of band rejection). The two or four multi-channel modes may also be used in the complex-to-real mode. Two channels can also be combined to process complex input data, thereby doubling the input bandwidth going into the chip. Four channels can be combined to both process complex input data and to double the output bandwidth of the chip.

4.11.1 16-Channel Narrow Band Configuration

Since each GC4016 chip contains four downconverter paths, the ICS-554v-w-MN(y) Rev.z can be configured for up to 16 downconverter channels in this mode. Each downconverter channel has individual input selection, tuning frequency, tuning phase, CFIR coefficients, PFIR coefficients and gain settings. The decimation of each channel is from 32 to 16384 and CIC decimation factor is from 8 to 4096. The outputs are normally complex sample pairs. Double rate real output can also be generated by using complex to real conversion. The outputs of the upper 8 channels are transferred into FIFO1, while the outputs of the lower 8 channels are transferred into FIFO2. The output data format for complex data is as shown in Table 4.4 in Section 4.15. Table 4.5 shows the data organization for real output.

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4.11.2 8-Channel Split-I/Q Configuration

Two channels work together in the Split-I/Q mode to double the output bandwidth of the downconverter. In the Split-I/Q mode, the real half of the complex output data is processed in one channel and the imaginary half in the other. The CIC has a minimum decimation of 4 instead of 8, which allows channel output at sample rates up to Fck/16. The two channels being combined in the Split-I/Q mode should be programmed identically, including the tuning frequency, except that the imaginary channel should have a +90 degree phase shift. The IONLY bit in the real channel should be set and the QONLY bit in the imaginary channel should be set. The decimation of each channel is from 16 to 8192 and CIC decimation factor is from 4 to 2048.

Typically the chip is configured in the Split-I/Q mode so that channels A and B are combined as one downconverter and C and D are combined as the other. Double rate real output can be generated by combining Split-I/Q and complex to real conversion. Note: in Split-I/Q and real output mode, the minimal CIC decimation factor is 5, while the minimal CIC decimation factor is 4 in Split-I/Q and complex output mode.

The ICS-554v-w-MN(y) Rev.z provides up to 8 Split-I/Q downconverter channels. The outputs of the upper 4 channels are transferred into FIFO1, while the outputs of the lower 4 channels are transferred into FIFO2. The output data format for complex data is as shown in Table 4.6 in Section 4.15. Table 4.7 shows the data organization for real output.

4.11.3 4-Channel Wideband Configuration

Even wider output bandwidth is possible than is available using the modes described previously, by combining all four channels of a DDC. This is done by noticing that PFIR decimates the signal by two. If one pair of channels in the Split-I/Q mode are used to generate even time sample outputs and the other pair are used to generate odd time sample outputs, then the PFIR filter effectively does not decimate the signal. This allows a wider bandwidth filter to be used in the CFIR and PFIR. Adjacent channel rejection, however, will be reduced due to the increase in the output bandwidth relative to the CICs stopbands. Also the increase in output bandwidth makes it harder for the CFIR and PFIR to achieve deep stop bands. The wide output mode uses the chip in the Split-I/Q mode. In addition the QDLY_PFIR bits are set in channels A and B. The delay of one input sample into the PFIR will offset the decimate by two operation so that the channel A and B outputs are the real and imaginary parts of the even time samples and the C and D outputs are the real and imaginary parts of the odd time samples. Double rate real output can be generated by combining wideband and complex to real conversion. The decimation of each channel is from 8 to 4094 and CIC decimation factor is from 4 to 2048. Note: in wideband and real output mode, the minimal CIC decimation factor is 5, while the minimal CIC decimation factor is 4 in wideband and complex output mode.

The ICS-554v-w-MN(y) Rev.z provides up to 4 wideband downconverter channels. The outputs of the upper 2 channels are transferred into FIFO1, while the outputs of the lower 2 channels are transferred into FIFO2. The output data format is as shown in Table 4.8 in Section 4.15 for complex data. Table 4.9 shows the data organization for real output.

4.11.4 8-Channel Complex Input Configuration

Complex input data can be processed using two channels. The real portion of the input (I_{IN}) is processed in one channel while the imaginary portion (Q_{IN}) is processed in the next channel. Channels A and B are described here, channels C and D can be combined as well. The desired mixer output is $I_{out} = (I_{IN}*\cos - Q_{IN}*\sin)$ and $Q_{out} = (I_{IN}*\sin + Q_{IN}*\cos)$. Channel A is used in the normal mode and will output ($I_{IN}*\cos$) and ($I_{IN}*\sin$). A 90 degree offset in channel B will cause channel B to output ($-Q_{IN}*\sin$) and ($Q_{IN}*\cos$). The desired result is achieved by adding the channel A outputs to the channel B outputs. The complex to real mode can be used in conjunction with the complex input mode. If both channels are configured as

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described, then the combined complex input downconverter will be in the complex to real mode. The decimation of each channel is from 32 to 16384 and CIC decimation factor is from 8 to 4096.

The ICS-554v-w-MN(y) Rev.z provides up to 8 pairs of complex input channels. The outputs of the upper 4 channels are transferred into FIFO1, while the outputs of the lower 4 channels are transferred into FIFO2. The output data format is same as for the 8-channel Split-I/Q mode, shown in Table 4.6 for complex output and Table 4.7 for real output.

4.11.5 4-Channel Complex Input with Split-I/Q Configuration

The complex input and Split-I/Q modes can be combined. In this mode, channels A and D of each chip process the (I_{IN}) inputs, while channels B and C process the (Q_{IN}) input data. Channel A will output (I_{IN} *cos) and channel B will output ($-Q_{IN}$*sin), if its phase is set to 90 degrees. Channel C will output (Q_{IN}*cos) and channel D will output(I_{IN} *sin) if its phase is set to -90 degrees. The I_{out} output is formed by adding channel A to channel B, and the Q_{OUT} output is formed by adding channel C to channel D. The IONLY bits must be set for channels A and B, and the QONLY bits must be set for channels C and D. The complex to real mode can be added to this mode by delaying the I word by half (set QDLY_PFIR in channels A and B) and mixing by Fs/4. The decimation of each channel is from 16 to 8192 and the CIC decimation factor is from 4 to 2048. Note: When real output is selected in this mode, the minimum CIC decimation factor is 5, while the minimum CIC decimation factor for complex output is 4.

The ICS-554v-w-MN(y) Rev.z provides up to 4 Complex input channel pairs. The outputs of the upper 2 channels are transferred into FIFO1, while the outputs of the lower 2 channels are transferred into FIFO2. The output data format is the same as for the 4-Channel Wideband mode shown in Table 4.8 for complex output and Table 4.9 for real output.

4.12 DDC Decimation Setting

The total decimation through each GC4016 channel is the product of the CIC, CFIR and PFIR decimations. The CIC decimation ratio is programmable (=N), while the CFIR decimation is fixed at 2, and the PFIR decimation is either 2 or 1, depending on whether complex or real output is selected. The decimation is therefore equal to 4N for complex output, or 2N for real output. The output rate, and therefore the decimation, must be the same for all channels feeding the same FIFO; therefore the programmed decimation must be same for DDC chips 1 and 2, and must be the same for DDC chips 3 and 4.

For a given bandwidth, the decimation factor should be as high as possible in order to avoid undesired frequency components within the passband. This is because the cut-off frequency of the low-pass filters is a function of the decimated output rate. The decimation should always be computed in relation to complex output data (output rate > bandwidth), bearing in mind that the output rate is doubled for real data.

The decimation (D) must be chosen according to the bandwidth (B) of interest:

$$D = INT [Fs/B]$$

and $D = 4N$

For complex output data, the output rate is given as follows:

$$Fo = Fs/D$$
$$= Fs/4N$$

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and the output signal bandwidth is Fo.

For real output data, the output rate is given as follows:

Fo = Fs/D
= Fs/2N

and the output signal bandwidth is Fo/2.

Example:

Assume that the downconverters are clocked at 64 MHz and the decimation value is set to 16 in the CIC Decimation register of each chip. This gives a decimation factor of 64 overall, assuming the PFIR filter stage is set to decimate by 2 (complex output data). The CIC Decimation register must be set to D-1, in this case 15 for a decimation of 16. (This is automatically done if the ICS device driver is used). Also assume that the signal of interest is centered at 30 MHz and the aim is to tune to this signal.

With this tuning frequency the tuning word is equal to:

2^{32} x 30 MHz/64 MHz = 4,294,967,296 = 0x78000000

The 2's complement of this value (0x88000000) is loaded into the channels' frequency registers. The decimated output sample rate is 64 MHz/64 = 1 MHz. Assuming an 80% filter, the bandwidth is 1 MHz and usable bandwidth is 800 kHz. The complex output spectrum extends from –400 kHz to +400 kHz and it is represented as a sequence of I and Q sample pairs.
If real mode is selected with the same value programmed to the CIC Decimation register, the overall decimation will be 32. The output sample rate is 2 MHz.

The output spectrum (real) is now centered on 500kHz and extends from 100 kHz to 900 kHz. The output data consists of a sequence of I samples.

4.13 DDC Synchronization

All four GC4016 downconverter circuits must be synchronized for changes in decimation. Tuning frequency, phase, CFIR, PFIR and gain are also synchronized. This is accomplished by generating a sync pulse on one of the chips, and receiving it on the other three. Two registers must be correctly programmed to achieve this, the General Sync register and the Count Sync register.

The ICS-554v-w-MN(y) Rev.z requires that downconverter chip 1 is used to generate sync. Chips 1, 2, 3 and 4 must be programmed to receive sync from chip 1. The correct programming of the General Sync register and the Count Sync register is described in the section relating to those registers.

The design of the ICS-554 also allows synchronization of DDCs on multiple modules. Cable/s must be connected between the Sync connectors of the modules to achieve this, and the modules must be configured as master/slave configuration, as described in Sections 5 and 6 below.

4.14 DDC Module Output Spectrum

The organization of the DDC module output spectrum depends on the output mode, real or complex and on whether the tuning frequency is entered as a positive or negative number.

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In Figure 6, the sampling frequency is represented as Fs and the tuning or centre frequency as F_T. The output rate will be:

Fo = Fs/Decimation,

where Decimation is the overall decimation of the downconverter.

In complex output mode, the tuning frequency, F_T, is translated to zero frequency at the output, and either the upper or lower sideband is located on the positive side of the frequency axis, depending on whether a negative or positive tuning frequency is programmed. The other sideband is present on the positive frequency axis, located above half the output frequency.
In real output mode, F_T is translated to F_C, where:

$F_C = 0.25Fo$

and the spectrum is centered on this frequency. It is either inverted or in original orientation depending on whether a positive or negative tuning frequency is programmed.

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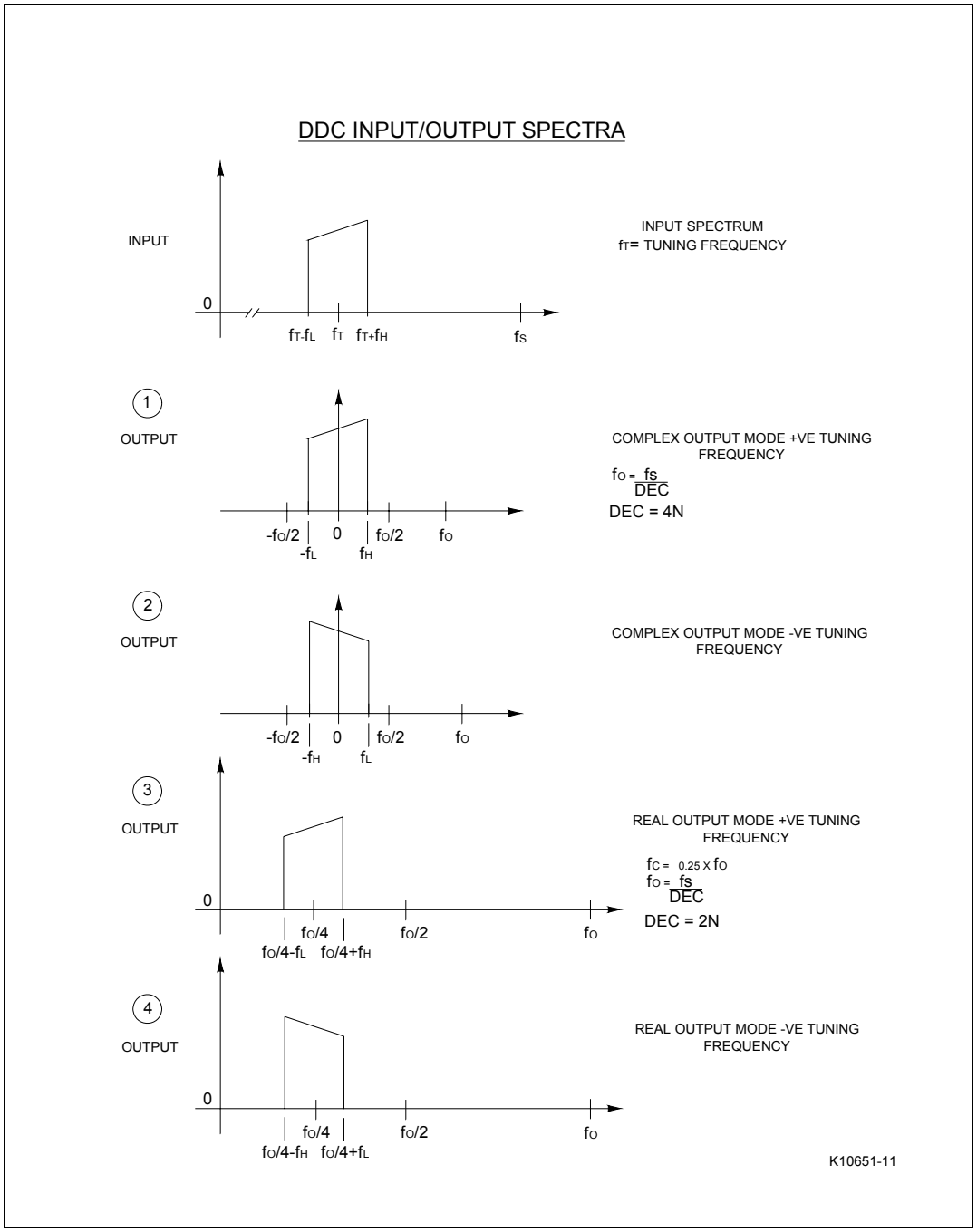


Figure 6 – ICS-554v-w-MN(y) Rev.z DDC Output Spectra

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4.15 DDC Data Output Format

The DDC output data is 24-bit 2's complement data. It is justified to the most significant 24 bits of each 32-bit part of the 64-bit PCI Bus word. The least significant eight bits of each 32-bit part are all set to ones.

The format of the data output varies depending on the GC4016 mode of operation, with regard to complex or real output data, mode of DDC operation (Narrow band, Split-I/Q, etc.) and number of output channels selected.

The following tables show the data format for FIFO 1, when N DDC channels have been selected for output in the Channel Count register (see Section 6.18). Data is generated in frames, where a frame contains a defined format of samples from each active DDC channel (sometimes one sample for each channel, sometimes more than one sample). The number of output channels that can be selected depend on the mode of operation (Narrow band, Split-I/Q or Wide band); each table shows the output format for the maximum number of channels available in that mode. The number of channels supported in that mode is given beneath each table. When less than the maximum number is selected, channels are dropped from the end of the frame (i.e. the Chip 2 Channel D frame is the first to be dropped when selecting 7 channels rather than the maximum 8, in Narrow band mode).

The format for FIFO 2 is identical, except that data for GC4016 chips 3 and 4 will be contained there. Since the output for a single FIFO is shown, the number of channels available when using both FIFOs is twice this number.

Table 4.4 – ICS-554v-w-MN(y) Rev.z Data Output Format, N Complex Narrow Band Channels/FIFO

64-bit PCI Bus Word				Frame No.	Sequence
63 40	39 32	31 8	7 0		
Chip 1 Chan A I1	11111111	Chip 1 Chan A Q1	11111111	1	1
Chip 1 Chan B I1	11111111	Chip 1 Chan B Q1	11111111	1	2
Chip 1 Chan C I1	11111111	Chip 1 Chan C Q1	11111111	1	3
Chip 1 Chan D I1	11111111	Chip 1 Chan D Q1	11111111	1	4
Chip 2 Chan A I1	11111111	Chip 2 Chan A Q1	11111111	1	5
Chip 2 Chan B I1	11111111	Chip 2 Chan B Q1	11111111	1	6
Chip 2 Chan C I1	11111111	Chip 2 Chan C Q1	11111111	1	7
Chip 2 Chan D I1	11111111	Chip 2 Chan D Q1	11111111	1	8
Chip 1 Chan A I2	11111111	Chip 1 Chan A Q2	11111111	2	9
Chip 1 Chan B I2	11111111	Chip 1 Chan B Q2	11111111	2	10
Chip 1 Chan C I2	11111111	Chip 1 Chan C Q2	11111111	2	11
Chip 1 Chan D I2	11111111	Chip 1 Chan D Q2	11111111	2	12
Chip 2 Chan A I2	11111111	Chip 2 Chan A Q2	11111111	2	13
Chip 2 Chan B I2	11111111	Chip 2 Chan B Q2	11111111	2	14
Chip 2 Chan C I2	11111111	Chip 2 Chan C Q2	11111111	2	15
Chip 2 Chan D I2	11111111	Chip 2 Chan D Q2	11111111	2	16

$1 \leq N \leq 8$
Frame length = N 64-bit words

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Table 4.5 – ICS-554v-w-MN(y) Rev.z Data Output Format, N Real Narrow Band Channels/FIFO

64-bit PCI Bus Word				Frame No.	Sequence
63 40	39 32	31 8	7 0		
Chip 1 Chan A I1	11111111	Chip 1 Chan B I1	11111111	1	1
Chip 1 Chan C I1	11111111	Chip 1 Chan D I1	11111111	1	2
Chip 2 Chan A I1	11111111	Chip 2 Chan B I1	11111111	1	3
Chip 2 Chan C I1	11111111	Chip 2 Chan D I1	11111111	1	4
Chip 1 Chan A I2	11111111	Chip 1 Chan B I2	11111111	2	5
Chip 1 Chan C I2	11111111	Chip 1 Chan D I2	11111111	2	6
Chip 2 Chan A I2	11111111	Chip 2 Chan B I2	11111111	2	7
Chip 2 Chan C I2	11111111	Chip 2 Chan D I2	11111111	2	8
Chip 1 Chan A I3	11111111	Chip 1 Chan B I3	11111111	3	9
Chip 1 Chan C I3	11111111	Chip 1 Chan D I3	11111111	3	10
Chip 2 Chan A I3	11111111	Chip 2 Chan B I3	11111111	3	11
Chip 2 Chan C I3	11111111	Chip 2 Chan D I3	11111111	3	12
Chip 1 Chan A I4	11111111	Chip 1 Chan B I4	11111111	4	11
Chip 1 Chan C I4	11111111	Chip 1 Chan D I4	11111111	4	12

N = 2, 4, 6, 8
Frame length = N/2

Table 4.6 – ICS-554v-w-MN(y) Rev.z Data Output Format, N Complex Split-I/Q Channels/FIFO

64-bit PCI Bus Word				Frame No	Sequence
63	39 32	31 8	7 0		
Chip 1 Chan A I1	11111111	Chip 1 Chan A Q1	11111111	1	1
Chip 1 Chan B I1	11111111	Chip 1 Chan B Q1	11111111	1	2
Chip 1 Chan A I2	11111111	Chip 1 Chan A Q2	11111111	1	3
Chip 1 Chan B I2	11111111	Chip 1 Chan B Q2	11111111	1	4
Chip 2 Chan A I1	11111111	Chip 2 Chan A Q1	11111111	1	5
Chip 2 Chan B I1	11111111	Chip 2 Chan B Q1	11111111	1	6
Chip 2 Chan A I2	11111111	Chip 2 Chan A Q2	11111111	1	7
Chip 2 Chan B I2	11111111	Chip 2 Chan B Q2	11111111	1	8
Chip 1 Chan A I3	11111111	Chip 1 Chan A Q3	11111111	2	9
Chip 1 Chan B I3	11111111	Chip 1 Chan B Q3	11111111	2	10
Chip 1 Chan A I4	11111111	Chip 1 Chan A Q4	11111111	2	11
Chip 1 Chan B I4	11111111	Chip 1 Chan B Q4	11111111	2	12
Chip 2 Chan A I3	11111111	Chip 2 Chan A Q3	11111111	2	13
Chip 2 Chan B I3	11111111	Chip 2 Chan B Q3	11111111	2	14
Chip 2 Chan A I4	11111111	Chip 2 Chan A Q4	11111111	2	15
Chip 2 Chan B I4	11111111	Chip 2 Chan B Q4	11111111	2	16

N = 2, 4
Frame length = 2N

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Table 4.7 – ICS-554v-w-MN(y) Rev.z Data Output Format, N Real Split-I/Q Channels/FIFO

64-bit PCI Bus Word				Frame No.	Sequence
63 40	39 32	31 8	7 0		
Chip 1 Chan A I1	11111111	Chip 1 Chan A I2	11111111	1	1
Chip 1 Chan B I1	11111111	Chip 1 Chan B I2	11111111	1	2
Chip 2 Chan A I1	11111111	Chip 2 Chan A I2	11111111	1	3
Chip 2 Chan B I1	11111111	Chip 2 Chan B I2	11111111	1	4
Chip 1 Chan A I3	11111111	Chip 1 Chan A I4	11111111	2	5
Chip 1 Chan B I3	11111111	Chip 1 Chan B I4	11111111	2	6
Chip 2 Chan A I3	11111111	Chip 2 Chan A I4	11111111	2	7
Chip 2 Chan B I3	11111111	Chip 2 Chan B I4	11111111	2	8

N = 2, 4
Frame length = N

Table 4.8 – ICS-554v-w-MN(y) Rev.z Data Output Format, N Complex Wide Band Channels/FIFO

64-bit PCI Bus Word				Frame No.	Sequence
63 40	39 3	31 8	7 0		
Chip 1 I1	11111111	Chip 1 Q1	11111111	1	1
Chip 1 I2	11111111	Chip 1 Q2	11111111	1	2
Chip 1 I3	11111111	Chip 1 Q3	11111111	1	3
Chip 1 I4	11111111	Chip 1 Q4	11111111	1	4
Chip 2 I1	11111111	Chip 2 Q1	11111111	1	5
Chip 2 I2	11111111	Chip 2 Q2	11111111	1	6
Chip 2 I3	11111111	Chip 2 Q3	11111111	1	7
Chip 2 I4	11111111	Chip 2 Q4	11111111	1	8
Chip 1 I5	11111111	Chip 1 Q5	11111111	2	9
Chip 1 I6	11111111	Chip 1 Q6	11111111	2	10
Chip 1 I7	11111111	Chip 1 Q7	11111111	2	11
Chip 1 I8	11111111	Chip 1 Q8	11111111	2	12
Chip 2 I5	11111111	Chip 2 Q5	11111111	2	13
Chip 2 I6	11111111	Chip 2 Q6	11111111	2	14
Chip 2 I7	11111111	Chip 2 Q7	11111111	2	15
Chip 2 I8	11111111	Chip 2 Q8	11111111	2	16

N = 1, 2
Frame length = 4N

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Table 4.9 – ICS-554v-w-MN(y) Rev.z Data Output Format, N Real Wide Band Channels/FIFO

64-bit PCI Bus Word				Frame No.	Sequence
63 40	**39 32**	**31 8**	**7 0**		
Chip 1 I1	11111111	Chip 1 I2	11111111	1	1
Chip 1 I3	11111111	Chip 1 I4	11111111	1	2
Chip 2 I1	11111111	Chip 2 I2	11111111	1	3
Chip 2 I3	11111111	Chip 2 I4	11111111	1	4
Chip 1 I5	11111111	Chip 1 I6	11111111	2	5
Chip 1 I7	11111111	Chip 1 I8	11111111	2	6
Chip 2 I5	11111111	Chip 2 I6	11111111	2	7
Chip 2 I7	11111111	Chip 2 I8	11111111	2	8

N = 1, 2
Frame length = 2N

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5 HARDWARE CONFIGURATION

5.1 Clock, Trigger and Sync Jumper Settings

A number of jumpers on the ICS-554 need to be set in order to configure clock trigger and sync behavior as internal or external. Figure 8 shows the jumper locations for all board assemblies other than B11608, and Table 5.1 describes the required jumper settings for these boards. Figure 9 shows the jumper locations for board assembly B11608, and Table 5.2 describes the required jumper settings for this board assembly. The assembly number is given on a label on the board. Figure 4 and Figure 5 show the position of the P6 JTAG port for each assembly.

Table 5.1– ICS-554 Jumper Functions (All Assemblies Except B11608)

Jumper	FUNCTION
J3. Pins 1,2,3	External Trigger input to TRIG: 1,2 connected; Internal Trigger output from TRIG: 2,3 connected (default setting)
J4. Pins 1,2,3	External Sync input to SYNC: 1,2 connected; Internal Sync output from SYNC: 2,3 connected (default setting)
J5. Pins 1,2,3	External Clock input to CLK: 1,2 connected; Internal Clock output from CLK: 2,3 connected (default setting)

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5.1.1 Jumpers for All Assemblies, Except B11608

The functions for Jumpers J3-J 5 are described in Table 5.1. Jumpers J11-J15 are used for JTAG configuration. The default settings (see Figure 8) enable programming of the user-programmable Xilinx FPGA from either the JTAG port, or by using the optional JTAG Emulator software tool over PCI bus.

Programming of the Xilinx FPGA may be disabled (by both methods) by removing all of the jumpers J11 – J15, inclusive.

All other combinations of settings of J11 through J15 are for factory use only.

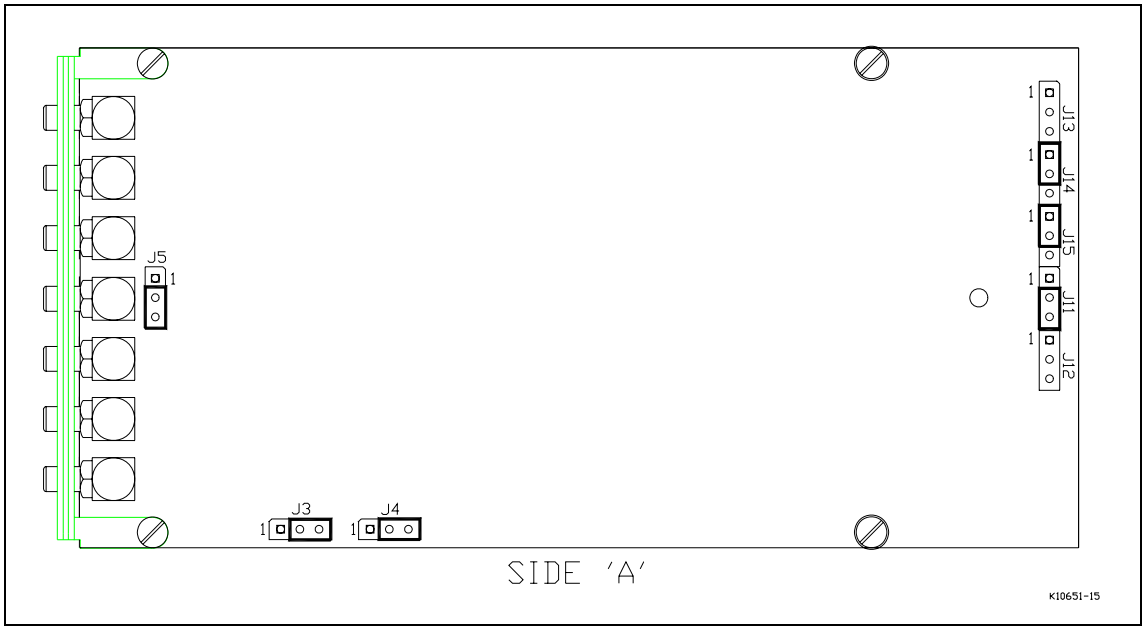


Figure 8 - ICS-554 Jumper Positions and Default Settings (All Versions Except B11608)

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5.1.2 Jumpers J3 – J9 (B11608 Assembly Only)

Table 5.2– ICS-554 Jumper Functions (B11608 Assembly Only)

Jumper	Function
J3. Pins 1,2,3	External Trigger input to TRIG: 1,2 connected; Internal Trigger output from TRIG: 2,3 connected (default setting)
J4. Pins 1,2,3	External Sync input to SYNC: 1,2 connected; Internal Sync output from SYNC: 2,3 connected (default setting)
J5. Pins 1,2,3	External Clock input to CLK: 1,2 connected; Internal Clock output from CLK: 2,3 connected (default setting)
J6. Pins 1,2,3	JTAG TDI to program Xilnx FPGA: 1,2 connected;(default setting) JTAG TDI to program CPLD: 2,3 connected (users do not use)
J7. Pins 1,2,3	JTAG TMS to program Xilnx FPGA: 1,2 connected;(default setting) Use JTAG TMS to program CPLD: 2,3 connected (users do not use)
J8. Pins 1,2,3	JTAG TDO to program Xilnx FPGA: 1,2 connected;(default setting) Use JTAG TDO to program CPLD: 2,3 connected (users do not use)
J9. Pins 1,2,3	JTAG TCK to program Xilnx FPGA: 1,2 connected;(default setting) Use JTAG TCK to program CPLD: 2,3 connected (users do not use)

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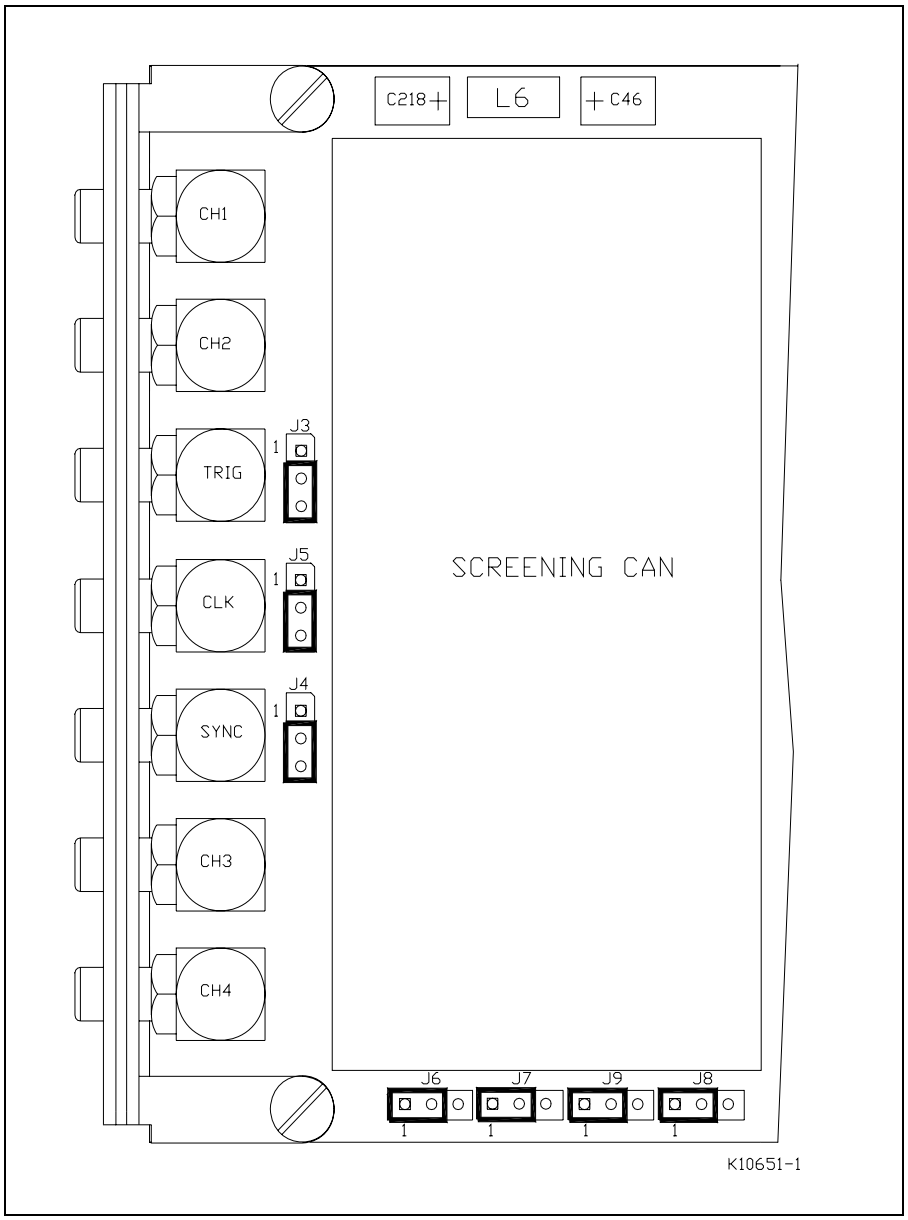


Figure 9 – ICS-554 Jumper Positions and Default Settings (B11608 Assembly Only)

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6 PROGRAMMING MODEL

The ICS-554 is controlled by means of memory-mapped registers accessed through the PCI Bus interface. The PCI address map is summarized in Table 6.1. The ICS-554 register set is listed in Table 6.2. Register bit allocations are given in Figure 10.

Data should be read from the PCI Bus interface using the chain mode DMA controller of the QL5064, as described in Section 6.3 below. However, it is also possible to read data by means of target mode access to the memory space of the board.

A detailed description of the QL5064 register and bit allocations is given in Reference [4].

Table 6.1 - PCI Address Map (summary)

Name	PCI address	Description	Size
QL5064 Internal registers	PCI_BASE0		4 KBytes
QL5064 Configuration Space 1	PCI_BASE0+ 0x00-0xFF	QL5064 control registers. Memory space, 32-bit addressing	256 Bytes
QL5064 Configuration Space 2	PCI_BASE0+ 0x1000-0x10FF	QL5064 control registers (FPGA side). Memory space, 32-bit addressing	256 Bytes
ICS-554 Register Set	PCI_BASE1+ 0x000-0xFFF	ICS-554 register access. Memory space, 32-bit addressing	4 KBytes
ICS-554 Memory Space	PCI_BASE2+ 0x0000000-0x3FFFFFF	ICS-554 buffer memory access	16 MBytes

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Table 6.2 - ICS-554 Address Map

Register	PCI Bus Address	Type
ICS-554 Register Set	**PCI_BASE1**	
Status Register	PCI_BASE1 + 0x000	Read/Write
Interrupt Mask Register (IMR)	PCI_BASE1 + 0x008	Read/Write
Control Register 1	PCI_BASE1 + 0x010	Read/Write
Control Register 2	PCI_BASE1 + 0x018	Read/Write
JTAG Program Register	PCI_BASE1 + 0x020	Read/Write
ADC Ch1 & Ch2 Decimation Register	PCI_BASE1 + 0x080	Read/Write
ADC Ch1 & Ch2 Acquisition Count Register	PCI_BASE1 + 0x088	Read/Write
ADC Ch3 & Ch4 Decimation Register	PCI_BASE1 + 0x090	Read/Write
ADC Ch3 & Ch4 Acquisition Count Register	PCI_BASE1 + 0x098	Read/Write
FIFO Level Control Register	PCI_BASE1 + 0x0D8	Write only
Trigger Register	PCI_BASE1 + 0x0E0	Write only
Software ADC Reset Register	PCI_BASE1 + 0x0F0	Write only
Software Board Reset Register	PCI_BASE1 + 0x0F8	Write only
GC4016 Configuration Registers	PCI_BASE1 + 0x100 - 0x1F8	Read/Write
User Programmable FPGA Registers	PCI_BASE1 + 0x200 - 0x2F8	Read/Write
ICS-554 Memory Space	**PCI Bus Address**	**Type**
DATA FIFO1	PCI_BASE2 + 0x00000000	Read only
DATA FIFO2	PCI_BASE2 + 0x00800000	Read only

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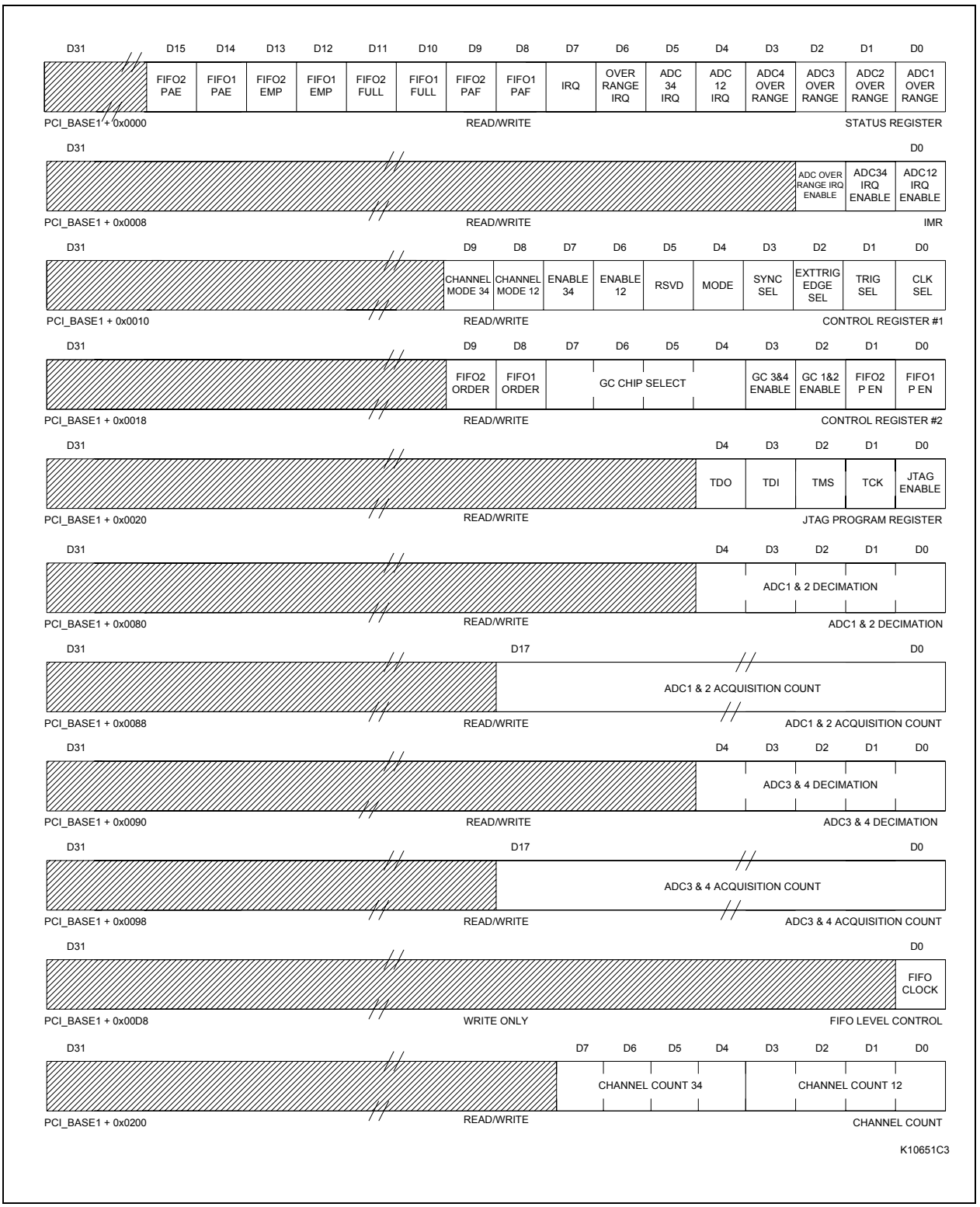


Figure 10 – ICS-554 Register Map

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6.1 General Notes

All programming and control of the ICS-554 is accomplished through the PCI Bus interface using 64-bit or 32-bit transfers. All control register bits that are not defined have no effect on the operation of the ICS-554. All undefined bits may be read as zero or one.

6.2 QL5064 Registers

The ICS-554 uses the QuickLogic QL5064 PCI Bus interface chip. The QL5064 is an FPGA containing a PCI interface core. The QL5064 register set is complex, and a complete description is not given here. Details of the QL5064 may be found in the QL5064 data sheet (see Reference [4]).

As with any PCI Bus device, the QL5064 has a unique 256 Byte region called the Configuration Header Space, or just Configuration Space (see References [3] and [4]). It is mandatory that portions of this configuration header are addressable in order for a PCI agent to be in full compliance with the PCI specification. In order for ICS-554 device registers to be addressable, it is necessary that information in the configuration space is read. Base address values and lengths must then be written to registers also in configuration space. This is normally done by the operating system.

The ICS-554 uses three of the available base address registers defined by the PCI specification for access the module. These base address registers, and the lengths assigned to the corresponding mapped areas of PCI address space are given in Table 6.1. The space addressed by PCI_BASE1 is split into two areas of 256 Bytes, with an unused area between them.

The QL5064 registers are described in Table 6.3.

The vendor and sub-vendor information contained in the PCI configuration space is as follows:

Vendor ID: 0x11E3
Device ID: 0x0006
Sub-vendor ID: 0x1464
Sub-system ID: 0x0554

6.3 Endian Conversion

Endian ordering refers to the significance with which data is ordered within a computer system. The ICS-554 implements “little-endian” ordering of data within larger data widths. When operating the ICS-554 within a PC- or Intel-based system, no endian conversion will be required, since these are little-endian systems. In little-endian systems, the highest address is applied to the most significant byte (or word) of data of a given size; in Big-endian systems (e.g. most Unix-based systems such as Sparc and PowerPC), the lowest address is applied to the most significant bytes (or word) of data in an element of data of a given size.

The QL5064 interface provides “endian” conversion for Big-endian systems for a variety of data types. This feature results in 8-bit, 16-bit or 32-bit word order being reversed within larger word sizes (16-bit, 32-bit or 64-bit). The selection of endian function is made in the QL5064 Control register, address offset 0x1008 (see Table 6.3). Table 6.4 describes the effects of the various settings of this register.

The Endian ordering should be set according to the type of system in which the ICS-554 is installed and the bus width employed (32-bit or 64-bit). The most commonly used settings are shown in bold type in Table 6.4.

Note that when using chain-mode DMA (see Section 6.4), the linked list data must be reordered by the user before being written to host memory, when using a Big-endian host. This is because the data is read directly by the DMA controller without being passed through the endian conversion hardware.

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Table 6.3 - QL5064 Control Registers

Register	Offset (PCI_BASE0)	Type	Width (bits)	Description
Master Write Address 0	0x00	R/W	64	PCI address for write to PCI target
Master Write Transfer Count 0	0x08	R/W	32	Write transfer count in bytes
Master Read Address 0 / Chain Descriptor Start Address	0x48	R/W	64	PCI address for read from PCI target / pointer to first chain descriptor PCI start address
Master Read Transfer Count 0	0x50	R/W	32	Read transfer count in bytes
FIFO Level Controls	0x68	R/W	64	Almost full and almost empty levels for 6 FIFOs Recommended setting is 0x0008.0020.0020.001B
DMA Control	0x90	R/W	64	Set Bit 16 to start Transmit 0 DMA transfer Set Bit 18 to start Receive 0 DMA transfer Set Bit 20 to start Chain Mode DMA transfer
Board Reset	0xE8	W	1 (bit 0)	Write 1 - perform a Host Total Reset Write 0 - no effect
Control Register	0x1008	R/W	8	[01:00] must be 00
LOC_XMT0_CNT_ADDR	0x1010	R/W	64	[31:00] Local Start Address for DMA Transmit 0 [63:32] Transfer count in bytes
LOC_RCV0_CNT_ADDR	0x1020	R/W	64	[31:00] Local Start Address for DMA Receive 0 [63:32] Transfer count in bytes
LOC_DMA_CANCEL	0x1030	W	8	Write 1 to this register to cancel unfinished DMA

Table 6.4- Endian Conversion when Transferring Data from ICS-554 Local Bus to PCI Bus

PCI Bus		**AD[63:56]**	**AD[55:48]**	**AD[47:40]**	**AD[39:32]**	**AD[31:24]**	**AD[23:16]**	**AD[15:8]**	**AD[7:0]**
	CR<5:2>								
ICS Local Data Bus	**0000**	**LD[63:56]**	**LD[55:48]**	**LD[47:40]**	**LD[39:32]**	**LD[31:24]**	**LD[23:16]**	**LD[15:8]**	**LD[7:0]**
	0001	**LD[31:24]**	**LD[23:16]**	**LD[15:8]**	**LD[7:0]**	**LD[63:56]**	**LD[55:48]**	**LD[47:40]**	**LD[39:32]**
	0010	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]
	0011	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]
	0100	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]
	0101	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]	LD[47:40]
	0110	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]	LD[55:48]
	0111	LD[55:48]	LD[47:40]	LD[39:32]	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]	LD[63:56]
	1000	**LD[7:0]**	**LD[15:8]**	**LD[23:16]**	**LD[31:24]**	**LD[39:32]**	**LD[47:40]**	**LD[55:48]**	**LD[63:56]**
	1001	**LD[39:32]**	**LD[47:40]**	**LD[55:48]**	**LD[63:56]**	**LD[7:0]**	**LD[15:8]**	**LD[23:16]**	**LD[31:24]**

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6.4 Performing DMA Transfers

When reading data from the board through the PCI interface, the DMA controller in the QL5064 is used. The controller can be used with or without chain mode (scatter-gather) operation. The QL5064 should normally be the PCI bus master (initiator) for transfers. When using chain mode DMA, the DMA controller requires the chain mode descriptor tables to be located in PCI addressable memory. This is usually located in the host processor. Please note that the starting PCI target address must be quadword (8 Byte or 64-bit) aligned for correct DMA mode operation.

The QL5064 PCI core uses the Transmit 0 DMA channel to move data from the ICS-554 to PCI Bus. The DMA engine supports both transmit and receive functions, but the ICS-554 does not use the receive function.

6.4.1 Non-Chain Mode DMA operation

To use DMA without scatter-gather, the QL5064 DMA controller must be programmed with the PCI Bus starting address for the target data, the source (ICS-554 local memory) starting address, which is 0x000000 for FIFO 1, and 0x800000 for FIFO 2, and the length of the transfer. The length programmed should not exceed the amount of data available in the FIFO.

The steps required to start Transmit 0 DMA operation for writing data to the ICS-554 are as follows:

1. Write the starting PCI target address to QL5064 control register "Master Write Address 0" (offset 0x00).
2. Write the transfer count (in bytes) to QL5064 control register "Master Write Transfer Count 0" (offset 0x08, bit[31:0]. The minimum transfer count is 8 Bytes (8 Bytes or 1 Quadword). The maximum transfer count is equal to the FIFO programmed almost full level. Transfers must always be in multiples of 8 Bytes. The transfer must be Quadword (8 Byte) aligned.
3. Write the transfer count and starting Local address to the ICS Local Bus control register LOC_XMT0_CNT_ADDR (offset 0x1010). The transfer count written to this register must be the same as that written to the Master Write Transfer Count 0 register (offset 0x08). The starting local address must be quad word (8 Byte) aligned.
4. To start the DMA transfer, write a "1" to the QL5064 control register DMA Control register Start/Done bit (offset 0x90, bit 16).
5. The transfer will continue until the transfer count expires or is cancelled.

6.4.2 Chain Mode DMA operation

The following steps are required to use chain mode DMA:

1. Write the chain mode DMA descriptor tables to PCI memory. The format of the Chain Mode DMA descriptor tables is given in Figure 11. The requirements for Local Starting Address and Transfer Count in the chain descriptors are the same as for non-chain mode DMA. If the host is a “Big-endian” machine, it will be necessary to reorder the descriptor data, as described in Section 6.3. The usual reordering required is byte order within 64-bit words. However, this may vary depending on the details of the system implementation.
2. Write the PCI address of the first descriptor pointer to QL5064 control register "Master Read Address/Chain Descriptor Start Address" (PCI offset 0x48).
3. Start execution of the instructions in the descriptor tables by writing "1" to "Chain Enable" (PCI offset 0x90, bit [20]).
4. The chain mode DMA will run until the end-of-chain flag is encountered or until the DMA transfer is cancelled.

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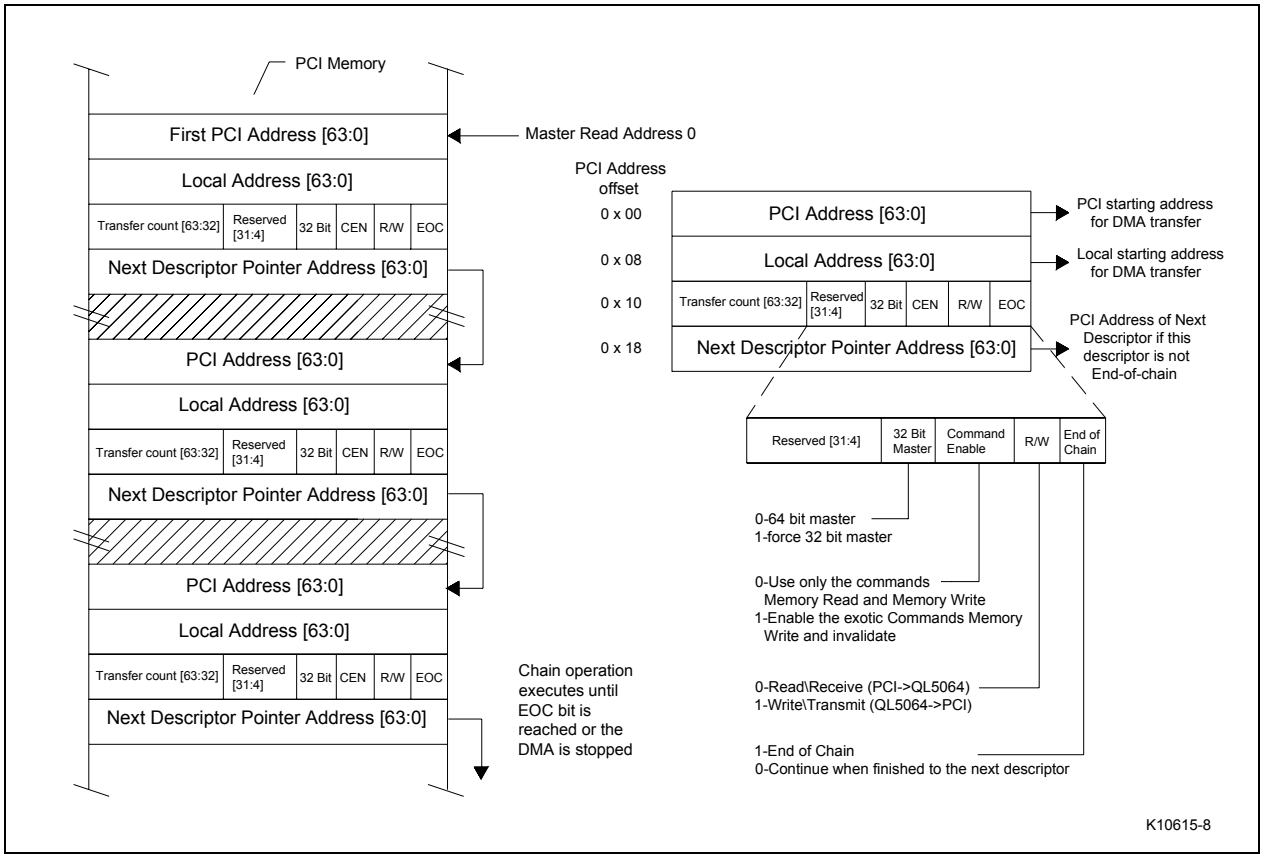


Figure 11 – DMA Chain Mode Descriptors

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6.4.3 Canceling a DMA Transfer

It may become necessary to cancel a DMA transfer that is in progress, for example if a time out has occurred. The procedure for doing this is as follows:

1. Cancel DMA in QL5064 core (see Reference [4]).
2. Write 1 to the LOC_DMA_CANCEL register (see Table 6.3 above).

The order of operations shown above must be observed.

6.4.4 PCI Target Mode

The ADC data area is mapped to PCI Base Address 2 (PCI_BASE2 – see Table 6.1 above). The host may read data from this area as a PCI slave device rather than use the ICS-554 DMA engine. However, the transfer rate achievable is very limited. The ICS-554 does not support target mode DMA, so a DMA engine on the host device may not be used; only single cycle reads are supported. The maximum length read must not exceed the programmed buffer length.

This area of the memory map is configured to be non-prefetchable. In one PCI read transaction, only one word is read from the board. If the transaction is in 32-bit PCI bus mode, a 32-bit word is read. If the transaction is in 64-bit PCI bus mode, a 64-bit word is read.

6.5 Status Register (SR)

Some bits Read Only, Some bits Read/Write

The Status Register contains information about the state of the ICS-554. It is used to determine the interrupt status of the ICS-554, and the source of the interrupt. It also contains error condition information.

6.5.1 SR<0> - ADC1 Over Range

This bit indicates that an analog input over range condition has occurred on ADC channel 1. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the four ADC Over Range bits to determine on which channel the over range occurred. This bit is latched; to clear it, a one must be written to it.

Note: It has been observed that this bit may be asserted if the ambient temperature is high. This is a characteristic of the converter chip.

SR<0>	**ADC 1 Over Range**
READ/WRITE	
0	No over range has been detected at ADC channel 1
1	Over range has been detected at ADC channel 1

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6.5.2 SR<1> - ADC2 Over Range

This bit indicates that an analog input over range condition has occurred on ADC channel 2. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the four ADC Over Range bits to determine on which channel the over range occurred. This bit is latched; to clear it, a one must be written to it.

Note: It has been observed that this bit may be asserted if the ambient temperature is high. This is a characteristic of the converter chip.

SR<1>	**ADC 2 Over Range**
READ/WRITE	
0	No over range has been detected at ADC channel 2
1	Over range has been detected at ADC channel 2

6.5.3 SR<2> - ADC3 Over Range

This bit indicates that an analog input over range condition has occurred on ADC channel 3. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the four ADC Over Range bits to determine on which channel the over range occurred. This bit is latched; to clear it, a one must be written to it.

Note: It has been observed that this bit may be asserted if the ambient temperature is high. This is a characteristic of the converter chip.

SR<2>	**ADC 3 Over Range**
READ/WRITE	
0	No over range has been detected at ADC channel 3
1	Over range has been detected at ADC channel 3

6.5.4 SR<3> - ADC4 Over Range

This bit indicates that an analog input over range condition has occurred on ADC channel 4. If the ADC Over Range interrupt has been enabled by setting the ADC Over Range mask bit of the IMR register, an interrupt will occur if an over range signal is detected on any channel. The occurrence of this interrupt is flagged by the Over Range bit (SR<06>). The user should then check the four ADC Over Range bits to determine on which channel the over range occurred. This bit is latched; to clear it, a one must be written to it.

Note: It has been observed that this bit may be asserted if the ambient temperature is high. This is a characteristic of the converter chip.

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SR<3>	ADC 4 Over Range
READ/WRITE	
0	No over range has been detected at ADC channel 4
1	Over range has been detected at ADC channel 4

6.5.5 SR<4> - ADC12 IRQ

This bit will be set when the quantity of data acquired in FIFO 1 reaches the almost full level programmed by the user to the FIFO Level Control register for FIFO 1. If ADC channel 1 & 2 interrupts have been enabled by setting bit 0 of the IMR register, an interrupt request will occur.

SR<4>	ADC Channel 1 & 2 Interrupt Request
READ ONLY	
0	ADC channel 1 & 2 not asserting IRQ
1	ADC channel 1 & 2 asserting IRQ

6.5.6 SR<5> - ADC34 IRQ

This bit will be set when the quantity of data acquired in FIFO 2 reaches the almost full level programmed by the user to the FIFO Level Control register for FIFO 2. If ADC channel 3 & 4 interrupts have been enabled by setting bit 1 of the IMR register, an interrupt request will occur.

SR<5>	ADC Channel 3 & 4 Interrupt Request
READ ONLY	
0	ADC channel 3 & 4 not asserting IRQ
1	ADC channel 3 & 4 asserting IRQ

6.5.7 SR<6> - Over Range IRQ

This bit indicates that an analog input over range condition has occurred on one or more of the ADC channels. If the ADC over range interrupt is enabled, an interrupt request will occur. The user should first check this bit and the ADC 12 IRQ and ADC 34 IRQ bits to determine which type of interrupt has occurred. If this bit is set, the user should then check the ADC1, 2, 3 and 4 Over Range bits to determine on which channel/s the input voltage swing exceeded the full scale for the ADC. The interrupt must be cleared by clearing the ADCx Over Range bit/s responsible for the interrupt (see above).

SR<6>	Over Range IRQ
READ ONLY	
0	An ADC over range IRQ has not occurred on any channel.
1	An ADC over range IRQ has occurred on one or more channel/s.

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6.5.8 SR<7> - IRQ

This bit indicates that the ICS-554 is asserting a PCI bus interrupt from either of the three available sources (i.e. ADC12, ADC34 or Over Range). It will therefore be set if any of bits 4, 5 and 6 of this register are set.

SR<7>	**PCI Bus Interrupt Request**
READ ONLY	
0	PCI Bus interrupt is not asserted
1	PCI Bus interrupt is asserted

6.5.9 SR<8> - FIFO 1 PAF

This bit indicates that data buffer FIFO 1 is ready for reading. When the amount of data from ADC channel 1 and/or channel 2 written into FIFO 1 reaches the buffer length value programmed to the FIFO Level Control register for FIFO 1, this bit is asserted low. The ADC12 IRQ will also be set. An interrupt will occur if the ADC12 IRQ enable bit in the IMR register is set. Users should check this bit to determine whether to read data from FIFO 1 or FIFO 2.

SR<8>	**FIFO 1 PAF**
READ ONLY	
0	FIFO 1 Programmable Almost Full is asserted
1	FIFO1 Programmable Almost Full is not asserted

6.5.10 SR<9> - FIFO 2 PAF

This bit indicates that data buffer FIFO 2 is ready for reading. When the amount of data from ADC channel 3 and/or channel 4 written into FIFO 2 reaches the buffer length value programmed to the FIFO Level Control register for FIFO 2, this bit is asserted low. The ADC34 IRQ will also be set. An interrupt will occur if the ADC34 IRQ enable bit in the IMR register is set. Users should check this bit to determine whether to read data from FIFO 1 or FIFO 2.

SR<9>	**FIFO2 PAF**
READ ONLY	
0	FIFO2 Programmable Almost Full is asserted
1	FIFO2 Programmable Almost Full is not asserted

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6.5.11 SR<10> - FIFO 1 Full

This bit indicates that data buffer FIFO 1 is full. When this occurs, data has been lost. On current revisions of this board, the FIFO full flags are latched, and must be proactively cleared by writing '1' to them. They are also cleared on Board reset and ADC reset. However, on earlier revisions of this board, the bit is not latched; it will clear when the FIFO level falls below the full level. For further details see APPENDIX B.

SR<10>	**FIFO 1 Full**
READ ONLY	
0	FIFO 1 is not full
1	FIFO 1 is full

6.5.12 SR<11> - FIFO 2 Full

This bit indicates that data buffer FIFO 2 is full. When this occurs, data has been lost. On current revisions of this board, the FIFO full flags are latched, and must be proactively cleared by writing '1' to them. They are also cleared on Board reset and ADC reset. However, on earlier revisions of this board, the bit is not latched; it will clear when the FIFO level falls below the full level. For further details see APPENDIX B.

SR<11>	**FIFO 2 Full**
READ ONLY	
0	FIFO 2 is not full
1	FIFO 2 is full

6.5.13 SR<12> - FIFO 1 Empty

This bit, when set, indicates that data buffer FIFO 1 is empty. When this occurs, the read length may have exceeded the quantity of data available in the FIFO, and the data read may include erroneous values. However, it will always be asserted when the board has not been triggered, since no data has been converted in this case.

SR<12>	**FIFO 1 Empty**
READ ONLY	
0	FIFO 1 not empty
1	FIFO 1 empty

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6.5.14 SR<13> - FIFO 2 Empty

This bit, when set, indicates that data buffer FIFO 2 is empty. It will always be asserted when the board has not been triggered, since no data has been converted in this case. When asserted during normal operation, it may indicate that the read length has exceeded the quantity of data available in the FIFO, and the data read may include erroneous values.

SR<13>	**FIFO 2 Empty**
READ ONLY	
0	FIFO 2 not empty
1	FIFO 2 empty

6.5.15 SR<14> - FIFO 1 PAE

This bit, when asserted low, indicates that the amount of data in FIFO 1 has fallen to the value programmed to the FIFO Level Control register for the FIFO 1 Almost Empty level.

SR<14>	**FIFO 1 PAE**
READ ONLY	
0	FIFO 1 Programmable Almost Empty is asserted
1	FIFO 1 Programmable Almost Empty is not asserted

6.5.16 SR<15> - FIFO 2 PAE

This bit, when asserted low, indicates that the amount of data in FIFO 2 has fallen to the value programmed to the FIFO Level Control register for the FIFO 2 Almost Empty level.

SR<15>	**FIFO 2 PAE**
READ ONLY	
0	FIFO 2 Programmable Almost Empty is asserted
1	FIFO 2 Programmable Almost Empty is not asserted

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6.6 Interrupt Mask Register (IMR)

Read/Write

This register is used to enable PCI bus interrupts for ADC buffer almost full and ADC analog input over range conditions. Masked interrupts are still seen in the corresponding bits of the status register, but do not cause an interrupt to occur.

6.6.1 IMR<0> - ADC12 IRQ Mask

This register is used to enable PCI bus interrupts for the ADC 1 & 2 buffer almost full condition. If the interrupt is masked, the ADC12 IRQ bit of the Status register will still indicate the occurrence of this condition, but no interrupt will occur. This bit must be cleared by the interrupt handler in order to prevent the possibility of a further interrupt before data has been read from FIFO 1.

IMR<0>	**ADC12 IRQ Mask**
READ/WRITE	
0	ADC12 interrupts are disabled
1	ADC12 interrupts are enabled

6.6.2 IMR<1> - ADC34 IRQ Mask

This register is used to enable PCI bus interrupts for the ADC 3 & 4 buffer almost full condition. If the interrupt is masked, the ADC34 IRQ bit of the Status register will still indicate the occurrence of this condition, but no interrupt will occur. This bit must be cleared by the interrupt handler in order to prevent the possibility of a further interrupt before data has been read from FIFO 2.

IMR<1>	**ADC34 IRQ Mask**
READ/WRITE	
0	ADC34 interrupts are disabled
1	ADC34 interrupts are enabled

6.6.3 IMR<2> - ADC Analog Input Over Range IRQ Mask

This bit enables the ADC analog input over range PCI bus interrupts. An analog signal voltage over range condition occurring on any input channel will cause this condition to be asserted. If the voltage over range condition has not been corrected, setting this bit again will immediately cause a further interrupt.

IMR<2>	**ADC Over Range IRQ Mask**
READ/WRITE	
0	ADC over range interrupts are disabled
1	ADC over range interrupts are enabled

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6.7 Control Register 1 (CR1)

Read/Write

The control register allows the user to configure the following operating parameters:

- internal/external clock selection
- internal/external trigger selection
- external trigger edge selection
- internal/external synchronization selection
- acquisition mode
- ADC1&2 enable
- ADC3&4 enable
- FIFO1 one/two channel selection
- FIFO2 one/two channel selection

The register bits are discussed in detail below. The reset default for each bit describes the state of the bit after a hardware PCI Bus reset or software reset via the Board Reset register.

6.7.1 CR1<00> - ADC Sampling Clock Select

This bit selects internal or external sampling clock. Board jumper block J5 must be configured in accordance with the setting of this bit (see Section 5 above).

CR1<00>	ADC Sampling Clock Select
0	Internal Sampling Clock
1	External Sampling Clock

6.7.2 CR1<01> - Trigger Select

This bit selects internal or external triggering of the board. Board jumper block J3 must be configured in accordance with the setting of this bit (see Section 5 above). When internal triggering is selected, the board must be triggered under software control by writing a 1 to Trigger register, after the board has been fully configured.

CR1<01>	Trigger Select
0	Internal Trigger
1	External Trigger

6.7.3 CR1<02> - External Trigger Edge Select

This bit selects which edge of an external trigger signal will cause triggering to occur. External triggering must be selected in CR1<01> in order for this bit to be meaningful.

CR1<02>	External Trigger Edge Select
0	Trigger on rising edge of External Trigger
1	Trigger on falling edge of External Trigger

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6.7.4 CR1<03> - Sync Select

This bit selects internal or external synchronization of the DDCs (if installed). Board jumper block J4 must be configured in accordance with the setting of this bit (see Section 5 above).

CR1<03>	Sync Selection
0	Internal Sync
1	External Sync

6.7.5 CR1<04> - Mode

This bit selects the operating mode of the ICS-554. In Capture mode, when triggered, the board will acquire a number of samples equal to the value programmed to the Acquisition Count registers before ceasing conversion. In Continuous mode, it will continuously convert data after the trigger, until stopped by clearing the enable bits, CR1<06> and/or CR1<07>.

CR1<04>	Mode
0	Continuous Mode
1	Capture Mode

6.7.6 CR1<05> - Reserved control bit

This control bit is reserved for future use.

CR1<05>	Reserved
0	Do not care
1	Do not care

6.7.7 CR1<06> ADC Channels 1 & 2 Acquisition Enable

This bit enables ICS-554 channels 1 and/or 2, with data storage in FIFO 1. The board must be triggered, after this bit is set, by writing to the Trigger register, if internal triggering was selected in CR1<01>. If external triggering was selected in CR1<01>, acquisition will start when the trigger signal occurs. Clearing this bit will cause acquisition to cease on channels 1 and 2.

CR1<06>	ADC12 Acquisition Enable
0	Acquisition disabled
1	Acquisition enabled

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6.7.8 CR1<07> ADC Channel 3 & 4 Acquisition Enable

This bit enables ICS-554 channels 3 and/or 4, with data storage in FIFO 2. The board must be triggered, after this bit is set, by writing to the Trigger register, if internal triggering was selected in CR1<01>. If external triggering was selected in CR1<01>, acquisition will start when the trigger signal occurs. Clearing this bit will cause acquisition to cease on channels 3 and 4.

CR1<07>	ADC34 Acquisition Enable
0	Acquisition disabled
1	Acquisition enabled

6.7.9 CR1<08> Channel Mode 12

This bit selects the channel mode of FIFO 1. If single channel mode is selected, only data from channel 1 is stored in FIFO 1, and the maximum acquisition count is 256K samples. If two channel mode is selected, data from both channels 1 and 2 is stored in FIFO 1, and the maximum acquisition count of each channel is 128K samples.

Note: CR1<08> and CR1<09> must be configured before doing a board reset. Also, board reset and ADC reset do not clear these two bits.

When using one or both DDCs attached to FIFO1, it is necessary to enable both ADC1 and ADC2.

CR1<08>	Channel Mode 12
0	Two channel mode (Channels 1 and 2)
1	Single channel mode (Channel 1)

6.7.10 CR1<09> Channel Mode 34

This bit selects the channel mode of FIFO 2. If single channel mode is selected, only data from channel 3 is stored in FIFO 2, and the maximum acquisition count is 256K samples. If two channel mode is selected, data from both channels 3 and 4 is stored in FIFO 2, and the maximum acquisition count of each channel is 128K samples.

Note: CR1<08> and CR1<09> must be configured before doing a board reset. Also, board reset and ADC reset do not clear these two bits.

When using one or both DDCs attached to FIFO2, it is necessary to enable both ADC3 and ADC4.

CR1<09>	Channel Mode 34
0	Two channel mode (Channels 3 and 4)
1	Single channel mode (Channel 3)

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6.8 Control Register 2 (CR2)

Read/Write

The control register allows the user to configure the following operating parameters:

- FIFO 1 level programming enable
- FIFO 2 level programming enable
- DDC channel 1 & 2 enable
- DDC channel 3 & 4 enable
- DDC chip 1, 2, 3 or 4 programming select

The control register bits are discussed in detail below. The reset default for each CR2 bit reflects the bit's state after a hardware PCI Bus reset or software reset via the Board Reset register.

6.8.1 CR2<00> FIFO 1 Programming Enable

This bit enables FIFO 1 almost full / almost empty threshold levels to be programmed. After setting this bit, the levels may be programmed using the FIFO Level Control register. The bit must be cleared after the levels have been programmed.

CR2<00>	FIFO 1 Programming Enable
0	FIFO 1 Programming Disable
1	FIFO 1 Programming Enable

6.8.2 CR2<01> FIFO 2 Programming Enable

This bit enables FIFO 2 almost full / almost empty threshold levels to be programmed. After setting this bit, the levels may be programmed using the FIFO Level Control register. The bit must be cleared after the levels have been programmed.

CR2<01>	FIFO 2 Programming Enable
0	FIFO 2 Programming Disable
1	FIFO 2 Programming Enable

6.8.3 CR2<02> - GC 1 & 2 Enable

This bit enables DDCs 1 & 2. When this bit is set, Digital Downconverters 1 & 2 are enabled, if installed. Data from ADC channels 1 & 2 are fed into the GC4016 DDC chips and the outputs from the DDCs are fed into FIFO 1. When this bit is set to 0, the DDCs are bypassed and data from the ADCs are fed directly into FIFO 1.

When using one or both DDCs attached to FIFO1, it is necessary to enable both ADC1 and ADC2 (CR1<08>).

CR2<02>	GC 1 & 2 Enable
0	DDC 1 & 2 bypassed
1	DDC 1 & 2 enabled

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6.8.4 CR2<03> - GC 3 & 4 Enable

This bit enables DDCs 3 & 4. When this bit is set, Digital Downconverters 3 & 4 are enabled, if installed. Data from ADC channels 3 & 4 are fed into the GC4016 DDC chips and the outputs from the DDCs are fed into FIFO 2. When this bit is set to 0, the DDCs are bypassed and data from the ADCs are fed directly into FIFO 2.

When using one or both DDCs attached to FIFO1, it is necessary to enable both ADC3 and ADC4 (CR1<09>).

CR2<03>	GC 3 & 4 Enable
0	DDC 3 & 4 bypassed
1	DDC 3 & 4 enabled

6.8.5 CR2<07:04> - GC Chip Select

Before writing to the GC4016 control registers, the appropriate DDC/s must be selected using these bits. Only one DDC may be selected at the same time for writing. After the DDCs have been configured, they must be deselected by writing 0000 to these bits.

CR2<07:04>	GC Chip Select
0001	DDC 1 configuration chip select
0010	DDC 2 configuration chip select
0100	DDC 3 configuration chip select
1000	DDC 4 configuration chip select
0000	No DDC selected

6.8.6 CR2<08> - FIFO1 Data Ordering

This bit controls the ordering of data in FIFO1; this feature is only available on later revision boards. When the bit is cleared, the data ordering is as shown in Table 4.4 to Table 4.9 and **Error! Reference source not found.** to Table 3.5. When the bit is set, the ordering is modified within each 64-bit word, as shown by Table 6.5 and Table 6.6 below.

Note: this feature is distinct from the Endian Conversion feature implemented in the PCI Bus interface, and should not be confused with it. The Endian Conversion feature is described in Section 6.3 above.

CR2<08>	FIFO1 Data Ordering
0	Normal ordering (**Error! Reference source not found.** to Table 3.5 and Table 4.3 to Table 4.8)
1	Reversed ordering

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Table 6.5 – FIFO Output Data Ordering for Single Channel ADC Input

Normal FIFO Output Ordering					Reversed FIFO Output Ordering			
D<63:48>	D<47:32>	D<31:16>	D<15:00>		D<63:48>	D<47:32>	D<31:16>	D<15:00>
1	2	3	4		4	3	2	1
5	6	7	8		8	7	6	5
9								9

Note: ADC samples are presented to the FIFO as 16-bit words. This table represents behavior for single channel ADC FIFO input only.

Table 6.6 – FIFO Output Data Ordering for Two Channel ADC Input and All DDC Modes

Normal FIFO Output Ordering			Reversed FIFO Output Ordering	
D<63:32>	D<31:00>		D<63:32>	D<31:00>
1	2		2	1
3	4		4	3
5				5

Note: This table indicates behavior for two channel ADC input and all modes of DDC input. For two channel ADC input, each 32-bit value consists of two 16-bit samples, once from each ADC channel. The ordering within each sample pair is not altered by the FIFO ordering control.

6.8.7 CR2<09> - FIFO2 Data Ordering

This bit controls the ordering of data in FIFO2; this feature is only available on later revision boards. When the bit is cleared, the data ordering is as shown in Table 4.4 to Table 4.9 and **Error! Reference source not found.** to Table 3.5. When the bit is set, the ordering is modified within each 64-bit word, as shown by Table 6.5 and Table 6.6 above.

Note: this feature is distinct from the Endian Conversion feature implemented in the PCI Bus interface, and should not be confused with it. The Endian Conversion feature is described in Section 6.3 above.

CR2<09>	FIFO2 Data Ordering
0	Normal ordering (**Error! Reference source not found.** to Table 3.5 and Table 4.3 to Table 4.8)
1	Reversed ordering

6.9 JTAG Program Register (JTAG_Pro)

Read/Write

This register programs the ICS-554 Xilinx FPGA over PCI Bus rather than using the P6 JTAG port. The register allows the user to configure the following operating parameters:

- Enable programming of the Xilinx FPGA or the EEPROM from PCI bus
- Generation of the JTAG signals TCK, TMS and TDI
- Read JTAG signal TDO

The control register bits are discussed in detail below. The reset default for each JTAG_Pro bit reflects the bit's state after a hardware PCI Bus reset or software reset via the Board Reset register. Before software programs Xilinx FPGA or EEPROM, set JTAG Programming Enable bit to ‘1’. During

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programming Xilinx FPGA or EEPROM, it is recommended that application software only read or write JTAG Program Register. After programming Xilinx FPGA or EEPROM, JTAG Programming Enable bit must be set back to default value '0'.

6.9.1 JTAG_PREG<00> JTAG Programming Enable

This bit enables generation of the JTAG programming signals and read back of TDO over PCI bus. After setting this bit, the Xilinx FPGA or EEPROM may be programmed over PCI bus. The bit must be cleared after programming is complete. The default value of this bit is '0', JTAG Programming Disable.

JTAG_PREG<00>	JTAG Programming Enable
0	JTAG Programming Disable
1	JTAG Programming Enable

6.9.2 JTAG_PREG<01:03> JTAG TCK, TMS, TDI

Application software generates JTAG TCK, TMS and TDI signals by writing these bits through PCI bus to program Xilinx FPGA or EEPROM.

6.9.3 JTAG_PREG<04> JTAG TDO

Application software reads JTAG TDO signal by reading this bit through PCI bus to verify JTAG commands and programming results. This bit is read only.

6.10 ADC 12 Acquisition Count Register

Read/Write

The ADC 12 Acquisition Count register determines the number of frames of data to be stored in the FIFO 1 buffer following each application of trigger, when operating in Capture mode. The value to be programmed to the register is one less than the required number of data frames, when DDCs are disabled. When DDCs are enabled, the value programmed to this register should be the actual frame size. A frame is defined as a block of data containing one or more sample/s or one or more complex sample/s from each active channel at a single point in time. When DDCs are disabled, each frame contains only one ADC sample per channel, as described in Section 3.3 above; data from one or two channels may be stored in the FIFO.

When DDCs are enabled, each frame will be formatted as described in Section 4.15 above; the format varies depending on the DDC operating mode (Wide band, Split-I/Q or Narrow band), and on the number of channels selected for output (see Channel Count register description, Section 6.18 below). When the DDCs are enabled (if installed) by setting CR2<02>, up to 8 output channels may be selected.

When not using DDCs, if FIFO 1 is set for one channel mode (CR1<08> = 0), only channel 1 data is stored, and the acquisition count may be programmed to be in the range 3 – 262143, in steps of 4. If FIFO 1 is set for two channel mode (CR1<08> = 1), data from channel 1 and 2 is stored, and the acquisition count may be programmed to be in the range 1 – 131071, in steps of 2. When DDCs are enabled with more than 2 channels selected for output, this register may be programmed in steps of 1. The rules for programming this register are given below.

When operating in Continuous mode, the Acquisition Count must be set to a non-zero value.

The following expressions show the relationship between the value programmed to the Acquisition Count registers, the operating mode, the frame size and the buffer length.

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Frame Size (16-bit words) = No_Chan x DDC_Mode x Data_Type,

where:

No_Chan	=	number of channels of output to one FIFO (1 or 2 when DDCs disabled, up to 8 when DDCs enabled)
DDC_Mode:		
	1	Disabled
	2	Narrow
	4	Split-I/Q (or complex input)
	8	Wide (or Split-I/Q with complex input)
Data_Type:		
	1	Real Data (DDC enabled or disabled)
	2	Complex Data (DDC enabled only)

Note: Some combinations are not allowed, such as 1-channel real output when DDCs are enabled. Legal combinations are described in Table 4.1 in Section 4.2 above.

Note: For some combinations when DDCs are enabled, data frames contain more than one sample for each output channel (see DDC data frame format descriptions in Section 4.15 above).

The minimum Acquisition Count value that may be programmed is given by:

Min Acq Cnt	=	3 for DDC disabled, one ADC enabled;
	=	1, all other cases
Step size	=	4 for one channel operation, DDC disabled;
	=	2 for two channel operation, DDC enabled or disabled
	=	1 for DDC enabled with more than two channels of output

The maximum Acquisition Count that may be programmed is given by:

Max Acq Cnt = 262144 / Frame Size

The relationship between the Buffer Length or FIFO level value programmed to the FIFO Level Control register (see Section 6.14) is given by:

BL (64-bit words) = Acq Cnt x Frame size (16-bit words) / 4

6.11 ADC 34 Acquisition Count Register

Read/Write

The ADC 34 Acquisition Count register determines the number of frames of data to be stored in the FIFO 2 buffer following each application of trigger, when operating in Capture mode. The value to be programmed to the register is one less than the required number of data frames, when DDCs are disabled. When DDCs are enabled, the value programmed to this register should be the actual frame size. A frame is defined as a block of data containing one or more sample/s or one or more complex sample/s from each active channel at a single point in time. When DDCs are disabled, each frame contains only one ADC sample per channel, as described in Section 3.3 above; data from one or two channels may be stored in the FIFO.

When DDCs are enabled, each frame will be formatted as described in Section 4.15 above; the format varies depending on the DDC operating mode (Wide band, Split-I/Q or Narrow band), and on the number of channels selected for output (see Channel Count register description, Section 6.18 below). When the DDCs are enabled (if installed) by setting CR2<03>, up to 8 output channels may be selected.

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When not using DDCs, if FIFO 2 is set for one channel mode (CR1<09> = 0), only channel 3 data is stored, and the acquisition count may be programmed to be in the range 3 – 262143, in steps of 4. If FIFO 2 is set for two channel mode (CR1<09> = 1), data from channel 3 and 4 is stored, and the acquisition count may be programmed to be in the range 1 – 131071, in steps of 2. When DDCs are enabled with more than 2 channels selected for output, this register may be programmed in steps of 1. The rules for programming this register are given below.

The ranges of values that may be programmed to this register according to the number of channels selected are the same as for the ADC 12 Acquisition Count register. See the expressions given in Section 6.10 above.

6.12 ADC 12 Decimation Register

Read/Write

The ICS-554 includes a programmable decimation feature independent of the DDCs. This feature may be used to decimate the output data stream by a factor of N. No filtering is applied to the decimated data stream. The feature should not be used when the DDCs are enabled.

This register is used to set the decimation factor for ADC channels 1 and 2. Decimation is done by periodically discarding a specified number of samples from each channel at the output of the converters, before the samples are written to the FIFO. The decimation is applied equally to data from ADC channels 1 and 2.

The register allows the user to specify the decimation factor in the range 1 to 32. If a value (N-1) is programmed to the register, the board will reject (N-1) out of every N samples before placing them in the buffer. This effectively reduces the output rate by a factor of N. the range of values that may be programmed is therefore 0 – 31, inclusive.

For example, when the value 0 is programmed, no decimation takes place. When the value 1 is programmed, every second data frame is discarded.

The Decimation register must be programmed with the value 0 when the DDCs are enabled.

6.13 ADC 34 Decimation Register

Read/Write

The ICS-554 includes a programmable decimation feature independent of the DDCs. This feature may be used to decimate the output data stream by a factor of N. No filtering is applied to the decimated data stream. The feature should not be used when the DDCs are enabled.

This register is used to set the decimation factor for ADC channels 3 and 4. Decimation is done by periodically discarding a specified number of samples from each channel at the output of the converters, before the samples are written to the FIFO. The decimation is applied equally to data from ADC channels 3 and 4.

The register allows the user to specify the decimation factor in the range 1 to 32. If a value (N-1) is programmed to the register, the board will reject (N-1) out of every N samples before placing them in the buffer. This effectively reduces the output rate by a factor of N. the range of values that may be programmed is therefore 0 – 31, inclusive.

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For example, when the value 0 is programmed, no decimation takes place. When the value 1 is programmed, every second data frame is discarded.

The Decimation register must be programmed with the value 0 when the DDCs are enabled.

6.14 FIFO Level Control Register

Write Only

This register allows the user to program the levels for the FIFO1 and FIFO2 programmable almost full (PAF) and programmable almost empty (PAE) flags. The values assigned to these levels determine the FIFO data levels at which the Status register FIFO1 PAF, FIFO2 PAF, FIFO1 PAE and FIFO2 PAE flags will be set or cleared. They also determine the levels at which the ADC12 IRQ and ADC34 IRQ interrupts occur, since these are triggered from the FIFO1 PAF and FIFO2 PAF flags.

The level values are programmed by writing a 32-bit programming word to this register. The PAE value is contained in the least significant 16 bits in the 32-bit word, while the PAF value is contained in the most significant 16 bits. The range of values that can be programmed for each parameter is therefore 0 – 65533, corresponding to the number of 64-bit words in the FIFO at which the level is set, less two. The value programmed to the PAF level sets the length of free space below the full state of the FIFO (i.e. the difference between the full and almost full levels), while the value programmed to the PAE level sets the length of filled space above the empty state of the FIFO (i.e. the difference between the empty and almost empty levels). Data is written serially to the FIFO, least significant bit first. One write must occur for each bit of data to be written to the FIFO, with the data to be programmed in bit 0 of the FIFO level control register.

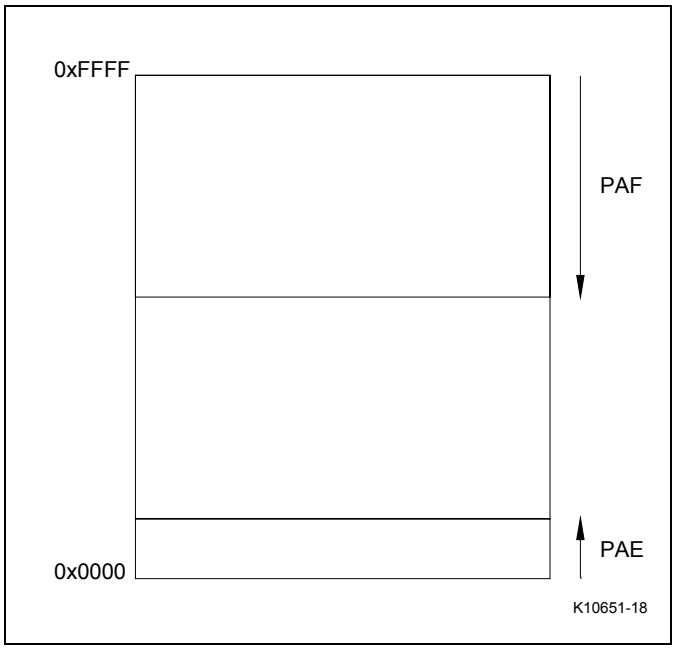


Figure 12 - PAF/PAE Buffer

Since the almost empty condition is not usually of interest to the user, and can not generate an interrupt, the value programmed is not important. However, the almost full level must be carefully selected, since the optimum setting will be determined by several factors. The PAF level must be programmed with the number of 64-bit words to be acquired in the FIFO buffer prior to each interrupt or to completion of acquisition. The ADC interrupt request will occur each time the FIFO fills to the PAF level. When operating in Capture mode, the

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value programmed must be an integral multiple of the Acquisition Count (see Section 6.10 above). When the ADC interrupt occurs, the user may read data to the programmed length (= PAF level), but not more.

In general, the PAF level should be set as high as possible, since it determines the length of data that can be read from the module in each DMA transfer. Increasing the size will result in more efficient transfers and greater throughput. However, setting the PAF level to near to the FIFO full condition (i.e. 0xFFFF) may result in FIFO overflow on systems that have poor or variable interrupt latency. In particular, this applies to non-real time systems such as Windows. Note that data is written to the FIFO in frames; the frame size is determined by the mode of operation (DDCs enabled or disabled, DDC mode, number of channels of output, complex or real data). In general, for maximum efficiency, the PAF level should be set to a multiple of the frame size, less two. The frame size can be as small as one quarter of a 64-bit word, for one channel output without DDC, or as large as 8 x 64-bit words for 8 channels of complex data.

Example: Program the FIFO1 programmable full (i.e. the ADC channel 1 & 2 buffer length) level to 90% of the FIFO size, and the programmable empty flag to 2 (minimum value possible). Calculate 90% of the FIFO size:

65535 64-bit words x (1 - .90) = 6553.5

Round this up to the nearest integer multiple of 8 (to allow for 8-channel complex output) for a value of 6560. The value to be programmed is two less than this for a value of 6558.

The hexadecimal equivalent of this number is 0x199E. The programming word required is therefore 0x199E0000. To program the data, set CR2<00> to select the FIFO1 chip, and write 0x199E0000 to the register. This is performed by a one bit write, 32 times, shifting the data right by one bit after each write.

The user must perform an ADC Reset (by writing to the ADC Reset register) after writing to the FIFO Level Control, Acquisition Count and Decimation registers in order for the new values to take effect.

Please note that the Buffer Length Set functions of the API (see Reference [1]) automatically set the PAE and PAF levels based on the desired buffer length.

6.15 Trigger Register

Write only

A write to this register causes acquisition to start if internal trigger is selected (by clearing CR1<01>). The data written to the register is unimportant. ADC channel 1 & 2 or ADC channel 3 & 4 must have been enabled previously. If J3 pins 2 and 3 are connected, the internal trigger signal will be available at the TRIG connector.

When Capture mode has been selected (CR1<04>), writing to this register will cause data acquisition to begin, and continue until the programmed aquisition count value has been reached. The board may be triggered multiple times in this way, until the total amount of data acquired is equal to the programmed buffer length. When this occurs, an ADC interrupt will occur, if enabled.

When Continuous mode has been selected (CR1<04>), writing to this register will cause data acquisition to begin, and continue until the module is disabled by clearing CR1<06> and/or CR1<07>.

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6.16 ADC Reset Register

Write only

A write to this register initializes memory pointers. It does not alter memory contents or the values of control registers. The data written to the register is unimportant. The register should be written to after the board is configured and before acquisition is started.

After writing to this register, a delay of at least one microsecond is required before the ICS-554 is triggered, to allow time for the DLL clock manager located in the Xilinx FPGA to lock, otherwise the data read from the board may be corrupted. The user may perform other board configuration activities immediately after writing to this register.

6.17 Board Reset Register

Write only

A write to this register masks all interrupts, resets all control register bits to their power-up defaults (zero) and resets all on-board memory except CR1<08> (channel mode 12) and CR1<09> (channel mode 34). QL5064 registers and status are unaffected. The data written to the register is unimportant. The register should only be written in order to perform a complete reset of the board prior to changing the board configuration.

Note: CR1<08> (channel mode 12) and CR1<09> (channel mode 34) must be configured before writing to this register. Board Reset and ADC Reset do not clear these two bits, and a board reset is required to load the values programmed to these bits to the FIFOs.

6.18 Channel Count Register

Read / Write

This register is used to specify the output data format when the optional DDCs are used. It is not necessary to program the register if the DDCs are not enabled. Please refer to Section 3.3 for information concerning the use of ADC data output format. Table 6.7 discusses the number of channels stored in FIFO1 or FIFO2. The FIFOs can be used separately or together for channel storage.

6.18.1 CC<03:00> - Channel Count 12

When DDCs 1 and 2 are enabled (CR2<02>), this field selects the output data format. The value to be programmed must be one less than the number of output channels required. Depending on the operating mode, only certain values are allowed, as shown in see Table 6.7. The output data formats are as shown in Section 4.15 above.

Note that the number of DDC output channels that can be selected is variable, depending on the mode of operation of the DDCs. Channels are always enabled in order starting with the lowest numbered DDC on the first chip, and proceeding with all DDCs on the first chip before assigning the first DDC on the second chip. For example, when 2 channel narrow band operation with complex output data is selected by programming the value 4 to Channel Count 12, the DDCs used will be Chip 1 DDC A and Chip 1 DDC B.

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6.18.2 CC<07:04> - Channel Count 34

When DDCs 3 and 4 are enabled (CR2<03>), this field selects the output data format. The value to be programmed must be one less than the number of output channels required. Depending on the operating mode, only certain values are allowed, as shown in see Table 6.7. The output data formats are as shown in Section 4.15 above.

Note that the number of DDC output channels that can be selected is variable, depending on the mode of operation of the DDCs. Channels are always enabled in order starting with the lowest numbered DDC on the first chip, and proceeding with all DDCs on the first chip before assigning the first DDC on the second chip. For example, when 2 channel narrow band operation with complex output date is selected by programming the value 4 to Channel Count 34, the DDCs used will be Chip 3 DDC A and Chip 3 DDC B.

Table 6.7 - Programming of Channel Count Values

DDC Mode	Channel Count 12 or 34 (N)	Data Stored in FIFO1 or FIFO2
Narrowband complex output	2,4,6,8,10,12,14,16	N/2 channels complex data.
Narrowband real output	2,4,6,8	N channels real data.
Split-I/Q complex output	8,16	N/4 channels complex data.
Split-I/Q real output	4,8	N/2 channels real data.
Wideband complex output	8,16	N/8 channels complex data.
Wideband real output	4,8	N/4 channels real data.
Narrowband pairs of complex input & complex output	8,16	N/4 channels complex data.
Narrowband pairs of complex input & real output	4,8	N/2 channels real data.
Split-I/Q complex input & complex output	8,16	N/8 channels complex data.
Split-I/Q complex input & real output	4,8	N/4 channels real data.

6.19 Programming the DDC Modules

As an option, the ICS-554 is available with up to four GC4016 DDC devices installed, one for each A/D channel (models ICS-554v-w-MN(y) Rev.z). Each of the four devices has an identical register set, and is independently programmed. The registers for programming these devices are located at PCI Bus address PCI_BASE1 + 0x0100 (see Table 6.2 above); the same register set is used for programming each of the four devices. The device to be programmed (ADC channel 1, 2, 3 or 4) must be selected using CR2<07:04> before programming. After the device has been programmed, CR2<07:04> must be cleared.

The user should not attempt to operate the ICS-554v-w-MN(y) Rev.z without configuring all four GC4016 down converters, since the results may be unpredictable.

Since the DDCs are divided into two groups of two GC4016 chips, one group feeding each of the two FIFO buffer memories, the two groups may be configured to operate with different bandwidths (output rates, decimation factors) and modes. For example, it is possible to set the upper 8 downconverter channels as 16 narrow band channels with real output data, while setting the lower 8 downconverter channels as 4 wide band channels with complex output data.

The GC4016 register set is divided into global registers and paged registers. Global registers apply to all four channels of each chip, and are accessible regardless of which page has been selected for access. Access to any of the paged register set requires that the page number be programmed to the Page

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register of the Global register set before any access is made to a paged register, in order to select the required page.

The programming details are not described here, since they are fully described in the Graychip data sheet, Reference [5], available from the Graychip web site. Users should follow the recommendations given there for the values to be programmed to each register. However, notes are given below on required programming with respect to the ICS-554 implementation, and where the default programming values given in the Graychip documentation should be modified.

In the Graychip documentation, the registers are given an address value ranging from 0 – 31. Each register is a single byte, and is mapped to the least significant 8 bits of a single 64-bit PCI Bus address. The required offset for any register in PCI address space is therefore computed by mutliplying the GC4016 register address by 8 and adding it to PCI_BASE1 + 0x100. Register 0 –15 are the global registers, while registers 16 – 31 are the paged registers, accessible on 98 different pages. The required page must be selected before attempting to read or write to the paged registers.

The output data from the GC4016 DDCs is formatted in the Xilinx FPGA. The formatting applied depends on the number of output channels required. A single register located in the FPGA, the Channel Count register must be programmed to select the data output format when the DDCs are enabled.

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7 TECHNICAL SUPPORT

Technical support for this product is available through ICS using the contact information given below.

When requesting technical support, please provide the following information:

- Product name - ICS-554 specific model and custom core (HDK-554/xxx number), if applicable.
- Serial number of board (of the form 31425, given on a bar code label located on the board)
- Equipment Number (Equ No. of the form 10987654, given on the board equipment number label)
- Software device driver used, if any (e.g. Windows, Linux or VxWorks driver).
- Installation environment – type of chassis, type of CPU, other boards installed.
- Nature of problem.

You may contact ICS Technical Support at:

Address: ICS Ltd.
Attn. Technical Support
5430 Canotek Road
Ottawa, Ontario
K1J 9G2

Phone: 613-749-9241 or (USA) 800-267-9794
Fax: 613-749-9461
Web: http://www.ics-ltd.com
E-mail: support@ics-ltd.com

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8 REFERENCES

1. ICS-554 Windows Software Development Kit User's Manual, Document Number E10713, Interactive Circuits and Systems Ltd., Ottawa

2. IEEE 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC, IEEE, 2001

3. PCI Local Bus Specification Revision 2.2 December 18, 1998

4. QL5064 Production Information, QuickLogic, http://www.quicklogic.com

5. GC4016 Multi-Standard Quad DDC Chip DATA SHEET Rev 1.0 August 27, 2001 (SLWS133A), http://www.ti.com/graychip

6. Xilinx Virtex-II product documentation, http://www.xilinx.com

7. ICS-554 Hardware Development Kit User's Manual, Document Number E10753, Interactive Circuits and Systems Ltd., Ottawa

8. HDK-554-R Custom FPGA Core User's Manual, Document Number E10830, Interactive Circuits and Systems Ltd., Ottawa

9. Performance of 14-Bit Data Converters for Software Radio Applications, Document Number AN-SR-2, Interactive Circuits and Systems Ltd. Application Notes, http://www.ics-ltd.com

10. Power and Cooling, http://www.antec-inc.com/

11. Power and Cooling, http://www.thecardcooler.com/

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APPENDICES

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APPENDIX A TYPICAL ORDER OF OPERATIONS FOR SIMPLE ACQUISITION

1. Configure jumpers to desired master/slave and internal/external clock and trigger configuration. Install ICS-554 in chassis.
2. Set channel mode control register bits CR1<08> and CR2<09>.
3. Reset board; clears control registers except CR1<08> and CR2<09>.
4. Set control register:
   - Select clock source (internal or external).
   - Select trigger source (internal or external).
   - Select external trigger edge if external trigger used.
   - Select Sync source (if use Tuner).
   - Select operation mode (capture or continuous).
   - Enable Tuners (if use Tuner).
5. Set decimation.
6. Set acquisition count.
7. Set buffer length.
8. Configure tuner module if use tuners.
9. Reset ADC (loads acquisition count, FIFO reset)
10. Set enable bit in control register.
11. If using internal trigger, writing trigger register, or wait for external trigger to occur.
12. Wait for interrupt from ICS-554 ADC 1&2 or ADC 3&4.
13. Read back acquired data.
14. If using continuous mode:
15. IF enough data acquired, disable acquisition.
16. ELSE repeat steps 12…14.
17. If using capture mode:
18. IF enough data acquired, disable acquisition.
19. ELSE repeat steps 9…17.

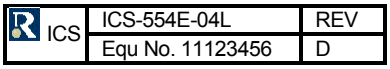
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APPENDIX B BOARD REVISIONS

The board revision is indicated on the product label, located on the ICS-554 board. There are two examples of product labels shown here:





On the ICS-554A, ICS-554B, and ICS-554C, for board revisions J (REV. J) and later, the FIFO full flags are latched and must be proactively cleared by writing '1' to them. They are also cleared on Board reset and ADC reset. For previous revisions (REV. H and earlier) of the ICS-554A, ICS-554B, and ICS-554C, the bit is not latched; it will clear when the FIFO level falls below the full level.

On the ICS-554D and ICS-554E, for board revisions D (REV. D) and later, the FIFO full flags are latched and must be proactively cleared by writing '1' to them. They are also cleared on Board reset and ADC reset. For previous revisions (REV. C and earlier) of the ICS-554D and ICS-554E, the bit is not latched; it will clear when the FIFO level falls below the full level.

If further information is required, please contact Technical Support.

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APPENDIX C ICS-554D/E LVDS PN4 CONNECTIONS

The ICS-554D and ICS-554E support the ordering option of LVDS compatible Pn4 connections. Figure 13 is a high level diagram of the FPGA and how it is configured to support LVDS signaling.

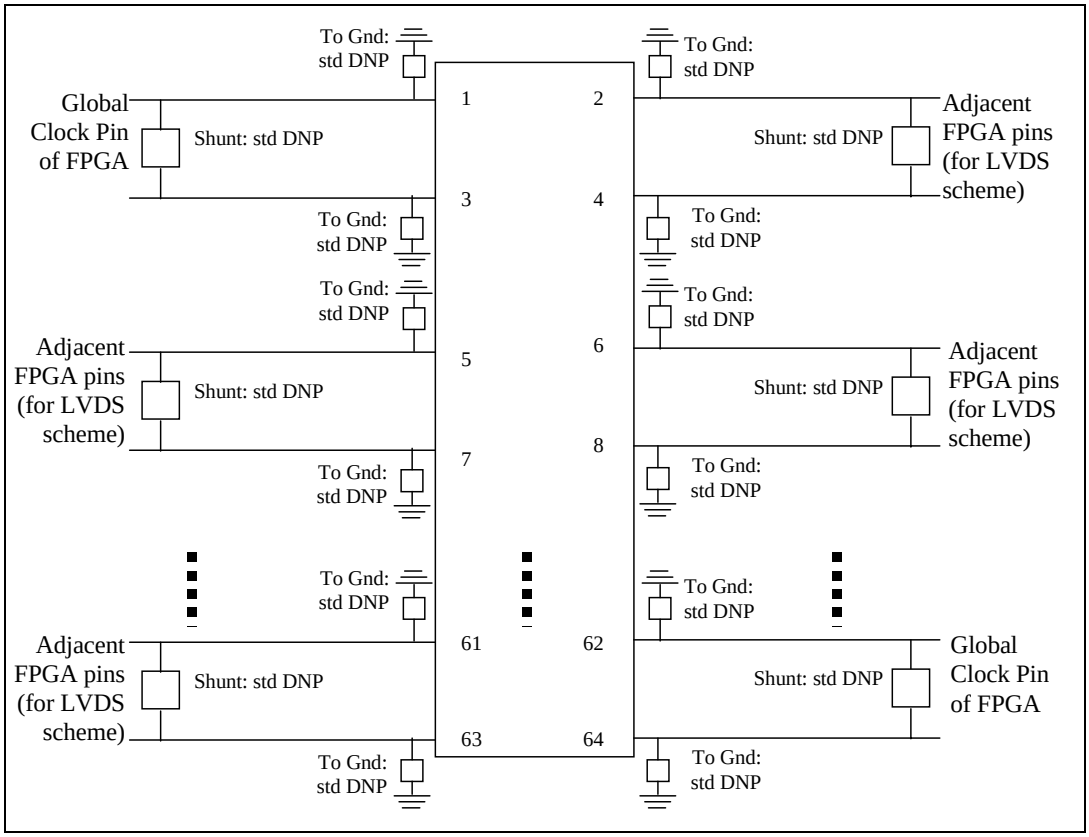


Figure 13 - Pn4 User I/O Connection for LVDS Signaling

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