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Find the *Abaco Systems / SBS ASF-PMC-1* at our website: *Click HERE*

ASF - PMC
1553 Interface

Features:

One Dual Redundant 1553 Channel Featuring 100% Independent Operation as a:
Bus Controller or
Remote Terminal or
Dual Function Bus Monitor

- **Bus Controller**
  Programmable Frame Lists
  BC - RT, RT - BC, RT - RT
  Mode Codes, Broadcasts, Time Delays

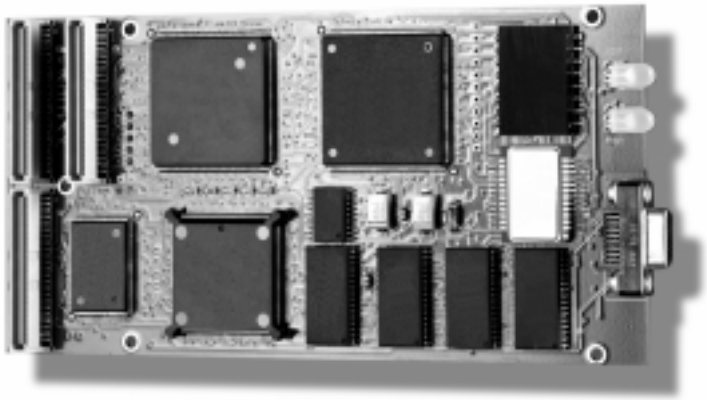
- **RT Functionality**
  RT Level Protocol Selection
  Definition Tables
  Programmable Response Time

- **Bus Monitor**
  Map Monitoring
  Sequential Monitoring
  Time Stamped, Double Buffered
  Error Tables & Definable Monitoring

- **Architecture**
  On-The-Fly Data Structures
  BC & RT Link Lists
  High Speed DSP
  Flexible Memory Structure
  Flash Memory

- **Mezzanine Card**
  IEEE P1386 Compliant

- **Software Support**
  No Cost Drivers & Libraries
  Including Source Code



The ASF-PMC (PCI Mezzanine Card) interface provides a flexible, single function, dual redundant MIL-STD-1553 interface to the PCI Mezzanine. This Advanced Single Function Interface (ASF) architecture provides independent operation of a Bus Controller (BC), or Remote Terminal (RT), or dual function Bus Monitor (BM). The ASF-PMC interface equips the PMC carrier with a complete 1553 interface, including 1553A and/or 1553B selections, programmable BC frame lists, BC scheduling capabilities, RT response tables, pointer driven transmit and receive buffers, Map Monitoring, 100% Independent Sequential Bus Monitoring and extensive programmable event interrupts.

BC simulation structures consist of linked lists of 1553 command messages: BC-to-RT, RT-to-BC, RT-to-RT, mode code, broadcast and time delay block transmissions. RT simulation is defined by a simple series of pointers to RT definition tables which subsequently point to control data buffers. Bus activity to be monitored is definable in both the Map and Sequential monitoring modes, providing user defined linked lists of data buffers and sequential, time stamped and double buffered 1553 activity respectively. Both monitoring modes perform broad error monitoring, and provide a comprehensive error table that can be read at any time by the host processor.

Hardware Overview

The ASF interface is based upon an advanced high speed DSP, programmable logic and dual port Flash RAM to deliver a highly reliable hardware platform that is feature rich and user friendly. Through the 128K bytes of dual port RAM, the host processor has access to set up, monitor, and change the 1553 interface data structures at any time. Link-list memory architecture allows the user to structure interface memory usage for the maximum in flexibility and usefulness.

Software Support Overview

SBS distributed software includes host processor device drivers to the dual port control and data structures, as well as, an application layer to these structures. Low level drivers and C libraries with source code are provided with the interface, at no cost.

2400 Louisiana Boulevard NE, #5-600, Albuquerque, NM 87110 • 1-800-SBS-1553 • 1-800-DATABUS
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ASF - PMC
Interface Specifications

ASF Functionality:

Bus Controller (BC)

- BC Retry
- Minor Frame Timing and Message Scheduling
- Intermessage Gap Selectable
- Programmable Delay Gaps and Null BC Blocks
- Multiple BC Data Buffers in a Link-List Structure
- Programmable RT No-Response Time-Out

Remote Terminal (RT)

- RT and All Subaddresses Supported
- Transmit/Receive Buffers for Each Subaddress
- Multiple RT Data Buffers in a Link-List Structure
- Programmable RT Response Time and No-Response Selection

Map Monitoring

- Multiple Linked Buffers for Each Transmit/Receive Subaddress
- Mapped Buffers Read by Host Processor as Time Permits
- Number of Buffers per Transmit/Receive Subaddress is Programmable or User Definable to Account for Various Host Speeds

Sequential Monitoring

- Host Driver Selected Messages are Double Buffered
- Messages Timed Stamped
  1 µSec 32 bit Clock or
  48 bit IRIG-B Clock *(available on request)*
- Standard Firmware Performs Broad Error Monitoring
- Comprehensive Error Table Readable at Any Time by Host Processor

Self Test:

- Power-up Test with Status Register Report
- BIT - RAM and Encoder/Decoder Test
- Run-time Health Status Register
- "Unit Test" Program for 1553 Bus Functionality

Multi-Purpose I/O:

- Bi-directional External Trigger
- IRIG Clock Input *(optional)*
- External TTL/RS-422 System Clock Input

PMC Functionality:

- PCI Bus is 2.1 Compliant
- 50 Mbyte per Second Max. Transfer Rate
- 16 Bit & 32 Bit Transfer Modes
- Memory Mapped
- Programmable DMA Controller
- Onboard Firmware Storage via Flash Memory

PCI Mezzanine Connection:

- IEEE P1386 PMC Connection
- PMC P4 to VMEbus P2 Support

Interface Connections:

- µMin $DB15_F$ to Coupling Harness (CA-2189)
- Coupling Harness to Bus and I/O Connectors
- DBI/O Connector
- $BJ77_F$ Triax Connector to 1553 Bus

Interface Card Specifications:

- Maximum Power Consumption (98% Bus Activity) - Single Channel:
  5V @ 1.5 Amps (1.0 Amps with Bus Inactive)
- Standard Commercial Temperature:
  0° C to +60° C
  ≤ 95% rH non-condensing
- Mechanical:
  Standard PMC Card
  Dimensions: Length 6.0" Width 2.9"

Software & Documentation Support:

- Low Level Drivers & C Library Sets with Source Code
- Borland and Microsoft C Compiler Compatible
- Hardware and Library Manual Set

Customer Support:

- Full One Year Warranty
- Extended Warranties Available
- Driver and Library Upgrades
- Over 18 Operating Systems Supported on Various Platforms

Interface Model Numbers:

- **ASF-PMC-1** Single Channel 1553 to PMC Interface

SBS guarantees a successful integration which includes no-cost phone, e-mail and ftp support, with on-site customer visits as necessary.

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