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Find the *Abaco Systems / SBS / Greenspring IP-Altera / IP-Altera-RO* at our website: *Click HERE*

IP-ALTERA

Customizable EIA-422/TTL IndustryPack with Altera Design File-Set

Features

- Single-wide IndustryPack
- 28 lines of digital I/O
- Altera design file set
- 6-foot 50-pin cable
- Terminal block

IP-Altera is a single-wide IndustryPack with 28 lines of digital I/O. It comes with a complete Altera design file-set that can be used as an effective starting point for customers implementing their own custom digital interface or protocols in Altera logic. It is ideally suited for interfacing to systems using non-standard communication protocols such as satellite and other aerospace test systems. It can also be used to emulate prototype hardware for early software development and system integration.

IP-Altera uses an Altera 10K40-3 FPGA with 20 differential I/O lines and 8 digital TTL I/O lines. Users must have their own Altera Development System to implement their own designs. SBS provides the Altera design for the IndustryPack bus control interface, an example of digital I/O, an interrupt implementation, and ID PROM. The 10K40 has 40,000 typical gates and has an internal 16K bit block of RAM. This is independent of the logic and may be used as RAM, ROM, FIFO, or functions such as multipliers, vector scalars, and error correction circuits. The 10K40-3 supports the 32 MHz IP Specification with one wait state.

The direction of each of the I/O lines is programmable. Each of the differential lines has a separate output enable bit while the TTL lines may use tri-state buffers. The TTL lines use SBS' LineSafe ESD protection circuit. The differential lines have socketed termination resistors, with 100 Ohm resistor networks installed as the factory default. A 1.5 volt reference output is provided on one of the I/O pins. This allows the differential receivers to be used as TTL inputs by connecting the minus side of the input to the reference.

The IP has a socket for quarter size crystal oscillator. The output of this runs to one of the global clock inputs in the 10K40, allowing users to use custom frequencies in their design. The IP also has an external RC network which may be used to determine the IP clock frequency.

A 3 1/2 inch high density floppy disk, included with IP-Altera, contains the following:

- Altera 7.1 basic design schematic;
- Altera 7.1 ACF file for placing the basic design;
- Altera 7.1 simulation of the basic design;
- Altera 7.1 simulation vector files for all supported IP Cycles.

Also included with the IP-Altera design kit is a 6-foot 50-pin ribbon cable and terminal block, a printed copy of the board schematics and Altera design files, and board assembly drawing.

Purchase of IP-Altera entitles the customer to a royalty-free license to use and modify the provided design.

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Specifications

Size	Single Wide IndustryPack.
Conformance	ANSI/VITA-4, IP-Modules
Digital Interface	28 digital signal lines. Each signal line is either an input or an output. 8 or 32 MHz IP interface
Interface Level	20 differential I/O lines with 100 Ohm termination resistors. 8 TTL I/O lines with 10 K Ohm pull up resistors. Each TTL I/O line has a LineSafe ESD filter. 12 mA current sink, 4 mA current source typical. One 1.5V reference, 1 ground pin.
IP Cycles Supported	I/O, Memory, ID, DMA and Interrupt.
Interrupts	Two supported, IntReq0*, IntReq1*.
DMA	Two channels supported, DMAReq0*, DMAReq1*.
Access Mode	Byte or word in I/O, Memory, ID and Interrupt Space.
Wait States	Zero for 8 MHz and one for 32 MHz as delivered; user programmable.
ESD Protection on TTL Lines	Measured per IEC 1000-4-2 level 4, 8 KV contact discharge, 15 KV air discharge.
Power Requirements	+5.0 VDC

Order Information

IP-ALTERA-IP	Altera FPGA & design files with flat ribbon cable and IP-Term-IP50
IP-ALTERA-HD50	Altera FPGA & design files with high density cable and IP-Term-HD50
IP-ALTERA-CM50	Altera FPGA & design files with champ cable and IP-Term-HD50
IP-ALTERA-RO	IP-ALTERA repeat orders
IP-ALTERATTL-IP	Altera FPGA with TTL I/O and design files
IP-ALTERATTLRO	Altera FPGA with TTL I/O – hardware only repeat orders

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