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IP-DAC

Six-Channel 12-Bit
Digital to Analog Converter
IndustryPack®

User Manual

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IP-DAC
Six-Channel 12-bit
Digital to Analog Converter
IndustryPack®

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Product Description

The IP-DAC provides six channels of 12-bit digital to analog conversion on a single-wide IndustryPack®. Any one of five output ranges may be selected individually for each DAC channel via shunts. A single high precision (3ppm/°C) reference provides exceptional stability. Alternatively, an external reference may be provided.

Each of the six channels is factory-calibrated and the offset and gain correction factors are stored in the ID PROM. Software may use this calibration information to provide output voltages accurate to within 1 least significant bit (LSB).

Key Features

- Six 12-bit DACs on a single-wide IndustryPack®
- Output ranges of -5, -10, 5, 10, ±2.5, ±5, and ±10 V individually selectable per channel
- 20 us settling time for 10 V output step
- Factory-calibrated; data in ID PROM
- High-precision reference
- Sense input for each channel
- Simple 16-bit software interface

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VMEbus Addressing

IP-DAC is accessed by 16-bit words only. It can be accessed in either the I/O space or the memory space.

Figure 1 below shows the memory map of the IP-DAC.

Address	DAC
base + 00	DAC channels 1 and 2
base + 02	DAC channel 2
base + 04	DAC channel 1
base + 08	DAC channels 3 and 4
base + 0A	DAC channel 4
base + 0C	DAC channel 3
base + 10	DAC channels 5 and 6
base + 12	DAC channel 6
base + 14	DAC channel 5

Note: All accesses are word-wide (16-bit) writes. Byte writes will not respond. All reads acknowledge, but the data is undefined.

Figure 1. Memory Map of IP-DAC on VMEbus

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DAC Output

Each of the 6 DACs can be set to any of 10 output ranges. Each DAC has it own output configuration block. These six configuration blocks are physically identical to assist in rapid selection.

Figure 2 lists the 10 output range options and shows their implementation via 4 shunts labeled A, B, C, and D.

Voltage Range	Shunt A	Shunt B	Shunt C	Shunt D	Note
0 to +5	1-2	OUT	IN	IN	CT*
0 to +10	1-2	OUT	OUT	IN	Cal*
–2.5 to +2.5	1-2	IN	IN	IN	
–5 to +5	1-2	IN	OUT	IN	Cal*
–10 to +10	1-2	IN	OUT	OUT	
0 to –5	2-3	OUT	IN	IN	
0 to –10	2-3	OUT	OUT	IN	
+2.5 to –2.5	2-3	IN	IN	IN	
+5 to –5	2-3	IN	OUT	IN	
+10 to –10	2-3	IN	OUT	OUT	

Note:
Cal* means that the range is both calibrated and recommended for voltage output.
CT* means that the range is calibrated and required for current transmitters.

Figure 2. DAC Output Range Selection

As indicated in Figure 2 and discussed in the Accuracy and Calibration section of this manual, only those output ranges with a 10-volt span are fully calibrated and recommended for use.

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Figures 3, 4, and 5 illustrate the output range selection shunts. Shunt A in the 1-2 position selects the + 5V reference as input to the DAC. Shunt A in the 2-3 position selects the -5V reference as input to the DAC. (Note: This option is not available if Remote Reference is used. For more information, please refer to the User Options section of this manual.) Shunt E is used for Remote Sense and is discussed in the User Options section of this manual.

Figure 3 illustrates how these shunts are physically arranged in each configuration block.

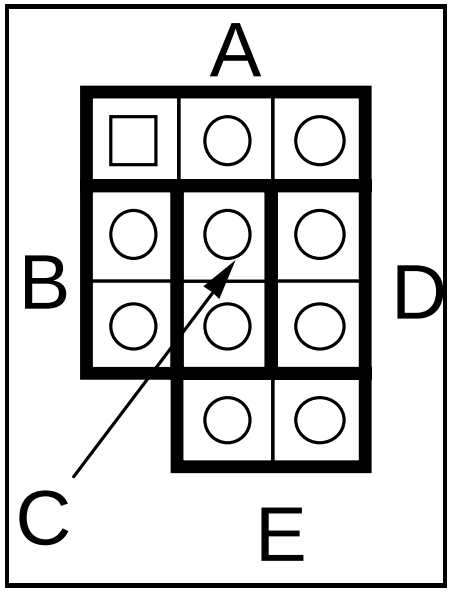


Figure 3. Range Selection Shunt Detail

Figure 4 illustrates the factory-default -5V to + 5V output range selection.

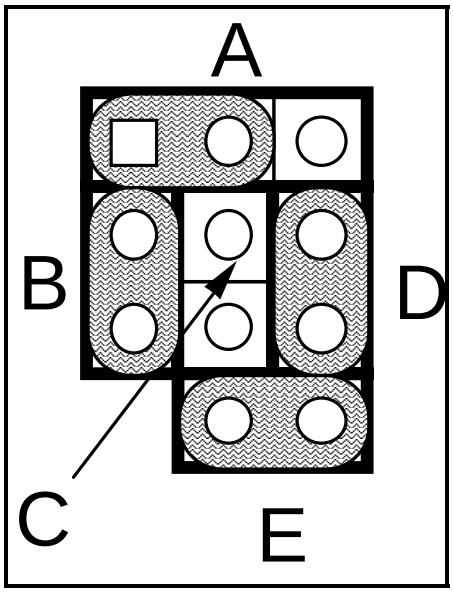


Figure 4. Default -5 to + 5 Range Shunt Detail

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Figure 5 shows the location of each of the six blocks on IP-DAC.

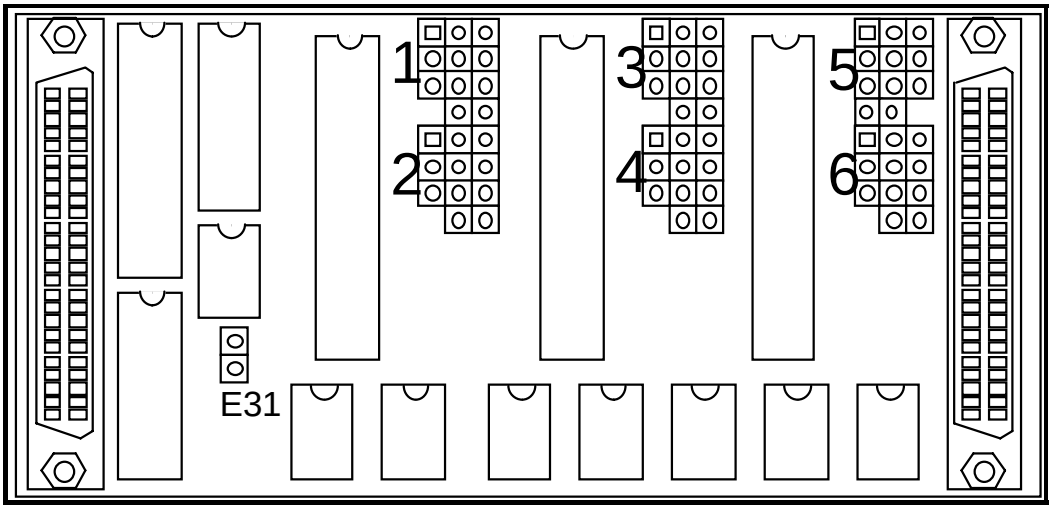


Figure 5. Range Selection Shunt Locations

Figure 6 lists additional output range information. Unipolar range means that a write of $000 to the DAC produces 0 volts at the output pin. A write of $FFF (decimal 4095) produces the maximum positive voltage.

Bipolar output means that a write of $000 produces the maximum negative voltage, a write of $800 produces zero volts, and $FFF produces the maximum positive voltage.

Inverted output means that a write of $000 produces zero output voltage and a write of $FFF produces the maximum negative voltage.

Ones-complement output is a bipolar range that uses $000 for the most positive output voltage, $800 for zero volts, and $FFF for the maximum negative voltage.

For more information on calibration, refer to the Accuracy and Calibration section of this manual.

Voltage Range	Type	Span	Calibrated
0 to +5	unipolar	5V	-
0 to +10	unipolar	10V	YES
–2.5 to +2.5	bipolar	5V	-
–5 to +5	bipolar	10V	YES
–10 to +10	bipolar	20V	-
0 to –5	inverted	5V	-
0 to –10	inverted	10V	YES
+2.5 to –2.5	ones-complement	5V	-
+5 to –5	ones-complement	10V	YES
+10 to –10	ones-complement	20V	-

Figure 6. DAC Output Type Detail

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Figure 7 lists the value in volts of 1 LSB for each output range. A 12-bit DAC provides 4096 discreet output values, from 0 times 1 LSB to 4095 times 1 LSB. The actual output (assuming no error) is also listed in Figure 7.

The calibration values in the on-board PROM use the actual range given in Figure 7's rightmost column as the target. For additional information regarding these calibration values, refer to the ID Prom and Accuracy and Calibration sections of this manual.

Nominal Range	LSB value	Span	Actual Range
0 to +5	1.2207 mV	5V	0 to +4.9988
0 to +10	2.4414 mV	10V	0 to +9.9976
-2.5 to +2.5	1.2207 mV	5V	-2.5 to +2.4988
-5 to +5	2.4414 mV	10V	-5.0 to +4.9976
-10 to +10	4.8828 mV	20V	-10.0 to +9.9951
0 to -5	1.2207 mV	5V	0 to -4.9988
0 to -10	2.4414 mV	10V	0 to -9.9976
+2.5 to -2.5	1.2207 mV	5V	+2.5 to -2.4988
+5 to -5	2.4414 mV	10V	+5.0 to -4.9976
+10 to -10	4.8828 mV	20V	+10.0 to -9.9951

Figure 7. DAC Actual Output Detail

Each DAC uses two op-amps to produce its output. The first op-amp converts the DAC's output current to a voltage, and the second implements the user-selected output range options. The Bi-CMOS op-amps used (AD648) are versatile and rugged. They can drive to the positive voltage rail (nominally + 12 volts) and within two volts of the negative voltage rail. Their exceptionally low drift makes them ideal for a high-precision calibrated IP-DAC. They have a rated short circuit current of 15 mA and can withstand indefinite output short circuits. They are also socketed, permitting field replacement if necessary. (Replacement requires re-calibration for full accuracy.)

Ranges that include -10V may not be capable of driving 2.5 mA if the negative power supply voltage is any less than 12 volts. Recommended alternatives include (1) using a lower voltage range, such as -5 to + 5, (2) buffering the output voltage in the receiving equipment to minimize the output current, and (3) raising the power supply voltages to ± 15 volts. For more information on this last alternative, refer to the User Options section of this manual.

The maximum-rated drive current for each output range is listed in Figure 8.

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Nominal Output Range	Maximum Output Current
0 to +5	10 mA
0 to +10	2.5 mA
-2.5 to +2.5	±10 mA
-5 to +5	±10 mA
-10 to +10	Note 1
0 to -5	-10 mA
0 to -10	Note 1
+2.5 to -2.5	±10 mA
+5 to -5	±10 mA
+10 to -10	Note 1

Note 1: -10V not recommended for current drive.
See text for recommended alternatives.

Figure 8. DAC Current Drive Detail

Figure 9 below lists the settling times for IP-DAC voltage outputs. The listed times are maximum, assuming a 100 pF, 10KΩ load, 10 feet of flat cable, settling to within 1 LSB. Minimum slew rate is 1 V/µsec.

Output Step	Settling Time
10 V	20 µsec
10 mV	12 µsec

Figure 9. DAC Settling Time

All DACs, including those in IP-DAC, produce a glitch when the internal current switches change state. The energy in this impulse is usually fairly small, although the amplitude may be moderate. On the -5 to + 5 range, single bit changes produce an impulse with a peak to peak amplitude of 600 mV typical. Changing all bits in the DAC produces a peak to peak impulse of 1200 mV typical. The width of the primary impulse is 1 µsecond, nominal. The ringing from the impulse settles within 12 µseconds for small changes, 20 µseconds for large ones.

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Current Transmitter

A 4 to 20 mA current transmitter on DAC channels 1 and 2 is a factory option. This option does not prohibit the use of the channels for voltage output.

When using the current transmitter option, channels 1 and 2 must be configured for 0 to + 5 volt operation. See Figures 2, 3, and 5 for implementation details. The calibration information used should be for the current transmitters, not for the voltage output of channels 1 and 2.

Each current transmitter provides a uni-directional current. One I/O pin is the current source, and the second pin the current sink. When operating, the source pin will always have a more positive voltage than the sink pin. The current sources are not floating. The source pin drives from roughly 0.2 to 11 volts above the analog ground. The current sources must be connected to floating or differential inputs. Unused current transmitters may be left open. For pin numbers, refer to the I/O Cable Pin Assignments section of this manual.

The current source can drive loads up to 500 Ohms resistive impedance.

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I/O Cable Pin Assignment

Analog Ground	1
DAC 1 Output	2
DAC 1 Sense	3
DAC 1 Current In	4
n/c	5
DAC 1 Current Out	6
Analog Ground	7
DAC 2 Output	8
DAC 2 Sense	9
DAC 2 Current In	10
n/c	11
DAC 2 Current Out	12
Analog Ground	13
DAC 3 Output	14
DAC 3 Sense	15
Analog Ground	16
n/c	17
n/c	18
Analog Ground	19
DAC 4 Output	20
DAC 4 Sense	21
Analog Ground	22
n/c	23
n/c	24
Analog Ground	25
DAC5 Output	26
DAC 5 Sense	27
Analog Ground	28
n/c	29
n/c	30
Analog Ground	31
DAC 6 Output	32
DAC 6 Sense	33
Analog Ground	34
n/c	35
n/c	36
Analog Ground	37
n/c	38
n/c	39
Analog Ground	40
n/c	41
n/c	42
Analog Ground	43
n/c	44
n/c	45
Analog Ground	46
n/c	47
Analog Ground	48
+5.000 V Drive Input/Output	49
n/c	50

Figure 10. I/O Cable Pin Assignments

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Programming

The IP-DAC can be used with or without the calibration data.

Accessing the IP-DAC without the calibration data is particularly simple. Each of the six DAC channels occupies a single 16-bit wide location. (These locations are listed in Figure 1.) DACs may also be accessed in pairs by writing to the appropriate addresses, also given in Figure 1.

DACs may be accessed equally in either the I/O or the memory space. The I/O and memory base addresses are set on the IP carrier.

Each write to a DAC must be 16-bits wide. Byte-wide writes will have no affect and will not be acknowledged. All reads to the IP will be acknowledged but the data is undefined.

Only address lines A1 through A4 are decoded. Thus, the DACs appear multiple times in the address space, repeating each 32 bytes.

In most cases, access to the IP-DAC will be via a software interface that uses the calibration data to correct the data prior to sending it to the IP. For details, refer to the documentation accompanying your driver or see the Accuracy and Calibration section of this manual. Using the calibration data is not complicated however, and users are encouraged to write or incorporate the few necessary instructions into their own code. Contact the factory for assistance, if needed.

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ID PROM

Every IP contains an ID PROM, the size of which is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software or a supplied driver may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

The ID PROM contains calibration data unique to each IP-DAC IndustryPack. Figure 11 lists the location of standard as well as calibration data in the ID PROM.

For more information on the standard data in the ID PROMs, refer to the IndustryPack Interface Specification. For more information on using the calibration data, see the Accuracy and Calibration section of this manual.

2F	DAC 6 gain error	
2D	DAC 5 gain error	
2B	DAC 4 gain error	
29	DAC 3 gain error	
27	DAC 2 gain error	
25	DAC 1 gain error	
23	DAC 6 offset	
21	DAC 5 offset	
1F	DAC 4 offset	
1D	DAC 3 offset	
1B	DAC 2 offset	
19	DAC 1 offset	
17	CRC	
15	No of bytes used	(14)
13	Driver ID, high byte	
11	Driver ID, low byte	
0F	reserved	(00)
0D	Revision	
0B	Model No	(16)
09	Manufacturer ID	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 11. ID PROM Data

Note: The calibration data stored in the ID PROM is specific to a voltage range. The default range is ± 5 volts. The calibrated voltage range is stored in the Driver ID word as indicated in Figure 12.

Driver ID Value	Calibrated Voltage Range
0	±5 volts
1	0 to 5 volts
2	±10 volts
3	0 to 10 volts
4	±2.5 volts
5	0 to 2.5 volts

Figure 12. Driver ID Values

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Accuracy and Calibration

This section provides a discussion of accuracy, calibration, sources of errors, and drift for the IP-DAC.

Sources of Error

Sources of error in any DAC channel output voltage come from each component in the circuit. The clearest model is a sequence of elements beginning with the reference voltage source and ending with the user's equipment. The basic elements include:

1. Reference voltage source
2. Digital input value
3. DAC
4. Current-to-voltage converter op-amp
5. Output op-amp
6. Current transmitter op-amp (if used)
7. Cabling from IP-DAC to user's equipment
8. User's equipment

Each of the above elements is discussed briefly in the following subsections.

The calibration information contained in the on-board ID PROM contains gain and offset information to fully correct for fixed, linear errors in elements 1 through 6 above. By the use of the Remote Sense option and careful wiring, the error from element 7 may also be compensated.

Uncalibrated offset error on the unipolar ranges (e.g., 0 to 10V) is typically less than 1 LSB. Uncalibrated gain error is typically less than 6 LSBs. Uncalibrated offset error on bipolar ranges (e.g., -5 to + 5V) is typically less than 3 LSBs.

Calibration is provided to ± 1/4 LSB. Accuracy after correction is specified to ± 1 LSB. Typical corrected accuracy is roughly ± 1/2 LSB, although often better.

The primary source of the unipolar offset error is from op-amp offset voltages. This error does not drift significantly. If any op-amp is replaced, the offset error for that channel must recomputed.

The primary source of the fixed gain error and the bipolar offset error (e.g., -5 to + 5V) is mismatched resistor values. The resistors used on the IP-DAC are 0.1% accurate. A secondary source of this error is from the voltage reference and the DAC. If the voltage reference or the DAC is replaced, or an external reference is used, then the gain error must be recomputed. Since the resistors normally track in both temperature and temperature coefficient, a significant change in gain with temperature does not occur. However, rapid temperature changes may produce uncorrected error.

Reference Voltage Source

The voltage source used (AD588) has an uncalibrated accuracy of ± 3 mV for its ± 5V reference outputs. Its drift is typically ± 2 ppm/°C for 0 to 70°C and guaranteed to be within ± 3 ppm/°C over -25°C to + 85°C. The initial error is removed by the calibration process, performed after 10 minutes of warm-up in typical operation. The drift is so low that it takes 30°C to produce an error of 1/4 LSB.

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Digital Input Value

A 12-bit DAC has one of 4096 discreet values. Assuming no error anywhere else in the system, this digitization produces a worst case error of ± 1/2 LSB, and an average error, randomly distributed, of ± 1/4 LSB.

DAC

The dual DAC ICs used (AD7547) have an uncorrected gain error of ± 6 LSB worst case. Typically, this error is 1 to 3 LSBs. They are guaranteed monotonic and linear to ± 1 LSB, and typically perform noticeable better. Their guaranteed gain drift is ± 5 ppm/°C, with a typical value of ± 1 ppm/°C. Gain error is corrected by calibration after a 10 minute warm-up in typical operation. Temperature drift is minor.

Current-to-Voltage Converter Op-Amp

The current-to-voltage converter is an AD648 op-amp. Error is introduced from leakage current from both the DAC and the op-amp. Typical source and feedback resistance is 14 kΩ. (9KΩ min, 20KΩ max.) Leakage current for the DAC is 10 nA max @25°C. Input bias current for the op-amp is 30 pA max over temperature. All leakage currents double for each 10°C temperature rise to a specified maximum of 150 nA for the DAC @70°C. This leakage current is code-dependent, making simple analysis more difficult. 10 nA into 14KΩ produces a voltage error of .14 mV, or .06 LSB at room temperature. 150 nA into 20KΩ produces a worst case error of 3 mV, or approximately 1 LSB @ 70°C. Even this error may be removed if the user executes a dynamic calibration subroutine. The current-to-voltage converter op-amp also has in input offset of voltage of 0.75 mV typical, 3 mV worst case. This error shows up as a fixed offset error on the output. It is relatively fixed, and so is canceled by the zero point calibration.

Output Op-Amp

The output op-amp also has input bias current and offset voltage errors. These errors look very similar to the those of the current-to-voltage converter stage, discussed in the previous paragraph. Note that the major error from the last paragraph was the DAC leakage current, which does not apply to this stage. The worst case error in this stage is 20 µV/°C input voltage drift, which produces an error of 1/4 LSB for 30°C change.

Error is also produced by mismatch in the surface mount resistors used in the last op-amp stage. Fixed errors in these resistors are canceled by the factory calibration. All resistors used in these circuits on the IP-DAC are the same value, and come from the same manufacturing lot, assuring matched temperature coefficients. The components are surface-mounted, which assures that they are normally within a few degrees of each other. The major error comes from uneven heating or cooling of the IP-DAC in an installed system. Since factory calibration is performed at nominal equilibrium temperature, most error is corrected.

The two errors from resistor mismatch are (1) temperature (departure from calibrated value) times differential temperature coefficient, and (2) differential temperature times absolute resistor temperature coefficient. As an example of the first error, a 20°C temperature difference from the calibrated temperature times a typical 5 ppm/°C tracking error produces an error of 100 ppm or 0.4 LSB. As an example of the second error, a differential error of 3°C on the board times 12 ppm/°C typical temperature coefficient results in an error of 0.15 LSB.

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Current Transmitter Op-Amp (if used)

The errors in the current transmitter are very similar to the output voltage stage. The errors contributed by the op-amp are negligible and are corrected with factory calibration. Large temperature differences in the precision resistors used in the current transmitter are the only uncorrected source of significant error. These resistors are all the same manufacturer and type, and are mounted close together.

Cabling from IP-DAC to User's Equipment

Error can be introduced into the system by cabling. For local sense connection (the factory default), this error is cable resistance times current drawn by the user's equipment. As an example, a 5KΩ load draws 1 mA on the -5 to + 5 range. 2Ω of cable resistance produces an error of 2 mV, just under 1 LSB. For additional information regarding cable-related errors, refer to the User Options, Remote Sense section of this manual.

Software Calibration

Software calibration compensates for the D/A, op-amp and gain resistor errors described above. Each channel is calibrated by sampling the voltage across a set of DAC inputs. A least squares linear fit is applied to the data and the resulting equation can be used to derive the actual DAC input needed to achieve the output desired by a given DAC count. The following sections provide correction formulas for unipolar and bipolar configurations.

Unipolar Calibration

The correction formula for unipolar channels is:

$$\text{corrected_DAC} = \frac{\left[(16384 + \text{gain_correction}) * \text{DAC}\right] + (4096 * \text{offset_correction})}{16384}$$

where:

DAC	- D/A input for a perfect DAC
corrected_DAC	- actual D/A input to achieve the desired output
gain_correction	- gain correction factor stored in the ID PROM
offset_correction	- offset correction factor stored in the ID PROM

Bipolar Calibration

The correction formula for bipolar channels is:

$$\text{corrected_DAC} = \frac{\left[(8192 + \text{gain_correction}) * \text{DAC}\right] + (2048 * \text{offset_correction})}{8192} + 2048$$

where:

DAC	- D/A input for a perfect DAC
corrected_DAC	- actual D/A input to achieve the desired output
gain_correction	- gain correction factor stored in the ID PROM
offset_correction	- offset correction factor stored in the ID PROM

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Gain Correction

The gain correction is stored in the ID PROM as four times the deviation from the DAC full range value when the output reaches its full scale output from zero volts. For unipolar channels, the DAC full range is 4096 counts. For bipolar channels, the DAC full range is 2048. The gain correction value is illustrated in Figure 13.

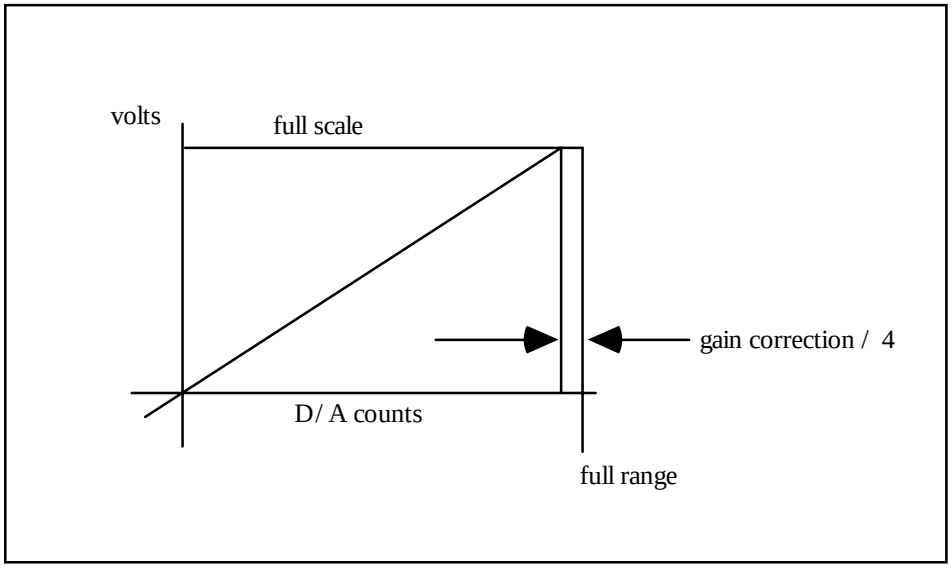


Figure 13. DAC Gain Correction

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Offset Correction

The offset correction is stored in the ID PROM as four times the deviation of the DAC input from its ideal input when the output reaches zero volts. For unipolar channels, the ideal DAC input for zero volts output is zero counts. For bipolar channels, the ideal DAC input for zero volts is 2048 counts. The offset correction value is illustrated in Figure 14.

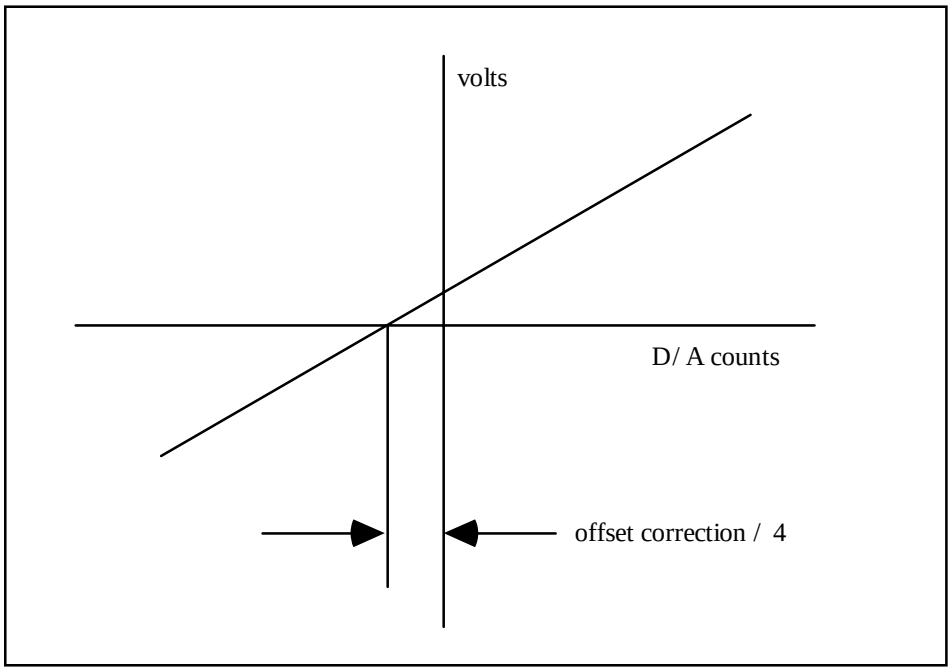


Figure 14. DAC Offset Correction

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User Options

The following user options were discussed in preceding sections of this manual:

- DAC output range
- Current transmitter

The following user options are discussed in subsections below:

- Remote sense
- Remote reference
- ± 15 volt operation

Remote Sense

As shown in Figure 15, the final op-amp stage for each of the six DACs may be converted to Remote Sense by removing a shunt. As shown in Figure 3, Shunt E for channel 5 is offset to the left as all other channels are offset to the right. Figure 3 also illustrates the location of each of the six configuration blocks on IP-DAC. After Shunt E is removed, the two I/O lines (Output and Sense) for each channel must be connected at the users' equipment.

Remote Sense	Shunt E
Remote Sense	OUT
Local Sense	IN

Figure 15. Remote Sense Selection

For many applications, a low current buffer in the receiving equipment is a preferred solution to Remote Sense. DAC error due to cabling is cable resistance times cable current. An op-amp buffer will typically have only a few pA input current, effectively reducing cable error to zero. Note that current flow through the Analog Ground cable lines should be no larger than the current in the signal lines. The user must be careful not to create ground loops in the system.

Remote Sense introduces a positive gain error in the output stage that is .005 percent per Ohm of cable resistance. (For 5V span: .010 %/Ω. For 10V span: .005 %/Ω. For 20V span: .0025 %/Ω.) If the DAC output current into the user's equipment is less than 0.25 mA, there is less cable-induced error from the voltage drop of local sense than from the gain error of Remote Sense.

Remote Reference

The on-board, high-precision voltage reference is buffered to provide up to 100 mA of external current. A single reference may be used to drive almost any number of IP-DACs. This configuration may be used to both lower cost and to have all DACs in the system accurately track.

Each DAC in the system represents approximately 14 KΩ load on the reference. For six DACs on one IP-DAC, this corresponds to roughly 2.1 mA. Note that cabling will introduce a reference voltage error of this current times the cable resistance.

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To implement the Remote Reference, E31 must be removed on all IP-DACs that will not be using their local reference. Figure 5 shows the location of E31. E31 is implemented on IP-DAC as a trace on the solder side of the board. IP-DACs may be ordered from the factory with this trace removed. Field removal is also possible.

In some installations, the use of the Remote Reference may cause instability in the voltage reference feedback loop. An oscilloscope should be used to verify reference stability. If necessary, the addition of a capacitor, ranging in value from 33 pF to 0.1 µF, across the base and emitter of Q1 (or alternatively between pins 1 and 3 of the AD588 U3 reference IC) should re-establish reference stability.

± 15 Volt Power Supply

The IP-DAC is rated for + 5 and ± 12 volt power supply input. The nominal ± 12 volt input specification is the same as for the VMEbus: + 0.60V –0.36V. However, the IP-DAC is designed to operate correctly at ± 15 volts. Most IndustryPacks from SBS as well as most VMEbus IP carrier boards are also designed to operate correctly at ± 15 volts.

Caution: SBS Technologies, Inc. does not recommend running the IP-DAC at voltages outside those specified by the IndustryPack Specification due to possible harm that may be caused to other components or subsystems connected to the user's system.

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-Serial is constructed out of 0.062-inch thick FR4 material. The six copper layers consist of two signal layers on the top and bottom, and four copper-filled internal layers. Two of the internal layers are power and ground planes. These two layers are split between logic power and logic ground close to the logic interface, and external power (+ V) and external ground (0V) close to the I/O interface. The two remaining internal layers are used for output trace wiring and are filled with copper for heat conductivity.

IndustryPacks use through-hole and surface mounting of components. IC sockets are gold-plated, screw-machined pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold-plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. They are not required for most applications.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat (based on the temperature coefficient of the base FR4 material of .31 W/m-°C and taking into account the thickness and area of the IP). If 0.89 Watts were applied uniformly on the component side, the temperature between the component and the solder side would differ by one degree Celsius.

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IndustryPack Logic Interface Pin Assignment

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	DMAreq0*	5	30
D2	MemSel*	6	31
D3	n/c	7	32
D4	n/c	8	33
D5	n/c	9	34
D6	IOSel*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	n/c	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	Strobe*	21	46
–12V	A6	22	47
+12V	Ack*	23	48
+5V	n/c (+5STBY)	24	49
GND	GND	25	50

Figure 16. Logic Interface Pin Assignments

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Pin 1 is marked with a square pad on the IndustryPack.

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Specifications

Form Factor	Single-wide IndustryPack
IndustryPack Bus Speed	8 MHz
Wait States	None on ID read One on DAC writes
Number of Channels	6
Precision	12 bits
Output Voltage Ranges	-5, -10, 5, 10, ±2.5, ±5, ±10 V Hardware selected for each channel individually
Output Current	±2.5 mA on 10 V output ±10 mA on 5 V output
Accuracy	± 1 LSB after calibration
Calibration	Onboard reference 3ppm/C Offset and gain factory calibrated
Settling Time	10 mV step: 12 us 10 V step: 20 us
Initialization	Reset does not change DAC outputs
Dimensions	3.9" x 1.8"
Weight	0.113 lb (0.051 kg)
Power Requirements	+ 5 VDC, 100 mA typical + 12 VDC, 25 mA typical -12 VDC, 25 mA typical All outputs unconnected
Environmental	Operating temperature: + 10° to + 50°C Humidity: 5% to 95% non-condensing Storage: -4° to + 85°C

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