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User Manual

IP-Digital 24

24 Line Digital Input/Output IndustryPack®

Manual Revision: v

Hardware Revision: B2

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IP-Digital 24

24 Line Digital Input/Output IndustryPack™

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Table of Contents

Product Description 5
VMEbus Addressing 7
ISA (IBM PC-AT) Addressing 8
I/O Pin Wiring 9
IndustryPack Logic Interface Pin Assignment 10
Programming 11
Applications Guide 12
Interrupts 14
ID PROM 18
Theory of Operation 19
Construction and Reliability 21
Warranty and Repair 22
User Options 23
Specifications 25
Order Information 27
Schematics 28

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List of Figures

Figure 1 Layout of IP-Digital 24 6
Figure 2 I/O Pin Assignment 9
Figure 3 Logic Interface Pin Assignment 10
Figure 4 Position of Interrupt-related Hardware 14
Figure 5 Interrupt Jumper Block 15
Figure 6 Standard Interrupt Options 15
Figure 7 ID PROM Data (hex) 18
Figure 8 Location of Driver ICs 24

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Product Description

IP-Digital 24 is part of the Industry Pack™ family of modular I/O components. It provides 24 lines of digital I/O. Each line may be individually set as input or output. Both read-back and loop-back registers are provided for maximum software convenience. 16-bit word, 8-bit byte, or bit operations (as read-modify-write) are supported.

The IP-Digital 24 conforms to the Industry Pack Interface Specification. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module, with final system implementation on a different one.

The industry standard 50-pin interface cable may be terminated in a screw terminal block, an OPTO-22™ Direct I/O Interface Module, or user-determined hardware. Alternate grounds on this cable assure reliable signals.

The standard drivers provide 48 mA of sink current on each line. Several options are available to increase this current, add source current capability, or use CMOS levels. See the section User Options later in this manual for more information.

Writing a "1" to any output line turns off the driver, allowing a passive pull-up resistor to set the line to a logic high. The line may now be used for input. Reset forces all lines to a passive high. Writing a "0" to any output line turns on the driver, forcing the line to a logic low. In this state, the line may not be used for input.

Two separate locations in the I/O space are provided for each signal line. The first location is used to set the output state and also to read back the written value. This read-back function is valuable to support bit operations (which are implemented by processors as read-modify-write cycles). This is also valuable in debugging, because it is possible to observe directly the last written value to the port. The second location is the "direct read" port, which is always used for reading input values. The first port is called the "read-back" register; the second port is called the "loop-back" register. The loop-back register may also be used to verify that the correct logic signal is actually in the interface cable.

A flexible interrupt structure permits the user to select any of nine signals for either or both of two interrupts. The standard interrupt control GAL implements switch debouncing and level detection. The user may program this device to perform special functions, including change of state detection, edge detection, and AND/OR logic functions. Eight of the 24 lines are used as a vector register. If interrupts are not used used, these lines are general purpose. If interrupts are used, then any number of these bits (one up to eight) are used for the "fixed" part of the interrupt vectors. The remaining bits (zero up to seven) are used as inputs to determine the "variable" part of the interrupt vector. For more information, see Interrupt GAL, below.

Figure 1, below, shows the layout of the components on the IP Digital 24. Major features are also shown in this figure.

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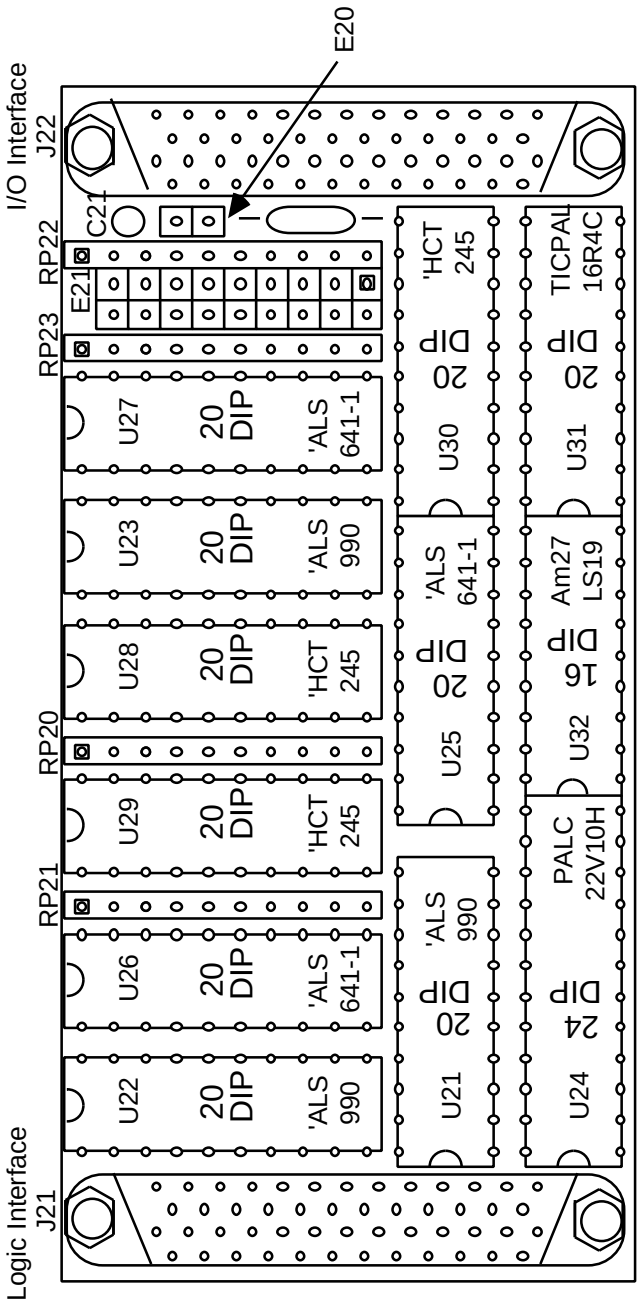


Figure 1 Layout of IP-Digital 24

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VMEbus Addressing

IP-Digital 24 is normally accessed one word at a time in the host's I/O space. Alternatively, byte or longword accesses may be used. If longwords are used, the host (or support module) must map 32-bit longwords into two 16-bit cycles. This is common for 68020 and 68030 implementation of the I/O space.

Standard Word Access, I/O Space

base + 0	word	write	Output Lines 1 through 16 *
base + 2	word	write	Output Lines 17 through 24 *
base + 0	word	read	Read-back Lines 1 through 16
base + 2	word	read	Read-back Lines 17 through 24
base + 4	word	read	Direct Read Lines 1 through 16
base + 6	word	read	Direct Read Lines 17 through 24

* Writing a one sets the line to input mode.

Bitmap of words at base + 0, base + 4

bit:	15	14	13	12	11	10	9	8
	I/O 16	I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9
bit:	7	6	5	4	3	2	1	0
	I/O 8	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1

Bitmap of words at base + 2, base + 6

bit:	15	14	13	12	11	10	9	8
bit:	7	6	5	4	3	2	1	0
	I/O 24	**I/O 23**	**I/O 22**	**I/O 21**	**I/O 20**	**I/O 19**	**I/O 18**	**I/O 17**

Note: data in bits 15 through 8 are ignored in writes, read as "1"s.

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ISA (IBM PC-AT) Addressing

base + 1	byte	write	Output Lines 1 through 8 *
base + 0	byte	write	Output Lines 9 through 16 *
base + 3	byte	write	Output Lines 17 through 24 *
base + 3	byte	write	Load Interrupt Vector *
base + 1	byte	read	Read-back Lines 1 through 8
base + 0	byte	read	Read-back Lines 9 through 16
base + 3	byte	read	Read-back Lines 17 through 24
base + 3	byte	read	Read-back Interrupt Vector
base + 5	byte	read	Direct Read Lines 1 through 8
base + 4	byte	read	Direct Read Lines 9 through 16
base + 7	byte	read	Direct Read Lines 17 through 24

* Writing a one sets the line to input mode.

Bitmap of byte at base + 1

bit:	7	6	5	4	3	2	1	0
	I/O 8	**I/O 7**	**I/O 6**	**I/O 5**	**I/O 4**	**I/O 3**	**I/O 2**	**I/O 1**

Bitmap of byte at base + 0

bit:	7	6	5	4	3	2	1	0
	I/O 16	**I/O 15**	**I/O 14**	**I/O 13**	**I/O 12**	**I/O 11**	**I/O 10**	**I/O 9**

Bitmap of byte at base + 3

bit:	7	6	5	4	3	2	1	0
	I/O 24	**I/O 23**	**I/O 22**	**I/O 21**	**I/O 20**	**I/O 19**	**I/O 18**	**I/O 17**

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I/O Pin Wiring

This section gives the pin assignments and wiring recommendations for IP-Digital 24.

The pin numbers given in Figure 2 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O 1	1	GND	2
I/O 2	3	GND	4
I/O 3	5	GND	6
I/O 4	7	GND	8
I/O 5	9	GND	10
I/O 6	11	GND	12
I/O 7	13	GND	14
I/O 8	15	GND	16
I/O 9	17	GND	18
I/O 10	19	GND	20
I/O 11	21	GND	22
I/O 12	23	GND	24
I/O 13	25	GND	26
I/O 14	27	GND	28
I/O 15	29	GND	30
I/O 16	31	GND	32
I/O 17	33	GND	34
I/O 18	35	GND	36
I/O 19	37	GND	38
I/O 20	39	GND	40
I/O 21	41	GND	42
I/O 22	43	GND	44
I/O 23	45	GND	46
I/O 24	47	GND	48
+5V (Option)	49	GND	50

Figure 2 I/O Pin Assignment

Caution

Note that when the IP-Digital 24 is used to directly connect with Opto 22, Allen Bradley, Grayhill or similar compatible parallel opto-isolation panels that these panels number their channels starting with pin 47. Thus the IP-Digital 24 line number ordering and the Opto Panel line number ordering are *reversed*.

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IndustryPack Logic Interface Pin Assignment

Figure 3 below gives the pin assignments for the IndustryPack Logic Interface on the IP-Digital 24. Pins marked n/c below are defined by the specification, but not used on IP-Digital 24. See also your User Manual for your IP Carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	n/c	5	30
D2	n/c	6	31
D3	n/c	7	32
D4	INTSel*	8	33
D5	n/c	9	34
D6	IOSel*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	INTReq0*	17	42
D14	A4	18	43
D15	INTReq1*	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	n/c	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 3 Logic Interface Pin Assignment

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Programming

Programming the IP-Digital 24 requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP carrier. This document refers to this address as "base."

Each of the 24 bits is individually configurable as either input or output. Output is accomplished by writing data directly to the I/O register location. To configure a line for input, first, write a "1" to the I/O bit location. This puts the I/O line in "high impedance" mode so it can receive data. Then, input data is read from the Direct Read Register.

Standard Word Access, I/O Space

base + 0	word	write	Output Lines 1 through 16 *
base + 2	word	write	Output Lines 17 through 24 *
base + 0	word	read	Read-back Lines 1 through 16
base + 2	word	read	Read-back Lines 17 through 24
base + 4	word	read	Direct Read Lines 1 through 16
base + 6	word	read	Direct Read Lines 17 through 24

* Writing a one sets the line to input mode.

The I/O locations are read/write latches that store data locally on the IP. Writing to the "Output Line" writes to this latch. Reading from the "Read-back Line" reads the contents of this latch. This is useful for verifying pervious writes and direction configuration. The "Direct Read Lines" is just that, they read the state of the I/O line at the pin, regardless of data direction.

Using word access, up to 16 bits may be programmed at once. The IP-Digital 24 implements a read-back register at the same address used for writing to the signal line I/O bits. This permits "set bit" and "clear bit" instructions to be used in programming, which are implemented by the host hardware as read-modify-write cycles. Thus single bits as well as bit fields may be accessed.

The IP-Digital 24 may also be accessed using byte or longword accesses. If longword accesses are used from a 68020 or 68030 host the I/O space must be mapped into "D16." 68000 and 68010 hosts internally map all longword accesses into 16 bits, so no special precaution is necessary.

All bits are set to a "1" (input mode) during Reset. This setting action occurs continually, so that the bits are effectively set to a safe value during both the beginning and end of the Reset period. This guarantees a power-up state of "1." It is recommended that the user assign bit polarity in his system in such a way that a logic "1" is off, or the fail-safe state.

Contact GreenSpring Computers for additional application assistance.

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Applications Guide

This section provides information to those users who wish the ultimate in low power consumption.

Most of the power on the IP-Digital 24 is consumed by the bipolar drivers and the ID PROM. For any 8-bit I/O group that is used entirely for input, the associated driver IC may be removed from the IP. See the schematic for details on which IC drives which I/O lines.

The ID PROM is not strictly required for operation of the IP. Please review the section above, ID PROM, before removing it.

Removing the socketed ID PROM and all three socketed drivers reduces the average power consumption from 250 mA to 125 mA. Most of this remaining power is consumed by the three 74ALS990 read-back registers. These parts will be replaced on new units by Advanced CMOS parts when they become available (sometime in 1989).

The 74ALS641 drivers may be replaced with CMOS drivers, such as 74HCT245, which draw less than 1 mA except for that necessary to drive signals. CMOS logic is not currently available in Open Drain configurations. Thus replacing the standard Open Collector driver with a 3-State driver requires that the associated eight I/O lines be used for Output only.

The passive pull-up resistors are also socketed and may be removed or replaced with a larger value. Removal is not generally recommended because the floating CMOS inputs will draw a significant amount of current, as well as produce unpredictable results for any undriven lines. However, if CMOS drivers, or no drivers, are used the pull-up resistors may have values as high as 200 K? .

Interfacing

There are many ways to take advantage of the general purpose nature of the IP-Digital 24. First, some general guidelines are presented below, then some simple examples are given. Do not hesitate to contact the factory if you need more assistance.

Sink, don't source current. The standard drivers can sink up to 48 mA. Up to 64 mA is available if 74AS641 drivers are substituted. Turn on LEDs, external logic, opto-couplers, reed relays, etc by driving the output line to ground. The standard source current is provided by a 10 K? pull-up resistor. Even if 3-State drivers are used, only several milliamperes is available in source current.

Use low for on, high for off. The IP-Digital 24 resets to a passive high. Be sure that Reset does not turn on external equipment. Another good idea is to have pull-up resistors on the receiving equipment, too. That way plugging and unplugging an IP interface cable should have no effect.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without impacting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common source.

Power all system power supplies from one switch. Connecting external voltage to the IP-Digital 24 when it is unpowered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels should be used.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-Digital 24 does not contain special input protection.

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We provide the components, You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within 0.7 volts of ground potential.

Sample Applications

Switch. A simple switch closure may be detected by connecting one side of the switch to any input line, and the other side to the nearest ground line on the cable. For example interface cable pin 1 for input and pin 2 for ground. A switch closure is read as a zero; an open switch is read as a one.

Opto-coupler Input. An opto-coupler may be received like a switch. Wire the output of the coupler (collector) to the input line, and the common (emitter) to ground. "On" is detected by reading a low.

LED. An LED may be turned on by connecting the cathode to the output pin, the anode to a 330? resistor, and the other end of the resistor to the +5V line (pin 49). Install a shunt at location E20 to enable the external +5V line. Turn the LED on by driving the line low. Turn the LED off by driving the line high. For a brighter LED use a 150? resistor.

Opto-coupler output. An opto-coupler may be driven like an LED. Some have internal resistors and some do not. Connect as described in the previous paragraph.

Optical Isolation. The 50-pin interface cable mates directly with OPTO-22™ Direct I/O panels. Compatible panels are made by several other companies. These panels provide optically isolated inputs and outputs, AC and DC, low and high voltage. It is easy to mix isolated and non-isolated signals on one IP-Digital 24 by splitting the flat cable.

Unlike many other digital I/O products, the IP-Digital 24 has the full 24 mA of sink current required to reliably operate OPTO-22 panels. Most other digital I/O boards use NMOS chips to directly drive the outputs (NMOS is rated at 4 mA).

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.

Many flat cable interface products are available from third party vendors to assist in your system integration or debugging. These include connectors, cable, test points, "Y"s, 50-pin in-line switches, breakout boxes, etc.

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Interrupts

Up to two interrupts may be generated by the IP-Digital 24. Flexibility is achieved by the combined use of a user jumper block, and a PAL. A standard PAL is provided with each Industry Pack. The standard PAL equations are given in the Appendix. Users are encouraged to generate their own interrupt PALs for special applications. The location of the jumper block E31 and the PAL U31 are shown in Figure 4 below.

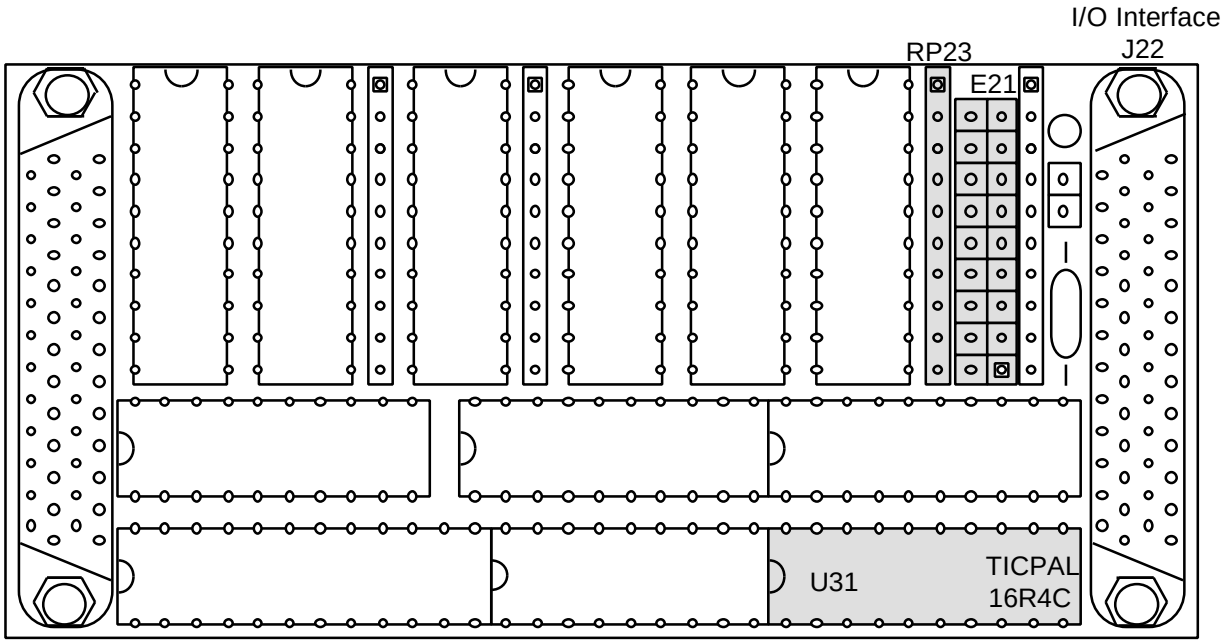


Figure 4 Position of Interrupt-related Hardware

The standard PAL implements interrupts on detecting either a high or a low for each of the two interrupts. An edge detection circuit using the 8 MHz IP clock first detects the transistion and generates the interrupt. A level sensing circuit keeps the interrupt asserted until the I/O line level is changed. A subset of the 24 I/O lines are used for interrupt generation. The available lines for interrupts are I/O 17 through I/O 23, plus I/O 1 and I/O 2. These are shown in Figure 5, on the next page.

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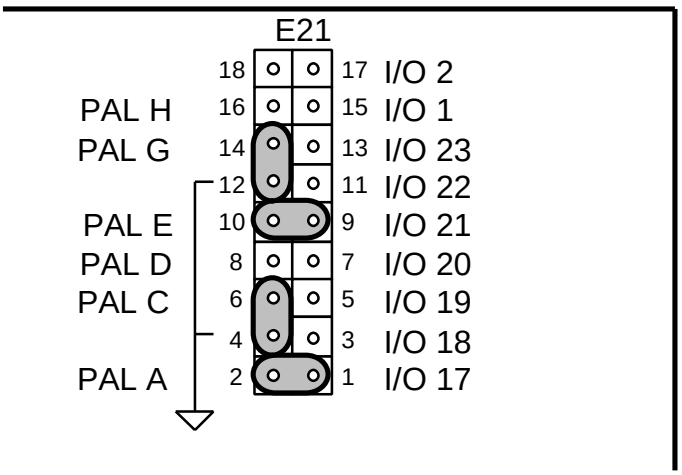


Figure 5 Interrupt Jumper Block Showing Default Shunts

The table below, Figure 6, shows the easiest way to configure E21 for interrupts. A shunt installed across the two E21 pins on any single line enables the identified function for the identified I/O line. Other I/O lines may be used for the listed functions by using wire-wrap wires between the E21 posts. I/O 18, I/O 22 and I/O 1 are available on the E21 jumper block, but are not shown in the table because they are not immediately adjacent to a PAL input pin.

For each interrupt used (IRQ0 or IRQ1), the "Interrupt Disable" function is required. Then either the Rising Edge, the Falling Edge, or both may be connected.

Function	Inter-rupt	PAL input	E21 Pin	I/O Line	E21 Pin
Int Disable	IRQ0	A	E21-2	I/O 17	E21-1
Rising Edge	IRQ0	C	E21-6	I/O 19	E21-5
Falling Edge	IRQ0	D	E21-8	I/O 20	E21-7
Int Disable	IRQ1	E	E21-10	I/O 21	E21-9
Rising Edge	IRQ1	G	E21-14	I/O 23	E21-13
Falling Edge	IRQ1	H	E21-16	I/O 2	E21-15

Figure 6 Standard Interrupt Options

IP Logic Interface Specifications require that interrupts be explicitly enabled. The standard PAL equations and jumpering implement I/O 17 as the active low INT0 enable, and I/O 21 as the active low INT1 enable. This is shown in the default jumpering on E21, in Figure 6, above. All PAL inputs have pullup resistors, thus an unconnected input is always a "1."

The standard Interrupt PAL detects both high and low levels. There is no "debounce" function built in, but un-debounced switches may still be used. Switches generally produce several transitions during both close and open operations, however this is not guaranteed. This means that a switch may generate an interrupt while being both opened and closed. Bounce times vary considerably, but average a few milliseconds. Either software debouncing may be used, or the interrupt routine may just as easily be able to tolerate being called several times on each switch operation.

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The Interrupt PAL may be used to provide switch debouncing functions. For additional assistance refer to the the Interrupt PAL listing in the Appendix, or contact the factory.

Interrupt Vectors

All Industry Pack interrupts use a vector. The vector from the IP-Digital 24 comes from the I/O bits 17 through 24, as shown below.

Bitmap of interrupt vector, at base + 3:

bit:	7	6	5	4	3	2	1	0
	I/O 24	**I/O 23**	**I/O 22**	**I/O 21**	**I/O 20**	**I/O 19**	**I/O 18**	**I/O 17**

The vector is written to all "1"s ($FF) on Reset.

The user may generate an 8-bit fixed vector by writing the desired vector to location base + 3. In this case the I/O bits 17 through 24 would be unused (as input or output).

Alternatively, some of these bits may be inputs from the user's system, permitting powerful vectoring directly to the desired interrupt handler. The "variable" bits are first set to a "1" when the vector is written. Then the associated I/O line is connected as an external input.

The user must provide an interrupt vector in the host's vector table for all possible combinations, generally 2^n, where n is the number of variable bits used. (n may be 0 up to 7.) Usually fewer than 2^n separate interrupt handlers are needed. Unless the user provides a way to prevent input bits from changing during interrupt acknowledge cycles on the host, it is important that all 2^n vectors be placed in the host's vector table.

A separate vector may be provided for the IP's A and B interrupt requests by using one or more variable bits in the vector that are also used by the Interrupt Request PAL in its equations. See the PAL listing in the Appendix for more information.

Any pending interrupts are cleared on Reset, as required by the Industry Pack Interface Specification.

Interrupt Sequence

The simplified sequence for setting up and processing an interrupt is given below.

1. Decide on the external event that you wish to cause an interrupt. Wire this to the appropriate I/O line, depending on if the event is an active high or active low. See Figure 6 to select the I/O line.

2. Place a shunt or wire on E21 to connect the selected I/O line to the correct Interrupt PAL input. See figure 5 for E21 layout.

3. Wire the system, install the IP on the Support Module (and set the base address), install the Support Module in the host system, and provide power.

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4. The (power-on) Reset will force all I/O lines to a passive high. This will (i) remove any pending interrupts and (ii) force the Interrupt Enable I/O line to Off.

5. Load the Interrupt Vectors into the host's processor's vector table. This host vector points to the interrupt handler, which should now be resident in memory.

6. Load the Interrupt Vector. This is the byte at base + 3. See the ADDRESS MAP section above for more information. Set the I/O line corresponding to the Interrupt Enable function to "1" to keep interrupts disabled. (The IP can generate 2^n separate vectors, where n is the number of bits in the interrupt vector that are "1" and are connected to external inputs.)

7. Enable interrupts internally in the host processor.

8. Enable the Interrupt on the IP by clearing the Interrupt Enable bit.

9. When an interrupt event occurs, the Interrupt PAL will detect the level change and signal with IRQ0 or IRQ1 to the Support Module. This change must occur after Reset, but may occur prior to the interrupts being enabled. The Support Module will pass the interrupt to the host via the host bus. The host processor will respond to the interrupt with an Interrupt Acknowledge cycle. The Support Module will use this cycle to read the IP's interrupt vector, passing this back to the host. The host will use this vector to jump through its vector table to the interrupt handler.

10. The interrupt handler may wish to disable further interrupts, respond explicitly to the interrupt, or merely continue. Interrupt handlers always terminate with a "Return from Exception" to restore the stack and prior interrupt level in the host processor. Since any interrupt acknowledge cycle clears both pending interrupts on the IP, the interrupt handler must check for both conditions, if two independent interrupts are used.

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ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-DIGITAL 24 is shown in Figure 7 below.
For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 10 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

The ID PROM used is an AMD 27LS19A or equivalent.

3F 19	(available for user)	
17	CRC	(A7)
15	No of extra bytes used	(00)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(B2)
0B	Model No	(11)
09	Manufacturer ID	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 7 ID PROM Data (hex)

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Theory of Operation

Industry Pack Standards

The IP digital 24 is part of the Industry Pack™ family of modular I/O products. It meets the Industry Pack Logic Specification. (Contact GreenSpring Computers, Inc. for a copy of this Specification.) It is assumed that the reader is at least casually familiar with both this document and 68000 family processor architecture.

Control Logic

A single CMOS 22V10 PAL (U24) controls the logic on the IP. This PAL is clocked by the 8 MHz IP Logic clock from the Support Module. The IP responds to I/O, ID, INTSEL and DMA selects. It does not respond to memory selects, however the MEMSEL line is routed to the control PAL, enabling easy modification for special needs.

Since all the logic on the IP is TTL or equivalent speed CMOS, no wait states for either read or write cycles is required. Thus the control PAL generates ACK on the clock cycle following any select. Hold cycles (from the Support Module) are supported for both read and write accesses by extending ACK, as required. If no hold cycles are requested by the Support Module, the IP Digital 24 is capable of supporting the full 8 MB per second data transfer rate of the IP Logic Interface Specification.

ID PROM

The ID PROM, which is a 32 x 8 bit low power bipolar device in a 16-pin DIP package, is directly enabled onto the low 8 bits of the IP Logic data bus by the ID select line. At the same time, the control PAL generates ACK.

For the contents of the ID PROM, see Figure 7 in the main text. For more information on ID PROMS on Industry Packs in general, see the Industry Pack Logic Interface Specification. The ID PROM may be removed by the user to add information, or may be left off for low power operation, although this is not recommended. See also the section, USER OPTIONS, in the main text.

Output Data

The 24 bits of output data are stored in three 74ALS990 Octal Read-back Registers. The control PAL generates the three required strobes. Both byte and word accesses are supported. The write strobe is a single clock wide. The PAL uses one bit (pin 18) to remember that a cycle is in progress. This prevents extended or multiple write strobes during hold states.

Reading of the output data is supported directly by using the read-back feature of the '990 registers. Read-back data is at the same addresses as the write data. The advantage of this is that processor bit operations (which are implemented as read-modify-write cycles) are directly supported by the hardware.

The 24 bits of data from the '990s passes through three octal drivers. The default driver is the Open Collector 74ALS641-1. This low power part can sink 48 mA of current on each line. These three parts are socketed. Thus they may be replaced in the field if a different driver is desired, or they are damaged.

Three SIP resistor networks provide passive pull-ups for the 24 I/O lines. These may be replaced with networks of a different value for special applications. Since CMOS inputs are used, the resistors should never be completely removed.

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Input and Loop-back

The Direct Read and Loop-back register is implemented with three CMOS Octal Buffers, 74HCT245 (U28, U29, U30). During read operations, these buffers place the logic levels on the 48 I/O lines onto the Industry Pack logic interface data bus. External input on any given I/O line can occur when the output driver is off, or "high."

No special input protection is provided. Modern CMOS inputs are relatively rugged. The high capacitance of flat cables also helps protect against static discharge damage. Nonetheless, the user must take standard precautions against damaging the input buffers with static or under- or over-voltage. If they are damaged, they are easily replaced in the field, since the parts are socketed. High voltage, high current connections to the I/O lines may produce component failures throughout the host system, however. See also information on optical isolation, under the Applications Guide, in the main text.

Interrupts

The interrupt structure is very flexible, but the IP Logic Specification does enforce two requirements: (i) Reset must clear any pending interrupts, (ii) interrupts must be specifically enabled. The first requirement is met within the Interrupt PAL (U31). The second requirement is implemented by a combination of the PAL and jumpering. PAL inputs A (pin 2) and E (pin 6) are implemented in the standard equations as active low interrupt enables. These two lines are jumpered to I/O 17 and I/O 21 respectively. Since all I/O lines are forced to a passive high on Reset, interrupts are disabled. The user's code sets either or both of these two lines low to enable interrupts IRQ0 and IRQ1 respectively.

The interrupt PAL also implements automatic removal of the interrupt request line on any pack interrupt acknowledge (INTSEL active) cycle. Although there are two interrupt requests, since they are both cleared by entering an interrupt routine, all interrupt handlers for the IP Digital 24 must check for both interrupt conditions.

The standard interrupt PAL equations implement, for each of the two interrupts, one active high edge and one active low edge input. These edges must occur after Reset is removed. To generate a second interrupt, a new edge is required. Many users will wish to modify the standard interrupt PAL equations to implement their own requirements. The default interrupt jumpering does not connect any I/O lines to interrupt PAL. See the section in the main text, Interrupts, for details on jumpering options.

Additional assistance is available from the factory, if needed.

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-Digital 24 is constructed out of 0.062 inch thick FR4 material. The four copper layers consist of two signal layers on the top and bottom, and two internal layers for power and ground planes. The power and ground planes minimize RF noise generation and assist in even dissipation of heat.

Through hole mounting of components is used. IC sockets are screw-machined pins, gold plated. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

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GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the factory for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one third of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

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User Options

There is one on board user jumper option, other than interrupt wiring and interrupt PAL programming (see section, INTERRUPTS, above).

Pin 49 of the interface cable may be optionally connected to +5V. To do this, install a shunt or wire at E20. E20 is visible at the right side of figure 8. There is a limit of 1 Amp from this power line because that is the rated limit of both the IP and flat cable connector pins. This line is not fused, so the user must take any necessary safety precautions to insure against excess current.

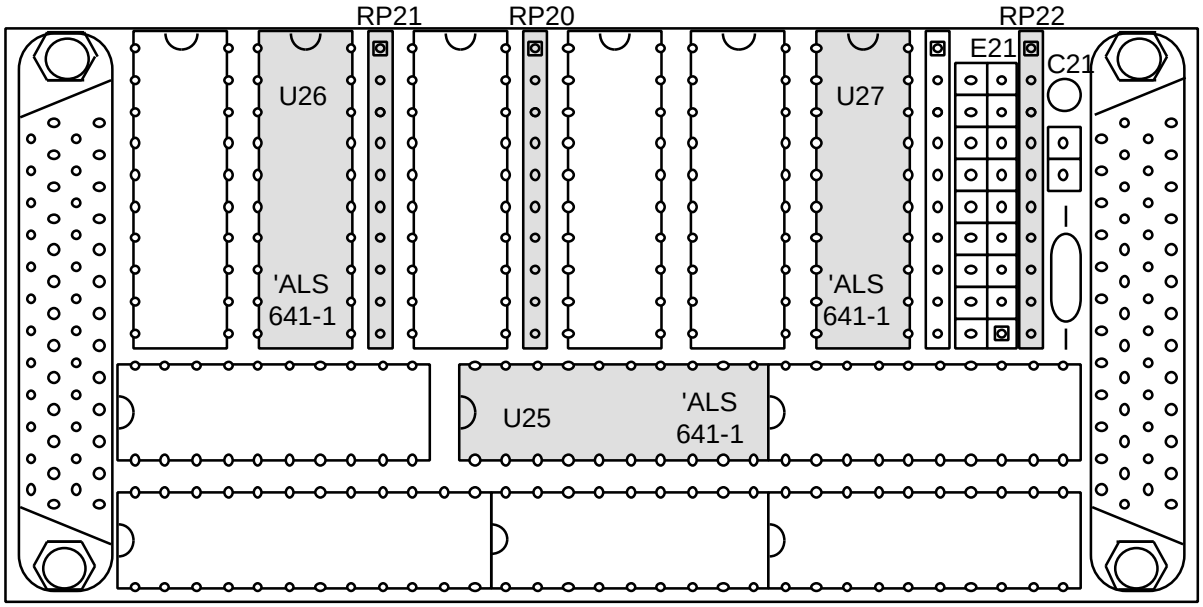
There is a choice of four different interface voltage standards for the I/O lines, selectable in 8-bit groups. The default is Advanced Low-Power Schottky TTL Open Collector drivers (74ALS641-1), which provide 48 mA of sink current on each line. The first option replaces the standard drivers with a higher current version, for 64 mA of sink current (Option 74AS641). An second option replaces these with bipolar 'ALS TTL outputs for positive source current during logic high (Option 74ALS645-1). The third option uses Advanced CMOS drivers for minimum power dissipation and maximum noise immunity (Option 74HCT245). These last two options may be used as outputs only.

Substitute drivers are installed at the factory if ordered with the IP, or they may be substituted in the field by the user.

The 74AS641 drivers provide 64 mA of sink current per line. These drivers also consume more power, and because of their fast switching time, may generate more system and cable noise than the standard drivers. The 74ALS645-1 alternative drivers are three-State, rather than open collector. Thus they may be used only when the I/O lines are dedicated to output, in groups of eight (eight lines per driver).

74HCT245 drivers may be used for the minimum power consumption, maximum noise immunity, and CMOS interface levels. Like the 74ALS645-1s, however, they may be used for output only (in groups of eight lines).

Figure 8 below shows the locations of the socketed drivers.



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Figure 8 Location of Driver ICs

The chart below shows the relationship between the driver ICs, the pullup resistor networks, and the I/O lines:

I/O Lines	Driver	Pullup Network
I/O 1 through I/O 8	U25	RP20
I/O 9 through I/O 16	U26	RP21
I/O 17 through I/O 24	U27	RP22

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Specifications

Logic Interface:	Industry Pack™ Logic Interface
Digital Interface:	24 Digital Signal Lines Each Line Input or Output Alternate Grounds on Interface Cable
Interface Level:	Choice of (in 8-bit groups): TTL Open Collector (standard), High Current (64ma) Open Collector, CMOS. Pull-up Resistor for Open Collector: 10K standard, Other values on special order, Field substitutable.
Interface Standard:	OPTO-22 Direct I/O Panels and equivalents
Software Interface:	Each 8-bit group has: Output Register Read-back Register Loop-back Register Interrupt Register
Initialization:	Reset forces all lines to Passive High Input
Access Modes:	Byte or Word in I/O Space, Read-Modify-Write (for bit operations), Vectored Interrupt
Access Time:	125 nanoseconds
Wait States:	Zero
Transfer Rate:	8 Mbyte/second maximum, continuous
Interrupt:	High order 8-bit group used as vector, Vector may be fixed or variable (externally), User PAL may be programmed for special features: debouncer, edge detection, quadrature detection, etc. Two interrupts supported
DMA:	Basic DMA read and write access to 16-bits No external handshake
On board Options:	Interrupt Jumpering, Interrupt PAL programming, +5V on pin 49 of interface cable
Interface Options:	50-pin flat cable, 50 screw terminal block interface
Documentation:	User Manual includes Schematics, PROM Listing, PAL Listings, Theory of

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Dimensions:	1.8 inches x 3.9 inches x 0.344 inches (max)
Construction:	Conformal Coated FR4 4-layer Printed Circuit, Through-Hole Mounting, Driver ICs, Programmable Parts in sockets
Temperature Coefficient:	0.89 W/°C for uniform heat across IP
Power:	245 mA @ +5V typical 330 mA maximum (outputs open)

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Order Information

IP-Digital 24	IndustryPack with 24 input/output lines
IP-Digital 24–ENG KIT	which includes: six foot 50-pin cable, 50-screw terminal block, Technical documentation: 1. IP-Digital 24 Bill of Materials 2. IP-Digital 24 Assembly Drawing 3. IP-Digital 24 Schematics 4. IP-Digital 24 PLD Listing

***Note**: Engineering Kits are strongly recommended for first time buyers.*

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Schematics

Schematics are provided here for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessary current or complete manufacturing data, nor is it part of the product specification. All information following is Copyright GreenSpring Computers, Inc.

Current manufacturing information, including schematics, programmed device listings, bills-of-material, and assembly diagrams are available from GreenSpring Computers as part of the Engineering Kit option or from your international distributor.

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