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IP-OCTALPLUS485

8 Channel RS485 Interface

User Manual

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IP-OCTALPLUS485

8 Channel RS485 Interface

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1 Product Description

The IP-OCTALPLUS485 provides eight channels of a high performance multi-mode serial RS485 interfaces.

Features include programmable baud rates up to 2 Mbit/sec, asynchronous or synchronous protocols including NRZ, NRZI, FM, T1, SDLC/HDLC.

Each of the eight serial channels of the IP-OCTALPLUS485 has a 4-byte transmit FIFO and an 8 byte receive FIFO. Programmable FIFO interrupt levels provide flexible interrupt response. Channel 1 to 4 generate interrupts on interrupt request line IP_INTREQ0# and channel 5 to 8 generate interrupts on interrupt request line IP_INTREQ1#.

Each RS485 transceiver is protected against electrostatic discharge (ESD).

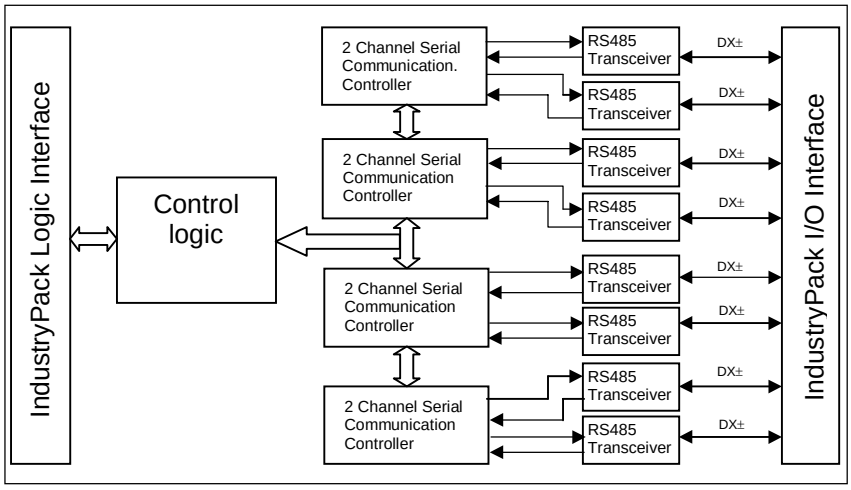


Figure 1: IP-OCTALPLUS485 Block Diagram

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2 Technical Specification

Logic Interface	IndustryPack® Logic Interface
I/O Interface	50-conductor flat cable
Size	Single wide IP Type I
Number of serial channels	Eight
I/O Signals per channel	TxD+ / TxD- and RxD + / RxD - ,
Serial Controller	Z85230
Clock Frequency	PCLK 8MHz RTxC 7.3728 MHz
FIFO	8 byte receive FIFO, 4 byte transmit FIFO per channel
Physical Interface	Half Duplex RS485 Interface
ESD Protection	±15kV – Human Body Model
Transfer Rate	Up to 500kbaud for IP-OCTALPLUS485
Wait States	No wait states for ID Prom access One wait state for SCC access Three wait states for interrupt vector read
Power Requirements	Typ. 370mA @ +5V, no load
Temperature Range	Operating 0°C to 70°C Storage –45°C to 125°C
Humidity	5 - 95% non-condensing

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3 ID Prom Contents

ADDRESS	FUNCTION	
$01	ASCII ‘I’	$49
$03	ASCII ‘P’	$50
$05	ASCII ‘A’	$41
$07	ASCII ‘C’	$43
$09	Manufacturer ID	$B3
$0B	Model Number	$24
$0D	Revision	$10
$0F	RESERVED	$00
$11	Driver-ID low-byte	$00
$13	Driver ID high byte	$00
$15	Number of bytes	$0D
$17	C R C	$D2
$19	Version	$0A

Figure 2: ID Prom Contents

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4 IP Addressing

The IP-OCTALPLUS485 is accessed in the I/O space through a set of external registers of the Z85230 Serial Communication Controller (SCC). Each channel of the Z85230 SCC can be accessed by two addresses in the IP's I/O address space. However the Z85230 SCC uses an internal set of registers for each channel, which can be accessed indirectly.

ADDRESS	Name	Function	Size
$01	CHCON0	Port0 control register (SCC1 B Control)	Byte
$03	CHDAT0	Port0 data register (SCC1 B Data)	Byte
$05	CHCON1	Port1 control register (SCC1 A Control)	Byte
$07	CHDAT1	Port1 data register (SCC1 A Data)	Byte
$09	CHCON2	Port2 control register (SCC2 B Control)	Byte
$0B	CHDAT2	Port2 data register (SCC2 B Data)	Byte
$0D	CHCON3	Port3 control register (SCC2 A Control)	Byte
$0F	CHDAT3	Port3 data register (SCC2 A Data)	Byte
$11	CHCON4	Port4 control register (SCC3 B Control)	Byte
$13	CHDAT4	Port4 data register (SCC3 B Data)	Byte
$15	CHCON5	Port5 control register (SCC3 A Control)	Byte
$17	CHDAT5	Port5 data register (SCC3 A Data)	Byte
$19	CHCON6	Port6 control register (SCC4 B Control)	Byte
$1B	CHDAT6	Port6 data register (SCC4 B Data)	Byte
$1D	CHCON7	Port7 control register (SCC4 A Control)	Byte
$1F	CHDAT7	Port7 data register (SCC4 A Data)	Byte

For more details of the Z85230 SCC, its internal registers and its programming refer to the Z85230 Data Sheet.

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5 Programming Hints

5.1 RS485 Transmitter Control

For Transmitter control the RTS# pin of the SCC is used. For RS485 applications the Auto Enable bit (WR3 D5 = ‘1’) must be set. In asynchronous mode the user must set the RTS bit (WR5 D1= ‘1’) before writing a character to the transmit buffer and reset the RTS bit (WR5 D1 = ‘0’) after writing to the transmit buffer. The RTS# pin enables the RS485 transmitter immediately and remains active until the transmitter is completely empty.

5.2 Baud Rates

Baud rates may be derived from a local 7.3728 MHz oscillator frequency permitting the generation of all standard baud rates (including 19200, 38400 and 57600 baud) with zero error. Some networks and communication protocols may require a different oscillator frequency.

5.2.1 Using internal baud rates

The local 7.3728 MHz oscillator is connected to the RTxC# pin of all channels of the Z85230 SCC. This is the standard configuration of supplying the programmable baud rate generator with an input clock. To enable the baud rate generator with the 7.3728 MHz clock, the software must set bit D1, D0 of the SCC’s internal register W14 to ‘01’.

To use the output of the baud rate generator as transmit clock and receive clock bit D4,D3 and D6,D5 of the internal register WR11 must be set to ‘10’.

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6 IP I/O Connector

IP I/O Connector
50p. flat cable conductor

Pin-No.	Name	Comment
1	GND	Signal Ground
2	DX-_0	Channel 0 Inverting Data I/O
3	DX+_0	Channel 0 Noninverting Data I/O
4	CLK-_0	Not used
5	CLK+_0	Not used
6	GND	Signal Ground
7	DX-_1	Channel 1 Inverting Data I/O
8	DX+_1	Channel 1 Noninverting Data I/O
9	CLK-_1	Not used
10	CLK+_1	Not used
11	GND	Signal Ground
12	DX-_2	Channel 2 Inverting Data I/O
13	DX+_2	Channel 2 Noninverting Data I/O
14	CLK-_2	Not used
15	CLK+_2	Not used
16	GND	Signal Ground
17	DX-_3	Channel 3 Inverting Data I/O
18	DX+_3	Channel 3 Noninverting Data I/O
19	CLK-_3	Not used
20	CLK+_3	Not used
21	GND	Signal Ground
22	DX-_4	Channel 4 Inverting Data I/O
23	DX+_4	Channel 4 Noninverting Data I/O
24	CLK-_4	Not used
25	CLK+_4	Not used
26	GND	Signal Ground
27	DX-_5	Channel 5 Inverting Data I/O
28	DX+_5	Channel 5 Noninverting Data I/O
29	CLK-_5	Not used
30	CLK+_5	Not used
31	GND	Signal Ground
32	DX-_6	Channel 6 Inverting Data I/O
33	DX+_6	Channel 6 Noninverting Data I/O
34	CLK-_6	Not used
35	CLK+_6	Not used
36	GND	Signal Ground
37	DX-_7	Channel 7 Inverting Data I/O
38	DX+_7	Channel 7 Noninverting Data I/O
39	CLK-_7	Not used
40	CLK+_7	Not used
41	GND	Signal Ground for External Termination
42	+5V	Power Supply for External Termination
43	n.c.	Not Connected
...	...	Not Connected
50	n.c.	Not Connected

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