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IP-PREC-ADC

20 Channel 12-bit A/D Converter with Two Channel DAC

IndustryPack®

Manual

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Hardware Revision: A
Part # 89002055 Rev. 1.0 20050119

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IP-PREC-ADC

20 Channel 12-bit A/D Converter with Two Channel DAC
IndustryPack

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Product Description

IP-PREC-ADC is part of the Industry Pack™ family of modular I/O components. It provides 20 single-ended input lines or 8 differential inputs lines. The single-ended and differential inputs may be dynamically mixed. The ADC provides 12 bits of resolution. A software programmable gain amplifier provides gain from 1 to 500 and a track and hold circuit provides accurate samples. Two 12 DAC lines provide precision output voltages.

A very high precision on board reference is used to provide exceptional stability. Software auto-calibration provides a continuous accuracy of plus or minus one LSB (least significant bit).

ADC conversion time is less than 14 microseconds. This provides a usable throughput rate of over 60,000 conversions per second.

The ADC has two access modes. In "instant conversion" mode a conversion is started and completed in a single I/O read cycle. This mode requires no software driver and so is particularly convenient to use. Each read cycle completes in 13 to 14 microseconds. Instant conversion mode is accessed by reading the IP-PREC-ADC in the I/O space.

In the "pipelined" mode each read starts a new conversion cycle and simultaneously passes the previous reading on the processor. The first reading may be discarded if not needed. Pipelining has the advantage that the processor and the ADC can both be working at the same time, providing higher total throughput. A "ready" bit is provided so that the processor may poll the ADC to see if the previously started conversion cycle has completed. Pipelined mode is accessed by reading the IP-PREC-ADC in the memory space.

An internal track and hold circuit is provided to aid in accurately measuring time varying signals. The IP-PREC-ADC changes from track to hold mode automatically as a conversion is initiated. The track and hold may also be placed in hold mode from an external signal. Driving either the Strobe pin on the logic interface or the Hold line on the I/O interface will place the track and hold into the hold mode. Typically a precision external timing circuit is used. The user must coordinate this circuit with the software accessing the IP-PREC-ADC. Prior to entering Hold, the control register must be set up to the correct channel and gain, and settling times must be met. After driving Hold externally, the software would perform a conversion, which may be either direct or pipelined mode. Following the start of the conversion the Hold line must be released so that a new sample may be obtained.

A single 16-bit read/write control register provides access to the channel select, gain setting, input mode, ready bit and calibration functions. Since this is a read/write control register bit field operations are supported (because these are implemented as read-modify-write cycles). Both 8-bit and 16-bit read cycles are supported, however only 16-bit (word) write cycles may be used to update the control register.

Each of the two DAC channels is individually pin selectable for 0 to 5 volt or 0 to –5 volt output. Both DACs may be written to simultaneously for tracking mode operation.

Both the ADC input and the DAC output are 12 bits. These bits are aligned in the least significant 12 bits of a 16 bit word. The upper four bits are discarded on DAC writes, and should be ignored on ADC reads. All ADC read cycles and DAC write cycles must be 16-bits (word) wide.

The IP-PREC-ADC conforms to the Industry Pack Interface Specification. This guarantees compatibility with multiple carrier boards, busses and form factors. This compatibility permits application code migration between otherwise incompatible systems and therefore provides for a longer life of the customers‘ software investment.

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Connection to the IP-PREC-ADC is via a standard 50-conductor ribbon cable. This cable may be terminated in a 50 position screw terminal block, available from SBS and other manufacturers, or any user-determined hardware. All of the ADC inputs are alternated on the cable with virtual grounds. These virtual ground pins are driven with a low impedance source that tracks the local analog ground without introducing any noise back into the local ground from the cable. This source is also protected against shorting the virtual ground wires to any power supply in the range of –12 volts to +12 volts. Differential inputs are on conductors two wire apart. This short spacing minimizes any differential temperature effects that could reduce the accuracy of a reading by introducing unwanted thermocouple voltages.

The four software programmable gain settings: 1, 5, 50, 500 provide for direct input of a wide range of sensors and instrumentation. All input ranges provide for symmetric bipolar input. This means that polarities do not have to observed when connecting sensors. Over voltage protection is provided from –22 to +22 volts, when the IP-ADC is powered.

The gain of 500 is suitable for direct input of thermocouple sensors. Megohm biasing resistors may optionally be switched in under software control for isolated sources, such as thermocouples. High current (100 mA) +5V and -5V precision voltages sources are provided for driving bridges. These voltage sources may also be used to provide an accurate, calibrated reference voltage to signal conditioning hardware or other analog functions.

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VMEbus Address Map

IP-PREC-ADC is accessed using 16-bit words only. It may be accessed in either the I/O space or the memory space of the carrier board. The ADC performs differently depending on which space is used. The control register and the DACs operate the same independent of whether I/O or memory space is used for access.

Shown below in Table 1 is the memory map of the IP-PREC-ADC.

Address	Access	Function
base + $0	read/write	16-bit control and status register
base + $10	read	ADC
base + $20	write	DAC channels A and B
base + $22	write	DAC channel B
base + $24	write	DAC channel A

Note: All accesses are word wide (16-bit). I/O reads of the ADC are instant access. Memory reads of the ADC are pipelined.

Table 1. Address Map of IP-PREC-ADC

On the next page the bits in the Control Register are shown in Table 2.

Control Register at location base + 0

bit:15	14	13	12	11	10	9	8	
	L	C	C	C	H	A	A	A

bit: 7	6	5	4	3	2	1	0	
	R		G	G		S	S	S

SSS = channel select
GG = gain select
R = ready (pipelined mode)
AAA = alternate select
H = high channel group enable
CCC = calibrate select
L = low channel group enable

Table 2. Bit Assignments of the Control Register

See the next section, Control Register, for the detailed description of the above bits. Bits 3 and 6 are not used. They are initialized to 1 on reset. They will read back either a 0 or 1 if written and can be used for user storage functions.

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Control Register

The 16-bit control register contains seven fields, shown on the previous page in Table 2. The text below describes the function of each field. Examples of usage are given in the following section, Programming. Figure 3 contains a block diagram of the ADC section of the IP-ADC. This figure will be helpful in pulling together the various aspect of controlling the ADC.

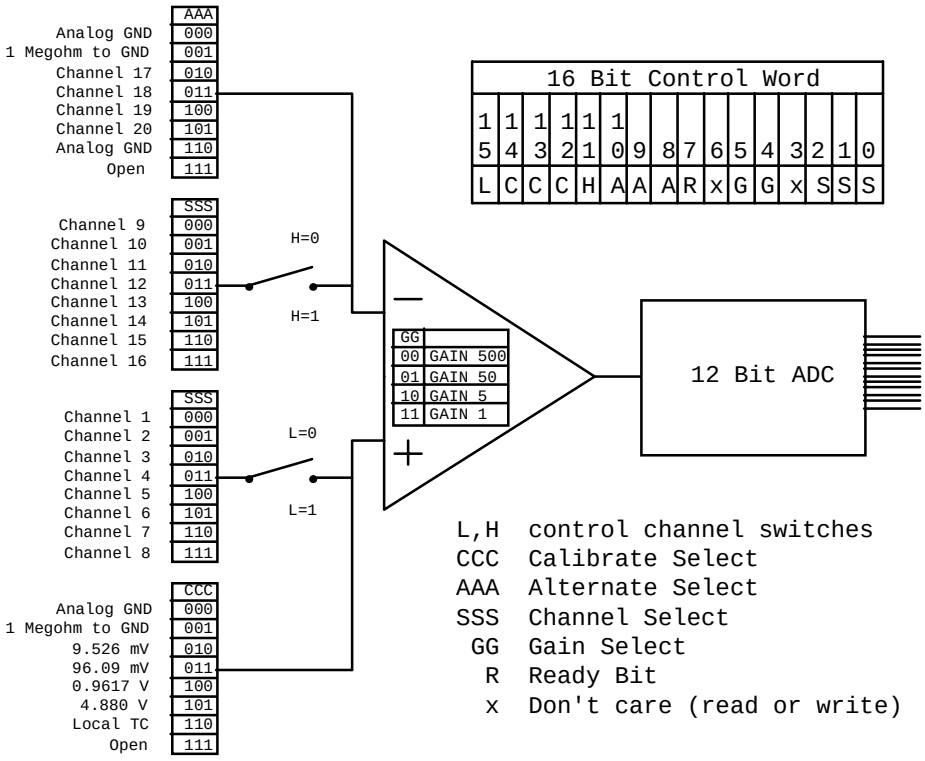


Figure 3. Diagram of ADC including Control Register

Channel Select [2..0]: SSS

This three bit field selects the basic input channels. The field is used in both differential and single-ended mode. See Table 3, below.

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Differential Input Channel	Channel Select [2..0]
1	000
2	001
3	010
4	011
5	100
6	101
7	110
8	111

Note: In Differential Mode both bits 11 and 15 must be set to 1.

Table 4. Differential Input Channel Selection

Input Channel	Channel Select [2..0]	Low Group Enable [15]	High Group Enable [11]
1	000	1	0
2	001	1	0
3	010	1	0
4	011	1	0
5	100	1	0
6	101	1	0
7	110	1	0
8	111	1	0
9*	000	0	1
10*	001	0	1
11*	010	0	1
12*	011	0	1
13*	100	0	1
14*	101	0	1
15*	110	0	1
16*	111	0	1

Table 5. Single-Ended Input Channel Selection

*Note 1: Channels 9 through 15 read out in reverse polarity in single-ended mode.

Note 2: All single-ended channels require that the Alternate or Calibrate Select input be set to Ground. See below for details.

Gain Select [5..4]: GG

This two bit field defines the input gain. See Table 6 below.

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Gain Value	Input Range	Gain Select [5..4]
1	-5 to +5 V	11
5	-1 to +1 V	10
50	-100 to +100 mV	01
500*	-10 to +10 mV	00

*Gain of 500 is designed for direct reading of thermocouple and bridge inputs.

Table 6. Gain Selection

Ready [7]: R

This one bit field is read-only. Any written value will be ignored. If Ready is low, the ADC is the process of converting and must not be read. If Ready is high, the ADC is done, and may be read or a new conversion cycle started. This bit is provided primarily for use in the pipelined mode of operation.

Pipeline mode consists of reading the ADC in the memory space (at base + $10). In this mode the prior reading is returned to the processor immediately and a new reading is starting simultaneously. The first reading may be discarded if desired. In this mode the ADC must not be read until it has completed the conversion. Use either an explicit processor delay of 14 microseconds or poll the Ready bit.

Alternate Select [10..8]: AAA

This three bit field is used during calibration, and to read channels 17 through 20. See Table 7 below.

Input	Alternate Select (bit 10..8)	High Group Enable (bit 11)	Notes
Analog Ground	000	0	Use for single-ended channels 1 through 8 and calibration.
1 Megohm to Ground	001	1	Use to ground to floating thermocouples
Ch 17	010	0	Read Ch 17 inverted.
Ch 18	011	0	Read Ch 18 inverted.
Ch 19	100	0	Read Ch 19 inverted.
Ch 20	101	0	Read Ch 20 inverted.
Local TC.	110	0	For local temperature calibration.
Open	111	1	Use for all other inputs.

Table 7. Alternate Select

High Channel Group Enable [11]: H

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Setting this bit to 1 enables channels 9 through 16. This bit must also be high for all differential channels. Setting this bit low disables channels 9 through 16. Use the low setting for calibration, single-ended reading of 1 through 8 and 17 through 20.

Calibrate Select [14..12]: CCC

This three bit field is used primarily for calibration. See Table 7.

Input	Calibrate (bits 14..12)	Low Group Enable (bits 15)	Notes	
Analog Ground	000	0	Use for single ended channels 9 through 20.	
1 Megohm to Ground	001	1	Use to ground floating thermocouples	9.5259 mV
010	0	Gain = 500 calibration.		
96.089 mV	011	0	Gain = 50 calibration.	
961.72 mV	100	0	Gain = 5 calibration.	
4.8801 V	101	0	Gains = 1 calibration.	
Local TC	110	0	For local temperature	open 111
1	Use for all other inputs.			

Table 8. Calibrate Select

Low Channel Group Enable [15]: L

Setting this bit to 1 enables single-ended channels 1 through 8. This bit must also be high for all differential channels. Setting this bit to 0 disables channels 1 through 8. Use the low high setting for calibration and single-ended reading of 9 through 20.

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Programming

This section contains example usages of the control register.

The following tables gives examples of the control register usage. First are shown isolated fields for different functions. Then complete control registers examples are given. The control register is shown in both binary and hexadecimal.

Binary Control Register	Hex	Function
---- ---- --11 ----	XX	Gain of 1
---- ---- --10 ----	XX	Gain of 5
---- ---- --01 ----	XX	Gain of 50
---- ---- --00 ----	XX	Gain of 500
0000 0000 XX11 XXXX	00--	GND (gain of 1)
0000 0000 XX00 XXXX	00--	GND (gain of 500)
1001 1001 ---- ----	99--	1 Megohm resistors to ground for floating diff. input.
1111 1111 ---- ----	FF--	Differential input for non-floating sensors.
1111 1000 ---- ----	F8--	Grounding low side of differential sensor.
1000 1111 ---- ----	8F--	grounding high side of differential sensor.
0000 0000 1011 0000	00B0	Reading local ground for offset calibration gain = 1.
0101 0000 1011 0000	50B0	Reading calibrator 4.8801 volts, gain = 1.
0100 0000 1010 0000	40A0	Reading calibrator 961.72 mV, gain = 5.
0011 0000 1001 0000	3090	Reading calibrator 96.089 mV, gain = 50.
0010 0000 1000 0000	2080	Reading calibrator 9.5259 mV, gain = 500.

Table 9. Control Register Usage examples by field.

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Binary Control Register	HEX	Function
1111 1111 00gg 0000	FF--	Differential Input Ch 1
1111 1111 00gg 0001	FF--	Differential Input Ch 2
1111 1111 00gg 0010	FF--	Differential Input Ch 3
1111 1111 00gg 0011	FF--	Differential Input Ch 4
1111 1111 00gg 0100	FF--	Differential Input Ch 5
1111 1111 00gg 0101	FF--	Differential Input Ch 6
1111 1111 00gg 0110	FF--	Differential Input Ch 7
1111 1111 00gg 0111	FF--	Differential Input Ch 8
1111 0000 00gg 0000	F0-0	Single-ended Input Ch 1
1111 0000 00gg 0001	F0-1	Single-ended Input Ch 2
1111 0000 00gg 0010	F0-2	Single-ended Input Ch 3
1111 0000 00gg 0011	F0-3	Single-ended Input Ch 4
1111 0000 00gg 0100	F0-4	Single-ended Input Ch 5
1111 0000 00gg 0101	F0-5	Single-ended Input Ch 6
1111 0000 00gg 0110	F0-6	Single-ended Input Ch 7
1111 0000 00gg 0111	F0-7	Single-ended Input Ch 8
0000 1111 00gg 0000	0F-0	Single-ended Input Ch 9
0000 1111 00gg 0001	0F-1	Single-ended Input Ch 10
0000 1111 00gg 0010	0F-2	Single-ended Input Ch 11
0000 1111 00gg 0011	0F-3	Single-ended Input Ch 12
0000 1111 00gg 0100	0F-4	Single-ended Input Ch 13
0000 1111 00gg 0101	0F-5	Single-ended Input Ch 14
0000 1111 00gg 0110	0F-6	Single-ended Input Ch 15
0000 1111 00gg 0111	0F-7	Single-ended Input Ch 16

Table 10. More Control Register Usage examples by field.
Note : gg is gain. See top entries in table for gain settings.

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Binary Control Register	Hex	Function
1001 1001 1111 1000	99F0	Differential Input Ch 1 W/ RES
1001 1001 1111 1001	99F1	Differential Input Ch 2 W/ RES
1001 1001 1111 1010	99F2	Differential Input Ch 3 W/ RES
1001 1001 1111 1011	99F3	Differential Input Ch 4 W/ RES
1001 1001 1111 1100	99F4	Differential Input Ch 5 W/ RES
1001 1001 1111 1101	99F5	Differential Input Ch 6 W/ RES
1001 1001 1111 1110	99F6	Differential Input Ch 7 W/ RES
1001 1001 1111 1111	99F7	Differential Input Ch 8 W/ RES
1111 0000 1111 1000	F0F8	Gain = 1, Single-ended Channel 1
1111 0000 1110 1000	F0E8	Gain = 5, Single-ended Channel 1
1111 0000 1101 1000	F0D8	Gain = 50, Single-ended Channel 1
0000 1111 1111 1000	0FF8	Gain = 1, Single-ended Channel 9
0000 1111 1110 1000	0FE8	Gain = 5, Single-ended Channel 9
0000 1111 1101 1000	0FD8	Gain = 50, Single-ended Channel 9

W/ RES means "with 1 Mohm pull-down resistor."

Table 11. Examples showing all bits of the Control Register.

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Accuracy

In any analog circuit there are many factors that determines its overall accuracy. In general, few of these factors must be understood by the user for effective use of the IP-PREC-ADC. This section provides some basic discussion of accuracy.

For more detailed information see the manufacturer's data sheets for the input multiplexors, the differential amplifier, the ADC and DAC ICs, and the buffer amplifiers.

DC Accuracy

There are two errors that affect basic DC accuracy. The first is zero error, or "offset." This is the error that the ADC makes when reading its own analog ground on single-ended, or shorted input terminals on differential input. This error is corrected by subtracting the known error from all readings.

The second error is gain error. Gain error is the difference between the ideal gain and the actual gain of the instrumentation amplifier, track and hold, and ADC, after offset is corrected. Gain error is corrected by multiplying readings by a correction factor. The closer the correction factor is to one, the less the gain error. Gain error is always corrected after the offset correction.

There are separate offset and gain correction factors for each of the four gain settings on the IP-PREC-ADC. Thus there are a total of eight calibration values. Only two of these are used to correct any one reading.

Analog to digital converters are sometimes specified by both their uncorrected and their corrected accuracy. Since it is expected that the IP-PREC-ADC will always be used in the corrected mode, only the corrected accuracy is specified. Information on uncorrected accuracy may be obtained from the manufacturer's data sheets, and by contacting SBS. The corrected accuracy is specified as plus or minus one LSB over temperature and on all gain settings, after software calibration.

The IP-ADC is factory calibrated. Calibration values are stored in the on board PROM. These values may be used to correct ADC readings and DAC output. Additional accuracy can be achieved by performing software calibration prior to a reading. The main advantage of the software calibration is compensation for the current operating temperature. Software calibration takes advantage of a very high precision (3 ppm/°C) on board reference. A separate calibration voltage is locally provided for each gain setting. The calibration algorithm measures offset and gain error on each of the four gain settings, storing these values in RAM. The software routine that reads the ADC then uses these recently computed RAM based correction factors instead of the PROM based factory-generated correction factors.

Some ADCs suffer from errors in addition to offset and gain. This error is usually called differential non-linearity. (If the error is linear, then the two standard correction factors will always provide complete correction.) The differential non-linearity of the IP-ADC is plus or minus one half LSB; this error is included in the overall accuracy specification of the IP-PREC-ADC. This specification means that the IP-PREC-ADC will have no missing codes.

For more information see the section, Calibration, refer to the manufacturer's data sheets for individual components, or contact SBS.

Settling Time

Settling time is primarily a function of gain, as the following Table shows. Input sensors that are a very high impedance may require additional settling time due to cable and input capacitance.

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Gain	Settling Time
1	15 µsec
5	15 µsec
50	35 µsec
500	200 µsec

Table 12. Settling Time vs. Gain

This settling time must be observed after switching channels or changing the gain setting.

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Track and Hold

An internal track and hold circuit is provided to aid in accurately measuring time varying signals. The IP-PREC-ADC changes from track to hold mode automatically as a conversion is initiated.

The track and hold may also be placed in hold mode from an external signal. Driving either the Strobe pin on the logic interface or the Hold line on the I/O interface will place the track and hold into the hold mode. These two pins are electrically connected on the IP-PREC-ADC. Typically a precision external timing circuit is used. The input requirements of the hold line are that a voltage of .25 or less must be maintained at a current of 2.5 mA. To restore track mode the hold line may be driven high or allowed to float high from its internal 2KΩ resistor.

The user must coordinate the external timing circuit with the software accessing the IP-PREC-ADC. Prior to entering hold, the control register must be set up to the correct channel and gain, and settling times must be met. After hold is driven externally, the software would perform a conversion, which may be either a direct or pipelined mode read. Following the start of the conversion the hold line may be released as the ADC will continue to hold until the completion of the conversion. However, the hold line must be released by the end of the conversion so that a new sample may be obtained.

Typically the external timing circuit connected to the hold or strobe line is also wired in such a way that the value may be read via a digital input or such that the high to low transition causes an interrupt.

For moderate frequencies, a square wave source for driving hold may be used. For very high and low frequencies, it is desirable to minimize the hold time to just that needed for the ADC to complete a conversion. In the case of high frequencies, this is to give the track and hold time to accurately acquire a new value. In the case of low frequencies it is to minimize droop error.

Note that the IP-PREC-ADC does not require an external hold input for accurate readings. Most software algorithms can read the ADC repeatedly to within a few microseconds (typically better) of a timer interrupt. Few sensor values will change significantly during this time.

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ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard Data for the ID PROM on the IP-PREC-ADC is shown in Table 13, below. For more information on IP ID PROMs refer to the Industry Pack Interface Specification.

The location of the ID PROM in the host's address space is dependent on which carrier is used. In a VMEbus carrier the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. In a NuBus system the ID space is specified in the carrier manual.

The ID PROM used is an AMD 27LS19A.

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3F 39	(available for user)	
37	DAC B Gain	
35	DAC A Gain	
33	DAC B Offset	
31	DAC A Offset	
2F	Gain500	
2D	Gain50	
2B	Gain5	
29	Gain1	
27	Offset 00	
25	Offset50	
23	Offset5	
21	Offset1	
1F	Error500	
1D	Error50	
1B	Error5	
19	Error1	
17	CRC	
15	No. of bytes used	($1C)
13	Driver ID, high byte	($00)
11	Driver ID, low byte	($00)
0F	reserved	($00)
0D	Revision	($B1)
0B	Model No IP-PREC-ADC	($15)
09	Manufacturer ID SBS	($F0)
07	ASCII "C"	($43)
05	ASCII "A"	($41)
03	ASCII "P"	($50)
01	ASCII "I"	($49)

Table 13. ID PROM Data (hex)

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Calibration

This section of the manual describes how to use the calibration data stored in the ID PROM. If an existing driver routine is being used, then the information is this section may already have been incorporated, and the user need not worry about calibration further.

Refer to the section on Accuracy for a more detailed discussion of definitions and sources of errors.

For copy of the factory calibration procedure, which explains in detail how each calibration number is derived, please contact SBS.

All errors are considered to be linear. For each of the four gain settings of the ADC two correction number are used. One corrects for offset (or zero) error, and the second corrects for gain (or span) error.

The calibration prom holds all correction numbers in units of 1/4 LSB. The correction numbers are treated as a signed byte (-128 to +127). In this section, all numbers shown are in decimal, unless preceded by a dollar sign ($). All equations in this sections are in units of bits unless otherwise labelled.

All inputs are bipolar. Zero corresponds to a hexadecimal reading on the ADC of $800. The maximum positive reading is $FFF, or 2047. The maximum negative reading is $000. It is assumed that the user converts the 12-bit reading to an appropriate signed number before applying the following correction algorithms.

To maintain necessary accuracy in the implementation of these algorithms it is recommended that the programmer use 32-bit signed integers, where 16 bits represents the equivalent ADC reading in bits, and 16 bits represents the fractional LSBs (least significant bits). This permits the use of fast integer arithmetic, without worrying about introduction computational rounding errors, or limiting range. Note that since the numbers stored in the calibration prom are in units of 1/4 LSB, they require normalization prior to computation.

The numbers in the calibration prom are signed 8-bit integers with units of 1/4 LSB. To normalize to the recommended data format in the previous paragraph, (i) sign extend from 8-bits to 32-bits, then (ii) shift left arithmetically (keeping the sign) 14 bits.

The Ideal Case

If there were no analog errors whatsoever, then the following would be true. The goal of the various correction factors and algorithms is to get as close to this ideal as possible.

1. The on board reference would produce +5.000 and –5.000 volts.

2. Full scale for both the ADC and the DAC is defined as 4096 counts. The ADC input, which is bipolar, actually ranges from
   0 counts to +4095. The DAC output ranges from 0 to 4095. Note that in both cases full scale (4096 counts) is not reachable.

3. For the ADC, one LSB is defined as taking the voltage of the full scale range and dividing by 4096.

Gain	Ideal Range	One LSB
1	-5 to +5 V	2.4414 mV
5	-1 to +1 V	.48828 mV
50	-100 to +100 mV	.048828 mV
500	-10 to +10 mV	.0048828 mV

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4. An ADC reading of zero, or $800, would correspond to an input of zero volts. Or more precisely, the transition from 0 to 1 would occur at one half LSB.

5. For the DAC, one LSB is defined as taking the full scale voltage of 5 volts dividing by 4096 to get 1.2207 mV.

ADC

The basic formula for correcting any ADC reading is:

$$Value = (Reading - Offset) * (1 + Gain/2048)$$

Value is the corrected input signal, Reading is the number read from the ADC, Gain is one of four correction factors from the calibration prom, Offset is also one of four correction factors from the calibration prom. The formula is in units of bits. Note that stored numbers in the calibration prom require normalization.

Gain and Offset correction factors are stored for each for the four possible programmable gain settings. These factors are called Gain1, Gain5, Gain50 and Gain500, with similar names for the four Offset factors. See Table 13 above for the locations in the calibration prom.

Please see the section titled ADC Calibration Code for sample 68000 code which performs this calibration using integer arithmetic.

DAC

The basic formula for correcting any DAC output is:

$$Data = Value * (1 + Gain/4096) - Offset$$

Data is the number that will be sent to the DAC. Value is the desired output voltage (in the range of 0 to 4095). Offset and Gain are stored separately for DAC channels A and B. They are called DAC A Offset and DAC A Gain with similar names for channel B. See Table 11 above for the locations in the calibration prom.

DAC output is 0 to +5 V or 0 to –5 V. The selection of output range in made via shunts. See the section User Options for shunt positions. Each DAC is independently configurable. In either case an output of zero corresponds to the hex data $000, and the full scale output corresponds to the hex data $FFF.

Note that the user's algorithm should check Data for underflow (below 0) and overflow (over 4095) after computation prior to output.

Calibrator

The IP-PREC-ADC includes an on board calibration circuit. This circuit produces four accurate voltages, which may be read under software control by the IP.

The precise value of each of the four calibration voltages may be calculated from values stored in the calibration prom. The formulas are:

$$V1 = 4.87915 + (Error1 * .000610352) \text{ volts}$$
$$V5 = .961548 + (Error5 * .00012207) \text{ volts}$$
$$V50 = .096069 + (Error50 * .000012207) \text{ volts}$$

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V500 = .00952393 + (Error500* .0000012207) volts

V1 through V500 are the four actual calibration voltages. Error1 through Error500 are four factors stored in calibration prom. See Table 11 above for the location of these numbers. Interpret the stored Error numbers as signed 8-bit integer.

(Error1 through Error500 are actually in units of 1/4 LSB for each of the four corresponding gain ranges. The formulas above take this into account, however, since the multipliers .000610352 through .0000012207 are “volts per 1/4 LSB” for each range.)

Note that the four calibration voltages are roughly 95 - 98% of positive full scale for each gain range.

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ADC Calibration Code

```
;-----------------------------------------------------------------
;   CALLED FROM PASCAL AS FOLLOWS:
;
;  PROCEDURE READCALADC(ADCBASEPTR, ADCIDPTR: PTR; DATPTR : LONGINTPTR); EXTERNAL;
;
;   NOTE:    THIS ROUTINE SHOULD IDEALLY BE SPLIT INTO TO FUNCTIONAL SECTIONS
;         THE FIRST SEDTION, CALLED INIT, PREPARES CONVERSION DATA WHICH NEED
;         ONLY BE CALCULATED ONCE.  THIS DATA WOULD BE STORED FOR LATER USE BY...
;         THE SECOND SECTION, CALLED CORECT, WHICH READS THE ADC AND PERFORMS
;         THE MANIPULATIONS REQUIRED ON EACH ADC READING.  DATA RETURN METHOD
;         CAN BE MODIFIED AS DESIRED.
;
;
;         THIS PROGRAM WRITTEN JULY 1999 BY CHRIS SCHAEFER
;         COPYRIGHT 1990 SBS
;
;         REVISION HISTORY:
;
;
;

          MACHINE      MC68020
          INCLUDE   'SYSEQU.A'


READCALADC    PROC   EXPORT


GAIN1     EQU $19                    ; OFFSET TO GAIN1 IN IDPROM
OFFSET1   EQU $21                    ; OFFSET TO OFFSET1 IN IDPROM
ADC    EQU$22             ; OFFSET TO ADC PORT ON NUBUS.  VME IS DIFFERENT.

          MOVEA.L   (A7)+,A0         ; REMOVE RETURN ADDRESS
          MOVE.L (A7)+,D2         ; DATPTR
          MOVE.L (A7)+,D1         ; ADCIDPTR
          MOVE.L (A7)+,D0         ; ADCBASEPTR
          MOVE.L A0,-(A7)         ; REPLACE RETURN ADDRESS
          MOVEM.L   A1/A2/D1-D4,-(A7)   ; SAVE REGISTERS TO STACK


INIT:     ADDI.L  #$FD000000,D0      ; NUBUS HACK TO PROVIDE PROPER 32 BIT ADDRESS
          ADDI.L  #$FD000000,D1
          MOVEA.L   D0,A0            ; LOADS BASE POINTER OF IP
          MOVEA.L D1,A1           ; LOADS THE ID BASE POINTER
          MOVEA.L D2,A2           ; LOADS THE DATPTR

          CLR.L  D0               ; CLEARS D0
          MOVE.B GAIN1(A1),D0     ; LOADS THE GAIN REGISTER INTO D0
          EXT.W  D0               ; SIGN EXTENDS D0 TO A WORD
          SWAP   D0     ; SWAP UPPER AND LOWER WORD TO CREATE SIGNED 16 BIT WITH
FRACTION

          MOVE.B  #$0D,D4         ; CONVERT QUARTERBITS TO BITS  AND
          ASR.L  D4,D0            ; SHIFT ELEVENBITS RIGHT, DIVIDING BY (WIDTH OF
ADC)DIV 2
                                  ; NOTE, SPAN IS DEFINED AS ZERO VOLTS TO FULL SCALE
                                  ; WHICH ON THIS BIPOLAR ADC IS $800 TO $FFF HENCE
ONLY
                                  ; HALF OF FULL SCALE OR 11 BITS
                                  ; THIS CREATES PART OF THE MULTIPLIER
          ADDI.L #$10000,D0          ; ADDS ONE TO CREATE WHOLE GAIN CORRECTION
MULTIPLIER
                                  ; THIS IS A 16 BIT NUMBER WITH 16 BIT FRACTION

          CLR.L     D1            ; NOW WE WILL DO OFFSET-----
          MOVE.B OFFSET1(A1),D1       ; LOAD IN 1/4 BIT VALUE
          EXT.W  D1               ; SIGN EXTEND IN WORD
          SWAP   D1               ; SWAP TO CREATE SIGNED 16 BIT NUMBER WITH 16
FRACTION
          ASR.L  #$02,D1             ; D1 IS OFFSET CORRECTION
```


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```
CORECT:   MOVE.W ADC(A0),D3          ; READS IN ADC VALUE
          ANDI.L #$0FFF,D3        ; MASKS UNWANTED BITS
          SWAP   D3               ; CREATES 16 BIT NUMBER WITH 16 BIT FRACTION

          ADD.L  D1,D3            ; ADDS OFFSET AND STORES IN D3
          MULS.L D0,D4:D3         ; MULTIPLIES THE GAIN CORRECTION AND STORES IN D4
                                  ; D3 IS NOW THE FRACTION COULD BE DISCARDED  OR
                                  ; WE COULD ADD $8000 TO D3, CHECK FOR CARRY AND ADD
                                  ; THIS TO D4, SO THAT WE ROUND THE FRACTION

                                  ; BUT INSTEAD WE CHOOSE TO MOVE TO A 24 BIT NUMBER
WITH 8
                                  ; BIT FRACTION AS FOLLOWS :
          LSL.L  #$8,D4           ; SHIFT 3 LEAST SIGNIFICANT BYTES UP BY ONE BYTE
          MOVE.B  #$18,D0
          LSR.L  D0,D3            ; SHIFT MOVE SIGNIFICANT BYTE TO LEAST SIGNIFICANT
          ADD.L  D4,D3            ; CREATES A LONGINT WHICH IS 24 BITS PLUS 8 BIT
FRACTION

          MOVE.L D3,(A2)          ; PUT THE RETURNED DATA INTO LOCATION POINTED TO IN
CALL
          MOVEM.L   (A7)+,A1/A2/D1-D4   ; POP ALL THOSE REGISTERS

          RTS

          ENDP


          END
```

Table 14. Sample Code for use of ADC calibration data

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User Options

There are two jumpers on the IP-PREC-ADC that the user may set to change the range of the two optional DACs. The choices are 0V to +5V or 0V to –5V for each DAC.

DAC	Shunt Position	Output Range
DAC A	E2-1 to E2-2	0 to –5 V
DAC A	E2-2 to E2-3	0 to +5 V
DAC B	E1-1 to E1-2	0 to –5 V
DAC B	E1-2 to E1-3	0 to +5 V

Note: Default ranges are 0 to +5 V.

Table 15. DAC Output Options

Users may install resistors across any or all of the differential channel input lines. These resistors are useful to convert a current output sensor, or current transmitter, to voltage. The accuracy of this current to voltage conversion will depend on the resistor used.

To convert a 4 to 20 mA current source to a 0 to 1 volt range, use a 50.0 ohm resistor. (This produces a .2 to 1.0 volt range.) If the source if floating, then grounding one end (either externally or via the programmable options) will produce a 0 to .8 volt range.

Differential Channel	Resistor Location
Ch 1	R1
Ch 2	R2
Ch 3	R3
Ch 4	R4
Ch 5	R5
Ch 6	R6
Ch 7	R7
Ch 8	R8

Table 16. Input Current Conversion Resistor Locations

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Construction and Reliability

Industry Packs were conceived and engineered for rugged industrial environments. The IP-PREC-ADC is constructed out of 0.062 inch thick FR4 material. The six copper layers consist of a power plane, ground plane, and four signal planes. The power and ground planes significantly reduce analog noise. The analog ground is connected to the digital ground at one point. The two solid planes also aid in maintaining a constant temperature across the IP. This avoids errors due to temperature gradients. Solder mask covers exposed traces on both sides.

Both surface mount and through hole components are used. Surface mount components are installed automatically and epoxied to the board. They are soldered by infrared reflow, then inspected. Programmable and replaceable components are placed in low profile sockets. These sockets are screw-machined pins, gold plated. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed component into the socket after final options are selected.

Completed boards pass an in-circuit automated test, as well as visual and function tests.

After burn-in, units are calibrated with semi-automated procedure using instrumentation traceable to NBS standards. After calibration a custom PROM is made and installed. Final tests are performed, verifying proper calibration and functionality.

After final test, the factory applies labels and coats both the component and solder side of the IP with a Conformal Coating. This Acrylic Resin based coating meets MIL-I-46058C Type AR. The coating provides a significant barrier to humidity, salt, corrosive vapors, fungus and airborne particulates. The dielectric strength is 2500 volts. This clear coating is UV detectable for inspection.

Some user options require installing shunts—0.100 inch shorting clips that push onto 0.025 inch square posts. Both the shunts and the posts are gold plated. For highest reliability, wire-wrap™ may be used in place of the shunts.

The Industry Pack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP can be secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The Industry Pack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

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Specifications

Logic Interface	Industry Pack™ Logic Interface
I/O Interface	50-conductor flat cable
Analog Input	Inputs and mode are software selectable. 8 differential inputs shared with 16 single-ended inputs, 4 dedicated single-ended inputs
Track and Hold	Automatic with conversion, External hold input
External Hold Delay	< 200 nsec
T & H Droop	15 µV/msec typ @ 25°C (gain = 1) .006 LSB/msec typ all ranges
Analog Output	2 DAC outputs
Input Range	Gain is software selectable Gain = 1 –5 to +5 V Gain = 5 –1 to +1 V Gain = 50 –100 to +100 mV Gain = 500 –10 to +10 mV
Output Range	0 to +5V or 0 to –5V pin selectable
Resolution	12 bits all Analog inputs and outputs
Accuracy	Plus or minus one LSB, after calibration
Conversion Time	14 µseconds, ±1 µsecond May be pipelined with processing
Throughput	Over 65,000 samples per second
Input Options	Floating, Differential, Single-ended, 1 MegΩ for biasing thermocouples
Input Bias Current	±30 nA typ @ 25°C
Input Capacitance	55 pF typical
Bridge Drive:	±5 V @ 100 mA
Access Modes	Instant Conversion or Pipelined.

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Calibration	On board 3 ppm/°C Reference. Offset and Gain factory calibrated all ranges, to NBS traceable accuracy of ±1/4 LSB. On board calibration voltages provided for all ranges
Correction	Supplied software performs auto-calibration and auto-correction of all readings
Over voltage	±22 V with power on ±10 V with power off
Initialization	Reset forces Gain =1, No input channel selected.
Access Modes	Word access in I/O or memory space
Wait States	No wait states on control register access No wait state on DAC output One wait state Pipelined ADC reads 13 to 14 µsec Instant ADC conversion
DMA	Basic DMA read in the memory space for pipelined conversion.
On board Options	Range on DAC outputs
Interface Options	50-pin flat cable, 50 screw terminal block interface
Dimensions	1.8 inches x 3.9 inches x 0.344 inches
Construction	Conformal coated FR4 6-layer printed circuit, SMD and through-hole components Calibration provided in PROM
Temperature Coefficient	0.89 W/°C for uniform heat across IP
Power	125 mA @ +5V typical 25 mA @ +12 V typical 15 mA @ –12 V typical
Environmental	Operating temperature +10° to +50°C Humidity 5 - 95% non-condensing Storage temperature –10° to +85°C

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Pin Assignment of Signal Names

Industry Pack Logic Interface

Signal Names				Pin No			
GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSel*		4		29
D1		DMAreq0*	5		30		
	D2		MemSel*		6		31
D3		n/c		7		32	
	D4		n/c		8		33
D5		n/c		9		34	
	D6		IOSel*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		n/c		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		A5		20		45
BS1*		Strobe*	21		46		
	–12V		A6		22		47
+12V		Ack*		23		48	
	+5V		n/c (+5STBY)	24		49	
GND		GND		25		50	

Note: The no-connect (n/c) signals above are defined by the Industry Pack Logic Interface Specification, but not used by this IP. See the Specification for more information.

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Interface Pin Assignment

Channel 1 +		1	
	Shield Drive		2
Channel 1 – (Ch 9 in single-ended)		3	
	Shield Drive		4
Channel 2 +		5	
	Shield Drive		6
Channel 2 – (Ch 10 in single-ended)		7	
	Shield Drive		8
Channel 3 +		9	
	Shield Drive		10
Channel 3 – (Ch 11 in single-ended)		11	
	Shield Drive		12
Channel 4 +		13	
	Shield Drive		14
Channel 4 – (Ch 12 in single-ended)		15	
	Shield Drive		16
Channel 5 +		17	
	Shield Drive		18
Channel 5 – (Ch 13 in single-ended)		19	
	Shield Drive		20
Channel 6 +		21	
	Shield Drive		22
Channel 6 – (Ch 14 in single-ended)		23	
	Analog Ground (Local TC –)	24	
Local TC +	25		
	Shield Drive		26
Channel 7 +		27	
	Shield Drive		28
Channel 7 – (Ch 15 in single-ended)		29	
	Shield Drive		30
Channel 8 +		31	
	Shield Drive		32
Channel 8 – (Ch 16 in single-ended)		33	
	Shield Drive		34
Channel 17	35		
	Analog Ground		36
Channel 18	37		
	DAC A Output		38
Channel 19	39		
	DAC B Output		40
Channel 20	41		
	Shield Drive		42
reserved		43	
	Ready Output		44
+12 P2		45	
	–12 P2		46
n/c		47	
	Hold Input		48
+5.000 V Drive Output		49	
	–5 .000V Drive Output		50

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