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Find the *Abaco Systems / SBS / Greenspring IP-PWI* at our website: ***Click HERE***

IP-PWI

IndustryPack® with 3 Channel Pulse Width Input

Features

- Selectable Trigger Modes:
  - Software Trigger
  - External Frame Trigger Input
  - Free Run
  - Software Trigger may drive Frame Trigger Out
- Fame Trigger:
  - 16-bit Programmable Timer, in increments of 100 nsec, minimum frequency 153 Hz, RS-422 output
- Channel Trigger
  - Triggered by the Frame Trigger
  - Individual drivers for each channel
  - Programmable width, in 100 nsec intervals up to 25 µsec,
  - All channels driven simultaneously
- Construction:
  - ICs SMT CMOS
  - 6 layer PCB
  - Internal solid ground plane
  - All connectors gold plated

IP-PWI (Pulse Width Input) is a 3 channel single-high IndustryPack designed to accurately measure the width an input pulse with a resolution of 8.333 nanoseconds minimum. IP-PWI is ideal for interface to MTS Corporation's Temposonics® transducers. Multiple IPs may be ganged in this application to drive all the transducers in a system simultaneously. All outputs and inputs are at differential RS-422 electrical levels.

The IP provides a dedicated 18-bit pulse width counter for each channel, running off of a common FAST clock generated by an on board, software programmable, high frequency clock synthesizer. Special precautions have been taken to eliminate metastability problems at this high clock rate.

The maximum FAST clock frequency is 120 MHz with 100 MHz, 68 MHz, 47 MHz, 34 MHz being alternative clock frequency choices. The nominal 15 MHz synthesizer input crystal can be changed to provide other FAST clock frequency choices if necessary, on special order. A software programmable divider divides the high frequency clock to provide a SLOW clock with a 100 nanosecond nominal period (8.333 nanoseconds at the fastest clock frequency).

A master trigger generator provides triggering from a software programmable bit, an external I/O input, or an internal 16-bit binary programmable timer that uses the SLOW clock to provide a repetitive trigger clock in the frequency range of 153 Hz to 5 MHz. This Master trigger generator output is delivered to the I/O connector.

Typically a single IP-PWI's Master trigger out is wired to all of the system IP-PWI IP Frame Trigger inputs to achieve system-wide synchronous (simultaneous trigger) operation.

The IP-PWI provides a dedicated Trigger Pulse Generator for each channel. The Trigger Pulse Generators are individually programmable to generate pulses from 1 to 255 SLOW clock periods wide, typically offering a pulse width range of 100 nanoseconds to 25.5 microseconds. The Trigger Pulse Generators are themselves triggered by either an identical and simultaneous Frame Trigger input pulse or by individual software programmable bits for each channel.

A programmable interrupt may be used to indicate several completion conditions or receipt of the frame trigger signal. Completion conditions are (1) all input pulses terminated or (2) at least one input pulse terminated with all channels being individually maskable. The status of each channel may be individually checked at any time via the busy bit in that channel's status register.

Each channel's busy bit is also brought out to the I/O connector as an open collector signal with a weak pullup resistor. These outputs may be connected together in a "wire-AND" configuration allowing a single interrupt to signal input pulse completion of all channels. Many IP-PWI boards can be so connected. To increase flexibility, a stronger pullup resistor is also provided for each channel on other dedicated I/O connector pins.

All inputs and outputs on the IP-PWI are RS-422 levels with the input structure consisting of an RS-422 receiver with 120 ohm input termination. The Frame Trigger and External Trigger input termination resistors have user selectable shunts in series so that the systems integrator may select only a single IP-PWI to have the terminator(s) installed. This eliminates the problem of multiple termination.

The implementation uses the RS-422 pulse input receiver to drive a 6-bit high-speed binary counter. The output of this counter drives, in turn, a 12-bit counter. The high-speed counters are implemented with the fastest available PLD ICs, using modern low-ground-bounce very high speed CMOS in a PLCC package. The 12-bit counters are implemented, with the other IP-PWI logic, in a common 100-pin quad-pitch Xilinx field programmable logic array. This combination permits three high resolution counters to be implemented in compact single-high, low power IndustryPack.

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Pin Assignment

Pin No.	Channel	Function	Notes
1	all	GND	
2	all	F Trig IN +	Frame trigger input.
3	all	F Trig IN –	
4	all	GND	
5	all	F Trig OUT +	Frame trigger output.
6	all	F Trig OUT –	
7	all	GND	
8		GND	
9		GND	
10		GND	
11		GND	
12	1	GND	
13	1	Pulse 1 IN+	Pulse input to be measured.
14	1	Pulse 1 IN–	
15	1	GND	
16	1	GND	
17	1	Pulse 1 OUT+	Trigger for Channel 1.
18	1	Pulse 1 OUT–	
19	1	GND	
20	2	GND	
21	2	Pulse 2 IN+	Pulse input to be measured.
22	2	Pulse 2 IN–	
23	2	GND	
24	2	GND	
25	2	Pulse 2 OUT+	Trigger for Channel 2.
26	2	Pulse 2 OUT–	
27	2	GND	
28	3	GND	
29	3	Pulse 3 IN+	Pulse input to be measured.
30	3	Pulse 3 IN–	
31	3	GND	
32	3	GND	
33	3	Pulse 3 OUT+	Trigger for Channel 3.
34	3	Pulse 3 OUT–	
35	3	GND	
36		GND	
37		open	
38		open	
39		open	
40		open	
41		open	
42		open	
43		open	
44		open	
45		open	

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Pin Assignments continued

46	open
47	open
48	open
49	open
50	open

Specifications

Logic Interface	Single-high IndustryPack,
Logic Interface Specification	IndustryPack Logic Interface Specification 0.7.1
Host bus width	16-bits
Number of Channels	Three
Resolution	< 10 nanoseconds, using a 120 MHz (nom) clock
Count Depth	18-bits, each channel independent
I/O Voltage Levels	RS-422 differential signaling, all inputs and outputs Inputs are terminated with 120Ω
IP Wait States	One wait-state
Interrupts	Programmable on pulse complete, channel selectable, or all channels complete Programmable vector register
Control Register	Read-writable
User Configuration Jumpers	None
Power Requirements	+ 5.0 V, 420 mA max, measured
Times and Frequencies	Crystal controlled, frequency synthesized. Operating frequency: tbd, 120 MHz nominal Accuracy: tbd Stabilty: tbd Jitter: tbd
Environmental	Operating temperature: 0° to 70°C Humidity: 5% to 95% non-condensing Storage: –10° to + 85°C

Order Information

IP-PWI	IP with Three Pulse Width Input channels

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