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VIPC610

VME Bus IP Carrier Board with Four IndustryPack® Slots

User's Manual

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VIPC610
VMEbus IP Carrier Board
with Four IndustryPack® Slots

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Product Description

The VIPC610 VMEbus IP carrier is part of the IndustryPack® family of modular I/O components. As a carrier board, the VIPC610 provides mechanical support and the electrical interfaces to four single high IndustryPacks, or two double high IPs.

Input/output, memory, and interrupt functions are supported. Battery backup is provided on board.

VIPC610 meets VMEbus Specification C.1 (also known as IEEE P1014/D1.2 and IEC 821 bus) for 6U, or "double high," form factor. Other VMEbus IP carrier boards are available with different capabilities, including 3U (single high) form factors, on board DMA, or a 68020 processor. Carrier boards are also available for other industry standard buses, including PC/AT bus and Nubus.

The VIPC610 conforms to the IndustryPack Logic Interface Specification. This guarantees compatibility with the wide range of IndustryPacks currently available and planned.

Each of the IndustryPacks interfaces with a 50-pin flat cable header accessible through the front panel of the VIPC610. The four IP positions are generally called slots, and are identified by the letters A, B, C, and D. The interfaces to the A and C packs mate with a straight receptacle connector; the interfaces to the B and D packs mate with a right angle connector. This arrangement provides for inherent strain relief. The interface connectors are mounted directly on the VME board (not on the IPs), providing a modular and reliable cabling system. Interface cable may be inserted or removed without removing the VIPC610 from the VME chassis. IPs may be snapped in or out without interfering with the I/O cabling.

In addition to the front panel cabling, the C and D packs are also pinned out on the VMEbus P2 backplane connector. This permits more flexible cabling options in many chassis. Shunts may be removed to prevent interference with secondary buses, such as VSB. (Three IP slots are available in this configuration.)

IndustryPack I/O is mapped into the VMEbus A16/D16 space. Both user and supervisor accesses are supported, as are read-modify-write ("test and set") operations. The size of I/O on each IP is fixed by the IP Specification at 64 16-bit words. In addition each IP has an identification PROM which occupies 64 words. Thus the four IPs occupy 1024 bytes out of the VMEbus' 64 Kbyte "short I/O" space. The VIPC610 occupies a total of 2048 bytes in the short I/O space.

Interrupts are fully supported with a simple but powerful architecture. Each of the four IPs is able to generate up to two interrupt requests. These eight request lines are paired with the seven available VMEbus interrupt request levels with a simple jumper block. Alternatively to this, a user provided PLD may be installed to perform arbitrarily complex interrupt mappings. Option -01 may be ordered which maps the interrupts identically to two VIPC310 carrier boards. This option permits unmodified software to run on both 3U and 6U VMEbus systems. IndustryPacks are the only I/O system that offers these capabilities.

Power-up, power-down, and reset functions are fully supported. Power-fail detect circuitry provides a local reset function to the four IPs, assuring reliable operation of battery-backed functions.

The VIPC610 provides isolated +5V, +12V, and -12V supplies to each IP by means of passive LC *pi* filters. This permits use of precision analog IndustryPacks together with high speed digital packs in the same VMEbus slot.

Six layer PCB construction minimizes conducted and radiated EMI. Extensive use of CMOS logic reduces both heat and electrical noise, while increasing reliability. All shunt, socket and connector pins are gold plated, assuring long reliable life.

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I/O Addressing

I/O addressing on the VIPC610 is determined by two elements. The first is the base address of the board. Second is the offset of the specific IP. The setting of the base address is explained below, followed by a map showing the offsets for the four IPs. Each IP has 64 16-bit words in its I/O space. Each IP also has an ID PROM that occupies another 64 words.

The VIPC610 occupies 1024 bytes in the VMEbus "short I/O," or A16/D16 space. This consists of 64 16-bit words for each IP's I/O and ID space. The board's base address is set with six shunts, or "jumpers." The location of this E3-E7 configuration block is shown in Figure 19 near the end of this manual.

An installed shunt selects a given address line as zero. A removed shunt selects the address line as a one. Thus a base address of $0000 (in A16) is created when all six shunts are installed. A base address of $FC00 (in A16) is created when all six shunts are removed. (For many host CPU boards the A16 space is accessed by beginning a 24-bit address with $FF, or a 32-bit address with $FFFF. See your CPU's User Manual for more information on address space mapping.) The relationship of shunt locations to address lines is shown in the chart below in Figure 1. E7 and E3 may be located on the board from Figure 19 near the end of this manual. Pin one of all configuration blocks is identified with a square pin, observable on the solder side of VIPC610.

The I/O base address shunts are also used to select the memory base address for the VIPC610, if memory is enabled. As an example, if the I/O base address is $6000 (in A16 space), then the memory base address is $600000 (in the A24 space). See the section following, Memory Addressing, for more information.

Shunt Location	Corresponding Address Line
E7-7 to E3-7	A15
E7-6 to E3-6	A14
E7-5 to E3-5	A13
E7-4 to E3-4	A12
E7-3 to E3-3	A11
E7-2 to E3-2	A10

Note: E7-1, E7-2, E3-1, E3-2 are not used for I/O Base Address Selection.

Figure 1 I/O Base Address Shunt Assignment

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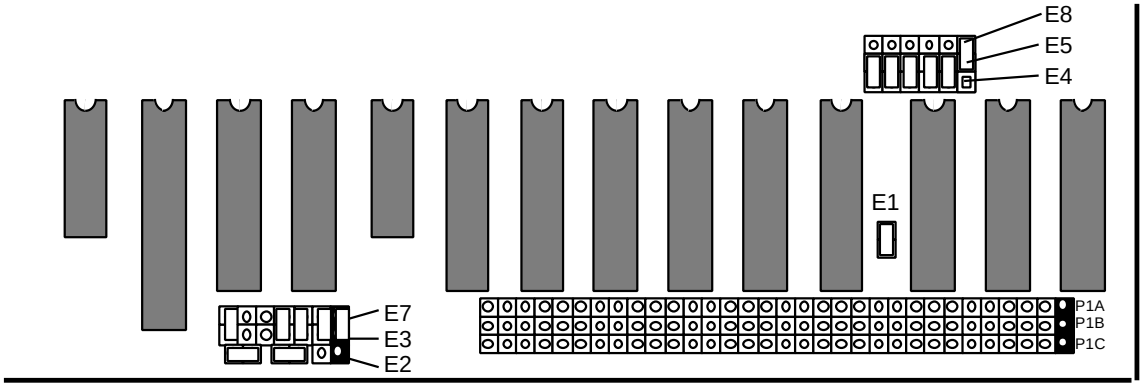


Figure 2 Default jumper setting for I/O Address of $6000.

The four IP slots are addressed on the VIPC610 as shown below in Figure 3.

Address Offset	Assignment
I/O Base + $0000	IP A, I/O Space
I/O Base + $0080	IP A, ID Space
I/O Base + $0100	IP B, I/O Space
I/O Base + $0180	IP B, ID Space
I/O Base + $0200	IP C, I/O Space
I/O Base + $0280	IP C, ID Space
I/O Base + $0300	IP D, I/O Space
I/O Base + $0380	IP D, ID Space

Figure 3 IP I/O Address Offset Assignments

Each IndustryPack has a fixed size I/O space of 64 16-bit words, which is 128 bytes ($80 bytes in hexadecimal). Many IPs use only the low order, or odd byte. In this case bytes are accessed at location offsets of $1, $3, etc. This odd byte I/O convention is a 68000 family processor and VMEbus standard. Most IPs do not use all 64 words of their allotted I/O space.

If multiple VIPC610 are used in a system they are commonly addressed in increments of $800 hex. Thus the first VIPC610 might have the factory default I/O address of $6000, the second starts at $6800, the third at $7000, etc.

Caution: Each IP may or may not decode unused bytes. If an IP does decode unused space, then accessing this space will then cause a VMEbus BERR from the offending CPU's bus timeout circuitry. If this CPU function is disabled then accessing unused space, or the space of an uninstalled IP, will cause the VMEbus to "hang." Due to partial address decoding some IP registers appear multiple times within its 64 word assigned address. An IP may or may not use even bytes in its I/O space. If it does not, it may or may respond to an even byte access. IPs may have different read and write maps. The use of a CPU's bus timeout function is recommended to detect possible invalid access attempts.

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Each IP must have an ID PROM. This ID PROM is at least 32 bytes. It provides certain fixed information about the IP, which is defined in the IndustryPack Specification. This information includes the IP's manufacturer, model code, and manufacturing revision level. It may also include a driver identification code and calibration information. Left over space in the ID PROM is available to add information from end users or systems integrators.

ID PROMs are typically used by software for auto configuration, auto calibration, and revision maintenance. Additional configuration management functions are possible. The ID PROM is not required to be accessed nor its information used by the host software. However, since the IP PROM may contain critical calibration or configuration information, software usage is highly encouraged.

Figure 4 below show the required information in each ID PROM. See the IndustryPack Specification and the Users Manual for each IP for more information.

$3F 2*nn+1	user space	
2*nn-1 $19	pack specific space	
$17	CRC	
$15	No of bytes used	[= nn]
$13	Driver ID, high byte	
$11	Driver ID, low byte	
$0F	reserved	($00)
$0D	Revision	
$0B	Model No	
$09	Manufacturer ID	
$07	ASCII "C"	($43)
$05	ASCII "A"	($41)
$03	ASCII "P"	($50)
$01	ASCII "I"	($49)

Figure 4 Required ID PROM Information

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Memory Addressing

IndustryPacks may contain memory as well as I/O. The IP Specification allows up to 4 Mbytes of memory on each IP.

If no memory IPs are used on the VIPC610, then memory accesses should be disabled by removing shunt E1 so the VIPC610 does not occupy any VMEbus memory space. This is the standard way the VIPC610 is shipped.

Memory addressing on the VIPC610 consists of three parts. The first is the setting of the base address. The second is the setting of the memory size. The third part is the memory offset from the base address for each of the four IP slots.

The base address is set with same shunts used to set the I/O base address, in the E7 and E3 configuration block. In a normal configuration, the memory and I/O base addresses "track" each other. The base address for memory is 256 times the base address of I/O. In hexadecimal this conversion is done by adding two zeros to the I/O address to generate the memory address. Thus if I/O is configured for $6000 in the A16 space, then memory begins at $600000 in the A24 space. In both cases the configuration shunts select the high address lines of the corresponding address space.

An installed shunt selects a given address line as zero. A removed shunt selects the address line as a one. Thus a base address of $000000 is created when all seven shunts are installed. A base address of $FE0000 is created when all seven shunts are removed. The correspondence between shunt location and address line is given below in Figure 5. Note that seven shunts are used to select the memory base address, whereas only six shunts are used to select the I/O base address.

Shunt Location	Corresponding Address Line
E7-7 to E3-7	A23
E7-6 to E3-6	A22
E7-5 to E3-5	A21
E7-4 to E3-4	A20
E7-3 to E3-3	A19
E7-2 to E3-2	A18
E7-1 to E3-1	A17

Note: Remove E1 shunt to disable all memory accesses to VIPC610.

Figure 5 Memory Base Address Shunt Assignment

The VIPC610 is normally shipped with the memory base address set to $600000, which is shown previously in Figure 2.

Caution: If memory address decoding is enabled by installing shunt E1, then the VIPC610 will attempt to respond to all memory accesses within its assigned memory address range. Even if no IndustryPacks are installed and no DTACK is generated, the VIPC610 data drivers will be enabled. This condition is cleared by the CPU's bus timeout circuit or by asserting reset.

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There are constraints which must be taken into account between the base address bit field, the memory capacity per IP and the IP slot containing the memory IP. The base address bit field is <A23:A19> for IP memory capacities </= 128 Kbytes and bits <A18:A17> are used as IP slot Selects.

The extent of the base address field decreases as IP memory capacities increase as illustrated in Figure 6.

	A23	A22	A21	A20	A19	A18	A17	A16
128 K	BA	BA	BA	BA	BA	IS	IS	D
256 K	BA	BA	BA	BA	IS	IS	D	D
512K	BA	BA	BA	IS	IS	D	D	D
1 MB	BA	BA	IS	IS	D	D	D	D
2 MB	BA	IS	IS	D	D	D	D	D

where: BA = Base Address
IS = IP Select
D = Displacement (high order)

Figure 6 Base Address Mapping for Memory IPs

As an example of the impact resulting from these constraints, consider the case of a 1 Mbyte IP in a VIPC610 configured for base address $600000. Because the IP Selects are mapped to <A21:A20>, but A21 must always be a "one" because of the base address configuration, the only valid IP Select decodes become "10" (slot C) and "11" (slot D). It therefore follows that in order to be able to select all four IP slots, the base address field must be restricted to <A23:A22>.

Size is set by installing or removing configuration shunts on pins in configuration groups. The location of the size configuration groups is shown in Figure 7 starting on the next page.

The configuration block E4-E5-E8 is used to set the total amount of memory that the VIPC610 will respond to on the VMEbus. Use either Figure 7 or 8 below to see this correspondence.

Memory size may be set from 128 Kbytes to 4 Mbytes per IP. Memory IPs may be installed in any of the four slots.

Decoding of memory addresses beyond the board level to each IP is done by memory select PLD U5. It uses the three "size" lines that are selected by configuration block E2. Based on this size information, the PLD selects one of six pairs of address lines to use for IP memory decoding.

This system permits the VIPC610 to decode the same amount of memory as installed in the IPs. The advantage to the systems integrator of this is that it permits contiguous addressing of system memory both above and below the VIPC610. Except for this convenience there is no reason not to have empty decoded memory IP slots. Figures 7 and 8 below may then be used, placing the memory IPs in which ever slot is most convenient.

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Memory Size for each IP	Shunts in group E2	Address Lines Used to Select IP
128 Kbytes	E2-3 to E2-4 E2-5 to E2-6	A17, A18
256 Kbytes	E2-1 to E2-2 E2-5 to E2-6	A18, A19
512 Kbytes	E2-5 to E2-6	A19, A20
1 Mbytes	E2-1 to E2-2 E2-3 to E2-4	A20, A21
2 Mbytes	E2-3 to E2-4	A21, A22

Figure 7 Decoding Details for Multiple Memory IPs

Memory Size On VIPC610	Shunts in group E2	Shunts in group E4-E5-E8
512 Kbytes 128 Kbytes in IP A @ Memory Base + $000000 128 Kbytes in IP B @ Memory Base + $020000 128 Kbytes in IP C @ Memory Base + $040000 128 Kbytes in IP D @ Memory Base + $060000 This configuration is shown in Figure 2 previously.	E2-3 to E2-4 E2-5 to E2-6 E1-1 to E1-2	E5-1 to E8-1 E5-2 to E8-2 E5-3 to E4-3 E5-4 to E4-4 E5-5 to E4-5 E5-6 to E4-6
1 Mbyte 256 Kbytes in IP A @ Memory Base + $000000 256 Kbytes in IP B @ Memory Base + $040000 256 Kbytes in IP C @ Memory Base + $080000 256 Kbytes in IP D @ Memory Base + $0C0000	E2-1 to E2-2 E2-5 to E2-6 E1-1 to E1-2	E5-1 to E8-1 E5-2 to E8-2 E5-3 to E8-3 E5-4 to E4-4 E5-5 to E4-5 E5-6 to E4-6

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2 Mbyte 512 Kbytes in IP A @ Memory Base + $000000 512 Kbytes in IP B @ Memory Base + $080000 512 Kbytes in IP C @ Memory Base + $100000 512 Kbytes in IP D @ Memory Base + $180000	E2-5 to E2-6 E1-1 to E1-2	E5-1 to E8-1 E5-2 to E8-2 E5-3 to E8-3 E5-4 to E8-4 E5-5 to E4-5 E5-6 to E4-6
4 Mbytes 1 Mbyte in IP A @ Memory Base + $000000 1 Mbyte in IP B @ Memory Base + $100000 1 Mbyte in IP C @ Memory Base + $200000 1 Mbyte in IP D @ Memory Base + $300000	E2-1 to E2-2 E2-3 to E2-4 E1-1 to E1-2	E5-1 to E8-1 E5-2 to E8-2 E5-3 to E8-3 E5-4 to E8-4 E5-5 to E8-5 E5-6 to E4-6
8 Mbytes 2 Mbyte in IP A @ Memory Base + $000000 2 Mbyte in IP B @ Memory Base + $200000 2 Mbyte in IP C @ Memory Base + $400000 2 Mbyte in IP D @ Memory Base + $600000	E2-3 to E2-4 E1-1 to E1-2	E5-1 to E8-1 E5-2 to E8-2 E5-3 to E8-3 E5-4 to E8-4 E5-5 to E8-5 E5-6 to E8-6
No memory	E1 shunt OUT Shunts in E2 are "don't care"	Shunts in E4-E4-E8 are "don't care"

Figure 8 Memory Size Configurations for Multiple Memory IPs

Other I/O and memory decoding options are available. See page 5 of the schematics in the VIPC610 Technical Documentation or contact GreenSpring Computers for more information.

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Interrupts

IndustryPacks are able to generate up to two interrupt requests each. Each interrupt request is serviced by an interrupt acknowledge cycle from the host CPU. During this cycle the requesting IP responds with an interrupt vector. The host CPU uses this vector to begin executing an interrupt service routine. This routine must access the requesting IP in such a way as to remove the interrupt request.

There are seven levels of interrupt requests on the VMEbus. IRQ7 is the highest, and is normally reserved for non-maskable requests. IRQ1 is the lowest level.

Configuration blocks are provided on the VIPC610 to route the eight possible interrupt requests from the IndustryPacks to the seven VMEbus levels. Similarly, matching configuration blocks are provided to route the seven interrupt acknowledge cycles to the requesting IP.

The simplest wiring scheme is to use a shunt to connect each pin of E10 straight across to the corresponding pin of E9. This is the factory default configuration. The correspondence of IP interrupt requests to VMEbus IRQ levels is then determined by reading across each line of the table in Figure 9. Many alternative mappings are possible by using wire-wrap™ wires instead of shunts. *Each encoding map provided by the E10-E9 configuration block must match a corresponding decoding map provided by the E11-E12 configuration block discussed below.*

Requesting IndustryPack	E10 Pin	E9 Pin	IRQ Level to VMEbus
IP A, IRQ 0	1	1	IRQ1
IP A, IRQ 1	2	2	IRQ2
IP B, IRQ 0	3	3	IRQ3
IP B, IRQ 1	4	4	IRQ4
IP C, IRQ 0	5	5	IRQ5
IP C, IRQ 1	6	6	IRQ6
IP D, IRQ 0	7	7	IRQ7
IP D, IRQ 1	8		

Figure 9 Interrupt Encoding Configuration Block

Note that the configuration block E10-E9 provides only for one-to-one mappings between IP requests and VMEbus IRQ levels. More complex mappings are possible by using a user-provide interrupt encoding PLD or equivalent device in socket U11. See page 6 of the schematics or contact the factory Application Engineering department for more information. When using an U11 mapping PLD, be sure that (1) the jumpers in E10-E9 are removed, and (2) that PLD U17 provides a complementary decoding map.

Figure 10 below shows the wiring of the interrupt decoding configuration block. This figure also shows the factory default programming of the interrupt decoding PLD U17. The simplest wiring scheme is to use a shunt to connect each pin of E11 straight across to the corresponding pin of E12. This is the factory default configuration. The correspondence of VMEbus interrupt acknowledge levels to IndustryPack Interrupt Selects is then determined by reading across each line of the table in the figure. Many alternative mappings are possible by using wire-wrap™ wires instead of shunts. *Each decoding map provided by the E11-E12 configuration block must match the corresponding encoding map provided by the E10-E9 configuration block discussed above.*

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VMEbus IACK cycle	E11 Pin	E12 Pin	IndustryPack Interrupt Select
IRQ7	1	1	IP D, Int Select 0
IRQ6	2	2	IP C, Int Select 1 IRQ5
3	3	IP C, Int Select 0	
IRQ4	4	4	IP B, Int Select 1 IRQ3
5	5	IP B, Int Select 0	
IRQ2	6	6	IP A, Int Select 1 IRQ1
7	7	IP A, Int Select 0	
		8	IP D, Int Select 1

Figure 10 Interrupt Decoding Configuration Block

Interrupt selection within an IndustryPack as accomplished with the A1 address line to each IP. A1 low corresponds to Interrupt Select 0; A1 high corresponds to Interrupt Select 1. During I/O and Memory cycles A1 to the IPs must match A1 from the VMEbus, of course. PLD U17 generates A1 to the four IP to implement these functions.

Option -01 may be ordered which provides an interrupt map equivalent to two VIPC310 boards. This map is useful to maintain software transparency between 3U and 6U VMEbus systems. This map is shown below in Figure 11.

Requesting IndustryPack	IRQ Level to VMEbus
IP A, IRQ 0	IRQ4
IP A, IRQ 1	IRQ5
IP B, IRQ 0	IRQ2
IP B, IRQ 1	IRQ1
IP C, IRQ 0	IRQ4
IP C, IRQ 1	IRQ5
IP D, IRQ 0	IRQ2
IP D, IRQ 1	IRQ1

Note: Packs A and B are higher priority than packs C and D.

Figure 11 Interrupt Encoding for Option -01

If users change the PLD in U17 to implement their own map, then the names given in Figures 10 and 11 above are not necessarily valid. These tables are best considered as a description of the default equations and jumpering on the VIPC610.

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Installation of IndustryPacks

IndustryPacks are installed on the VIPC610 carrier board by simply snapping them in. Press the IP and the carrier board together with your fingers until the two pairs of mating connectors are flush. The connectors are keyed, so the IP can only be installed correctly.

There are four locations for IPs. These are identified as A, B, C and D. The white lettering on the VIPC610 shows the location of each.

IPs A and C mate with straight 50-pin flat cable receptacle connectors for their I/O. IPs B and D mate with right angle 50-pin connectors. All connectors are accessible through the front panel on the VIPC610. The front panel labeling and LEDs also indicate which connector is associated with which IP. Pin 1 for each cable is identified on the front panel with a black dot. Route the cable for IPs B and D under the ears in the front panel provided for this purpose.

Many connector manufacturers are able to provide suitable receptacles. The following are recommended:

AMP 1-499506-2
Robinson Nugent IDS-C50NPK-SR-TG

Cables and Engineering Kits are available from SBS GreenSpring.

The right angle mounting in conjunction with the front panel ears provides an effective strain relief for the B and D cables. To add this strain relief function to the A and C cables, securely tie the A-B or C-D cables together at the front panel.

Occasionally it is desirable to be able to connect and disconnect a cable without removing the carrier board from the backplane. This is easily done with the A and C cables. To accomplish the same function with the B and D cables, place a dual 50-pin male-male header in the cable near the front panel, then disconnect at this header. It is still possible to use the built-in strain relief function by tying both cables to the portion of the cable before the added in-line header.

Caution: IndustryPack slot D is also connected to rows A and C of the VMEbus P2 connector. If the user's system has rows A and C of P2 committed to another use (such as VSB) then either slot D must be left empty, or a memory IP must be used in slot D. (Most memory IPs from GreenSpring Computers do not use any I/O lines.)

The pin assignment for slot D is shown in Figure 15 in the section User Options, below.

IndustryPack C may optionally also connect to pins on the P2 connector, although the factory default is no connection. Up to 14 signals from the IP in slot C may be assigned to P2. See the section User Options below for information on how to implement this option.

After an IP has been installed, four stainless steel screws may be used to secure the IP to the carrier board. This is normally necessary only in high vibration or shock environments. Insert the screw through the IP and the two connectors. Attach the nut on the solder side of the VIPC610. Tighten using small tools, taking care not to damage either the IP or the support board. The screws used are standard (metric) M2 x 18 stainless slotted flat head. These screws and nuts come with each IP.

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Caution: This revision of the VIPC610 has fuses added on the power inputs to all IP positions. This change in consistent with safety related requirements of some organizations. Current limitation imposed by these fuses are shown in Figure 13 below:

Supply	Applies To	Fusing
+5V	each IP individually	0.5 amps each
+12V	four IPs aggregate	0.5 amps total
–12V	four IPs aggregate	0.5 amps total

Figure 12 IP Current Limitations

The fuses are AVX 1206 surface mount. Blown fuses may be detected by the use of a standard DVM. Use the chart in Figure 14 below to associate a fuse with an IndustryPack position.

Fuse	Applies To	Fuse Value
F1	+5V IP A	0.5 amps
F2	+5V IP B	0.5 amps
F3	+5V IP C	0.5 amps
F4	+5V IP D	0.5 amps
F5	–12V IP A,B,C,D	0.5 amps
F6	+12V IP A,B,C,D	0.5 amps

Figure 13 Fuse Chart

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Front Panel Indicators

There are four green LED indicators on the front panel of the VIPC610. These are labeled IndustryPack Select A through D. Each time IP A is successfully accessed the A indicator will turn on for one third of a second. Similarly for the B, C and D indicators. Accesses more frequent than three times a second will show as a continuously illuminated indicator.

The LEDs respond to I/O, memory and interrupt accesses.

The trigger for the pulse stretcher that drives the LEDs is the acknowledge signal from the IPs. Thus if the host software attempts to access an IP, but selects an unused location to which the IP does not respond, or a location that is empty, the indicator LED on the front panel will not light. The indicators do not show that the VIPC610 is being selected, but rather that the associated IP has completed an access. Similarly, the indicator LEDs do not show interrupts pending, but do show interrupt acknowledge cycles.

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User Options

Most user options are explained elsewhere in this Manual. The chart below gives these options and lists the corresponding section of the manual. The text following the chart discusses some specialized options not explained elsewhere.

I/O Addressing Page 6
Memory Addressing Page 9
Interrupts Page 14

Alternative Power Supplies

The VMEbus Specification requires a backplane voltage of +12 volts (within +0.60V –0.36V) and –12 volts (within –0.60V +0.36V). The VIPC610 is designed to operate correctly at the alternative voltages of +15V and –15V. Most IndustryPacks from GreenSpring Computers are also designed to operate at these alternative voltages.

Caution: GreenSpring Computers cannot recommend running the VIPC610 at voltages outside those specified by the VMEbus Specification due to possible harm that may be caused to other components or subsystems connected to the user's system.

Strobes

Each IndustryPack has one pin on the logic interface labeled "Strobe." The Interface Specification does not define this pin, but suggests that it be used for alternative clocking signals in or out of an IP. A four position configuration block E6 is provided on the VIPC610 to permit user interconnection of the IP Strobe signals. Figure 15 below shows the assignment of pins on this configuration block. The location of the block is shown in Figure 19 near the end of this Manual.

E6 Pin	IndustryPack
Pin 1	IP Slot A
Pin 2	IP Slot B
Pin 3	IP Slot C
Pin 4	IP Slot D

Figure 14 Strobe Interconnection

Ground Planes under IndustryPack I/O Connectors

Four shunt positions are provided so that users or system integrators may connect a floating ground plane under the IndustryPack I/O connectors.

The VIPC610 has an internal power plane and ground plane used to distribute voltage to the components and IndustryPacks via the *pi* power line filters. These two planes serve to significantly reduce both conducted and emitted EMI. A third important function of these copper planes is to distribute the heat generated by components for more rapid dissipation into the surrounding air.

These power and ground planes stop just short of the four IP I/O connectors. A floating (unconnected) ground plane is provided inside the board, however. Digital ground planes normally carry some RF noise. By removing the plane from the vicinity of the I/O lines it is possible to have high precision, low

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noise analog signals on IndustryPacks. In some applications, however, it is desirable to have a close ground plane by all I/O lines to maintain a uniform impedance. For these applications users may re-connect the floating planes to the primary VIPC610 ground plane.

There is one common floating ground plane under the I/O connectors for IPs A and B, and a second common floating ground plane under the I/O connectors for IPs C and D. See Figure 16 below to re-connect these planes.

Ground Plane	Shunt Location
IP A and IP B	E16, E18 IN
IP C and IP D	E17, E19 IN

Figure 15 Ground Plane Shunts

I/O on P2 Connector

Normally all four IPs have their I/O cabling via the front panel. Four 50-pin flat ribbon cable connectors are provided for this purpose.

IndustryPack slots C and D may also have their I/O connected via the VMEbus P2 connector. This I/O may be used whether or not a VMEbus P2 backplane is installed. The VMEbus leaves rows A and C of the T2 connector open for this I/O use. Note however that some systems use these 64 lines for a secondary bus (such as VSB).

IndustryPack slot D is hard wired to the P2 connector. The pin assignment is shown below in Figure 17. If the users' system has rows A and C of P2 committed to another use, then either slot D must be left empty, or a memory IP must be used in slot D. (Most memory IPs from GreenSpring Computers do not use any I/O lines.)

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IndustryPack Slot D I/O Pin	VMEbus P2 Pin	VMEbus P2 Pin	IndustryPack Slot D I/O Pin
1	C1	A1	2
3	C2	A2	4
5	C3	A3	6
7	C4	A4	8
9	C5	A5	10
11	C6	A6	12
13	C7	A7	14
15	C8	A8	16
17	C9	A9	18
19	C10	A10	20
21	C11	A11	22
23	C12	A12	24
25	C13	A13	26
27	C14	A14	28
29	C15	A15	30
31	C16	A16	32
33	C17	A17	34
35	C18	A18	36
37	C19	A19	38
39	C20	A20	40
41	C21	A21	42
43	C22	A22	44
45	C23	A23	46
47	C24	A24	48
49	C25	A25	50

Figure 16 IP Slot D I/O to P2 Wiring

Up to 14 signals from IndustryPack slot C may also be assigned to P2 connections. The configuration block E13-E14-E15 is available to implement this interconnection. In most cases wire-wrap™ will be the most convenient implementation method.

E13 has 50 pins, which are connected to the 50 pins of the Slot C I/O connector numbered identically (pin 1 to pin 1 through pin 50 to pin 50). Figure 18 below shows the Pin Assignments for E14 and E15. Note that for all configuration blocks on VIPC610 that pin 1 has a square pad, observable from the solder side of the board.

E14 Pin	VMEbus P2 Pin	VMEbus P2 Pin	E15 Pin
1	C26	A26	1
2	C27	A27	2
3	C28	A28	3
4	C29	A29	4
5	C30	A30	5
6	C31	A31	6
7	C32	A32	7

Note: E13 pins are numbered to match Slot C I/O connector pins.

Figure 17 IP Slot C I/O to P2 Wiring

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User I/O Wiring

Each of the 50 pins on each I/O connector for the four IndustryPack slots—A, B, C and D—connects to a like-numbered pin on the four corresponding flat cable connectors on the VIPC610 front panel. The IndustryPack I/O connector, the VIPC610 flat cable connectors, and the wires on the ribbon cables are all numbered identically from 1 to 50.

Pin 1 on IP and VIPC610 connectors is marked with a square pad, observable from the solder side of the respective board. Pin 1 is shown on the VIPC610 front panel with a black dot. Pin 1 is typically marked on ribbon cable with a red stripe and on ribbon cable connectors with a manufacturer's mark, often a molded textured triangle.

Caution: This consistent pin numbering system is not maintained with many mass-terminated connectors, however. Each type of connector has its own intrinsic pin numbering system. Systems integrators or users making their own cables must be certain which pin corresponds to which signal.

The pin assignment of the IP I/O connector is fixed by the connector manufacturer and repeated in the IndustryPack Specification. This assignment is shown in Figure 19 below.

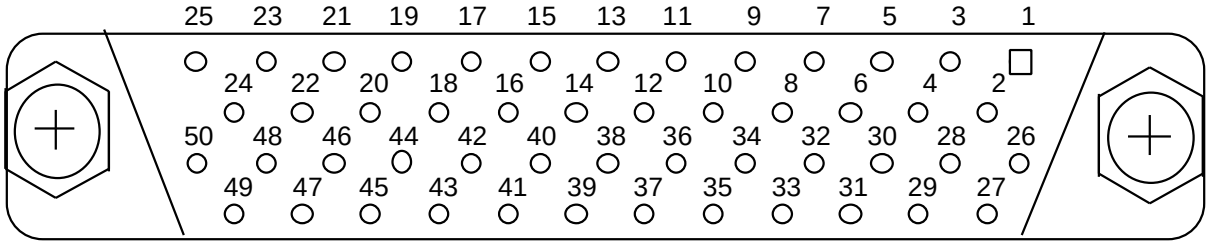


Figure 18 IndustryPack Connector Pin Numbering from solder side

The VIPC610 carrier board connects the mating I/O connector pins to a 50-pin flat cable connector accessible through the front panel. All pins from the IndustryPack go to the like numbered pins on the front panel connector. The pin numbering assignment of the four 50-pin front panel connectors is shown below in Figure 20. The wires in ribbon cables themselves are numbered sequentially across the flat cable starting with a red stripe on pin 1.

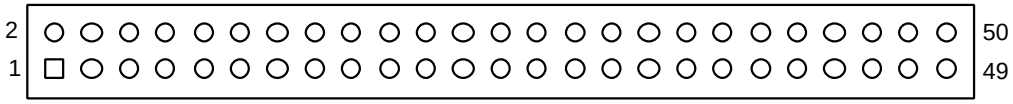


Figure 19 Flat Cable Connector Pin Numbering from Component Side

GreenSpring Computers offers cables, Engineering Kits, and terminal blocks.

Interfacing to the outside world—the I/O cabling—remains the responsibility of the systems integrator or end-user/engineer.

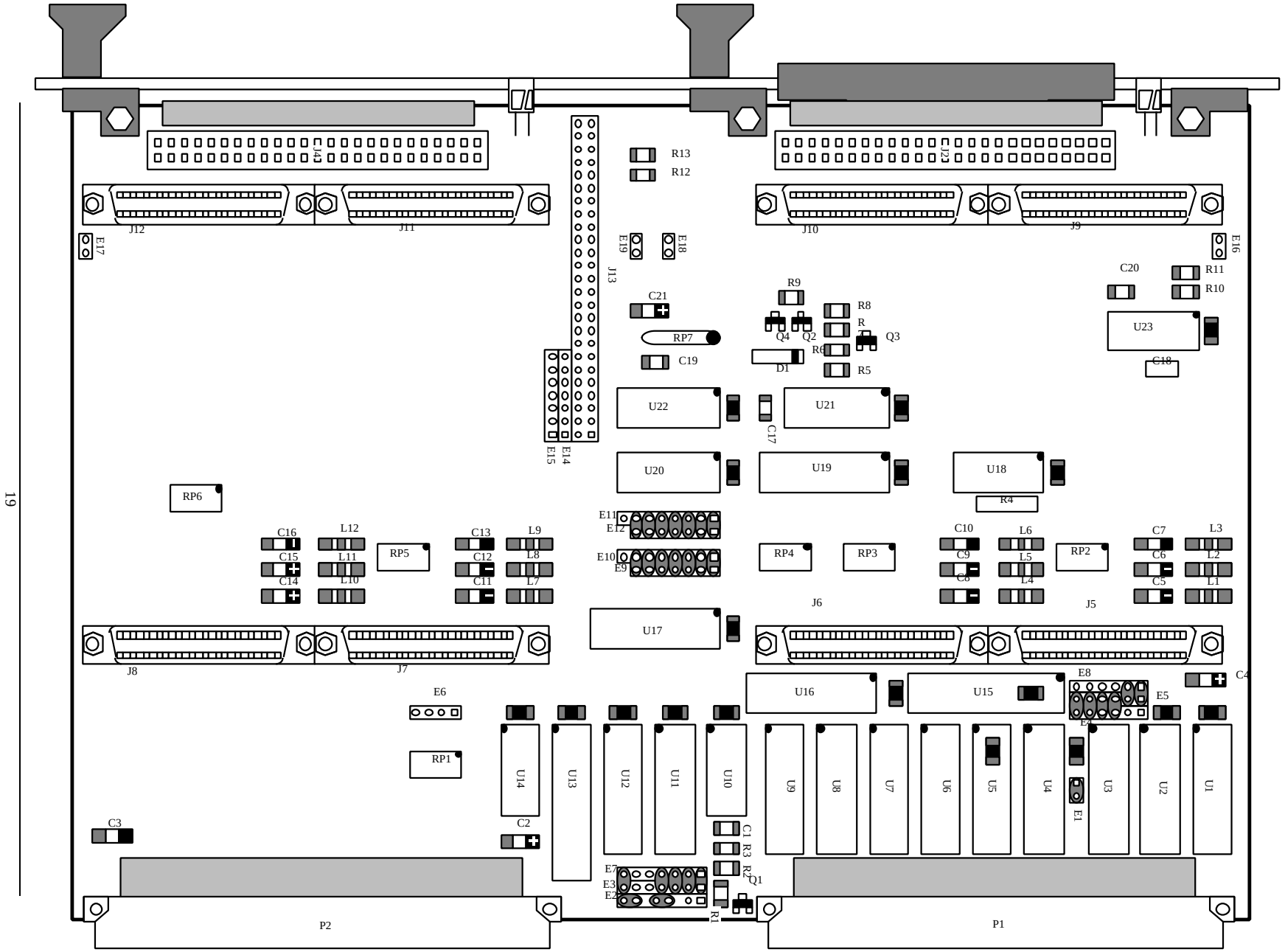
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Specifications

VMEbus Conformance	Revision C.1
VMEbus Form Factor	6U (double high)
Number of IndustryPacks	4 single-high, or 2 double-high
IP Memory Mapping	A24/D16
Memory Size	None, or 128 Kbytes to 4 Mbytes in 6 increments
IP I/O Mapping	A16/D16
I/O Size	1024 bytes usable out of 2048
VMEbus Interrupts	IRQ1 through IRQ7, jumper or PLD selectable
I/O Interconnect	Four 50-pin 0.100 inch flat cable connectors Two IP's I/O available on P2
Front Panel Indicators	Four green LED's
Power Requirements	+ 5 V @ 590 mA typical +12 V @ 0 mA – 12 V @ 0 mA Additional power is consumed by IndustryPacks
Power Restrictions on IPs	+ 5 V @ 0.5 amp each IP +12 V @ 0.5 amp total all IPs –12 V @ 0.5 amp total all IPs
Environmental	0^{o} C to 70^{o} C operating 5 to 95% relative humidity (non condensing) –10 to + 85^{o} C storage
Size	189 mm deep (incl. front panel) 262 mm high (incl. front panel) 19.8 mm thick (incl. front panel)
Weight	0.34 Kg

Figure 20 Location of Configuration Blocks on VIPC610 shown on next page

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Warranty and Repair

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Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS GreenSpring will not be responsible for damages due to improper packaging of returned items. For service on SBS GreenSpring products not purchased directly from SBSGreenSpring, contact your reseller. Products returned to SBS GreenSpring for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
SBS GreenSpring Modular I/O
181 Constitution Drive
Menlo Park, CA 94025
(415) 327-1200
FAX: (415) 327-3808
email: support@greenspring.com
http://www.sbs-greenspring.com

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