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VG5

Dual PowerPC™ 6U VME
Single Board Computer

Hardware User's Manual

Revision 1.1

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Revision	By	Date	Chapter	Comments
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			Table 33	A_SYS_OUT Register: A_LED/BOOTSEL (Bit2) updated additional bits (16,17)for Single Node Version:
			3.6.2.10	FPGA in Single Node Version: Remark added to A_SYS_OUT register
			Table 34	B_SYS_OUT Register: B_LED/BOOTSEL updated
			Table 25	A_CNTRLSTAT: Version Structure updated + Remark
			Table 26	A_CNTRLSTAT: Version Structure updated + Remark
			Table 30	Watchdog A ControlBits: A_WDG1A/B_EXP updated
			Table 31	Watchdog B ControlBits: B_WDG1B/A_EXP updated
			3.6.2.7	Watchdog Timer A/B: text updated (A/B_WDG1B/A_EXP)
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1.1	TD	16.03.2004	4.2.5, Table 49	removed product configuration codes in table, now only discription; added line in table regarding Ethernet LED function on VTM20
			Table 53	removed product configuration codes in table, now only discription; added warning

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Unpacking and Handling Instructions

1. Please read this manual carefully before unpacking the module or fitting it into your system. This will certainly save time and avoid trouble.
2. Please observe the precautions for electrostatic sensitive modules.
3. If the product contains batteries, please do not place the board on conductive surfaces or anti-static plastic or sponge, which can cause shorts and lead to battery or board trace damage.
4. Please do not exceed the specified operational temperatures. Please note that batteries might have temperature restrictions.
5. Keep all original packaging material for future storage or warranty shipments of the board.

Caution



Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type recommended by SBS Technologies. Dispose of used batteries according to the instructions of SBS Technologies.



Vorsicht!
Explosionsgefahr bei unsachgemäßem Austausch der Batterie.
Ersatz nur durch denselben oder einen von SBS Technologies empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

Warning

This is a Class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

Notes

Drain static electricity before you install or remove any parts. Installing or removing modules without observing this precaution could result in damage to this and/or other modules in your system.

Installation

Use the following steps to install your SBS Technologies hardware.

General Advisories

1. Before installing or removing any board, please ensure that the system power and external supplies have been turned off.
2. Check that the jumpers and piggybacks are correctly configured for your application.
3. Mount the board/piggyback/transition module very carefully. See also additional advisories for VMEbus and CompactPCI products below.
4. Connect all IO cables.
5. Once you are certain that all modules are correctly fitted into the system and all connections have been made properly, restore the power.

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Advisories for VMEbus products

On a standard VMEbus backplane, remove the jumpers on the IACKIN - IACKOUT interrupt daisy chain (1 jumper) and on the BGxIN - BGxOUT busgrant daisy chains (4 jumpers) for the slot where the board is to be mounted. The daisy chain jumpers on the VMEbus backplane should be mounted on all free slots.

Setting jumpers is not necessary for the SBS Technologies Auto-Daisy-Chain VMEbus backplane (order number: VBUSxxAD). Please read additional advisories within the manual.

A board with system controller functionality must be fitted at slot 1 (for SBS Technologies products, see additional notes within the manual).

Advisories for Compact PCI products

Mount the CPU board carefully on the first CPCI bus slot (called system slot). Note that on some boards connectors are used for IO purposes which must not be inserted into a CPCI bus backplane. A transition module must be used instead.

Disclaimer

The information in this document has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies.
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SBS Technologies do not accept any liability concerning the use of their products in life support systems.

Warranty

SBS Technologies grants the original purchaser of SBS Technologies products a warranty of 12 month from the date of delivery. For details refer to the "Allgemeine Geschäftsbedingungen".

In the event of repair, please return the product together with additional written information about

the kind of defect
is the defect restricted to certain environmental conditions
what was the hardware environment when the defect appeared
were there input signals; if yes which
warranty/no warranty repair

Please use the error report form sheet at the end of this manual and use the original packing material to avoid damage. Otherwise warranty may be lost.

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Glossary

TBD	to be defined
TBC	to be confirmed
SBC	Single Board Computer
Node A	Unit on VG5 consisting of Chipset A, CPU A, L3 Cache A, DDR RAM A, FLASH A.
Node B	Unit on VG5 consisting of Chipset B, CPU B, L3 Cache B, DDR RAM B, FLASH B.
Devicebus	A 32bit bus from the Chipset (MV64360) used for connecting Flash Memory, UART, RTC and FPGA . Each node has an independent Devicebus.
FPGA	Field Programmable Gate Array
MPSC	Multi Protocol Serial Controller (Unit of MV64360)
MPP	Multi Purpose Port (Unit of MV64360)
NDA	Non Disclosure Agreement

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1 General Information

This manual applies to the VG5 single board computer version 0.x, until superseded.



The product is still under development.
Please do not rely on this revision.
The content is subject to change without notice.

1.1 Features

- Microprocessor
  Single or dual Motorola® PowerPC™
  Motorola® PowerPC™ MPC7455 processor 800MHz-1000MHz
  Motorola® PowerPC™ MPC7457 processor 800MHz-1300MHz
- Cache RAM
  on chip 32KBytes instruction + 32KBytes data first level cache
  On chip 256kByte or 512kByte second level cache
  external 2MByte third level cache for each processor node
- System Controller
  Discovery II Marvell® MV64360 system controller for each processor node for independent operation
  Up to 133MHz CPU bus frequency
  DDR SDRAM Controller supports up to 1GBit devices
  Two 64-bit PCI-X buses
  Separate device bus interface
  Two integrated Gigabit Ethernet MAC controller
  Two Multi Protocol Serial Controller (MPSC)
- DRAM
  One bank for each system controller,
  256MByte, 512MByte or 1Gbyte DDR SDRAM per bank,
  memory interface with 133MHz,
  memory banks are ECC controlled and on-board soldered.
- Single/Dual Node
  In Dual Node configuration each node has CPU, System Controller, DDR SDRAM bank, PMC site, Flash Bank and system devices.
  Interconnection of the two Nodes with 64bit PCI-X bus and via FPGA dual port SRAM
  Single Node configuration has one CPU, System Controller,
  DDR SDRAM bank, PMC site, and Flash Bank, second PMC site is connected via a jumper bridge
- FPGA
  Field Programmable Gate Array for internal logic, provides additional 1kByte Dual Port SRAM for message interchange and also 32 user programmable IO signals
  50% of the FPGA is free for user defined features
- Flash
  Each Node has 128MByte Flash which includes Boot Program
- NVRAM
  NVRAM build with a 512kbit Serial EEPROM for NodeA and the same for NodeB

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• Ethernet	Each Node has one Gigabit Ethernet and one Fast Ethernet channel coming directly from the MV64360 System Controller. These Ethernet channels are either front or rear (NodeA) available or only rear (NodeB).
• PMC slots	Two 64-bit PCI mezzanine connectors for standard PMC as well as for rugged PMC. IO signals available at the rear connectors. PMC1 is usable with PCI 33/66MHz or PCI-X 100MHz. PMC2 is limited to 33MHz. In Dual Node configuration PMC1 is bound to Node A and PMC2 is bound to Node B.
• Real Time Clock	MC146818 compatible RTC only with external battery voltage supply and 114 byte non-volatile SRAM
• Serial IO	Up to six serial interfaces, three for each node. For each node one async. 16550 compatible full duplex RS-232 channel transfer rate up to 115.2kbaud For each node two Multi Protocol Interface RS-422/485 channels for transfer rates up to 12Mbps. One of the NodeA serial channels is software selectable RS-232 or RS-422/485 (120kpbs/250kbps) Serial interfaces are available at rear or front (three of them)
• General Purpose IO	32 bit general purpose IOs individually programmable for input, output or edge triggered interrupt. IO signals are available at rear IO (shared with PMC IO)
• Timer/Counter	8 timers each 32bit wide for system timing and periodic interrupt
• VME bus	PCI bus to VMEbus bridge (Tundra Universe IID) , up to 60 MByte/s transfer rates Big endian / Little endian conversion control FIFOs for write posting, DMA controller with linked list support Master and Slave transfer modes: BLT, ADOH, RMW, LOCK, RETRY A32 / A24 / A16 and D64 (MBLT) / D32 / D16 / D8 Full VMEbus system controller
• Serial ATA	PCI to SATA Bridge (SIL3112): One channel SATA interface available at rear (shared with PMC IO).
• Temperature Sensors	Three sensors (LM75) show temperature of system board near both CPUs and in the board centre, software readable in 0.5°C increments from -55 to +125 °C
• Watchdog	Watchdog for each CPU activates reset under software control
• COP Interfaces	Processor debug interface for external emulator for each node. Available at rear or on-board
• JTAG Interface	JTAG interface for all devices with JTAG interface. Optional available at rear (shared with PMC IO and COP interface)
• LED Indicators	CPU Fail LEDs for each node and one User LED

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- Front Panel — Two PMCs, one DSUB9 Serial Connector, RJ45 Fast Ethernet Jack, LEDs and Reset Button
  Optional RJ45 Gigabit Ethernet Jack, and DSUB9 Serial Interface
- Backpanel IO — COM1-6, GPIO, Serial ATA (option), reset, watchdog, PMC IO, Ethernet, Boot Select, JTAG (option), COP
  Transition module VTM20 available for compatible connectors
- Power — Dual Power Supply +5V and +3,3V.
- Conduction Cooling — Conduction Cooling available
- Conformal Coating — The board is optionally conformal coated to protect against humidity and fungus

1.2 Specification

- **PCB** — FR4 Multilayer
- **Size** — Total size: 1 board : 6U, 4 TE
- **Dimensions** — PCB: 233.35 mm x 160 mm x 20 mm
- **Weight:** — VG5 single node C/I Style 440g (with frontpanel, heatsink)
  VG5 dual node C/I Style tbd g (with frontpanel, heatsink)
  VG5 N Style single node 650g
  VG5 N Style dual node tbd g
- **Power Requirements** — +5V min 4.87V max 5.25V,
  +3.3V min 3.25V max 3.45V
  Max Power at VMEbus connectors: 1.25A/pin @ 60°C ambient:
  +3.3V with 10 pins at VME backplane can supply nominal 41W
  +5V with 9 pins at VME backplane can supply nominal 56W
- **Power Consumption**

The table below helps customers calculate the power consumption of a VG5 system. For measurement, the VG5 is mounted on a VME backplane, without any other IO interfaces. During measurement, the power consumption of the backplane is ignored. The power is measured during VxWorks prompt no application software is running.

Order No.	Typical current @ +5V	Typical current @ +3.3V	Total Power Consumption	Remarks
VG5 SJ7xxxxxxx	3.3A	2.4A	24.5W	Single CPU 7455 133MHz/1000MHz, 256MB
VG5 SI7xxxxxxx	2.8A	2.2A	21.3W	Single CPU 7455 133MHz/800MHz, 256MB

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Table 1: Power Consumption

- **External Battery Voltage for RTC** input range 4.87V – 5,25 V, max. current @5.0V 3µA

Environment	C-Style	I-Style	R-Style	N-Style
High Temperature [°C]				
Operating [1]:	+70°C	+70°C	+70°C	+70°C (card edge)
Storage:	+85°C	+85°C	+85°C	+85°C
☞ Note 1: Please refer to section **Thermal Behaviour** for more information.				
Low Temperature				
Operating	+0°C	-40°C	-40°C	-40°C
Storage	-40°C	-40°C	-40°C	-40°C
Rel. Humidity				
Operating		up to 95% @ 40°C, non-condensing		
Storage		up to 95% @ 40°C, non-condensing		
Altitude				
Operating	4.5 km	4.5 km	4.5 km	vacuum
Storage	12 km	12 km	12 km	vacuum
☞ Note: 4.5 km (15,000 ft.), 12 km (40,000 ft.)				
Shock				
Amplitude	12g	12g	20g	100g / 40g
Duration	6 ms	6 ms	6 ms	6 ms / 11 ms
☞ Note: half sine (peak), 3 axis up & down, 5 hits / direction				
Vibration (operating)				
Spectrum	5 to 100 Hz	5 to 100 Hz	5 to 2000 Hz	5 to 2000 Hz
Acceleration	$2g_{rms}$	$2g_{rms}$	$2g_{rms}$	$14g_{rms}$
☞ Note: random, 30 min , 3 axis				

Table 2: Environment

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1.3 Thermal Behaviour

This section describes in short the thermal behaviour of the VG5 boards. For more detailed information, please check the thermal report document of the VG5 (Doc Ref TR-HW-006).

1.3.1 Thermal Condition C/I/R-Style

The thermal condition of the C-Style VG5 is for use in an air stream cooled environment. This means the maximum ambient temperature can only achieved with sufficient airflow. The diagram below gives the maximal ambient temperature of the CPU (hottest spot) related to the forced airflow under worst case power condition.

> ☞ **Note:** Please note that the airflow must be valid for the complete board surface (front and backside) to achieve the ambient temperature and a mounted PMC Module changes the thermal behaviour of the VG5 board.

It is not recommended to operate the VG5 system without sufficient airflow. As the thermal situation depends on the actual power consumption and a defined airflow, which may be difficult to determine, there are some hints to determine the maximum operating temperature.

The hottest spots at the VG5 board are the CPU and devices under the heatsink. Under worst case power consumption the heatsink surface shall not exceed the specified value, which can be found in the table below.

Table tbd

To determine the maximum possible ambient temperature (T_{amax}) the user shall take the maximum heatsink temperature from Table above and measure the current ambient temperature (T_{ameas}) and the heatsink surface temperature ($T_{heatsinkmeas}$) under typical application and actual airflow in the system rack.

The maximum ambient temperature is then calculated with following formula.

$$\mathbf{T_{amax} < T_{heatsinkmax} - T_{heatsinkmeas} + T_{ameas}}$$

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1.3.2 Thermal Condition N-Style

The thermal condition of the N-Style VG5 is for use in conduction cooling environment. This means the base is not related to the ambient temperature but to the maximum card edge temperature.
The table below gives the maximal junction temperature at 85°C card edge temperature and worst case power condition.

☞ **Note:** Please note that a mounted PMC Module will change the thermal behaviour of the VG5 board.

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2 Hardware Installation

The VG5 is a single slot VME controller equipped with either dual PowerPC 7455/57 or single PowerPC 7455/57. It is equipped with all functions a conventional system controller can only offer with several add-on cards. Extension boards can be connected via the VME interface and 2 PMC interfaces. The minimised board size and the large number of interfaces and functions enable the VG5 for use in many applications.

2.1 Block Diagram Dual Node

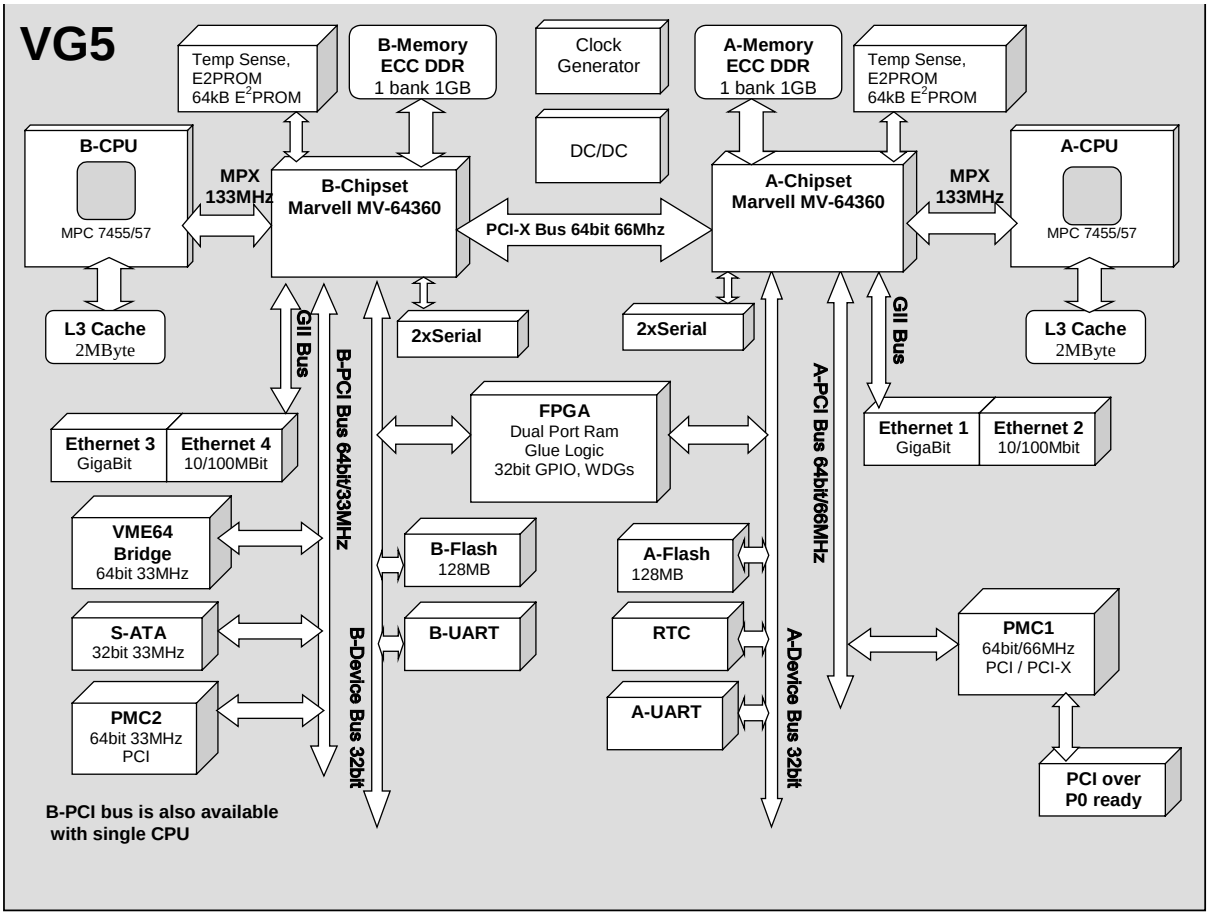


Figure 1: VG5 Blockdiagram (Dual Node)

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2.2 Block Diagram Single Node

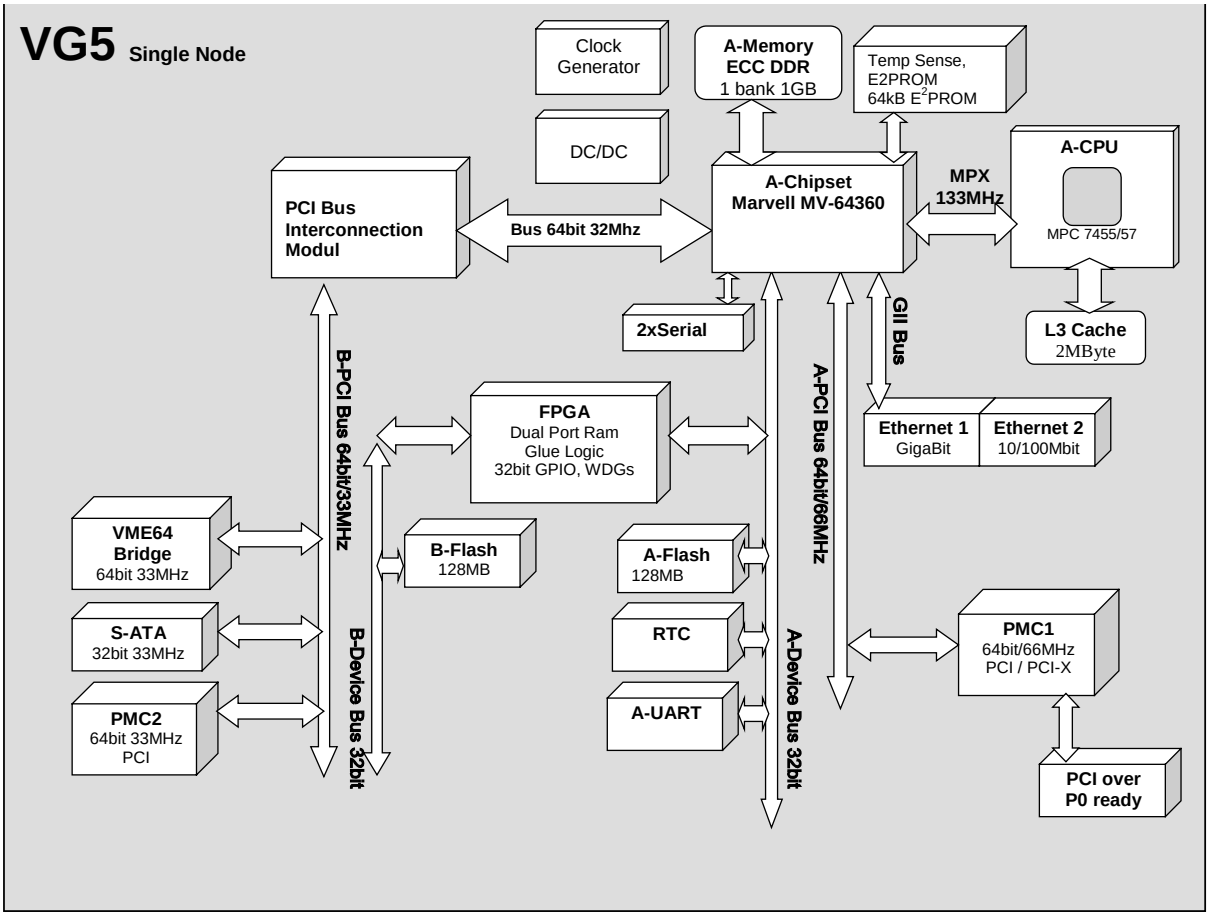


Figure 2: VG5 Blockdiagram (Single Node)

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2.3 Placement Plan Component Side

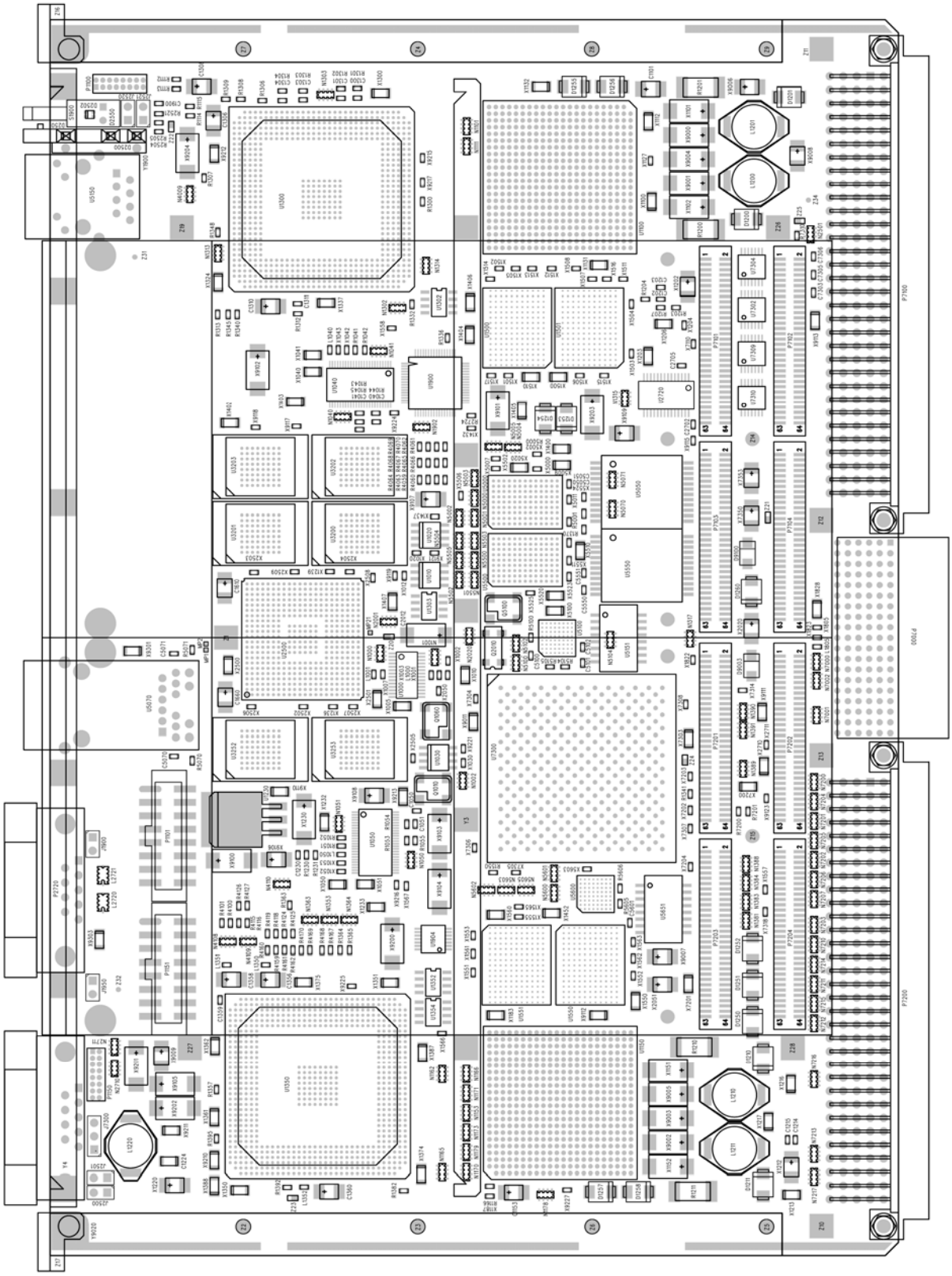


Figure 3: Board V0.x Placement Top Side

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2.4 Placement Plan Solder Side

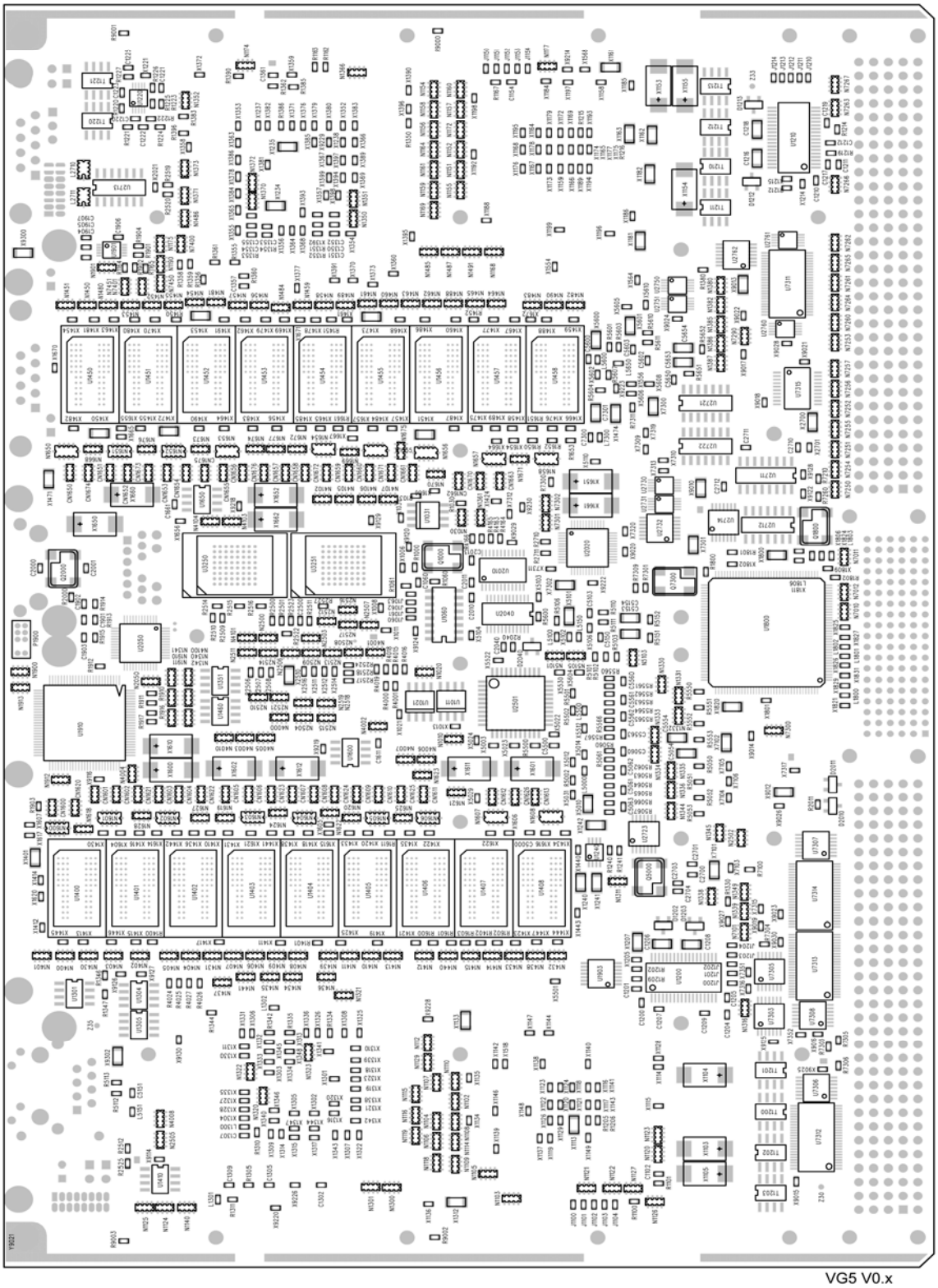


Figure 4: Board V0.x Placement Bottom Side

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2.5 Front Panel

VG5 with two front Ethernet, two front COM ports and one PMC site:

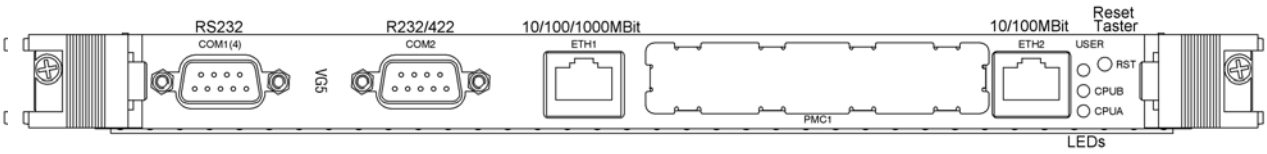


Figure 5: Front Panel with one PMC site

VG5 with one front Ethernet, on front RS232 COM port and two PMC sites:

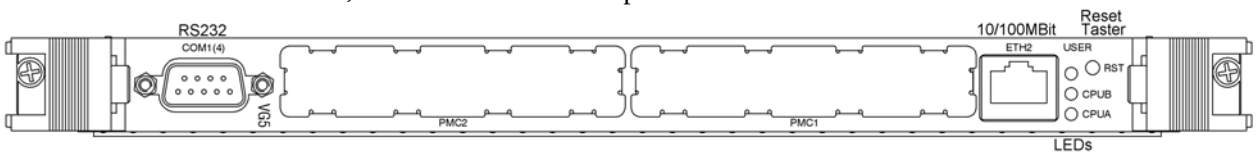


Figure 6: Front Panel with two PMC sites

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2.6 Socket Installation

There are several accessible jumpers on the VG5.

2.6.1 VME Reset Jumper

The jumper J7301 defines the strategy for VME bus resets.

J7300 1-2	J7300 2-3	J7300 open
The VG5 detects automatically if the board is system controller or not. The VMEbus reset is generated only if the VG5 is system controller.	VMEbus reset generated (factory default setting)	VMEbus reset is never generated

Table 3: VME Reset Jumper J7300

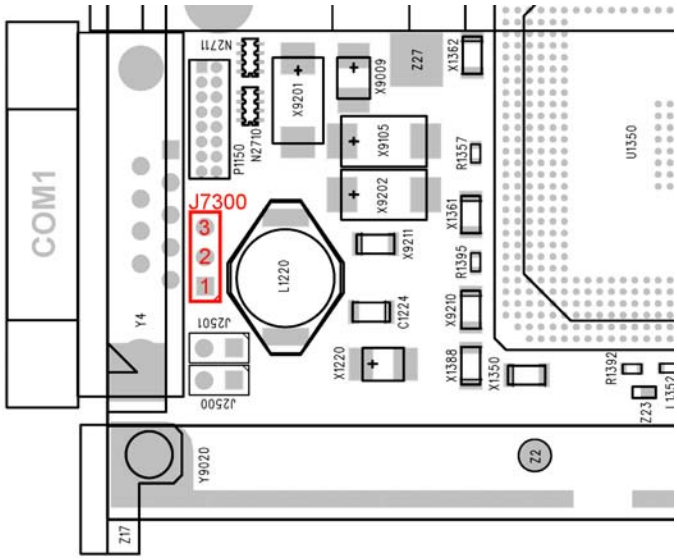


Figure 7: Location of VME-Reset Jumper J7300

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2.6.2 Bootselect Jumper

The jumpers J2520 and J2521 select the booting source of Node A and B. Not mounted in conduction cooled version (N-style). Both Bootselect jumpers are available at rear IO too.
The boot behaviour depends on the software installed in the boot flash. The boot software is responsible for the evaluation of the BOOTSEL jumper.
Due to limited pins at P0/P2 the boot select signals share the function with the card fail LEDs of CPU A and CPU B. If a jumper is closed the program will read and store the status of the boot select function, after this read function the signal will be an output and controls the card fail LEDs.
That means if a jumper is closed the LED is in on-state as long the jumper is installed. The LED output is protected against this short cut.

J2520 open	**J2520 closed**
Booting from user boot source for CPU A	Booting from emergency boot source for CPU B.
J2521 open	**J2521 closed**
Booting from user boot source for CPU B	Booting from emergency boot source for CPU B.

Table 4: Bootselect Jumper J2520, J2521

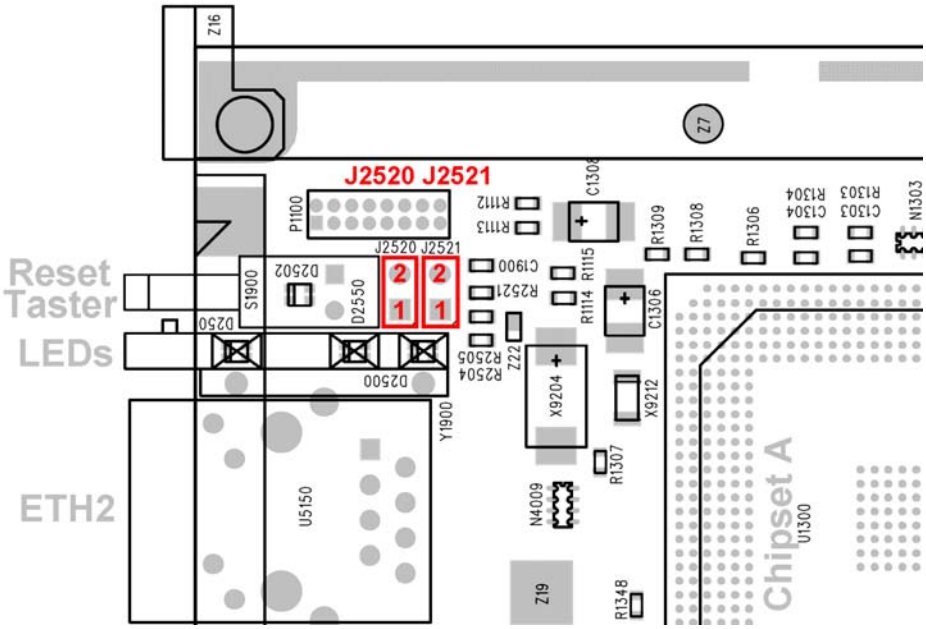


Figure 8: Location of Bootselect Jumpers J2520, J2521

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2.6.3 Watchdog Jumper

Jumpers J2500 and J2501 define the Watchdog functions.
Not mounted in conduction cooled version (N-style).

J2500 open	**J2500 closed**
Watchdog-Reset for Node A is enabled after hard reset.(factory default setting)	Watchdog-Reset for Node A is disabled after hard reset and even if activated by software
J2501 open	**J2501 closed**
Watchdog-Reset for Node B is enabled after hard reset. (factory default setting)	Watchdog-Reset for Node B is disabled after hard reset and even if activated by software

Table 5: Watchdog Jumpers J2500, J2501

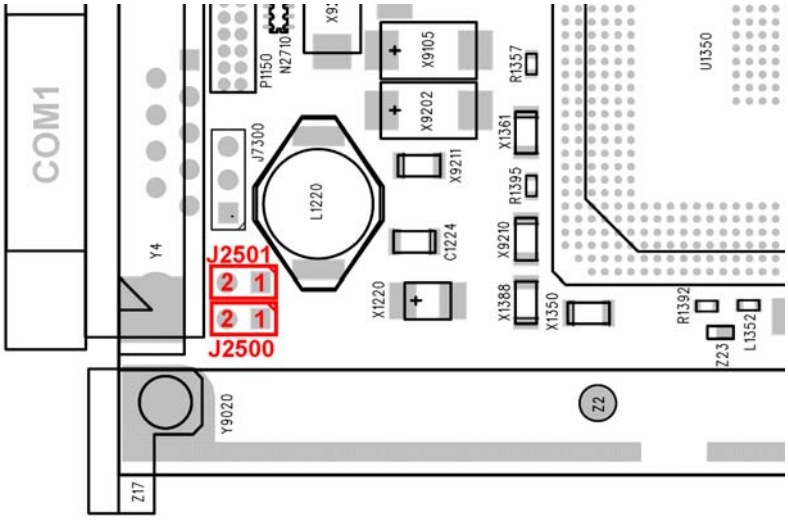


Figure 9: Location of Watchdog Jumpers J2500, J2501

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2.6.4 Flash Write Protect Jumpers (Resistors)

The following jumpers are not generally available and only for emergency usage. The jumpers are mounted with high value resistor and can be shortcut by a suitable tool, e.g. with a small clip. If one of these resistors are shortcut it outvotes the write protection of blocks of the boot flash.

R2506 disables the write protection of boot block of Node A (upper 1MByte, see chapter 3.6.2.4)
(see also chapter: 3.6.2.5: A_FB1_BootWP bit in A_CNTRLSTAT Register)

R2507 disables the write protection of system block of Node A (upper 8MByte, see chapter 3.6.2.4)
(see also chapter: 3.6.2.5: A_FB1_SysWP bit in A_CNTRLSTAT Register)

R2508 disables the write protection of boot block of Node B (upper 1MByte, see chapter 3.6.2.4)
(see also chapter: 3.6.2.5: B_FB1_BootWP bit in B_CNTRLSTAT Register)

R2509 disables the write protection of system block of Node B (upper 8MByte, see chapter 3.6.2.4)
(see also chapter: 3.6.2.5: B_FB1_SysWP bit in B_CNTRLSTAT Register)

Bottom side of VG5 board, near centre:

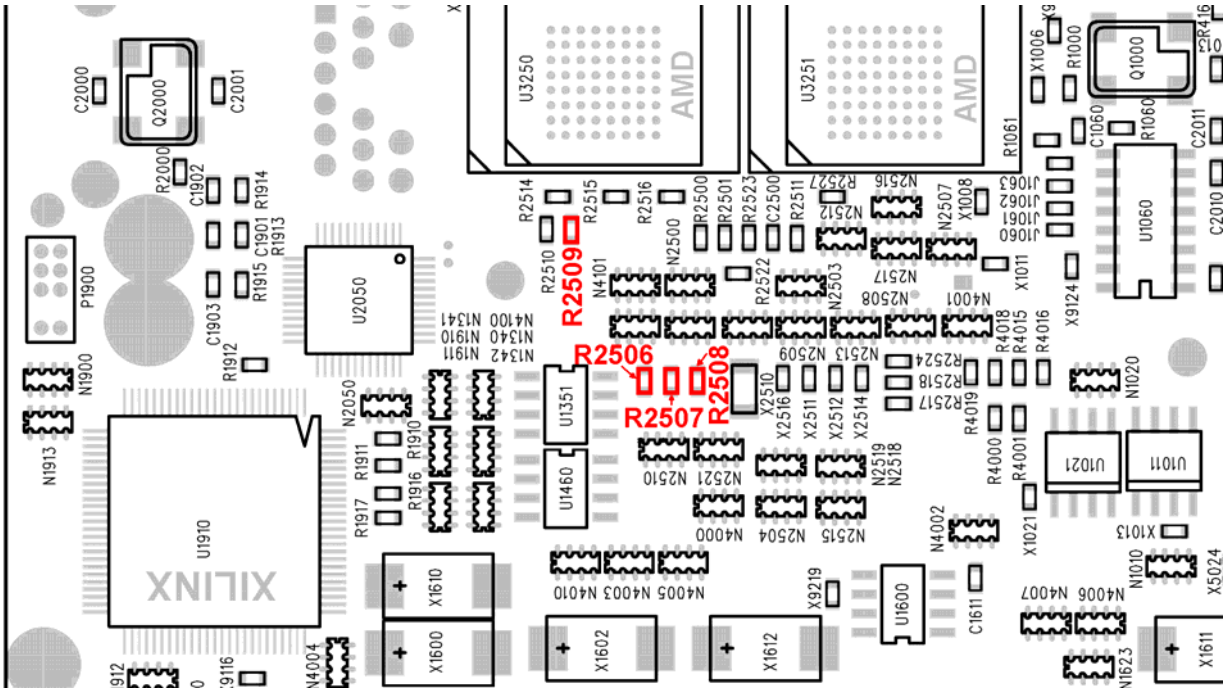


Figure 10: Location of Write Protect Jumpers (Resistors)

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2.7 Clocking

The clock scheme of the VG5 is very flexible and the blocks are independent. Main clock is a 133MHz clock for CPU, CPU bus, and device bus with FPGA and memory. The CPU core clock is a multiple of the main clock.

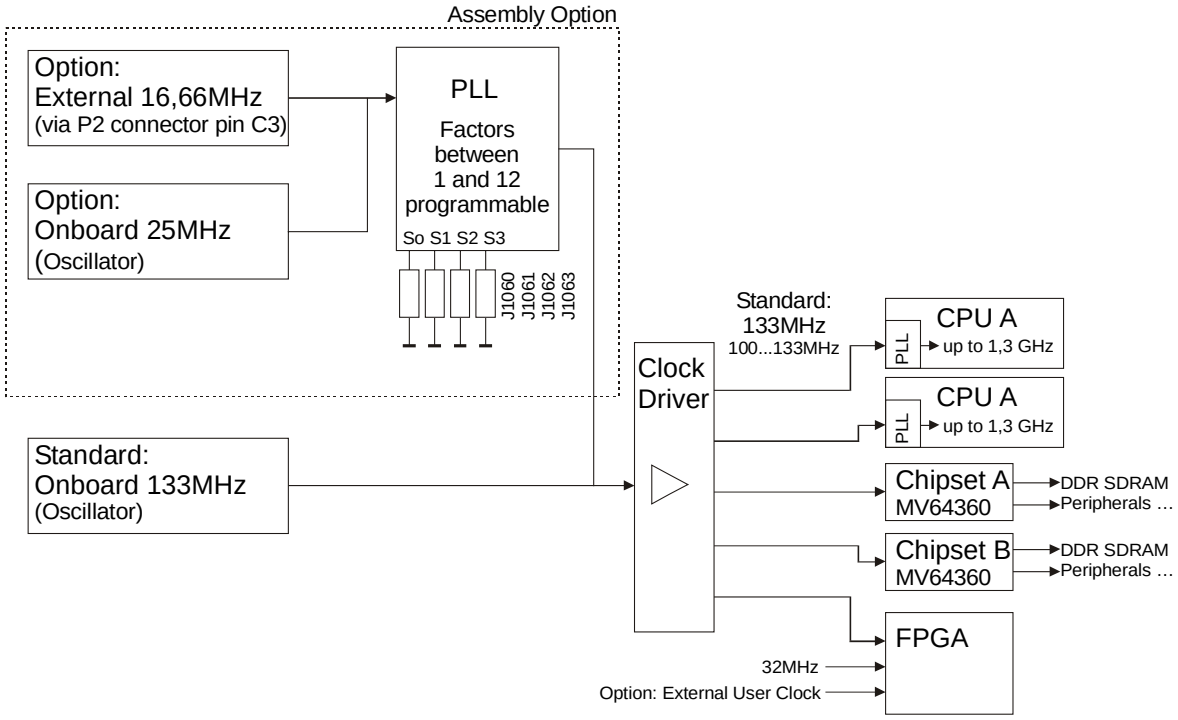


Figure 11: Main Clock Tree

Each PCI bus has its own clock which is completely independent from the other PCI bus. The frequencies of the PCI busses are self-selectable (depending from the used configuration and PMC card) in steps between 33..133Mhz.

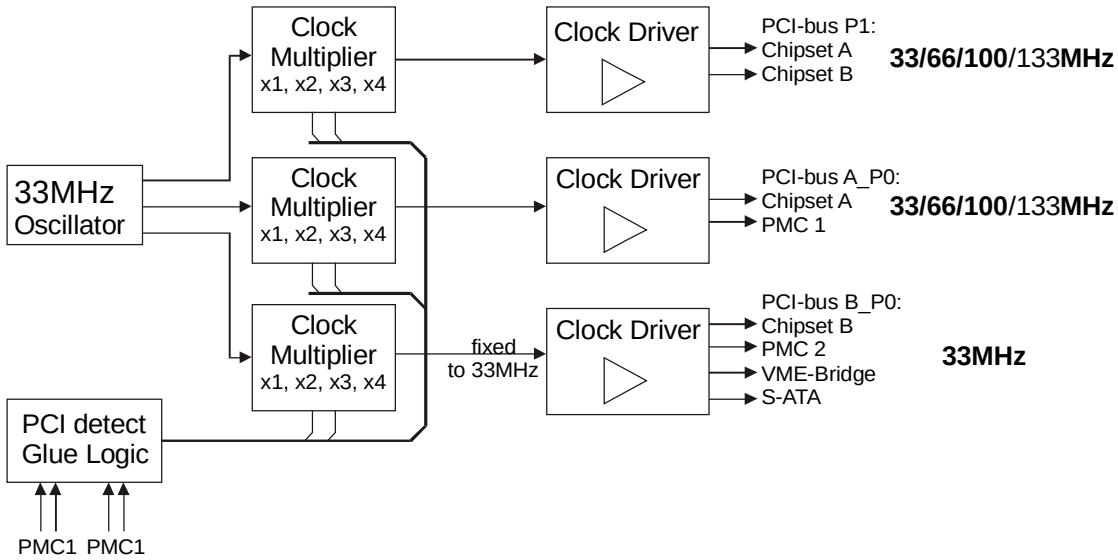


Figure 12: PCI Bus Clocks

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2.8 Interfaces and Connectors on the VG5

The connectors P0, P1 and P2 carry the signals for the VMEbus as well as all the IO signals of the VG5. For easy connection of the IO signals to standard connectors a transition module is available from SBS Technologies. The order number for the transition module is “VTM20”.

2.8.1 Pin Description for the Following Tables:

Signal groups:

PMC IO signals of Slot 1:	PMC1_IO…
PMC IO signals of Slot 2:	PMC2_IO…
COM1, COM2, ... signals:	C1....., C2.....,
User General Purpose IO	UGpio_...
Node A Gigabit Ethernet signals:	Eth1_…
Node A Fast Ethernet signals:	Eth2_…
Node B Gigabit Ethernet signals:	Eth3_…
Node B Fast Ethernet signals:	Eth4_…
VME signals:	VME....
Serial ATA channel:	ATA_...

Remark to the Gigabit LAN-Port signal names:

Gigabit Ethernet has 4 differential pairs per Port, e.g.for Eth1:

Eth1_DA ±	used in 100MBit mode as	TxD±	⎫ located on P0
Eth1_DB ±	used in 100MBit mode as	RxD±	⎪
Eth1_DC ±			⎪
Eth1_DD ±			⎭
Eth1_LED	link LED		⎫ located on P2

Gigabit Ethernet has: 4 differential pairs per Port, e.g.for Eth3:

Eth3_DA ±	used in 100MBit mode as	TxD±	⎫ located on P0
Eth3_DB ±	used in 100MBit mode as	RxD±	⎪
Eth3_DC ±			⎪
Eth3_DD ±			⎭
Eth3_LED	link LED		⎫ located on P2

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2.8.2 VMEbus Connector P1 (P7100)

The following table lists the pin assignments of connector P1. The connector is compatible to the P1 connector of the VMEbus specification ANSI/IEEE STD 1014-1987, IEC 821 and 297, VME64 Vita 1.-1994 and VME64 Extension VITA 1.1-1997.

	z	A	b	c	d
1	NC	D00	BBSY*	D08	+5V (VPC)
2	GND	D01	NC	D09	GND
3	NC	D02	ACFAIL*	D10	NC
4	GND	D03	BG0IN*	D11	NC
5	NC	D04	BG0OUT*	D12	NC
6	GND	D05	BG1IN*	D13	NC
7	NC	D06	BG1OUT*	D14	NC
8	GND	D07	BG2IN*	D15	NC
9	NC	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*
11	NC	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3,3V
13	NC	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3,3V
15	NC	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3,3V
17	NC	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3,3V
19	NC	GND	AM3	A19	NC
20	GND	IACK*	GND	A18	+3,3V
21	NC	IACKIN*	NC	A17	NC
22	GND	IACKOUT*	NC	A16	+3,3V
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7*	A14	+3,3V
25	NC	A06	IRQ6*	A13	NC
26	GND	A05	IRQ5*	A12	+3,3V
27	NC	A04	IRQ4*	A11	NC
28	GND	A03	IRQ3*	A10	+3,3V
29	NC	A02	IRQ2*	A09	NC
30	GND	A01	IRQ1*	A08	+3,3V
31	NC	-12V	+5V STDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V (VPC)

Table 6: P1 Connector

☞ If the ACFAIL* function is not driven by the power supply, ACFAIL* should be strapped to V_{CC} on the VMEbus backplane to avoid spurious interrupts caused by cross talking.
For explanation of signals see VME bus specification.

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2.8.3 VMEbus Connector P2 (P7200)

The following table lists the pin assignments of connector P2. Row b of the connector is compatible to connector P2 of the VMEbus specification ANSI/IEEE STD 1014-1987, IEC 821 and 297, VME64 Vita 1.- 1994 and VME64 Extension VITA 1.1-1997. Row a and c complies to VITA 35-2000 PMC-P4 to VME-P2 rows a and c (P4V2-64ac), optionally row a and c may alternatively be used by VG5 specific signals.

	z	**a** PMCIO or VG5 function::		**B**	**c** PMCIO or VG5 function:			**d** user defined
		VG5_Func.	PMC2_IO		VG5_Func.		PMC2_IO	
1	C2_DCD/TXD-	Eth1_LED	PMC2_IO02	+5V	Eth3_LED		PMC2_IO01	Eth2_TxD-
2	GND	Eth2_LED	PMC2_IO04	GND	Eth4_LED		PMC2_IO03	Eth2_TxD+
3	C2_DSR/TXD+	CPUVIO	PMC2_IO06	Rsv	WDG_REL	EXT16.66MHZ	PMC2_IO05	Eth2_RxD-
4	GND	ACOP_HRST#	PMC2_IO08	VMEA24	BCOP_HRST#		PMC2_IO07	Eth2_RxD+
5	LED A#/BOOTSEL	ACOP_SRST#	PMC2_IO10	VMEA25	BCOP_SRST#		PMC2_IO09	C2_CTS/RXC-/CTS-
6	GND	ACHKSTP_OUT#	PMC2_IO12	VMEA26	BCHKSTP_OUT#		PMC2_IO11	C2_TXD/RXC+/CTS+
7	LED B#/BOOTSEL	ACOP_TCK	PMC2_IO14	VMEA275	BCOP_TCK	JTAG_TCK	PMC2_IO13	C2_RXD/TXC-/RTS-
8	GND	ACOP_TDI	PMC2_IO16	VMEA28	BCOP_TDI	JTAG_TDI	PMC2_IO15	C2_RTS/TXC+/RTS+
9	C1_RxD	ACOP_TMS	PMC2_IO18	VMEA29	BCOP_TMS	JTAG_TMS	PMC2_IO17	C2_RXD-
10	GND	ACOP_TRST	PMC2_IO20	VMEA30	BCOP_TRST#	JTAG_TRST#	PMC2_IO19	C2_DTR/RXD+
11	C1_TxD	ACOP_TDO	PMC2_IO22	VMEA31	BCOP_TDO	JTAG_TDO	PMC2_IO21	Eth4_TxD-
12	GND	AQREQ#	PMC2_IO24	GND	BQREQ#		PMC2_IO23	Eth4_TxD+
13	C4_RxD	AQACK#	PMC2_IO26	+5V	BQACK#		PMC2_IO25	Eth4_RxD-
14	GND	ACHKSTP_IN	PMC2_IO28	VMED16	BCHKSTP_IN#		PMC2_IO27	Eth4_RxD+
15	C4_TxD	-	PMC2_IO30	VMED17	-		PMC2_IO29	C3_RxD-
16	GND	-	PMC2_IO32	VMED18	-		PMC2_IO31	C3_RxD+
17	C6_RxD-	UGPIO0	PMC2_IO34	VMED19	UGPIO16		PMC2_IO33	C3_RXC-/CTS-
18	GND	UGPIO1	PMC2_IO36	VMED20	UGPIO17		PMC2_IO35	C3_RXC+/CTS+
19	C6_RxD+	UGPIO2	PMC2_IO38	VMED21	UGPIO18		PMC2_IO37	C3_TXC-/RTS-
20	GND	UGPIO3	PMC2_IO40	VMED22	UGPIO19		PMC2_IO39	C3_TXC+/RTS+
21	C6_RXC-/CTS-	UGPIO4	PMC2_IO42	VMED23	UGPIO20		PMC2_IO41	C3_TxD-
22	GND	UGPIO5	PMC2_IO44	GND	UGPIO21		PMC2_IO43	C3_TxD+
23	C6_RXC+/CTS+	UGPIO6	PMC2_IO46	VMED24	UGPIO22		PMC2_IO45	C5_RXC-/CTS-
24	GND	UGPIO7	PMC2_IO48	VMED25	UGPIO23		PMC2_IO47	C5_RXC+/CTS+
25	C6_TXC-/RTS-	UGPIO8	PMC2_IO50	VMED26	UGPIO24		PMC2_IO49	C5_TXC-/RTS-
26	GND	UGPIO9	PMC2_IO52	VMED27	UGPIO25		PMC2_IO51	C5_TXC+/RTS+
27	C6_TXC+/RTS+	UGPIO10	PMC2_IO54	VMED28	UGPIO26		PMC2_IO53	C5_TxD-
28	GND	UGPIO11	PMC2_IO56	VMED29	UGPIO27		PMC2_IO55	C5_TxD+
29	C6_TxD-	UGPIO12	PMC2_IO58	VMED30	UGPIO28		PMC2_IO57	C5_RxD-
30	GND	UGPIO13	PMC2_IO60	VMED31	UGPIO29		PMC2_IO59	C5_RxD+
31	C6_TxD+	UGPIO14	PMC2_IO62	GND	UGPIO30		PMC2_IO61	GND
32	GND	UGPIO15	PMC2_IO64	+5V	UGPIO31		PMC2_IO63	+5V (VPC)

Table 7: P2 Connector

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2.8.4 VMEbus Connector P0 (P7000)

The pinning of the Gigabit Ethernet signals complies with VITA31.1-2000 (Giga Ethernet on VME64 backplanes). The mapping of PMC IO follows the VITA 35 2000 (PMC-P4 Pin Out Mapping To VME-P0 and VME64x-P2) as long as not violated by VITA 31.1.
That means PMC 1_IO 01...PMC1_ IO25 don't comply with VITA 35. Optionally some PMC1 IO pins may alternatively be used by Serial ATA signals (unique VG5).

	a	b		C		d		e		f
1	GND	GND		GND		GND		GND		GND
2	**ETH1_DA+**	**ETH1_DA-**		GND		**ETH1_DC+**		**ETH1_DC-**		GND
3	**ETH1_DB+**	**ETH1_DB-**		GND		**ETH1_DD+**		**ETH1_DD-**		GND
4	**ETH3_DA+**	**ETH3_DA-**		GND		**ETH3_DC+**		**ETH3_DC-**		GND
5	**ETH3_DB+**	**ETH3_DB-**		GND		**ETH3_DD+**		**ETH3_DD-**		GND
6	GND	GND		GND		GND		GND		GND
7	PMC1_IO05	PMC1_IO04		PMC1_IO03		PMC1_IO02		PMC1_IO01		GND
8	PMC1_IO10	PMC1_IO09		PMC1_IO08		PMC1_IO07		PMC1_IO06		GND
9	PMC1_IO15	PMC1_IO14		PMC1_IO13		PMC1_IO12		PMC1_IO11		GND
10	PMC1_IO20	PMC1_IO19		PMC1_IO18		PMC1_IO17		PMC1_IO16		GND
11	PMC1_IO25	PMC1_IO24		PMC1_IO23		PMC1_IO22		PMC1_IO21		GND
12	PMC1_IO30	PMC1_IO29		PMC1_IO28		PMC1_IO27		PMC1_IO26		GND
13	PMC1_IO35	PMC1_IO34		PMC1_IO33		PMC1_IO32		PMC1_IO31		GND
14	PMC1_IO40	PMC1_IO39		PMC1_IO38		PMC1_IO37		PMC1_IO36		GND
15	PMC1_IO45	PMC1_IO44		PMC1_IO43		PMC1_IO42		PMC1_IO41		GND
16	PMC1_IO50	PMC1_IO49		PMC1_IO48		PMC1_IO47		PMC1_IO46		GND
17	PMC1_IO55	P1_IO54	GND	P1_IO53	GND	P1_IO52	GND	P1_IO51	GND	GND
18	PMC1_IO60	P1_IO59	GND	P1_IO58	ATA_TX+	P1_IO57	GND	P1_IO56	ATA_RX-	GND
19	RSTBUT#	P1_IO64	GND	P1_IO63	ATA_TX-	P1_IO62	GND	P1_IO61	ATA_RX+	GND

Table 8: P0 Connector

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2.8.5 PMC Slot 1 connectors (P7101, P7102, P7103)

The following table lists the pin assignments of the onboard PMC1 connector. The PMC slot is 64bit and can operate at PCI-33, PCI-66 or PCI-X-100Mhz and is connected to the first PCI bus of Node A. The PMC is electrical and mechanical compliant to the specification P1386 and P1386.1 with enhancements of the Processor PMC Standard VITA 32-199x. The VG5 enhancements provide pins for PCI-X support and a second device (IDSELB and REQB/GNTB), but doesn't support a monarch PMC card.

P7101	P7102	P7103	Pin	Pin	P7101	P7102	P7103
TCK	+12V	rsv	**01**	**02**	-12V	TRST#	GND
GND	TMS	GND	**03**	**04**	A_INTB# (inta#)	TDO	C/BE7
A_INTC# (intb#)	TDI	C/BE6	**05**	**06**	A_INTD# (intc#)	GND	C/BE5
PRESENT#	GND	C/BE4	**07**	**08**	+5V	rsv	GND
A_INTA# (intd#)	rsv	V(IO)	**09**	**10**	rsv	rsv	PAR64
GND	PUP	AD63	**11**	**12**	nc	+3.3V	AD62
PCICLK	PCIRST#	AD61	**13**	**14**	GND	PDN	GND
GND	+3.3V	GND	**15**	**16**	GNT0#	PDN	AD60
REQ0#	PME#	AD59	**17**	**18**	+5V	GND	AD58
V(IO)	AD30	AD57	**19**	**20**	AD31	AD29	GND
AD28	GND	V(IO)	**21**	**22**	AD27	AD26	AD56
AD25	AD24	AD55	**23**	**24**	GND	+3.3V	AD54
GND	AD30(idsel)	AD53	**25**	**26**	C/BE3#	AD23	GND
AD22	+3.3V	GND	**27**	**28**	AD21	AD20	AD52
AD19	AD18	AD51	**29**	**30**	+5V	GND	AD50
V(IO)	AD16	AD49	**31**	**32**	AD17	C/BE2#	GND
FRAME#	GND	GND	**33**	**34**	GND	AD29(idselb)	AD48
GND	TRDY#	AD47	**35**	**36**	IRDY#	+3.3V	AD46
DEVSEL#	GND	AD45	**37**	**38**	+5V	STOP#	GND
PCIXCAP	PERR#	V(IO)	**39**	**40**	LOCK#	GND	AD44
rsv	+3.3V	AD43	**41**	**42**	res	SERR#	AD42
PAR	C/BE1#	AD41	**43**	**44**	GND	GND	GND
V(IO)	AD14	GND	**45**	**46**	AD15	AD13	AD40
AD12	M66EN	AD39	**47**	**48**	AD11	AD10	AD38
AD9	AD8	AD37	**49**	**50**	+5V	+3.3V	GND
GND	AD7	GND	**51**	**52**	C/BE0#	REQB#	AD36
AD6	+3.3V	AD35	**53**	**54**	AD5	GNTB#	AD34
AD4	rsv	AD33	**55**	**56**	GND	GND	GND
V(IO)	nc	V(IO)	**57**	**58**	AD3	EREADY	AD32
AD2	GND	rsv	**59**	**60**	AD1	RESETOUT#	rsv
AD0	ACK64#	rsv	**61**	**62**	+5V	+3.3V	GND
GND	GND	GND	**63**	**64**	REQ64#	nc	rsv

Table 9: PMC Slot 1 Connectors

Nc	Not connected
Rsv	Reserved. Do not connect anything
V(IO)	IO Voltage, connected with +5V
+12V/-12V	Only available if connected at the VME backplane.
PUP	Weak 10kΩ pull-up to VIO
PDN	Weak 10kΩ pull-down to GND

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2.8.6 PMC Slot 2 connectors (P7201, P7202)

PMC2 is only available without the front Ethernet and/or front COM2 (P2720) connector.
The following table lists the pin assignments of the onboard PMC2 connector. The PMC slot is 64bit and PCI 33MHz capable and is connected to the first PCI bus of Node B. In single node configuration this bus is connected to the second PCI bus of Node A. The PMC is electrical and mechanical compliant to the specification P1386 and P1386.1 with enhancements of the Processor PMC Standard VITA 32-199x. The enhancements provide pins for a second device (IDSELB and REQB/GNTB) but don't support a monarch PMC card.

P7101	P7102	P7103	Pin	Pin	P7101	P7102	P7103
TCK	+12V	rsv	**01**	**02**	-12V	TRST#	GND
GND	TMS	GND	**03**	**04**	B_INTC# (inta#)	TDO	C/BE7
B_INTD# (intb#)	TDI	C/BE6	**05**	**06**	B_INTA# (intc#)	GND	C/BE5
PRESENT#	GND	C/BE4	**07**	**08**	+5V	rsv.	GND
B_INTB# (intd#)	Rsv	V(IO)	**09**	**10**	rsv	rsv	PAR64
GND	PUP[1)]	AD63	**11**	**12**	nc	+3.3V	AD62
PCICLK	PCIRST#	AD61	**13**	**14**	GND	#PDN[1)]	GND
GND	+3.3V	GND	**15**	**16**	GNT0#	PDN[1)]	AD60
REQ0#	PME#	AD59	**17**	**18**	+5V	GND	AD58
V(IO)	AD30	AD57	**19**	**20**	AD31	AD29	GND
AD28	GND	V(IO)	**21**	**22**	AD27	AD26	AD56
AD25	AD24	AD55	**23**	**24**	GND	+3.3V	AD54
GND	AD29(idsel)	AD53	**25**	**26**	C/BE3#	AD23	GND
AD22	+3.3V	GND	**27**	**28**	AD21	AD20	AD52
AD19	AD18	AD51	**29**	**30**	+5V	GND	AD50
V(IO)	AD16	AD49	**31**	**32**	AD17	C/BE2#	GND
FRAME#	GND	GND	**33**	**34**	GND	AD28(idselb)	AD48
GND	TRDY#	AD47	**35**	**36**	IRDY#	+3.3V	AD46
DEVSEL#	GND	AD45	**37**	**38**	+5V	STOP#	GND
GND	PERR#	V(IO)	**39**	**40**	LOCK#	GND	AD44
rsv	+3.3V	AD43	**41**	**42**	rsv	SERR#	AD42
PAR	C/BE1#	AD41	**43**	**44**	GND	GND	GND
V(IO)	AD14	GND	**45**	**46**	AD15	AD13	AD40
AD12	M66EN	AD39	**47**	**48**	AD11	AD10	AD38
AD9	AD8	AD37	**49**	**50**	+5V	+3.3V	GND
GND	AD7	GND	**51**	**52**	C/BE0#	REQB#	AD36
AD6	+3.3V	AD35	**53**	**54**	AD5	GNTB#	AD34
AD4	Rsv	AD33	**55**	**56**	GND	GND	GND
V(IO)	Nc	V(IO)	**57**	**58**	AD3	EREADY	AD32
AD2	GND	rsv	**59**	**60**	AD1	RESETOUT#	rsv
AD0	ACK64#	rsv	**61**	**62**	+5V	+3.3V	GND
GND	GND	GND	**63**	**64**	REQ64#	nc	rsv

Table 10: PMC Slot 2 Connectors

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☞	nc	Not connected
	rsv.	Reserved. Do not connect anything
	V(IO)	IO Voltage, connected with +5V
	+12V/-12V	Only available if connected at the VME backplane.
	PUP	Weak 10kΩ pull-up to VIO
	PDN	Weak 10kΩ pull-down to GND

2.8.7 PMC-IO connector (P7104 and P7204)

The VG5 provides all PMC IO of both PMC slots at the rear connector. These PMC IO signals can be accessed via connectors at the transition module VTM20 (see Appendix). The pinning of PMC1 IO and PMC2 IO are the same for both.

Pin	P7104/P7204 (Pn4)		Pin
01	PMCx_IO01	PMCx_IO02	02
03	PMCx_IO03	PMCx_IO04	04
05	PMCx_IO05	PMCx_IO06	06
07	PMCx_IO07	PMCx_IO08	08
09	PMCx_IO09	PMCx_IO10	10
11	PMCx_IO11	PMCx_IO12	12
13	PMCx_IO13	PMCx_IO14	14
15	PMCx_IO15	PMCx_IO16	16
17	PMCx_IO17	PMCx_IO18	18
19	PMCx_IO19	PMCx_IO20	20
21	PMCx_IO21	PMCx_IO22	22
23	PMCx_IO23	PMCx_IO24	24
25	PMCx_IO25	PMCx_IO26	26
27	PMCx_IO27	PMCx_IO28	28
29	PMCx_IO29	PMCx_IO30	30
31	PMCx_IO31	PMCx_IO32	32
33	PMCx_IO33	PMCx_IO34	34
35	PMCx_IO35	PMCx_IO36	36
37	PMCx_IO37	PMCx_IO38	38
39	PMCx_IO39	PMCx_IO40	40
41	PMCx_IO41	PMCx_IO42	42
43	PMCx_IO43	PMCx_IO44	44
45	PMCx_IO45	PMCx_IO46	46
47	PMCx_IO47	PMCx_IO48	48
49	PMCx_IO49	PMCx_IO50	50
51	PMCx_IO51	PMCx_IO52	52
53	PMCx_IO53	PMCx_IO54	54
55	PMCx_IO55	PMCx_IO56	56
57	PMCx_IO57	PMCx_IO58	58
59	PMCx_IO59	PMCx_IO60	60
61	PMCx_IO61	PMCx_IO62	62
63	PMCx_IO63	PMCx_IO64	64

Table 11: PMC1/2 IO Connector

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2.8.8 COP Interface Connectors (J1100, J1101)

Each of the two CPUs has its own COP interface for debugging.
J1100 is dedicated to CPU A and J1101 for CPU B.

J1100 and J1101 are 16 pin connectors in 1.27mm grid but only accessible at the board. For connecting a compatible 2.54mm pitch connector an interface is necessary.

Signal	J1100		Signal
ACOP_TDO	1	2	A_\QACK
ACOP_TDI	3	4	A_\COP_TRST
A_\QREQ	5	6	VIO Sense (2.5V)
ACOP_TCK	7	8	NC
ACOP_TMS	9	10	NC
A_\COP_SRESET	11	12	NC
A_\COP_HRESET	13	14	NC
A_\CHKSTOP	15	16	GND

Signal	J1101		Signal
BCOP_TDO	1	2	B_\QACK
BCOP_TDI	3	4	B_\COP_TRST
B_\QREQ	5	6	VIO Sense (2.5V)
BCOP_TCK	7	8	NC
BCOP_TMS	9	10	NC
B_\COP_SRESET	11	12	NC
B_\COP_HRESET	13	14	NC
B_\CHKSTOP	15	16	GND

Table 12: J1100 A-COP, J1101 B-COP

The COP interface signals are also available at the P2 connector but are shared with other signals, please see P2 pin listing for configuration.
For the COP interface pull-up and pull-down resistors are recommended. The following table list the used resistor values.

Signal	Resistor Value, pull-up or pull down
\COP_HRESET	1kΩ, pull-up 2.5V
\COP_SRESET	1kΩ, pull-up2.5V
COP_TMS	10kΩ, pull-up 2.5V
COP_TCK	10kΩ, pull-up 2.5V
\COP_TRST	1kΩ, pull-down GND
COP_TDI	10kΩ, pull-up 2.5V
\CHKSTOP	10kΩ, pull-up 2.5V
VIO Sense	220Ω serial resistor to 2.5V

Table 13: COP Terminations

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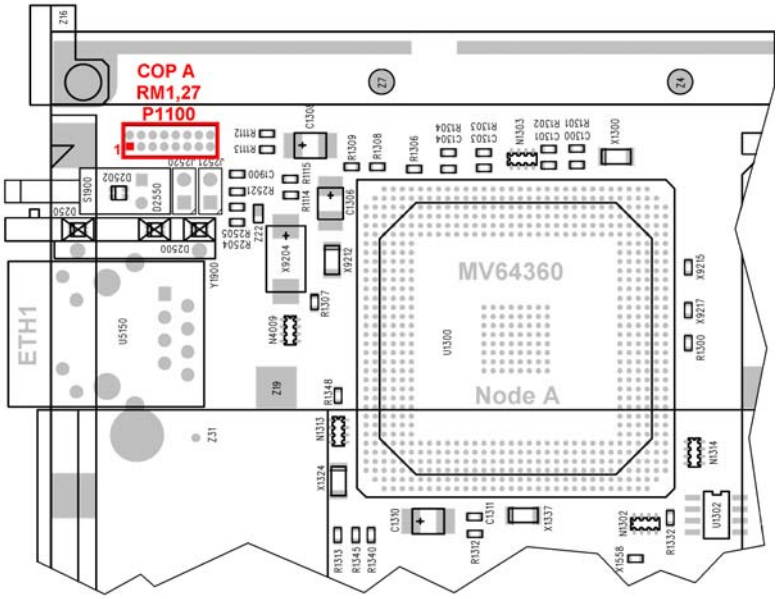


Figure 13: COPA P1100 Connector Location

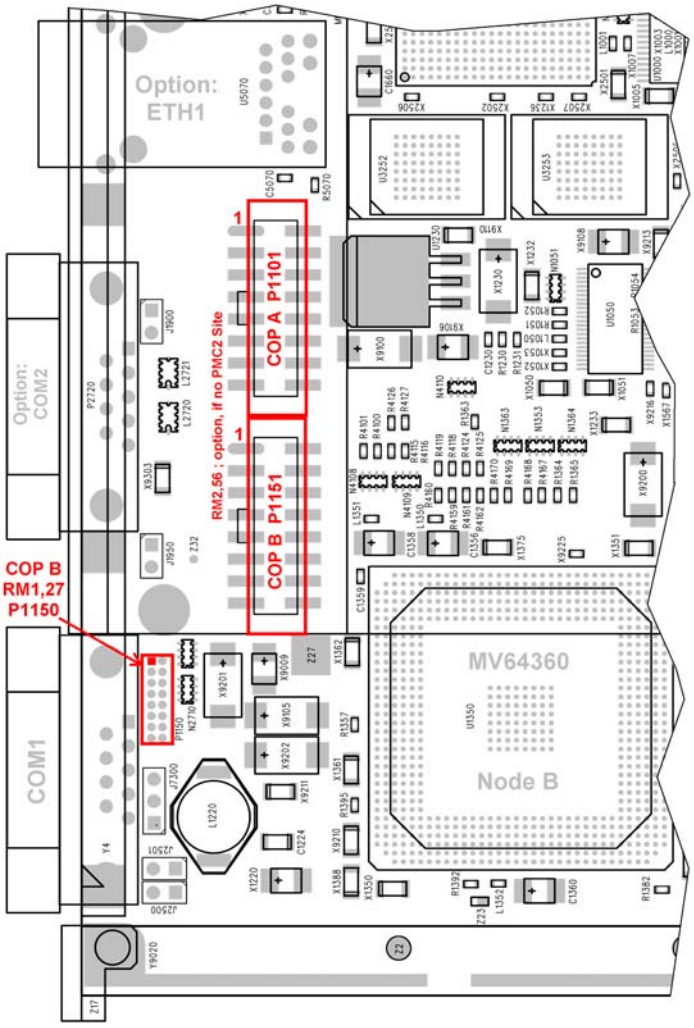


Figure 14: COPA: P1101 , COP B: P1150/1

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2.8.9 JTAG Interface

A JTAG interface is available for testing the connected devices according IEEE1149.1. Please call the factory for the actual JTAG chain ordering.
The JTAG interface signals are available at the P2 connector but are shared with other signals see P2 pin listing.

2.9 PCI-IDSEL

Each PCI device has a unique PCI address/data signal connected to the IDSEL input. The following table provides the IDSEL on the VG5 board for the three separate PCI buses (dual node) respectively two PCI buses (single node).

Dual Node PCI 0 of Node A:

IDSEL	Device
AD31	Chipset PCI 0 Controller of Node A
AD30	First IDSEL of PMC1
AD29	Second IDSEL of PMC1

Dual Node PCI 1 Interconnection Node A/B:

IDSEL	Device
AD31	Chipset PCI 1 Controller of Node A
AD30	Chipset PCI 1 Controller of Node B

Dual Node PCI 0 of Node B:

IDSEL	Device
AD31	Chipset PCI 0 Controller of Node B
AD30	VME Bus Controller
AD29	First IDSEL of PMC2
AD28	Second IDSEL of PMC2
AD27	SATA Controller

Single Node PCI 0 of Node A:

IDSEL	Device
AD31	Chipset PCI 0 Controller of Node A
AD30	First IDSEL of PMC1
AD29	Second IDSEL of PMC1

Single Node PCI 1 of Node A:

IDSEL	Device
AD31	Chipset PCI 1 Controller of Node AB
AD30	VME Bus Controller
AD29	First IDSEL of PMC2
AD28	Second IDSEL of PMC2
AD27	SATA Controller

Table 14 a-e: PCI-IDSEL

Remark: IDSEL is driven High during a Configuration Access – so for a Configuration Read on e.g. the VME Bus Controller AD30 of PCI0 Node B has to be 1 during address phase, when C/BE# = CFG-RD , see PCI-Spec for details.

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2.10 Interrupts

On the VG5 board two chip devices perform interrupt handling with integrated interrupt controllers, these are the MV64360 chipsets and the FPGA. The master IRQ controller is the chipset for each node. The FPGA has a small IRQ controller for each node included, which extends the IRQ controller of the chipset. Sources of interrupts may be any of the following:

MV64360 Chipset Intern:	CPU, DRAM, Device Interface, integrated SRAM, PCI0/1, Ethernet0/1, IDMA, Timers, Serial Communication controllers (MPSC0/1), SDMA, Baud Rate Generators, GPP, TWSI
MV64360 Chipset extern:	PCI busses INTA/B/C/D, VME Bridge, S-ATA, FPGA-IRQ
managed by FPGA:	RTC, UGPIO, Thermo Sensor A/B/C, UART, Watchdog, Dual Port RAM Mailbox IRQ, VMEbus Error IRQ.

The IRQ-cause can be determined very quickly by querying at first the Main Interrupt Cause Register and then the next in the tree structure of cause registers:

MV64360 Interrupt Cause registers (per Node)
- CPU Cause register
- CPU Doorbell register
- DRAM Cause register
- Device Interface Cause register
- Integrated SRAM Cause register
- PCI0 Cause register
- PCI0 Inbound Cause register
- PCI0 Outbound Cause register
- PCI1 Cause register
- PCI1 Inbound Cause register
- PCI1 Outbound Cause register
- Ethernet Unit Cause register
- Ethernet0 Cause register
- Ethernet1 Cause register
- IDMA Cause register
- Timers Cause register
- Comm Unit Cause register
- MPSC0 Cause register
- MPSC1 Cause register
- SDMA Cause register
- BRG Cause register
- GPP Cause register
- TWSI Cause register

FPGA Cause register:
- A_IRQ_CAUSE register (Node A)
- B_IRQ_CAUSE register (Node B)
- UGPIO: A_IRQEVENT register (Node A)
- UGPIO: B_IRQEVENT register (Node B)

See also the MV64360 datasheet and chapter 3.6.2.2 and 3.6.2.3 and Figure 17.
The MV64360 datasheet is directly available from Marvell, but you have to sign a NDA with Marvell.

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Usage of Chipset (MV64360) MPP input pins for interrupts:

Node A: (Dual and Single Node Board)

A Chipset GPP bit	Interrupt Function	Remark
MPP20	A_FPGA_IRQ	Input for normal interrupts coming from FPGA IRQ-Controller A (for example UART, RTC, GPIO...)
MPP21	AG0_INT	Interrupt Input for Gigabit-Ethernet PHY A
MPP22	P1_INTA	PCI bus 1 Interrupt A (only for link of Nodes)
MPP23	P1_INTB	PCI bus 1 Interrupt B (only for link of Nodes)
MPP24	A_INTA	Node A PCI bus 0 Interrupt A (PMC1 slot)
MPP25	A_INTB	Node A PCI bus 0 Interrupt B (PMC1 slot)
MPP26	A_INTC	Node A PCI bus 0 Interrupt C (PMC1 slot)
MPP27	A_INTD	Node A PCI bus 0 Interrupt D (PMC1 slot)
MPP28	B_INTA	Node B PCI bus 0 Interrupt A (single node only)
MPP29	B_INTB	Node B PCI bus 0 Interrupt B (single node only)
MPP30	B_INTC	Node B PCI bus 0 Interrupt C (single node only)
MPP31	B_INTD	Node B PCI bus 0 Interrupt D (single node only)

Table 15: IRQ inputs Node A (MPP of Chipset A)

Node B: (Dual Node Board)

B Chipset GPP bit	Interrupt Function	Remark
MPP20	B_FPGA_IRQ	Input for normal interrupts coming from FPGA IRQ-Controller B (for example UART, GPIO...)
MPP21	BG0_INT	Interrupt Input for Gigabit-Ethernet PHY A
MPP22	P1_INTB	PCI bus 1 Interrupt A (only for link of Nodes)
MPP23	P1_INTA	PCI bus 1 Interrupt B (only for link of Nodes)
MPP24	-	not used
MPP25	-	not used
MPP26	-	not used
MPP27	-	not used
MPP28	B_INTA	Node B PCI bus 0 Interrupt A (dual node only)
MPP29	B_INTB	Node B PCI bus 0 Interrupt B (dual node only)
MPP30	B_INTC	Node B PCI bus 0 Interrupt C (dual node only)
MPP31	B_INTD	Node B PCI bus 0 Interrupt D (dual node only)

Table 16: IRQ inputs Node B (B Chipset MPP)

See also chapter 3.6.2.2 and 3.6.2.3 and Figure 17 for details to A/B_FPGA_IRQ.

Attention: Other MPP pins are used for other functions as e.g. MPSC inputs.

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2.11 Reset

The VG5 has five different sources of reset.

- Power-on reset
- Reset switch
- Watchdog Timer reset
- Reset from the COP debug interface
- VMEbus SYSRESET* signal

The affected devices of the various reset types are listed in the table below:

	Processor Node A	Chipset Node A	PCI Node A	Processor Node B	Chipset Node B	PCI Node B	VME Bus [1]
Power Monitor reset	X	X	X	X	X	X	X
Reset switch	X	X	X	X	X	X	X
Watchdog reset Node A[2]	X	X	X				
Reset COP interface Node A	X	X	X				
Watchdog reset Node B[2]				X	X	X	X
Reset COP interface Node B				X	X	X	X
VME SYSRESET	X	X	X	X	X	X	X

Table 17: Reset Sources

1) Only valid if VG5 is VME System Controller
2) Kind of watchdog reset depends on bits A/B_WDGRSTMODE[1:0] in register A/B_CNTRLSTAT (see chapter 3.6.2.5 and 3.6.2.7)

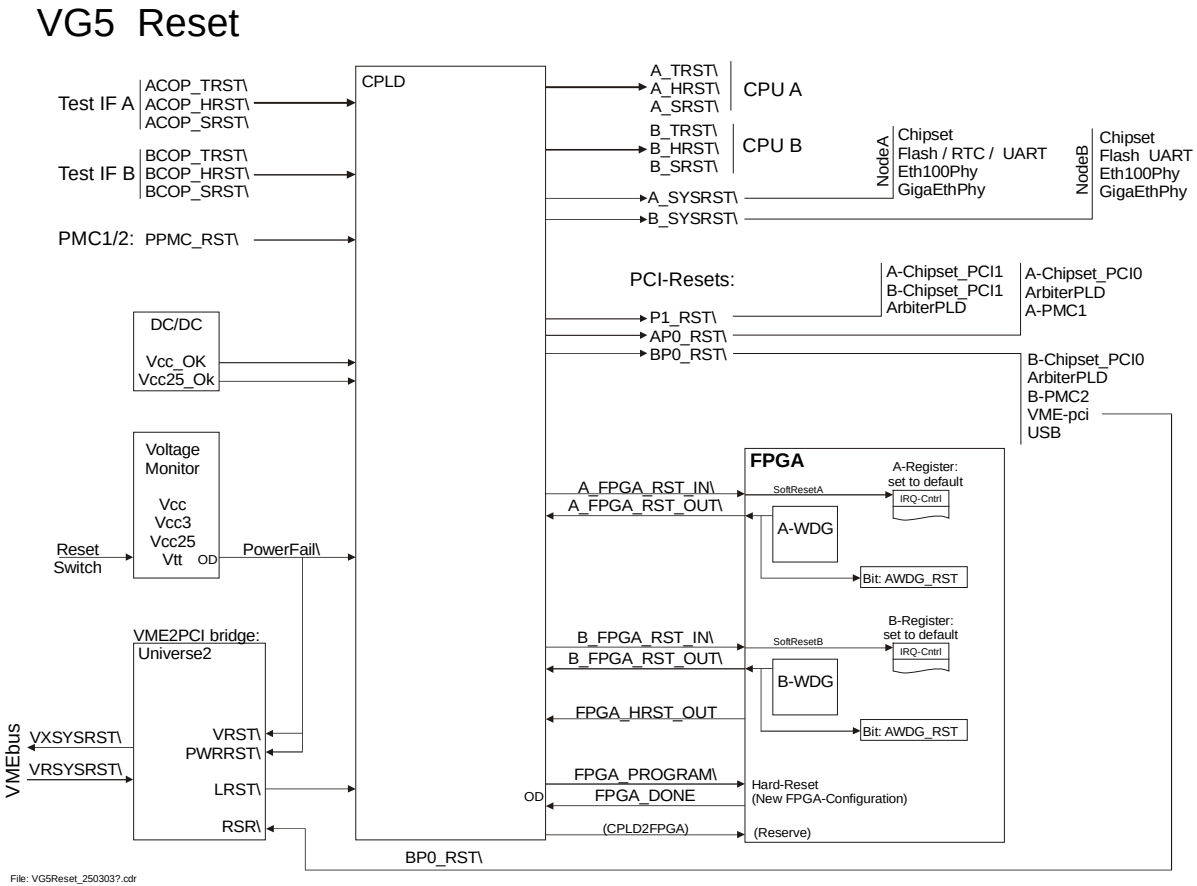


Figure 15: Reset Structure

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3 Function Blocks

3.1 PowerPC Processor

The VG5 board provides the usage of MPC7455 and MPC7457 PowerPC processors. With frequencies from 800MHz to +1300MHz and core voltage supplies from 1.75V down to 0.6V. The VG5 can support either one or two CPUs. Each CPU has its own chipset and memory for independent operation.

3.2 L3 Cache

The L3 cache of 2MByte (PowerPC MPC7455) or 4MByte (PowerPC MPC7457 with 2MByte cache and 2MByte conventional SRAM) has an direct interface to the CPU and works with a maximal speed of 200MHz. It consists of Synchronous Pipelined Burst SRAM with an access time <3ns. The L3 cache is ECC protected.

3.3 Chipset

The VG5 uses the Marvell MV64360 chipset. This is a highly integrated system controller which provides a PowerPC CPU bus interface, memory controller, device controller (direct connection to standard logic), 2 PCI bus interfaces, two Ethernet MAC controllers and two Multi-Protocol Serial Controllers as the main features. Each Processor Node has one chipset for independent operation. For a complete description see the Marvel MV64360 datasheet.

3.4 DDR-SDRAM Memory

The VG5 provides at each chipset one bank of 64bit wide Double Data Rate-SDRAM memory with 133MHz memory clock. It is controlled by the MV64360 chipset controller with ECC single-bit error correction and double-bit error detection. The size of each bank can be 256MByte, 512MByte or 1Gbyte.

3.5 Flash ROM

The VG5 contains for each node two banks of Flash memory. This provides 64MByte (one bank) or 128MByte (two banks) of Flash memory capacity for each node - so maximum Flash memory per board is 256MByte. The Flash memory is connected to the 32bit wide Device Bus of the chipset. In single node version the two banks of node B can be assigned to Node A, that will increase the Flash memory to max. 256MByte for Node A.
The Flash memory contains the boot program and the emergency boot program, theses two blocks are individually write protected by hardware jumpers. Additionally the BOOTSEL jumpers select the boot process either from the normal boot or the emergency boot program.
For erase and reprogramming the Flash device and boot behaviour please refer to the software manual.

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3.6 FPGA

3.6.1 Overview (including Registers)

The FPGA is connected to the device busses of Node A and Node B. A device bus is a 32bit wide multiplexed address/data bus. The device busses of Node A and B are independent and only coupled through the dual port RAM inside of the FPGA. The FPGA is a Xilinx Spartan2e type. The base address of the FPGA address decoding is the programmed value of DevCS1 in the chipsets. The default base address after reset is 0x1C80_0000.

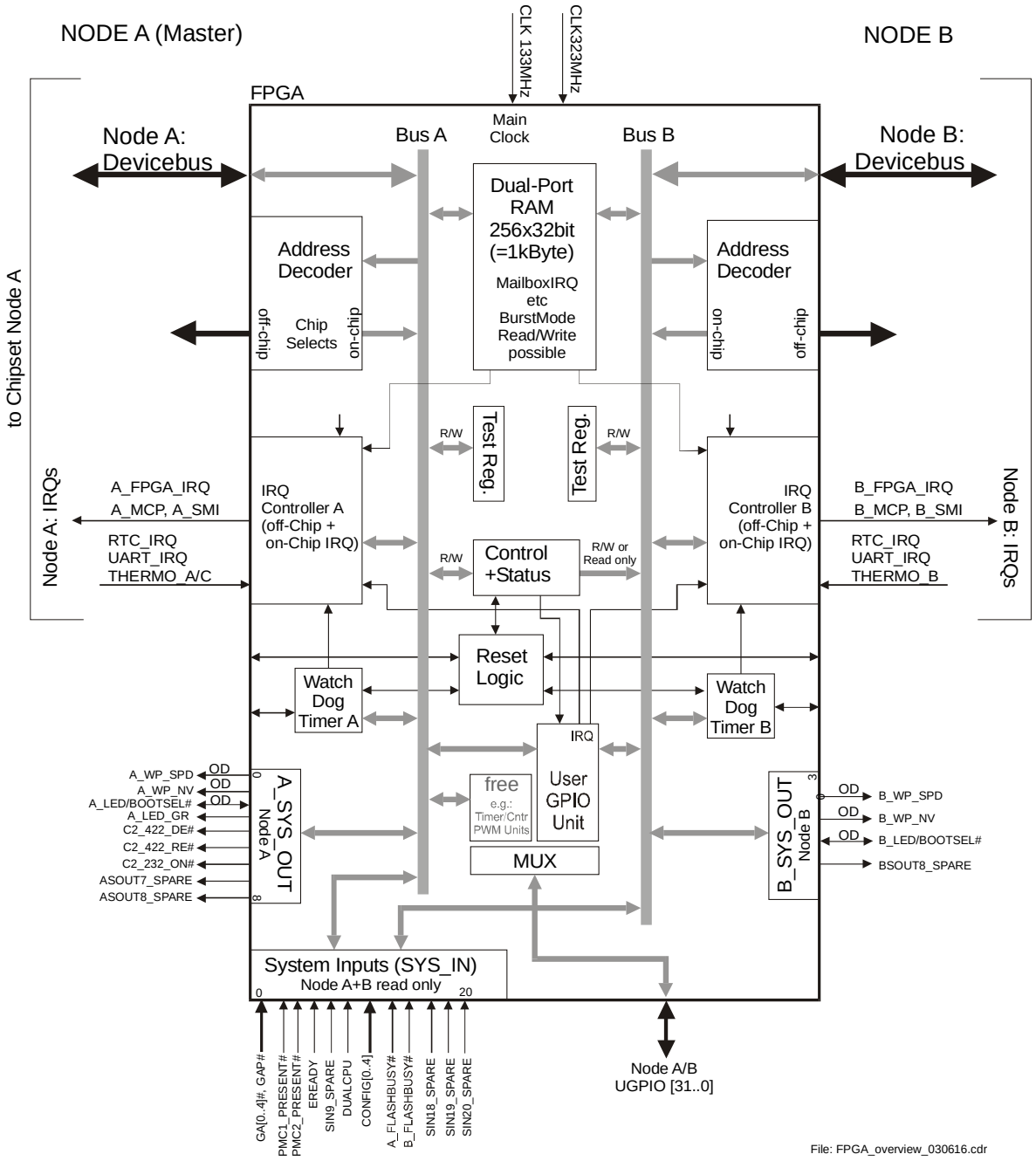


Figure 16: FPGA Block Diagram Dual Node

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Register	Offset	Accessible by Node	Kind of Access	Remarks
Dual-Port-RAM				(for details see chapter 3.6.2.1)
A_DPRAM B_DPRAM	0-0x3FF	A B	R/W R/W	1kByte Dual Port RAM simultaneously accessible by Node A and B
A_DPCNTRL	0x8000	A B	W R	Write Access generates DPRAM_IRQ Interrupt on B-Node side. B-Node can read the written value.
B_DPCNTRL	0x8000	B A	W R	Write Access generates DPRAM_IRQ Interrupt on B-Node side. A-Node can read the written value.
On Board IO Registers				(for details see chapter 3.6.2.8)
A_SYS_OUT	0x8104	A	R/W	Outputs for special onboard functions. Only accessible by Node A. (for details see Table 33)
B_SYS_OUT	0x8104	B	R/W	Outputs for special onboard functions. Only accessible by Node B (for details see Table 34)
SYS_IN	0x8100	A + B	R(W)	Inputs for special onboard functions. Readable for Node A and B (for details see Table 32)
IRQ-Controller Node A				(for details see chapter 3.6.2.29
A_IRQ_CAUSE	0x8300	A	R/W	Node A Interrupt cause register (for details see Table 19)
A_IRQ_MASK	0x8304	A	R/W	Node A Interrupt mask register (for details see Table 21)
IRQ-Controller Node B				(for details see chapter 3.6.2.3)
B_IRQ_CAUSE	0x8300	B	R/W	Node B Interrupt cause register (for details see Table 22)
B_IRQ_MASK	0x8304	B	R/W	Node B Interrupt mask register (for details see Table 24)
UGPIO				(for details see chapter 3.6.2.9)
UGPIO_CONFIG	0x8600	A B	R/W R (WProt)	User GPIO configuration register. Selects which Node a UGPIO bit belongs. Only writeable by Node A (Master) – both nodes can read simultaneously. Write Protection!
UGPIO_MUX	0x8518	A	R/W R/W	For Future extension: Selects between UGPIO function and a secondary funct.(depends on settings in UGPIO_CONFIG)
UGPIO_DIR	0x8504	A B	R/W R/W	Selects if a UGPIO-bit is Input or Output (depends on settings in UGPIO_CONFIG)
UGPIO_IN	0x8500	A+B	R	UGPIO Input register (readable by both nodes)
UGPIO_OUT	0x8500	A B	W W	UGPIO Output register: writeability depends on settings in GPIO_CONFIG
UGPIO_IRQMASK1	0x8508	A B	R/W R/W	Interrupt Mask Register1: Setup for UGPIO[0..15] (depends on settings in UGPIO_CONFIG)
UGPIO_IRQMASK2	0x8510	A B	R/W R/W	Interrupt Mask Register2: Setup for UGPIO[16..31] (depends on settings in UGPIO_CONFIG)
A_IRQEVENT	0x8514	A	R/W	UGPIO IRQ Event register Node A.
B_IRQEVENT	0x8514	B	R/W	UGPIO IRQ Event register Node B.
Watchdog A				(for details see chapter 3.6.2.7)
A_WDGCOMP1/0	0x8200	A	R/W	Watchdog A Compare Register: COMP1: Compare value for Reset (High Word) COMP0: Compare value for A_MCP Interrupt (Low Word)
A_WDGDATA +(Service)	0x8204	A	R(W)	Read: High Word of the 32Bit A_WDG-Counter. Write 0x2A: Service for Watchdog A
Watchdog B				(for details see chapter 3.6.2.7)
B_WDGCOMP1/0	0x8200	B	R/W	Watchdog B Compare Register: COMP1: Compare value for Reset (High Word) COMP0: Compare value for B_MCP Interrupt (Low Word)
B_WDGDATA +(Service)	0x8204	B	R(W)	Read: High Word of the 32Bit B_WDG-Counter. Write 0x2A: Service for Watchdog B
Others				
A_CNTRLSTAT	0x8008	A	R/W (WProt)	Node A Control and Status bits including write protection for CNTRLSTAT and UGPIO_CONFIG register (for details see Table 25)
B_CNTRLSTAT	0x8008	B	R/W (WProt)	Node B Control and Status bits including write protection for B_CNTRLSTAT register (for details see Table 26)
A_TEST	0x8004	A	R/W	Node A Test Register (for details see chapter 3.6.2.6)
B_TEST	0x8004	B	R/W	Node B Test Register (for details see chapter 3.6.2.6)

Table 18: Overview FPGA Registers (Node A and B)

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Remarks to Table 18:

- FPGA Registers names starting with 'A_' are Node A registers.
- FPGA Registers names starting with 'B_' are Node B registers.
- Some registers are read/write for Node A and read only for Node B.
- All register are located on long word boundaries, so all addresses are divideable by four.
- All registers are 32bit wide but some registers use not all bits.
- UGPIO_CONFIG register controls to which node UGPIO register bits belong.
- Register address map is identical seen from Node A or node B side.
- Registers on node B side have some functions less than their counterparts on node A side.
- Register address is calculated : FPGA Base Address + Offset.
- FPGA Base Address is set in the DEVCS1base Register (0x228)in the Node A or B Chipset. Page size has to be 64kByte (DEVCS1SIZE (0x230) = 0)

3.6.2 FPGA Function Blocks

3.6.2.1 Dual Port RAM

The FPGA has a built-in true Dual Port Memory organised as 256x32bit (=1kByte).
The address area is base address+0000h to 03FFh
With two mailbox registers interrupts can be generated on the other node.

A_DPCNTRL Register:	Mailbox A → B 32bit register; Node A write only ; Node B read only a write on side A causes a B_DPRAM_IRQ on side B
B_DPCNTRL Register:	Mailbox B → A 32bit register; Node B write only ; Node A read only a write on side B causes a A_DPRAM_IRQ on side A

Performance: max peak read/write rate to the Dual Port RAM is about 100MByte/sec.

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3.6.2.2 Interrupt Controller A

Each Node has its own independent Interrupt Controller in the FPGA.
The FPGA Interrupt Controller A extends the huge interrupt capabilities of the Chipset of Node A.

Interrupt Controller for Node A has following sources:

FPGA external:	A_RTC_IRQ	Real Time Clock	
	A_UART_INTA	UART A, Channel A	
	A_UART_INTB	UART A, Channel B	(only used in Single Node VG5)
	VME_BERR	VME Bus error	
	THERMO_A	Thermosensor near CPU-A	
	THERMO_B	Thermosensor near CPU-B (used by Node B)	
	THERMO_C	Thermosensor Centre of board	
FPGA internal	A_DPRAM_IRQ	Mailbox Interrupt from Dual Port RAM	
	A_GPIO_IRQ	Interrupt caused by User General Purpose IO (GPIO)	
	A_WDG_IRQ	Watchdog A MCP step reached (causes high Priority MCP IRQ)	
	B_WDG_IRQ	caused by a Fast Reset on Node B side due to Watchdog B	

The Interrupt Controller A has following outputs:

A_FPGA_IRQ	Standard IRQ, connected to the MPP20 pin of chipset A
A_SMI	System Management Interrupt, high Priority IRQ, directly connected to CPU A
A_MCP	Machine Check Interrupt, high Priority IRQ, directly connected to CPU A

A_IRQ_CAUSE Register: This register shows pending IRQs. Address: Base Address + 8300h

		Bit	IRQ-Name	routed to IRQ output	Read/ Write	Remark
A_IRQ_CAUSE-Register	external IRQs	0	A_RTC_IRQ	A_FPGA_IRQ	R	
		1	A_UARTA	A_FPGA_IRQ	R	
		2	A_UARTB	A_FPGA_IRQ	R	
		3	-	-	R=0	Reserve for future off chip IRQ source
		4	VME_BERR	A_MCP	R/W	latched [1) 3)]
		5	THERMO_A	A_SMI	R	[2)]
		6	THERMO_B	A_SMI	R	also connected to Node B IRQ Controller[2) 3)]
		7	THERMO_C	A_SMI	R	[2)]
	internal IRQs	8	-	-	R=0	Reserve for future on-chip IRQ source
		9	-	-	R=0	Reserve for future on-chip IRQ source
		10	-	-	R=0	Reserve for future on-chip IRQ source
		11	-	-	R=0	Reserve for future on-chip IRQ source
		12	A_DPRAM_IRQ	A_FPGA_IRQ	R/W	latched [1)]
		13	A_GPIO_IRQ	A_FPGA_IRQ	R	see A_GPIO IRQ Event Register
		14	A_WDG_IRQ	A_MCP	R/W	latched [1)]
		15	B_WDG_IRQ	A_FPGA_IRQ	R/W	latched [1)]

Table 19: A_IRQ_CAUSE Register

See notes on next page

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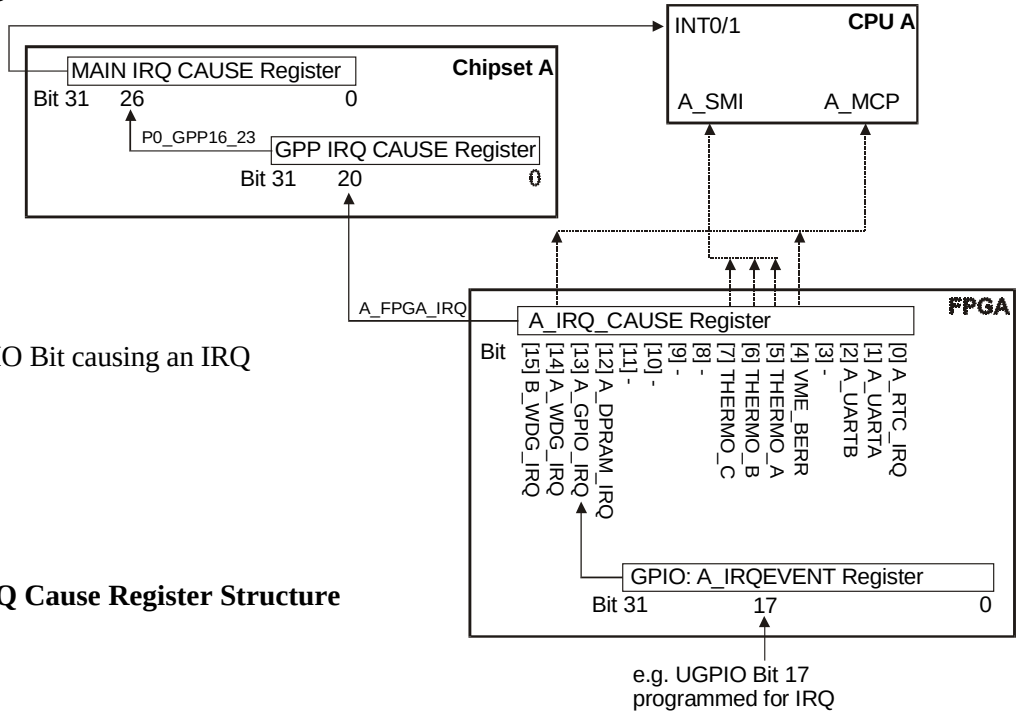
Notes:

1) to reset IRQs that are latched a '1'-bit must be written at the bit in the A_IRQ_CAUSE register, all other IRQs are cleared in the source chip of the IRQ (e.g. RTC chip).
2) THERMO_A/B/C IRQs are connected to the LM75 Temperature sensors. The LM75 must be programmed for interrupt mode. (see LM75 Datasheet). A pending IRQ at the THERMO_A/B/C is cleared by reading any register of the corresponding LM75.
3) VME-BusERR and THERMO_B are also connected to Node B. Software has to select through the IRQ-Mask which node is servicing the IRQ. This feature is also important for the single node VG5 version. Default is:

Interrupt	DualCPU	SingleCPU (only Node A)
VME-BusErr	Node B	Node A
THERMO_A	Node A	Node A
THERMO_B	Node B	Node A
THERMO_C	Node A	Node A

Table 20: VMEbusErr, Thermo_A/B/C IRQs

IRQ Cause Register Structure in VG5:



Example UGPIO Bit causing an IRQ

Figure 17: IRQ Cause Register Structure

A_IRQ_MASK Register:		Address: Base Address + 8304h	
		Bit	**Mask for...**
A_IRQ_MASK Register	external IRQs	0	A_RTC_IRQ#
		1	A_UARTA
		2	A_UARTB
		3	-
		4	VME_BERR#
		5	THERMO_A#
		6	THERMO_B#
		7	THERMO_C#
	internalal IRQs	8	-
		9	-
		10	-
		11	-
		12	A_DPRAM_IRQ
		13	A_GPIO_IRQ
		14	A_WDG_IRQ
		15	B_WDG_IRQ

Table 21: A_IRQ_MASK Register

After a reset the MASK Register is set 0x0000, all IRQs are disabled.

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3.6.2.3 Interrupt Controller B

The FPGA Interrupt Controller B extends the huge interrupt capabilities of the Chipset of Node B. It's structure is identical to Interrupt Controller A, but has less external interrupt sources.

Interrupt Controller for Node B has following IRQ sources:

FPGA external:	B_RTC_IRQ	Real Time Clock
	B_UART_INTA	UART B, Channel A
	VME_BERR	VME Bus error
	THERMO_B	Thermo sensor near CPU-B (also connected to Node A)
FPGA internal	B_DPRAM_IRQ	Mailbox Interrupt from Dual Port RAM
	B_GPIO_IRQ	Interrupt caused by User General Purpose IO (UGPIO)
	B_WDG_IRQ	Watchdog B MCP step reached (causes high Priority MCP IRQ)
	A_WDG_IRQ	caused by a soft reset on Node A side due to Watchdog A

The Interrupt Controller B has following IRQ outputs:

B_FPGA_IRQ	Standard IRQ, connected to the MPP20 pin of chipset B (GPIO of Chipset)
B_SMI	System Management Interrupt, high Priority IRQ, directly connected to CPU B
B_MCP	Machine Check Interrupt, high Priority IRQ, directly connected to CPU B

B_IRQ_CAUSE Register: This register shows pending IRQs. Address: Base address + 8300h

		Bit	IRQ-Name	routed to IRQ output	Read/ Write	Remark
B_IRQ_CAUSE-Register	external IRQs	0	-		R=0	-
		1	B_UARTA	B_FPGA_IRQ	R	
		2	-	-	R=0	-
		3	-	-	R=0	Reserve for future off chip IRQ source
		4	VME_BERR	B_MCP	R/W	latched [1) 3)]
		5	-	-	R=0	-
		6	THERMO_B	B_SMI	R	also connected to Node A IRQ Controller[2) 3)]
		7	-	-	R=0	-
	internal IRQs	8	-	-	R=0	Reserve for future on-chip IRQ source
		9	-	-	R=0	Reserve for future on-chip IRQ source
		10	-	-	R=0	Reserve for future on-chip IRQ source
		11	-	-	R=0	Reserve for future on-chip IRQ source
		12	B_DPRAM_IRQ	B_FPGA_IRQ	R/W	latched [1)]
		13	B_GPIO_IRQ	B_FPGA_IRQ	R	see B_GPIO IRQ Event Register
		14	B_WDG_IRQ	B_MCP	R/W	latched [1)]
		15	A_WDG_IRQ	B_FPGA_IRQ	R/W	latched [1)]

Table 22: B_IRQ_CAUSE Register

See notes on next page

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Notes:

1) to reset IRQs that are latched a '1'-bit must be written at the bit in the B_IRQ_CAUSE register, all other IRQs are cleared in the source chip of the IRQ (e.g. UART chip).
2) THERMO_B IRQ is connected to the LM75 Temperature sensors. The LM75 must be programmed for interrupt mode. (see LM75 Datasheet). A pending IRQ at the THERMO_B is cleared by reading any register of the corresponding LM75.
3) VME-BusERR and THERMO_B are also connected to Node B. Software has to select through the IRQ-Mask which node is servicing the IRQ. This feature is also important for the single node VG5 version. Default is:

Interrupt	DualCPU	SingleCPU (only Node A)
VME-BusErr	Node B	Node A
THERMO_A	Node A	Node A
THERMO_B	Node B	Node A
THERMO_C	Node A	Node A

Table 23: VMEbusErr, Thermo_A/B/C IRQs

B_IRQ_MASK Register:		Address: Base address + 8304h	
		Bit	**Mask for...**
B_IRQ_MASK Register	external IRQs	0	-
		1	B_UARTA
		2	-
		3	-
		4	VME_BERR#
		5	-
		6	THERMO_B#
		7	-
	internal IRQs	8	-
		9	-
		10	-
		11	-
		12	B_DPRAM_IRQ
		13	B_GPIO_IRQ
		14	B_WDG_IRQ
		15	A_WDG_IRQ

Table 24: B_IRQ_MASK Register

After a reset the MASK Register is set 0x0000, all IRQs are disabled.

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3.6.2.4 Address decoder A/B

The device bus address decoder for Node A generates all control signals for RTC, A_UART and the two Flash Memory banks and also for all FPGA internal resources seen from Node A.
The device bus address decoder for Node B generates all control Signals for B_UART and the two Flash Memory banks and also for all FPGA internal resources seen from Node B.
Special function of the address controller is the Flash Write Protect function for some areas of the Flash Memory Bank 1 (Boot Node A/B).

Flash Bank 1 is located at the upper boundary of the 4GByte address space. The entrance point after Reset or Power-Up is in the upper 1MByte where the boot loader is located.
This area is hardware write protected by the FPGA.

The upper 8MByte are per default write protected by the FPGA, but this write protection can be switched of via the A/B_FB1_SYSWP bits in the A/B_CNTRLSTAT register.

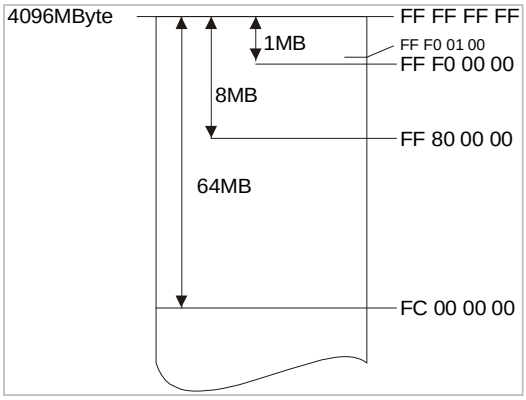


Figure 18: Memory Write Protection Areas

Of course the standard Software Write Protection of the Flash Memory devices can be also used to protect Bank1 and Bank2.

3.6.2.5 Control and Status Register A/B_CNTRLSTAT

In the Node A Control/Status register A_CNTRLSTAT following bits can be found:

A_CNTRLSTAT (Control&Status Register A)					Address: Base address + 8008h
	Bit	**Name**	Read/Write	Default	**Remark**
Byte 0	0	A_WDGRSTMODE0)1	R/W)2	11	00 = No reset when Watchdog A expires)1 (but an MCP can be generated) 01 = A_WDG generates Fast-Reset A when Watchdog A expires
	1	A_WDGRSTMODE1)1	R/W)2		10 = A_WDG generates Fast-Reset A and Fast-Reset B)3 11 = A_WDG generates a hard reset (including FPGA)
	2	A_RESETB	R/W)2	1	0 = Node B normal operation 1 = Node B is held in Reset (if used, Node A software has to control that minimum reset duration of B is 1,1ms)
	3	A_FB1_BootWP	R/W)2	1	0= no write protection 1= Write-Protect for Flash Bank1 (boot area) on
	4	A_FB1_SysWP	R/W)2	1	0= no write protection 1= Write-Protect for Flash Bank1 (system area) on
	5	-	-	0	-
	6	-	-	0	-
	7	WHOAMI	R	0	Node A reads always 0
Byte 1	8	A_RWP[0]	R/W	1	**Write protection** for A_CNTRLSTAT and UGPIO_CONFIG register: Write to this registers is only possible with the magic constant in A_RWP[7:0] = 0b0010'1010=42. This sets A_RWP[0]=0 and the write protection is disabled. Then the next access to A_CNTRLSTAT can be a successful write access. After this access A_RWP[0] is set to one again and the write protection is on again.
	9	A_RWP[1]	W		
		⋮	⋮		
	15	A_RWP[7]	W		
Byte3+2	16	16Bit FPGA-Version)4	R	-	Bit 31..28: min. required VG5 PCB (0.x=0, 1.x=1, 2.x=2,...) Bit 27: Single/DualNode FPGA (0=Single / 1=Dual) Bit 26..20: Standard-FPGA-Version (1=Betas, 2,3,4...) Bit 19..16: Reserve (0000)
	31				

Table 25: A_CNTRLSTAT Register

See notes on next page

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Node B **B_CNTRLSTAT** register is identical to A_CNTRLSTAT, but has some functions missing:

Bit 2 is not used. (A_RESETB is here located in A_CNTRLSTAT, there is no B_RESETA)

Bit 7: WHOAMI reads always 1

Bit15..8: B_RWP[7:0] is only write protection for B_CNTRLSTAT (but not for UGPIO_CONFIG).

B_CNTRLSTAT (Control&Status Register B)					Address: Base address + 8008h
	Bit	**Name**	Read/Write	Default	**Remark**
Byte 0	0	B_WDGRSTMODE0[1]	R/W[2]		00 = No reset when Watchdog B expires [1] (but an MCP can be generated) 01 = B_WDG generates Fast-Reset B when Watchdog B expires
	1	B_WDGRSTMODE1[1]	R/W[2]	11	10 = B_WDG generates Fast-Reset B and Fast-Reset A [3] 11 = B_WDG generates a hard reset (including FPGA)
	2	-	-	-	-
	3	B_FB1_BootWP	R/W[2]	1	0= no write protection 1= Write-Protect for Flash Bank1 (boot area) on
	4	B_FB1_SysWP	R/W[2]	1	0= no write protection 1= Write-Protect for Flash Bank1 (system area) on
	5	-	-	0	-
	6	-	-	0	-
	7	WHOAMI	R	0	Node B reads always 1
Byte 1	8	B_RWP[0]	R/W	1	**Write protection** for B_CNTRLSTAT Register: Write to this registers is only possible with the magic constant in B_RWP[7:0] = 0b0010'1010=42. This sets B_RWP[0]=0 and the write protection is disabled. Then the next access to B_CNTRLSTAT can be a successful write access. After this access B_RWP[0] is set to one again and the write protection is on again.
	9	B_RWP[1]	W		
	⋮	⋮	⋮		
	15	B_RWP[7]	W		
Byte3+2	16 ⋮ 31	16Bit FPGA-Version[4]	R	-	Bit 31..28: min. required VG5 PCB (0.x=0, 1.x=1, 2.x=2,...) Bit 27: Single/DualNode FPGA (0=Single / 1=Dual) Bit 26..20: Standard-FPGA-Version (1=Betas, 2,3,4...) Bit 19..16: Reserve (0000)

Table 26: B_CNTRLSTAT Register

Notes:
1) If the A or B_WDG_Off_Jumper is set, A/B_WDGRSTMODE[1:0] is always 00, so Watchdog Reset A/B is off
2) Write protected by A/B_RWP[7:0]
3) A/B_WDGRST bits located in SYS_IN register are set when a Fast-Reset A/B occurs. See also chapter 3.6.2.8.
4) **Remark regarding 16-Bit FPGA version register**

FPGA-Beta-Versionen (Single/Dual) 0x1010

Single Node PCB0.x, first FPGA-version with new version register:
0000'0000'0010'0000 = 0x0020
e.g.: further SingleNode FPGA-Versions 0x0030, 0x0040, 0x0050, ... 0x07F0

Dual Node PCB0.x, first FPGA-version with new version register:
0000'1000'0010'0000 = 0x0820
e.g.: further DualNode FPGA-Versionen 0x0830, 0x0840, 0x0850, ... 0x0FF0

E.g.: A future FPGA-Version (with a changed pinout), which would require a special VG5-PCB version (e.g. PCB 2.x and higher), would have the dual-version : e.g.: 0x2830 = PCB2.x,Dual,FPGA3

3.6.2.6 Test Register A/B

The test register A/B is only used for Factory testing

Test-Register Node A/B			Address: Base address + 8004h
Name	Bit	Read/Write	Remark
A/B_TEST	32Bit width	R/W	the written long word will be read inverted.

Table 27: Test register A/B

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3.6.2.7 Watchdog Timer A/B

For security of application software, the VG5 offers a software controlled hardware watchdog capable of issuing a reset signal if its time-out interval expires. To prevent the watchdog from generating a reset signal, it must be serviced within a programmable interval by writing a magic constant to the watchdog register WDGDATA.

There is for Node A Watchdog A and for Node B Watchdog B. Each watchdog is exclusively bound to its Node.

The Watchdog consists of a 32bit counter using the 133MHz system clock as input clock. The upper 16 bit of the counter are compared against the 16bit registers COMP0 and 1, and if equal a MCP is caused by COMP0 and a reset by COMP1.

So the Watchdog expire time is programmable in steps of 492µs up to the max. time of 32,29s using the standard 133MHz system clock.

(at 100MHz system clock 656µs up to 43s)

Watchdog A has following registers:

- A_WDGCOMP0 and A_WDGCOMP1
- A_WDGDATA (+ service)
- A_WDGRSTMODE[1:0] bits
  located in A_CNTRLSTAT register
- A_WDG1A/B_EXP bits
  located in SYS_IN register

Watchdog B has following registers:

- B_WDGCOMP0 and B_WDGCOMP1
- B_WDGDATA (+ service)
- B_WDGRSTMODE[1:0] bits
  located in B_CNTRLSTAT register
- B_WDG1B/A_EXP bits located in SYS_IN register

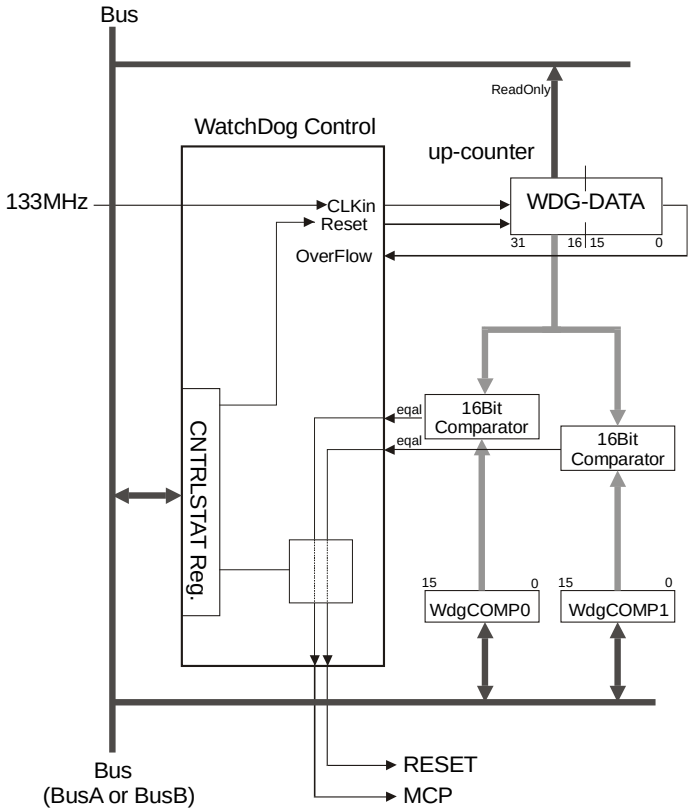


Figure 19: Watchdog Block Diagram

The Figure below shows some different working examples of the Watchdog:

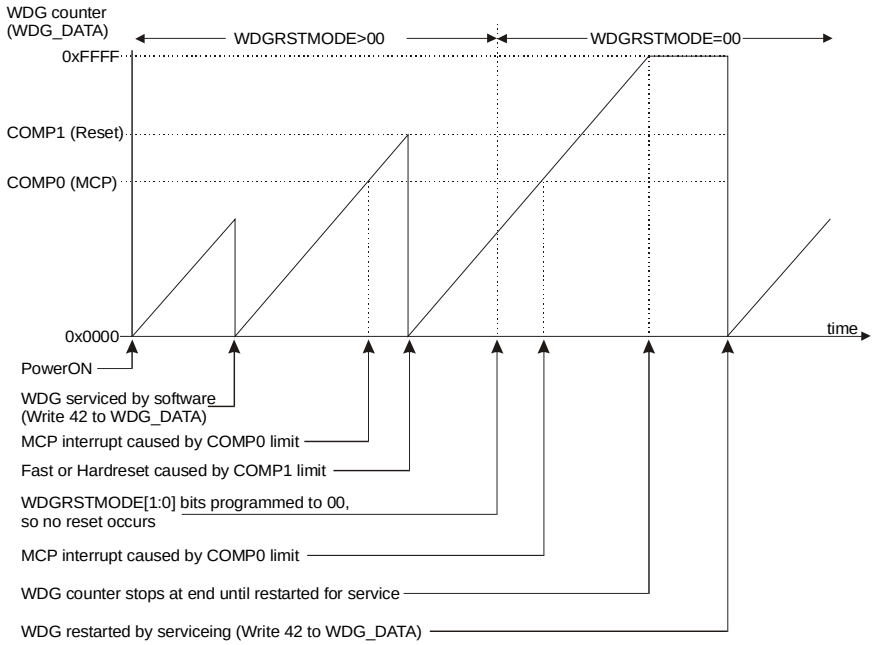


Figure 20: Watchdog Timing Diagram

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3.6.2.7.1 Watchdog A/B Registers detailed

Watchdog A/B Compare Register (0+1)			Address: Base address + 8200h
Name	Bit	Read/Write	Remark
A/B_WDGCOMP0	Bit[15..0] (Low Word)	R/W	These 16bit set the limit, where a A/B_MCP interrupt is generated. Default after PowerOn: 0x27B3 = 5s
A/B_WDGCOMP1	Bit[31..16] (High Word)	R/W	These 16bit set the limit where, depending on the A/B_WDGRSTMODE[1:0] bits, a Fast or hard reset is generated Default after PowerOn: 0x2FA3 = 6sec

Table 28: A/B_WDGCOMP0/1

The value of A/B_WDGCOMP0 should be normally lower then A/B_COMP.

Watchdog A/B_WDGDATA Register			Address: Base address + 8204h
Name	Bit	Read/Write	Remark
A/B_WDGDATA +(Service)	Bit[15..0]	R/W	Read: The actual value of the watchdog counter high word can be read. The value can change during read – so the software has to read it multiple times in less than 492µs and check the value for correctness. Write: The watchdog will be serviced (reset), when writing the magic constant 0b0010'1010=42 into the A/B_WDG_DATA register

Table 29: A/B_WDGDATA + Service

Watchdog A Control-Bits located in A_CNTRLSTATregister			Address: Base address + 8008h
Bit	Name	Read/Write	Remark
in A_CNTRLSTAT-Register (see also chapter 3.6.2.5)			
0	A_WDGRSTMODE0[1]	R/W[2]	00 = No reset when Watchdog A expires [1] (but an A_MCP can be generated) 01 = A_WDG generates Fast-Reset A when Watchdog A expires Node B will get an A_WDG_IRQ for information
1	A_WDGRSTMODE1[1]	R/W[2]	10 = A_WDG generates Fast-Reset A and Fast-Reset B [3] 11 = A_WDG generates a hard reset (including reload of FPGA)
in SYS_IN-Register			
26	A_WDG1A_EXP	R/W	=0 after Hardreset, =1 if A_WDG ≥ A_WDGCOMP1 (WDG_A expired → Fast Reset) Only Node A can clear the bit by writing '0'.
27	A_WDG1B_EXP	R/W	=0 after Hardreset, =1 if B_WDG ≥ B_WDGCOMP1 (WDG_B expired → Fast Reset) Only Node A can clear the bit by writing '0'.

Table 30: Watchdog A Control-Bits

Watchdog B Control-Bits located in B_CNTRLSTAT register			Address: Base address + 8008h
Bit	Name	Read/Write	Remark
in B_CNTRLSTAT-Register (see also chapter 3.6.2.5)			
0	B_WDGRSTMODE0[1]	R/W[2]	00 = No reset when Watchdog B expires [1] (but an B_MCP can be generated) 01 = B_WDG generates Fast-Reset B when Watchdog B expires Node A will get an B_WDG_IRQ for information
1	B_WDGRSTMODE1[1]	R/W[2]	10 = B_WDG generates Fast-Reset B and Fast-Reset A [3] 11 = B_WDG generates a hard reset (including reload of FPGA)
in SYS_IN-Register			
28	B_WDG1B_EXP	R/W [3]	=0 after Hardreset =1 if B_WDG ≥ B_WDGCOMP1 (WDG_B expired → Fast Reset) Only Node B can clear the bit by writing '0'.
29	B_WDG1A_EXP	R/W [3]	=0 after Hardreset, =1 if A_WDG ≥ A_WDGCOMP1 (WDG_A expired → Fast Reset) Only Node B can clear the bit by writing '0'.

Table 31: Watchdog B Control-Bits

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Notes: [1] If the A or B_WDG_Off_Jumper is set, A/B_WDGRSTMODE[1:0] is always 00, so Watchdog Reset A/B is off
[2] Write protected by A/B_RWP[7:0]
[3] A/B_WDG1A/B_EXP bits located in SYS_IN register are set when a Fast-Reset A/B occurs.
See also chapter 3.6.2.8.

3.6.2.8 System IO

The System IOs are used for VG5 on board IO. They consist of three registers:

In SYS_IN all onboard Inputs are located. Node A and B can read simultaneously.
In A_SYS_OUT are Node A Outputs. Only Node A can read and write this register.
In B_SYS_OUT are Node B Outputs located. Only Node B can read and write this register.

See detailed register information below.

Register SYS_IN (readable by Node A and B)					Address: Base address + 8100h
	Pin-Name	**Function**	**Bit**	**Register –Bit**	**Default / Remark**
Byte 0 (extern)	GA[4..0]#	VME Geographical Addressing	4..0		Static during PowerOn
	GAP#	VME Geographical Addressing Parity	5		Static during PowerOn
	PMC1_PRESENT#	PMC1 Site populated when Low	6	=0 populated =1 empty	Static during PowerOn
	PMC2_PRESENT#	PMC2 Site populated when pin Low	7	=0 populated =1 empty	Static during PowerOn
Byte 1 (extern)	EREADY	PMC1/2: Processor of PMC ready	8	=0 =1 Ready	
	SIN9_SPARE	Reserve	9	-	
	DUALCPU	High-active Input	10	=0 one CPU =1 dual CPU	Static during PowerOn
	Config[4..0]#	Configuration Pins	15..11	=0 Pull-down R set =1	
Byte 2 (extern)	A_FLASHBUSY#	Low if NodeA Flash Bank 1 or 2 is busy	16	=0 Busy =1 Ready	
	B_FLASHBUSY#	Low if Node B FlashBank 1 or 2 is busy	17	=0 Busy =1 Ready	
	SIN18_SPARE	Reserve	18	-	
	SIN19_SPARE	Reserve	19	-	
	SIN20_SPARE	Reserve	20	-	
	-		21		
	-		22		
	-		23		
Byte 3 (intern)	-		24		
	-		25		
	A_WDG1A_EXP	Bit: read (A/B) write (A) Info for Node A: WDG_A has reached limit of A_WDGCOMP1.	26	=0 after Hardreset, =1 if A_WDG ≥ A_WDGCOMP1	Default 0 Only Node A can clear the bit by writing ‘0’
	A_WDG1B_EXP	Bit: read (A/B) write (A) Info for Node A: WDG_B has reached limit of B_WDGCOMP1.	27	=0 after Hardreset, =1 if B_WDG ≥ B_WDGCOMP1	Default 0 Only Node A can clear the bit by writing ‘0’.
	B_WDG1B_EXP	Bit: read (A/B) write (B) Info for Node B: WDG_B has reached limit of B_WDGCOMP1.	28	=0 after Hardreset, =1 if B_WDG ≥ B_WDGCOMP1	Default 0 Only Node B can clear the bit by writing ‘0’
	B_WDG1A_EXP	Bit: read (A/B) write (B) Info for Node B: WDG_A has reached limit of A_WDGCOMP1.	29	=0 after Hardreset, =1 if A_WDG ≥ A_WDGCOMP1	Default 0 Only Node B can clear the bit by writing ‘0’.
	-		30		
	-		31		

Table 32: SYS_IN Register

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Register: A_SYS_OUT (only readable by Node A)				Address: Base address + 8104h
Pin-Name	**Function**	**Bit**	**Bit Description**	**Default / Remark**
A_WP_SPD	Write-Protect Serial SPD-EEPROM Node A	0	=0 Write Enabled =1 Write Protected	Default: 1 Protected
A_WP_NV	Write-Protect Serial NV-EEPROM Node A	1	=0 Write Enabled =1 Write Protected	Default: 1 Protected
A_LED/BOOTSEL	Output: Open-Drain A_LED: Red Node A LED	2	=0 LED On =1 LED Off	Default: 0 = LED On
	Input: BootSelect: Flashbank1/2		=0 Jumper set =1 Jumper not set	Read: The external pin status will be read, so it can be detected if the A_Bootselect-Jumper is set or not. To be able to detect the external pin status, the Output has to be set to one (LED off)
A_LED_GR#	LED Green, User	3	=1 LED Off =0 LED on	Default: 1 = LED Off
C2_422_DE#	Com2 RS422 Transmitter Data Enable	4	=0 Enabled =1 Disabled	Default: 1 Disabled
C2_422_RE#	Com2 RS422 Receiver Enable	5	=0 Enabled =1 Disabled	Default: 1 Disabled
C2_232_ON#	Com2 RS232 Enable	6	=0 Enabled =1 Disabled	Default: 1 Disabled
ASOUT7_SPARE	Output; Reserve	7	-	-
ASOUT8_SPARE	Output; Reserve	8	-	-
	Only for Single Node Version:			
B_WP_NV	High-active Output; Open-Drain Write-Protect Serial NV-EEPROMS Node B	16	=0 Write Enabled =1 Write Protected	Default: 1 Protected
B_LED #	Low-active Output; Open-Drain B_LED: Red Node B LED	17	=0 LED On =1 LED Off	Default: 1 LED Off

Table 33: A_SYS_OUT Register

Register: B_SYS_OUT (only readable by Node B)				Address: Base address + 8104h
Pin-Name	**Function**	**Bit**	**Bit Description**	**Default / Remark**
B_WP_SPD	Write-Protect Ser. SPD-EEPROM Node B	0	=0 Write Enabled =1 Write Protected	Default: 1 Protected
B_WP_NV	Write-Protect Serial NV-EEPROM Node B	1	=0 Write Enabled =1 Write Protected	Default: 1 Protected
B_LED/BOOTSEL	Output: Open-Drain B_LED: Red Node B LED	2	=0 LED On =1 LED Off	Default: 0 = LED On
	Input: BootSelect: Flashbank1/2		=0 Jumper set =1 Jumper not set	Read: The external pin status will be read, so it can be detected if the B_Bootselect-Jumper is set or not. To be able to detect the external pin status, the Output has to be set to one (LED off)
BSOUT3_SPARE	Output, Reserve	3		

Table 34: B_SYS_OUT Register

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3.6.2.9 User General Purpose IO (UGPIO)

The VG5 provides 32 General Purpose IOs (UGPIO). The UGPIOs are controlled by the FPGA logic. Each of these UGPIO bits is separately programmable by the user as input, output and with rising/falling/any edge sensitive interrupt. All 32 bits are available at rear IO but shared with PMC2 IO signals.

Node A as the Master can configure which UGPIO bits belong to Node A or B.

IO Signal	P2 Connector	IO Signal	P2 Connector
UGPIO00	A17	UGPIO16	C17
UGPIO01	A18	UGPIO17	C18
UGPIO02	A19	UGPIO18	C19
UGPIO03	A20	UGPIO19	C20
UGPIO04	A21	UGPIO20	C21
UGPIO05	A22	UGPIO21	C22
UGPIO06	A23	UGPIO22	C23
UGPIO07	A24	UGPIO23	C24
UGPIO08	A25	UGPIO24	C25
UGPIO09	A26	UGPIO25	C26
UGPIO10	A27	UGPIO26	C27
UGPIO11	A28	UGPIO27	C28
UGPIO12	A29	UGPIO28	C29
UGPIO13	A30	UGPIO29	C30
UGPIO14	A31	UGPIO30	C31
UGPIO15	A32	UGPIO31	C32

Table 35: UGPIO at P2

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3.6.2.9.1 UGPIO Registers

Register	Function
UGPIO_CONFIG Base address + 8600h	Selects for each UGPIO bits (and the belonging bits in other configuration registers), if it is writeable by Node A or Node B. Only Node A (Master) can set this register. 0 = Node A, 1 = Node B PowerON Default: 0xFFFF 0000 Node A: Read/Write Node B: Read only **Write protected** by A_CNTRLSTAT (see Table 25)
UGPIO_MUX Base address + 8518h	Foreseen for future use, if a special function module is included in the FPGA, that shares IOs with the UGPIO function block. This register is shared by between Node A and B, depending of the configuration in the UGPIO_CONFIG register. 0= UGPIO-Function 1= Special function PowerON Default: 0x0000 0000 Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
UGPIO_DIR Base address + 8504h	Selects the direction of a UGPIO bit. Node A or B can select the direction (Input or Output), depending of the settings in UGPIO_CONFIG. The direction for Node A bits can only be set by Node A and also only Node B can set the direction for Node B bits. 0 = Input 1 = Output PowerON Default: 0x0000 0000 Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
UGPIO_IN Base address + 8500h	Input data from 32 UGPIO inputs. Can be read simultaneously by Node A and B. Node A: read only Node B: read only
UGPIO_OUT Base address + 8500h	Shared between Node A and B for data Output. PowerON Default: 0x0000 0000 Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
UGPIO_IRQMASK1 Base address + 8508h UGPIO_IRQMASK2 Base address + 8510h	Configuration of the edge recognition. These registers are shared by between Node A and B, depending of the configuration in the UGPIO_CONFIG register. Two neighbouring bits set the edge recognition mode of the belonging UGPIO_IN bits. 00= IRQ off (default) PowerON Default: 0x0000 0000 01= IRQ on falling Edge 10= IRQ on rising Edge 11= IRQ on Edge (rising or falling) Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
A_IRQEVENT Base address + 8514h	32bit edge detection event register for Node A stores UGPIO_IN edge events, if the belonging UGPIO bit is configured for Node A. A detected event will be stored as '1' in the event register. It can only be cleared by NodeA by writing a '1' onto this bit in the A_IRQEVENT register. Bits that are configured to Node B are always read as 0. Multiple event bits can be set in the A_IRQEVENT register. If minimum one event bit is set, the A_GPIO_IRQ is set active in the A_IRQ-Controller.
B_IRQEVENT Base address + 8514h	32bit edge detection event register for Node B stores UGPIO_IN edge events, if the belonging UGPIO bit is configured for Node B. A detected event will be stored as '1' in the event register. It can only be cleared by NodeB by writing a '1' onto this bit in the B_IRQEVENT register. Bits that are configured to Node A are always read as 0. Multiple event bits can be set in the B_IRQEVENT register. If minimum one event bit is set, the B_GPIO_IRQ is set active in the B_IRQ-Controller.

Table 36: UGPIO Registers

Base address = FPGA base address. Base and size of page is set in the Chipset
see MV64360 Datasheet , DevCS[1]# Base Address (Offset: 0x228). The VxWorks Board Support Package has a system function returning the FPGA base address: fpgaBasePtr.

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3.6.2.9.2 UGPIO – Electrical Specifications

Absolute maximum ratings

Parameter	Condition	min	tip	max
Input clamp current I_{IC}	V_{IH} < 0V			-/+10mA
Input voltage range V_I		-0.5V		4V
Output source or sink current I_O	V_O> -0.5V, V_O < 4.0V			+/-24mA

Remarks: V_i should not exceed V_{CCO}=0V(power) by more than 3.6V over extended periods of time (e.g., longer than a day). Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve.
The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

Operating

Parameter	Condition	min	typ	max
Input voltage high V_{IH}		2.0V		
Input voltage low V_{IL}				0.8V
Input voltage V_I		0 V		3.6V
Input transition rise or fall time				250 ns
Input capacitance C_I			8pF	
Output voltage high V_{OH}	I_{OH} = 8mA	2.4V		
Output voltage low V_{OL}	I_{OL} = 8mA		0.4V	0.5V

Table 37 a-b: UGPIO Electrical Specification

Remark:
- The IO standard used for the UGPIO pins is LVTTL (3,3V) with 8mA cells.
- 5V IOs can be connected to the UGPIO-Pins when using the VG5 transition module VTM20. Take care to use the UGPIO-5V connector on the transition module.

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3.6.2.10 FPGA in single Node VG5 Version

The FPGA in the VG5 single Node configuration is nearly the same as in dual node configuration. The following differences exist:

- Dual Port RAM not included
- Only Node A specific modules included (e.g. no B_IRQ-Controller or B_WDG)
- Node B FlashBank0/1 can be used for Node A. Node A bus is routed completely through FPGA to reach the Node B Flash Banks. So now up to 128MB+128MB Flash Memory are possible in single node configuration. Slight read/write performance impact for the B-Flash Memories has to be taken into account.
- Register Layout compatible to dual node configuration. Some registers have to be initialised for Node A only usage. (e.g. UGPIO_CONFIG=0x00000000 etc)
- A_SYS_OUT Register has inherited some bits of Node B B_SYS_OUT Register.(see Table 33)

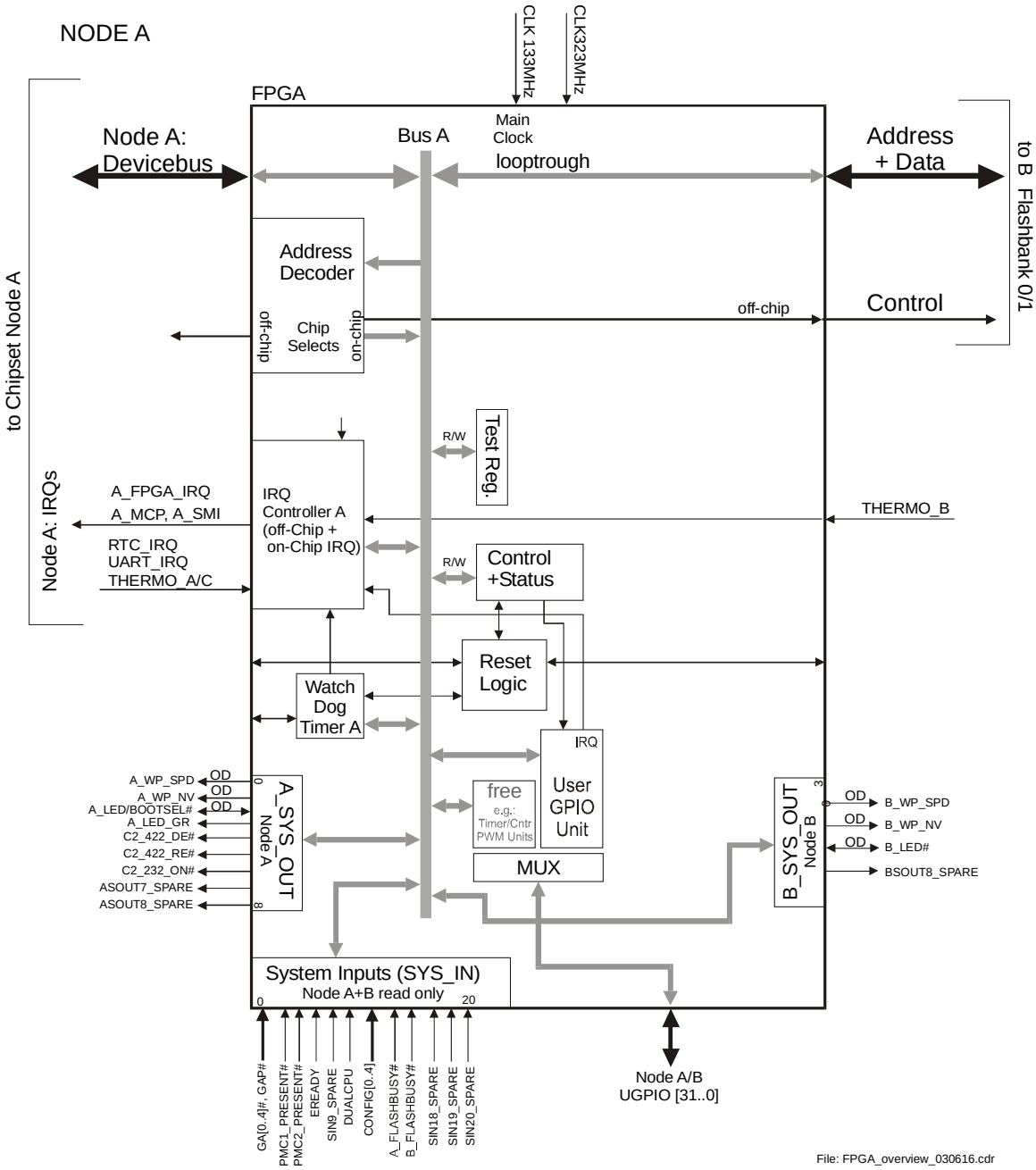


Figure 21: FPGA Block Diagram (Single Node)

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3.6 PCI Buses

The VG5 has in dual Node version three PCI buses. Each chipset provides two 64bit PCI buses, one of each is dedicated to PCI devices like PMC, VME Controller etc, and the other PCI bus interconnects both chipsets to access the resources of the other node respectively to communicate between the two CPUs. Each PCI bus is theoretically 133MHz PCI-X capable, but due to electrical and timing restrictions this is not possible.

Node A:	PCI bus 0 has a maximum of PCI-X 100MHz
Node A/B:	PCI bus maximum PCI-X 100MHz
Node B:	PCI bus 0 PCI 33MHz

In single node version the VG5 has only one chipset with two PCI busses. In this version the interconnection PCI bus will be shortcut with the Node B PCI bus via a device which simply connects the traces of these two buses. The speed of this PCI bus stays at PCI 33MHz.

3.7 Asynchronous Serial Ports COM1, COM4

The VG5 supports two asynchronous serial ports. The serial ports are fully compatible with the NS16450 and NS16550. Address area: offset + 0000h to 0007h. Offset is the programmed value of DevCS2 in the chipset.
The UARTs have programmable baud rate generators capable of 50 to 115200 baud.
The asynchronous ports are COM1 and COM4 and are dedicated for the command terminal of each CPU node. In single node configuration COM4 can be controlled by Node A, too. The address area is offset + 0008h
The signals are buffered through EIA-232-D drivers and receivers and routed to the P2 connector and to the front IO at a SUBD-9pin (P2710) connector. At the rear connector (P2) only the receive and transmit signals are connected, at the front SUBD connector COM1 has additional status signals and COM4 uses pins of this connector for the transmit/receive line. To use two terminals a proprietary split cable is necessary to separate the RS-232 signal of both interfaces. In single node version COM4 is only connected to rear IO and the freed pins at P2710 are used by additional COM1 status signals.

Signal COM1	**P2 connector**
C1_RXD	Z9
C1_TXD	Z11
Signal COM4	**P2 connector**
C4_RXD	Z13
C4_TXD	Z15

Signal	**SUBD 9pin P2710**
C4_RXD/C1_DCD (1	1
C1_RXD	2
C1_TXD	3
C4_TXD/C1_DTR (1	4
GND	5
C1_DSR	6
C1_RTS	7
C1_CTS	8
C1_RI	9

Figure 22 a-b: COM1+4 Pinning at P2 and front connector P2710

Note 1): Either COM4 signals (dual node) or COM1 signals (single node) are connected.

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3.8 Serial Communication Interface COM2, COM3, COM5, COM6

Each of the Marvell MV64360 chipset contains two high performance Multi-Protocol Serial Controllers which support HDLC, BISYNC, UART (sync/async), and Transparent protocols.
On the VG5 theses channels are COM2, COM3 (Node A) and COM5, COM6 (NodeB) with RS-232 up to 115kBaud and/or RS-422/485 driver/receivers up to 12Mbit/s (COM2 limited to 250kbit/s). COM2 is a software selectable RS-232 or RS-422/485 interface, COM3, COM5, and COM6 are RS-422/485 only. The signals of all four serial interfaces are available at rear IO P2 and additionally there is a version with COM2 front IO at P2720 but this will restrict the usage of the second PMC site.

Signal COM2			**P2 connector**	**9-pin SUBD P2720**
RS-232 Signal (max 115kbit)	RS-422/485 sync (max 250kbit)	RS-422/485 async (max 250kbit)		
C2_CTS	C2_ RXC-	C2_CTS-	D5	8
C2_TXD	C2_ RXC+	C2_CTS+	D6	3
C2_RXD	C2_TXC-	C2_RTS-	D7	2
C2_RTS	C2_TXC+	C2_RTS+	D8	7
Not used	C2_RXD-	C2_RXD-	D9	9
C2_DTR	C2_RXD+	C2_RXD+	D10	~~5~~ 4
C2_DCD	C2_TXD-	C2_TXD-	Z1	1
C2_DSR	C2_TXD+	C2_TXD+	Z3	6
GND	GND	GND	-	5

Table 38: COM2 Signals at P2 and front connector P2720

Signal COM3 (max 12MBit)		**P2 Connector**
RS-422/485 sync	RS-422/485 async	
C3_ RXC-	C3_CTS-	D17
C3_ RXC+	C3_CTS+	D18
C3_TXC-	C3_RTS-	D19
C3_TXC+	C3_RTS+	D20
C3_RXD-	C3_RXD-	D15
C3_RXD+	C3_RXD+	D16
C3_TXD-	C3_TXD-	D21
C3_TXD+	C3_TXD+	D22

Table 39: COM3 Signals at P2

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Signal COM5 (max 12MBit)		P2 Connector
RS-422/485 sync	RS-422/485 async	
C5_ RXC-	C5_CTS-	D23
C5_ RXC+	C5_CTS+	D24
C5_TXC-	C5_RTS-	D25
C5_TXC+	C5_RTS+	D26
C5_RXD-	C5_RXD-	D29
C5_RXD+	C5_RXD+	D30
C5_TXD-	C5_TXD-	D27
C5_TXD+	C5_TXD+	D28

Table 40: COM5 Signals at P2

Signal COM6 (max 12MBit)		P2 Connector
RS-422/485 sync	RS-422/485 async	
C6_ RXC-	C6_CTS-	Z21
C6_ RXC+	C6_CTS+	Z23
C6_TXC-	C6_RTS-	Z25
C6_TXC+	C6_RTS+	Z27
C6_RXD-	C6_RXD-	Z17
C6_RXD+	C6_RXD+	Z19
C6_TXD-	C6_TXD-	Z29
C6_TXD+	C6_TXD+	Z31

Table 41: COM6 Signals at P2

3.9 Counter and Timer

There are four 32-bit wide timer/counters in each MV64360 chipset.
So the Dual Node VG5 configuration has 8 timer/counters in total, the Single Node configuration has 4 timer/counters in total.
Each timer/counter can be selected to operate as a timer or as a counter. Each timer/counter increments with every System Clock rising edge (System Clock=100 or 133MHz).
In Counter mode, the counter counts down to terminal count, stops, and issues an interrupt.
In Timer mode, the timer counts down, issues an interrupt on terminal count, reloads itself to the programmed value, and continues to count. Reads from the counter or timer are done from the counter itself, while writes are to its register. This means that read results are in the counter's real time value. See details in the MV64360 datasheet.

Additional to the Counters in the chipset the A/B watchdog counters in the FPGA can be used to generate an A/B_MCP interrupt after a given time. The A/B_WDGRSTMODE bits have to be set to 00 or a reset will occur after the watchdog expired. The time can be set with the A/B_WDGCOMP0 16bit register in steps of 492µs between 492µs and about 32,3s. See details in chapter 3.6.2.7.

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3.10 Real Time Clock

The VG5 has a Real Time Clock (RTC) chip on-board at address offset + 00010h for address index and offset+0020h for data index. Offset is the programmed value of DevCS2 in the chipset.
The RTC provides a 100-year calendar with alarm function, a timer with periodic interrupt and 114 bytes of general purpose SRAM. In power-off state the RTC can be supplied from the VMEbus via the +5VSTDBY (+4.85V to 5,25V) voltage. The maximum battery supply current is 3µA (typ 1µA).

3.11 COP Interface

The COP (Common On-chip Processor) interface of the PowerPC processor provides a serial interface for boundary scan and special interface for debug and control. The VG5 has allows for each CPU node a separate COP interface. Both COP interfaces are connected as follows:
(see Figure 13 and Figure 14 for connector location)

- Access COP A via 16-pin connector P1100 with 1.27mm grid near the front or via optional P1101 with 2.54mm grid in the PMC2 area.
- Access COP B via 16-pin connector P1150 with 1.27mm grid near the front or via optional P1151 with 2.54mm grid in the PMC2 area.
- Both COP interfaces are wired to the P2 connector but shared with PMC2 IO signals

3.12 PMC Interfaces

The VG5 allows the installation of up to two additional PMC modules with user defined IO routed to P0 for PMC1 and P2 for PMC2. Some PMC1 IO signals and all PMC2 IO signals are shared with other signals see section 2.8.5, 2.8.6 for pin assignment.
Both PMCs are 64bit, PMC1 is connected to Node A and has a maximum performance of PCI-X 100MHz. PMC2 belongs to Node B (or in single node it is connected to the second PCI bus of Node A) and has a maximum PCI 33MHz performance.
Both PMC interfaces of the VG5 are +5V/+3.3V signalling tolerant but the PMC1 is keyed for +3.3V VIO and PMC2 is keyed for +5V VIO.

3.12.1 PMC Power Requirements

The VG5 board provides +5V, +3.3V, and +/-12V to the PMC connectors. The +5V and +3.3V is limited by the max possible power consumption of PMC module to 7.5W each. +/-12V is limited by the thickness of the power traces. The VME backplane has to provide +5V, +3.3V and +/-12V.
The maximal current for each voltage is defined in the table below.

Voltage	Max. current for single PMC	Max. current for both PMCs
+5V	1.5A	3A
+3.3V	2.3A	4.6A
+12V	0.5A	0.5A
-12V	0.5A	0.5A

Table 42: PMC Power Requirements

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3.13 Serial ATA

The VG5 has implemented one serial ATA channel to support one serial ATA device and has following features.
• Integrated Serial ATA Link and PHY logic
• Compliant with Serial ATA 1.0 specifications
• Supports Serial ATA Generation 1 transfer rate of 1.5Gb/s.
• Supports Spread Spectrum in receiver
• Programmable drive strengths for Backplane applications

The serial ATA signals are available at P0 and are shared with some of the PMC1 IO signals.

3.14 Ethernet Interfaces

Each of the Marvell Chipsets has two Ethernet MAC controllers, which have Gigabit Ethernet capability. On the VG5 each node implements a Fast Ethernet and Gigabit Ethernet PHY Transceiver. The MAC addresses of the Ethernet ports are stored in the SPD serial EEPROM.

All Ethernet signals are available at the rear IO connector P0 and P2, alternativly both Ethernet ports of Node A are also available at the front IO via RJ45 connectors.

The link status of all 4 Ethernet channel is available at the rear IO of P2, but these signals are shared with PMC2 IOs. At the front RJ-45 connectors each interface has two LEDs to indicate link and speed status.

Eth1	Green LED	Yellow/green LED
	on: Link	yellow: 1000Mbit
	off: no Link	green: 100Mbit
	blink: TX/RX activity	off: 10Mbit or none

Eth2	Green LED	Yellow LED
	on: 10Mbit	on: Link
	off: 100Mbit	off: no Link

3.15 VMEbus Interface

The VG5 provides the UNIVERSE VMEbus interface chip. It contains a complete high performance 64-bit VMEbus interface with 32-bit PCI master/slave capability. Furthermore a system controller is implemented to allow the VG5 to reside in slot 1 without the necessity of an extra system controller. The VME controller is controlled by the Node B PCI-bus (dual node) but may also controlled via the interconnection PCI bus by Node A.

Universe Register
All of the controlling registers are located in the UNIVERSE. The registers are memory mapped and after Power-On the base address is assigned dynamically by the software. 64 KBytes address space is reserved but only the first 4 KBytes are used.

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Universe PCI bus Address Space
By default the VMEbus interface is disabled. In this case the PCI address space reserved for the VMEbus is available. If the VG5 needs to access the VMEbus, the VMEbus logic must be enabled and the PCI address spaces must be defined. Multiple PCI to VMEbus address space mappings with different attributes (A16, A24, D16, D32, User, ...) are possible.

Universe VMEbus Address Space
VMEbus address space may be defined when an other VMEbus master needs to access internal memory. Any location accessible over the PCI bus can be used.

Local Interrupt
UNIVERSE Interrupt line LINT 0 may be assigned by Setup to one free internal interrupt. Interrupt sharing with other PCI devices may be allowed when all interrupt lines support level driven mode (typical for PCI devices) and all interrupt service handler are known of this feature. The other seven interrupt lines LINT 1 .. LINT 7 are not connected.

Features
- Fully compliant, 64-bit, 33 MHz PCI local bus interface
- Fully compliant, high performance 64-bit VMEbus interface
- Integral FIFOs for write posting to maximize bandwidth utilization
- Programmable DMA controller with linked list support
- VMEbus transfer rates of 60MBytes/sec
- Complete suite of VMEbus address and transfer modes
    - A32/A24/A16 master and slave
    - D64 (MBLT)/D32/D16/D8 master and slave
    - BLT, ADOH, RMW, LOCK
- Flexible register set, programmable from both the PCI and VMEbus ports
- Full VMEbus system controller functionality

Programming
For detailed information about programming the UNIVERSE refer to 'VMEbus Interface Components Manual UNIVERSE' available from Tundra Semiconductor Corporation. This manual can be downloaded from the Tundra web site (http://www.tundra.com) in PDF-Format. The web site also contains sample code for the first initialisation.

SBS Technologies also recommends raeding carefully the device errata available on the VG5 utility disk.

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3.16 Two-Wire-Serial-Interface (TWSI) Devices

The VG5 uses two (dual node) or one (single node) Two-Wire-Serial-Interface TWSI to communicate with several onboard devices. The TWSI master is the corresponding chipset of Node A or B.

Device Node A (dual and single node)	TSWI address
Chipset Init 8kByte EEProm	1010 000Xb
SPD and Factory 512Byte EEProm	1010 100Xb
NVRAM User 64kByte EEProm	1010 010Xb
Near CPU A Temperature sensor	1001 111Xb
Mid board Temperature sensor	1001 101Xb
Device Node B (dual node)	**TSWI address**
Chipset Init 8kByte EEProm	1010 000Xb
SPD 512Byte EEProm	1010 100Xb
NVRAM User 64kByte EEProm	1010 010Xb
Near CPU B Temperature sensor	1001 111Xb

Table 43: TWSI Devices Node A and B Addresses

3.16.1 Chipset Init EEPROM

Each chipset has an serial EEPROM of 8kByte for storage of pre-initialisation values for the chipset. These values are read and stored in the appropriate chipset register after reset. Chipset Init and Factory/SPD EEPROM are protected by an output port for unintentional writes.

3.16.2 SPD and Factory EEPROM

For storage of factory SDRAM data a serial EEPROM is implemented on the VG5 board. This 512Byte EPROM stores the data according to the **PC SDRAM Serial Presence Detect (SPD) Specification** and also factory data like MAC addresses, serial number, variants stored into this device. Chipset Init and Factory/SPD EEPROM are protected by an output port for unintentional writes.

3.16.3 NVRAM - User Serial EEPROM

The NVRAM is build with a serial EEPROM and is used for storage of user data. The size is 512kbit (64kByte) at each Node. These devices are protected by an output port against unintentional writes.

3.16.4 Temperature Sensor

Three National Semiconductors LM75 temperature sensor are implemented on the VG5 board. The sensors are located close to the CPUs and one in mid board area and shows the board temperature at this locations. The sensor has an over-temperature output integrated, which can be used to take actions like reducing the CPU power.

See temperature sensor locations in Figure 3:

Thermo A: U1302	near CPU A
Thermo B: U1352	near CPU B (only mounted on dual node boards)
Thermo C: U1303	centre of VG5

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3.17 LED

The VG5 has three LED indicators at the front. The two red LEDs are Card Fail of CPU A and/or B. After reset, the LEDs are turned on by hardware and turned off if the boot loader sequence was performed successfully. (E.g.: The Card Fail LED of CPU A will be on if the boot flash will be corrupt and no boot code could be loaded)
During application these LEDs can be used for any user-defined purpose. Both red LEDs are also available at the rear connector P2 (z5 and z7). The both card fail LEDs are used by the BOOTSEL jumpers too, if a boot selector jumper is closed the LED will always lit.
The third LED is a green LED for user purposes. After reset it is off and can be used by any application.

LED Front	Owner	Pin Name	Register / Bit Name / Bit No.	Remark
CPU A Red	Node A	A_LED/Bootsel	A_SYS_OUT / A_LED / 2	See Table 33 in chapter 3.6.2.8.
CPU B Red	Node B (Dual Node VG5)	B_LED/Bootsel	B_SYS_OUT / B_LED / 2	See Table 34 in chapter 3.6.2.8.
	Node A (Single Node VG5)		A_SYS_OUT / B_LED / 17	See Table 33 in chapter 3.6.2.8.
Green	Node A	A_LED_GR	A_SYS_OUT / A_LED / 3	See Table 33 in chapter 3.6.2.8.

Table 44: LEDs and their registers

3.18 Reset Button

A push button at the front will release a hard reset. The reset signal is active for all subsystems of the VG5. Additionally the reset signal RST_BUT (open collector) at P0-a19 can release a reset from the backplane.

The hard reset can also be released by the reset button on the VTM20 transition module.

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4 Appendix Transition Module VTM20

The VTM20 is a transition module which is used to route IO signals from the VG5 Single Board Computer for interface to external peripherals. The module is a 6U x 80mm rear IO module which has to be plugged into the VG5 slot with the backplane in between. Make sure that your selected chassis supports this type of rear IO transition module. Please notice that many IO signals have alternative functions, so the interface signals are only available if the corresponding interface signals are provided by the VG5 board.
The VTM20 transition module is compliant with IEEE 1101.11-1998.

The +5V and +3,3V power available at connectors are protected by overcurrent circuits.
The +12V and –12V power (if needed by PIM modules) must be protected by the user.

Overview of available connectors on this module :
(depending on the configuration not all connectors may be available).

- Transition Module front panel connectors
  - Three Ethernet RJ45 connectors with LED's for link status
  - Reset button
  - Slot opening for two PMC IO Modules (PIM)

- Transition Module onboard connectors
  - COM1 to COM6 10-pin headers
  - Ethernet 2 10-pin header
  - COP A and COP B Interface 16-pin header
  - PMCIO IO connectors of PMC1 and PMC2 with 64-pin header
  - General Purpose IO +5V tolerant at a 34 pin header
  - Serial ATA connector compliant to SATA specification
  - Miscellaneous 10-pin header
  - JTAG interface at a 10 pin header
  - +12V, -12V and GND terminals for external power supply

The following chapters describe the connectors and interfaces in detail.

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4.1 Placement Plan

VTM20 V0.x

Top Side (BS)

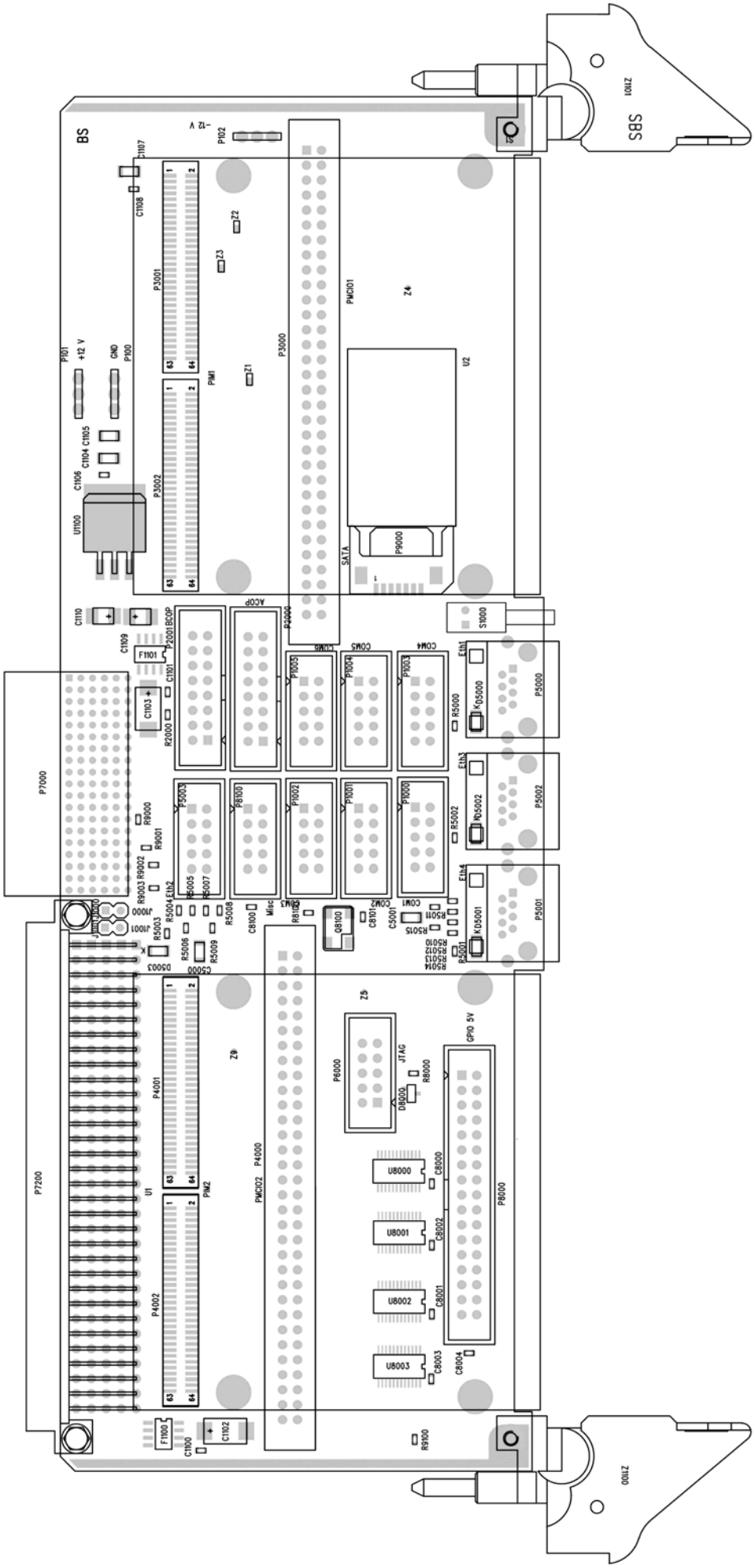


Figure 23: VTM20 placement plan

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4.2 Connectors

4.2.1 Backplane Connectors P0/P2

The transition module can be connected to a VME64 backplane using the user defined pins at P0 and P2.

4.2.1.1 P0 Connector P7000

	a	b		c		d		e		f
1	GND	GND		GND		GND		GND		GND
2	**ETH1_DA+**	**ETH1_DA-**		GND		**ETH1_DC+**		**ETH1_DC-**		GND
3	**ETH1_DB+**	**ETH1_DB-**		GND		**ETH1_DD+**		**ETH1_DD-**		GND
4	**ETH3_DA+**	**ETH3_DA-**		GND		**ETH3_DC+**		**ETH3_DC-**		GND
5	**ETH3_DB+**	**ETH3_DB-**		GND		**ETH3_DD+**		**ETH3_DD-**		GND
6	GND	GND		GND		GND		GND		GND
7	PMC1_IO05	PMC1_IO04		PMC1_IO03		PMC1_IO02		PMC1_IO01		GND
8	PMC1_IO10	PMC1_IO09		PMC1_IO08		PMC1_IO07		PMC1_IO06		GND
9	PMC1_IO15	PMC1_IO14		PMC1_IO13		PMC1_IO12		PMC1_IO11		GND
10	PMC1_IO20	PMC1_IO19		PMC1_IO18		PMC1_IO17		PMC1_IO16		GND
11	PMC1_IO25	PMC1_IO24		PMC1_IO23		PMC1_IO22		PMC1_IO21		GND
12	PMC1_IO30	PMC1_IO29		PMC1_IO28		PMC1_IO27		PMC1_IO26		GND
13	PMC1_IO35	PMC1_IO34		PMC1_IO33		PMC1_IO32		PMC1_IO31		GND
14	PMC1_IO40	PMC1_IO39		PMC1_IO38		PMC1_IO37		PMC1_IO36		GND
15	PMC1_IO45	PMC1_IO44		PMC1_IO43		PMC1_IO42		PMC1_IO41		GND
16	PMC1_IO50	PMC1_IO49		PMC1_IO48		PMC1_IO47		PMC1_IO46		GND
17	PMC1_IO55	P1_IO54	GND	P1_IO53	GND	P1_IO52	GND	P1_IO51	GND	GND
18	PMC1_IO60	P1_IO59	GND	P1_IO58	ATA_TX+	P1_IO57	GND	P1_IO56	ATA_RX-	GND
19	RSTBUT#	P1_IO64	GND	P1_IO63	ATA_TX-	P1_IO62	GND	P1_IO61	ATA_RX+	GND

Table 45: TM P0 Connector P7000

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4.2.1.2 P2 Connector P7200

	z	A PMCIO or VG5 function::		B	c PMCIO or VG5 function:		d user defined
		VG5_Func.	PMC2_IO		VG5_Func.	PMC2_IO	
1	C2_DCD/TXD-	Geth1_LED	PMC2_IO02	+5V	Geth3_LED	PMC2_IO01	Eth2_TxD-
2	GND	Eth2_LED	PMC2_IO04	GND	Eth4_LED	PMC2_IO03	Eth2_TxD+
3	C2_DSR/TXD+	CPUVIO	PMC2_IO06	-	WDG_REL / EXT16.66MHZ	PMC2_IO05	Eth2_RxD-
4	GND	ACOP_HRST#	PMC2_IO08	-	BCOP_HRST#	PMC2_IO07	Eth2_RxD+
5	LED A#/BOOTSEL	ACOP_SRST#	PMC2_IO10	-	BCOP_SRST#	PMC2_IO09	C2_CTS/RXC-/CTS-
6	GND	ACHKSTP_OUT#	PMC2_IO12	-	BCHKSTP_OUT#	PMC2_IO11	C2_TXD/RXC+/CTS+
7	LED B#/BOOTSEL	ACOP_TCK	PMC2_IO14	-	BCOP_TCK / JTAG_TCK	PMC2_IO13	C2_RXD/TXC-/RTS-
8	GND	ACOP_TDI	PMC2_IO16	-	BCOP_TDI / JTAG_TDI	PMC2_IO15	C2_RTS/TXC+/RTS+
9	C1_RxD	ACOP_TMS	PMC2_IO18	-	BCOP_TMS / JTAG_TMS	PMC2_IO17	C2_RXD-
10	GND	ACOP_TRST	PMC2_IO20	-	BCOP_TRST# / JTAG_TRST#	PMC2_IO19	C2_DTR/RXD+
11	C1_TxD	ACOP_TDO	PMC2_IO22	-	BCOP_TDO / JTAG_TDO	PMC2_IO21	Eth4_TxD-
12	GND	AQREQ#	PMC2_IO24	GND	BQREQ#	PMC2_IO23	Eth4_TxD+
13	C4_RxD	AQACK#	PMC2_IO26	+5V	BQACK#	PMC2_IO25	Eth4_RxD-
14	GND	ACHKSTP_IN	PMC2_IO28	-	BCHKSTP_IN#	PMC2_IO27	Eth4_RxD+
15	C4_TxD	-	PMC2_IO30	-	-	PMC2_IO29	C3_RxD-
16	GND	-	PMC2_IO32	-	-	PMC2_IO31	C3_RxD+
17	C6_RxD-	UGPIO0	PMC2_IO34	-	UGPIO16	PMC2_IO33	C3_RXC-/CTS-
18	GND	UGPIO1	PMC2_IO36	-	UGPIO17	PMC2_IO35	C3_RXC+/CTS+
19	C6_RxD+	UGPIO2	PMC2_IO38	-	UGPIO18	PMC2_IO37	C3_TXC-/RTS-
20	GND	UGPIO3	PMC2_IO40	-	UGPIO19	PMC2_IO39	C3_TXC+/RTS+
21	C6_RXC-/CTS-	UGPIO4	PMC2_IO42	-	UGPIO20	PMC2_IO41	C3_TxD-
22	GND	UGPIO5	PMC2_IO44	GND	UGPIO21	PMC2_IO43	C3_TxD+
23	C6_RXC+/CTS+	UGPIO6	PMC2_IO46	-	UGPIO22	PMC2_IO45	C5_RXC-/CTS-
24	GND	UGPIO7	PMC2_IO48	-	UGPIO23	PMC2_IO47	C5_RXC+/CTS+
25	C6_TXC-/RTS-	UGPIO8	PMC2_IO50	-	UGPIO24	PMC2_IO49	C5_TXC-/RTS-
26	GND	UGPIO9	PMC2_IO52	-	UGPIO25	PMC2_IO51	C5_TXC+/RTS+
27	C6_TXC+/RTS+	UGPIO10	PMC2_IO54	-	UGPIO26	PMC2_IO53	C5_TxD-
28	GND	UGPIO11	PMC2_IO56	-	UGPIO27	PMC2_IO55	C5_TxD+
29	C6_TxD-	UGPIO12	PMC2_IO58	-	UGPIO28	PMC2_IO57	C5_RxD-
30	GND	UGPIO13	PMC2_IO60	-	UGPIO29	PMC2_IO59	C5_RxD+
31	C6_TxD+	UGPIO14	PMC2_IO62	GND	UGPIO30	PMC2_IO61	GND
32	GND	UGPIO15	PMC2_IO64	+5V	UGPIO31	PMC2_IO63	+5V (VPC)

Table 46: TM P2 Connector P7000

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4.2.2 Power Supply

The VTM20 is supplied from the backplane with +5V only. This +5V is used to generate +3.3V via an intern linear voltage regulator. If +12V and –12V voltages are necessary these voltage has to be supplied to the transition module via terminals P100, P101, P102.

P100	GND
P101	+12V
P102	-12V

4.2.2.1 Power Supply Electrical Specification

The user must not exceed the current in the Transition Module as listed below.

Voltage	Max Current
+5V	3.0 A
+3.3V	1.0 A
+12V	1.0 A
-12V	1.0 A

Table 47: TM Power Ratings

4.2.3 Card Fail LED and Boot Select Jumper

The VTM20 has two jumper positions J1000 and J1001. The jumpers select the booting source of Node A and B. The boot behaviour depends on the software installed in the boot flash. The boot software is responsible for the evaluation of the BOOTSEL jumper.

Due to limited pins at P0/P2 connector the boot select signals share the function with the card fail LEDs of CPU A and CPU B. If a jumper is closed the program will read and store the status of the boot select function, after this read function the signal will be an output and controls the card fail LEDs. That means if a jumper is closed the LED is in on-state as long the jumper is installed. The LED output is protected against this short cut.
To connect a LED use a 680Ω serial resistor to +3.3V.

J1000 open	**J1000 closed**
Node A will boot from default boot loader. The A_LED (CPU A, red) can be controlled by software	Node A will boot from emergency boot loader. The A_LED (CPU A, red) will be on and can not be controlled by software
J1001 open	**J1001 closed**
Node B will boot from default boot loader. The B_LED (CPU B, red) can be controlled by software	Node B will boot from emergency boot loader. The B_LED (CPU B, red) will be on and can not be controlled by software

Table 48: TM Boot Select jumper

4.2.4 Reset Button

A push button at the front will release a hard reset. The reset button has the same function as the reset button at the VG5 .

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4.2.5 Ethernet Interfaces

The VG5 has a maximum of four Ethernet interfaces. Three of these four interface can be accessed via RJ45 8-pin connectors mounted at the transition module's front panel, the fourth interface via a 10 pin header.

Remark: Eth1 (Node A, 100MBit) and Eth2 (Node A, 1000MBit) on the VTM20 have no function, if the VTM20 transition module is used in conjunction with a VG5 with Eth1 and/or Eth2 as front IO.

VG5 Variant with	VGTM20
no Ethernet	Eth1, Eth2, (Dual Node VG5: Eth3, Eth4) non functional
with Eth1 and Eth2 rear	both functional
with Eth1 front Eth2 rear	Eth2 port is functional
with Eth1 rear Eth2 front	Eth1 port is functional
with Eth1 front Eth2 front	Eth1 and Eth2 port are non functional
with Eth3 and Eth4 rear	Eth3 and Eth4 are only on dual node VG5 available
with PMC2 rear IO	Ethernet LED function for Eth1-4 is not available on VTM20
with no PMC2 rear IO but GPIO, COP and Eth-LEDs	Ethernet LED function for Eth1-4 is available on VTM20

Table 49: VG5 Ethernet Variants

4.2.5.1 Gigabit Ethernet Connectors P5000, P5002

These two Ethernet connectors are Gigabit Ethernet (10/100/1000BaseTX) capable. The Ethernet interface at P5000 correspond to the NodeA and has the number Eth1, the Ethernet interface at P5002 correspond to NodeB and has the number Eth3.

Name	**Ethernet1** P5000 **Ethernet3** P5002
LPx_DA+ (TxD+)	1
LPx_DA- (TxD-)	2
LPx_DB+ (RxD+)	3
LPx_DC+	4
LPx_DC-	5
LPx_DB- (RxD-)	6
LPx_DD+	7
LPx_DD-	8
FGND	Frame Ground

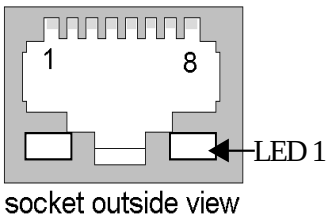


Table 50: TM Gigabit RJ45 Jacks

4.2.5.2 Fast Ethernet Connectors P5001, P5003

These two Ethernet connectors are only Fast Ethernet (10/100BaseTX) capable. The Ethernet interface at P5003 corresponds to the Node A and has the number Eth2, the Ethernet interface at P5003 corresponds to Node B and has the number Eth4. Eth4 at P5001 is a RJ45 connector at the front panel and Eth2 at P5003 is available as a 10 pin header. The unused pin pairs are terminated with a resistor network.

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Ethernet Signals	P5003
E2_TXD+	1
E2_TXD-	2
Term	3
Term	4
E2_RXD+	5
E2_RXD-	6
Term	7
Term	8
-	9
-	10

Table 51: TM Fast Ethernet RJ45 Jack

Name	**Ethernet4** P5002
E4_TxD+	1
E4_TxD-	2
E4_RxD+	3
Term	4
Term	5
E4_RxD-	6
Term	7
Term	8
FGND	Frame Ground

Table 52: TM Fast Ethernet Header

4.2.5.3 Link Status LEDs

Each Ethernet connector has provision for a green Link Status LED. At the front panel the link LEDs are integrated in the RJ45 connectors. The status LED for Eth2 (10 pin header) is located at the Transition Module (D5000).
All four Link status signals are shared with PMC IOs (see connector P2 pin out). Depending on the VG5 variant and the matching VTM20 variant the LEDs are available. The customer has to take care of using the matching VTM20 transition module to his VG5. See table below.

VG5 variant with	matching VTM20 variant with
no PMC2, no PMC2 rear IO, with COM2 front, with COPA/B, GPIO, **Eth-LEDs**	no PIM2, GPIO, partly PMCIO2
PMC2 full rear IO, without COPA/B, GPIO, Eth-LEDs	no PIM2, no GPIO, full PMCIO2 or PIM2, no GPIO, no PMCIO2
PMC2 no rear IO with COPA/B, UGPIO, **Eth-LEDs**	no PIM2, GPIO, partly PMCIO2

Table 53: matching VTM variant for use of Link Status LEDs

Warning: If you use a VG5 with PMC2 rear IO capability and a VTM20 with GPIO/COP functionality I/Os of the VTM20 or the PMC in PMC site 2 may be damaged or PMC-rear IO signals may be disturbed !

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4.2.6 COP Debug and JTAG Interfaces P2000, P2001, P6000

Two 16pin headers P2000 and P2001 provide the COP debug interfaces for the both PowerPC processor of the VG5. The COP A and B signals are shared with the PMC2_IO and JTAG interface. The VG5 variant determines which signal group is valid.

A COP Interface	P2000	Remarks
PMC2_IO22/**ACOP_TDO**	1	
PMC2_IO26/**AQACK#**	2	
PMC2_IO16/**ACOP_TDI**	3	
PMC2_IO20/**ACOP_TRST#**	4	
PMC2_IO24/**AQREQ#**	5	
PMC2_IO06/**CPUVIOSense**	6	220Ω to 2.5V
PMC2_IO14/**ACOP_TCK**	7	
PMC2_IO28/**ACHKSTPIN#**	8	
PMC2_IO18/**ACOP_TMS**	9	
-	10	
PMC2_IO10/**ACOP_SRST**#	11	
GND	12	
PMC2_IO08/**ACOP_HRST#**	13	
Key	14	
PMC2_IO12/**ACHKSTOP #**	15	
GND	16	

Table 54: TM COP A Header

B COP Interface	P2001	Remarks
PMC2_IO21/JTAG_TDO/**BCOP_TDO**	1	
PMC2_IO25/**BQACK#**	2	
PMC2_IO15/JTAG_TDI/**BCOP_TDI**	3	
PMC2_IO19/JTAG_TRST/**BCOP_TRST#**	4	
PMC2_IO23/**BQREQ#**	5	
PMC2_IO06/**CPUVIOSENSE**	6	220Ω to 2.5V
PMC2_IO13/JTAG_TCK/**BCOP_TCK**	7	
PMC2_IO27/**BCHKSTPIN#**	8	
PMC2_IO17/JTAG_TMS/**BCOP_TMS**	9	
-	10	
PMC2_IO09/**BCOP_SRST**#	11	
GND	12	
PMC2_IO07/**BCOP_HRST#**	13	
Key	14	
PMC2_IO11/**BCHKSTOP #**	15	
GND	16	

Table 55: TM COP B Header

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JTAG Interface	P60000
PMC2_IO13/**JTAG_TCK**/BCOP_TCK	1
GND	2
PMC2_IO21/**JTAG_TDO**/BCOP_TDO	3
-	4
PMC2_IO19/**JTAG_TRST**/BCOP_TRST#	5
PMC2_IO17/**JTAG_TMS**/BCOP_TMS	6
-	7
-	8
PMC2_IO15/**JTAG_TDI**/BCOP_TDI	9
GND	10

Table 56: TM JTAG Header

4.2.7 Serial Interfaces COM1...COM6 P100x

The signals of the six (6) serial interfaces are at 10pin headers P1000..P1005 available.

COM1 and COM4 are RS232 only interfaces with solely transmit/receive capability. COM3, COM4 and COM5 are RS422/485 (sync/async) interfaces and additional COM2 can be either RS232 (sync/async) or RS422/485 (sync/async). The function of these interfaces is determined by the VG5.
Some COM interface headers have at pin 10 a +5V voltage (VCC). This power supply is fused by a 2A electronic fuse should not exceed 100mA per interface.

4.2.7.1 COM1 P1000

COM1 is a RS232 interface at P1000.

COM1	P1000	Remarks
-	1	
-	2	
C1_RXD	3	
-	4	
C1_TXD	5	
-	6	
-	7	
-	8	
GND	9	
-	10	

Table 57: TM COM1

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4.2.7.2 COM2 P1001

COM2 is a software selectable RS422/485 (sync/async) or RS232 (async) interface at P1001.

COM2	P1001	RS-232 async	RS-422/485 async	RS-422/485 sync
C2_DCD/TXD-	1	DCD	TXD-	TXD-
C2_DSR/TXD+	2	DSR	TXD+	TXD+
C2_RXD/TXC-/RTS-	3	RXD	RTS-	TXC-
C2_RTS/TXC+ /RTS+	4	RTS	RTS+	TXC+
C2_TXD/RXC+/CTS+	5	TXD	CTS+	RXC+
C2_CTS/RXC-/CTS-	6	CTS	CTS-	RXC-
C2_DTR/RXD+	7	DTR	RXD+	RXD+
C2_RXD-	8	-	RXD-	RXD-
GND	9			
VCC	10	Fused VCC		

Table 58: TM COM2

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4.2.7.3 COM3 P1002

COM3 is a RS422/485 sync/async interface at P1002.

COM3	P1002	RS-422/485 async	RS-422/485 sync
C3_TXD-	1	TXD-	TXD-
C3_TXD+	2	TXD+	TXD+
C3_TXC-/RTS-	3	RTS-	TXC-
C3_TXC+ /RTS+	4	RTS+	TXC+
C3_RXC+/CTS+	5	CTS+	RXC+
C3_RXC-/CTS-	6	CTS-	RXC-
C3_RXD+	7	RXD+	RXD+
C3_RXD-	8	RXD-	RXD-
GND	9		
VCC	10	Fused VCC	

Table 59: TM COM3

4.2.7.4 COM4 P1003

COM4 is a RS232 interface at P1003.

COM4	P1003	Remarks
-	1	
-	2	
C4_RXD	3	
-	4	
C4_TXD	5	
-	6	
-	7	
-	8	
GND	9	
-	10	

Table 60: TM COM4

4.2.7.5 COM5 P1004

COM5 is a RS422/485 sync/async interface at P1004.

COM5	P1004	RS-422/485 async	RS-422/485 sync
C5_TXD-	1	TXD-	TXD-
C5_TXD+	2	TXD+	TXD+
C5_TXC-/RTS-	3	RTS-	TXC-
C5_TXC+ /RTS+	4	RTS+	TXC+
C5_RXC+/CTS+	5	CTS+	RXC+
C5_RXC-/CTS-	6	CTS-	RXC-
C5_RXD+	7	RXD+	RXD+
C5_RXD-	8	RXD-	RXD-
GND	9		
VCC	10	Fused VCC	

Table 61: TM COM5

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4.2.7.6 COM6 P1005

COM6 is a RS422/422 sync/async interface at P1005.

COM6	P1005	RS-422/485 async	RS-422/485 sync
C6_TXD-	1	TXD-	TXD-
C6_TXD+	2	TXD+	TXD+
C6_TXC-/RTS-	3	RTS-	TXC-
C6_TXC+ /RTS+	4	RTS+	TXC+
C6_RXC+/CTS+	5	CTS+	RXC+
C6_RXC-/CTS-	6	CTS-	RXC-
C6_RXD+	7	RXD+	RXD+
C6_RXD-	8	RXD-	RXD-
GND	9		
VCC	10	Fused VCC	

Table 62: TM COM6

4.2.7.7 RS422 / RS485 Termination

There are provisions on the VTM20 transition module's bottom side (LS marked side) to terminate the RS-485 differential inputs RXC/CTS and RXD with 120Ω (1W SMD 2512 size) termination resistors.

Termination Resistor	COM Port , Signal (sync/async)
R7000	C2 , RXC / CTS
R7001	C2 , RXD
R7002	C3 , RXD
R7003	C3 , RXC / CTS
R7004	C5 , RXC / CTS
R7005	C5 , RXD
R7006	C6 , RXD
R7007	C6 , RXC / CTS

Table 63: RS422 / 485 Termination Resistors

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4.2.8 PMC-IO connectors

The PMC IO signals of both PMC slots are either available at 64-pin male headers (P3000/P4000) or via VITA36 compliant PIM (PMC IO Module) connectors (P3001/P3002 and P4001/P4002). The availability of a PIM interface or 64-pin header is mutually exclusive.
The PMC IOs of PMC1 are shared with serial ATA signals so either the PMCIO1 or the SATA function is available at the pins.

4.2.8.1 PMC1-IO connectors P300x

The following table lists the pin assignments of the onboard PIM1 P3002, P3002 connectors.

P3001	P3002	Pin	Pin	P3001	P3002
	PMC1_IO01	**01**	**02**	+12V(3	PMC1_IO02
	PMC1_IO03	**03**	**04**		PMC1_IO04
+5V(1	PMC1_IO05	**05**	**06**		PMC1_IO06
	PMC1_IO07	**07**	**08**		PMC1_IO08
	PMC1_IO09	**09**	**10**	+3.3V(2	PMC1_IO10
	PMC1_IO11	**11**	**12**		PMC1_IO12
GND	PMC1_IO13	**13**	**14**		PMC1_IO14
	PMC1_IO15	**15**	**16**		PMC1_IO16
	PMC1_IO17	**17**	**18**	GND	PMC1_IO18
	PMC1_IO19	**19**	**20**		PMC1_IO20
+5V(1	PMC1_IO21	**21**	**22**		PMC1_IO22
	PMC1_IO23	**23**	**24**		PMC1_IO24
	PMC1_IO25	**25**	**26**	+3.3V(2	PMC1_IO26
	PMC1_IO27	**27**	**28**		PMC1_IO28
GND	PMC1_IO29	**29**	**30**		PMC1_IO30
	PMC1_IO31	**31**	**32**		PMC1_IO32
	PMC1_IO33	**33**	**34**	GND	PMC1_IO34
	PMC1_IO35	**35**	**36**		PMC1_IO36
+5V(1	PMC1_IO37	**37**	**38**		PMC1_IO38
	PMC1_IO39	**39**	**40**		PMC1_IO40
	PMC1_IO41	**41**	**42**	+3.3V(2	PMC1_IO42
	PMC1_IO43	**43**	**44**		PMC1_IO44
GND	PMC1_IO45	**45**	**46**		PMC1_IO46
	PMC1_IO47	**47**	**48**		PMC1_IO48
	PMC1_IO49	**49**	**50**	GND	PMC1_IO50
	PMC1_IO51(4	**51**	**52**		PMC1_IO52(4
+5V(1	PMC1_IO53(4	**53**	**54**		PMC1_IO54(4
	PMC1_IO55	**55**	**56**		PMC1_IO56(4
	PMC1_IO57(4	**57**	**58**	+3.3V(2	PMC1_IO58(4
	PMC1_IO59(4	**59**	**60**		PMC1_IO60
-12V(3	PMC1_IO61(4	**61**	**62**		PMC1_IO62(4
	PMC1_IO63(4	**63**	**64**		PMC1_IO64(4

Table 64: TM PIM1 connector

(1 +5V fused supplied via VG5 max 2A
(2 +3.3V generated from +5V via a linear voltage regulator and fused max 1A
(3 +12V, -12V supplied via the terminal from external power connector P101, P102 max current 500mA each
(4 not available with SATA option

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The following table list the pin-out of the PMC1 IO signals of the 64pin header P3000.

PMC1	P3000		PMC1
PMC1_IO01	1	2	PMC1_IO02
PMC1_IO03	3	4	PMC1_IO04
PMC1_IO05	5	6	PMC1_IO06
PMC1_IO07	7	8	PMC1_IO08
PMC1_IO09	9	10	PMC1_IO10
PMC1_IO11	11	12	PMC1_IO12
PMC1_IO13	13	14	PMC1_IO14
PMC1_IO15	15	16	PMC1_IO16
PMC1_IO17	17	18	PMC1_IO18
PMC1_IO19	19	20	PMC1_IO20
PMC1_IO21	21	22	PMC1_IO22
PMC1_IO23	23	24	PMC1_IO24
PMC1_IO25	25	26	PMC1_IO26
PMC1_IO27	27	28	PMC1_IO28
PMC1_IO29	29	30	PMC1_IO30
PMC1_IO31	31	32	PMC1_IO32
PMC1_IO33	33	34	PMC1_IO34
PMC1_IO35	35	36	PMC1_IO36
PMC1_IO37	37	38	PMC1_IO38
PMC1_IO39	39	40	PMC1_IO40
PMC1_IO41	41	42	PMC1_IO42
PMC1_IO43	43	44	PMC1_IO44
PMC1_IO45	45	46	PMC1_IO46
PMC1_IO47	47	48	PMC1_IO48
PMC1_IO49	49	50	PMC1_IO50
PMC1_IO51(1	51	52	PMC1_IO52(1
PMC1_IO53(1	53	54	PMC1_IO54(1
PMC1_IO55	55	56	PMC1_IO56(1
PMC1_IO57(1	57	58	PMC1_IO58(1
PMC1_IO59(1	59	60	PMC1_IO60
PMC1_IO61(1	61	62	PMC1_IO62(1
PMC1_IO63(1	63	64	PMC1_IO64(1

Table 65: TM PMC1 IO header

(1 not available with SATA option

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4.2.8.2 PMC2-IO connectors P400x

The PMC IO of PMC2 is shared with other signals so either the PMC2-IO or the other function is available at the pins.
The following table lists the pin assignments of the onboard PIM2 P4001/P4002 connector.

P4002	P4002	Pin	Pin	P4001	P4002
	PMC2_IO01/Geth3_LED	**01**	**02**	+12V(3	**PMC2_IO02/**Geth1_LED
	PMC2_IO03/Eth4_LED	**03**	**04**		**PMC2_IO04/**Eth2_LED
+5V(1	**PMC2_IO05/**WDG_REL/EXT16.66MHZ	**05**	**06**		**PMC2_IO06/**CPUVIO
	PMC2_IO07/BCOP_HRST#	**07**	**08**		**PMC2_IO08/**ACOP_HRST#
	PMC2_IO09/BCOP_SRST#	**09**	**10**	+3.3V(2	**PMC2_IO10/**ACOP_SRST#
	PMC2_IO11/BCHKSTP_OUT#	**11**	**12**		**PMC2_IO12/**ACHKSTP_OUT#
GND	**PMC2_IO13/**BCOP_TCK/JTAG_TCK	**13**	**14**		**PMC2_IO14/**ACOP_TCK
	PMC2_IO15/BCOP_TDI/JTAG_TDI	**15**	**16**		**PMC2_IO16/**ACOP_TDI
	PMC2_IO17/BCOP_TMS/JTAG_TMS	**17**	**18**	GND	**PMC2_IO18/**ACOP_TMS
	PMC2_IO19/BCOP_TRST#/JTAG_TRST#	**19**	**20**		**PMC2_IO20/**ACOP_TRST
+5V(1	**PMC2_IO21/**BCOP_TDO/JTAG_TDO	**21**	**22**		**PMC2_IO22/**ACOP_TDO
	PMC2_IO23/BQREQ#	**23**	**24**		**PMC2_IO24/**AQREQ#
	PMC2_IO25/BQACK#	**25**	**26**	+3.3V(2	**PMC2_IO26/**AQACK#
	PMC2_IO27/BCHKSTP_IN#	**27**	**28**		**PMC2_IO28/**ACHKSTP_IN
GND	**PMC2_IO29**	**29**	**30**		**PMC2_IO30**
	PMC2_IO31	**31**	**32**		**PMC2_IO32**
	PMC2_IO33/UGPIO16	**33**	**34**	GND	**PMC2_IO34/**UGPIO0
	PMC2_IO35/UGPIO17	**35**	**36**		**PMC2_IO36/**UGPIO1
+5V(1	**PMC2_IO37/**UGPIO18	**37**	**38**		**PMC2_IO38/**UGPIO2
	PMC2_IO39/UGPIO19	**39**	**40**		**PMC2_IO40/**UGPIO3
	PMC2_IO41/UGPIO20	**41**	**42**	+3.3V(2	**PMC2_IO42/**UGPIO4
	PMC2_IO43/UGPIO21	**43**	**44**		**PMC2_IO44/**UGPIO5
GND	**PMC2_IO45/**UGPIO22	**45**	**46**		**PMC2_IO46/**UGPIO6
	PMC2_IO47/UGPIO23	**47**	**48**		**PMC2_IO48/**UGPIO7
	PMC2_IO49/UGPIO24	**49**	**50**	GND	**PMC2_IO50/**UGPIO8
	PMC2_IO51/UGPIO25	**51**	**52**		**PMC2_IO52/**UGPIO9
+5V(1	**PMC2_IO53/**UGPIO26	**53**	**54**		**PMC2_IO54/**UGPIO10
	PMC2_IO55/UGPIO27	**55**	**56**		**PMC2_IO56/**UGPIO11
	PMC2_IO57/UGPIO28	**57**	**58**	+3.3V(2	**PMC2_IO58/**UGPIO12
	PMC2_IO59/UGPIO29	**59**	**60**		**PMC2_IO60/**UGPIO13
-12V(3	**PMC2_IO61/**UGPIO30	**61**	**62**		**PMC2_IO62/**UGPIO14
	PMC2_IO63/UGPIO31	**63**	**64**		**PMC2_IO64/**UGPIO15

Table 66: TM PIM2 connector

(5 +5V fused supplied via VG5 max 2A
(6 +3.3V generated from +5V via a linear voltage regulator and fused max 1A
(7 +12V, -12V supplied via the terminal from external power connector P101, P102 max current 500mA each

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The following table lists the pin-out of the PMC2IO signals of the 64pin header P4000.

P4000	Pin	Pin	P4000
PMC2_IO01/Geth3_LED	**01**	**02**	**PMC2_IO02/**Geth1_LED
PMC2_IO03/Eth4_LED	**03**	**04**	**PMC2_IO04/**Eth2_LED
PMC2_IO05/WDG_REL/EXT16.66MHZ	**05**	**06**	**PMC2_IO06/**CPUVIO
PMC2_IO07/BCOP_HRST#	**07**	**08**	**PMC2_IO08/**ACOP_HRST#
PMC2_IO09/BCOP_SRST#	**09**	**10**	**PMC2_IO10/**ACOP_SRST#
PMC2_IO11/BCHKSTP_OUT#	**11**	**12**	**PMC2_IO12/**ACHKSTP_OUT#
PMC2_IO13/BCOP_TCK/JTAG_TCK	**13**	**14**	**PMC2_IO14/**ACOP_TCK
PMC2_IO15/BCOP_TDI/JTAG_TDI	**15**	**16**	**PMC2_IO16/**ACOP_TDI
PMC2_IO17/BCOP_TMS/JTAG_TMS	**17**	**18**	**PMC2_IO18/**ACOP_TMS
PMC2_IO19/BCOP_TRST#/JTAG_TRST#	**19**	**20**	**PMC2_IO20/**ACOP_TRST
PMC2_IO21/BCOP_TDO/JTAG_TDO	**21**	**22**	**PMC2_IO22/**ACOP_TDO
PMC2_IO23/BQREQ#	**23**	**24**	**PMC2_IO24/**AQREQ#
PMC2_IO25/BQACK#	**25**	**26**	**PMC2_IO26/**AQACK#
PMC2_IO27/BCHKSTP_IN#	**27**	**28**	**PMC2_IO28/**ACHKSTP_IN
PMC2_IO29	**29**	**30**	**PMC2_IO30**
PMC2_IO31	**31**	**32**	**PMC2_IO32**
PMC2_IO33/UGPIO16	**33**	**34**	**PMC2_IO34/**UGPIO0
PMC2_IO35/UGPIO17	**35**	**36**	**PMC2_IO36/**UGPIO1
PMC2_IO37/UGPIO18	**37**	**38**	**PMC2_IO38/**UGPIO2
PMC2_IO39/UGPIO19	**39**	**40**	**PMC2_IO40/**UGPIO3
PMC2_IO41/UGPIO20	**41**	**42**	**PMC2_IO42/**UGPIO4
PMC2_IO43/UGPIO21	**43**	**44**	**PMC2_IO44/**UGPIO5
PMC2_IO45/UGPIO22	**45**	**46**	**PMC2_IO46/**UGPIO6
PMC2_IO47/UGPIO23	**47**	**48**	**PMC2_IO48/**UGPIO7
PMC2_IO49/UGPIO24	**49**	**50**	**PMC2_IO50/**UGPIO8
PMC2_IO51/UGPIO25	**51**	**52**	**PMC2_IO52/**UGPIO9
PMC2_IO53/UGPIO26	**53**	**54**	**PMC2_IO54/**UGPIO10
PMC2_IO55/UGPIO27	**55**	**56**	**PMC2_IO56/**UGPIO11
PMC2_IO57/UGPIO28	**57**	**58**	**PMC2_IO58/**UGPIO12
PMC2_IO59/UGPIO29	**59**	**60**	**PMC2_IO60/**UGPIO13
PMC2_IO61/UGPIO30	**61**	**62**	**PMC2_IO62/**UGPIO14
PMC2_IO63/UGPIO31	**63**	**64**	**PMC2_IO64/**UGPIO15

Table 67: TM PMC2 IO header

4.2.9 Miscellaneous Connector P8100

A 10pin header P8100 provides miscellaneous interface signals.

	P8100		
A_LED#/BOOTSEL#	1	2	B_LED#/BOOTSEL#
PMC2_IO29	3	4	PMC2_IO30
PMC2_IO31	5	6	PMC2_IO32
RST_BUT#	7	8	WDG_REL/EXT16.66/PMC2_IO05
Fused VCC3	9	10	GND

Table 68: TM Misc Connector

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4.2.10 Serial ATA Connector P9000

The VTM20 provides one serial ATA complaint connector to support one SATA hard disk drive. The SATA signal are shared with PMC1IO signals, therefore this interface can only be used if the VG5 has the SATA option.

P9000	Pin
GND	1
ATA_TX+/PMC1_IO58	2
ATA_TX-/PMC1_IO63	3
GND	4
ATA_RX-/PMC1_IO56	5
ATA_RX+/PMC1_IO61	6
GND	7

Table 69: TM Serial ATA connector

4.2.11 User General Purpose IO +5V P8000

At this connector the 32 User General Purpose IO (UGPIO) signals are available. The normal GPIO signals are available (shared with PMC2-IO) at connector P4000, but at this stage the GPIO is not 5V tolerant (max 3,3V).
Between P4000 and P8000 are bi-directional voltage level converters inserted for 5V tolerant signals at P8000 connector.

Name	P8000		Name
UGPIO00	1	2	UGPIO01
UGPIO02	3	4	UGPIO03
UGPIO04	5	6	UGPIO05
UGPIO06	7	8	UGPIO07
UGPIO08	9	10	UGPIO09
UGPIO10	11	12	UGPIO11
UGPIO12	13	14	UGPIO13
UGPIO14	15	16	UGPIO15
UGPIO16	17	18	UGPIO17
UGPIO18	19	20	UGPIO19
UGPIO20	21	22	UGPIO21
UGPIO22	23	24	UGPIO23
UGPIO24	25	26	UGPIO25
UGPIO26	27	28	UGPIO27
UGPIO28	29	30	UGPIO29
UGPIO30	31	32	UGPIO31
GND	33	34	Fuse VCC

Table 70: TM UPGIO 5V header

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- Product & Serial Number
- Part Number
- Version
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- Detailed Description of the Problem/Defect

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SBS Technologies GmbH & Co.KG	Company Name
Memminger Str. 14	Department
86159 Augsburg	Contact Person
	Mailing Address
Phone Number **+49 821 5034-170**	Phone Number
Fax Number **+49 821 5034-119**	Fax Number
	Email Address

Part. N. **VG5**_____ Version _ . _ Date __ __ __ Serial N. _____

Error Description:
Hardware Environment:
Operating System/Software:
Warranty repair: ❑ YES ❑ NO (Please see section 'Warranty')

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2400 Louisiana Blvd. NE, Suite 5-600	Department
Albuquerque, NM 87110	Contact Person
	Mailing Address
Phone Number **+1 505 875 0600**	Phone Number
Fax Number **+1 505 875 0400**	Fax Number
	Email Address

Part. N. **VG5**_____ Version _ . _ Date __ __ __ Serial N. _____

Error Description:

Hardware Environment:

Operating System/Software:

Warranty repair: ❑ YES ❑ NO (Please see section 'Warranty')

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