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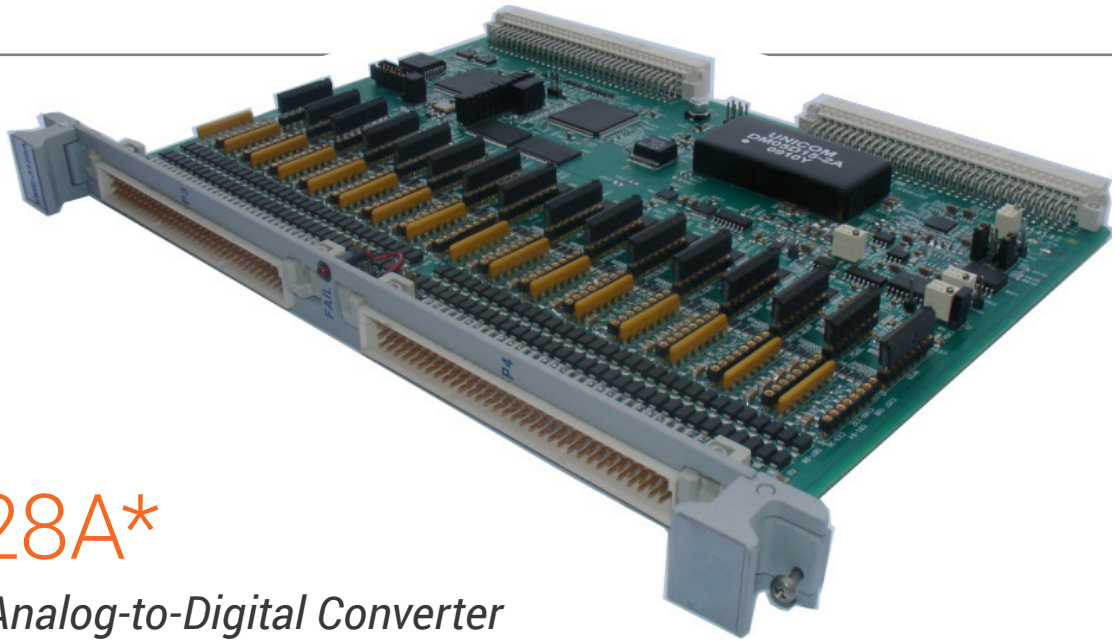
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VME-3128A*

Scanning 14-bit Analog-to-Digital Converter Board with Programmable Gain Memory

Features:

- 64 differential or single-ended inputs
- 14-bit A/D conversion
- 58 kHz conversion rate
- Program-selectable scanning of 16, 32, 48, or 64 channels
- Continually digitizes all input channels & stores the results
- Six operating modes
- Auto scanning mode
- Single channel random polling mode
- Timed burst mode
- Locally triggered burst mode
- Remotely triggered burst mode
- Gain loading mode
- Programmed VMEbus interrupts
- User-programmable interval timer
- Software-programmable gain 1, 10, 100
- External trigger to synchronize multiple boards simultaneously
- Jumper-selectable A/D ranges of 0 to +5, 0 to +10, ±2.5, ±5, and ±10 V
- Optional low pass filter
- Over voltage protected inputs
- 1,024-word data buffer (16-word deep buffer x 64 channels)
- Selectable output coding
- Powers up in auto-scanning mode with gain of 1

Applications

- Factory automation and instrumentation
- Process control and monitoring
- Laboratory instrumentation
- Machine monitoring
- Data acquisition and control

abaco SYSTEMS

VME-3128A* *Scanning 14-bit Analog-to-Digital Converter Board with Programmable Gain Memory*

Ordering Options							
May 12, 2010 800-9310003128-000 A		A	B	C	D	E	F
VME-3128A	–				0		

A = Input filter Options
0 = No filter*
1 = 10 Hz Filter ±24% (-3dB)
2 = 50 Hz Filter ±24% (-3dB)
3 = 100 Hz Filter ±24% (-3dB)
4 = 500 Hz Filter ±24% (-3dB)
B = Input Buffer Option
0 = with input buffers
1 = without input buffers
C = Input Type Option
0 = 64 Diff/SE analog input channels with 96 pin connector
1 = 64 SE analog input channels with 96 pin connector
2 = Reserved
D = Reserved for Future use
E = Over voltage protection
0 = No over voltage protection
1= with over voltage protection
F = Conformal Coating Option
0 = without conformal coating
2 = with conformal coating

Connector Data		
Style	Recommended Connecting Component	P3 and P4 I/O Connectors
64-pin IDC	Mating Connector (64-pin) Strain Relief (for 64-pin Connector)	Panduit 120-964-435E Panduit 100-000-032
96 pin Discrete Wire	Mating Connector (96-pin Discreet) Female Crimp Contacts (96-pin Discreet)	AMP 925486-1 AMP 530151-6**
	Connector Housing (for 96-pin Connectors)	Harting 0903 096 0501
96-pin IDC	Mating Connector (96-pin Mass Terminated)	ERNI 913.031
	0.033-inch Ribbon Cable (96-pin Mass Terminated)	ERNI 913.049
	Strain Relief Insert (0.033-inch Ribbon Cable)	Harting 09020009912
	Connector Housing (for 96-pin Connectors)	Harting 09030960501
PC Board I/O Connector Part Number		Panduit 101-096-033A

Notes

*Bandwidth limited at 300kHz
** AMP crimp tool part number 90301-2

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
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Intorduction

Overview: The VME-3128A* is a member of Abaco Systems extensive family of analog input/output products for the VMEbus. This product is designed to support 64 channels of differential or single-ended wide range (±25 mV to ±10 V) analog inputs.

The VME-3128A supports the following operating modes:

- Autoscanning
- Single Channel Random Polling
- Timed Burst
- Locally Triggered Burst
- Remotely Triggered Burst
- Gain Loading

One thousand and twenty-four dual-port Data Registers provide storage for continuous scanning of all channels. The scanning modes are executed automatically at power up, system reset, or are entered under program control. The dual-port registers allow VMEbus access at any time to read the latest stored data.

Channel gain can be jumper selected as x1, x10, or x100, or can be software programmed individually for each channel. Scan rate is fixed at 58 kCPS (thousand channels). Low pass input filters are available.

A functional block diagram is provided in Figure 1, and the Ordering Options are provided in this specification.

The VME-3128A employs a buffered 64-channel input multiplexer (*unbuffered option also available).

Functional Characteristics

(Typical at +25° C and rated power supplies, unless otherwise stated.)

Operating Modes:

Autoscanning Mode: This default operating mode is selected by a reset operation, or by clearing both CSR Mode control bits. All active channels are scanned continuously in this mode, and any channel value can be read at any time.

Single Channel Random Polling Mode: Each input channel is accessed individually, and the digitized channel value is read from the Converter Data Register (CDR).

Timed Burst Mode: A single data burst (scan of all buffer locations) is acquired at the end of a programmed interval, or the process can be repetitive.

Locally Triggered Burst: A single burst is initiated through the Control and Status Register (CSR).

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Remotely Triggered Burst: A single data burst (scan of all enabled channels) is initiated through the P2 connector by an external TTL trigger source.

Gain Loading Mode: If the board is jumper configured for automatic gain control, gain loading is performed by first selecting the gain loading mode, and by then loading the gain code for each channel into a 64-location gain buffer. The gain codes (0 for x1, 1 for x10, 2 for x100) for all channels are initialized to zero (gain = x1) automatically after a reset operation.

Channel Autogain: The unique gain code for each channel is loaded from the VMEbus into a gain buffer (see Gain Loading Mode). The assigned code is retrieved from the buffer in real-time for each channel acquisition.

Synchronization: A single scan or burst, can be initiated by an external TTL trigger through the P2 connector (Remotely Triggered Burst), or locally through the CSR (Locally Triggered Burst). Either event generates a P2 trigger output, which can be used to synchronize up to 15 boards.

Board Address: Jumper located on word boundary anywhere in the short I/O A16 space, or the standard A24 space. Required word boundary is 1000h in either space.

VMEbus Access: Response to address modifiers is jumper-selectable as:

Short I/O A16 or standard A24 address space
Supervisory or user privilege, or both
Data or program access

VMEbus Compliance: This product complies with VMEbus Specification ANSI/IEEE STD 1014-1987 IEC 821 and 297 with the following mnemonics:

A24/A16:D16/D8 (EO) DTB Slave
Interrupter I(1 to 7) ROAK (DYN)
Interrupter Vector: D08 (O) (DYN)
6U form factor

VMEbus Interrupt: An interrupt request can be generated at the end of a buffer scan in all modes except auto-scanning mode. Response vectors are controlled through Interrupt Vector Registers.

Data Ready Flag: A data ready flag in the CSR is set when the data buffer is filled (endscan) or half-filled (midscan).

Interval Timer: a programmable interval timer provides bursts intervals of up to 536 s.

Reset Operations: Board reset occurs in response to a system reset or by setting a reset bit in the CSR. For programming-free initial operation, a reset operation automatically establishes the following default conditions:

Auto-scanning mode
64-channel block size
64-channel data buffer
Channel Gain = x1

PGA: Channel gains of x1, x10, and x100 are selected through a Programmable Gain Amplifier (PGA). PGA gain can be jumper configured with a single gain for all channels, or it can be controlled in real-time with unique gains assigned for each channel. See Channel Autogain.

Panel Indicator: Program-controlled front panel LED is energized during reset, and is extinguished through the CSR.

Board Identification: A Board Identification Register (BIR) contains the VME-3128A identification code.

Input Characteristics

Number of Input Channels: There are 64 differential or single-ended channels.

Full-Scale Ranges: ±2.5, ±5, ±10, 0 to +5, 0 to +10 V; jumper-selectable

Channel Gain: Program selected or jumper selected as x1, x10, or x100. See Channel Autogain.

Full-Scale Input Range: ±25 mV to ±10 V

Input Impedance: 5 M Ω in parallel with 10 nF (DC measurement)

Input Bias Current: 96nA maximum with zero input

RMS Input Noise (mV): 0.7

Input Filters: Optional low pass single-pole filters

-3 dB at 10 Hz ±24%
-3 dB at 50 Hz ±24%
-3 dB at 100 Hz ±24%
-3 dB at 500 Hz ±24%

Over voltage Protection: ±35V maximum*
* à One channel at a time

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Transfer Characteristics

Resolution: 14 bits

Input Sampling: Sequential, starting at channel 00

Conversion Cycle Time*: 17µs, total time for acquisition, A/D conversion, and storage

A/D Conversion Rate: 58 KSPS (thousand samples per second)

Channel Sample Rate (Maximum): 3.625 KSPS (58 KSPS ÷ number of channels in scanning block, 16 channels minimum)

Inter channel crosstalk (DC to 1 kHz):

	Max Crosstalk (dB)	Max Crosstalk (dB)	Max Crosstalk (dB)
	Adjacent channels	Alternate Channels	All Victim Channel
No Filter	69	69	69
10Hz	66	69	69
50Hz	66	69	69
100Hz	66	69	69
500Hz	66	69	69

Timed Burst Interval: 305µs to 536 s

Common-Mode Voltage (Maximum):
CMV ±9 V: maximum input voltage = ±11 on either input line for linear operation

Common-Mode Rejection: CMRR = 66 dB, DC to 100 Hz, 64-channel block size.

Data Coding: Program selectable as two's complement, or straight/offset binary. 14-bit data is left justified in a 16-bit data word[1].

Accuracy

System Accuracy (% of FSR) (Including Linearity Error):

Gain	Buffer	With out Buffer
x1	0.025	0.012
x10	0.100	0.025
X100	0.950	0.200

Based on average of 1024 samples

Stability (Over Temperature): System Accuracy Drift:

Gain	Drift (ppm/degC)
x1	26
x10	26
x100	26

Data Buffer Memory

Buffer Size: 16 to 1,024 contiguous 16-bit data words, in six equal ratios of 2:1; program controlled.

Block Size: 16, 32, 48, or 64 channels; program controlled.

VMEBus Access: D8 or D16

Availability: Accessible at any time from the VMEbus. Buffer and block sizes are controlled through a Buffer Control Register (BCR).

Physical/Environmental Specifications

Dimensions: 6U (4HP) single slot Eurocard form factor
Height: 9.2 in. (233.25mm)
Depth: 6.3 in. (160mm)
Thickness: 0.8 in. (20.3mm)

Temperature:
Operating: 0° C, to 55° C
Storage: -40° to +85° C

Humidity: 10-80% RH, non condensing

Input Connectors (P3, P4): 96-pin DIN connector, center row grounded (accepts 64- and 96-pin mating connectors).

Power Requirements: 4A Maximum at +5 VDC

MTBF: Contact factory.

Trademarks

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1 Each channel is sampled during the A/D conversion of the preceding channel

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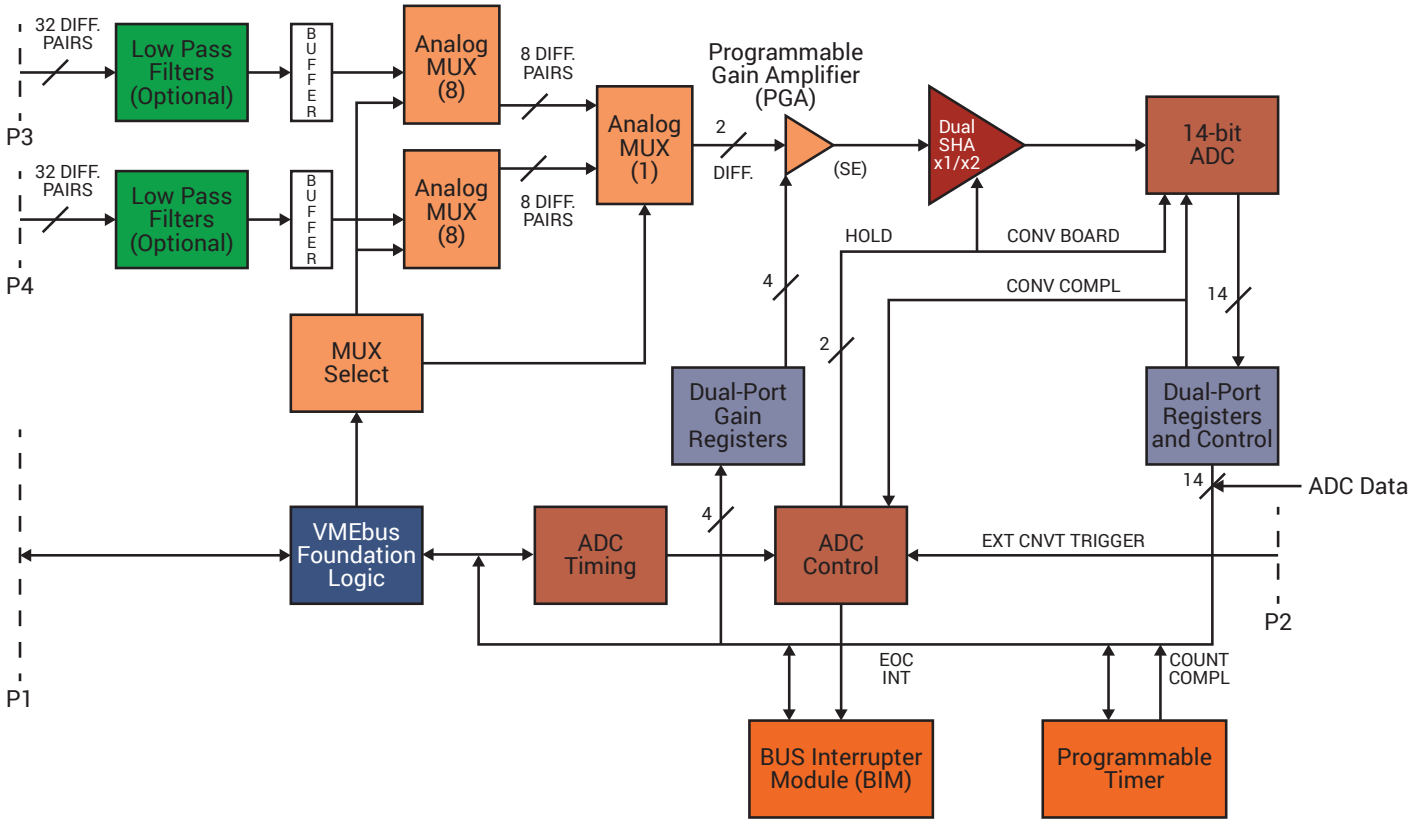


Figure 1. VME-3128A Functional Block Diagram

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