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Hardware Reference Manual

VME-3128A* Scanning 14-bit Analog-to-Digital Converter Board with Programmable Gain

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abaco SYSTEMS

Document History

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About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

$$\text{One dozen} = 12_D = 0x0C = 1100_b$$

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when “k”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.


NOTE
When describing transfer rates, “k”, “M” and “G” mean $x10^3$, $x10^6$ and $x10^9$ *not* $x2^{10}$, $x2^{20}$ and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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For a detailed explanation of the VMEbus and its characteristics, refer to "The VMEbus Specification" available from:

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Additional Notes

The VME-3128A* board is a member of the Abaco extensive family of analog input/output products for the VMEbus. With 14-bit digitizing resolution, program-controlled gain, and automatic scanning of 64 differential or single-ended analog inputs, the VME-3128A board provides exceptional dynamic range and analog input channel density. Various operating modes are supported, including continuous scanning, data bursts, external synchronization, and single channel operation. This board is designed to interface directly with the Abaco line of signal conditioning boards for digitizing the outputs from thermocouples, RTDs, and strain gages.

Individual channel gains are downloaded for selection in real-time during scanning operations, or the board can be configured with a fixed gain that is common to all channels. Multiple boards can be synchronized together to enable as many as sixteen boards to initiate each scan simultaneously. An interval timer, bus interrupter, channel counter, and midscan/endscan flag simplify the monitoring of data within the dual-port data buffer. The broad range of system applications that can benefit from the VME-3128A capabilities include factory automation, process control, data acquisition systems, training simulators, and laboratory instrumentation. The following brief overview of principal features illustrates the flexibility and performance that is available with the VME-3128A board.

Features

- 64 differential or single-ended analog inputs
- 14-bit A/D conversion
- 58 kHz scanning rate
- Program-selectable gains of x1, x10, or x100
- A/D Converter ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, and 0 to +10 V
- Real-time automatic selection of individual channel gains
- 16- to 1,024-word dual-port data buffer
- Operation in short I/O (A16) or standard (A24) data space
- Program-controlled channel block size and buffer size
- Optional low pass input filters
- Continuous, burst, and single channel operating modes
- Free running operation or external/internal triggering
- Bus interrupter for midscan or endscan indication
- Program-controlled interval timer for timed data bursts
- Direct cabling from Abaco signal conditioning boards
- Initializes after a reset in autoscan mode with gain = x1

Functional Description

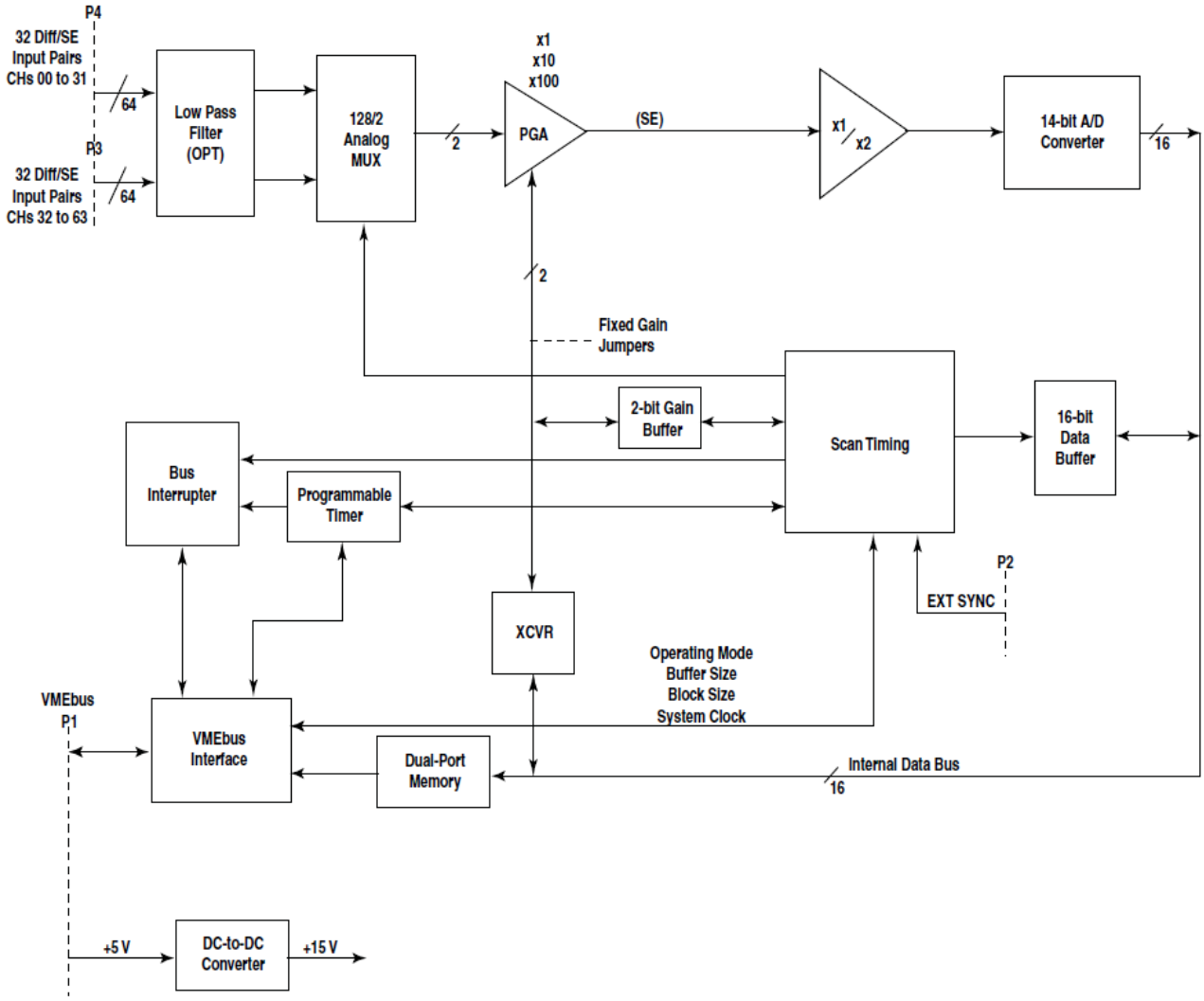
The VME-3128A (***Figure 1, VME-3128A Functional Block Diagram***) is a high-resolution, 14-bit, 64-channel analog scanning and digitizing input board for VMEbus system applications. Dual-ported data memory, onboard timers, automatically controlled gain, and a program-controlled bus interrupter enable the VME-3128A board to support extensive analog input traffic with minimum involvement of the host processor.

Analog inputs are scanned and digitized sequentially in blocks of 16 to 64 channels, and the digital values are stored in a dual-port data buffer which can be accessed at any time from the VMEbus. The gain of each channel can be program-controlled individually in real-time from an on-board gain buffer, or can be jumper-configured for a fixed gain that is common to all channels. Channel gain is software or jumper-selectable as x1, x10, or x100. A/D Converter voltage ranges are jumper-selectable from ±2.5 V, ±5 V, ±10 V, 0 to 5 V, and 0 to 10 V.

When a system or program reset occurs, the board initializes in the 64-channel continuous scanning mode, and if automatic gain control has been selected, all channel gains are initialized to unity (x1). After a reset operation, the program can select the timed burst, triggered burst or random access single channel modes, and can modify the block size, buffer size, and channel gains as necessary. The channel block is adjustable as 16, 32, 48, or 64 channels, and the data buffer size can be selected from 16 to 1,024 data words in six equal ratios of 2:1.

Timed data bursts are controlled by an interval timer which can provide repetitive or single-shot burst intervals of up to 536 s. A burst can consist of from 16- to 1,024-channel samples. A data ready flag is available at the middle or end of a scan, and an interrupt request can be generated simultaneously with the flag. The interrupt can also be initiated after a specific number of samples have been acquired.

Figure 1VME-3128A Functional Block Diagram



Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

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1 • Handling and Installation

1.1 Introduction

This chapter explains how to unpack, install and remove the VME-3128A.

1.2 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Systems Customer Care.

1.3 Handling Precaution

Electronic assemblies use devices that are sensitive to static discharge. Observe anti-static procedures when handling these boards. All products should be in an anti-static plastic bag or conductive foam for storage or shipment. Work at an approved anti-static workstation when unpacking boards.

1.4 Physical Installation



CAUTION

Do not install or remove the boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

1.4.1 Before Applying Power: Checklist

Before applying power to the VMEbus chassis in which the board is installed, use the following checklist to ensure that the board has been correctly prepared for operation.

1. Verify that the sections referring to programming and configuration, ***Chapter 3, Programming*** and ***Chapter 1, Handling and Installation***, have been reviewed and applied to system requirements._____
2. Review ***Section 1.5, Operational Configuration*** on page 14 and ***Table 1-1, Programmable Jumper Functions*** on page 16 to verify that all jumpers are configured correctly for the application._____
3. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to ***Appendix A, Connectors and Pinouts***. _____
4. Physical installation should have been completed as described above. _____
5. Ensure that all system cable connections are correct._____

1.5 Operational Configuration

VMEbus access modes and analog input configurations are controlled by field replaceable jumpers. This section describes the use of these jumpers, and their effects on the board's performance. Locations and functions of all VME-3128A jumpers are shown in ***Figure 1-1, VME-3128A Location of User-Configurable Jumpers*** on page 15 and ***Table 1-1, Programmable Jumper Functions*** on page 16. Typical jumper configurations are summarized in ***Table 1-2, Typical Jumper Configurations*** on page 17.

1.5.1 Factory-Installed Jumpers

Each VME-3128A board is configured at the factory with the specific jumper arrangement shown in ***Table 1-1, Programmable Jumper Functions*** on page 16. The factory configuration establishes the following functional baseline for the VME-3128A board, and ensures that all essential jumpers are installed.

- Board Identification is located at *$0000* in the short I/O space, with either *supervisory* or *nonprivileged* access
- Automatic gain control (Per channel gain selection under software control)
- ±10 V range
- Differential inputs
- External trigger I/O is enabled
- Input COMM bus is connected to analog return (AGND)
- LOW inputs for channels 31 and 63 are disconnected from COMM and AGND

Figure 1-1 VME-3128A Location of User-Configurable Jumpers

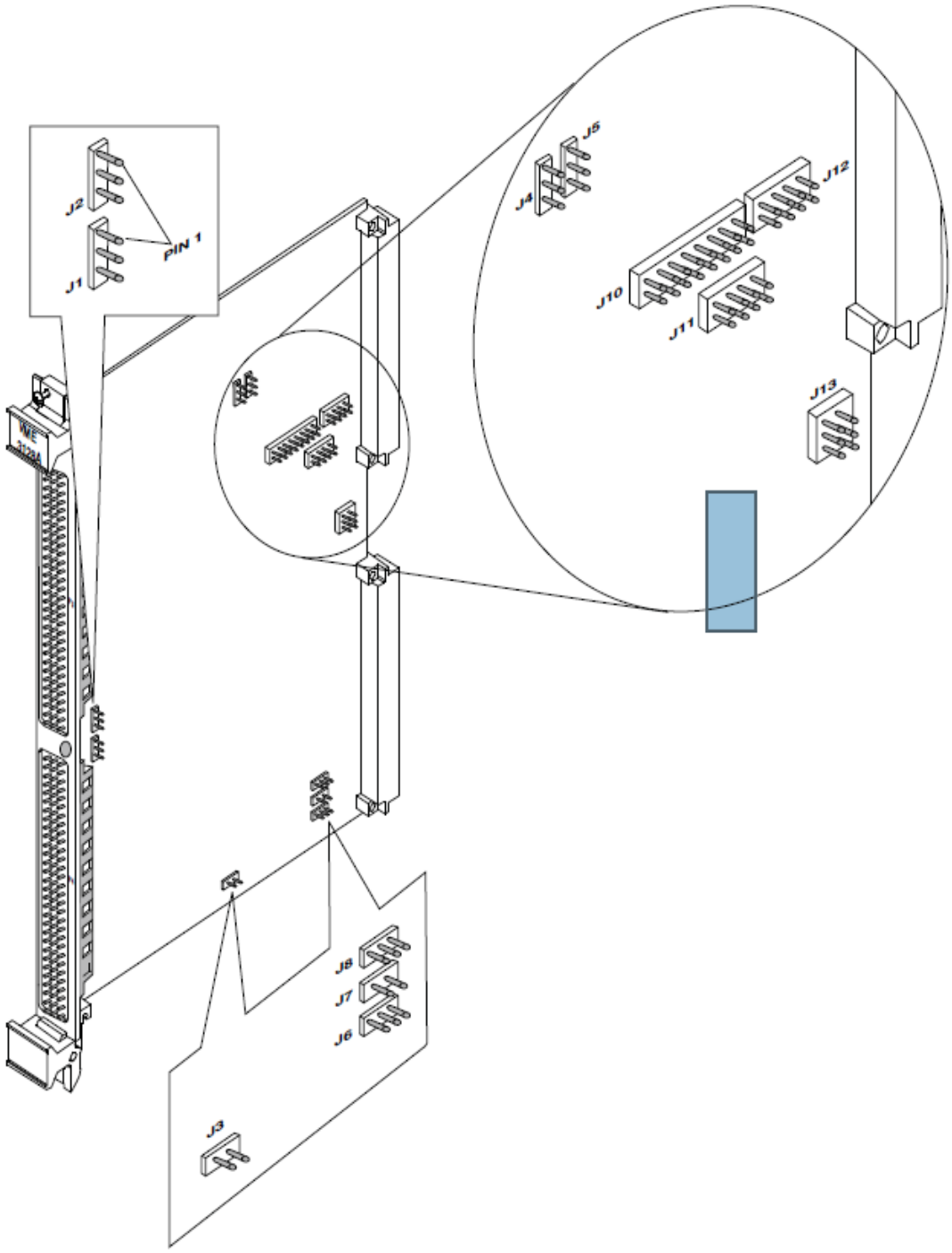


Table 1-1 Programmable Jumper Functions

Jumper IDENT	Function (Installed)	Fact CONFIG
J11-1,2	Short I/O Operation	Installed
J11-3,4	Supervisory (Privileged) Access	Installed
J11-5,6	User (Nonprivileged) Access	Installed
J11-7,8	Data Access	Installed
J12-1,2	Address Bit A12 = 0	Installed
J12-3,4	Address Bit A13 = 0	Installed
J12-5,6	Address Bit A14 = 0	Installed
J12-7,8	Address Bit A15 = 0	Installed
J10-1,2	Address Bit A16 = 0	Installed
J10-3,4	Address Bit A17 = 0	Installed
J10-5,6	Address Bit A18 = 0	Installed
J10-7,8	Address Bit A19 = 0	Installed
J10-9,10	Address Bit A20 = 0	Installed
J10-11,12	Address Bit A21 = 0	Installed
J10-13,14	Address Bit A22 = 0	Installed
J10-15,16	Address Bit A23 = 0	Installed
J4-1,2	Gain Bit A1 = 1 (Jumper selection all channels)	Removed*
J4-2,3	Gain Bit A1 = 0 (SW selection per channel)	Installed
J5-1,2	Gain Bit A0 = 1 (Jumper selection all channels)	Removed
J5-2,3	Gain Bit A0 = 0 (SW selection per channel)	Installed
J6-1,2	Bipolar Analog Inputs	Installed
J6-2,3	Unipolar Analog Inputs	Removed
J7	±2.5 V or 0 to +5 V Ranges	Removed
J8-1,2	±10 V Range	Installed
J8-2,3	±2.5 V, 0 to +5 V, ±5 V, 0 to +10 V Ranges	Removed
J13-1,2	External Trigger Enabled	Installed
J13-3,4	External Trigger Enabled	Installed
J13-5,6	External Trigger Enabled	Installed
J3	Input COMM Grounded to AGND	Installed
J1-1,2	Ch 31 LOW Input Conn to AGND	Removed
J1-2,3	Ch 31 LOW Input Conn to COMM	Removed
J2-1,2	Ch 63 LOW Input Conn to AGND	Removed
J2-2,3	Ch 63 LOW Input Conn to COMM	Removed



NOTE

*See Input Gain in ***Table 1-3, Input Gain*** on page 17 and ***Section 3.3.5, Gain Selection*** on page 40 and ***Section 3.3.6, Gain Initialization Preload*** on page 40 for details.

1.5.2 Example of Jumper J10 through J12 Configuration

- Standard Memory Access;
- Supervisory Only;
- Data Space
- Address $00D1 F000

Table 1-2 Typical Jumper Configurations

Jumper	State	Position*
J11-1,2	STD MEMORY	Removed
J11-3,4	SPVSR	Installed
J11-5,6	USER	Removed
J11-7,8	DATA	Installed
J12-1,2	A12=1	Removed
J12-3,4	A13=1	Removed
J12-5,6	A14=1	Removed
J12-7,8	A15=1	Removed
J10-1,2	A16=1	Removed
J10-3,4	A17=0	Installed
J10-5,6	A18=0	Installed
J10-7,8	A19=0	Installed
J10-9,10	A20=1	Removed
J10-11,12	A21=0	Installed
J10-13,14	A22=1	Removed
J10-15,16	A23=1	Removed

Table 1-3 Input Gain

Input Gain				
Jumper	x1	x10	x100	Auto (SW Selection)
J4	1,2	1,2	REM	2,3 (Default)
J5	1,2	REM	1,2	2,3 (Default)



NOTE

Auto (SW Selection) defaults to x1 gain for all channels after power-up or system reset

Table 1-4 ADC Voltage Range

ADC Voltage Range*					
Jumper	±10 V	±5 V	±2.5 V	0 TO +10 V	0 TO +5 V
J6	1,2	1,2	1,2	2,3	2,3
J7	REM	REM	INS	REM	INS
J8	1,2	2,3	2,3	2,3	2,3

Table 1-5 External Trigger

External Trigger *		
Jumper	Enabled	Disabled
J13 (All)	INS	REM
* "INS" = Jumper installed, "REM" = Jumper removed.		

1.5.3 Access Modes

Supervisory (privileged) access is selected by installing J11-3,4, and user (nonprivileged) access is selected by installing J11-5,6. Installing both J11-3,4 and J11-5,6 selects either supervisory or user access. J11 also permits memory operation in the A24 memory space to be designated for either *data access* (J11-7, 8 installed) or *program access* (J11-7,8 removed).



NOTE

To be consistent with conventional VMEbus development system nomenclature, hexadecimal numbers in this document are designated a "$" prefix unless otherwise indicated. Decimal numbers are presented without a prefix.

1.5.4 Board Location in Short I/O or Memory Space

Jumper J11 selects operation in either the short I/O A16 space with J11-1, 2 installed, or in the standard A24 memory space with J11-1,2 removed (see ***Section 3.2, General Control Features*** on page 33). Jumper blocks J10 and J12 locate the board on any 4,096-word boundary in the A16 or A24 space.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit positions in jumper blocks J10 and J12, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A12 is the least significant address bit that can be jumper-selected, and has a weight of 4,096 words.

1.5.5 Analog Input Gain

Jumpers J4 and J5 control the analog input gain, as shown in ***Table 1-3, Input Gain*** on page 17. Jumper-selected gains of x1, x10, and x100 are fixed and apply to all input channels. The AUTO gain configuration places the gain of each input channel under software control (see ***Section 3.3, Data Organization and Control*** on page 38).

1.5.6 Converter Voltage Range

The A/D Converter voltage range is controlled by jumpers J6, J7, and J8 as shown in ***Table 1-4, ADC Voltage Range*** on page 17.

1.5.7 Input Voltage Range

The input voltage range (full-scale voltage at the input of each channel) is determined by both the analog input gain and the A/D Converter voltage range:

INPUT VOLTAGE RANGE = CONVERTER VOLTAGE RANGE ÷ INPUT GAIN

For example, an input gain of x10 combined with a converter voltage range of ±5 V produces an input voltage range of ±500 mV (±0.5 V).

1.5.8 External Triggering

The selection of either internal or external triggering of single scan is under software control. Jumper block J13 connects the trigger signals at the P2 connector to the internal control logic, and usually is configured with all jumpers installed as shown in ***Table 1-1, Programmable Jumper Functions*** on page 16. If the application does not require external triggering, all J13 jumpers can be removed. If external triggering has been selected through software, and if all J13 jumpers are installed, a data scan begins at the HIGH to LOW transition of the EXT STRT L input at P2.

1.5.9 Input Configurations

The analog inputs can be configured as single-ended, differential or pseudo-differential channels, as shown in ***Table 1-6, Input Configuration Selection*** on page 20. The configurations are selected in groups of four consecutive channels by the positions of jumpers J1, J2, and J3, and by the locations of SIP (single-in-line-package) resistor networks.

In pseudo-differential operation, the LOW input for channels 31 or 63 acts as the external return. Input configurations can be mixed in groups of four channels with no restriction except that the pseudo-differential operation of any group commits either channels 31 or 63 also as single-ended.

Table 1-6 Input Configuration Selection

Input Configuration (Note 1)									
P4 Channel Group	Single-Ended			Differential			Pseudo-Diff		
	SIP POS (Note 2)	Jumpers		SIP POS (Note 2)	Jumpers		SIP POS (Note 2)	Jumpers	
		J1	J2		J1	J2		J1	J2
00 to 03	RP33	1,2	---	RP1	---	---	RP33	2,3	---
04 to 07	RP34	1,2	---	RP3	---	---	RP34	2,3	---
08 to 11	RP35	1,2	---	RP5	---	---	RP35	2,3	---
12 to 15	RP36	1,2	---	RP7	---	---	RP36	2,3	---
16 to 19	RP37	1,2	---	RP9	---	---	RP37	2,3	---
20 to 23	RP38	1,2	---	RP11	---	---	RP38	2,3	---
24 to 27	RP39	1,2	---	RP13	---	---	RP39	2,3	---
28 to 31	RP40	1,2	---	RP15	REM	---	RP40	2,3	---
	CH 31 is Single-End						Return is CH 31 Low		

Input Configuration (Note 1)									
P3 Channel Group	Single-Ended			Differential			Pseudo-Diff		
	SIP POS (Note 2)	Jumpers		SIP POS (Note 2)	Jumpers		SIP POS (Note 2)	Jumpers	
		J1	J2		J1	J2		J1	J2
32 to 35	RP41	---	1,2	RP17	---	---	RP41	---	2,3
36 to 39	RP42	---	1,2	RP19	---	---	RP42	---	2,3
40 to 43	RP43	---	1,2	RP21	---	---	RP43	---	2,3
44 to 47	RP44	---	1,2	RP23	---	---	RP44	---	2,3
48 to 51	RP45	---	1,2	RP25	---	---	RP45	---	2,3
52 to 55	RP46	---	1,2	RP27	---	---	RP46	---	2,3
56 to 59	RP47	---	1,2	RP29	---	---	RP47	---	2,3
60 to 63	RP48	---	1,2	RP31	---	REM	RP48	---	2,3
	CH 63 is Single-End						Return is CH 63 Low		

NOTES:
1. Jumper positions are indicated as: 1,2 Shorting plug between pins 1 and 2.
2,3 Shorting plug between pins 2 and 3.
REM Shorting plug removed.
--- "Don't care;" shorting plug can be installed or removed.
2. "SIP POS" = "Single-in-line-package position" The indicated position is one of two possible locations for the input SIP. Only one of the two locations is occupied. For example, the SIP for channel groups 00 to 03 can be located as either RP33 or RP1.

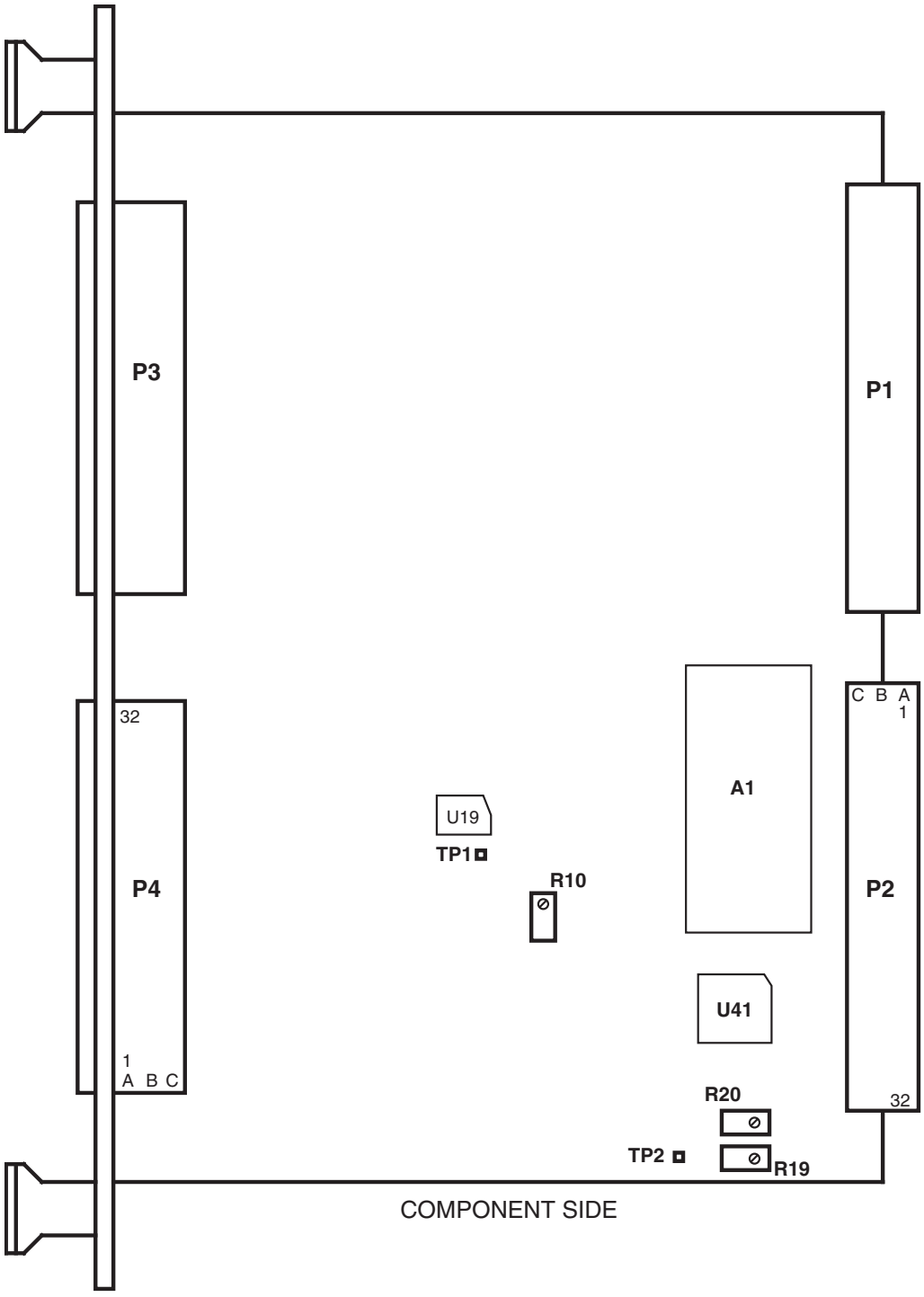
1.5.10 Internal Ground Connections

All pins in the center "B" rows of both input connectors P3 and P4 are connected together as the COMM return, and provide a ground path and interchannel guards between differential input pairs when 96-wire 0.033-inch ribbon cables are used. The COMM return can be connected to the internal analog ground (AGND) by installing jumper J3.

1.6 Calibration

Before delivery from the factory, the VME-3128A board is fully calibrated and conforms to all specifications listed in the default range ±10V. Should recalibration be required, refer to ***Section 1.6.1, Equipment Required*** on page 22 and the ***Section 1.6.2, Calibration Procedure*** on page 22, perform the indicated procedures in the order shown. The locations of test points and adjustments are shown in ***Figure 1-2, Locations of Test Points and Adjustments*** on page 21.

Figure 1-2 Locations of Test Points and Adjustments



1.6.1 Equipment Required

1. Digital Voltmeter (DVM) - 1.000 and 10.000 VDC ranges; 5 or more digits; ±0.003 percent of reading measurement accuracy; 10MΩ minimum input impedance.
2. Digital Voltage Source - 10.000 VDC ±0.001 VDC voltage source; ±0.003 percent setting resolution and accuracy. 10Ω maximum source resistance.
3. Chassis - VMEbus backplane or equivalent, with J1 connector, 68000 Series master controller, +5 ±0.1 VDC, 7 A (reserve current) power supply. One slot allocated for testing the VME-3128A board.
4. Extender Board - VMEbus extender board
5. Software utility capable of reading and writing VME bus data. This utility should be able to display all ADC channel data with an update rate of approximately one second. The capability to average the channel data will be helpful for configurations using gains of x10 or x100.



CAUTION

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

1.6.2 Calibration Procedure

1. Restore all program jumpers to the factory configuration, as shown in ***Table 1-1, Programmable Jumper Functions*** on page 16.
2. Install the VME-3128A board in such a way that jumpers (on an extender board) and trimpots are easily accessible in the VMEbus chassis
3. Apply power to the chassis backplane. Allow a minimum warm-up interval of ten minutes before proceeding
4. Connect the digital voltage source to the channel 00 and channel 01 input pins or to all channels
5. Connect the digital voltmeter between TP1 (+) and TP2 (-).
6. Adjust the voltage source output to 0.0000 VDC.
7. Write the following data to the indicated board relative addresses:

Table 1-7 Relative Addresses

Address	Data	Register	Mode
$0002	$C000	CSR	Reset
$0002	$8,040	CSR	Random Access mode, multiplexer discharged

8. Set Gain to x1. Set J4 1, 2 and J5 1, 2.
9. Adjust potentiometer R19 for a digital voltmeter indication of 0.0000 VDC ±0.0003 VDC.
10. Set the Gain to x100. Set J5 1, 2 and J4 removed
11. Adjust potentiometer R10 for a digital voltmeter indication of 0.0000 VDC ±0.0003 VDC.
12. Set jumpers J4, 5, 6, 7, and 8 for the required input gain and range configuration to be calibrated. See ***Table 1-3, Input Gain*** on page 17 and ***Table 1-4, ADC Voltage Range*** on page 17.
13. Remove the DMM from TP1, TP2

14. Set the Voltage source for the "Zero" voltage setting shown in ***Table 1-8, Range X1*** on page 23 for X1 Gain, ***Table 1-9, Range X10*** on page 23 for X10 Gain, or ***Table 1-10, Range X100*** on page 23 for X100 Gain. Note that for unipolar ranges, this setting is actually half of full scale instead of zero.
15. For calibration using x1 gains without channel data averaging and using a basic vmebus read and write utility, set the autoscan mode by repeating step 7 writing 0x8000 instead of 0x8040. For x10 and x100 gains it may be necessary to average several readings. See Note below.

Table 1-8 Range X1

Hex	Setting	±10V	±5V	±2.5V	0-10V	0 to 5V
FF80	+FSR	9.960938	4.980469	2.490234	9.980469	4.990234
8000	Zero	0.000000	0.000000	0.000000	5.000000	2.5000000
0080	-FSR	-9.960938	-4.980469	-2.490234	0.019531	0.009766

Table 1-9 Range X10

Hex	Setting	±1.0V	±500mV	±250mV	0-1.0V	0 to 500mV
FF80	+FSR	0.996094	0.498047	0.249023	0.998047	0.499023
8000	Zero	0.000000	0.000000	0.000000	0.500000	0.250000
0080	-FSR	-0.996094	-0.498047	-0.249023	0.001953	0.000977

Table 1-10 Range X100

Hex	Setting	±100mV	±50mV	±25mV	0-100mV	0 to 50mV
FF80	+FSR	0.099609	0.049805	0.024902	0.099805	0.049902
8000	Zero	0.000000	0.000000	0.000000	0.050000	0.025000
0080	-FSR	-0.099609	-0.049805	-0.024902	0.000195	0.000098

16. Adjust R19 to get ADC readings of 0x8000 (±4 LSB) in bipolar range and 0x0080 (±4 LSB) in unipolar range
17. Set the +FSR voltage (given in table) in the voltage source
18. Adjust R20 to get ADC readings of 0xFF80 (±4 LSB)
19. Repeat steps 14 to 19 until both the readings are correct
20. Set the -FSR voltage (given in table) in the voltage source
21. Verify that the reading is 0x0080



NOTE

The readings may fluctuate at higher gains. In such cases take more ADC readings, average them and use it to adjust the pots for the desired value. In case of fluctuations in the ADC reading trim the pot such that fluctuations are equal on both sides of desired reading.

1.6.3 Functional Verification

This procedure tests the programmable gain amplifier (PGA), and verifies the integrity of all input channels. Steps 1 through 5 are identical to steps 1 through 5 in the ***Section 1.6.2, Calibration Procedure*** on page 22, and can be omitted if the calibration procedure has been performed within the previous hour, and if power has not been removed from the board.

1. Restore all program jumpers to the factory configuration, as shown in ***Table 1-1, Programmable Jumper Functions*** on page 16.
2. Locate the board at an address that is compatible with the VME operating system. Install jumpers J4-1,2 and J5-1,2 to select minimum PGA gain (x1).
3. Install the VME-3128A on an extender board in the VMEbus chassis.
4. Apply power to the chassis backplane. Allow a minimum warmup interval of ten minutes before proceeding.
5. Connect the digital voltage source to the channel 00 input pins P4-A1 (+) and P4-C1 (-). Adjust the voltage source output to 0.0000 VDC.
6. Write the following data to the indicated relative addresses of the board.

Table 1-11 P4 Relative Addresses

Address	Data	Register	Mode
$0002	$C000	CSR	Reset
$0002	$8000	CSR	Continuous scanning

7. Read and display board word location $0080 (input channel 00) repetitively, at 3 to 5 readings/s.
8. Verify that jumper J4 is removed and that J5-1,2 is installed to select a gain of x100. Adjust the voltage source output to +99.219 mVDC, and verify that the displayed value is between $FED0 and $FF30.
9. Remove the J5 jumper. Install jumper J4-1,2 to select a gain of x10.
10. Adjust the voltage source output to +992.19 mVDC, and verify that the displayed value is between $FED0 and $FF30.
11. Install jumper J5-1,2 to select a gain of x1. Verify that J4-1,2 is installed.
12. Adjust the voltage source output to +9.9219 VDC, and verify that the displayed value is between $FEFC and $FF04.
13. Refer to the P3 and P4 connector descriptions in ***Table A-1, Input/Output Connector Pin Assignments*** on page 52 to determine the input pairs used in the remainder of this procedure.
14. Move the digital voltage source test leads to the channel 01 input pins. Connect the positive test lead to the A row pin, and the negative test lead to the C row pin.
15. Change the address of the displayed data to $0082 (input channel 01). Verify that the displayed value is between $FEFC and $FF04.
16. Repeat steps *14* and *15* for the remaining channels 02 through 63. Increase the displayed address by $0002 for each successive channel, to a maximum address of $00FE for channel 63.
17. Functional verification is completed. Remove power from the board. Remove all test connections. Restore the board to the factory configuration, as shown in ***Table 1-1, Programmable Jumper Functions*** on page 16.

1.7 System Considerations

1.7.1 Applications with Signal Conditioning Boards

The VME-3128A board serves as a multiplexer/digitizer for low level input signal conditioning boards.

When used with signal conditioning boards, the VME-3128A is configured with either differential or pseudo-differential inputs, and with a low-input gain of x1 or x10. These applications should utilize the appropriate input filter option.

1.7.2 Operation with Direct Analog Inputs

When used without signal conditioning input boards, the VME-3128A board provides direct full-scale input ranges from ±25 mV to ±10 V. The optimum input filter for these applications is the 50 Hz filter, although the 10 Hz filter will provide improved attenuation of power line frequency interference at the expense of decreased common-mode rejection. To minimize the effects of direct input multiplexing (in unbuffered boards), the source impedance of analog inputs should not exceed 1,500Ω for the ±10 V input range, or 10Ω for the ±25 mV range. Use the lowest input gain and the largest block size (see ***Section 3.3.3, Data Block*** on page 38) that are practical for the application.

If inputs are obtained directly from remote sources, the grounding scheme used can have a major effect on system performance. Each system has its own unique interference considerations, but the following general guidelines will apply in most cases.

1. Long Input Lines: Long input lines (greater than 10 feet), or inputs from grounded sources (sources which are not floating), should be connected to ***differential inputs***, and overall shields should be extended from the input sources to as close to the board as possible. ***Single-ended inputs*** are susceptible to ground loop errors, and should be used only with high-level floating sources.
2. Source Impedance: Use signal sources with the lowest available source impedances. Susceptibility to crosstalk and induced interference increases as the source impedance increases.
3. Floating Signal Sources: The shield from a floating signal source (RTD, strain gage, etc.) should be connected to the LOW (negative) terminal at the source. For low impedance sources (less than 10Ω), or for sources which are protected from interference fields, connect the board end of the shield to analog return (AGND) at the board. For high impedance sources, connect all shield terminals of the sources together, and leave the board ends of the shields open.
4. Grounded Signal Sources: Outputs of grounded sources (sources which are not floating) must be referenced to a common ground which ensures that the input voltage will not exceed the input range (± 10 V) of the board. Shields from grounded sources should be connected to the LOW terminal of the sources, and left open at the board.
5. Unused Inputs: Unused inputs within each group of eight channels (0 through 7, 8 through 15, etc.) should be connected to a common ground to avoid interference with active channels. Grounding of unused 8-channel groups is not essential, but will assist in minimizing susceptibility to system noise.

2 • Theory of Operation

The following sections describe the internal organization of the VME-3128A board, and review the general principles of operation. Internal Functional Organization summarizes the major board functions, and the remainder of this chapter addresses each function individually. The information in this section is supplemented by programming details in ***Chapter 3, Programming***.

2.1 Internal Functional Organization

The VME-3128A board contains the following principal hardware functions, as shown in ***Figure 1, VME-3128A Functional Block Diagram*** on page 7:

- Analog input multiplexing and digitizing
- VMEbus interface
- Scan timing and control
- Data and gain buffers
- Interval timer and channel counter
- Bus interrupter
- Power converter

An analog multiplexer, a programmable amplifier, and a 14-bit A/D Converter digitize the analog input channels, and the digitized values are stored in a dual-ported data buffer for access from the VMEbus. Low pass input filters minimize the effects of system noise and eliminate high frequency signal components which would otherwise cause aliasing problems. The conversion rate is constant at 17µs for all operating modes except the single scan random access mode (***Section 2.4, Operating Modes*** on page 29). Operating modes are described in detail in ***Chapter 3, Programming***. Regulated ±15 VDC power for the analog networks is obtained from the 5 VDC bus through a DC-to-DC Converter.

A separate gain buffer permits the input gain of each channel to be assigned individually. Gain codes ($0 = x1, $1 = x10, $2 = x100) are first loaded into the gain buffer from the bus, and the gain for each channel is then used during the scanning process. Programmable fixed gain jumpers provide a fixed gain for all channels if software programmable gain is not required.

Control signals and data transfers take place through the VMEbus P1 connector. VMEbus interface logic controls data transfers through the P1 interface, and latches the operating mode parameters. Status monitoring and sequence timing are supported by a bus interrupter and programmable timer, both of which are controlled from the bus. Scan timing logic controls the analog input scanning process, uses the gain buffer to adjust input gain, and routes digitized channel data to the data buffer.

2.2 Control Interface

2.2.1 Board Selection

VMEbus data transfer requests are accepted when the board-selection comparator detects a match between the onboard selection jumpers shown in ***Figure 2-1, VMEbus Interface Logic*** on page 28, and the address and address modifier lines from the backplane. When a match is detected, the board responds with a data transfer, after which the open-collector DTACK interface signal is asserted (LOW). DTACK returns to the negated (HIGH) state when the transfer has been completed. During an interrupt response, DTACK is provided by the interrupt controller.

2.2.2 Read/Write Operations

Data Bus lines D00 through D15 are bidirectional and move data to or from the board through a 16-bit data transceiver in response to control signals from interface timing and control logic. The data transceiver isolates the VMEbus data lines from the internal data bus. Address lines A12 through A23 map the board into either the short I/O A16 space or the standard A24 space. Data transfer control signals from the VMEbus determine whether data is moved to the board (Write) or from the board (Read). Both D8 (EO) and D16 transfers are supported.

The Control and Status Register (CSR) establishes the operational mode of the board and selects the input channel during random access A/D conversions. The Buffer Control Register (BCR) controls the size of the data buffer and the number (block) of channels being scanned.

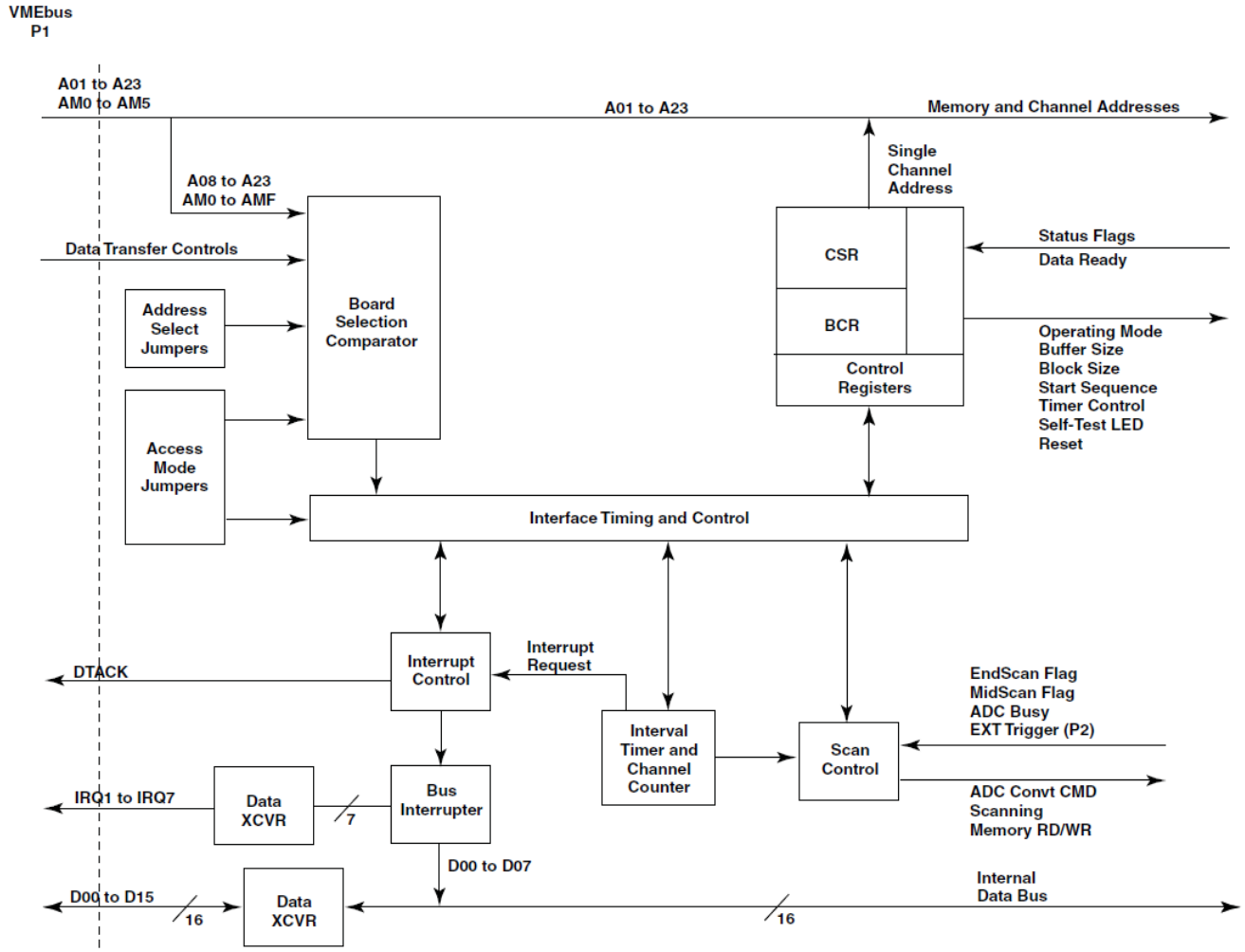
2.2.3 Bus Interrupter

Access to the VMEbus interrupt structure is provided through a bus interrupter. If the interrupt is enabled, an interrupt is generated in response to a request either by the scan timing logic as a data ready flag, or by the channel counter after a specific number of buffer locations have been updated. The interrupt function is implemented with the Bus Interrupter Module (BIM). Details of the interrupter capabilities are described in ***Chapter 3, Programming***.

2.2.4 Interval Timer and Channel Counter

A triple 16-bit counter device contains the interval timer and channel counter. Two of the counter sections are driven from an 8 MHz clock, and can be cascaded as a 32-bit timer for delays up to 536 s. Timed data acquisition bursts (***Section 2.5, Analog Input Multiplexing, Sampling and Digitizing*** on page 30 and ***Section 2.4, Operating Modes*** on page 29) occur periodically at the interval programmed into the interval timer. The channel counter can be programmed to generate an interrupt after a programmed number of data buffer locations have been updated, or can be read directly to serve as a data pointer.

Figure 2-1 VMEbus Interface Logic



2.3 Data Buffer Memory

2.3.1 Organization and Control

Digitized inputs are stored in a 16-bit data buffer, the size of which can be software configured from 16 data words to 1,024 data words. Data in the buffer is organized into consecutive channel blocks, each of which represents a complete scan of all active channels. Both buffer size and block size are controlled by the BCR. The input channels are sampled consecutively, starting with channel 00 located at the bottom (lowest address) of each block in the buffer, and proceeding through the highest channel at the top of the block.

Total data memory buffer size is 2,048 words. The remaining memory that is not used for storage of scanning input data may be used as on-board scratch pad memory.

2.3.2 Data Storage and Retrieval

The data buffer can be loaded or read from the bus at any time. Arbitration for the buffer occurs at the beginning of an update from the A/D Converter. If the converter has control of the memory when a bus transfer is initiated, the transfer will be extended by approximately 250 ns while the buffer update is completed.

If a bus transfer is in progress when a converter access is requested, the bus transfer will proceed normally and the converter access will take place after the transfer has been completed. Because the converter access must be completed before the scanning sequence can continue, a long data transfer (greater than 600 ns) may extend the 17 µs channel update period.

A data ready flag is set at the top, or highest address, of the buffer, and can be programmed to occur also at the middle of the buffer. The data ready flag can initiate an interrupt request, or can be read from the bus as a status flag.

2.4 Operating Modes

All operating modes available with the VME-3128A are controlled through the CSR and BCR. Operating modes are described in detail in ***Chapter 3, Programming***, and are summarized here as:

- Continuous scanning
- Single scan random access
- Timed burst
- Locally triggered burst
- Remotely triggered burst
- Gain loading

Continuous scanning is selected by clearing both mode control bits in the CSR (***Section 3.2.4, Control Registers*** on page 34), and is the default selection after a reset operation. All active channels are scanned continuously in this mode. A single channel can be selected at random for conversion in the single channel random access mode. The resulting digitized value is read from a dedicated Converter Data Register (CDR).

Three operating modes acquire data in bursts with each burst representing an entire update of the data buffer. Timed burst data is acquired in a single data scan, or burst, of all buffer locations when the interval timer times out. A single burst can be acquired at the end of the programmed interval, or the process can be repetitive. In the repetitive mode, a burst is acquired at the end of each interval until either a different mode is selected, or the interval timer is disabled by clearing CSR bit D09. Timer control is described in ***Section 3.2.9, Timer/Counter Registers*** on page 37.

Two "triggered burst" modes generate a single burst each time a trigger occurs. In the locally triggered burst mode, the trigger occurs when the "start sequence" control bit in the CSR is set (***Section 3.2.4, Control Registers*** on page 34). In the remotely triggered burst mode, the trigger occurs at the falling edge of the EXT STRT L digital input at the P2 connector.

Remotely triggered burst capability permits multiple boards to be synchronized. All boards will begin each scan simultaneously together. Multiboard synchronization is obtained by connecting the TRIG OUT L output from P2 of a synchronizing "master" to the EXT STRT L input of all slave boards. As many as 16 boards in a single chassis can be synchronized together.

If automatic selection of channel gain (autogain) is required, the gain code for each channel is loaded into the gain buffer while operating in the gain loading mode (see ***Section 2.1, Internal Functional Organization*** on page 26 for more information).

2.5 Analog Input Multiplexing, Sampling and Digitizing

2.5.1 Input Configuration

Analog inputs from connectors P3 and P4 are routed through low pass input filters to the input multiplexers shown in ***Figure 2-2, Analog Multiplexer and PGA*** on page 31. Channels 00 to 31 are connected through P4 and channels 32 to 63 are connected through P3.

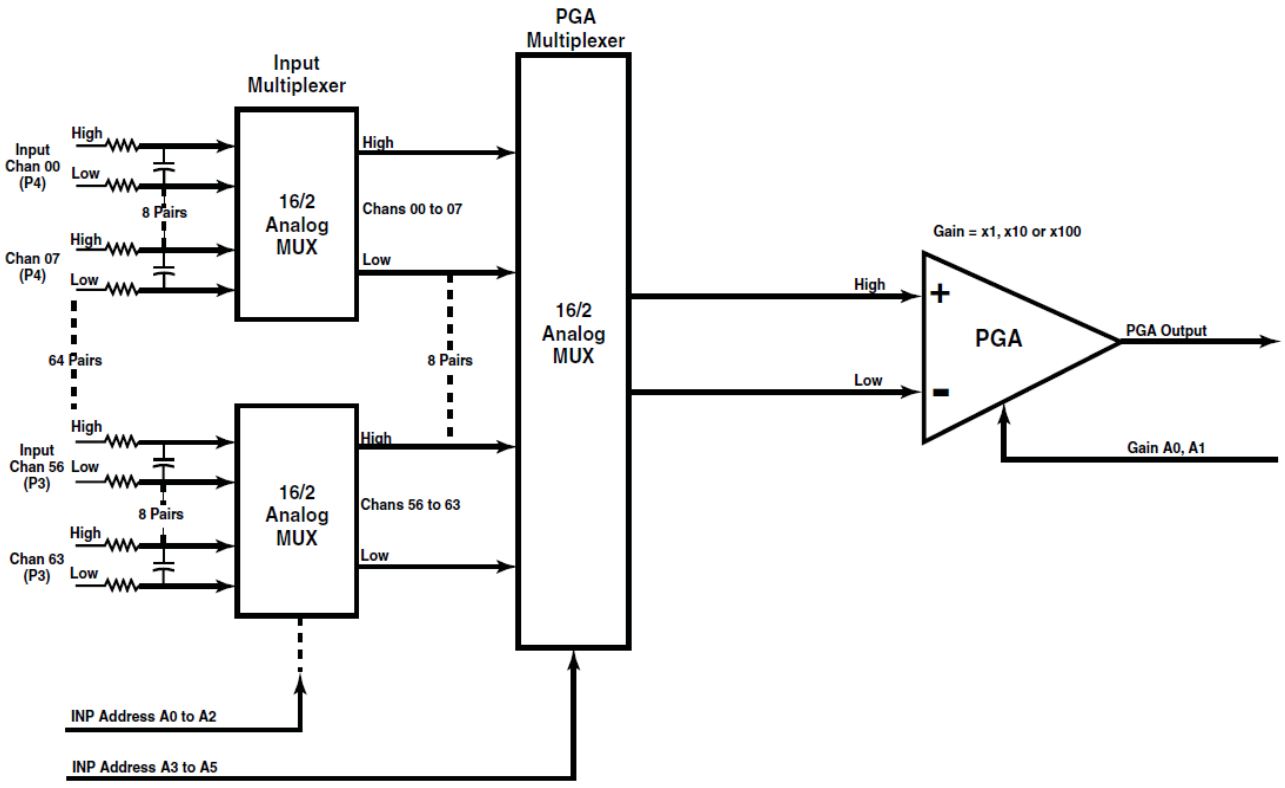

NOTE

The options A0CDEF have unity gain buffers between the input filters and multiplexer.

To provide at least one ground in each of the input connectors, the LOW inputs for channels 31 and 63 can be jumpered individually to either AGND or COMM, or can be left ungrounded (***Section 1.5, Operational Configuration*** on page 14 and ***Appendix A.1, Connector Descriptions***). AGND is the internal analog ground, and COMM is a bus which connects all center row (B row) pins together on P3 and P4. The COMM bus provides a return connection for all channels if 96-wire cables are used for the analog inputs.

The analog multiplexers route one of each group of eight channels to the PGA multiplexers, which in turn selects an input to route to the PGA. Input address lines A0, A1, and A2 control the input multiplexer, and A3, A4, and A5 select the PGA multiplexer input.

Figure 2-2 Analog Multiplexer and PGA



2.5.2 Gain Control

The programmable gain amplifier (PGA) applies a gain of x1, x10, or x100 to the differential channel from the PGA multiplexer, and produces a single-ended output. PGA gain is selected by the GAIN A0 and A1 control lines which originate either from the gain buffer, or from fixed gain jumpers (see *Section 2.1, Internal Functional Organization* on page 26).

2.5.3 Sampling and Digitizing

The output of PGA is buffered by a high-speed buffer, which takes care of ADC driving requirements. A convert command is issued after the required settling time from the channel selection. After the conversion is completed, a read ADC strobe stores the digitized value in the data buffer.

2.5.4 Analog-to-Digital Conversion

The output of the gain buffer is digitized by the 14-bit successive approximation A/D Converter. Each conversion is initiated by the convert command, and the Read ADC strobe writes the digitized value to the data buffer through the internal data bus. Total conversion time is 4µs.

Each conversion is initiated after allowing settling time of 12µs after channel selection. The remaining 1µs in the 17µs is used for house keeping operations such as reading the converter, storing in the RAM.

2.6 Power Converter

Electrical power for the analog networks is supplied by a single DC-to-DC Converter which converts 5 VDC logic power from the VMEbus into isolated and regulated ±15 VDC. This method is used so that this product does not require the optional ±12 V on the VMEbus backplane.

3 • Programming

3.1 Controlling the VME-3128A

VMEbus communication takes place through Control, Status, and Data Registers which can be jumper-located in either the A16 short I/O space or the A24 standard address space. A resident bus interrupter is under program control and can be configured to generate any interrupt request from IRQ1 through IRQ7.

Digitized input data is accumulated in a dual-port data buffer which consists of from 16 to 1,024 data words, where each data word contains the 14-bit digitized value of a single analog input channel. Data accumulates in the buffer in blocks of from 16 to 64 input channels. Buffer size and block size both are under program control, and the buffer can be read at any time without affecting the scanning sequence.

Data scaling is adjustable with jumper-controlled voltage ranges, and with either jumper-controlled or program-controlled channel gain. A Data Ready flag can be programmed to occur when the buffer is either filled or half-filled. An interrupt can be generated simultaneously with the Data Ready flag, or after a specific number of samples have been acquired.

The analog inputs can be scanned continuously or in triggered data bursts. Bursts (single scans) can be acquired automatically at intervals up to 536s, or can be triggered by an external event. Single channel random access is also supported.

References to programming jumpers are made throughout this section. Jumper installation requirements are described in *Chapter 1, Handling and Installation*.

3.2 General Control Features

3.2.1 Addressing Modes and Board Location

Programmable address jumpers permit the VME-3128A board to be located in either the short I/O (A16) space or the standard address (A24) space. The board can be located on any 4,096-word boundary. Board operation is jumper-configured in either program space or data space. Access privilege is jumper-designated as either short supervisory, short nonprivileged, or both.

3.2.2 Data Transfers

Registers at addresses $0000 to $0026 respond to both D08 and D16 data transfers, within the limitations described in *Section 3.2.4, Control Registers* on page 34. Data buffer locations can be read with either D8 (EO) or D16 transfers, but should be written with D16 transfers. Any register or buffer location can be accessed at any time without affecting the existing scanning sequence, although data transfers longer than 600 ns may extend conversion times.

3.2.3 Reset Operations and Initialization

All control registers are reset either by a system reset operation or by setting the software reset control bit D14 in the CSR. Either reset operation initializes the board to the following configurations:

- Continuous scanning operating mode
- 64-channel block size
- 64 data word buffer size
- Automatic gain set to x1
- Offset binary data coding
- Self-test LED ON
- Data Ready flag at end-of-buffer
- Interrupt disabled

The automatic gain codes for all channels will be initialized to "zero" (gain = x1) after a reset operation, as described in ***Section 3.3.6, Gain Initialization Preload*** on page 40. If the automatic gain mode has been jumper-selected, channel gains other than x1 must be initialized as described in ***Section 3.4.7, Gain Loading*** on page 42.

Conventions

Hexadecimal Notation: To be consistent with conventional VMEbus development system nomenclature, hexadecimal numbers throughout this document are indicated with the prefix "$" unless otherwise indicated, and are expressed in byte "$XX," word "$XXX," or longword "$XXXX XXXX" formats. Decimal numbers are presented without a designating prefix.

Logic States: This document uses the convention that a data bit or control line is "set" when it is in the "one," or HIGH state, and is "cleared" when "zero" or LOW.

3.2.4 Control Registers

Register designations and locations are summarized in ***Table 3-1, VME-3128A Board Register Map*** below.

Table 3-1 VME-3128A Board Register Map

Register Address (HEX)	Register Designation	DESIG	Access	Notes
$0000	Board Identification	BID	R	2
$0002	Control and Status	CSR	R/W	
$0004	Buffer Control	BCR	R/W	3
$0006 TO $000E	(Reserved)			
$0010	Interrupt Control	ICR	R/W	3
$0012 TO $0016	(Reserved)			
$0018	Interrupt Vector	IVR	R/W	3
$001A TO $001E	(Reserved)			
$0020	Internal Timer 0	TR0	R/W	3
$0022	Internal Timer 1	TR1	R/W	3
$0024	Data Counter	DCR	R/W	3
$0026	Timer/Counter Control	TCR	R/W	3
$0028 TO $007E	(Reserved)			

Table 3-1 VME-3128A Board Register Map (Continued)

$0080 TO $087E	Data Buffer	BUFF	R/W	4,5
$0800 TO $0FFE	Scratch Pad Memory	RAM	R/W	

NOTES:
1.Unless indicated otherwise, all registers are 16-bit words.
2.D08 to D15.
3.D00 to D07.
4.Buffer location $0080 is replaced with the Gain Code Buffer Register when operating in the gain loading mode, or the Converter Data Register when operating in the random access mode.
5. See ***Section 3.3.4, Data Buffer/RAM*** on page 40

3.2.5 Board Identification Register (BID)

The Board Identification Register (BID) contains the board identification code ($49XX) for the VME-3128A board, and occupies the upper eight data bits at board relative location $0000. This code can be used during system configuration to identify the board as a VME-3128A.

3.2.6 Control and Status Register (CSR)

CSR functions are summarized in ***Table 3-2, Control and Status Register (CSR) Bit Map*** on page 35. All control register bits are mapped directly to the status register. The CSR can be accessed with either D8 or D16 data transfers, and provides control and monitoring of the following board functions:

- Random access channel selection
- Operating mode
- Scan sequence start
- Timer and flag control
- Data Ready flag
- Data coding
- Board reset
- Self-test LED

Table 3-2 Control and Status Register (CSR) Bit Map

Control/Status Register							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Self-Test LED L	Software Reset H	Two's Compl H	Data Ready H (Status only)	EN Midscan Flag H	EN External Start H	EN Interval Timer H	Start Sequence H
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
MODE 1 H	MODE 0 H	INP A5 H	INP A4 H	INP A3 H	INP A2 H	INP A1 H	INP A0 H

Control/Status Register (CSR) Bit Definitions

Bit 15: **Self-Test LED** - The "Self-Test" LED is OFF if Bit 15 is set, or ON if Bit 15 is cleared.

Bit 14: **Software Reset** - All board functions are reset when Bit 14 is set. Bit 14 is cleared automatically when reset has been completed.

Bit 13: **Two's Compl** - Digitized input data is presented in offset binary format if Bit 13 is cleared, or in two's complement format if Bit 13 is SET.

Bit 12: **Data Ready (Status Only)** - Bit 12 is set according to: (a) the selected operating mode, (b) the Enable Midscan Flag (Bit 11), and (c) the status of the scanning sequence. An interrupt can be programmed to occur when Data Ready is set. Bit 12 is cleared automatically by the first data register access.

Table 3-3 Bit 12 Data Ready (Status Only)

Operating Mode	Bit 11	Bit 07	Bit 06	Condition for Setting Data Ready
Random Access	X	0	1	End-of-Conversion
Single or Autoscan	0	X	0	Data Buffer filled
Single or Autoscan	1	X	0	Data Buffer half-filled
Gain Loading	X	1	1	Data Ready not active

Bit 11: **Enable Midscan Flag** - Bit 11 controls the occurrence of the Data Ready flag (Bit 12) in the Single Scan and Autoscan operating modes.

Bit 10: **Enable External Timer** - When Bit 10 is set, the selected operating sequence is initiated by the falling edge of the External Start input at P2. Bit 10 permits multiple VME-3128A boards to be synchronized together to a single external signal.

Bit 09: **Enable Interval Timer** - The Autoscan Interval Timer operates when Bit 09 is set, and is disabled when Bit 09 is cleared. The selected operating sequence is initiated at the end of each interval. Bit 09 has no effect if Bit 10 is set.

Bit 08: **Start Sequence** - Random Access or Single Scan operation initiates when D08 is SET. Bit 08 has no effect if either Bit 09 or Bit 10 is set. Bit 08 is cleared automatically after sequence initiation.

Bits 07 through 06: **Mode [1:2]** - Bit 07 and Bit 06 select the operating sequence mode as:

Table 3-4 Mode [1:2] Bit 07 and Bit 06

D07	D06	Operating Mode
0	*0	Autoscanning
0	1	Random Access to any channel for conversion
1	0	Single Scan of data buffer
1	1	Gain Loading of AUTOGAIN channel-gain codes
* Default mode at reset.		

Bits 05 through 00: **Input Channel Select [INP A5:A0]** - Bits 00 through 05 select an input channel for random access and for auto gain loading.

3.2.7 Buffer Control Register (BCR)

Block size and data buffer size are controlled by the BCR, as shown in *Table 3-5, Buffer Control Register* on page 38. The BCR also controls the size of the interval timer as either 16 or 32 bits, and determines whether an interrupt will be generated by the data ready flag or by the channel counter.

3.2.8 Interrupter Registers

The interrupter control and vector registers are used to establish the interrupt parameters, and to enable or disable the interrupt. The interrupter registers are described in *Section 3.6, Bus Interrupter* on page 43.

3.2.9 Timer/Counter Registers

The timer/counter registers control three 16-bit counters, two of which are available for adjusting the time between scans in the timed-burst operating mode, and one of which can provide an interrupt at a specific data word count. These registers are described in *Section 3.7, Timer/Counter Control* on page 45.

3.2.10 Converter Data Register (CDR)

A/D Converter data is read from the CDR when the board is operating in the random access mode (*Section 3.4.2, Single Channel Random Access* on page 42).

3.3 Data Organization and Control

3.3.1 Data Word

The contents of each 16-bit word location in the data buffer is a *data word*, and represents the 14-bit left-justified digitized value of a single analog input channel.

3.3.2 Scaling and Coding

Table 3-6, ADC Data Format and Codings on page 39 shows the data word scaling and coding for all three available channel gains of x1, x10, and x100. Data Bit 15 is the most significant bit and Bit 00 is the least significant bit. Coding is straight binary or offset binary if CSR Bit 13 is cleared, and is two's complement if CSR Bit 13 is set.

3.3.3 Data Block

A complete set of digitized values for all active input channels is a data block, and it can consist of 16, 32, 48, or 64 channels. Block size is controlled by Bits 00 and 01 in the BCR, as shown in ***Table 3-6, ADC Data Format and Codings*** on page 39. Data words within a block are organized with channel 00 at the lowest address in the block, and with the highest numbered channel at the highest address.

Table 3-5 Buffer Control Register

BIT 00 and BIT 01	Input Block Size (Number of Active Channels)			
	BIT 01	Bit 00	Block Size	Active Input Channels
	0	0	*64 Channels	00 Through 63
	0	1	48	00 Through 47
	1	0	32	00 Through 31
	1	1	16	00 Through 15
Bit 02 Through Bit 04	Input Buffer Size (Total Data Storage)			
	Bit 04	Bit 03	Bit 02	Buffer Size (dec)
	0	0	0	*64 Words
	0	0	1	16
	0	1	0	32
	0	1	1	64
	1	0	0	128
	1	0	1	256
	1	1	0	512
	1	1	1	1,024
Bit 05	Interval Timer Select (Number of Cascaded 16-bit Timers)			
	Bit 05	Number of Timers		
	0	*1		
	1	2		
Bit 06	Interrupt Source Control			
	Bit 06	Interrupt Source		
	0	*Data Ready Flay (CSR)		
	1	Channel Counter		
Bit 07	Not Used			
* Default mode at reset.				

Table 3-6 ADC Data Format and Codings

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
ADC13	ADC 12	ADC 11	ADC 10	ADC 09	ADC 08	ADC 07	ADC 06
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
ADC 05	ADC 04	ADC 03	ADC 02	ADC 01	ADC 00	0	0

Table 3-7 ADC Data Format

ADC Data Coding (Gain = x1)			
Unipolar Range		Straight Binary	
Input	0 to +10 V	MSB	LSB
+FS-1 LS	+9.99939 V	1111 1111 1111 11	
+1/2 FS	+5.00000 V	1000 0000 0000 00	
+1 LSB	+0.00061 V	0000 0000 0000 01	
Bipolar Range		Offset Binary	
Input	±10V	MSB	LSB
+FS-1 LSB	+9.99878 V	1111 1111 1111 11	
+1/2 FS	+5.00000 V	1100 0000 0000 00	
+1 LSB	+0.00122 V	1000 0000 0000 01	
Zero	0.00000 V	1000 0000 0000 00	
-1 LSB	-0.00122V	0111 1111 1111 11	
-FS+1 LSB	-9.99878 V	0000 0000 0000 01	
-FS	-10.00000 V	0000 0000 0000 00	
Bipolar Range		Two's Complement	
Input	±10V	MSB	LSB
+FS-1 LSB	+9.99878 V	0111 1111 1111 11	
+1/2 FS	+5.00000 V	0100 0000 0000 00	
+1 LSB	+0.00122 V	0000 0000 0000 01	
Zero	0.00000 V	0000 0000 0000 00	
-1 LSB	-0.00122V	1111 1111 1111 11	
-FS+1 LSB	-9.99878 V	1000 0000 0000 01	
-FS	-10.00000 V	1000 0000 0000 00	
LSB Bit Weight Versus Input Gain			
Input Range	Gain = x1	x10	x100
0 to +5 V, ±2.5 V	305.176 µV	30.5176 µV	3.05176 µV
0 to +10 V, ±5 V	610.352 µV	61.0352 µV	6.10352 µV
±10 V	1.22070 mV	122.070 µV	12.2070 µV

3.3.4 Data Buffer/RAM

The *data buffer* contains from 1 to 64 data blocks, and is located at board address $0080. The size of the buffer is controlled by the Input Buffer Size bits (Bits 02 to 04) in the BCR. The buffer can be adjusted from 16 to 1,024 data words in six equal ratios of 2:1. A single update of all locations in the buffer is a *data scan*, and is executed at the maximum A/D conversion rate of 58 kHz. Data blocks within the buffer are organized with the first block located at the lowest word address in the buffer, and with the data word in the last block located at the highest address.

3.3.5 Gain Selection

A fixed channel gain of x1, x10, or x100 can be jumper-selected for all channels, or can be assigned individually for each channel. A jumper-selected gain applies to all channels and cannot be modified by the program. The automatic gain mode provides program control of the gain of each channel.

For automatic gain control, a gain code for each channel is loaded into board memory while operating in the Gain Loading mode (***Section 3.4.7, Gain Loading*** on page 42). The gain is adjusted automatically as each channel is selected and digitized. Gain codes for all channels are initialized to "zero" (gain = x1) automatically after a reset operation.

3.3.6 Gain Initialization Preload

Directly after each reset operation, an automatic initialization sequence presets all gain codes to "zero," and establishes a gain of x1 for all channels. The sequence is approximately 1.2 ms in length and is completed when the data ready flag (CSR Bit 12) is set at the end of the first buffer scan. During this initialization interval, the gain buffer should not be accessed from the VMEbus and the Enable Midscan Flag control bit (CSR Bit 11) should not be set.

3.4 Operating Modes

The VME-3128A board can be programmed to scan the input channels continuously, to read input channels individually, or to acquire data in timed or synchronized bursts. ***Table 3-8, Operating Mode Selection*** summarizes the various operating modes, all of which are described in this section.

3.4.1 Continuous Scanning

This ***default*** operating mode is selected by a reset operation, or by clearing both CSR Mode control bits. All active channels are scanned continuously in this mode, and any channel can be read at any time without affecting the scanning operation. (also see ***Section 3.2.3, Reset Operations and Initialization*** on page 34.)

Table 3-8 Operating Mode Selection

	CSR Control Bits					CSR Code (Note 1)		
Operating Mode	Bit 10	Bit 09	Bit 08	Bit 07	Bit 06		Initiation	Termination
Continuous Scanning (Note 2)	0	0	0	0	0	$8000	Select Mode	Change Mode
Random Access	0	0	1	0	1	$8140	Set CSR Bit 08 (Note 3)	Automatic (single sample)
Timed Bursts	0	1	0	1	0	$8280	Timer zero	Reset or Change mode
Locally Triggered Burst	0	0	1	1	0	$8180	Set CSR Bit 08 (Note 3)	Automatic (single Scan)
Remotely Triggered Burst	1	0	0	1	0	$8480	EXT trigger	Automatic (single scan)
Gain Loading (Note 5)	0	0	0	1	1	$80C0	Select Mode (Note 4)	Reset or change mode

NOTES:
1. The indicated CSR code also establishes the following conditions:
   a. Self-test LED is OFF. Subtract $8000 to turn the LED ON.
   b. Data coding is binary. Add $2000 for two's complement coding.
   c. Data Ready Flag occurs at end-of-scan. Add $0400 for a midscan flag.
   d. Random access channel is 00. Add channel HEX code for any other channel, e.g.: $001A for channel 26.
2. Continuous Scanning is the default mode after a reset operation.
3. CSR Bit 08 clears automatically after sequence initiation.
4. Input sampling and conversion are disabled in the gain loading mode.
5. Automatic channel gain is initialized to unity (x1) at reset, and is specified with a gain code as:

Gain Code	Channel Gain
$00	x1
$01	x10
$02	x100
$03	Invalid Code

3.4.2 Single Channel Random Access

In this mode, the digitized channel value is read from the Converter Data Register (CDR) at board address $0080. Each input channel is accessed individually by loading the channel number into CSR control Bits 00 through 05, and by setting the Start Sequence bit (CSR Bit 08). The Start Sequence bit clears automatically when the sample is initiated, and the Data Ready flag (CSR Bit 12) is set when the digitized value is available in the CDR.

3.4.3 Timed Burst

Timed burst data is acquired in a single data scan, or burst, of all buffer locations when the interval timer times out. A single burst can be acquired at the end of the programmed interval, or the process can be repetitive. In the repetitive mode, a burst is acquired at the end of each interval until either a different mode is selected, or the interval timer is disabled by clearing CSR Bit 09. Timer control is described in *Section 3.7, Timer/Counter Control* on page 45.

3.4.4 Locally Triggered Burst

An acquisition burst, or data scan, is produced each time the Start Sequence bit (CSR Bit 08) is set. The Start sequence bit clears automatically when the burst is initiated.

3.4.5 Remotely Triggered Burst

This mode is similar to the **locally triggered burst** mode, except that the burst is initiated by a HIGH to LOW transition on the EXT STRT L input at the P2 connector.

3.4.6 Synchronizing Multiple VME-3128A Boards

Multiple VME-3128A boards can be synchronized together by connecting the TRIG OUT L output from P2 of a synchronizing "master" to the EXT STRT L input of all slave boards. As many as sixteen boards in a single chassis can be synchronized in this manner, thereby providing up to 1,024 synchronized input channels and the simultaneous sampling of like numbered channels on all boards.

3.4.7 Gain Loading

If the **automatic gain** mode has been jumper-selected (*Section 3.4, Operating Modes* on page 41), the gain codes for channels with gains other than unity (x1) must be loaded into board memory after each reset operation. Gain loading is performed by first selecting the **gain loading** mode, and by then loading the gain code for each channel into the gain buffer, as listed in *Table 3-8, Operating Mode Selection* on page 41. Selection of the **gain loading** mode replaces the first word of the data buffer with the ***gain buffer*** register. A gain code for each channel is loaded into the gain buffer register, by selecting the channel in the CSR.

The address for each gain value is loaded into the CSR as the input address INPA0H to INPA5H (Bits 00 through 05). After all gain codes have been initialized, the **scanning mode** can be selected and the gain for each channel will be adjusted automatically.

The gain codes for all channels are initialized to "zero" (gain = x1) directly after a reset operation. The gain buffer should not be accessed during this initialization interval. The data ready flag is set when initialization is complete and the board may be accessed normally.

3.5 Scan Monitoring

3.5.1 Data Ready Flag and Interrupt

CSR Bit 12 is the Data Ready flag, and is set to "one" at the end of a scan if CSR Bit 11 is "zero," or at the middle of a scan if CSR Bit 11 is "one." The data ready flag clears automatically when any buffer location is accessed from the VMEbus.

If the interrupt is enabled and the BCR control bit D06 (*Table 3-5, Buffer Control Register* on page 38) is "zero," an interrupt will be generated when the data ready flag is set.

3.5.2 Data Counter and Interrupt

The Data Counter Register (DCR) can be programmed to provide a data word count directly, or to generate an interrupt when a specific number of A/D conversions have occurred. Control of the DCR is described in *Section 3.7, Timer/Counter Control* on page 45.

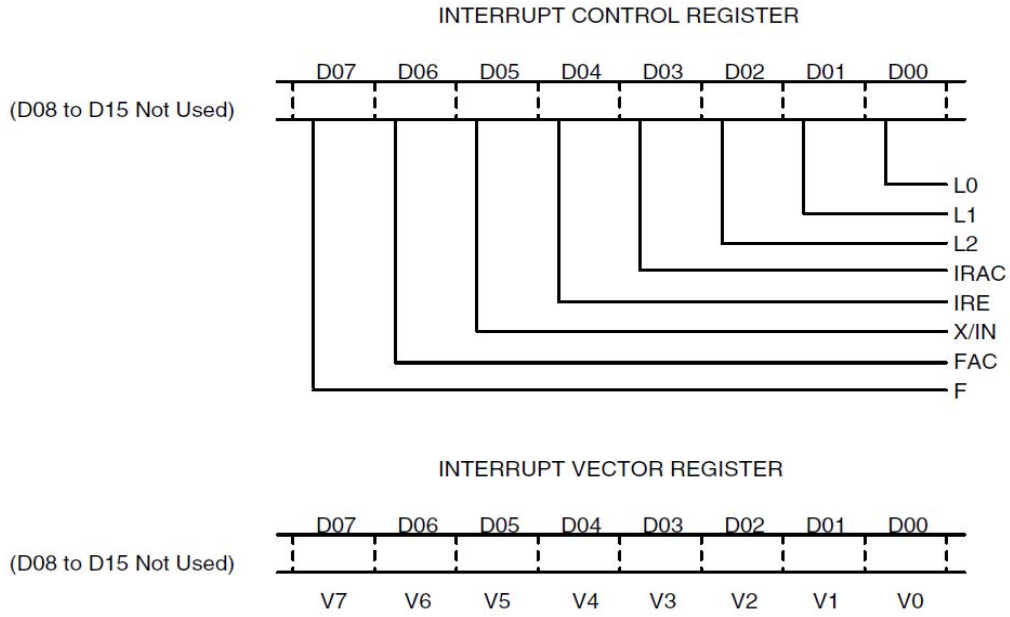
3.6 Bus Interrupter

An interrupt can be generated when the data buffer is filled or half-filled, or after a specific number of A/D conversions have been completed (*Section 3.5, Scan Monitoring* on page 43). The interrupt response is established through the Interrupt Control and Interrupt Vector registers which are shown in *Figure 3-1, Interrupt Registers Organization* below. During board reset or system reset operations, the Interrupt Control register is cleared to "$00" and the Interrupt Vector register is preset to "$0F."

3.6.1 Interrupt Control Register

The Interrupt Control register controls the interrupt level, as well as enabling or disabling the interrupt. The function of each control bit is described in *Table 3-9, Interrupt Control Register Functions* on page 45.

Figure 3-1 Interrupt Registers Organization



3.6.2 Interrupt Vector Register

Contents of the Interrupt Vector register are supplied as a data byte (Bits 07 through 00) on the data bus during the board's interrupt acknowledge cycle. The function of the vector is determined by the system user.

3.7 Timer/Counter Control

3.7.1 General Characteristics

Interval timing and data counting capabilities are provided by a triple 16-bit programmable timer/counter which is controlled by the timer/counter registers at board addresses $0020 to $0026 (*Table 3-1, VME-3128A Board Register Map* on page 34). Interval timer register TR0 is driven by an 8 MHz clock, and TMR1 is driven by the output of TMR0.

The Data Counter Register (DCR) operates independently of the two timers, and is used to monitor the progress of data through the buffer. Operating modes and data transfers for all three counters are controlled by the timer/counter register (TCR).

INTERRUPT LEVEL (L2, L1, L0, Bits 02, 01 and 00):

Determines the level at which an interrupt will occur:

Table 3-9 Interrupt Control Register Functions

Register Bit			
L2	L1	L0	IRQ Level
0	0	0	Disabled
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

INTERRUPT ENABLE (IRE, Bit 04): When this bit is set HIGH, the bus interrupt is enabled; the interrupt is disabled if IRE is LOW.

INTERRUPT AUTO-CLEAR (IRAC, Bit 03): If the IRAC bit is set HIGH, the interrupt enable bit (IRE) is cleared during the interrupt acknowledge cycle which responds to the request. The IRE bit must then be set HIGH again to enable the interrupt.

EXTERNAL/INTERNAL (X/IN, Bit 05): This control bit has no valid function on the VME-3128A board, and MUST be cleared LOW at all times.

FLAG (F, Bit 07): This control bit has no effect on the operation of the VME-3128A board, and is available for use by the controlling processor as a utility flag.

FLAG AUTO-CLEAR (FAC, Bit 06): If "FAC" is set HIGH, the flag bit "F" is automatically cleared during an interrupt acknowledge cycle.

All timer/counter data transfers are eight bits wide and use data Bits 00 through 07. Two data transfers are required to read or write each 16-bit counter, with the least significant byte transferred first and the most significant byte transferred second. The control word determines the type of transfer, and must be written to the timer/counter before each data transfer. *Table 3-10, Timer/Counter Data Transfer Sequences* on page 47 lists the data transfer sequences for the timers and counter.

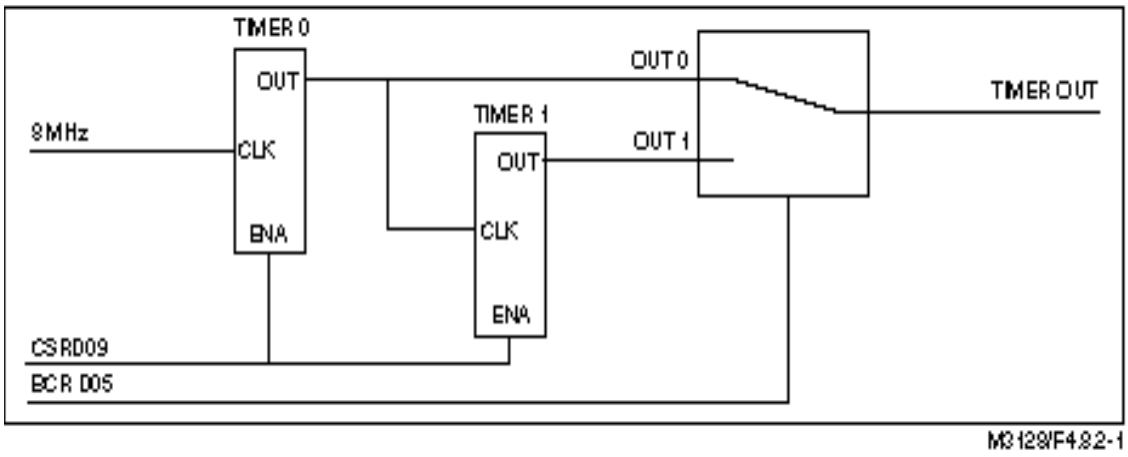
3.7.2 Scan Interval Timer

By operating in the "timed burst mode," the data buffer can be scanned (filled) repetitively at specific intervals, or a single scan can be initiated after the first interval. The timed burst mode is selected as follows:

- Operating Mode 2 CSR Bit 07 = 1, CSR Bit 06 = 0
- Interval Timer enabled CSR Bit 09 = 1

When operating in this mode, a buffer scan will occur at the end of the time interval programmed into the timer.

Figure 3-2 VME-3128A Timer Functional Block Diagram



If BCR Bit 05 is cleared, Timer 0's output is selected as the timer's output and the product of the timer's output will be:

```
Formula for 16-bit Timer: Time/.125 = T0
```

If BCR Bit 05 is set, then Timer 1's output is selected as the timer's output and the output of timer 0 is used as the clock for timer 1. The period of the timer's output will be:

Formula for 2 Cascaded 16-bit Timers: Time/.125 = T1 X T0

Where: Time = Period of Timer out in μs up to 536.8454 s.

- T0 = Timer 0's 16-bit value in decimal (1 to 6535).
- T1 = Timer 1's 16-bit value in decimal (1 to 65535).

See ***Figure 3-2, VME-3128A Timer Functional Block Diagram*** above for a functional block diagram of the interval timer circuitry.

Table 3-10 Timer/Counter Data Transfer Sequences

Operation	Load Sequence	Register Address	Register Name	Transferred Data, Bits 00-07 (Note 2)	XFR Mode
Load Timer 0	1 2 3	$26 $20 $20	Control Word TMR 0 LS Byte TMR 0 MS Byte	$34 (Select Timer) Least Significant Byte Most Significant Byte	Write Write Write
Load Timer 1 (Note 1)	1 2 3	$26 $22 $22	Control Word TMR 1 LS Byte TMR 1 MS Byte	$74 or $78 (Note 3) Least Significant Byte Most Significant Byte	Write Write Write
Load Data Counter	1 2 3	$26 $24 $24	Control Word CNTR LS Byte CNTR MS Byte	$B4 Least Significant Byte Most Significant Byte	Write Write Write
Read Timer 0	1 2 3 4	$26 $26 $20 $20	Control Word Control Word TMR 0 LS Byte TMR 0 MS Byte	$00 (Latch Timer Value) $34 (Select Timer) Least Significant Byte Most Significant Byte	Write Write Read Read
Read Timer 1 (Note 1)	1 2 3 4	$26 $26 $22 $22	Control Word Control Word TMR 1 LS Byte TMR 1 MS Byte	$40 $74 or $78 (Note 3) Least Significant Byte Most Significant Byte	Write Write Read Read
Read Data Counter	1 2 3 4	$26 $26 $24 $24	Control Word Control Word CNTR LS Byte CNTR MS Byte	$80 $B4 Least Significant Byte Most Significant Byte	Write Write Read Read

NOTES:
1. BCR control bit D05 must be set to "one" to include Timer 1 in the interval timer (see text). The 32-bit timer is configured as:

	Timer 1 (Bits 31 through 16)		Timer 0 (Bits 15 through 00)		
MSB	MS Byte	LS Byte	MS Byte	LS Byte	LSB

2. Timer values $0001 0000, $0001 0001, and $0001 are invalid.
3. A Timer 1 control word of $0074 will produce repetitive data bursts at the programmed interval. A control word of $0078 will limit the acquisition to a single data burst at the end of the first interval. The single burst can be repeated by reloading the timer 1 load sequence

Programmed timer intervals less than the time required to fill the buffer can cause unpredictable operation and should be avoided. The time, in microseconds, required to fill a buffer is 17 times the buffer word size. For example, a 64-word buffer fills in 1,088 µs.

3.7.3 Data Counter Control

The data counter can generate an interrupt after a predetermined number of data words have been stored in the buffer. The counter can be read directly to monitor the data count. To use the counter to generate an interrupt:

1. Load the data counter with the required data count (*Table 3-10, Timer/ Counter Data Transfer Sequences*).
2. Set the source control Bit 06 in the BCR (*Table 3-8, Operating Mode Selection* on page 41) to "one." (This disables the midscan/endscan interrupt.)
3. Enable the interrupt as described in *Section 3.6, Bus Interrupter* on page 43.
4. Initiate the scanning operation.

Table 3-10, Timer/Counter Data Transfer Sequences on page 47 shows the sequence required for reading the data counter directly. The data counter can be accessed at any time, regardless of which operating mode is selected. Because the counter counts down, the value read is the remaining data count.

3.8 Typical Programming Examples

The following examples of VME-3128A programming illustrate typical applications for various operating modes.

We assume the following conditions:

- Type 68010 or later system processor
- Automatic gain
- Short I/O location $FBFF 0000
- Offset binary data coding

3.8.1 Example C Header File

```
/*-------------------------------------------------------------------*/
/* 3128.H 3128 HEADER FILE                                           */
/*-------------------------------------------------------------------*/

/*  DEFINE  Bytes, Words, AND Longs  FROM C DATA SIZES.              */

typedef unsigned char  Byte;        /* BYTES ARE UNSIGNED CHAR'S    */
typedef unsigned short Word;        /* WORDS ARE UNSIGNED SHORT'S   */
typedef unsigned int   Long;        /* LONGS ARE UNSIGNED INT'S     */
typedef struct v3128_reg Reg3128;   /* 3128 register type           */
typedef struct v3128_buf Buf3128;   /* 3128 ram buff type           */

struct v3128_reg
{
Word reg3128[20];               /* 3128 REGISTERS ARE AN ARRAY OF 20 WORDS     */
};

struct v3128_buf
{
Word  adc3128[1024]; /* 3128 ADC MEMORY IS AN ARRAY OF 1024 WORDS   */
};

/*  REGISTER OFFSET (ARRAY) DEFINITIONS                              */

#define   BID          00        /* BOARD ID REGISTER (1 word)      */
#define   CSR          01        /* CONTROL AND STATUS REGISTER     */
#define   BCR          02        /* BUFFER CONTROL REGISTER         */
#define   ICR          08        /* INTERRUPT CONTROL REGISTER      */
#define   IVR          12        /* INTERRUPT VECTOR  REGISTER      */
#define   TR0          16        /* INTERVAL TIMER REGISTER 0       */
#define   TR1          17        /* INTERVAL TIMER REGISTER 1       */
#define   DCR          18        /* DATA COUNTER REGISTER           */
#define   TCR          19        /* TIMER/COUNTER CONTROL REGISTER  */
/*-------------------------------------------------------------------*/
```

3.8.2 Example C Program

```
/*--------------------------------------------------------------------*/
/*EXAMPLE C ROUTINES FOR THE VME-3128A 64-CHANNEL ANALOG INPUT BOARD */
/*--------------------------------------------------------------------*/
/*--------------------------------------------------------------------*/
/*  INCLUDE NEEDED SUPPORT CODE                                       */
/*--------------------------------------------------------------------*/
#include <stdio.h>                /* STANDARD I/O HEADER FILE       */
#include  "3128.h"                /* VME-3128A HEADER FILE          */
/*--------------------------------------------------------------------*/
/*  SETUP MEMORY POINTERS AND STORAGE                                 */
/*--------------------------------------------------------------------*/

void init_gain( Reg3128 *board, Buf3128 *buffer, Word gain );
void set_gain( Reg3128 *board, Buf3128 *buffer, Word channel, Word gain );
void auto_scan( Reg3128 *board, Buf3128 *buffer, Word num_of_scans );
void timed_scan( Reg3128 *board, Buf3128 *buffer, Word num_of_scans );
void local_burst( Reg3128 *board, Buf3128 *buffer ) ;
void remote_burst( Reg3128 *board, Buf3128 *buffer, Word num_of_scans );
struct
{
Word storage[1024] ;
} memory ;
Word loop, oldcsr, gain, channel, num_of_scans, num_done;
main()
{
Reg3128 * brd_base = ((Reg3128 *) 0xFBFF0000) ;
Buf3128 * buf_base = ((Buf3128 *) 0xFBFF0080) ;

gain = 0x0001;         /* GAIN SET EQUAL TO X10                      */
channel = 0x0005;      /* CHANNEL SELECTED IS CHANNEL 5              */
num_of_scans = 0x0100; /* NUMBER OF SCANS IS EQUAL TO 100 HEX BUFFERS */

init_gain( brd_base, buf_base, gain ) ;
set_gain( brd_base, buf_base, channel, gain ) ;
auto_scan( brd_base, buf_base, num_of_scans ) ;
timed_scan( brd_base, buf_base, num_of_scans ) ;
locally_burst( brd_base, buf_base ) ;
remote_burst( brd_base, buf_base, num_of_scans ) ;
}

/*--------------------------------------------------------------------*/

void init_gain( Reg3128 *board, Buf3128 *buffer, Word gain )
{
oldcsr = board->reg3128[CSR] ;
for( loop = 0x0000; loop < 0x0040; loop++ )
{
board->reg3128[CSR] = (0x80c0 + loop) ;    /* 80C0 = GAINLOAD MODE   */
buffer->adc3128[00] = gain ;
{
board->reg3128[CSR] = oldcsr ;
}

/*--------------------------------------------------------------------*/

void set_gain( Reg3128 *board, Buf3128 *buffer, Word channel, Word gain)
{
oldcsr = board->reg3128[CSR] ;
board->reg3128[CSR] = (0x80c0 + channel) ;  /* 80C0 = GAINLOAD MODE  */
buffer->adc3128[00] = gain ;
board->reg3128[CSR] = oldcsr ;
}
```

```
/*-------------------------------------------------------------------*/

void auto_scan( Reg3128 *board, Buf3118 *buffer, Word num_of_scans )
{
oldcsr = board->reg3128[CSR] ;
num_done = 0x0000 ;
board->reg3128[BCR] = 0x001C ; /* 64 CHANNELS, 1024 WORDS            */
board->reg3128[CSR] = 0x8800 ; /* AUTO SCAN, MIDSCAN ENABLED         */
do
{
if( board->reg3128[CSR] = = 0x9800 ) /* CHECK FOR DATA READY FLAG    */
{
for( loop = 0x0000; loop < 0x0400; loop ++ )
{
memory.storage[ loop ] = buffer->adc3128[ loop ] ;
}
num_done++ ;
}
} while ( num_done < num_of_scans ) ;
board->reg3128[CSR] = oldcsr ;
}

/*-------------------------------------------------------------------*/

void timed_scan( Reg3128 *board, Buf3128 *buffer, Word num_of_scans )
{
oldcsr = board->reg3128[CSR] ;
num_done = 0x0000 ;

board->reg3128[TCR] = 0x0034 ;  /* SELECT TIMER 0                    */
board->reg3128[TR0] = 0x00E8 ;  /* WRITE TR0 LSB                     */
board->reg3128[TR0] = 0x0003 ;  /* WRITE TR0 MSB                     */
board->reg3128[TCR] = 0x0074 ;  /* SELECT TIMER 1                    */
board->reg3128[TR1] = 0x0040 ;  /* WRITE TR1 LSB                     */
board->reg3128[TR1] = 0x001F ;  /* WRITE TR1 MSB                     */
board->reg3128[BCR] = 0x003C ;  /* 64 CHANNELS,1024 WORDS,TR1 ENABLED */
board->reg3128[CSR] = 0x8280 ;  /* TIMER ENABLED, SINGLE SCAN        */

do
{
if( board->reg3128[CSR] = = 0x9280 ) /* CHECK FOR NEW DATA READY FLAG */
{
for( loop = 0x0000; loop < 0x0400; loop ++ )
{
memory.storage[ loop ] = buffer->adc3128[ loop ] ;
}
num_done++ ;
}
} while ( num_done < num_of_scans ) ;
board->reg3128[CSR] = oldcsr ;
}
/*-------------------------------------------------------------------*/

void local_burst( Reg3128 *board, Buf3128 *buffer )
{
oldcsr = board->reg3128[CSR] ; /* STORE CSR FOR FUTURE USE          */
board->reg3128[BCR] = 0x001C ; /* 64 CHANNELS, 1024 WORDS           */
board->reg3128[CSR] = 0x8080 ; /* SINGLE SCAN                       */
board->reg3128[CSR] = 0x8180 ; /* TRIGGER BURST                     */
for( loop = 0x0000; loop < 0x0400; loop ++ )
{
memory.storage[ loop ] = buffer->adc3128[ loop ] ;
num_done++ ;
```

```
}
board->reg3128[CSR] = oldcsr ;
}
/*--------------------------------------------------------------------*/
void remote_burst( Reg3128 *board, Buf3128 *buffer, Word num_of_scans )
{
oldcsr = board->reg3128[CSR] ;
num_done = 0x0000 ;
board->reg3128[BCR] = 0x001C ; /* 64 CHANNELS, 1024 WORDS           */
board->reg3128[CSR] = 0x8480 ; /* WAIT REMOTE TRIGGER               */
do
{
if( board->reg3128[CSR] = = 0x9480 )
{
for( loop = 0x0000; loop < 0x0400; loop ++ )
{
memory.storage[ loop ] = buffer->adc3128[ loop ] ;
}
num_done++ ;
}
} while ( num_done < num_of_scans ) ;
board->reg3128[CSR] = oldcsr ;
}
/*--------------------------------------------------------------------*/
```

A • Connectors and Pinouts

Appendix A displays the connectors and pinouts for VME-3128A.

A.1 Connector Descriptions

Electrical connections to the VME-3128A board are made through four 96-pin DIN connectors P1 through P4, all of which have the pin configuration shown in *Figure A-1, P3 and P4 Connector Pin Configuration* on page 54 and *Figure A-2, P1 and P2 Connector Pin Configuration* on page 54.

P1 connects the VME-3128A board to the VMEbus backplane, and contains the address, data, and control lines, and all additional signals necessary to control VMEbus functions related to the board. P2 provides the user pins necessary for external synchronization of the board. User pin assignments are listed in *Table A-1, Input/Output Connector Pin Assignments* below and *Table A-2, P4 and P3 Connector Pinouts* on page 53.

Table A-1 Input/Output Connector Pin Assignments

P2 Connector User Pins		
Pin Number	Input/Output Signal	
	Row A	Row C
01 to 26	N/C	N/C
27	EXT STRT L	N/C
28	EXT STRT RTN	N/C
29	TRIG OUT L	N/C
30	N/C	N/C
31	EN EXT STRT H	N/C
32	N/C	N/C

Table A-2 P4 and P3 Connector Pinouts

P4 Connector	Input Signal			P3 Connector	Input Signal		
Pin Number	Row A	Row B	Row C	Pin Number	Row A	Row B	Row C
01	CH 00 High	COMM	CH 00 Low	01	CH 32 High	COMM	CH 32 Low
02	CH 01 High	COMM	CH 01 Low	02	CH 33 High	COMM	CH 33 Low
03	CH 02 High	COMM	CH 02 Low	03	CH 34 High	COMM	CH 34 Low
04	CH 03 High	COMM	CH 03 Low	04	CH 35 High	COMM	CH 35 Low
05	CH 04 High	COMM	CH 04 Low	05	CH 36 High	COMM	CH 36 Low
06	CH 05 High	COMM	CH 05 Low	06	CH 37 High	COMM	CH 37 Low
07	CH 06 High	COMM	CH 06 Low	07	CH 38 High	COMM	CH 38 Low
08	CH 07 High	COMM	CH 07 Low	08	CH 39 High	COMM	CH 39 Low
09	CH 08 High	COMM	CH 08 Low	09	CH 40 High	COMM	CH 40 Low
10	CH 09 High	COMM	CH 09 Low	10	CH 41 High	COMM	CH 41 Low
11	CH 10 High	COMM	CH 10 Low	11	CH 42 High	COMM	CH 42 Low
12	CH 11 High	COMM	CH 11 Low	12	CH 43 High	COMM	CH 43 Low
13	CH 12 High	COMM	CH 12 Low	13	CH 44 High	COMM	CH 44 Low
14	CH 13 High	COMM	CH 13 Low	14	CH 45 High	COMM	CH 45 Low
15	CH 14 High	COMM	CH 14 Low	15	CH 46 High	COMM	CH 46 Low
16	CH 15 High	COMM	CH 15 Low	16	CH 47 High	COMM	CH 47 Low
17	CH 16 High	COMM	CH 16 Low	17	CH 48 High	COMM	CH 48 Low
18	CH 17 High	COMM	CH 17 Low	18	CH 49 High	COMM	CH 49 Low
19	CH 18 High	COMM	CH 18 Low	19	CH 50High	COMM	CH 50 Low
20	CH 19 High	COMM	CH 19 Low	20	CH 51 High	COMM	CH 51 Low
21	CH 20 High	COMM	CH 20 Low	21	CH 52 High	COMM	CH 52 Low
22	CH 21 High	COMM	CH 21 Low	22	CH 53 High	COMM	CH 53 Low
23	CH 22 High	COMM	CH 22 Low	23	CH 54 High	COMM	CH 54 Low
24	CH 23 High	COMM	CH 23 Low	24	CH 55 High	COMM	CH 55 Low
25	CH 24 High	COMM	CH 24 Low	25	CH 56 High	COMM	CH 56 Low
26	CH 25 High	COMM	CH 25 Low	26	CH 57 High	COMM	CH 57 Low
27	CH 26 High	COMM	CH 26 Low	27	CH 58 High	COMM	CH 58 Low
28	CH 27 High	COMM	CH 27 Low	28	CH 59 High	COMM	CH 59 Low
29	CH 28 High	COMM	CH 28 Low	29	CH 60 High	COMM	CH 60 Low
30	CH 29 High	COMM	CH 29 Low	30	CH 61 High	COMM	CH 61 Low
31	CH 30 High	COMM	CH 30 Low	31	CH 62 High	COMM	CH 62 Low
32	CH 31 High	COMM	*CH 31 Low	32	CH 63 High	COMM	*CH 63 Low

* Channels 31 and 63 Low inputs can be jumpered individually to either COMM or AGND returns.

Figure A-1 P3 and P4 Connector Pin Configuration

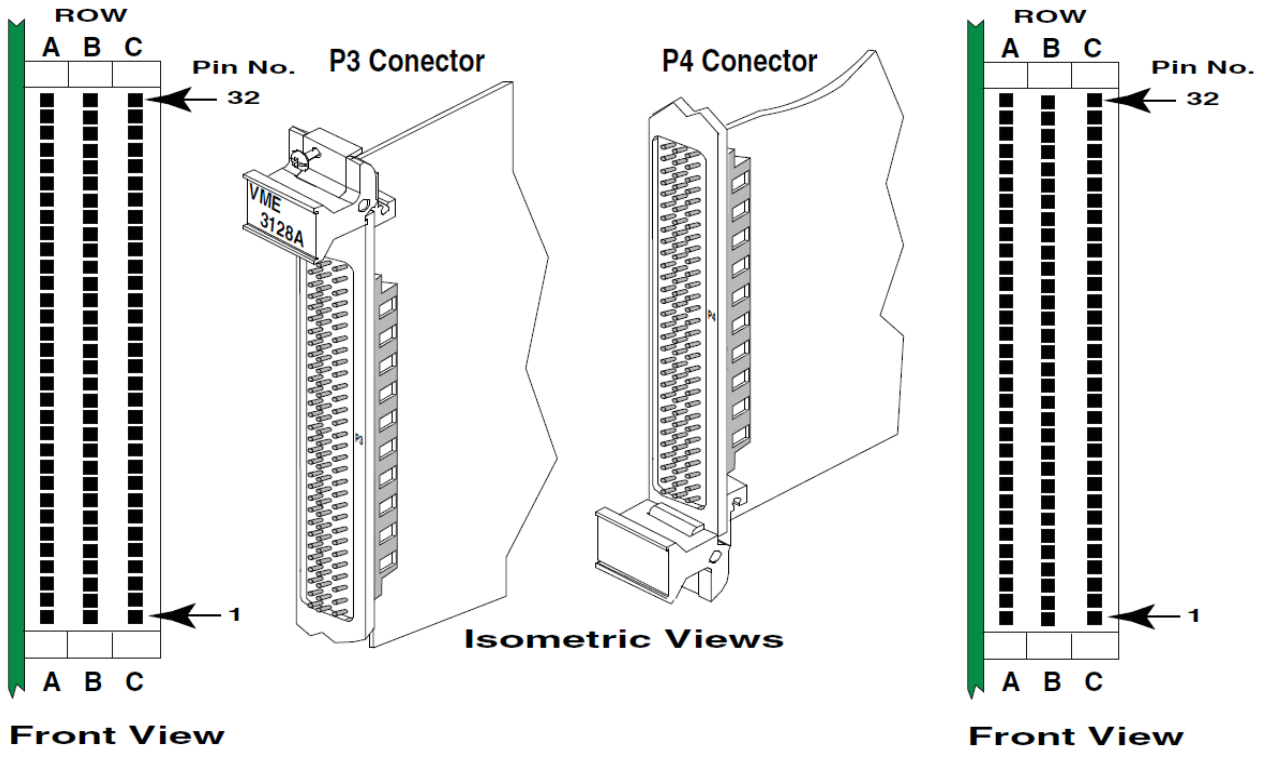
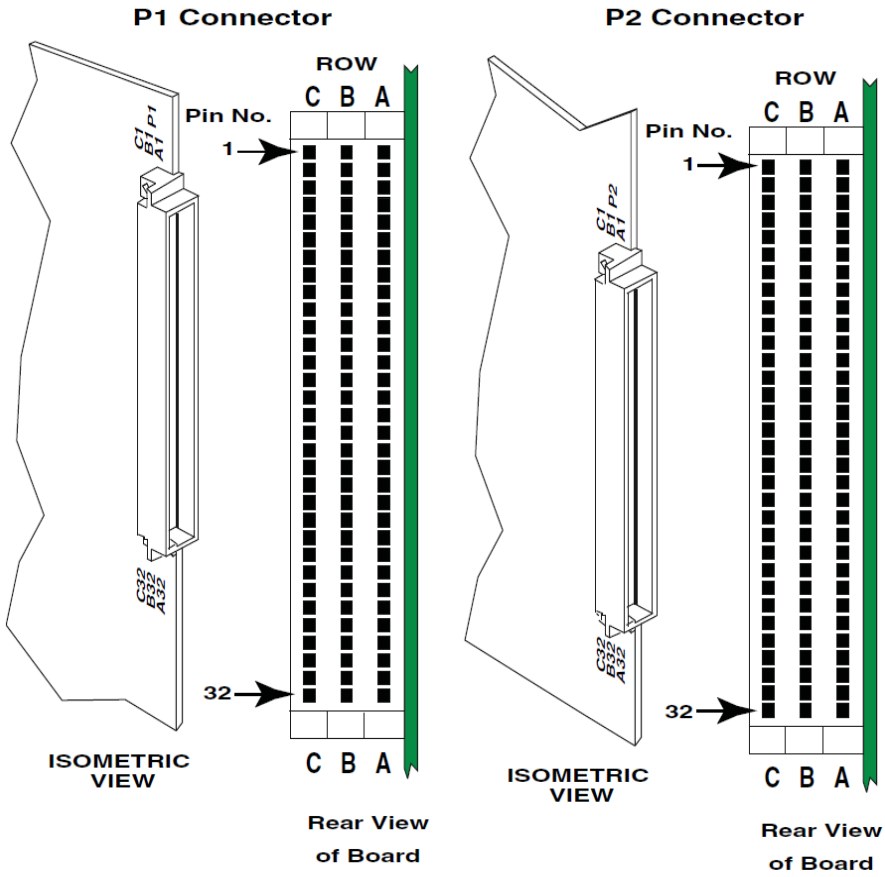


Figure A-2 P1 and P2 Connector Pin Configuration



A.2 Input Modes

Analog inputs are connected to the board through front panel connectors P3 and P4. P4 contains the input pins for channels 00 to 31, and P3 contains the input pins for channels 32 to 63. Pin assignments for P3 and P4 are summarized in ***Table A-2, P4 and P3 Connector Pinouts*** on page 53. The center "B" rows in P3 and P4 are connected together to a COMM bus, which can be used as a guard bus for 96-wire cables. Refer to ***Section 1.5.9, Input Configurations*** on page 19 and ***Table 1-6, Input Configuration Selection*** on page 20 for the selection of single-ended, differential, or pseudo-differential input configurations.

A.3 Input Cables

If 96-wire 0.033-inch ribbon cables or discrete wire type cables are used for the analog inputs, the center row COMM bus can provide a ground reference to the analog return (AGND) on the board by installing Jumper J3. If 64-wire 0.050-inch ribbon cables are used, "vari twist" or equivalent twisted-pair cables are recommended to minimize crosstalk and induced noise. Access to AGND is available in 64-wire cables at pin C32 of P3 and P4 by installing J1-1,2 for P4, or J2-1, 2 for P3.

A.4 External Synchronization

External TTL-level synchronization triggers are connected to the EXT STRT L input at the P2 connector (refer to ***Section 1.5.8, External Triggering*** on page 19). The EN EXT STRT H output is a flag to the triggering device that the VME-3128A is ready to accept an external trigger. To synchronize multiple VME-3128A boards together, connect the TRIG OUT H output from the designated "master" board to the EXT STRT L input of all boards to be synchronized to the master.

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