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VMIVME-7805

Intel Pentium 4 Processor-M Based VMEBus SBC

Product Manual

A GE Fanuc Company

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

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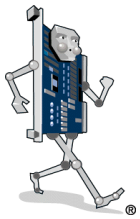
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Overview

Introduction

The VMIVME-7805 is a full-featured Pentium 4 Processor-M compatible SBC in a single-slot, passively cooled, Eurocard form factor that utilizes the advanced technology of Intel's 852GM chipset running a front-side bus rate of 400 MHz. The VMIVME-7805 is compliant with the VMEbus Specification Rev. C.1 and features a transparent PCI-to-VMEbus bridge, allowing the board to function as a system controller or peripheral CPU in multi-CPU systems.

The VMIVME-7805 provides features typically found on desktop systems such as:

- Up to 1GB PC2100 DDR SDRAM
- Built-in SVGA support with 4 Mbytes DRAM display cache
- Two built-in Ethernet controllers (one supporting Gigabit Ethernet, the other supporting 10 / 100 Mbit Ethernet)
- IDE drive support (VMEbus P2)
- Floppy drive support (VMEbus P2)
- Two high-performance 16550-compatible serial ports (COM1 and COM2)
- Front panel USB port Rev. 2.0
- Real-Time clock / calendar
- Front panel reset switch
- Miniature speaker
- Keyboard / Mouse port

The VMIVME-7805 is capable of executing many of today's desktop operating systems such as Microsoft's Windows XP, Windows 2000 and a wide variety of Linux-based operating systems. The standard desktop features of the VMIVME-7805 are described in Chapter 2 of this manual.

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The VMIVME-7805 provides features useful to embedded applications such as:

- I^2C bus support
- Remote Ethernet booting
- Up to 1 Gbyte of bootable CompactFlash (optional)
- Four general-purpose programmable timers (two 16-bit and two 32-bit)
- Software-selectable Watchdog Timer with reset
- 32 kbyte Non-volatile SRAM

Additionally, the VMIVME-7805 offers a PMC expansion site with front-panel access. The VMIVME-7805 is capable of executing many of today's embedded operating systems such as VxWorks, QNX, Solaris, LynxOS and Microsoft's Windows XP. The embedded features of the VMIVME-7805 are described in Chapter 3 of this manual.

The VMIVME-7805 is suitable for use in a variety of applications, such as: telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance processing power in a single VMEbus slot is desired.

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Intel 852GM Chipset

The VMIVME-7805 incorporates the latest Intel chipset technology, the 852GM. The Intel 852GM chipset is an optimized integrated graphics solution with a 400 MHz system bus and integrated 32-bit 3D core at 133 MHz with dynamic video memory technology (DVMT). The chipset has a low power design, advanced power management, supporting up to 1 Gbyte of DDR system Memory. The 852GM is a Graphics Memory Controller Hub component (GMCH), providing the processor interface, system memory interface (DDR SDRAM), Hub interface, CRT, LVDS and one DVO port.

Key features for the 852GM:

- 400 MHz Processor system bus controller
- Graphics controller interface
- Dual channel 18-bit LVDS interface for TFT panel support
- One digital video out port
- Supports DDR200 / 266 MHz memory technology
- High-speed accelerated hub architecture interface for communication with the ICH4-M (I / O controller)

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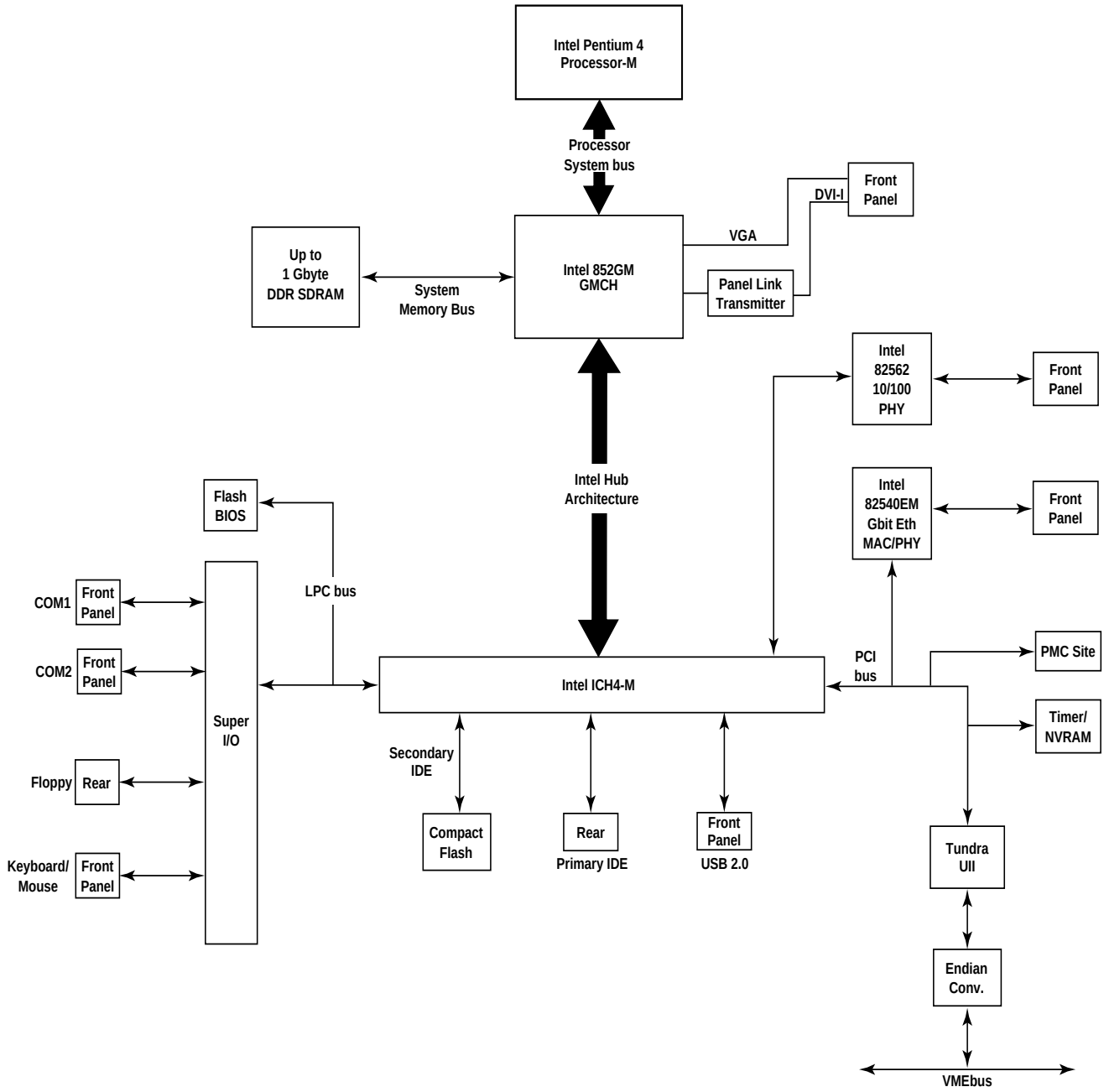


Figure 1 VMIVME-7805 Block Diagram

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Organization of the Manual

This manual is composed of the following chapters and appendices:

Chapter 1 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup and operation of the VMIVME-7805.

Chapter 2 - Standard Features describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 3 - Embedded PC/RTOS Features describes the unit features that are beyond standard functions.

Chapter 4 - Maintenance provides information relative to the care and maintenance of the unit.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - AMI BIOS describes the menus and options associated with the American Megatrends, Inc.(system) BIOS.

Appendix C -System Driver Software provides details for installing drivers under Windows 2000 and Windows XP.

Appendix D - Argon BIOS describes the menus and options associated with the remote Ethernet booting BIOS.

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References

Pentium 4 Processor-M µFCPGA package at 1.7 to 2.2GHz
January 2003, Order Number 250686-005

Intel 852GM Graphics and Memory Controller Hub (GMCH)
January 2003, Order Number 252338-001

Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)
January 2003, Order Number 252337-001

Intel 82540EM Gigabit Ethernet Controller
April 2003

PCI Local Bus Specification, Rev. 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

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Tundra Universe II Based VMEbus Interface
Doc. No. 500-000211-000
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(800) 322-3616
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For a detailed description and specification of the VME bus, please refer to:

VMEbus Specification Rev. C. and the VMEbus Handbook

VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

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Notation and Terminology

This product bridges the traditionally divergent worlds of Intel-based PC's and Motorola-based VMEbus controllers; therefore, some confusion over "conventional" notation and terminology may exist. Every effort has been made to make this manual consistent by adhering to conventions typical for the Motorola/VMEbus world; nevertheless, users in both camps should review the following notes:

- Hexadecimal numbers are listed Motorola-style, prefixed with a dollar sign: $F79, for example. By contrast, this same number would be signified 0F79H according to the Intel convention, or 0xF79 by many programmers. Less common are forms such as $F79_h$ or the mathematician's $F79_{16}$.
- An 8-bit quantity is termed a "byte," a 16-bit quantity is termed a "word," and a 32-bit quantity is termed a "longword." The Intel convention is similar, although their 32-bit quantity is more often called a "doubleword."
- Motorola programmers should note that Intel processors have an I/O bus that is completely independent from the memory bus. Every effort has been made in the manual to clarify this by referring to registers and logical entities in I/O space by prefixing I/O addresses as such. Thus, a register at "I/O $140" is not the same as a register at "$140," since the latter is on the memory bus while the former is on the I/O bus.
- Intel programmers should note that addresses are listed in this manual using a linear, "flat-memory" model rather than the old segment:offset model associated with Intel Real Mode programming. Thus, a ROM chip at a segment:offset address of C000:0 will be listed in this manual as being at address $C0000. For reference, here are some quick conversion formulas:

Segment:Offset to Linear Address

Linear Address = (Segment × 16) + Offset

Linear Address to Segment:Offset

Segment = ((Linear Address ÷ 65536) – *remainder*) × 4096

Offset = *remainder* × 65536

Where *remainder* = the fractional part of (Linear Address ÷ 65536)

Note that there are many possible segment:offset addresses for a single location. The formula above will provide a unique segment:offset address by forcing the segment to an even 64 Kbyte boundary, for example, $C000, $E000, etc. When using this formula, make sure to round the offset calculation properly!

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CHAPTER 1

Installation and Setup

Contents

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Introduction

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the VMIVME-7805.

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Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC Customer Care along with a request for advice concerning the disposition of the damaged item(s).

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

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Hardware Setup

The VMIVME-7805 is factory populated with user-specified options as part of the VMIVME-7805 ordering information. The processor speed, memory size and CompactFlash memory size are not user-upgradable. To change processor speeds or RAM / Flash size, contact Customer Care to receive a Return Material Authorization (RMA).

VMIC Customer Care is available at: 1-800-240-7782.

Or E-mail us at customer.service@vmic.com

The VMIVME-7805 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the single board CPU are illustrated in Figure 1-1 on page 26. The definitions of the CPU board jumpers and connectors are included in Table 1-1 through Table 1-8.

CAUTION: All jumpers marked *User Configurable* in the following tables may be changed or modified by the user. All jumpers marked factory configured should not be modified by the user.

Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper not marked “User Configurable” will void the Warranty and may damage the unit. The default jumper condition of the VMIVME-7805 is expressed in Table 1-1 through Table 1-8 with **bold text** in the table cells.

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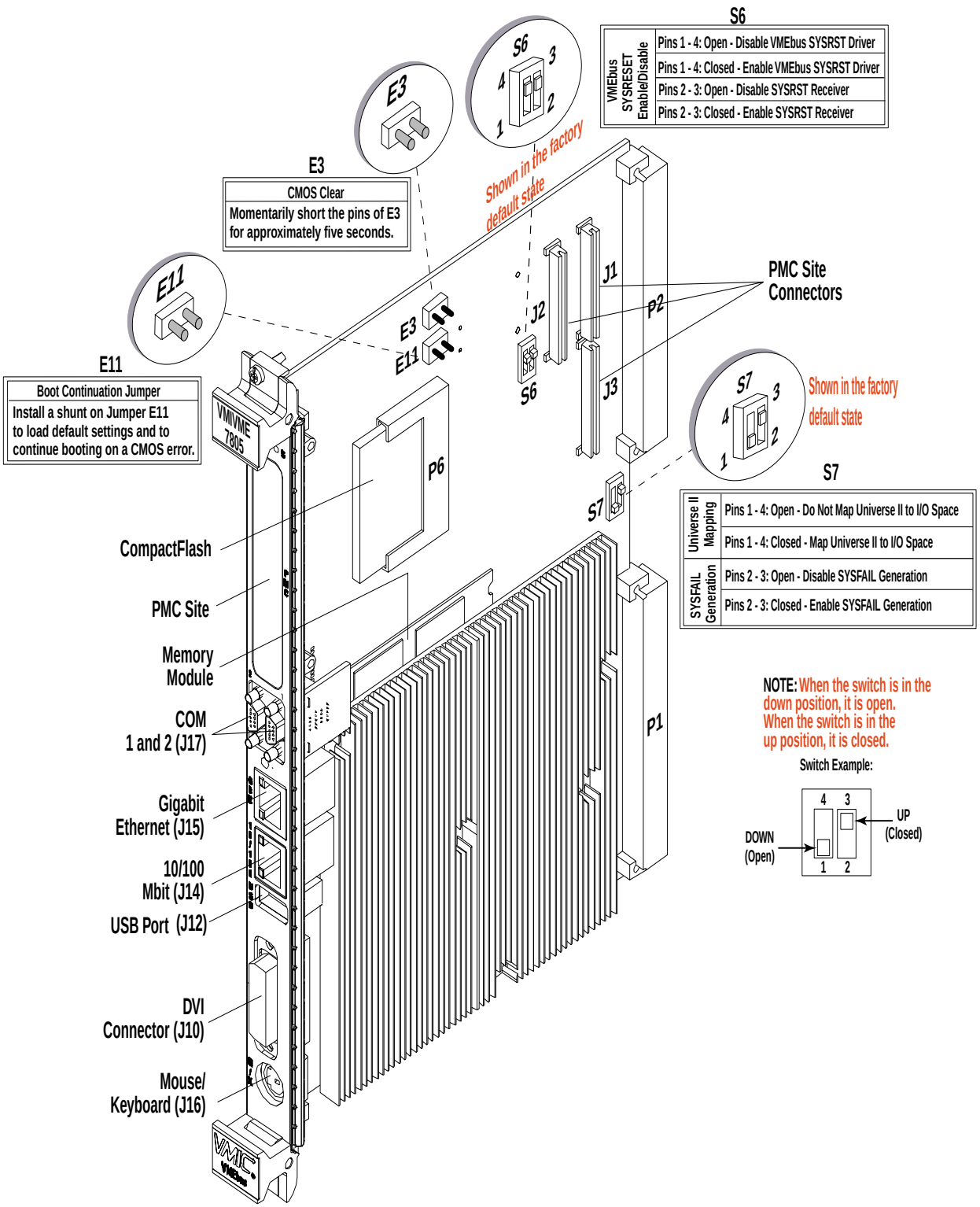


Figure 1-1 VMIVME-7805 Board Layout

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Table 1-1 CPU Board Headers, Jumpers and Connectors

Connector	Function
J16	Mouse / Keyboard
J15	10 / 100 / 1000 Gbit Ethernet
J14	10 / 100 Mbit Ethernet
P2	IDE (PRI), Floppy
J12	USB port
J10	DVI Video
J9	Board-to-Board Connector
E1, E2, E4, E9, E10, E17, E18	Factory Reserved Do Not Use
E3	CMOS Clear Jumper
E5	BIOS Block Lock Jumper
E6	BIOS Write Protect Jumper
E11	Boot Continuation Jumper
E17	I^2C Header
S6, S7	VME Switches
J1, J2, J3	PMC Site Connectors
P6	CompactFlash Connector
J17	COM 1, COM 2
P1, P2	VMEbus Backplane Connectors

NOTE: The BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper allows the user to clear the password in the case of a forgotten password.

CMOS Password

To clear the CMOS password:

1. Turn off power to the unit.
2. Momentarily short the pins of E3 for approximately five seconds.
3. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared.

Table 1-2 Clear CMOS (**User Configurable**) - Jumper (E3)

Select	Jumper Position
Normal	**Open**
Clear CMOS / Password	Momentarily Short

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Table 1-3 Factory Configured - BIOS Block Lock - Jumper (E5)

Select	Jumper Position
Locked	In
Not Locked	**Out**

Table 1-4 Factory Configured - BIOS Write Protect - Jumper (E6)

Select	Jumper Position
Write Protected	In
Not Write Protected	**Out**

Table 1-5 Boot Continuation - Jumper (E11)

Select	Jumper Position
Load Default settings and tcontinue booting on CMOS error	In
Stop booting on CMOS error	**Out**

Table 1-6 VMEbus SYSRESET Enable/Disable (**User Configurable**) - Switch (S6)

Select	Switch Position	Switch No.
Disable VMEbus SYSRST Driver	Open	1 - 4
Enable VMEbus SYSRST Driver	**Closed**	**1 - 4**
Disable VMEbus SYSRST Receiver	Open	2 - 3
Enable SYSRST Receiver	**Closed**	**2 - 3**

Table 1-7 Universe II Mapping/SYSFAIL Generation (**User Configurable**) - Switch (S7)

Select	Switch Position	Switch No.
Do not Map UNIV2 to I/O Space	Open	1-4
Map UNIV2 to I/O Space	**Closed**	**1-4**
Disable SYSFAIL Generation	Open	2-3
Enable SYSFAIL Generation	**Closed**	**2-3**

Power Requirements

The VMIVME-7805 requires +5V from the VMEbus backplane. Below are the voltage and current requirements.

Supply	Current (Typical)	Current (Maximum)
+5V	6.08A	8.2A

The VMIVME-7805 provides power to the PMC site in accordance with the PMC specification. The maximum current provided on the +5V supply is 1.5A per PMC site. The maximum current provided on the +3.3V supply is 1.5A per PMC site.

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Installation

The VMIVME-7805 conforms to the VMEbus physical specification for a single slot 6U Eurocard (dual height). It can be plugged directly into any standard chassis accepting this type of board.

CAUTION: Do not install or remove the board while power is applied.

The following steps describe the VMIC recommended method for VMIVME-7805 installation and power-up:

1. Make sure power to the equipment is off.
2. Choose chassis slot. The VMIVME-7805 ***must*** be attached to a P1/P2 VMEbus backplane.

   If the VMIVME-7805 is to be the VMEbus system controller, choose the first VMEbus slot. If a different board is the VMEbus system controller, choose any slot **except** slot one. The VMIVME-7805 does not require jumpers for enabling/disabling the system controller function.

NOTE: Air flow requirements as measured at output side of heatsink is to be greater than 350LFM.

3. Connect all needed peripherals to the front panel. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A. Minimally, a keyboard and a monitor are required if the user has not previously configured the system.
4. Apply power to the system. Several messages are displayed on the screen, including names, versions and copyright dates for the various BIOS modules on the VMIVME-7805.
5. The VMIVME-7805 features an optional Flash Disk resident on the board. Refer to Chapter 3 for set up details.
6. If an external drive module is installed, the BIOS Setup program must be run to configure the drive types. See Appendix C to properly configure the system.
7. If a drive module is present, install the operating system according to the manufacturer's instructions.

See Appendix B for instructions on installing VMIVME-7805 peripheral driver software during operating system installation.

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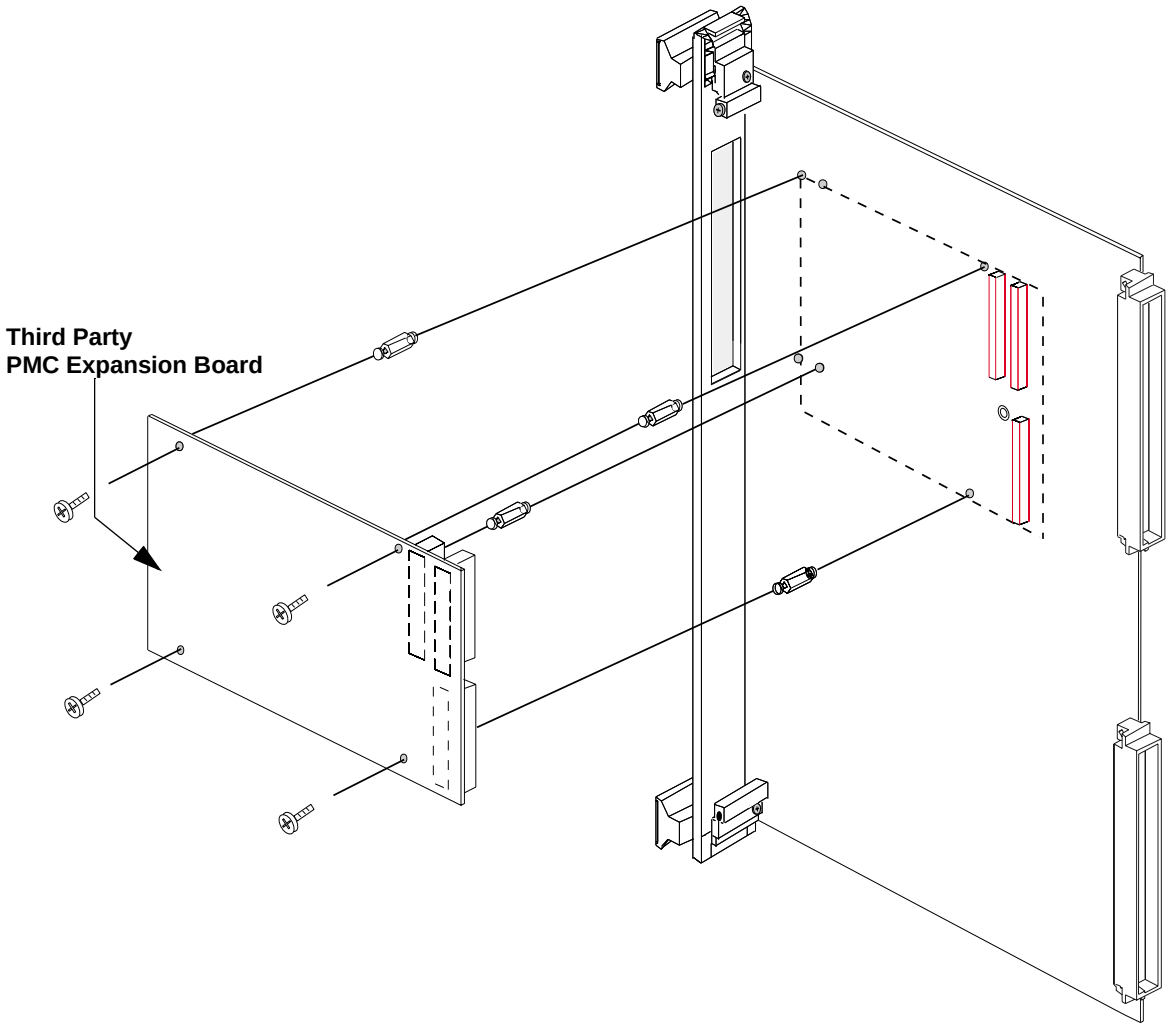


Figure 1-2 Installing a PMC Card on the VMIVME-7805

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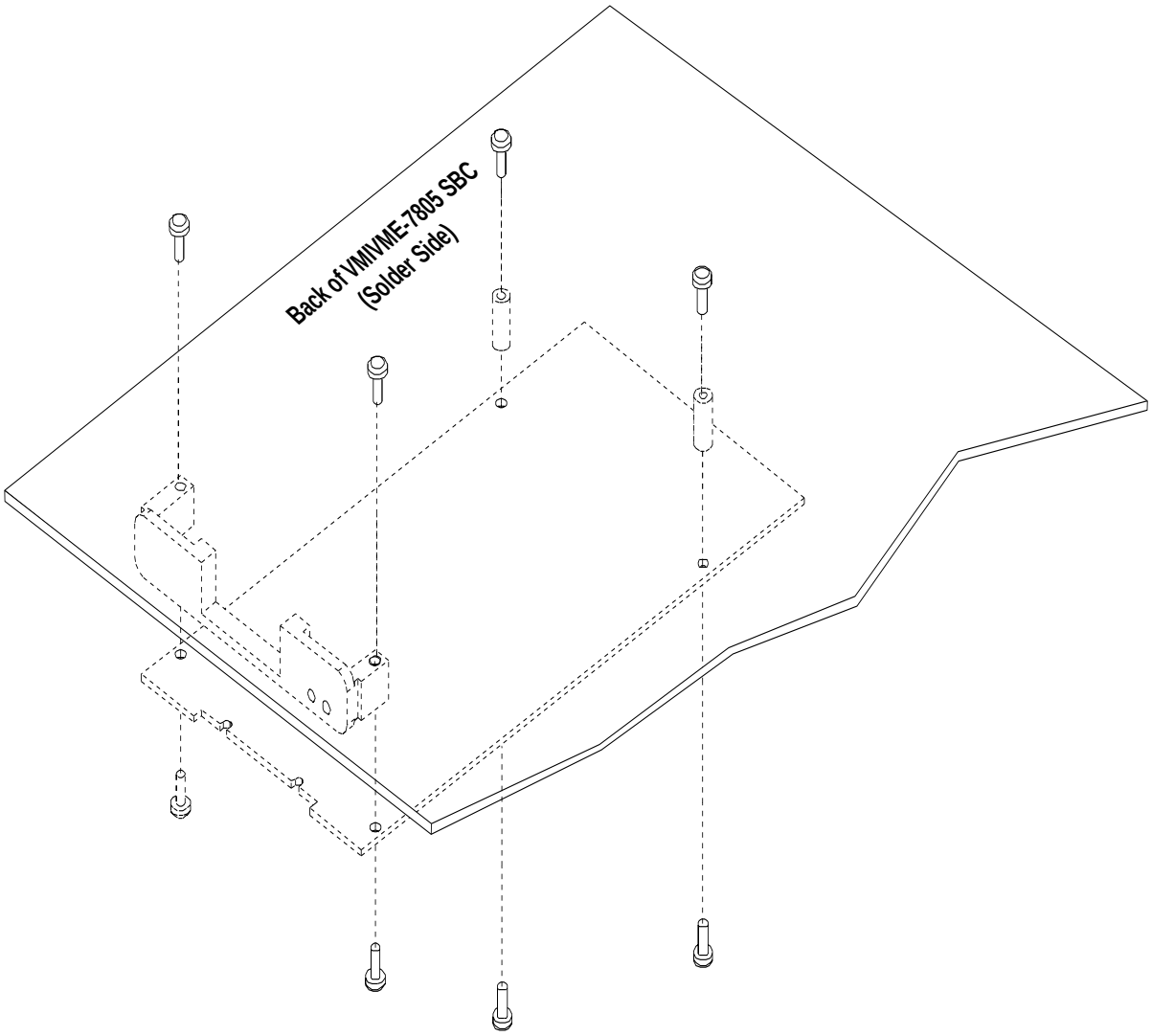


Figure 1-3 Backside Mounting for the VMIVME-7805 PMC Site

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Front/Rear Panel Connectors

The VMIVME-7805 provides front-panel access to the PMC expansion site, the DVI connector, the 10/100 and Gigabit Ethernet connectors, the manual reset switch, COM ports 1 and 2, one USB port and the status LEDs. A drawing of the VMIVME-7805 front-panel is shown in Figure 1-4. The front-panel connectors and indicators are labeled as follows:

- GBE Gigabit Ethernet connector
- 10/100 10/100 Mbit Ethernet connector
- DVI DVI video connector
- RST Manual reset switch
- COM 1:2 Two COM ports
- M/K Combination mouse/keyboard connector
- USB USB connector
- RPIB Status LEDs

The VMIVME-7805 provides rear I/O support for the following: PMC, IDE drive and floppy drive. These signals are accessed by the use of a rear-panel transition board such as the VMIACC-0562, which terminates into industry standard connectors.

The front panel connectors, including connector pinouts and orientation, for the VMIVME-7805 are defined in Appendix A. Rear panel connections are defined in the appropiate rear panel transition utility board Installation Guide. See the VMIVME-7805 product specification for compatible rear panel transistion utility boards offered by VMIC.

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LED Definition

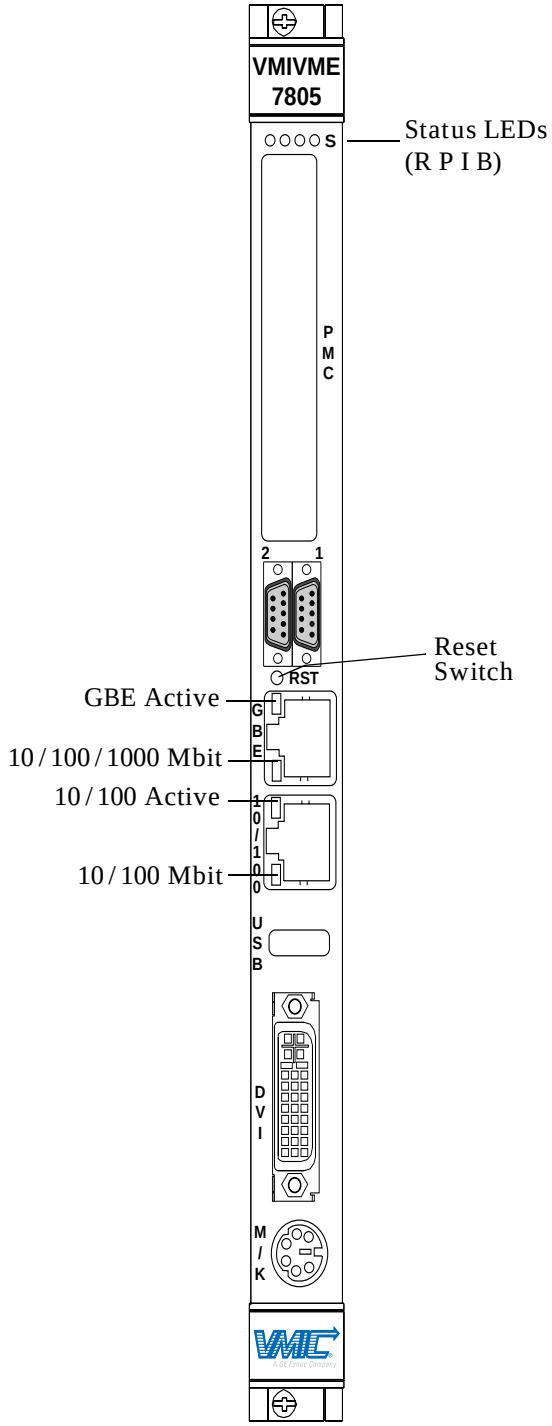


Figure 1-4 Front Panel LED Positions

LED R	*Reset* - Lights during reset condition, (Red LED).
LED P	*Power* - Indicates when power is applied to the board, (Green LED). This LED also indicates throttling by blinking slowly.
LED I	*IDE Indicator* - Indicates when IDE activity is occurring, (Yellow LED).
LED B	*Booting* - Indicates BIOS Boot is in progress. When LED is off, CPU has finished POST and is ready, (Red LED). Once booting has completed, any VMEbus 'SYSFAILS' will be indicated by this LED.
Reset Switch	*Reset* - Allows the system to be reset from the front panel.
GBE Active	Indicates the Ethernet is active, (Yellow LED).
10 / 100 / 1000 Mbit	Indicates whether 10, 100 or 1000 Mbit Ethernet mode. OFF indicates 10BaseT, Yellow indicates 100BaseTx and Green LED indicates 1000BaseT.
10 / 100 Active	Indicates the Ethernet is active, (Yellow LED).
10 / 100 Mbit	Indicates whether 10BaseT or 100BaseTx mode. OFF indicates 10BaseT, and Yellow LED indicates 100BaseTx.

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In addition, the front-panel LEDs are used to indicate various modes of operational status that can occur with the VMIVME-7805. The table below is a summary of these indications.

Table 1-8 Status Indications

State	Indication
Board is in Reset	"LAN 10BaseT / 100BaseT" LED rapidly alternates Yellow / Green and the Red "Reset" LED is illuminated.
CPU Not Present	Green "Power" LED is illuminated and the Red "Reset" LED flashes at a rapid rate.
VMEbus SYSFAIL	Red "B" LED illuminates with each VME SYSFAIL 'seen' on the bus. The LED will remain on as long as the failure lasts.
VRM Failure	Green "Power" LED is off and the Red "Reset" LED flashes at a rapid rate.
Normal Operation	LED R = Off (out of reset) LED P = On (power is good) LED I = Off, or Flashing (IDE activity) LED B = Off (boot completed)

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BIOS Setup

The VMIVME-7805 has an on-board BIOS Setup program (AMI) that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's 'CMOS Configuration'. The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

The VMIVME-7805 is shipped from the factory with hard drive type configuration set to AUTO in the CMOS.

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CHAPTER
2

Standard Features

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Physical Memory 38
Memory and Port Maps 39
I/O Port Map 40
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Integrated Peripherals. 49
Ethernet Controllers 50
Video Graphics Adapter 51
Universal Serial Bus. 53

Introduction

The VMIVME-7805 is an Intel Pentium 4 Processor-M based single board computer compatible with modern industry standard desktop systems. The VMIVME-7805 therefore retains industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB port, IDE drives, floppy drives, video controller and Ethernet controller) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the VMIVME-7805.

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CPU Socket

The VMIVME-7805 CPU socket is factory populated with a high-speed Pentium 4 Processor-M CPU. The CPU speed and RAM/flash size are user specified as part of the VMIVME-7805 ordering information.

To change CPU speeds, RAM size or flash size contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Care is available at: 1-800-240-7782.

Physical Memory

The VMIVME-7805 provides DDR Synchronous DRAM (SDRAM) as on-board system memory. Memory can be accessed as bytes, words or longwords.

The VMIVME-7805 accepts two PC2100 DDR SDRAM SODIMMs for a maximum capacity of 1 Gbyte. The on-board SDRAM is dual-ported to the VMEbus through the PCI-to-VMEbus bridge and is addressable by the local processor, as well as the VMEbus slave interface by another VMEbus master. Caution must be used when sharing memory between the local processor and the VMEbus to prevent a VMEbus master from overwriting the local processor's operating system.

NOTE: When using the Configure utility of VMIC's IOWorks Access to configure RAM, do not request more than 25 percent of the physical RAM. Exceeding the 25 percent limit may result in known bugs that causes unpredictable behavior during the boot sequence, and requires the use of an emergency repair disk to restore the computer. It is recommended that an emergency repair disk be kept up-to-date and easily accessible.

The VMIVME-7805 includes 32 Kbyte of non-volatile SRAM which can be accessed by the CPU at any time, and is used to store system data that must not be lost during power-off conditions.

NOTE: Memory capacity may be extended as parts become available.

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Memory and Port Maps

Memory Map - Tundra Universe II-Based PCI-to-VMEbus Bridge

The memory map for the Tundra Universe II-based interface VMIVME-7805 is shown in Table 2-1. All systems share this same memory map, although a VMIVME-7805 with less than the full 256 Mbyte of SDRAM does not fill the entire space reserved for On-Board Extended Memory.

Table 2-1 VMIVME-7805, Universe II-Based Interface Memory Address Map

MODE	MEMORY ADDRESS RANGE	SIZE	DESCRIPTION
PROTECTED MODE	$FFFF 0000 - $FFFF FFFF	64 Kbyte	ROM BIOS Image
	$0400 0000 - $FFFE FFFF	3.9 Gbyte	Unused *
	$0010 0000 - $0FFF FFFF	255 Mbyte	Reserved for ** On-Board Extended Memory (not filled on all systems)
REAL MODE	$E0000 - $FFFFF	128 Kbyte	Reserved for BIOS Area
	$D8018 - $DFFFF	32 Kbyte	
	$D8016 - $D8017	2 bytes	
	$D8014 - $D8015	2 bytes	
	$D8010 - $D8013	2 bytes	
	$D800E - $D800F	2 bytes	
	$D8000 - $D800D	14 bytes	
	$C8000 - $D7FFF	64 Kbyte	
	$C0000 - $C7FFF	32 Kbyte	
	$A0000 - $BFFFF	128 Kbyte	
	$00000 - $9FFFF	640 Kbyte	

* This space can be used to set up protected mode PCI-to-VMEbus windows (also referred to as PCI slave images). BIOS will also map on-board PCI based NVRAM, Timers and Watchdog Timers in this area.

** This space can be allocated as shared memory (for example, between the Pentium processor-based CPU and VMEbus Master). Note that if a PMC board is loaded, the expansion BIOS may be placed in this area.

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I/O Port Map

Like a desktop system, the VMIVME-7805 includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64 Kbyte I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 2-2.

Table 2-2 VMIVME-7805 I/O Address Map

I/O Address Range	Size In Bytes	HW Device	PC/AT Function
$000 - $00F	16		DMA Controller 1
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, System Configuration
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2

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Table 2-2 VMIVME-7805 I/O Address Map (Continued)

I/O Address Range	Size In Bytes	HW Device	PC/AT Function
$0E0 - $16F	142		Reserved
$170 - $177	8	ICH2	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	ICH2	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip*	LPT2 Parallel I/O*
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super-I/O Chip	Secondary Floppy Disk Controller
$378 - $37F	8	Super-I/O Chip*	LPT1 Parallel I/O*
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Super-I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF	256		Reserved
$500 - CFF	2048		Reserved

* While these I/O ports are reserved for the listed functions, they are not implemented on the VMIVME-7805. They are listed here to make the user aware of the standard PC usage of these ports.

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Interrupts

System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-3 along with their functions. Table 2-4 on page 43 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 2-4 on page 43.

The interrupt hardware implementation on the VMIVME-7805 is standard for computers built around the PC architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 2-1 on page 47.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 2-3 Interrupt Line Assignments

IRQ	AT Function	Comments
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by VMIVME-7805 PCI bus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2	
4	COM1	
5	Unused	
6	Floppy Controller	
7	Unused	
8	Real-Time Clock	
9	Old IRQ2	SVGA or Network I/O
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	
14	AT Hard Drive	
15	Flash Drive	

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Table 2-4 Interrupt Vector Table

Interrupt No.		IRQ Line	Real Mode	Protected Mode
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VME Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Unassigned	Unassigned
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	Unassigned	Unassigned
10	16		BIOS Video I/O	Coprocessor Error
11	17		System Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode

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Table 2-4 Interrupt Vector Table (Continued)

Interrupt No.		IRQ Line	Real Mode	Protected Mode
HEX	DEC			
1A	26		Time of Day	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-6F	103-111		Reserved by DOS	Same as Real Mode
70	112	IRQ8	Real Time Clock	
71	113	IRQ9	Redirect to IRQ2	
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	

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Table 2-4 Interrupt Vector Table (Continued)

Interrupt No.		IRQ Line	Real Mode	Protected Mode
HEX	DEC			
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	AT Hard Drive	
77	119	IRQ15	Flash Drive	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 2-1 on page 47 depicts the VMIVME-7805 interrupt logic pertaining to VME operations and the PMC site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the VMEbus interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

PCI Device Interrupt Map

The PCI bus-based external devices include the PMC sites, Ethernet controller and the PCI-to-VMEbus bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the ICH2. This mapping is illustrated in Figure 2-1 on page 47 and is defined in Table 2-5.

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The device PCI interrupt lines (INTA through INTD) that are present on each device *cannot* be modified.

Table 2-5 PCI Device Interrupt Mapping by the BIOS

Device	Component	Vendor ID	Device ID	CPU Address Map ID Select	PCI IRQ	Arbitration Request Line
PCI-to-VME Bridge	Tundra Universe IIB	0x10E3	0x0000	AD19	INTA	REQ0
Timer / SRAM FPGA	VMIC Proprietary	0x114A	0x6504	AD20	INTE	N / A
PMC	N / A	N / A	N / A	AD31	INTC	REQ2
Ethernet Controller	Intel 82540EM	0x8086	0x1209	AD22	INTB	REQ1
PCI Host Bridge	GMCH	0x8086	0x1130	N / A	N / A	N / A
VGA Controller	GMCH	0x8086	0x1132	N / A	N / A	N / A
PCI-LPC Bridge	ICH4	0x8086	0x2440	N / A	N / A	N / A
VGA Controller	ICH4	0x8086	0x2442	N / A	N / A	N / A
USB Controller #1	ICH4	0x8086	0x2443	N / A	N / A	N / A
SMBus Controller	ICH4	0x8086	0x2444	N / A	N / A	N / A
LAN Controller	ICH4	0x8086	0x2449	N / A	N / A	N / A
USB Controller #2	ICH4	0x8086	0x244B	N / A	N / A	N / A
PCI-to-Hub Bridge	ICH4	0x8086	0x244B	N / A	N / A	N / A

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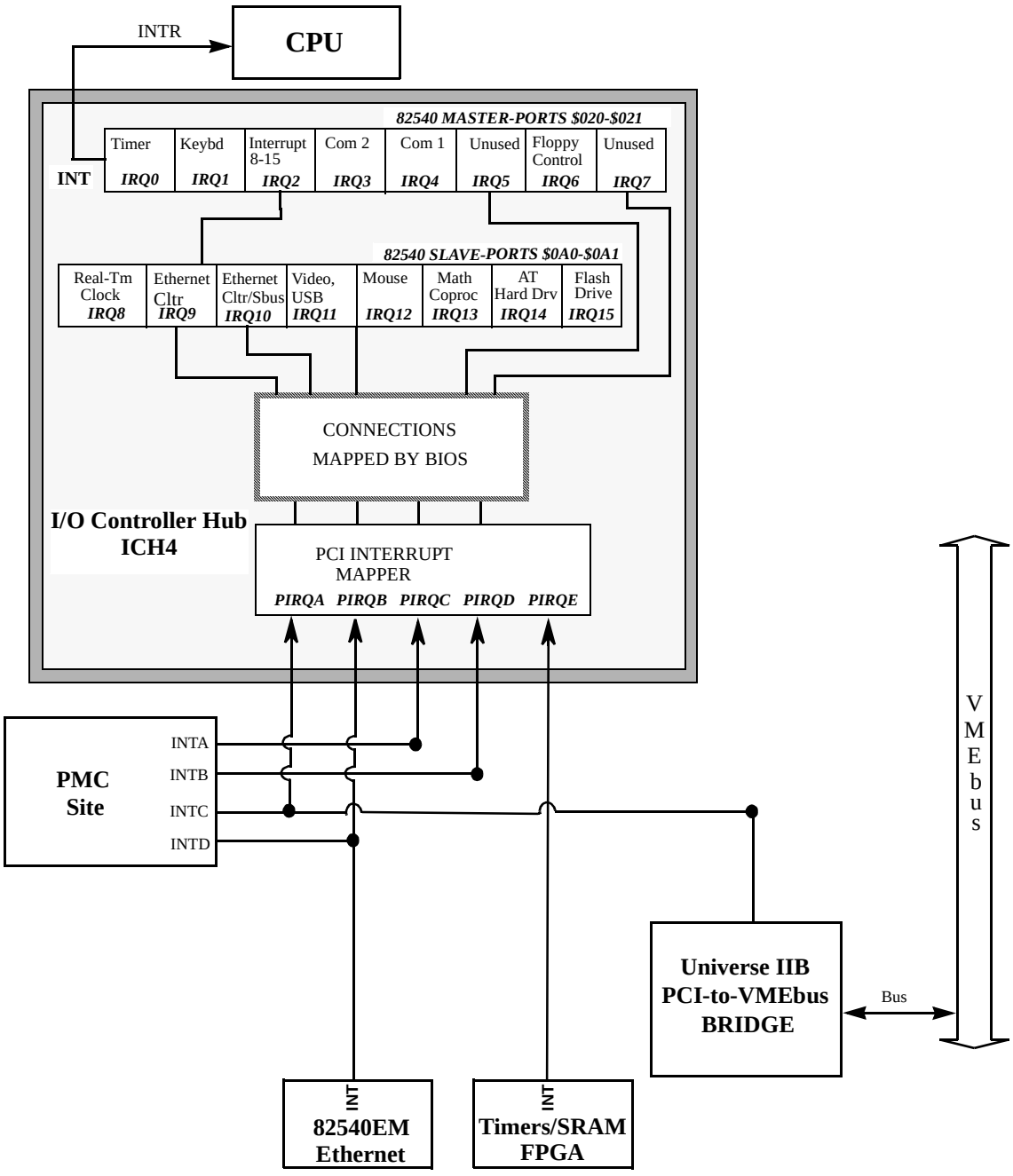


Figure 2-1 Connections for the PC Interrupt Logic Controller

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The PCI-to-VMEbus Bridge has the capability of generating a Non-Maskable Interrupt (NMI) via the PCI SERR# line. Table 2-6 describes the register bits that are used by the NMI. The SERR interrupt is routed through logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable / disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable / enable all NMI sources.

Table 2-6 NMI Register Bit Descriptions

Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set Bit 2 to 0 and then set it to 1. When writing to port $061, Bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read/Write) - 1 = Clear and Disable, 0 = Enable
Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

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Integrated Peripherals

The VMIVME-7805 incorporates a National Semiconductor Super I/O (SIO) chip. The SIO provides the VMIVME-7805 with a standard floppy drive controller, two 16550 UART-compatible serial ports, keyboard and mouse ports and general purpose I/O for system monitoring functions. Both serial port signals are available from the front panel. The floppy signals are available via the VME backplane connectors and can be accessed with the appropriate transition utility board (VMIACC-0562).

The IDE interface is provided by the Intel I/O Controller Hub (ICH4) chip. The IDE interface supports two channels known as the primary and secondary channels. The secondary channel is routed on-board to the optional compact flash socket. The primary channel is routed out the VME backplane to a VMIACC-0562 transition utility board which terminates into a standard 40-pin header. This channel can support two drives, a master and slave. The IDE interface on the VMIVME-7805 supports ATA-33, ATA-66 and ATA-100 drives and automatically determines the proper operating mode based on the type of drive used. In order to properly function in the ATA-100 mode, a special 80 conductor cable must be used instead of the standard 40 conductor cable. This cable is typically available from the ATA-100 drive manufacturer.

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Ethernet Controllers

The VMIVME-7805 supports Ethernet LANs with two Intel Ethernet controllers (one 82540EM Gigabit Ethernet controller and the other internal to Intel's chipset ICH4). 10BaseT, 100BaseTX and Gbit Ethernet options are supported via one front panel RJ-45 connector. 10BaseT and 100BaseTX is supported via a second RJ-45 connector.

10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ-45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters.

100BaseTx

The VMIVME-7805 also supports the 100BaseTx Ethernet. A network based on a 100BaseTx standard uses unshielded twisted-pair cables and a RJ-45 connector. 100BaseTx has a maximum length of 100 meters.

1000BaseT

The VMICPCI-7761 supports Gigabit Ethernet offering speeds of 1000 Mbps. It is fully compatible with existing Ethernets, as it uses the same CSMA/CD and MAC protocols. 1000BaseT has a maximum length of 3000 meters using Single-mode Fiber-Optic cables.

Boot ROM BIOS

The VMIVME-7805 supports booting on either LAN1 or LAN2 using a ROM Ethernet BIOS. Refer to *Argon BIOS* on page 107 for more information on remote Ethernet booting.

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Video Graphics Adapter

High-resolution graphics and multimedia-quality video are supported on the VMIVME-7805 using the 852GM (GMCH) chipset internal graphics controller. Screen resolutions up to 1,600 x 1,200 x 256 colors (single view mode) are supported by the graphics adapter.

Table 2-7 Partial List of Display Modes Supported

Resolution	Bits Per Pixel (Frequency in Hz)		
	8-bit Indexed	16-bit	24-bit
320 x 200	70	70	70
320 x 240	70	70	70
352 x 480	70	70	70
352 x 576	70	70	70
400 x 300	70	70	70
512 x 384	70	70	70
640 x 400	70	70	70
640 x 480	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
720 x 480	75, 85	75, 85	75, 85
720 x 576	60, 75, 85	60, 75, 85	60, 75, 85
800 x 600	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
1,024 x 768	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
1,152 x 864	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 72, 75, 85
1,280 x 720	60, 75, 85	60, 75, 85	60, 75, 85
1,280 x 960	60, 75, 85	60, 75, 85	60, 75, 85
1,280 x 1,024	60, 70, 72, 75, 85	60, 70, 72, 75, 85	60, 70, 75, 85
1,600 x 900	60, 75, 85	60, 75, 85	
1,600 x 1,200	60, 70, 72, 75		

NOTE: Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 85 Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

Digital Visual Interface (DVI)

The VMIVME-7805 has a Digital Visual Interface that provides a high-speed digital connection for visual data types that are display technology independent. DVI is a display interface developed in response to the proliferation of digital flat-panel displays. For the most part, these displays are currently connected to an analog Video Graphics Array (VGA) interface and, thus, require a double conversion. The digital

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signal from the computer must be converted to an analog signal for the analog VGA interface, then converted back to a digital signal for processing by the flat-panel display. This inherently inefficient process takes a toll on performance and video quality and adds cost. In contrast, when a flat-panel display is connected to a digital interface, no digital-to-analog conversion is required.

DVI uses Silicon Image's PanelLink, a high-speed serial interface that uses Transition Minimized Differential Signaling (TMDS) to send data to the monitor. The DFP and VESA Plug and Display interfaces also use PanelLink. For this reason, DVI can work with these previous interfaces by using adapter cables (depending on the signal quality of the adapter.)

TMDS conveys data by transitioning between "on" and "off" states. An advanced encoding algorithm that uses Boolean exclusive OR (XOR) or exclusive NOR (XNOR) operations is applied to minimize the transitions. Minimizing transitions avoids excessive electromagnetic interference (EMI) levels on the cable. An additional operation is performed to balance the DC signal.

DVI also supports the VESA Display Data Channel (DDC) and the Extended Display Identification Data (EDID) specifications. DDC is a standard communications channel between the display adapter and monitor. EDID is a standard data format containing monitor information such as vendor information, monitor timing, maximum image size, and color characteristics. EDID information is stored in the display and is communicated over the DDC. EDID and DDC enable the system, display and graphics adapter to communicate so that the system can be configured to support specific features available in the display.

DVI Connectors

The DVI connector has 24 pins that can accommodate up to two TMDS links and the VESA DDC and EDID services. The DVI specification defines two types of connectors (see Figure 1):

- DVI-Digital (DVI-D) supports digital displays only (not supported)
- DVI-Integrated (DVI-I) supports digital displays and is backward compatible with analog displays (used on the VMIVME-7805)

The VMIVME-7805 uses the DVI-I connector with a single TMDS link. The DVI-I interface accommodates a 12- or 24-pin DVI plug connector or a new type of analog plug connector that uses four additional pins, plus a ground plane plug to maintain a constant impedance for the analog RGB signals. The DVI-I adapter is supplied by VMIC.

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Universal Serial Bus

The VMIVME-7805 provides a single Universal Serial Bus (USB) connection on the front panel. The on-board USB controller supports the standard USB interface Rev. 2.0.

The USB Host Controller moves data between system memory and the USB by processing and scheduling data structures. The controller executes the scheduled lists, and reports status back to the system.

NOTE: Default CMOS settings of the VMIVME-7805 have USB functions disabled. This allows more interrupts and less Interrupt Latency for Real Time system. If USB is enabled, the user must be aware that Interrupt Sharing and Latency will be affected.

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CHAPTER 3

Embedded PC/RTOS Features

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Introduction

VMIC's VMIVME-7805 features additional capabilities beyond those of a typical desktop computer system. The unit provides four software-controlled, general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The VMIVME-7805 also provides a bootable Flash Disk system and 32 Kbyte of non-volatile SRAM. Also, the VMIVME-7805 supports an embedded intelligent VMEbus bridge to allow compatibility with the most demanding VMEbus applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used. The VMIVME-7805 also supports I^2C by integrating specialized circuitry for these functions.

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VMEbus Bridge

In addition to its PC / AT functions, the VMIVME-7805 has the following VMEbus features:

- Complete six-line Address Modifier (AM-Code) programmability
- VME data interface with separate hardware byte / word swapping for master and slave accesses
- Support for VME64 multiplexed MBLT 64-bit VMEbus block transfers
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VMEbus arbiter (PRI, SGL and RRS modes are supported)
- VMEbus BERR bus error timer (software programmable)
- Slave access from the VMEbus to local RAM and mailbox registers
- Full-featured programmable VMEbus requester (ROR, RWD and BCAP modes are supported)
- System Controller auto detection
- Complete VMEbus master access through five separate Protected-mode memory windows

The VMIVME-7805 supports High Throughput DMA transfers of bytes, words and longwords in both Master and Slave configurations.

If Endian conversion is not needed, VMIC offers a special “Bypass” mode that can be used to further enhance throughput (not available for byte transfers).

The VMIVME-7805 VMEbus interface is provided by the PCI-to-VMEbus bridge built around the Tundra Semiconductor Corporation Universe II VMEbus interface chip. The Universe II provides a reliable high-performance 64-bit VMEbus-to-PCI interface in one design. The functions and programming of the Universe-based VMEbus interface are addressed in detail in a companion manual titled: *VMIC’s Tundra Universe II Based VMEbus Interface Product Manual (500-000211-000).*

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I²C Support

The VMIVME-7805 supports the I²C-bus and can operate as an I²C-bus master or slave per the I²C-bus specification, version 2.0, developed by Philips Semiconductor. Communication over the I²C-bus is accomplished through the use of the National Semiconductor Super I/O I²C-bus controller. This controller is capable of communicating on the I²C-bus on a byte-wise basis using interrupt or polled handshaking and supports a programmable clock rate when operating in Master mode. The I²C-bus signals are available through the VMIVME-7805's E17 header as shown in Table 3-1.

Table 3-1 I²C-bus Through E17

Signal Name	Pin
+5.0V	1
I2C_SDA	2
I2C_SCL	3
GND	4

The VMIVME-7805 provides termination on the I²C signals.

The controller can issue interrupts to the VMIVME-7805 when handshaking on the I²C-bus. When the I²C-bus controller drives the interrupt active, software must service and then clear the interrupt. Software can determine the cause of the interrupt by reading the bit of the status register.

For more information related to programming the I²C-bus controller, see the section "Access, Bus Interface (ACB)" in the *"PC87366 128-pin LPC Super I/O with System Hardware Monitoring and MIDI and Game Ports"* datasheet available from National Semiconductor.

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Embedded PCI Functions

The VMIVME-7805 provides non-volatile RAM (NVRAM), Timers and a Watchdog Timer via the PCI bus. These functions are required for embedded and real time applications. The PCI configuration space of these embedded functions are shown below.

Table 3-2 PCI Configuration Space Registers

31	16	15	00	Register Address
Device ID 0004		Vendor ID 114A		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
PCI Base Address 0 for Memory-Mapped VMEbus Control registers (BAR0)				10h
PCI Base Address 1 for Memory-Mapped 32kB NVRAM (BAR1)				14h
PCI Base Address 2 for memory-mapped Watchdog and other timers (BAR2)				18h
Reserved				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID 7805		Subsystem Vendor ID 114A		2Ch
Reserved				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_gnt	Interrupt Pin	Interrupt Line	3Ch

The “Device ID” field indicates that the device is for VMEbus products (00) and indicates the supported embedded feature set.

The “Vender ID” and “Subsystem Vendor ID” fields indicate VMIC’s PICMG assigned Vender ID (114A).

The “Subsystem ID” field indicates the model number of the product (7805).

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Timers

General

The VMIVME-7805 provides four user-programmable timers (two 16-bit and two 32-bit) which are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2MHz, 1MHz, 500kHz and 250kHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

Timer Control Status Register 1 (TCSR1)

The timers are controlled and monitored via the Timer Control Status Register 1 (TCSR1) located at offset 0x00 from the address in BAR2. The mapping of the bits in this register are as follows:

Field	Bits	Read or Write
Timer 1 Caused IRQ	TCSR1[0]	R/W
Timer 1 Enable	TCSR1[1]	R/W
Timer 1 IRQ Enable	TCSR1[2]	R/W
Timer 1 Clock Select	TCSR1[4..3]	R/W
Timer 2 Caused IRQ	TCSR1[8]	R/W
Timer 2 Enable	TCSR1[9]	R/W
Timer 2 IRQ Enable	TCSR1[10]	R/W
Timer 2 Clock Select	TCSR1[12..11]	R/W
Timer 3 Caused IRQ	TCSR1[16]	R/W
Timer 3 Enable	TCSR1[17]	R/W
Timer 3 IRQ Enable	TCSR1[18]	R/W
Timer 3 Clock Select	TCSR1[20..19]	R/W
Timer 4 Caused IRQ	TCSR1[24]	R/W
Timer 4 Enable	TCSR1[25]	R/W
Timer 4 IRQ Enable	TCSR1[26]	R/W
Timer 4 Clock Select	TCSR1[28..27]	R/W
Reserved	All Other Bits	R/W

All of these bits default to "0" after system reset.

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Each timer has an independently selectable clock source which is selected by the bit pattern in the “Timer x Clock Select” field as follows:

Clock Rate	MSb	LSb
2MHz	0	0
1MHz	0	1
500kHz	1	0
250kHz	1	1

Each timer can be independently enabled by writing a “1” to the appropriate “Timer x Enable” field. Similarly, the generation of interrupts by each timer can be independently enabled by writing a “1” to the appropriate “Timer x IRQ Enable” field.

If an interrupt is generated by a timer, the source of the interrupt may be determined by reading the “Timer x Caused IRQ” fields. If the field is set to “1”, then the respective timer caused the interrupt. Note that multiple timers can cause a single interrupt. Therefore, the status of all timers must be read to ensure that all interrupt sources are recognized.

A particular timer interrupt can be cleared by writing a “0” to the appropriate “Timer x Caused IRQ” field. Alternately, a write to the appropriate Timer x IRQ Clear (TxIC) register will also clear the interrupt. When clearing the interrupt using the “Timer x Caused IRQ” fields, note that it is very important to ensure that a proper bit mask is used so that other register settings are not affected. The preferred method for clearing interrupts is to use the “ Timer x IRQ Clear” registers described on page 63.

Timer Control Status Register 2 (TCSR2)

The timers are also controlled by bits in the Timer Control Status Register 2 (TCSR2) located at offset 0x04 from the address in BAR2. The mapping of the bits in this register are as follows:

Field	Bits	Read or Write
Read Latch Select	TCSR2[0]	R/W
Reserved	All Other Bits	R/W

All of these bits default to “0” after system reset.

The “Read Latch Select” bit is used to select the latching mode of the programmable timers. If this bit is set to “0”, then each timer output is latched upon a read of any one of its address. For example, a read to the TMRCCR12 register latches the count of timers 1 and 2. A read to the TMRCCR3 register latches the count of timer 3. This continues for every read to any one of these registers. As a result, it is not possible to

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capture the values of all four timers at a given instance in time. However, by setting this bit to “1”, all four timer outputs will be latched only on reads to the Timer 1 & 2 Current Count Register (TMRCCR12). Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR12 first (with a 32-bit read), followed by a read to TMRCCR3 and TMRCCR4. The first read (to the TMRCCR12 register) causes all four timer values to be latched at the same time. The subsequent reads to the TMRCCR3 and TMRCCR4 registers do not latch new count values, allowing the count of all timers at the same instance in time to be obtained.

Timer 1 & 2 Load Count Register (TMRLCR12)

Timers 1 & 2 are 16-bits wide and obtain their load count from the Timer 1 & 2 Load Count Register (TMRLCR12), located at offset 0x10 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 2 Load Count	TMRLCR12[31..16]	R/W
Timer 1 Load Count	TMRLCR12[15..0]	R/W

When either of these fields are written (either by a single 32-bit write or separate 16-bit writes), the respective timer is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 3 Load Count Register (TMRLCR3)

Timer 3 is 32-bits wide and obtains its load count from the Timer 3 Load Count Register (TMRLCR3), located at offset 0x14 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 3 Load Count	TMRLCR3[31..0]	R/W

When this field is written, Timer 3 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

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Timer 4 Load Count Register (TMRLCR4)

Timer 4 is 32-bits wide and obtains its load count from the Timer 4 Load Count Register (TMRLCR4), located at offset 0x18 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 4 Load Count	TMRLCR4[31..0]	R/W

When this field is written, Timer 4 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 1 & 2 Current Count Register (TMRCCR12)

The current count of timers 1 & 2 may be read via the Timer 1 & 2 Current Count Register (TMRCCR12), located at offset 0x20 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 2 Count	TMRCCR12[31..16]	R.O.
Timer 1 Count	TMRCCR12[15..0]	R.O.

When either field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the “Read Latch Select” bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 3 Current Count Register (TMRCCR3)

The current count of Timer 3 may be read via the Timer 3 Current Count Register (TMRCCR3), located at offset 0x24 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 3 Count	TMRCCR3[31..0]	R.O.

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When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 4 Current Count Register (TMRCCR4)

The current count of Timer 4 may be read via the Timer 4 Current Count Register (TMRCCR4), located at offset 0x28 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 4 Count	TMRCCR4[31..0]	R.O.

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x30 from the address in BAR2, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x34 from the address in BAR2, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x38 from the address in BAR2, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

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Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x3C from the address in BAR2, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a “0” to the appropriate “Timer x Caused IRQ” field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

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Watchdog Timer

General

The VMIVME-7805 provides a programmable Watchdog Timer (WDT) which can be used to reset the system if software integrity fails.

WDT Control Status Register (WCSR)

The WDT is controlled and monitored by the WDT Control Status Register (WCSR) which is located at offset 0x08 from the address in BAR2. The mapping of the bits in this register are as follows:

Field	Bits	Read or Write
SERR / RST Select	WCSR[16]	R / W
WDT Timeout Select	WCSR[10..8]	R / W
WDT Enable	WCSR[0]	R / W

All of these bits default to "0" after system reset. All other bits are reserved.

The "WDT Timeout Select" field is used to select the timeout value of the Watchdog Timer as follows:

Timeout	WCSR[10]	WCSR[9]	WCSR[8]
135s	0	0	0
33.6s	0	0	1
2.1s	0	1	0
524ms	0	1	1
262ms	1	0	0
131ms	1	0	1
32.768ms	1	1	0
2.048ms	1	1	1

The "SERR / RST Select" bit is used to select whether the WDT generates an SERR# on the local PCI bus or a system reset. If this bit is set to "0", the WDT will generate a system reset. Otherwise, the WDT will make the local PCI bus SERR# signal active.

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The “WDT Enable” bit is used to enable the Watchdog Timer function. This bit must be set to “1” in order for the Watchdog Timer to function. Note that since all registers default to zero after reset, the Watchdog Timer is always disabled after a reset. The Watchdog Timer must be re-enabled by the application software after reset in order for the Watchdog Timer to continue to operate. Once the Watchdog Timer is enabled, the application software must refresh the Watchdog Timer within the selected timeout period to prevent a reset or SERR# from being generated. The Watchdog Timer is refreshed by performing a write to the WDT Keepalive register (WKPA). The data written is irrelevant.

WDT Keepalive Register (WKPA)

When enabled, the Watchdog Timer is prevented from resetting the system by writing to the WDT Keepalive Register (WKPA) located at offset 0x0C from the address in BAR2 within the selected timeout period. The data written to this location is irrelevant.

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NVSRAM

The VMIVME-7805 provides 32KBytes of non-volatile SRAM. This memory is mapped in 32K of address space starting at the address in BAR1. This memory is available at any time and supports byte, short word and long word accesses from the PCI bus. The contents of this memory is retained when the power to the board is removed.

VMEbus Control

The following table shows the register definitions for the VMIVME-7805 (offset from BAR0).

Table 3-3 Register Definitions Offset From BAR0

Register Name	**Offset**	
VMECOMM	0x00	
Bit Name	**Bit**	**Definition**
MEC_SEL	0	Master big-endian enable bit 1=Big Endian 0=Little Endian bit
SEC_SEL	1	Slave Big-Endian enable bit 1=Big Endian 0=Little Endian
ABLE	2	Auxiliary BERR logic enable bit 1=Aux. BERR enabled 0=Aux. BERR disabled
BTO	3	Bus error timer enabled 1=enabled 0=disabled
BTOV [1:0]	5:4	Timeout value
		00 - 16uS
		01 - 64uS
		10 -256uS
		11 - 1.00mS
BERRI	6	BERR interrupt enable 1=Interrupt enabled 0=Interrupt disabled
BERRST	7	BERR status read / clear bit 1=Clear BERR status 0=Do nothing
SFENA	8	Enables generation of VME SYSFAIL upon WDT timeout 1= Enable SYSFAIL generation 0=Disable

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Table 3-3 Register Definitions Offset From BAR0 (Continued)

Register Name	Offset	
Unused	9	Not Used
BPENA	10	Endian conversion bypass bit 1 = bypass 0 = not bypassed
VBENA	11	VMEbus enable bit 1 = enabled 0 = disabled
Unused	31:12	Not Used
VBAR	**0x04**	
VME_ADDR	All	Latched VME Address
VBAM	**0x08**	
VME_ADDR	5:0	Latched VME Address Modifier
Unused	31:6	Not Used
SEC_SEL	0x001	

Please refer to Table 3-2, “PCI Configuration Space Registers,” on page 58 for more information concerning BAR0.

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Flash Disk

The VMIVME-7805 features an optional on-board Compact Flash mass storage system with a capacity of up to 512 Mbyte. This Flash Disk appears to the user as an intelligent ATA (IDE) disk drive with the same functionality and capabilities as a “rotating media” IDE hard drive. The VMIVME-7805 BIOS includes an option to allow the board to boot from the Flash Disk.

Configuration

The Flash Disk resides on the VMIVME-7805 as the secondary IDE bus master device (the secondary IDE bus slave device is not assignable). The default setting in the AMI BIOS ‘STANDARD CMOS SETUP’ screen is the ‘AUTO’ setting. In the AMI BIOS ‘PERIPHERAL SETUP’ screen, the secondary PCI IDE interface must be enabled for the Flash Disk to be functional. Refer to Appendix C for additional details.

Figure 3-1 maps the configuration possibilities for a typical system consisting of the VMIVME-7805 with a resident Flash Disk, a hard drive attached to the Primary IDE interface, and a floppy drive attached to the floppy interface.

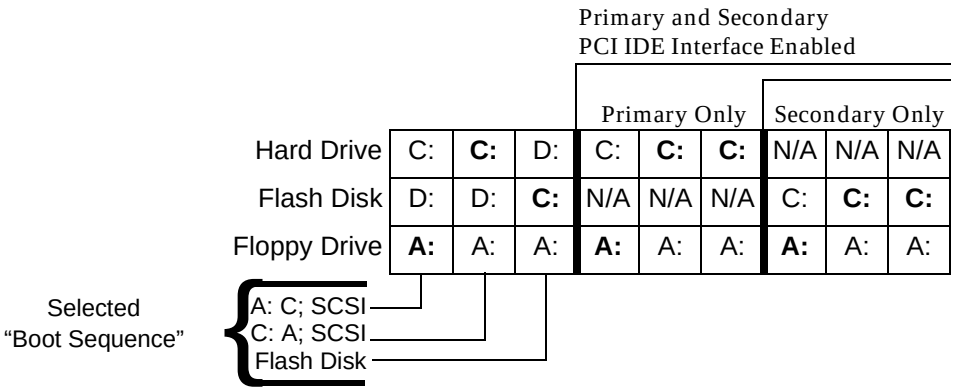


Figure 3-1 Typical System Configuration

The Primary and Secondary PCI IDE Interfaces are controlled (enabled or disabled) in the Integrated Peripheral Setup screen of the Phoenix BIOS. The First Boot Device is selected in the BIOS Features Setup screen.

Figure 3-1 identifies the drive letter assigned to each physical device, and indicates in bold lettering the device booted from in each configuration, using devices that are bootable. A bootable device is one on which an operating system has been installed, or formatted as a system disk using MS-DOS.

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Functionality

The Flash Disk performs identically to a standard IDE hard drive. Reads and writes to the device are performed using the same methods, utilizing DOS command line entries or the file managers resident in the chosen operating system.

Advanced Configuration

The previous discussion is based on using the IDE disk devices formatted as one large partition per device. Some applications may require the use of multiple partitions. The following discussion of these partitions includes special procedures that must be followed to create multiple partitions on the VMIVME-7805 IDE disk devices (including the resident Flash Disk).

Partitions may be either a primary or an extended partition. An extended partition may be subdivided farther into logical partitions. Each device may have up to four main partitions; one of which may be an extended partition. However, if multiple primary partitions are created, only one partition may be active at a time. Data in the non-active partitions are not accessible.

Following the creation of the partitioning scheme, the partitions can be formatted to contain the desired file system.

As discussed earlier, a typical system consists of the VMIVME-7805 with its resident Flash Disk configured as the Secondary IDE device, a hard drive attached to the Primary IDE interface, and a floppy drive attached to the floppy interface.

Using this configuration, it may be desirable to have a logical device on either IDE device, configured as a bootable device, allowing the selection of the first boot device by way of the Advanced CMOS Setup screen. Using this capability, a user could have a system configured with multiple operating systems that would be selectable by assigning the IDE logical device as the boot device.

The DOS utility FDISK is commonly used to configure the partition structure on a hard drive. Comments on the following page pertain to partitioning efforts using FDISK.

CAUTION: Deleting a partition will erase all the data previously stored in that partition.

The Flash Disk will be configured as a single partition device as delivered from the factory. The following sample sequence illustrates a proven method for creating two 8 Mbyte partitions, with one as an active primary partition. Take note of the instructions to exit FDISK. This has been shown to be an important step in a successful partitioning effort.

1. Power up the VMIVME-7805 and enter the CMOS set-up.
2. Set IDE HDD Master to “Not Installed”.

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3. Set Flash Disk Master to “AUTO”.
4. Set boot device to floppy.
5. Boot DOS from the floppy, and verify that the System Configuration Screen shows only the Flash Disk.
6. Run FDISK.
7. Delete all current partitions (any data currently stored in the partitions will be lost).
8. Exit FDISK (this will cause a reboot), then run FDISK again.
9. Create an 8 Mbyte primary partition.
10. Create an 8 Mbyte extended partition.
11. Set-up a logical device for the 8 Mbyte extended partition.
12. Set the Primary partition as an active partition.
13. Exit FDISK.

If an operating system has been installed on the Flash Disk that modifies the Master Boot Record (MBR), the following steps are required to rewrite the MBR for DOS.

14. Run FDISK/MBR.
15. Run FORMAT C: (use the extension /s option if you want the Flash Disk as a bootable DOS device).
16. Format D: (this is only required if two partitions were created).
17. Reset the CPU and enter the CMOS set-up.
18. Set Primary Master to “AUTO”.
19. Set boot device to desired boot source.

Drive letter assignments for a simple system are illustrated in Figure 3-1 on page 69. Understanding the order the operating system assigns drive letters is necessary for these multiple partition configurations. The operating system assigns drive letter C to the active primary partition on the first hard disk (the boot device). Drive D is assigned to the first recognized primary partition on the next hard disk. The operating system will continue to assign drive letters to the primary partitions in an alternating fashion between the two drives. The next logical partitions will be assigned drive letters starting on the first hard drive, lettering each logical device sequentially, until all are assigned a drive letter. The system will then perform the same sequential lettering of each logical partition on the second hard disk.

NOTE: Drive letter changes caused by adding an additional drive or changing the initial partitioning scheme may cause difficulties with an operating system installed prior to the changes. Plan your configuration prior to installing the operating system to minimize difficulties.

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Remote Ethernet Booting

The VMIVME-7805 is capable of booting from a server using either LAN1 or LAN2 over a network utilizing ARGON's Boot ROM BIOS. The Boot ROM BIOS gives you the ability to remotely boot the VMIVME-7805 using a variety of network protocols. The Ethernet must be connected through either LAN front panel (RJ-45) connector to boot remotely. This feature allows users to create systems without the worry of disk drive reliability, or the extra cost of adding Flash drives.

BootWare Features:

- Netware (802.1, 802.3 or EthII), TCP / IP (DHCP or BootP), RPL and PXE boot support
- Unparalleled boot sector virus protection
- Detailed boot configuration screens
- Comprehensive diagnostics
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

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Maintenance

If a VMIC product malfunctions, please verify the following:

1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

VMIC Customer Care is available at: 1-800-240-7782.
Or E-mail us at customer.service@vmic.com

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Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

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Appendix

A

Connector Pinouts

Contents

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PMC Connector Pinout 84

Introduction

The VMIVME-7805 VMEbus SBC has several connectors for its I/O ports. Wherever possible, the VMIVME-7805 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a VMEbus chassis.

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VMEbus Connector Pinout

Figure A-1 shows the location of the VMEbus P1 and P2 connectors and their orientation on the VMIVME-7805. Table A-1 shows the pin assignments for the VMEbus connectors. Note that only Row B of connector P2 is used; all other pins on P2 are reserved and should not be connected.

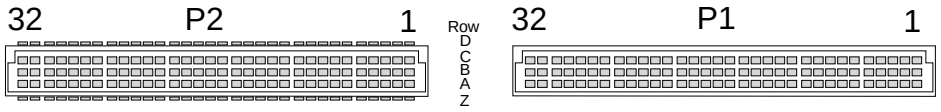


Figure A-1 VMEbus Connector Diagram

Table A-1 VMEbus Connector Pinout

Pin#	P1 Row A Signal	P1 Row B Signal	P1 Row C Signal	P2 Row Z Signal	P2 Row A Signal	P2 Row B Signal	P2 Row C Signal	P2 Row D Signal
1	D00	BBSY#	D08	CONN [2]	CBL_DETECT	+5 V	IDE RST#	CONN [1]
2	D01	BCLR#	D09	GND	PDD8	GND	PDD7	CONN [3]
3	D02	ACFAIL	D10	CONN [5]	PDD9	Reserved	PDD6	CONN [4]
4	D03	BG0IN#	D11	GND	PDD10	A24	PDD5	CONN [6]
5	D04	BG0OUT#	D12	CONN [8]	PDD11	A25	PDD4	CONN [7]
6	D05	BG1IN#	D13	GND	PDD12	A26	PDD3	CONN [9]
7	D06	BG1OUT#	D14	CONN [11]	PDD13	A27	PDD2	CONN [10]
8	D07	BG2IN#	D15	GND	PDD14	A28	PDD1	CONN [12]
9	GND	BG2OUT#	GND	CONN [14]	PDD15	A29	PDD0	CONN [13]
10	SYSCLK	BG3IN#	SYSFAIL#	GND	IDE_PDDREQ	A30	VCC_5.0	CONN [15]
11	GND	BG3OUT#	BERR#	CONN [17]	IDE_PDIOW#	A31	GND	CONN [16]
12	DS1#	BR0#	SYSRST#	GND	IDE_PDIOR#	GND	GND	CONN [18]
13	DS0#	BR1#	LWORD#	CONN [20]	IDE_PIORDY	+5 V	GND	CONN [19]
14	WRITE#	BR2#	AM5	GND	GND	D16	GND	CONN [21]
15	GND	BR3#	A23	CONN [23]	GND	D17	PDDACK#	CONN [22]
16	DTACK#	AM0	A22	GND	GND	D18	IDE IRQ14	CONN [24]
17	GND	AM1	A21	CONN [26]	PDA[1]	D19	PDA[2]	CONN [25]
18	AS#	AM2	A20	GND	PDCS1 #	D20	PDA[0]	CONN [27]

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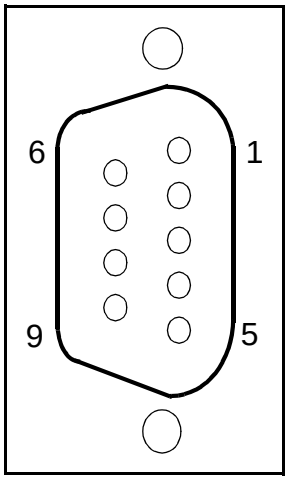
Table A-1 VMEbus Connector Pinout (Continued)

Pin#	P1 Row A Signal	P1 Row B Signal	P1 Row C Signal	P2 Row Z Signal	P2 Row A Signal	P2 Row B Signal	P2 Row C Signal	P2 Row D Signal
19	GND	AM3	A19	CONN [29]	HD_ACTA#	D21	IDE CS03#	CONN [28]
20	IACK#	GND	A18	GND	FDC_DRATE0	D22	DENSEL	CONN [30]
21	IACKIN#	N / C	A17	CONN [32]	GND	D23	INDEX#	CONN [31]
22	IACKOUT#	N / C	A16	GND	FDC_DR1#	GND	MTR0#	CONN [33]
23	AM4	GND	A15	CONN [35]	GND	D24	DR0#	CONN [34]
24	A07	IRQ7	A14	GND	GND	D25	MTR1#	CONN [36]
25	A06	IRQ6	A13	CONN [38]	GND	D26	STEP#	CONN [37]
26	A05	IRQ5	A12	GND	GND	D27	WDATA#	CONN [39]
27	A04	IRQ4	A11	CONN [41]	GND	D28	TRK0#	CONN [40]
28	A03	IRQ3	A10	GND	GND	D29	RDATA#	CONN [42]
29	A02	IRQ2	A09	CONN [44]	DSKCHG #	D30	HDSEL#	CONN [43]
30	A01	IRQ1	A08	GND	GND	D31	DIR#	CONN [45]
31	VCC_-12 V	N / C	VCC_12.0	CONN [46]	VCC_5.0	GND	WGATE#	GND
32	VCC_5.0	VCC_5.0	VCC_5.0	GND	VCC_5.0	VCC_5.0	WPT#	N / C

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Serial Connector Pinout

Each standard RS-232 serial port connector is a Microminiature DB9 male as shown in Figure A-2. Adapters to connect standard DB9 serial peripherals to the board are available. Please refer to the product specification sheet for ordering information.



COM 1 and COM 2 Serial Port Connectors			
DB9 Pin	**DIR**	**RS-232 Signal**	**Function**
1	In	DCD	Data Carrier Detect
2	In	RX	Receive Data
3	Out	TX	Transmit Data
4	Out	DTR	Data Terminal Ready
5		GND	Signal Ground
6	In	DSR	Data Set Ready
7	Out	RTS	Request to Send
8	In	CTS	Clear to Send
9	In	RI	Ring Indicator
Shield			Chassis Ground

Figure A-2 Serial Connector Pinouts

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USB Connector (J12)

The USB port uses an industry standard four-position shielded connector. Figure A-3 shows the pinout of the USB connector.



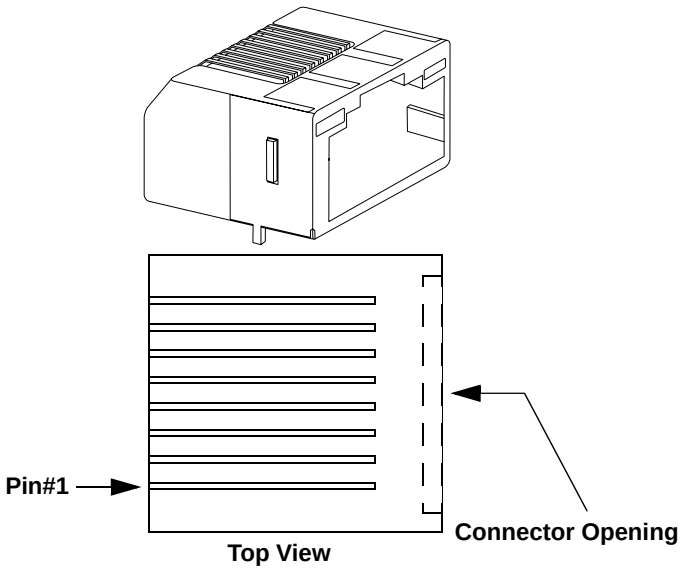
USB Connector (J12)		
Pin	**Signal**	**Function**
1	USBV	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

Figure A-3 USB Connector Pinout

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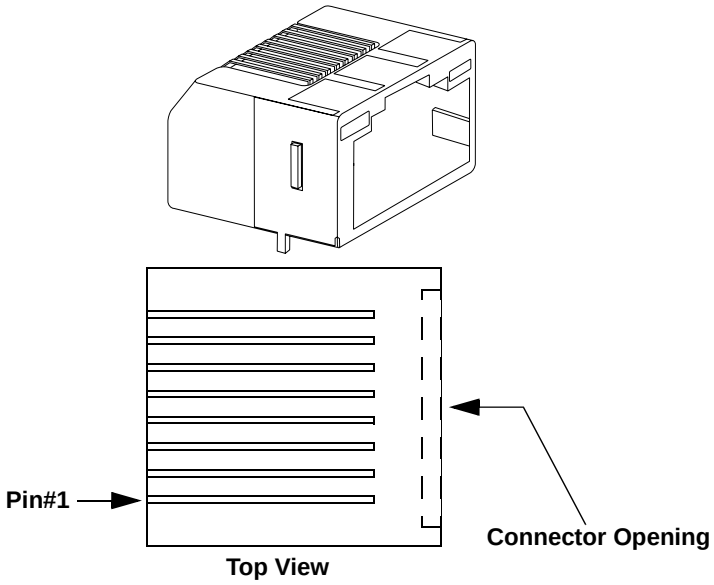
Ethernet Connector Pinout (J14 and J15)

The pinout diagram for the Ethernet 10/100 Mbit and the Gigabit Ethernet connectors are shown in Figure A-4 and Figure A-5.



J14 Ethernet Connector (10/100Mbit)		
PIN	**Signal Name**	
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	TX_CT_OUT	Transmit Center Tap Out
5	TX_CT_OUT	Transmit Center Tap Out
6	RD-	Receive Data
7	RX_CT_OUT	Receive Center Tap Out
8	RX_CT_OUT	Receive Center Tap Out

Figure A-4 10/100Mbit Ethernet Connector (J14) and Pinout



J15 Ethernet Connector (1000Mbit)		
PIN	**Signal Name**	
1	VCC	2.5VCC
2	MDI_0+	
3	MDI_0-	
4	MDI_1+	
5	MDI_1-	
6	MDI_2+	
7	MDI_2-	
8	MDI_3+	
9	MDI_3-	
10	GND	Ground

Figure A-5 Gigabit Ethernet Connector (J15) and Pinout

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DVI-I Connector and Pinout (J10)

The DVI interface accommodates a 24-pin DVI-I connector that uses four additional pins, plus a ground plane plug to maintain a constant impedance for the analog RGB signals. The DVI-I adapter is included with the VMIVME-7805.

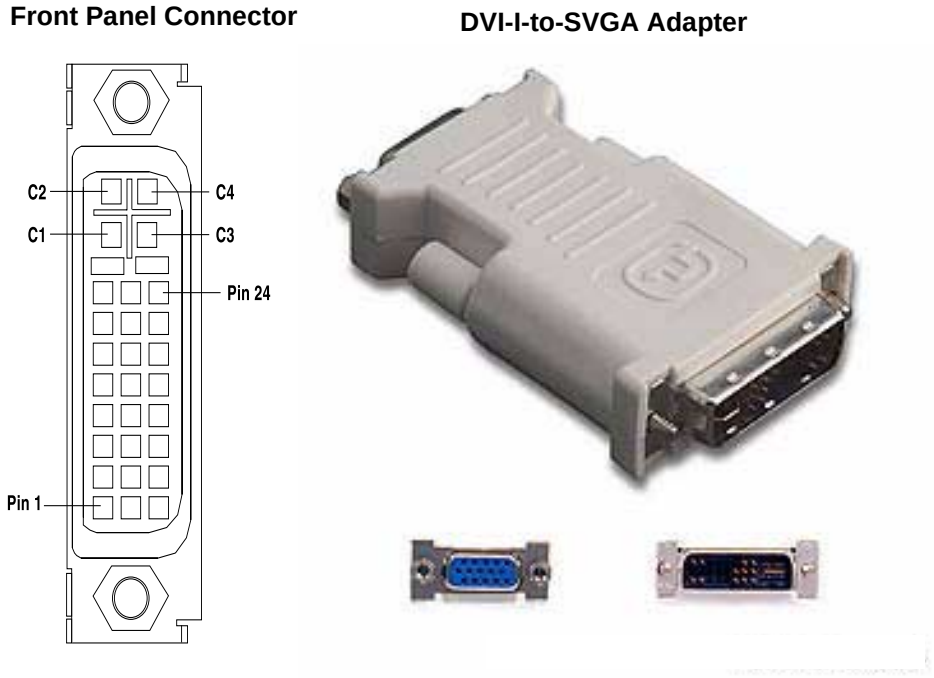


Figure A-6 DVI-I Connector and DVI-I-to-SVGA Adapter

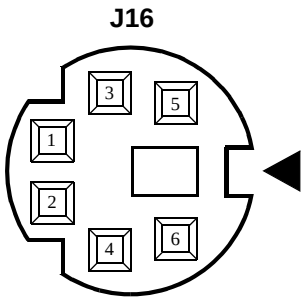
Table A-2 DVI-I Connector Pinout

Pin#	Signal Assignment	Pin#	Signal Assignment	Pin#	Signal Assignment
1	Data 2-	9	Data 1-	17	Data 0-
2	Data 2+	10	Data 1+	18	Data 0+
3	Data 2/4 Shield	11	Data 1/3 Shield	19	Data 0/5 Shield
4	N/C	12	N/C	20	N/C
5	N/C	13	N/C	21	N/C
6	DDC Clock	14	+5VDC Power (750 mA)	22	Clock Shield
7	DDC Data	15	GND (Return for +5, HSync and VSync)	23	Clock+
8	Analog VSync	16	Hot Plug Detect	24	Clock-
C1	Analog Red	C2	Analog Green	C3	Analog Blue
C4	Analog HSync	C5	Analog GND (RGB return)		

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Keyboard and Mouse Connector and Pinout (J16)

The keyboard and mouse connector are standard 6-pin female mini-DIN PS/2 connector as shown in Figure A-7 and Table A-3.



Keyboard/Mouse Connector*		
Pin	**Dir**	**Function**
1	In/Out	Mouse Data
2	In/Out	Keyboard Data
3		Ground
4		+5 V
5	Out	Mouse Clock
6	Out	Keyboard Clock
Shield		Chassis Ground
*An adapter cable is included with the VMIVME-7805 to separate the keyboard and mouse connector.		

Figure A-7 Keyboard/Mouse Connector and Pinout

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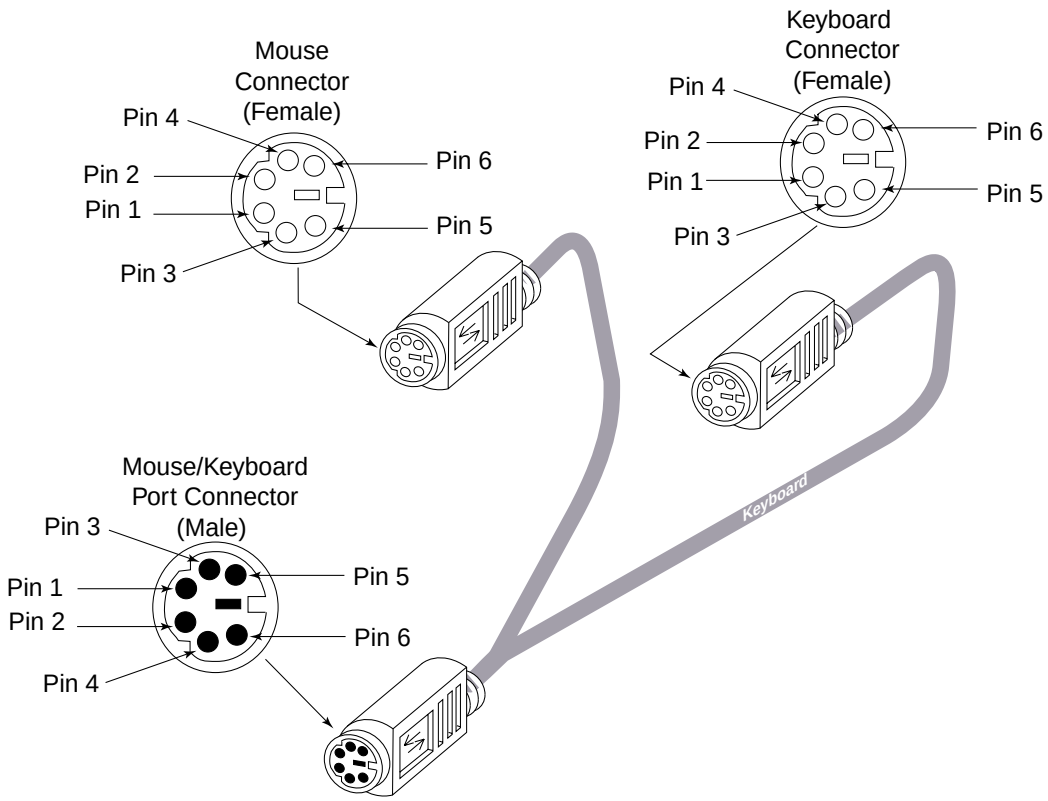


Figure A-8 Mouse/Keyboard Y Splitter Cable

Table A-3 Keyboard/Mouse Y Splitter Cable

Keyboard			Mouse		
Pin	**Dir**	**Function**	**Pin**	**Dir**	**Function**
1	In / Out	Keyboard Data	1	In / Out	Mouse Data
2		Unused	2		Unused
3		Ground	3		Ground
4		+5 V	4		+5 V
5	Out	Keyboard Clock	5	Out	Mouse Clock
6		Unused	6		Unused
Shield		Chassis Ground	Shield		Chassis Ground

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PMC Connector Pinout

PMC #1 (J1) Connector and Pinout

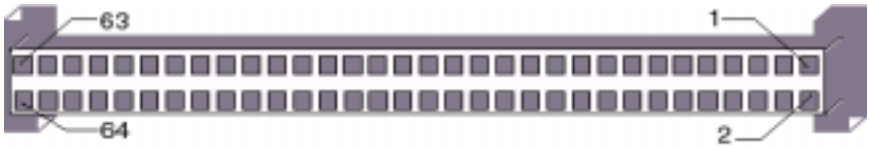


Table A-4 PMC #1 (J1) Connector Pinout

PMC Connector (J1)				PMC Connector (J1)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	+5 V	33	GND	34	NC
3	GND	4	NC	35	TRDY	36	+3.3 V
5	+5 V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3 V	42	SERR#
11	PRSNT2	12	+3.3 V	43	C/BE1#	44	GND
13	RST#	14	GND	45	AD[14]	46	AD[13]
15	+3.3 V	16	GND	47	GND	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3 V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3 V	54	NC
23	AD[24]	24	+3.3 V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3 V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3 V
31	AD[16]	32	C/BE2#	63	GND	64	NC

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PMC #1 (J2) Connector and Pinout

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-6 through A-4 are the pinouts for the PMC connectors (J1, J2 and J3).

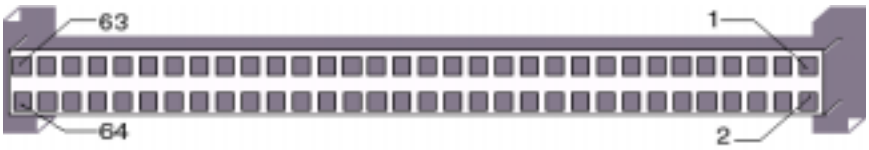


Table A-5 PMC #1 (J2) Connector Pinout

PMC Connector (J2)				PMC Connector (J2)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5 V
7	BMODE1A	8	+5 V	39	GND	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	NC
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+5 V	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	+5 V	20	AD[31]	51	GND	52	C / BE0#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C / BE3#	57	+5 V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	+5 V	32	AD[17]	63	GND	64	REQ64#

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PMC #1 (J3) Connector and Pinout

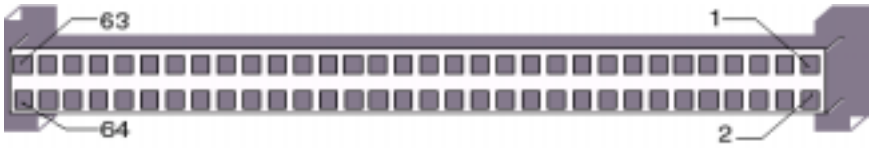


Table A-6 PMC #1 (J3) Connector Pinout

PMC Connector (J3)						PMC Connector (J3)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	CONN[1]	P2 pin D1	2	CONN[2]	P2 pin Z1	33	CONN[33]	P2 pin D22	34	CONN[34]	P2 pin D23
3	CONN[3]	P2 pin D2	4	CONN[4]	P2 pin D3	35	CONN[35]	P2 pin Z23	36	CONN[36]	P2 pin D24
5	CONN[5]	P2 pin Z3	6	CONN[6]	P2 pin D4	37	CONN[37]	P2 pin D25	38	CONN[38]	P2 pin Z25
7	CONN[7]	P2 pin D5	8	CONN[8]	P2 pin Z5	39	CONN[39]	P2 pin D26	40	CONN[40]	P2 pin D27
9	CONN[9]	P2 pin D6	10	CONN[10]	P2 pin D7	41	CONN[41]	P2 pin Z27	42	CONN[42]	P2 pin D28
11	CONN[11]	P2 pin Z7	12	CONN[12]	P2 pin D8	43	CONN[43]	P2 pin D29	44	CONN[44]	P2 pin Z29
13	CONN[13]	P2 pin D9	14	CONN[14]	P2 pin Z9	45	CONN[45]	P2 pin D30	46	CONN[46]	P2 pin Z31
15	CONN[15]	P2 pin D10	16	CONN[16]	P2 pin D11	47	CONN[47]	NC	48	CONN[48]	NC
17	CONN[17]	P2 pin Z11	18	CONN[18]	P2 pin D12	49	CONN[49]	NC	50	CONN[50]	NC3
19	CONN[19]	P2 pin D13	20	CONN[20]	P2 pin Z13	51	CONN[51]	NC	52	CONN[52]	NC
21	CONN[21]	P2 pin D14	22	CONN[22]	P2 pin D15	53	CONN[53]	NC	54	CONN[54]	NC
23	CONN[23]	P2 pin Z15	24	CONN[24]	P2 pin D16	55	CONN[55]	NC	56	CONN[56]	NC
25	CONN[25]	P2 pin D17	26	CONN[26]	P2 pin Z17	57	CONN[57]	NC	58	CONN[58]	NC
27	CONN[27]	P2 pin D18	28	CONN[28]	P2 pin D19	59	CONN[59]	NC	60	CONN[60]	NC
29	CONN[29]	P2 pin Z19	30	CONN[30]	P2 pin D20	61	CONN[61]	NC	62	CONN[62]	NC
31	CONN[31]	P2 pin D21	32	CONN[32]	P2 pin Z21	63	CONN[63]	NC	64	CONN[64]	NC

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Appendix

B

BIOS Setup Utility

Contents

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PCI/PnP Setup 91
Boot Setup 92
Security Setup 93
Chipset Setup 94
Exit Menu 95

Introduction

This appendix gives a brief description of the setup options in the system BIOS. Due to the custom nature of VMIC's Single Board Computers, your BIOS options may vary from the options discussed in this appendix.

AMI refers to their BIOS setup screens as ezPORT. For a complete description of all the options available with the AMI BIOS, please visit www.ami.com and download their ezPORT PDF file. The options listed on AMI's web site may not be available on your system.

To Access the First Boot setup screen press the F11 key at the beginning of boot.

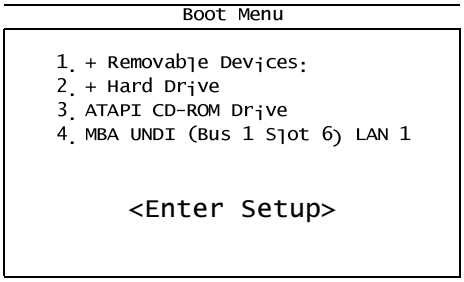
To access the ezPORT setup screens, press the DEL key at the beginning of boot.

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First Boot

The VMIVME-7805 has a First Boot menu enabling the user to, on a one time basis, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing Windows XP from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the ESC key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system. If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.



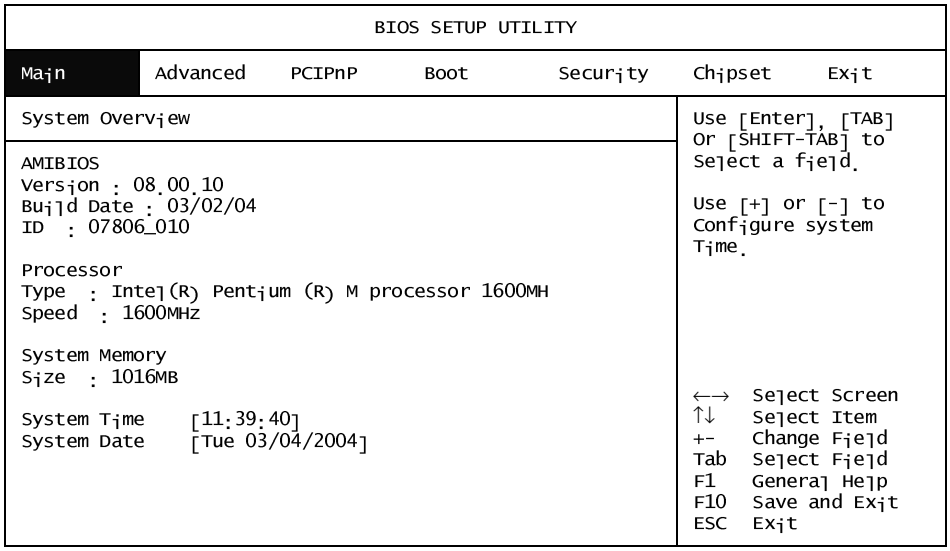
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Main

The Main BIOS setup menu screen has two main areas. The left frame displays all the options that can be configured. “Grayed-out” options cannot be configured. Options in blue can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white and a text message in the right frame gives a brief description of the option.

The Main menu reports the BIOS revision, processor type and clock speed, and allows the user to set the system’s clock and calendar. Use the left and right arrow keys to select other screens.

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.



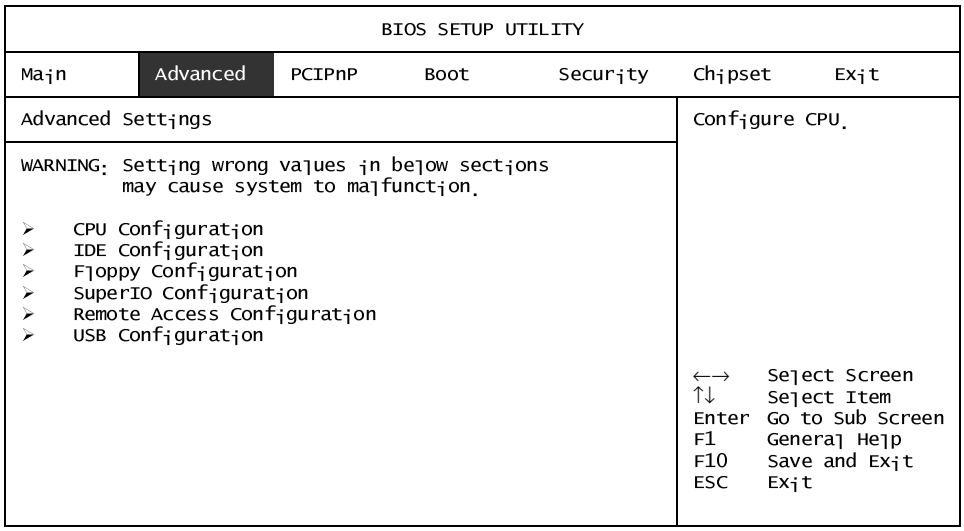
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Advanced BIOS Setup

The Advanced BIOS Setup menu allows the user to configure some CPU settings, the IDE bus, SCSI devices, other external devices and internal drives.

Select the *Advanced* tab from the ezPORT setup screen to enter the Advanced BIOS Setup screen. You can select the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. A sample of the Advanced BIOS Setup screen is shown below.

NOTE: Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select 'Load Failsafe Defaults' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Chapter One for instructions on clearing the CMOS.



Options shown may not be available on your system.

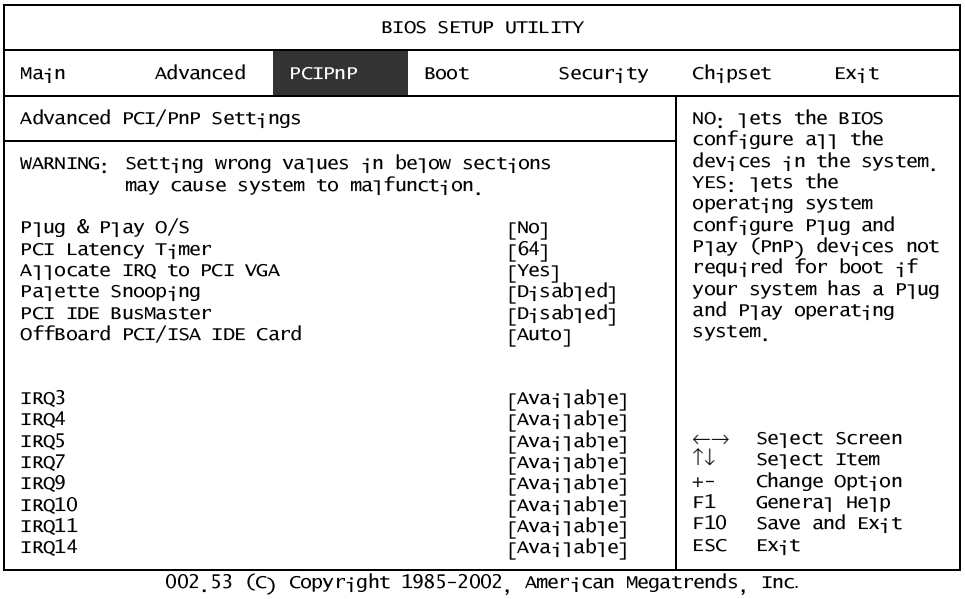
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PCI/PnP Setup

Included in this screen is the control of internal peripheral cards, as well as various interrupts. From this menu, the user can also determine if the system's plug-and-play is enabled or disabled.

NOTE: Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select 'Load Failsafe Defaults' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Chapter One for instructions on clearing the CMOS.

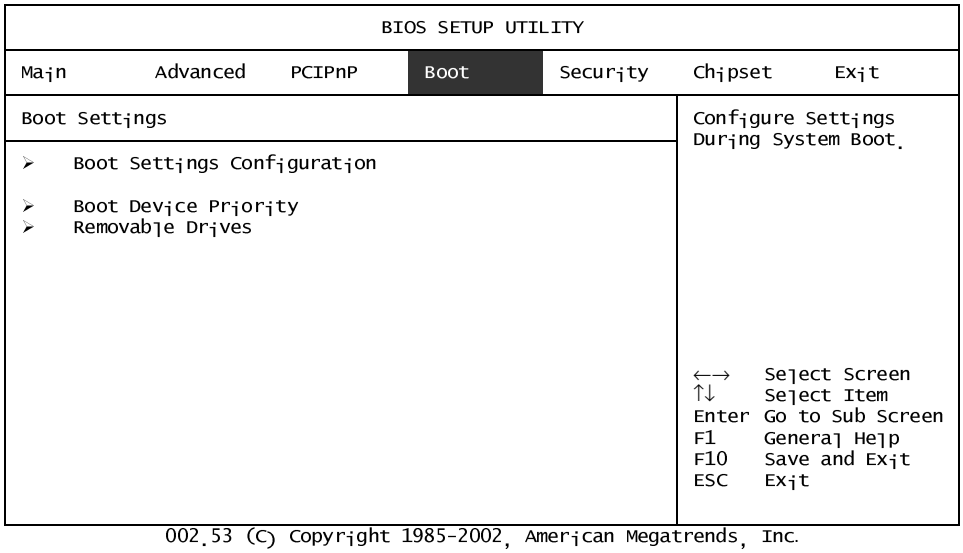
Below is a sample screen of the PCI/PnP menu; options in your system may be different from those shown.



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Boot Setup

Use the Boot Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation. Also available in this screen are 'Boot Settings' which allow the user to set how the basic system will act, for example, support for PS/2 mouse and whether to use 'Quick Boot' or not.

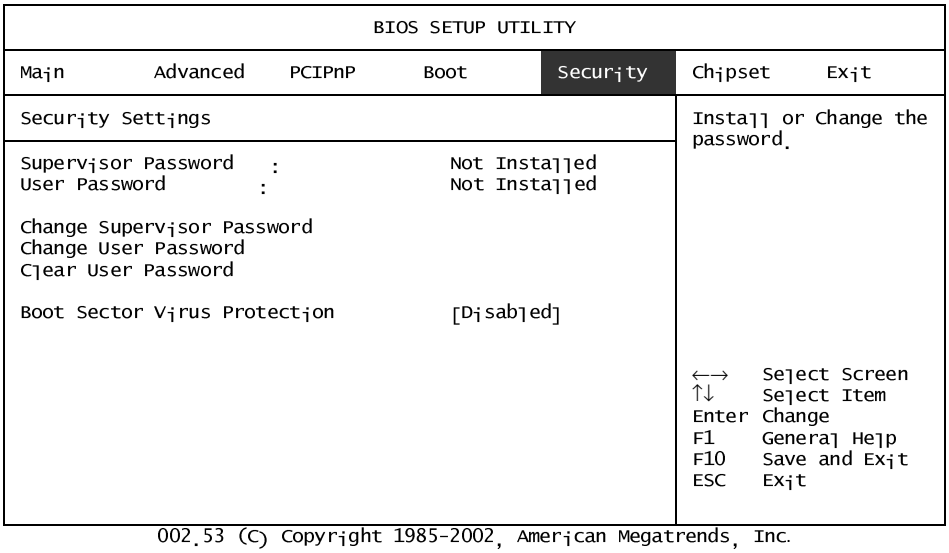


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Security Setup

The ezPORT setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when ezPORT setup is executed, using either the Supervisor password or User password.



To reset the security in the case of a forgotten password you must drain the NVRAM and reconfigure.

To clear the CMOS password:

- Turn off power to the unit.
- Momentarily short pins 2-3 of E4 for approximately five seconds.
- Power up the unit.

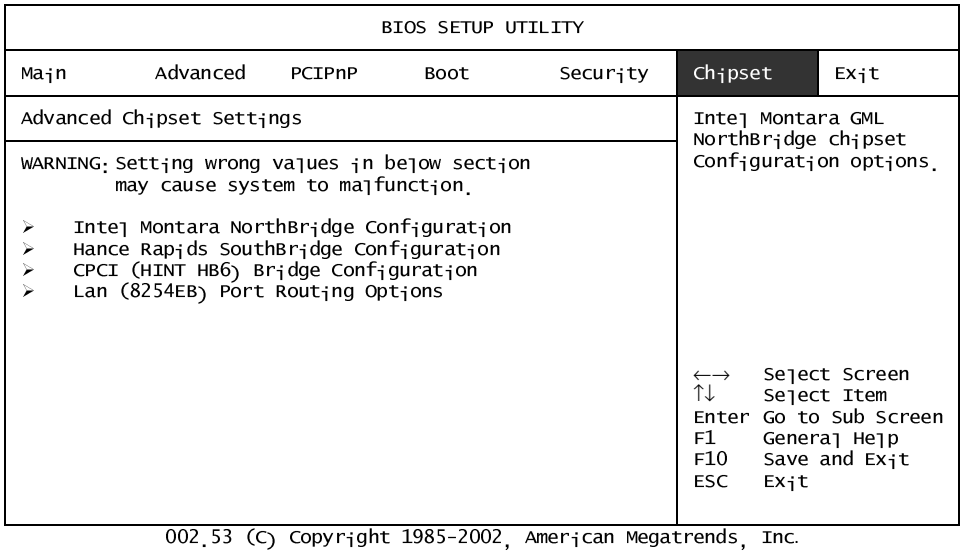
When power is reapplied to the unit, the CMOS password will be cleared.

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Chipset Setup

Select the various options for chipsets located in the system (for example, the CPU configuration and configurations for the North and South Bridge). The settings for the chipsets are processor dependent and care must be used when changing settings from the defaults set at the factory. Below is a sample of the Chipset Setup screen; the actual options on your system may vary.

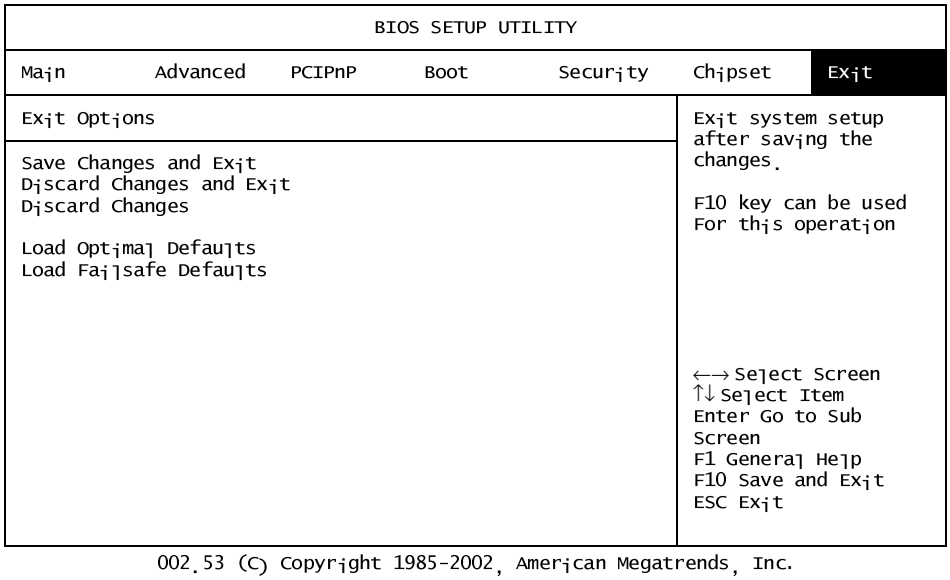
NOTE: Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select 'Load Failsafe Defaults' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Chapter One for instructions on clearing the CMOS.



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Exit Menu

Select the *Exit* tab from the ezPORT setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. The Exit BIOS Setup screen is shown below.



If changes have previously been made in the BIOS and the system malfunctions, reboot the system and access this screen. Select 'Load Failsafe Defaults' and continue the reboot.

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Appendix

C

OS and System Driver Software

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Introduction

The VMIVME-7805 provides high-performance video and Local Area Network (LAN) access by means of the video and LAN chipsets. The two LAN adapters can be configured to allow the VMIVME-7805 access to two separate, physical networks. One LAN adapter is capable of running 10BaseT and 100BaseTx and the other is the Gbit Ethernet adapter (1000Mbps).

To optimize performance of each of these PCI-based subsystems, install the driver software located on the distribution CD-ROM provided with the unit. Detailed instructions for installation of the drivers during the installation of Microsoft Windows XP Professional and Windows 2000 operating systems are provided in the following sections.

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Driver Software Installation

In order to properly use the Video and LAN on the VMIVME-7805, install the driver software located on the distribution CD-ROM provided with the unit.

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Windows 2000

1. Follow normal Windows 2000 installation procedures.
2. After installing Windows 2000, and rebooting the computer, install the 69030 driver. Please read license.txt before continuing (win_drivers / win2k / license.txt).
3. Double click 'My Computer' icon.
4. Double click on the Control Panel folder.
5. Double click the System icon.
6. Click on Hardware tab.
7. Click the Device Manager button.
8. Under Other Devices right click on Video Controller and select Uninstall.
9. Click OK and close the Device Manager.
10. Click OK to close system properties with changes.
11. Close all windows, and reboot your system.
12. After Windows reboots, the Found New Hardware wizard will appear. Click Next.
13. Insert CD-ROM 385-000098-000.
14. Select "Search For A Suitable Driver For My Device" and click Next.
15. On the Locate Drivers Files, specify location by selecting Browse, browse to your CD-ROM drive then to the Display folder and click Next.
16. Select OEMSETUP and click Open.
17. When the hardware wizard is displayed click OK (the path to OEMSET should be displayed in the Copy Manufacturers Files From box).
18. The Driver Files Search Results dialog box will now display E7501.
19. Click next and complete driver installation.

Windows 2000 82562 and 82541EI Driver Installation

After installing Windows 2000 as described above, install the Ethernet drivers. To install the Ethernet drivers you must make a floppy disk to contain the files.

1. Place a blank floppy disk in drive A, then browse to the Ethernet folder on the VMIC distribution CD-ROM.
2. Double click makedisk.bat. This will format the floppy disk and copy files necessary for Ethernet drivers installation.
3. Open My Computer, then open Control Panel.

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4. From the control panel, open System and select the Hardware tab.
5. Click on the Device Manager button.
6. Right click Ethernet Controller within the Network Adapters menu and select Properties.
7. Choose Reinstall Drivers to start the upgrade device driver wizard.
8. Select Next to continue.
9. Ensure Search For Suitable Driver For My Device is selected, then click Next.
10. Click in the box next to Floppy Disk Drives and ensure the disk you created in steps 1 and 2 is inserted in the floppy drive, then click Next.
11. The Drivers File Search Results window should identify A:\W2K_Onboard_NIC_82562.exe (for 10/100 Mbit) and A:\W2K_Onboard_NIC_82541EI.exe for the Gbit Ethernet as the driver it found. Select Next to continue.
12. The Digital Signature Not Found box indicates this is not a Microsoft driver. Select Yes to continue.
13. After the files have been copied, select Finish to complete the driver installation.
14. You must now close the Driver Manager window, remove the floppy disk from the drive and reboot the system for the changes to take affect.
15. This process must be completed for both Ethernet adapters, 1 and 2.

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Installation for Windows XP Professional

When installing a new operating system, you need to make several choices. The Windows XP Setup Wizard and this document guide you through these choices. You will also learn how to connect your computer to a network.

Important: Before you begin, you should also read the file Read1st.txt, which is on the CD-ROM 385-000027-000. This file contains late-breaking information that was unavailable when the release notes and the product documentation was written, including preinstallation notes vital to the success of your installation.

The following release notes describe how to run the Windows XP Professional Setup Wizard and install Windows XP Professional on a single computer.

Before You Begin

When you set up Windows XP Professional, you have to provide information about how you want to install the operating system. The following procedures help to provide the necessary information to ensure a successful installation. Complete the following tasks, which are described in the sections that follow, before you install Windows XP Professional:

- Make sure your hardware components meet the minimum requirements.
- Obtain compatible hardware and software, such as upgrade packs and new drivers.
- Obtain network information.
- Back up your current files in case you need to restore your current operating system.
- Determine whether you want to perform an upgrade or install a new copy of Windows XP Professional.
- If you're installing a new copy, identify and plan for any advanced setup options you might want.

Hardware Requirements

Before you install Windows XP Professional, make sure your computer meets the following minimum hardware requirements:

- 233 MHz Pentium or higher microprocessor (or equivalent)
- 128 Mbyte recommended (64 Mbyte of RAM minimum; 4 Gbytes of RAM maximum)
- 1.5 Gbyte of free space on your hard disk
- VGA monitor
- Keyboard
- Mouse or compatible pointing device
- CD-ROM or DVD drive

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For network installation:

- Compatible network adapter card and related cable

For more information, see the Hardware Compatibility List (HCL) or see "Checking Hardware and Software Compatibility".

- Access to the network share that contains the Setup files

Checking Hardware and Software Compatibility

The Windows XP Professional Setup Wizard automatically checks your hardware and software and reports any potential conflicts. To ensure a successful installation, however, you should determine whether your computer hardware is compatible with Windows XP Professional before you start the wizard.

You can view the Hardware Compatibility List (HCL) at the Microsoft Web site:

http://www.microsoft.com/hcl/

NOTE: Windows XP Professional supports only those devices listed in the HCL. If your hardware isn't listed, contact the hardware manufacturer and request a Windows XP Professional driver for the component. To ensure that programs using 16-bit drivers function properly afterwards, request 32-bit drivers from the software vendor.

During the setup process, you can use upgrade packs to make your existing software compatible with Windows XP Professional. Upgrade packs are available from the appropriate software manufacturers.

Obtaining Network Information

If your computer won't be connected to a network, you can skip this section. First, you need to decide whether your computer is joining a domain or a workgroup. If you don't know which option to choose, or if your computer won't be connected to a network, select the workgroup option. (You can always join a domain after you install Windows XP Professional.) If you select the domain option, ask your network administrator to create a new computer account in that domain or reset your existing account.

If your computer is currently connected to a network, request the following information from your network administrator before you begin the setup process:

- Name of your computer
- Name of the workgroup or domain
- TCP/IP address (if your network doesn't have a Dynamic Host Configuration Protocol (DHCP) server)

To connect to a network during the setup process, you must have the correct hardware installed on your computer and be connected by a network cable.

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Backing Up Your Files

If you're upgrading from an earlier version of Windows, you should back up your current files. You can back up files to a disk, a tape drive, or another computer on your network.

How you back up your files depends on your current operating system. If your computer is running Microsoft Windows 95 or Windows 98, you might need to install the Windows Backup program. If you're using Windows NT 4.0, Windows Backup is installed by default. You must have a tape drive installed to use the Backup tool in Windows NT.

Upgrading vs. Installing a New Copy

After you start the Windows XP Professional Setup Wizard, one of the first decisions you have to make is whether to upgrade your current operating system or to perform an entirely new installation. During the setup process, you must choose between upgrading or installing a new copy of Windows (a "clean install").

During an upgrade, the Windows XP Professional Setup Wizard replaces existing Windows files but preserves your existing settings and applications. Some applications might not be compatible with Windows XP Professional and therefore might not function properly after an upgrade. You can upgrade to Windows XP Professional from the following operating systems:

- Windows 98 (all versions)
- Windows Millennium Edition
- Windows NT 4.0 Workstation (Service Pack 6 and later)
- Windows 2000 Professional (including service packs)
- Windows XP Home Edition

If your computer is currently running an unsupported operating system, you must install a new copy. The wizard installs Windows XP Professional in a new folder. After the installation is complete, you will have to reinstall applications and reset your preferences.

If you want to modify the way the wizard installs Windows XP Professional, click Advanced Options, and then perform any of the following tasks:

- Change the default location of the setup files.
- Store system files in a folder other than the default folder (\Windows).
- Copy the installation files from the CD to the hard disk.
- Select the partition on which to install Windows XP Professional.

Unless you're an advanced user, you should use the default settings.

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Running Windows XP Professional Setup

The Windows XP Professional Setup Wizard gathers information, including regional settings, names, and passwords. The wizard then copies the appropriate files to your hard disk, checks the hardware, and configures your installation. When the installation is complete, you're ready to log on to Windows XP Professional. Note that your computer restarts several times during the process.

How you start the Windows XP Setup Wizard depends on whether you're upgrading or installing a new copy of Windows. Determine your installation method, locate the appropriate section in this manual, and then follow the procedures for your Setup scenario.

If You're Installing a New Copy (Clean Install)

If your computer has a blank hard disk or your current operating system isn't supported, you need to start your computer by using the Windows XP Professional CD. Some newer CD-ROM drives can start the installation from the CD and automatically run the Windows XP Professional Setup Wizard.

To install a new copy by using the CD:

1. Start your computer by running your current operating system, and then insert the Windows XP Professional CD into your CD-ROM drive.
2. If Windows automatically detects the CD, click Install Windows. The Windows XP Setup Wizard appears.

If Windows doesn't automatically detect the CD, click Start, and then click Run. Type the following path to the setup file, replacing 'd' if necessary with the letter of your CD-ROM drive: d:\setup.exe

3. Press ENTER.
4. When prompted to choose an installation type, select New Installation, and then click Next.
5. Follow the instructions that appear on your screen.

To install a new copy by using a network connection:

1. Using your existing operating system, establish your connection to the shared network folder that contains the Setup files. You can also use an MS-DOS or network installation disk to connect to the network server, if the disk contains network client software.

Your network administrator will be able to provide you with this path.

2. If your computer is currently running Windows 98, Windows Millennium Edition, or an earlier version of Windows NT, then at the command prompt, type the path to the file setup.exe.
3. Press ENTER.
4. Follow the instructions that appear on your screen.

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If You're Upgrading

The upgrade process is simple. The Windows XP Professional Setup Wizard detects and installs the appropriate drivers, or it creates a report listing devices that couldn't be upgraded, so you can be sure your hardware and software is compatible with Windows XP Professional.

To upgrade from the CD:

1. Start your computer by running your current operating system, and then insert the Windows XP Professional CD into your CD-ROM drive.
2. If Windows automatically detects the CD, the Windows XP Professional CD dialog box appears. To start your upgrade, click Install Windows. If Windows doesn't automatically detect the CD, click Start, and then click Run. Then type the path to the setup file, replacing 'd' if necessary with the letter of your CD-ROM drive: d:\setup.exe
3. Press ENTER.
4. When prompted to choose an installation type, select Upgrade, and then click Next.
5. Follow the instructions that appear on your screen.

To upgrade from a network connection:

1. Using your current operating system, establish a connection to the shared network folder that contains the Setup files. If you have an MS-DOS or network installation disk that contains network client software, you can use that disk to connect to the shared folder. Your network administrator will be able to provide you with this path.
2. At the command prompt, type the path to the file setup.exe.
3. Press ENTER.
4. Select Upgrade, and then click Next.
5. Follow the instructions that appear on your screen.

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Appendix

D

Argon BIOS

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Introduction

The VMIVME-7805 includes an Argon BIOS option which allows the VMIVME-7805 to be booted from a network. This appendix describes the procedures to enable this option and the Argon BIOS Setup screens.

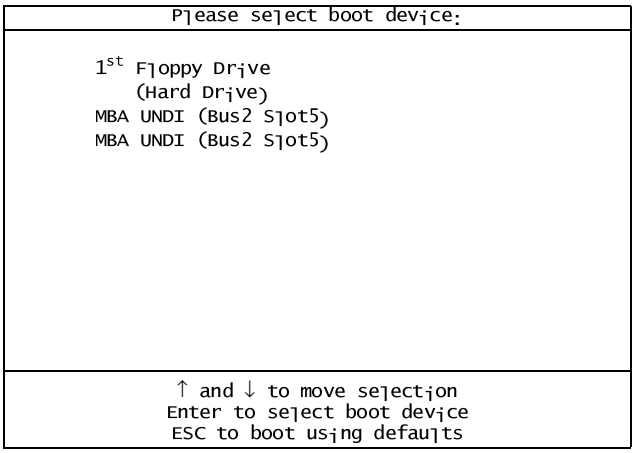
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Boot Menus

There are two methods of enabling the Argon BIOS option. The first method is the *First Boot* menu. The second is the *Boot* menu from the BIOS Setup Utility.

First Boot Menu

Press F11 at the very beginning of the boot cycle, which will access the *First Boot* menu. Selecting “Managed PC Boot Agent (MBA)” to boot from the LAN in this screen applies to the current boot only, at the next reboot the VMIVME-7805 will revert back to the setting in the Boot menu.



Using the arrow keys, highlight *Managed PC Boot Agent (MBA)*, and press the ENTER key to continue with the system boot.

Boot Menu

The second method of enabling the Argon BIOS option is to press the DEL key during system boot. This will access the BIOS Setup Utility. Advance to the Boot menu, and to the Boot Device Priority sub-menu. Use the arrow keys to highlight the Managed PC Boot Agent (MBA) option. Repeat entering <+> until the desired MBA is at the top of the list.

Advance to the Exit menu, select “Exit Saving Changes” and press ENTER. When the system prompts for confirmation, press “Yes”. The computer will then restart the system boot-up.

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.

BIOS SETUP UTILITY		
Boot		
Boot Device Priority		Specifies the boot sequence from the available devices.
1st Boot Device 2nd Boot Device 3rd Boot Device	[MBA UNDI (Bus2 Slot5)] [1st Floppy Drive] [Hard Drive]	←→ Select Screen ↑↓ Select Item +- Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

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BIOS Features Setup

After the Managed PC Boot Agent has been enabled, there are several boot options available to the user. These options are RPL (default), TCP/IP, Netware and PXE. The screens below show the defaults for each boot method.

RPL

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(C) Copyright 2002 Argon Technology Corporation
All rights reserved
```

```
                              Configuration

     Boot Method:             RPL

     Config Message:          Enabled
     Message Timeout:         3 Seconds
     Boot failure Prompt:     Wait for timeout
     Boot Failure:            Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

TCP/IP

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
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```

```
                              Configuration

     Boot Method:             TCP/IP

     Protocol                 DHCP
     Config Message:          Enabled
     Message Timeout:         3 Seconds
     Boot failure Prompt:     Wait for timeout
     Boot Failure:            Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```


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Netware

```
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```

```
                                Configuration

     Boot Method:               Netware

     Protocol                   802.3
     Config Message:            Enabled
     Message Timeout:           3 Seconds
     Boot failure Prompt:       Wait for timeout
     Boot Failure:              Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

PXE

```
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```

```
                                Configuration

     Boot Method:               PXE

     Config Message:            Enabled
     Message Timeout:           3 Seconds
     Boot Failure Prompt:       Wait for timeout
     Boot Failure:              Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```


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Appendix

E

Sample C Software

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Introduction

This appendix provides listings of a library of sample code that the programmer may utilize to build applications. These files are provided in the directory "\sample code" on CD 320-500077-000, labeled "Windows Drivers", included with the VMIVME-7805.

These files are provided without warranty. All source code is ©2001, VMIC Corporation.

Directory \VME

This directory contains code used to setup the Universe IIB chip with one PCI-to-VMEbusVMIVME-7805 window and enable Universe IIB registers to be accessed from the VMEbus to allow mailbox access.

Directory \fpga

This directory contains code used to test the functions of the VMIC-designed FPGA such as timers, SRAM controller and Watchdog Timer.

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Directory \i2c

This directory contains code that demonstrates how to send data using the I^2C controller in the super I/O component, and also how to manipulate the I^2C mux which is used to direct the super I/O's I^2C back to the VME backplane.

Directory \include

This directory contains common files required to compile several of the sample code applications.

Directory \max1617

This directory contains code that demonstrates how to read the temperatures from the max1617 device on the VMIVME-7805.

Directory \support

This directory contains memory and PCI access routines used by many of the sample code applications.

Directory \vlm

This directory contains code that demonstrates how to read the voltages from the analog inputs of the super I/O component on the VMIVME-7805.

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