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Hardware Reference Manual

VMIVME-1129*

128-bit Digital Input Board with Built-In-Test

Publication No. 500-001129-000 Rev. F.0

abaco SYSTEMS

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Document History

Revision	Date	Description
E.0	March 2012	
F.0	October 2016	Reformatting

Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

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About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when “k”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.


NOTE
When describing transfer rates, “k”, “M” and “G” mean $x10^3$, $x10^6$ and $x10^9$ *not* $x2^{10}$, $x2^{20}$ and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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Third Party Documents

Refer to "The VMEbus Specification" for a detailed explanation of the VMEbus which is available from the following source:

VITA
VMEbus International Trade Association
PO Box 19658
Fountain Hills, AZ 85269
Ph: 480-837-7486
Email: info@vita.com
www.vita.com

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LINK
support@abaco.com

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If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.

LINK
www.abaco.com/embedded-support

Do not return products without first contacting the Abaco Repairs facility.

Additional Notes

The VMIVME-1129 Digital Input Board is designed to read a voltage from a variety of devices. The signals may originate from electronic switching circuits, standard logic circuits, mechanical switch contacts, relay contacts, Opto 22 type signal conditioning modules, or numerous other sources. The inputs can be configured to receive current sinking or voltage sourcing signals.

Features

The VMIVME-1129 Digital Input Board has several unique features as specified below:

- 128 bits of voltage sourcing or current sinking digital inputs
- 3 msec input noise suppression filter
- Each group of 8 inputs are jumper selectable to monitor, voltage source, or current sinking signals
- Onboard Built-in-Test logic for fault detection and isolation
- Front panel with Fail LED
- User-selectable input voltage thresholds (1.25 to 34 V)
- VMEbus compatible
- 8-, 16- or 32-bit data transfers
- Double Eurocard form factor

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Functional Description

The VMIVME-1129 Board has input circuitry that permits the user to select and configure the basic input functions. The input functions and threshold levels are built into the circuitry. The configuration of the board by the user sets up these functions. This allows the user to set some of the inputs for one function and the rest to another.

The basic function of this board is to sample the external inputs (when the board is accessed by the host) and place this data on the appropriate data lines of the VMEbus. In other words, this board takes a snapshot of the external data and guides it to the host via the VMEbus.

This board supports built-in-testing of its active components. Test registers are mapped into the same addresses as the input registers they are to test. In this way, the host simply writes data to an address then reads the same address, and compares the data read with the data sent to determine the health of the board. Testing can be done with the board off-line or on-line. The Control and Status Register (CSR) controls the operating state of the board.

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this Manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

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1 • Theory of Operation

1.1 Operational Overview

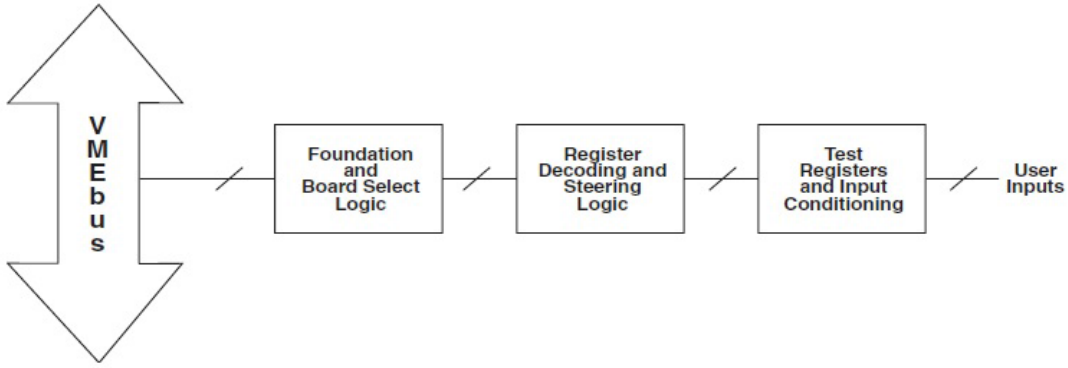
The VMIVME-1129 Digital Input Board is designed to read voltage sourcing or current sinking devices (for example: contact closure to ground). The input voltage levels and threshold trip levels are set up by the user.

The VMIVME-1129 is a snapshot type board. When the VMEbus address decoded by this board matches its address, the inputs are stored in an associated input register. The data is then steered to the proper data lines on the backplane for the host to use.

The VMIVME-1129 has built-in-test registers. They are used to check the board. The host simply writes data to the register or registers to be checked. Then by reading these registers and comparing the data read to the data written, the user can determine if the board is working. This can be done whenever the user wishes to check the board. The written data will overwrite the external input level. The VMIVME-1129 has input noise filters for the external inputs.

Figure 1-1 below is a block diagram of the basic functions of the VMIVME-1129 Board.

Figure 1-1 VMIVME-1129 Block Diagram



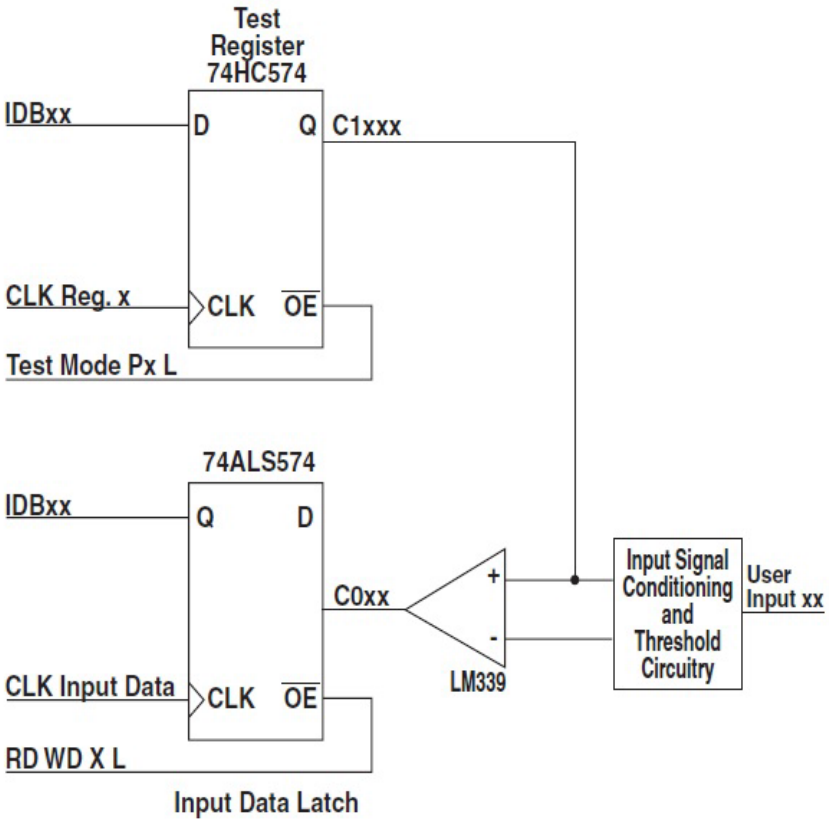
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1.2 Test Registers

The test registers are used to check the "health" of the board. The user writes data into these registers. If their outputs are enabled (TEST MODE active), the data in these registers will overwrite the external inputs. This enables the active components to be checked without disconnecting the external inputs. The test registers are mapped into the same address as their corresponding input registers. In this way, the user simply writes to and then reads from the port to be checked. If the data written is different from the data read, there is a problem.

Figure 1-2 below is a block diagram of the Test and Input Data Registers of the VMIVME-1129 Board.

Figure 1-2 VMIVME-1129 Test and Input Data Registers



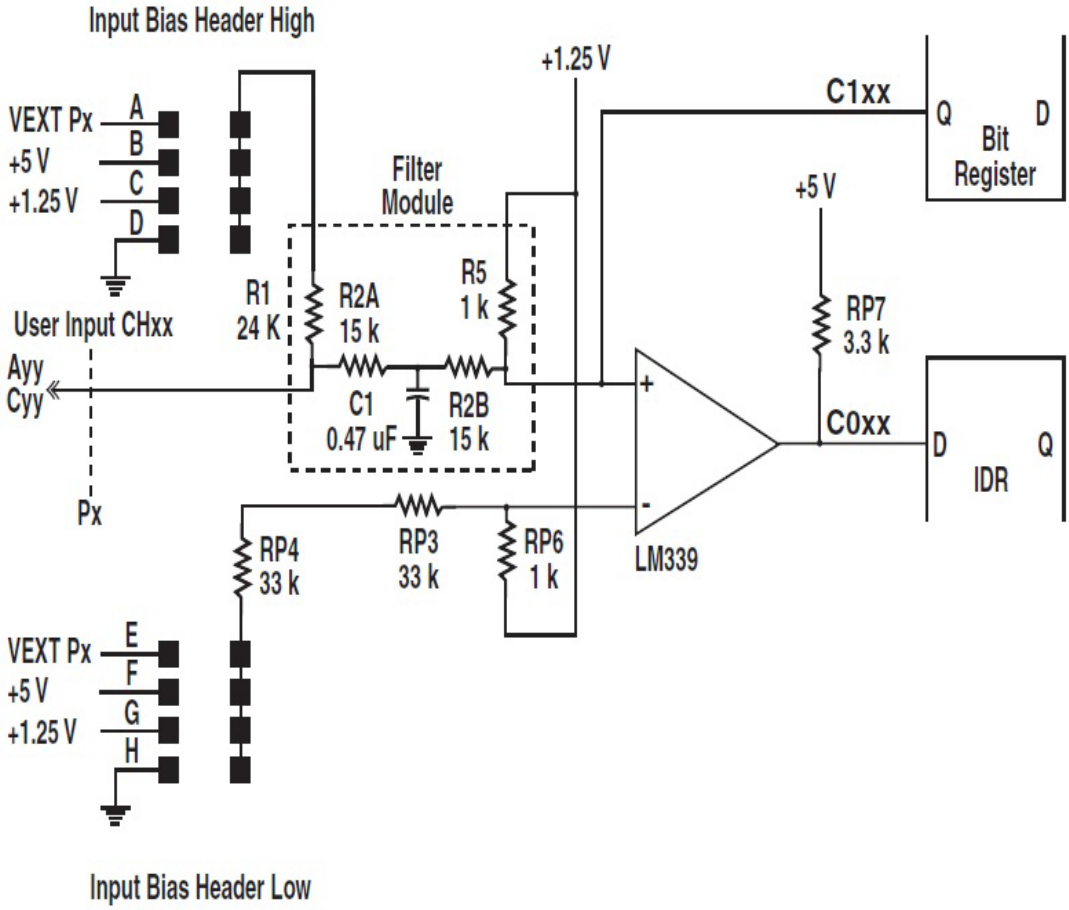
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1.3 Input Circuitry

The Figure below shows the basic topology for each input. The BIT (Built-in-Test) Register is shown with only one of its eight lines (each register controls eight input circuits). The comparator output goes to an Input Data Register (IDR). When the board is selected, these registers are clocked. This is the snapshot effect. The incoming data is then held in these registers while the board guides the data to the appropriate VMEbus data lines. The filter module provides the 3 msec input noise suppression circuitry.

The input circuit uses RP4, RP3, and associated header to set the threshold (or trip) level for the comparator. ***Table 2-1*** on page 16 is a detailed listing of the thresholds for some common input levels. The threshold equation is also provided. The user can use this to calculate the trip voltage for the specific input voltage range he is using.

Figure 1-3 Basic Input Circuit Topology



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1.4 Input Types

The VMIVME-1129-000 inputs can be configured in one of two types, either as voltage sourcing or current sinking. In the voltage sourcing input setup, R1's jumper is grounded. The input must be a voltage across R1. RP4 has its jumper going to a voltage the user chooses. The voltage chosen will establish the threshold level for the input voltage. Please refer to *Table 2-1* on page 16 for the actual value of the trip voltage. In the current sinking configuration, R1's jumper is connected to V_{EXT}. Now R1 acts as a pull up for the user's external circuit. RP4 and its jumper work as before.

The VMIVME-1129-100 option is only for contact sensing using an external voltage of 24 V. This input requires R1's jumper to be connected to V_{EXT}. This makes R1 a wetting resistor for the contacts, and limits the contact current to 1 mA. This requires one end of the contacts to be connected to ground. In this option, RP4 is 100 k Ohm. If RP4's jumper is set to V_{EXT} (24 V), the threshold voltage is approximately:

$$7.5\ V, \text{ or } V_T = \left[\left(\frac{V_R - 1.25}{134\ k}\right) \times 34\ k\right] + 1.25\ V$$

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2 • Unpacking/Handling, Configuration and Installation

This chapter describes the unpacking, handling, installation and configuration of the VMIVME-1129

2.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Technical Support.

2.2 Handling Precautions

CAUTION
Handle the board by the edges or front panel only.



CAUTION
Some of the components assembled on Abaco products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

WARNING
Use extreme caution when handling, testing and adjusting this equipment. This device may operate in an environment containing potentially dangerous voltages.

Ensure that all power to the system is removed before installing any device.

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

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2.3 Board Configuration

The VMIVME-1129 circuitry permits the user to configure the inputs based on the application. The following sections of the Manual are intended to instruct the user in the implementation of these input configurations. The user must first decide which input topology to use: the inputs can receive either current sinking; i.e., open-collector or voltage sourcing signals. Next, the user must select a threshold level; the threshold can be set as shown in ***Table 2-1*** below. The input channels are configured in groups of 8 so the channels can be setup on a byte-by-byte basis.

2.3.1 Input Topology

The input topology is configured by placing jumpers in certain positions of a header field. ***Figure 2-2*** on page 18 shows the circuit topology for a current sink input. ***Figure 2-3*** on page 18 shows a voltage source input. Jumper J1 selects the pull-up voltage applied to input resistor RP1 and J2 selects the reference voltage applied to the threshold resistor RP4. Jumpers J1 and J2 in these figures represent the jumpers used to control a group of 8 input channels. The physical location of these jumpers (E1 through E16) is shown in ***Figure 2-1*** on page 17.

If J1 is in the ground position, the input circuit is voltage sourcing. In any other position, the input is current sinking. In the circuit shown in ***Figure 2-3*** on page 18, the voltage is 5 V. If the voltage you are using is greater than 5 V, then you should use Vext for J1. ***Table 2-2*** on page 19 shows the location of Vext for each group of channels.

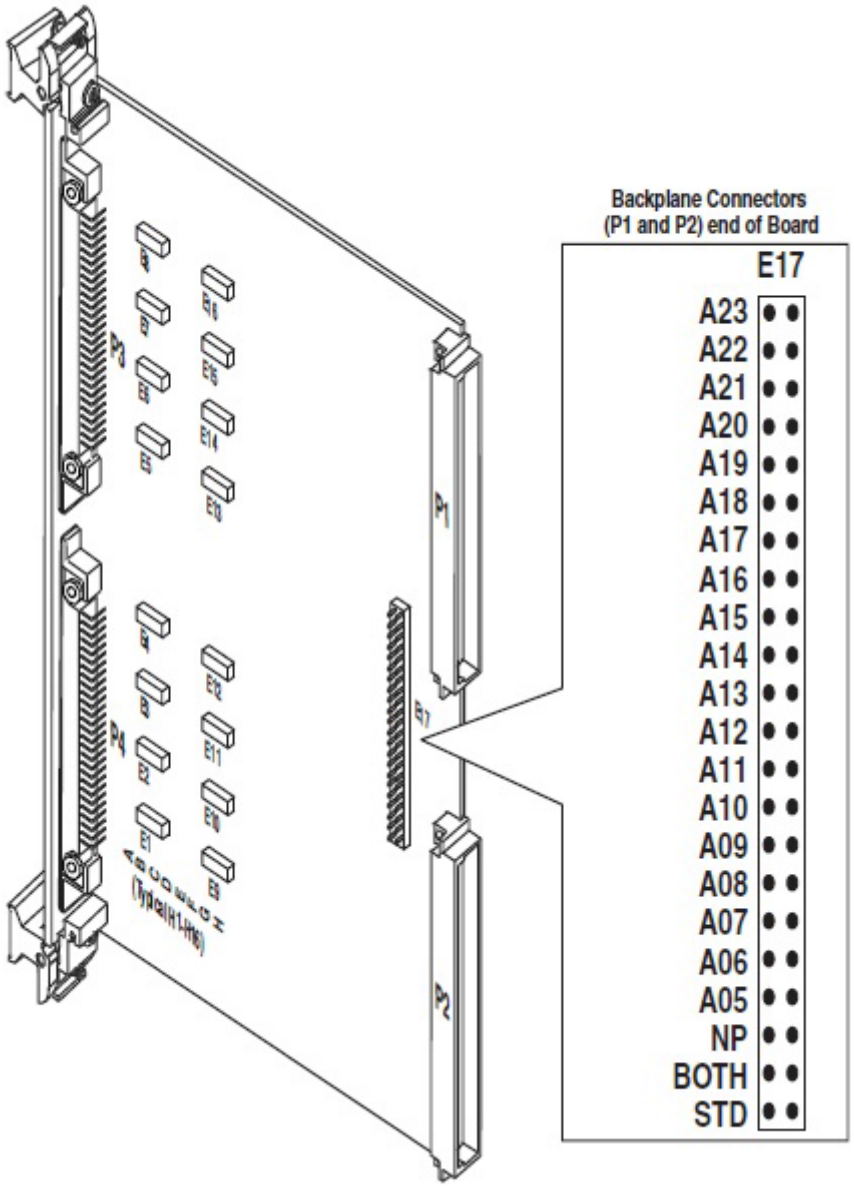
Jumper J2 chooses the reference voltage (V_r) for the threshold level (V_t). ***Table 2-1*** below lists several threshold values as a function of reference voltage. An equation for the threshold voltage is given if the value you require is not listed. ***Figure 2-4*** on page 20 describes the possible jumper configurations.

Table 2-1 Threshold Voltages

$V_t = 0.46\ V_r + 0.67$	
V_r	V_t
0 V	0.67 V
1.25 V	1.25 V
5 V	3.0 V
12 V	6.2 V
24 V	11.7 V
28 V	13.6 V
48 V	22.8 V
66 V	31.0 V

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Figure 2-1 Physical Location of Jumpers



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Figure 2-2 Basic Voltage Sourcing Input

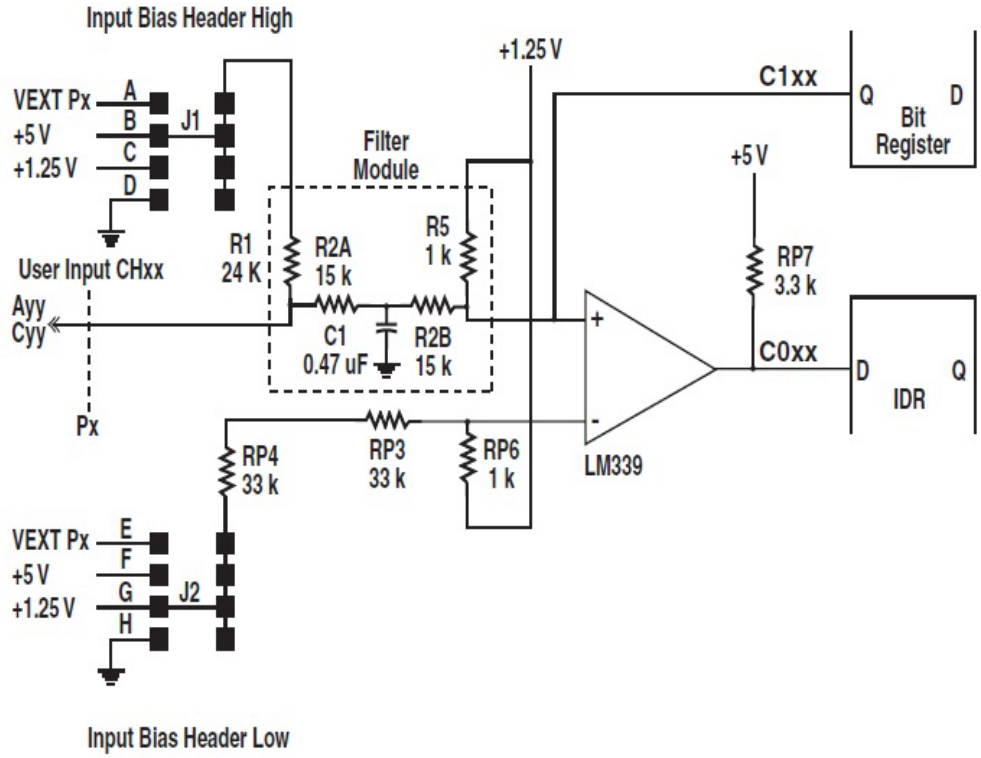
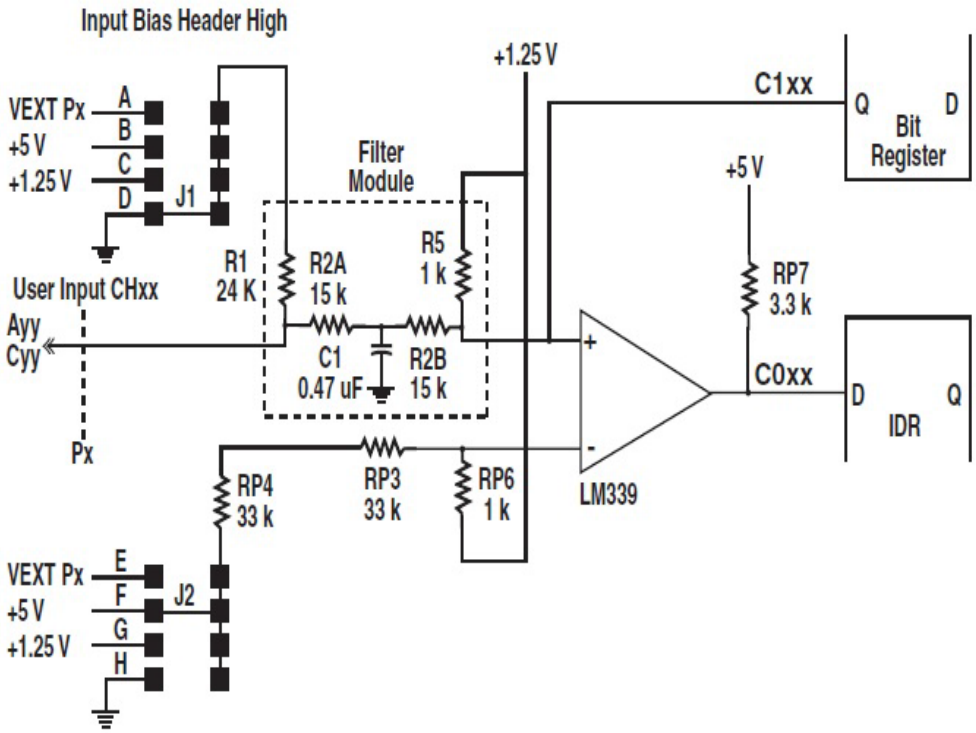


Figure 2-3 Basic Voltage Sourcing Input



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Table 2-2 Header Assignments

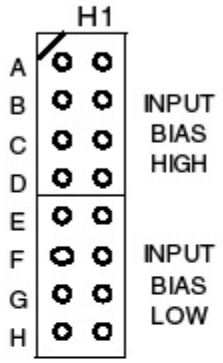
Header Ref. Des.	Associated Channels	Location of VEXT
E1	CH07 - CH00	P2-C32
E2	CH15 - CH08	P2-C30
E3	CH23 - CH16	P2-C28
E4	CH31 - CH24	P2-C26
E5	CH64 - CH71	P2-C16
E6	CH72 - CH79	P2-C14
E7	CH80 - CH87	P2-C12
E8	CH88 - CH95	P2-C10
E9	CH32 - CH39	P2-C24
E10	CH40 - CH47	P2-C22
E11	CH48 - CH55	P2-C20
E12	CH56 - CH63	P2-C18
E13	CH103 - CH96	P2-C8
E14	CH111 - CH104	P2-C6
E15	CH119 - CH112	P2-C4
E16	CH127 - CH120	P2-C2

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Figure 2-4 Input Circuitry Jumper Configurations

INPUT BIAS HIGH JUMPER LOCATION

INPUT BIAS LOW JUMPER LOCATION	A	B	C	D
E	T = CS $V_P = V_{EXT}$ V_{OC} = Eq 2 V_T = Eq 1	T = CS V_P = +5 V V_{OC} = +3.35 V V_T = Eq 1	T = CS V_P = +1.25 V V_{OC} = +1.25 V V_T = Eq 1	T = VS V_T = Eq 1
F	T = CS $V_P = V_{EXT}$ V_{OC} = Eq 2 V_T = +3.2 V	T = CS V_P = +5 V V_{OC} = +3.35 V V_T = +3.2 V	NOT USED	T = VS V_T = +3.2 V
G	T = CS $V_P = V_{EXT}$ V_{OC} = Eq 2 V_T = +1.25 V	T = CS V_P = +5 V V_{OC} = +3.35 V V_T = +1.25 V	NOT USED	FACTORY CONFIGURATION T = VS V_T = +1.25 V
H	T = CS $V_P = V_{EXT}$ V_{OC} = Eq 2 V_T = +0.61 V	T = CS V_P = +5 V V_{OC} = +3.35 V V_T = +0.61 V	NOT USED	T = VS V_T = +0.61 V



T =Input Circuit Topology

VS =Voltage Sourcing Input

CS =Current Sinking Input

V_T =Threshold Voltage

V_P =Pull-Up Voltage (applied to 24 k_ pull-up resistor)

V_{OC} =Open Circuit Input Voltage

Eq 1 =0.46 V_{EXT}+ 0.67

Eq 2 =0.56 V_{EXT}+ 0.55

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2.4 Address Modifiers

The VMIVME-1129 is configured at the factory, as shown in ***Figure 2-5***, to respond to short supervisory I/O access. This configuration can be changed by installing jumpers at the appropriate locations in header E17 as shown in the corresponding figures.

Table 2-3 Configuration of VMIVME-1129

I/O ACCESS	CORRESPONDING FIGURE - Figures below
Short Supervisory	Figure 2-5 (factory configuration)
Standard Supervisory	Figure 2-6
Short Nonprivileged	Figure 2-7
Standard Nonprivileged	Figure 2-8
Short (responds to either supervisory or nonprivileged)	Figure 2-9
Standard (responds to either supervisory or nonprivileged)	Figure 2-10

Figure 2-5 Jumper Configuration for Short Supervisory Access (Factory Default)

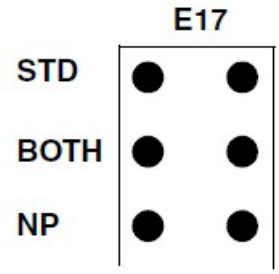
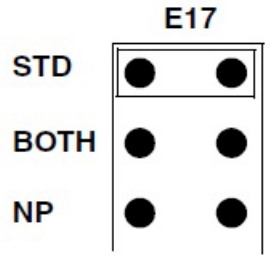


Figure 2-6 Jumper Configuration for Standard Supervisory Access



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Figure 2-7 Jumper Configuration for Short Nonprivileged Access

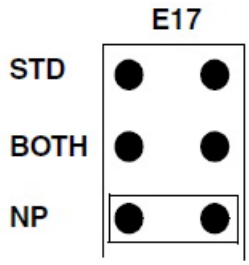


Figure 2-8 Jumper Configuration for Standard Nonprivileged Access

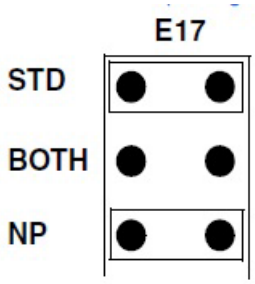


Figure 2-9 Jumper Configuration for Short Addressing and Supervisory or Nonprivileged Access

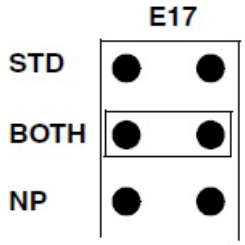
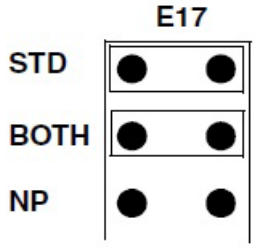
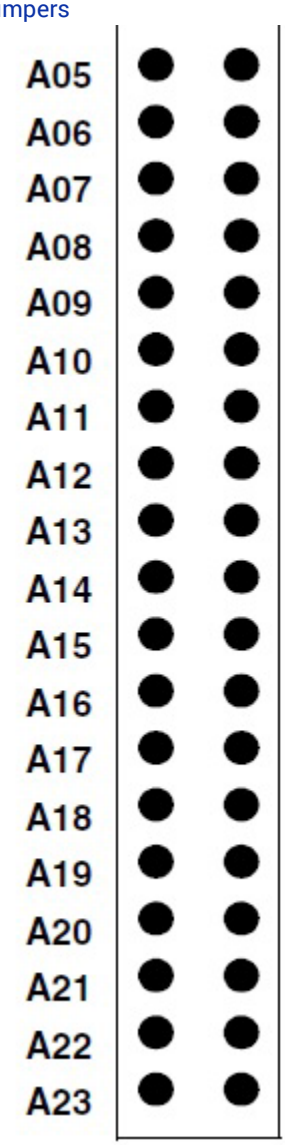


Figure 2-10 Jumper Configuration for Standard Addressing and Supervisory or Nonprivileged Access



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Figure 2-11 Base Address Select Jumpers



NOTE

The example shown is for a short I/O base address of FF00 Hexadecimal (FFFFFF00 for Standard I/O access.

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2.5 Address Selection Jumpers

The VMIVME-1129 is designed with a bank of address select jumpers that specify the beginning board address for data transfers. The address selection jumpers are shown in ***Figure 2-11*** on page 23. The VMIVME-1129 is factory configured to respond to FF00 HEX.

2.5.1 Before Applying Power: Checklist

Before installing the board in a VMEbus system, perform the following checklist to verify that the board is ready for the intended operation:

- Verify the sections in Theory and Programming of the VMIVME-1129 Manual have been read and applied to system requirements.
- Review this chapter to verify factory installation of the jumpers. See ***Figure 2-5*** on page 21 for factory configuration.
  - To change the address jumpers, refer to the section above, "***Address Selection Jumpers***.
  - To change the address modifier response, refer to ***Figure 2-5*** to respond to short supervisory I/O access. This configuration can be changed by installing jumpers at the appropriate locations in header E17 as shown in the corresponding figures on page 22 and 23.

The VMIVME-1129 is designed to accommodate either current sink or voltage source inputs. See ***Figure 2-2*** and ***Figure 2-3*** on page 18, respectively, for the correct configuration of the desired input.

Verify that the cables, with proper mating connectors, been connected to the input connectors.

After completing the checklist, the VMIVME-1129 Board may be installed. Generally the VMIVME-1129 may be installed in any slot position except slot one, which is usually reserved for the system controller processing unit.

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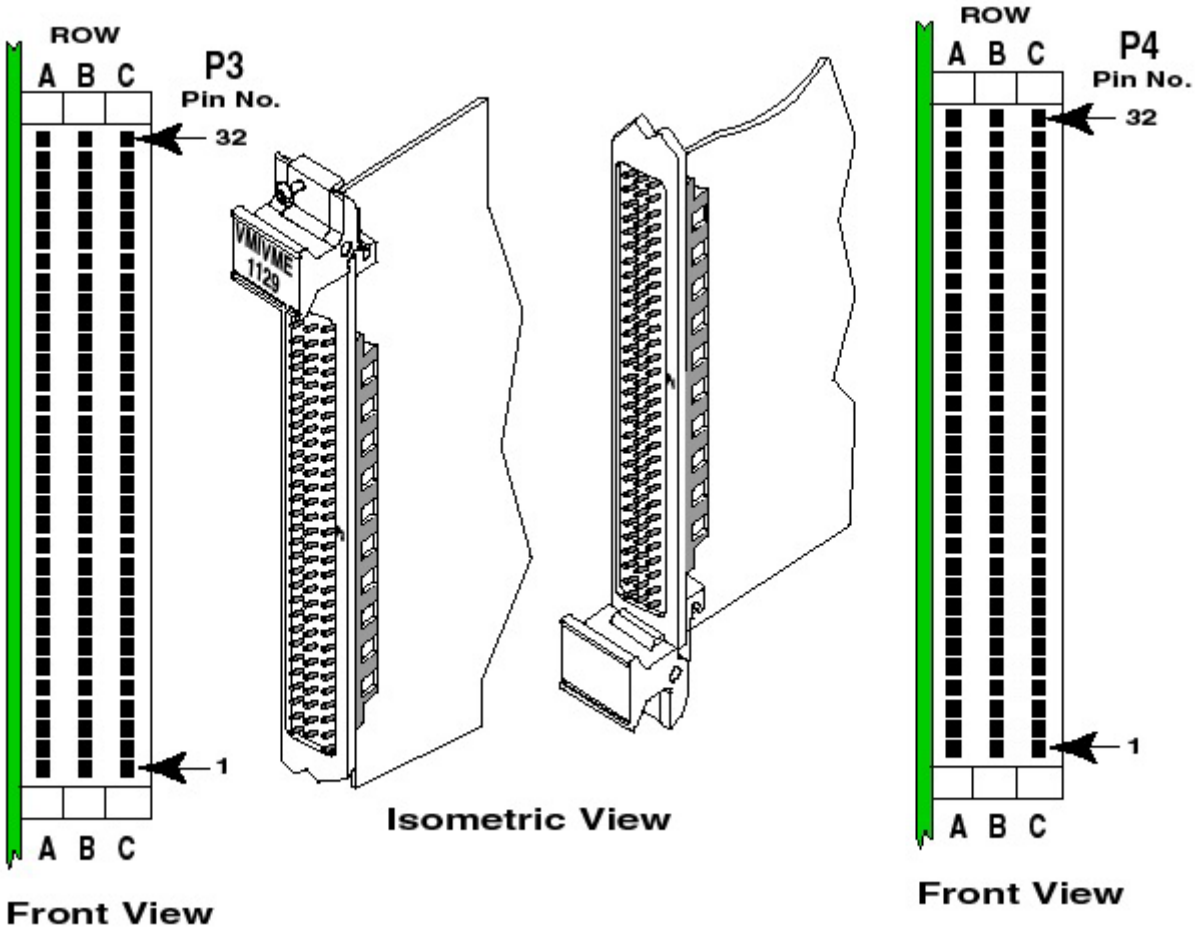
2.6 I/O Cable and Front Panel Connector Configuration

The input connectors (P3 and P4) on the VMIVME-1129 are 96-pin DIN standard and were selected by Abaco because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements.

Figure 2-12 below shows the pin layout of the P3 and P4 connectors. *Table 2-4* and *Table 2-5* on page 26 and *Table 2-6* and *Table 2-7* on page 27 detail the connector pin assignments. The P2 connector pin layout is shown in *Figure 2-13*, while the pin assignments are listed in *Table 2-8* on page 29.

Refer to specification number 800-001129-000 for the type of connector to use.

Figure 2-12 P3/P4 Connector Pin Layout



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Table 2-4 P3 (Row C) Pin - Channel Assignments

P3		P3	
ROW C Pin	CHANNEL No.	ROW C Pin	CHANNEL No.
32	127	16	111
31	126	15	110
30	125	14	109
29	124	13	108
28	123	12	107
27	122	11	106
26	121	10	105
25	120	09	104
24	119	08	103
23	118	07	102
22	117	06	101
21	116	05	100
20	115	04	99
19	114	03	98
18	113	02	97
17	112	01	96
All Pins in Row B are grounded.			

Table 2-5 P3 (Row C) Pin - Channel Assignments

P3		P3	
ROW A Pin	CHANNEL No.	ROW A Pin	CHANNEL No.
32	95	16	79
31	94	15	78
30	93	14	77
29	92	13	76
28	91	12	75
27	90	11	74
26	89	10	73
25	88	09	72
24	87	08	71
23	86	07	70
22	85	06	69
21	84	05	68
20	83	04	67
19	82	03	66
18	81	02	65
17	80	01	64
All Pins in Row B are grounded.			

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Table 2-6 P4 Pin - Channel Assignments (Row C)

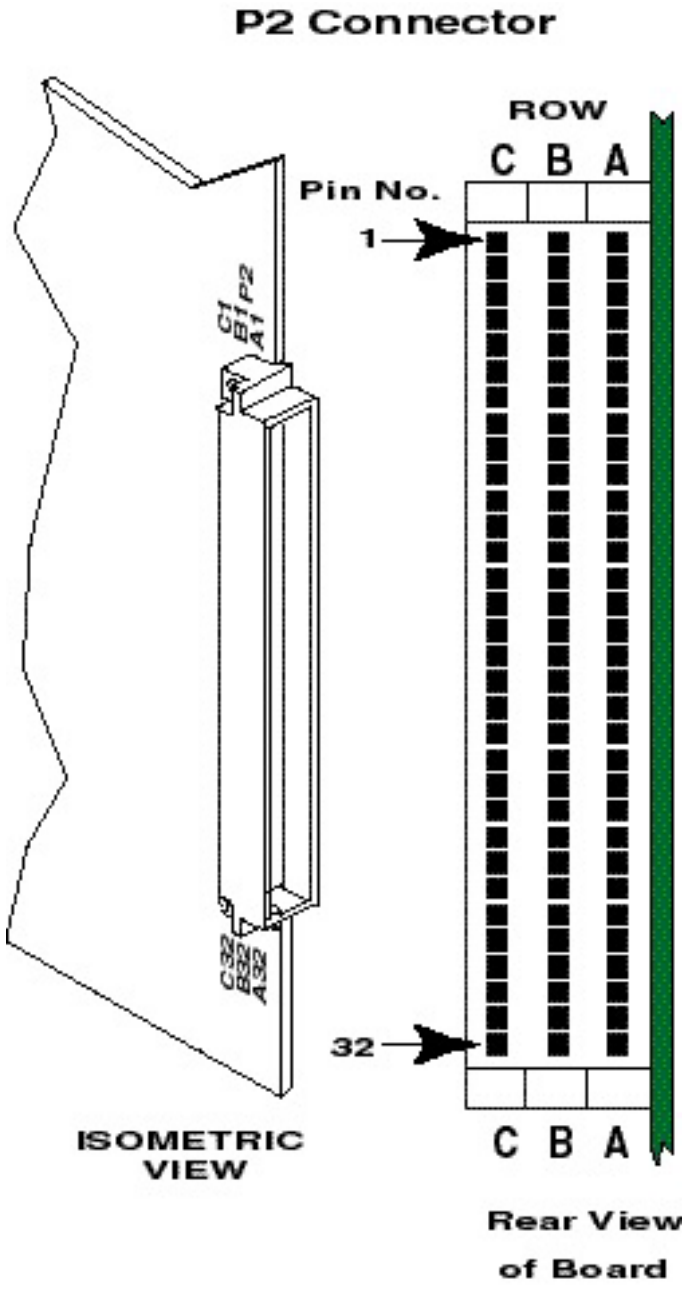
P4		P4	
ROW C Pin	**CHANNEL No.**	**ROW C Pin**	**CHANNEL No.**
32	63	16	47
31	62	15	46
30	61	14	45
29	60	13	44
28	59	12	43
27	58	11	42
26	57	10	41
25	56	09	40
24	55	08	39
23	54	07	38
22	53	06	37
21	52	05	36
20	51	04	35
19	50	03	34
18	49	02	33
17	48	01	32
All Pins in Row B are grounded.			

Table 2-7 P4 Pin - Channel Assignments (Row A)

P4		P4	
ROW A Pin	**CHANNEL No.**	**ROW A Pin**	**CHANNEL No.**
32	31	16	15
31	30	15	14
30	29	14	13
29	28	13	12
28	27	12	11
27	26	11	10
26	25	10	09
25	24	09	08
24	23	08	07
23	22	07	06
22	21	06	05
21	20	05	04
20	19	04	03
19	18	03	02
18	17	02	01
17	16	01	00
All Pins in Row B are grounded.			

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Figure 2-13 P2 Connector Pin Layout



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Table 2-8 P2 Connector Pin Assignments

Pin No.	ROW A	ROW B	ROW C
1	NC	+5 V	GND
2	NC	GND	VEXT CH 120_127
3	NC	N/C	GND
4	NC	N/C	VEXT CH 112_119
5	NC	N/C	GND
6	NC	N/C	VEXT CH 104_111
7	NC	N/C	GND
8	NC	N/C	VEXT CH 96_103
9	NC	N/C	GND
10	NC	N/C	VEXT CH 88_95
11	NC	N/C	GND
12	NC	GND	VEXT CH 80_87
13	NC	+5 V	GND
14	NC	D16	VEXT CH 72_79
15	NC	D17	GND
16	NC	D18	VEXT CH 64_71
17	NC	D19	GND
18	NC	D20	VEXT CH 56_63
19	NC	D21	GND
20	NC	D22	VEXT CH 48_55
21	NC	D23	GND
22	NC	GND	VEXT CH 40_47
23	NC	D24	GND
24	NC	D25	VEXT CH 32_39
25	NC	D26	GND
26	NC	D27	VEXT CH 24_31
27	NC	D28	GND
28	NC	D29	VEXT CH 16_23
29	NC	D30	GND
30	NC	D31	VEXT CH 8_15
31	NC	GND	GND
32	NC	+5 V	VEXT CH 0_7

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3 • Programming

The VMIVME-1129 is a snapshot board. The user simply performs a read or write operation within the board's address space and the appropriate transfer is performed. The only setup involved with this board deals with the Control and Status Register. Once this register is programmed, the user performs data transfers to or from this board. The following table (***Table 3-1*** below) lists the address map for the VMIVME-1129. X's in the address are determined by the address select header E17. This board will respond to nonprivileged, supervisory, or both accesses depending on how the jumpers are positioned.

Table 3-1 Address Map

RELATIVE ADDRESS*	MNEMONIC	NAME/FUNCTION
XXX0 0000	IDU	BOARD ID REGISTER UPPER BYTE
XXX0 0001	IDL	BOARD ID REGISTER LOWER BYTE
XXX0 0010	CSRU	CSR UPPER BYTE
XXX0 0011	CSRL	CSR LOWER BYTE
XXX0 0100 through XXX0 1111		NOT USED**
XXX1 0000	DR0U	TEST REGISTER 0 UPPER BYTE
XXX1 0001	DR0L	TEST REGISTER 0 LOWER BYTE
XXX1 0010	DR1U	TEST REGISTER 1 UPPER BYTE
XXX1 0011	DR1L	TEST REGISTER 1 LOWER BYTE
XXX1 0100	DR2U	TEST REGISTER 2 UPPER BYTE
XXX1 0101	DR2L	TEST REGISTER 2 LOWER BYTE
XXX1 0110	DR3U	TEST REGISTER 3 UPPER BYTE
XXX1 0111	DR3L	TEST REGISTER 3 LOWER BYTE
XXX1 1000	DR4U	TEST REGISTER 4 UPPER BYTE
XXX1 1001	DR4L	TEST REGISTER 4 LOWER BYTE
XXX1 1010	DR5U	TEST REGISTER 5 UPPER BYTE
RELATIVE ADDRESS*	MNEMONIC	NAME/FUNCTION
XXX1 1011	DR5L	TEST REGISTER 5 LOWER BYTE
XXX1 1100	DR6U	TEST REGISTER 6 UPPER BYTE
XXX1 1101	DR6L	TEST REGISTER 6 LOWER BYTE
XXX1 1110	DR7U	TEST REGISTER 7 UPPER BYTE
XXX1 1111	DR7L	TEST REGISTER 7 LOWER BYTE

* The relative address is defined by A4-A0. All other address lines help to define the base address.

** A read or write access to these addresses will not result in a bus error; however, any data written to these addresses will not be stored. Any data read from these addresses will not be meaningful.

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3.1 Board ID Register (BD ID)

The BD ID Register is a read-only register. Its data is fixed at $2900. You can write to this address; however, the data you write will be lost and there will be no effect on the board. If you choose to write to this location, the board will DTACK to prevent any bus errors. The BD ID can be read as a word or as two bytes. The following table (*Table 3-2* below) shows the bit values for this register.

Table 3-2 BD ID Register Bit Map

XXX0 0000		BOARD ID UPPER BYTE			(Read Only)		
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
L	L	H	L	H	L	L	H
XXX0 0001		BOARD ID LOWER BYTE			(Read Only)		
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 23**
L	L	L	L	L	L	L	L

3.2 Control and Status Register Bit Definitions

The Control and Status Register (CSR) is a 16-bit register that is used to control the board's Fail LED and the test registers' outputs. *Table 3-3* shows the bits used to perform these functions. Bit 15 controls the LED. Bit 14 controls the test registers for P4 and P3 Row A (Channels 0 through 31 and Channels 64 through 95) while Bit 13 controls the test registers for P4 and P3 Row C (Channels 32 through 64 and Channels 96 through 127). P3 and P4 channel assignments are shown in *Table 2-4* and *Table 2-5* on page 26 (P3) and *Table 2-6* and *Table 2-7* on page 27 (P4). The Bit map for each channel is shown in *Table 3-4* on page 32.

All of these bits are active low. All of the other bits are not used. When the board is powered up or after a system reset, these signals are activated. Writing a logic high into each bit location will deactivate them. Writing a logic low in these locations will subsequently activate the function. Each of the functions are independent of the others. Thus, the LED can be turned ON and OFF as you wish.

Table 3-3 CSR Bit Map

XXX0 0010		CSR UPPER BYTE			(Bits 12 through 08 are Read Only)		
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
FAIL_L	TEST_ MODE_ P3/P4 ROW A_L	TEST_ MODE_ P3/P4 ROW C_L	L	L	L	L	L
XXX0 0011		CSR LOWER BYTE			(Read Only)		
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
L	L	L	L	L	L	L	L

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3.3 Input Registers Bit Definitions

The following table lists the input channels and their associated register bit locations. The internal data bit can be used as a guide to locate an input channel when you are doing a longword transfer. When doing word or byte transfers, the even address bytes will go to bits 15 through 8 on the VMEbus data bus while the odd address bytes go to bits 7 through 0.

Table 3-4 Input Data Registers Bit Map

XXX1 0000		DATA REGISTER 0 UPPER BYTE				(Read /Write)	
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120
XXX1 0001		**DATA REGISTER 0 LOWER BYTE**				**(Read /Write)**	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	CH 112
XXX1 0010		**DATA REGISTER 1 UPPER BYTE**				**(Read /Write)**	
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104
XXX1 0011		**DATA REGISTER 1 LOWER BYTE**				**(Read /Write)**	
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 103	CH 102	CH 101	CH 100	CH 099	CH 098	CH 097	CH 096
XXX1 0100		**DATA REGISTER 2 UPPER BYTE**				**(Read /Write)**	
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH 095	CH 094	CH 093	CH 092	CH 091	CH 090	CH 089	CH 088
XXX1 0101		**DATA REGISTER 2 LOWER BYTE**				**(Read /Write)**	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH 087	CH 086	CH 085	CH 084	CH 083	CH 082	CH 081	CH 080
XXX1 0110		**DATA REGISTER 3 UPPER BYTE**				**(Read /Write)**	
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 079	CH 078	CH 077	CH 076	CH 075	CH 074	CH 073	CH 072
XXX1 0111		**DATA REGISTER 3 LOWER BYTE**				**(Read /Write)**	
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 071	CH 070	CH 069	CH 068	CH 067	CH 066	CH 065	CH 064
XXX1 1000		**DATA REGISTER 4 UPPER BYTE**				**(Read /Write)**	
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH 063	CH 062	CH 061	CH 060	CH 059	CH 058	CH 057	CH 056
XXX1 1001		**DATA REGISTER 4 LOWER BYTE**				**(Read /Write)**	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH 055	CH 054	CH 053	CH 052	CH 051	CH 050	CH 049	CH 048
XXX1 1010		**DATA REGISTER 5 UPPER BYTE**				**(Read /Write)**	
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 047	CH 046	CH 045	CH 044	CH 043	CH 042	CH 041	CH 040
XXX1 1011		**DATA REGISTER 5 LOWER BYTE**				**(Read /Write)**	
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 039	CH 038	CH 037	CH 036	CH 035	CH 034	CH 033	CH 032
XXX1 1100		**DATA REGISTER 6 UPPER BYTE**				**(Read/Write)**	

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Table 3-4 Input Data Registers Bit Map (Continued)

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH 031	CH 030	CH 029	CH 028	CH 027	CH 026	CH 025	CH 024

XXX1 1101		DATA REGISTER 6 LOWER BYTE				(Read/Write)	
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH 023	CH 022	CH 021	CH 020	CH 019	CH 018	CH 017	CH 016
XXX1 1110		**DATA REGISTER 7 UPPER BYTE**				**(Read/Write)**	
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH 015	CH 014	CH 013	CH 012	CH 011	CH 010	CH 009	CH 008
XXX1 1111		**DATA REGISTER 7 LOWER BYTE**				**(Read/Write)**	
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 007	CH 006	CH 005	CH 004	CH 003	CH 002	CH 001	CH 000



NOTE

Input channels CH00 through CH63 are routed from input connector P4 while inputs CH64 through CH127 are routed from the P3 connector.

3.4 Built-In-Test Programming

Built-in-test is activated when either or both test mode bits in the CSR are cleared. When test mode is active, data written to a data register will overwrite the external inputs. Then when the same register is read, the data stored in the test register should be read. If there is a difference, then the board has a problem. When you are through testing the board, the test mode bits **MUST** be set to a one (1) in the CSR; otherwise, the board will not be able to monitor the external inputs.

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