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GE Industrial Systems

# Digital Signal Processor Control Board IS200DSPXH_A – C

**Safety Symbol Legend**

**Warning**

**Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in injury or death.**

**Caution**

**Indicates a procedure or condition that, if not strictly observed, could result in**

*These instructions do not purport to cover all details or variations in equipment, or to provide for every possible contingency to be met during installation, operation, and maintenance. If further information is desired, or if particular problems arise that are not covered sufficiently for the purchaser's purpose, the matter should be referred to GE Industrial Systems.*

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**damage to or destruction of equipment.**

***Note*** Indicates an essential or important procedure or statement.


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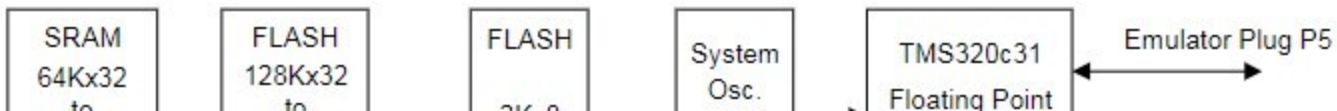


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# Functional Description

The IS200DSPX Digital Signal Processor Control Board (DSPX) is the primary controller for the bridge and motor regulator and gating functions for Innovation Series™ drives. It also controls generator field control functions for EX2100 exciters. The board provides logic, processing, and interface functions.

The DSPX board includes a high performance digital signal processor (DSP), standard memory components, and an application specific integrated circuit (ASIC) that performs custom logic functions, as shown in Figure 1.



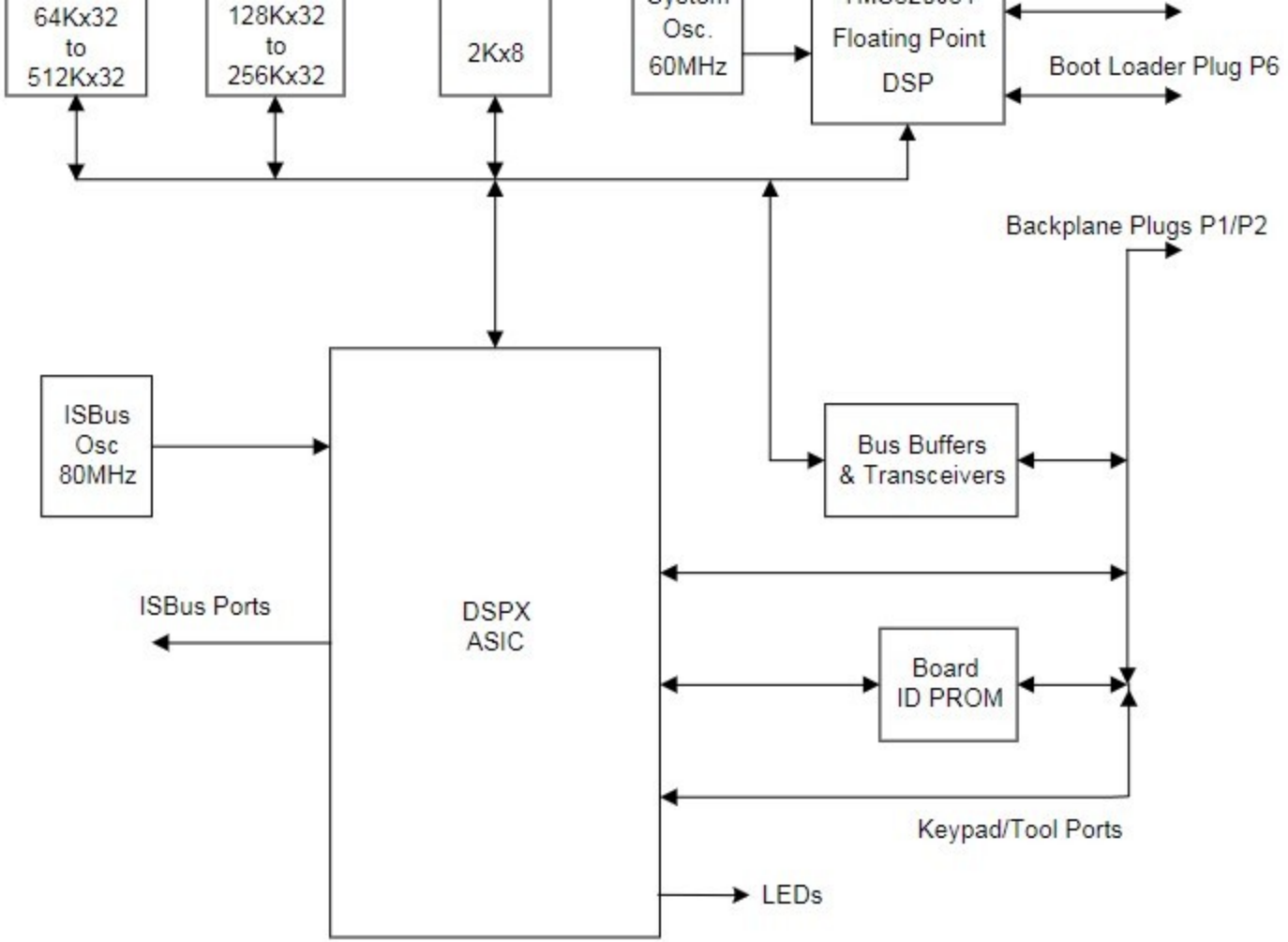



*Figure 1. DSPX Board Block Diagram*

There are several variations of the DSPX board. Refer to the section, *Board Identification,* for details.

## Standard Hardware Features

*Refer to Figure 2.*

The DSPX's Digital Signal Processor (DSP) runs at 60 MHz. Four external interrupts to the DSP are provided during normal operation:

- Stack overflow (INT0)
- Inner loop load pulse (INT1)
- Two configurable inputs (INT2, INT3)

The following types of memory are provided on the DSPX board:

- FLASH memory for DSP boot images, code execution, and configurable item storage, along with system history records
- RAM for data storage and code execution
- NVRAM for nonvolatile data storage
- Add-only memory for board revision identification

## Specialized Hardware Functions

*An ASIC revision identification register that is readable by the DSP is provided.*

Specialized functions of the DSPX board are provided through custom logic in Field Programmable Gate Arrays (FPGA) or ASICs with supporting circuits as required. Most specialized and support functions are contained in a single ASIC. Refer to Figure 2, *DSPX Board ASIC Block Diagram*.

Four serial interfaces to P1 are provided as follows:

- Two 5 Mb/s ISBus™ interfaces used as either master or slave
- One asynchronous TTL interface for a pc-based configuration tool, including RX, TX, and TXEN/RTS data signals
- One asynchronous TTL interface to a programmer board, including RX, TX, and RTS data signals

Synchronizing *load pulse* signals perform the following functions:

- An inner loop load pulse signal captures the values of I/O such as bridge, motor, or generator voltages and current VCOs, tachometer counters, and discrete inputs. It can also synchronize the ISBus channels, the software, and gating outputs to bridges.
- At a sub-multiple or multiple of the inner loop load pulse, an application loop load pulse signal is used to capture values of other application VCOs and optionally the tachs.

**Note** To facilitate firmware synchronizing of the load pulse signals, a 6-bit register increments on each inner loop load pulse and resets on each application loop load pulse.

Stack overflow detection is provided for both the foreground stack (from internal memory) and the background stack (from external SRAM). Interrupt INT0 is generated if either stack overflows. If both stacks overflow, a hard reset is generated. A configuration register is provided to allow the stack overflow reset to be disabled.

A watchdog timer is enabled and periodically toggled by the DSP (toggle interval is configurable). A time-out of the watchdog timer will generate a hard reset. A 24-bit free running timer is also provided and used as a reference for certain functions.



*A marker pulse is used to latch or reset the up/down counter.*

Five differential (HIFI) pair application inputs may be used as two quadrature incremental tach interfaces (one with marker capability). The signals drive two 16-bit up/down counters. It maintains its present state when the inputs are at the same level, and changes state when the inputs are differentially opposite.

A 5 MHz timer resets each time the counter increments or decrements, and a state register records the direction of the last count. Associated with each of these counters, timers, and registers is a capture register that can be configured to capture the values on the occurrence of either the inner loop load pulse or the application loop load pulse.

The five differential HIFI inputs can be used as application layer VCO counters or single-channel tach interfaces. Five 16-bit counters increment on the differentially decoded and filtered inputs. These counter values are captured into registers the DSP can read by the application loop load pulse.

The five differential HIFI inputs can also be used as up to ten discrete inputs. Each input is filtered for three system clock cycles and directly readable by the DSP in a buffer.

*Miscellaneous expansion board I/O (SYNC_OUT) is provided for synchronizing functions at the BIC_ board layer.*

Six inputs from the backplane are digitally filtered and input to the VCO counters. These are 16-bit counters with capture registers latched by the inner loop load pulse and readable by the DSP. The inputs come from technology specific I/O cards such as BIC (bridge interface) or exciter interface cards.

Two PWM outputs are provided. These outputs are at 24 kHz fixed frequency with 10-bit resolution each and occupy one 20-bit register. These can be used to drive instrumentation meters or other outputs.

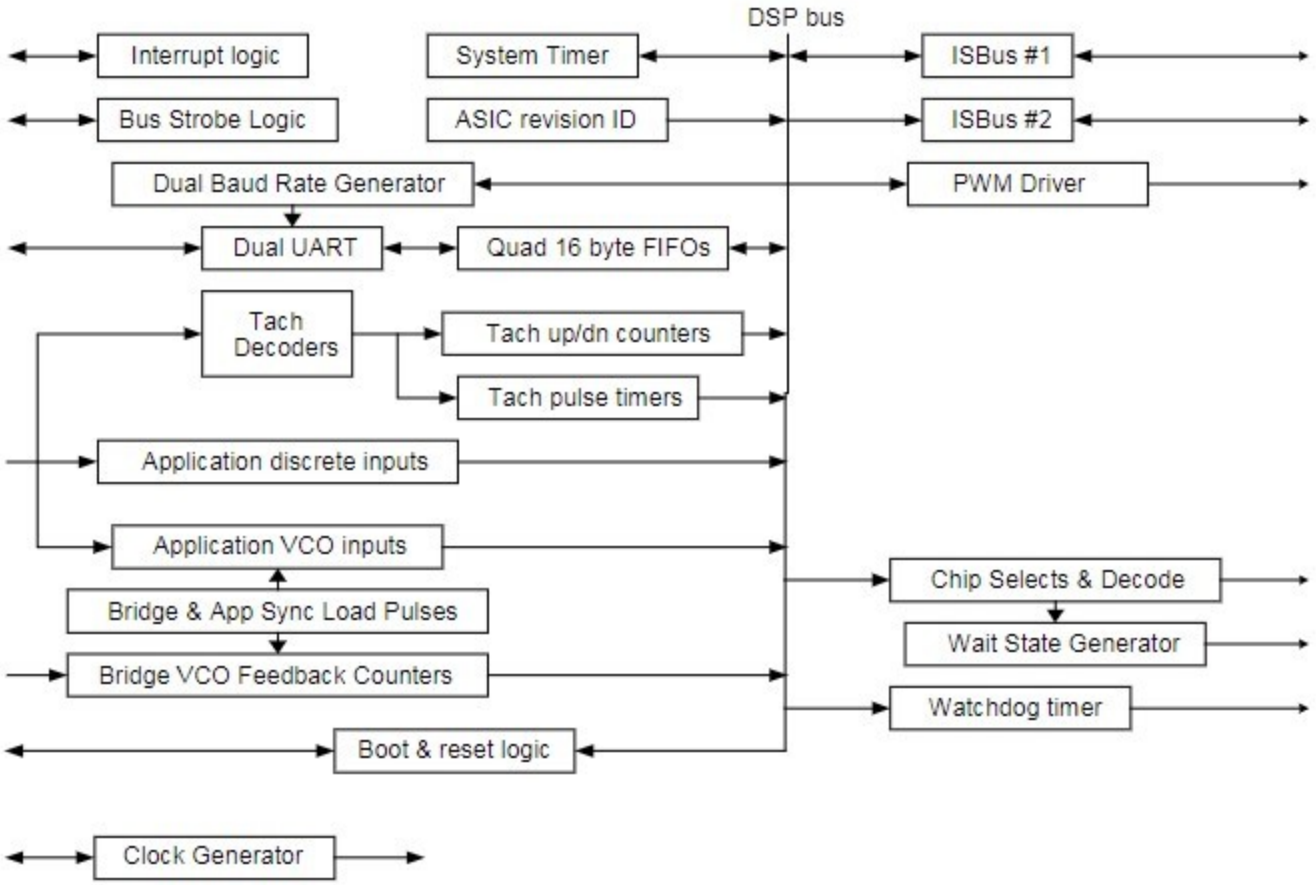



*Figure 2. DSPX Board ASIC Block Diagram*

## Onboard Firmware

Onboard firmware is stored in Flash memory. There are three main types:

- Boot loader controls the power up sequence and should not be reloaded in the field.
- Application code defines the specific control functions for the drive or exciter product. This code is loaded through the Tool port on the exciter.
- Configuration parameters are loaded using the toolbox. Exciter parameters are loaded over the Unit Data Highway. Drive parameters are loaded through a serial port, ISBus, or Ethernet to ACL_, if applicable.

# Application Data

*The DSPX has no fuses, adjustable hardware devices, or user testpoints.*

The DSPX board is mounted in the board rack and connects to the backplane through a 4-row, 128-pin DIN connector (P1). In the EX2100, the DSPX is attached to another board, the EISB. These two boards can be detached if required, refer to the section, *How To Replace The Board*.

Refer to Figure 3 and Figure 4 for the board layout.

## Indicating Lights

The DSPX includes two LEDs on its front panel.

| LED | Nomenclature | Color | Description |
|---|---|---|---|
| DS1 | FAULT | Red | Fault LED driven by the DSP<br>ON or flashing: A fault has occurred or during reset<br>OFF: No faults are present |
| DS2 | STATUS | Green | Status monitor LED driven by the DSP<br>Flashing: Running<br>ON: Stopped<br>OFF: A fault has occurred or during reset |

## I/O Definitions

The DSPX includes three I/O connectors as follows:

- P1 backplane connector
- P5 DSP emulator port
- P6 engineering monitor port

*The 5 V power supply input (P5, –2%/+5%) is also through P1.*

The P1 connector provides memory mapped process bus address space with four chip select signals to support interfaces to bridge and customer input/output (I/O). It also contains individual controls for a standard UART serial interface to a programmer board and a configuration tool, and two additional ISBus proprietary serial interfaces, for Application Control Layer (ACL) or local expansion functions.

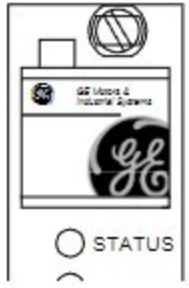
The P5 emulator port (located on the board front panel) provides an interface to the TI emulator port. It provides a scan interface (similar to JTAG) to allow emulation as well as FLASH programming.



The P6 engineering monitor port (located on the board front panel) connects to the DSP synchronous serial port (at TTL levels) and allows connection to a terminal for GE engineering use only.

***Note*** The P6 and P7 test point ports (located on the board surface) are for test/development use only.

Refer to the following tables for pin signal descriptions.



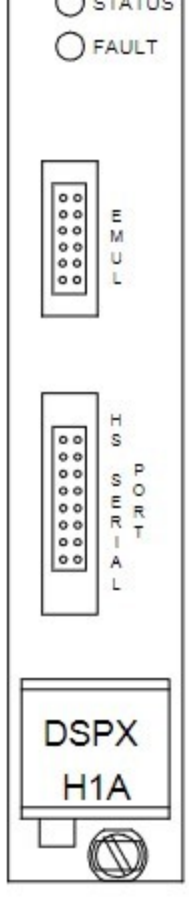



*Figure 3. DSPX Board Front Panel (H1A, H1B, H1C, H2B, or H2C)*

# Renewal/Warranty Information

When ordering a replacement board for a GE drive or exciter, you need to know:

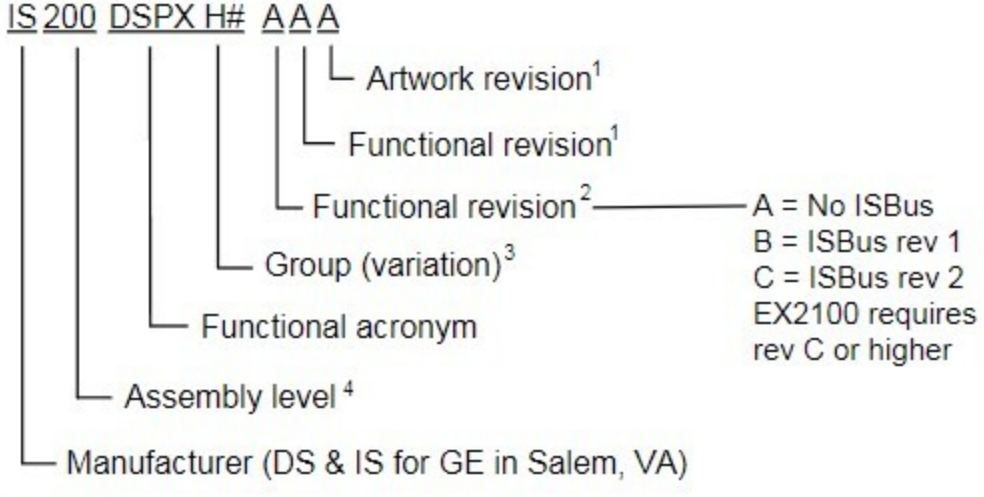
- How to accurately identify the part
- If the part is under warranty
- How to place the order

This information helps ensure that GE can process the order accurately and as soon as possible.

## Board Identification

A printed wiring board is identified by an alphanumeric *part (catalog) number* located near its edge. *Board Part Number Conventions* explains the structure of the part number.

The board's functional acronym is normally based on the *board description*, or name. For example, the *DSPX* board is described as the *Digital Signal Processor Control Board*.




[1]Backward compatible
[2]Not backward compatible
[3]*G* = normal coating; *H* = conformal coating
[4]*200* indicates a base-level board; *215* indicates a higher-level assembly or added components (such as PROM)

*Board Part Number Conventions*

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