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GE Industrial Systems

Application Control Layer Module (ACL)
IS215ACL_H_A_ _

Safety Symbol Legend

Warning

Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in personal injury or death.

Caution

Indicates a procedure or condition that, if not strictly observed, could result in damage to or destruction of equipment.

Note Indicates an essential or important procedure or statement.

These instructions do not purport to cover all details or variations in equipment, nor to provide for every possible contingency to be met during installation, operation, and maintenance. If further information is desired or if particular problems arise that are not covered sufficiently for the purchaser's purpose, the matter should be referred to GE Industrial Systems.

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Section **Page**

Functional Description 2
- Hardware Features 4
- Software Features 7
- GE Control Systems Toolbox 8
- Related Documents 9

Application Data 10
- Power Requirements 10
- Adjustable Hardware 10
- Connector Pin Signals 10
- Status and Fault Indicators 10

Board/Module Replacement 16
- Handling Precautions 16
- For Drives 16
- For Exciters (Offline) 17
- For Redundant Exciters (Online) 18

Renewal/Warranty Replacement 20
- Board Identification 20
- Warranty Terms 20

Placing the Order 21

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Functional Description

The IS215ACL_ Application Control Layer Module (ACL) is a microprocessor-based master controller used to perform multiple duties over communication networks such as Ethernet™ and ISBus. The ACL mounts in a standard Innovation Series™ drive or EX2100 exciter board rack and occupies two half-slots. The ACL and board rack are located in the control cabinet. In drive applications, the ACL's P1 connector (4-row 128-pin) plugs into the Control Assembly Backplane Board (CABP). In the EX2100 exciter, the ACL mounts in the Exciter Backplane (EBKP).

The ACL can be ordered in two different I/O configurations as follows:

- IS215ACLAH1A Module with one 10BaseT Ethernet port and two serial communication ports (COM1 and COM2), as used in the EX2100
- IS215ACLIH1A Module with one 10BaseT Ethernet port, two serial

communication ports (COM1 and COM2), and two ISBus ports

Refer to Figure 1 for the module faceplates.

Optional hardware accessories are available. These items must be ordered separately from the ACL and include the following:

- Serial adapter cable (336A4929G1)
- Serial cable (336A3582P1)

Primary features of the ACL core software include:

- Control blockware language and library
- Online application configuration loading
- I/O points and internal Booleans forcing
- Diagnostics for broken run/start permissives
- Application level alarm messages
- Non-volatile flash memory
- Toolbox interface and support through Ethernet
- Application control for Innovation Series drives

Note Do not reset or power down the ACL when the FLSH LED is lit (see Figure 1 for location). Doing so may corrupt the flash file system and a flash reload may be required.

Hardware Features

Integrated circuits on the ACL provide the following features:

- Central processing unit (CPU)
- Peripheral component interconnect (PCI) controller
- 128 K byte level 2 cache
- 8 MB dynamic random access memory (DRAM)
- 4 MB flash memory basic input/output system (BIOS)
- Ethernet
- Bus target interface
- Serial ports COM1 and COM2
- Ethernet
- ISBus communication ports (IS215ACLI only)

Refer to Figure 3 for an ACL functional flow diagram.

CPU incorporates 16 K byte of internal L1 cache. It is a 486 type processor operating at 100 MHz.

PCI controller manages all memory, I/O, and configuration transfers to and from the PCI bus. Memory and I/O transfers are normal reads/writes from the CPU. Configuration reads/writes must be accessed as 32-bit transfers by writing the configuration address to an I/O port, and then accessing another I/O port to read/write the configuration register.

128 KB Level 2 (L2) Cache is controlled by the PCI controller. The L2 cache is preset to produce 152 Ns cache line fills between the L2 cache and the L1 cache.

BIOS is a 1 MB (128 KB x 8) 5 V flash memory device and mounts in a socket on the ACL. See Table 4, *Basic BIOS Settings*, for settings accessible through the toolbox, as well as through the setup utility. The BIOS will redirect the video display to COM1 if a video BIOS is not found (if there is no PC/104 VGA board installed).

The flash memory BIOS is divided into three sections:

- main BIOS
- BIOS setup utility
- GE Industrial Systems Extended BIOS

Note To corrupt the CMOS for reset, remove power and then short all three pins of J1 together for ten seconds, then reset the drive. (Refer to Figure 4 for J1 location.)

DRAM consist of 8 MB of 60 Ns EDO nonparity. The PCI controller controls access to the DRAM.

Bus Target interface provides a bridge between the PCI bus and the ACL local bus ISA controller. The interface can select up to four local bus devices, although only three are used in the drives. Figure 2 shows the Bus Target interface connection.

DPRAM can only be used on modules that do not use the ISBus.

Dual-Ported RAM (DPRAM) (8k x 8 size) is located on the local bus and identified as Device0. The ACL communicates with the Digital Signal Processor board (DSPX) through the 32-bit P1 bus and the DPRAM. The DSPX board generates the P1 bus cycles. If simultaneous accesses occur on the same address, the ACL may hold the DSPX board in an OFF condition for a maximum of 100 Ns.

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