PCI-40A

Quad IndustryPack®
Carrier for the PCI Bus

User Manual

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PCI-40A
Quad IndustryPack®
Carrier Board For The
PCI Bus

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Product Description

The PCI-40A IndustryPack® carrier board provides four IndustryPack slots on a single desktop or industrial PCI slot card. The IndustryPack bus clock is software-selectable on a per-slot basis between 8 and 32 MHz.

The standard 8 MByte memory space is available for each IndustryPack site. High-speed 32-bit PCI host address space permits desirable linear mapping and fixed address partitions of memory, I/O, and ID spaces for each IndustryPack module.

The PCI-40A uses a PLX PCI9080 controller as the PCI bus interface chip and Altera FPGA logic, which provides fully configurable PCI interrupt vector space. The PCI bus interface supports 5.0 V signaling.

Each IndustryPack site has an adjacent 50-pin I/O connector for exiting the host system through the PCI slot panel. One connector is accessible via the rear panel. The standard connector permits most of SBS Technologies transition modules and terminal blocks to be used.

The PCI-40A meets the PCI specification and conforms to the VITA-4 IndustryPack Logic Interface Specification. This guarantees compatibility with a wide range of IndustryPacks.

Key Features

- Four IndustryPack slots on a full-length PCI slot board
- I/O via four 50-pin keyed, shrouded ribbon cable headers
- Switchable 8/32 MHz IndustryPack bus
- LEDs for CPU access and power monitor
- Filtered power rails and resettable fuses
- Interrupt acknowledge space for retrieving IndustryPack vectors
- Software-compatible with the PCI-40A
- Reduced memory-map version available by special order

Address Map

The PCI-40A is mapped into the PCI memory space. PCI I/O space is not used. IP I/O, ID, memory, and interrupt vector registers are mapped in the PCI memory space. Two address maps are supported: a small memory map consuming 32 KBytes and a standard memory map consuming 64 Mbytes of address space. Size is an order option.

The PCI bus allocates only one interrupt line to the PCI-40A per the PCI 2.1 Specification. However, the PCI-40A provides an interrupt status register that quickly identifies which IP slot generated the interrupt.

I/O Connections

The four IP positions are referred to as slots and identified by the letters A, B, C, and D. Each slot has an upright 50-pin flat cable header accessible through the rear panel of the PCI-40A for I/O connections. The I/O connectors are mounted directly on the PCI-40A board to provide a modular and reliable cabling system with inherent strain relief. I/O cables may be inserted or removed without removing the PCI-40A from the chassis. IPs in slots A and B may be installed or removed without interfering with the I/O cabling.

PCI-40A provides protected filtered +5V, +12V, and -12V supplies to each IP by means of passive "T" filters, capacitors, and fuses. The three terminal filters provide excellent RF rejection of power supply conducted noise. This permits use of precision analog IndustryPacks together with high speed digital IndustryPacks in the same PCI-40A. The IP slots feature other power handling features such as separated ground planes to reduce conducted noise.

PCI-40A IP interface is compliant with the **ANSI/VITA 4 IP Module Specification Revision 1.0**. This guarantees compatibility with the wide range of IPs currently available and planned.

Figure 1 is a block diagram of the PCI-40A.

Block Diagram

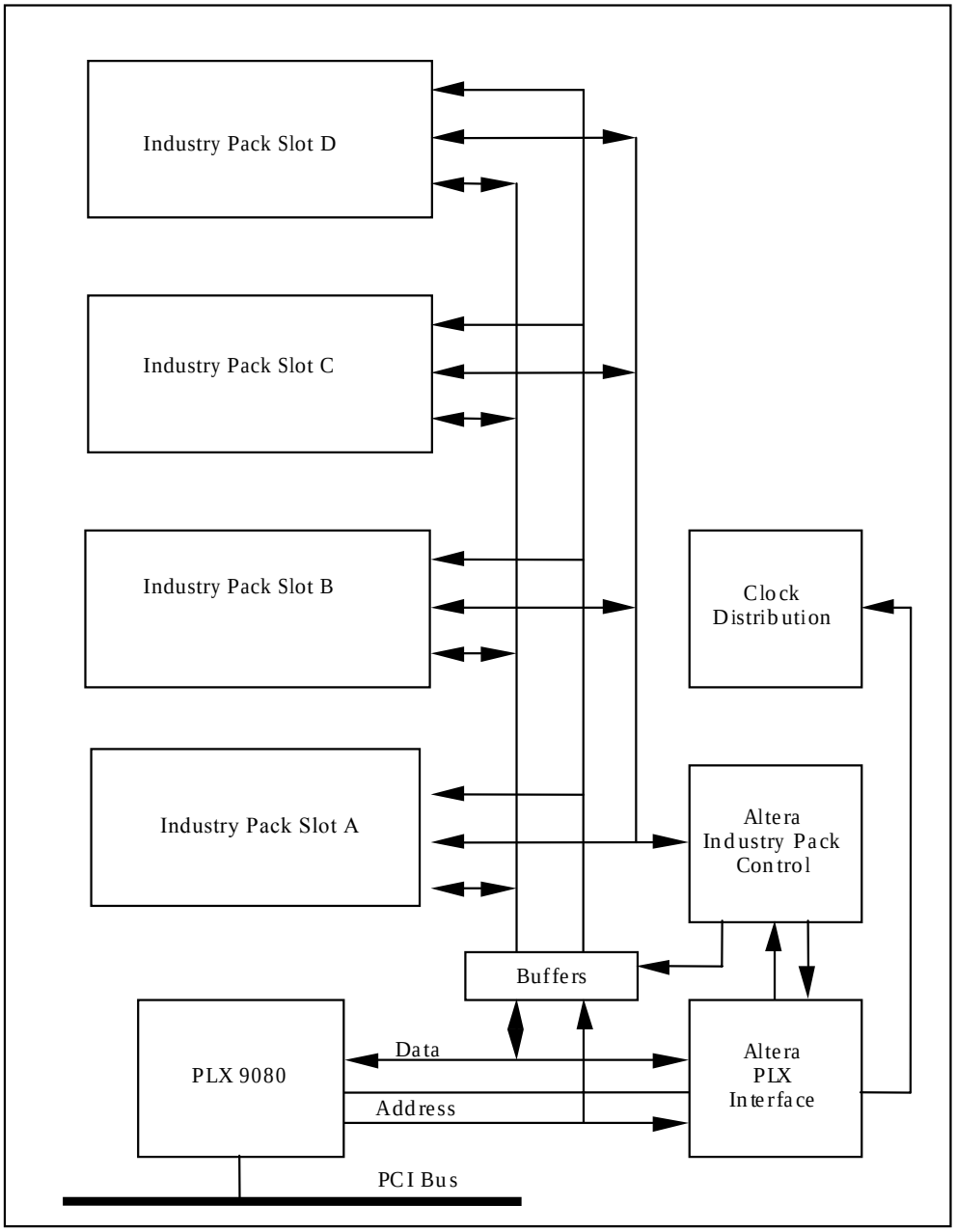

Figure 1. Block Diagram

PCI-40A Hardware Overview

Addressing Overview

The PCI-40A is mapped into the PCI memory space. PCI I/O space is not used. IP I/O, ID, memory, and interrupt vector registers are mapped in the PCI memory space. Two address maps are supported, a small memory map consuming 32 KBytes and a standard memory map consuming 64 MBytes of address space. The size is programmed into the PCI-40A configuration EEPROM.

IndustryPacks have four separate address spaces across the IP Logic interface: ID, I/O, memory, and (interrupt) vector. It is the job of the carrier board, the PCI-40A, to map these spaces into the host's address space. The PCI-40A maps all IP spaces into the PCI bus' memory space.

The IP I/O, ID, and vector spaces are fixed size. The IP memory size can vary up to 8 MB per IP. The PCI-40A has two address map options. The PCI-40A allocates 8 MBytes of IP memory space to each IP slot and consumes a total of 64 MBytes of space on the PCI bus. The PCI-40A-R allocates 2 KBytes of IP memory space to each IP slot and consumes a total of 64 KBytes of space on the PCI bus. The lowest 16 KBytes is the same for both memory maps and provides the I/O, ID, and INT spaces for the four slots plus local register decoding.

Selecting the PCI-40A Base Address

PCI-40A base address and address map are selected through the PCI configuration registers. Unlike VME and ISA systems, the base addresses in PCI systems are set at run time by the BIOS. The BIOS uses PCI configuration cycles to query each slot on the PCI bus. Upon detecting a card, the BIOS writes all Fs to the Base Address Registers (BARs) and then reads them back. The card responds by placing 0s in all the address bits that it uses. The BIOS uses this information to determine how much memory the card is requesting, then assigns an address and writes it back to the BAR.

There are three base address registers for the PCI-40A. The first, BAR0, is the address of the PCI-9080 PCI accessible registers in PCI memory space. The second, BAR1, is the address of the PCI-9080 PCI accessible registers in PCI I/O space. The third address, BAR2, is the address to use for accessing the IPs and PCI-40A Local Control registers in PCI memory space. The PCI-40A does not use the PCI-9080 BAR1 for local spaces. The addresses depicted in Figures 2 and 3 are relative to contents of BAR2. Please refer to the programming section for more information.

Note that addresses within each IP's own space are specific to that IndustryPack. Refer to that IP's User Manual for information relating to the IP specific addressing.

Memory Maps

Address		Name
From	To	
0000 0500	0000 07FF	PCI-40A Local Control
0000 1000	0000 10FF	SlotA I/O
0000 1100	0000 11FF	SlotA ID
0000 1200	0000 12FF	SlotA INT
0000 2000	0000 20FF	SlotB I/O
0000 2100	0000 21FF	SlotB ID
0000 2200	0000 22FF	SlotB INT
0000 3000	0000 30FF	SlotC I/O
0000 3100	0000 31FF	SlotC ID
0000 3200	0000 32FF	SlotC INT
0000 4000	0000 40FF	SlotD I/O
0000 4100	0000 41FF	SlotD ID
0000 4200	0000 42FF	SlotD INT
0100 0000	017F FFFF	SlotA MEM
0180 0000	01FF FFFF	SlotB MEM
0200 0000	027F FFFF	SlotC MEM
0280 0000	02FF FFFF	SlotD MEM

Figure 2. PCI-40A Memory Map - 64 MBytes

Address		Name
From	To	
0000 0500	0000 07FF	PCI-40A Local Control
0000 1000	0000 10FF	SlotA I/O
0000 1100	0000 11FF	SlotA ID
0000 1200	0000 12FF	SlotA INT
0000 2000	0000 20FF	SlotB I/O
0000 2100	0000 21FF	SlotB ID
0000 2200	0000 22FF	SlotB INT
0000 3000	0000 30FF	SlotC I/O
0000 3100	0000 31FF	SlotC ID
0000 3200	0000 32FF	SlotC INT
0000 4000	0000 40FF	SlotD I/O
0000 4100	0000 41FF	SlotD ID
0000 4200	0000 42FF	SlotD INT
0000 5000	0000 57FF	SlotA MEM
0000 5800	0000 5FFF	SlotB MEM
0000 6000	0000 67FF	SlotC MEM
0000 6800	0000 6FFF	SlotD MEM

Figure 3. PCI-40A-R Memory Map - 32 KBytes

I/O Space

The I/O space on each IP is fixed at 128, 16-bit words (256 Bytes). (The I/O space above 64 words is for future use.) This occupies a space of $100 Bytes. The four IP I/O spaces are accessible at fixed offsets from the PCI-40A's Base Address, as shown in Figures 2 and 3. Typically, IPs do not fully decode their entire 64 long word space. Some IPs support both word and byte accesses to I/O

space, while others require accesses to be byte only or word only. See each IP's User Manual for details.

Caution: Each IP may or may not fully decode its I/O space. Incomplete decoding will often cause IP registers to appear in multiple places within the 64 word I/O space. IPs may have different read and write maps. Some IPs require 16-bit accesses only. If an IP does not respond to an invalid access, then the PCI-40A bus timer will respond (if enabled) and cause an interrupt to alert the software.

ID Space

Every IP must have an ID PROM. The ID space on each IP is fixed at 128, 16-bit words. (The ID space above 32 Bytes is for future use.) The ID PROM is required by the ANSI/VITA 4 IP Module Specification 1.0. ID PROM data is at least 12 Bytes and is found in the lowest byte of the first 12 words. Newer IndustryPacks may support the ID PROM Data Format II that uses 16-bit words instead of 8-bit bytes. The ID PROM provides information about the IP, which is defined in the IndustryPack Specification and the IP's User Manual. This information includes the IP's manufacturer, model code, and manufacturing revision level. It may also include a driver identification code and calibration information.

Figure 4 shows the required information in each ID PROM. For additional information, see the IndustryPack Specification and the Users Manual for each IP.

$FF 2A	user space	
2*nn $18	pack specific space	
$16	CRC	
$14	No of bytes used	[= nn]
$12	Driver ID, high byte	
$10	Driver ID, low byte	
$0E	reserved	($00)
$0C	Revision	
$0A	Model No	
$08	Manufacturer ID	
$06	ASCII "C"	($43)
$04	ASCII "A"	($41)
$02	ASCII "P"	($50)
$00	ASCII "I"	($49)

Figure 4. Required IP ID PROM Information

Memory Space Accesses

The memory space of an IP is optional, and varies in size up to 8 MBytes per IP. Implementation among IPs varies widely. It may be used for RAM, EPROM, Flash, video frame buffers, communication data buffers, SRAM, local processor space, expanded registers space, special functions, or some combination thereof. The memory is generally, but not always, 16-bits wide.

The PCI-40A supports two configurations of IP memory space. The simplest configuration allocates a 2 KByte partition for each of the four IPs. This is adequate to service many IPs that use the memory space as an alternate or expanded register space. However, it is not sufficient for some IP designs that implement real memory in this space.

Interrupt Space

The PCI-40A maps all interrupt levels to the INTA# signal on the PCI back plane as required for single function devices by the PCI Spec. 2.1. Because the PCI interrupts are shared, an interrupt can be from any slot on the back plane or from the motherboard itself. The interrupt service routine (ISR) must first check that the interrupt came from the PCI-40A by reading the CNTL2 register on the PCI-40A. If an IP is requesting the interrupt, the CNTL1 register can be read to determine which one. Each of the eight IndustryPack interrupt lines (two per IP) has a bit in this register. An interrupt will be generated whenever one of these bits is set and interrupts are enabled. It is up to the ISR to prioritize multiple interrupts if more than one bit is set. Each bit can be cleared only by clearing the interrupt source on the IndustryPack.

The interrupt space of each IP slot is directly accessible at any time. Typically, the ISR will access the INT space to determine the local cause of the interrupt. A read to the INT space will generate an IP Interrupt Acknowledge Cycle. During this cycle, the IP places its interrupt vector on the data lines. Some IPs may require this access to clear the interrupt. Check the IP's User Manual for specific details on clearing interrupts.

Please refer to the Control and Status register bit map section for more information.

IP Bus Time-Out

The PCI-40A has a programmable IP bus error timer. When enabled, the PCI-40A will time out if the IP being accessed does not respond. This allows the IP slots to be interrogated during start up to determine which IPs are installed in which slots. Without this feature, accessing an IP slot that does not respond will usually put the PCI bus in an infinite retry loop, essentially locking up the host processor.

When the Bus Error feature is enabled, the hardware will create a “bus reply” for an IP that does not respond within 3.2 µs. The hardware can also generate an interrupt to the host when the reply is from the timer instead of the IP. Interrupts may also be disabled and the bus error timer status may be polled. Three bits are used to control the way the bus error timer works. The AUTO_ACK bit in CNTL0 enables the bus error timer. When set to “1”, the bus error timer will generate an Ack* whenever an IP is accessed but does not respond. A status bit in CNTL2, AUTO_INT_SET, will be set if the CLR_AUTO bit in CNTL0 is set to “1”. Once set, the AUTO_ INT_SET bit will stay set until the CLR_AUTO bit is cleared to “0”. The AUTO_ INT_SET bit will generate an interrupt if the INT_EN bit in CNTL0 is set to “1” and the Local Interrupt Enable bit in the PCI 9080 Interrupt Control/Status Register is set to “1”. With the INT_EN bit cleared to “0”, the AUTO_ INT_SET bit may be polled.

The PCI 9080 always posts to its internal write FIFO before actually performing the write to the local bus side (the IP or CNTRL register). This will lead to problems when a write causes a bus error on the local bus side and the AUTO_ACK feature is not enabled. The write appears to complete with no problems. However, the next access to the PCI-40A will put the PCI bus in an infinite retry loop as the PCI 9080 is still waiting for the previous access to complete. Eventually, this will lock-up the host computer.

Please refer to the bit map section for more information.

Status and Control Register Bit Maps

Three registers reside within the PCI-40A Local Control space as shown in Figures 2 and 3. The relative offsets and bit map definitions follow.

CNTL0: BAR2 offset 0x00000500 = Control Register 0 [CNTL0]

D7	D6	D5	D4	D3	D2	D1	D0
INTSET	INTEN	AUTO_ACK	CLR_AUTO	CLKD	CLKC	CLKB	CLKA

Bit	Definition
CLKA	0 = 8 MHz, 1 = 32 MHz for IP slot A
CLKB	0 = 8 MHz, 1 = 32 MHz for IP slot B
CLKC	0 = 8 MHz, 1 = 32 MHz for IP slot C
CLKD	0 = 8 MHz, 1 = 32 MHz for IP slot D
CLR_AUTO	0 = clear, 1 = enable AUTO_INT_SET bit in CNTL2
AUTO_ACK	0 = disable, 1 = enable bus error timer
INTEN	0 = disable interrupts, 1 = enable interrupts
INTSET	0 = turn off, 1 = force local interrupt [INTEN = 1]

Default value = 0x00. Word access and read-writeable.

CLK[A..D]
The CLK[x] bits control the clock rate for each IP. The clock to the slot is always at the frequency selected. The State Machine clock is altered to match the slot clock rate for each access automatically. A PLL is used to allow clean switching between frequencies without “glitching”.

CLR_AUTO
The CLR_AUTO control bit is used to enable and clear the AUTO_INT_SET bit in CNTL2. The AUTO_INT_SET bit is held clear when this bit is “0”. Setting this bit to a “1” removes the clear from the AUTO_INT_SET bit, allowing it to be set when the bus error timer expires and an Ack* is generated for an IP. Once the AUTO_INT_SET bit is set, a "0" must be written to the CLR_AUTO bit to clear the AUTO_INT_SET bit. The CLR_AUTO bit must be set back to a "1" to re-enable the AUTO_INT_SET bit. The CLR_AUTO bit defaults to a “0” on power up or after a reset.

AUTO_ACK
The AUTO_ACK bit enables the auto acknowledge feature when set to a “1”. When enabled, the PCI-40A will create a response to the PCI bus if an IP does not respond within 3.2 usec, or is not present. A response will be generated only for valid IP addresses. Clearing this bit to a “0” will disable this function. If the CLR_AUTO, AUTO_ACK, and INTEN are all set to “1”, an interrupt will be generated if the software accesses a location that does not respond. The software must read CNTL2 and, if necessary, CNTL1 to determine the source of the interrupt. AUTO_ACK can be used with INTEN disabled and CLR_AUTO enabled by polling the status after each access. The power up and reset default is “0”.

INTEN
The INTEN enables interrupts from the PCI-40A onto the PCI bus when set to “1”. If cleared to "0", the interrupt remains pending but blocked from the PCI-9080. The PCI-9080 will cause INTA# of the PCI bus to be asserted if INTEN is enabled and an interrupt source is active. The PCI-9080 must also be set up to pass interrupts by having its Local Interrupt Enable bit and the PCI Interrupt Enable bit in the Interrupt Control/Status Register set to “1”s. Only the PCI Interrupt Enable bit defaults to “1” as set by the EEPROM. The power up and reset default is “0”.

INTSET
The INTSET bit is used with INTEN to create an interrupt. The interrupt source is within the Altera control PLD. With INTEN enabled, setting INTSET to a "1" will generate an interrupt input to the PCI-9080. If interrupts from the local bus are enabled, the PCI bus INTA# will be activated. This is a useful feature for debugging.

CNTL1: BAR2 offset 0x00000600 = control register 1 [CNTL1]

Write

D7	D6	D5	D4	D3	D2	D1	D0
Unused	Unused	Unused	Unused	Unused	Unused	Unused	Reserved

Do not write to this register.

Read

D7	D6	D5	D4	D3	D2	D1	D0
IRQD1	IRQD0	IRQC1	IRQC0	IRQB1	IRQB0	IRQA1	IRQA0

Bit	Definition [read only]
IRQA0	0 = no interrupt, 1 = interrupt pending
IRQA1	0 = no interrupt, 1 = interrupt pending
IRQB0	0 = no interrupt, 1 = interrupt pending
IRQB1	0 = no interrupt, 1 = interrupt pending
IRQC0	0 = no interrupt, 1 = interrupt pending
IRQC1	0 = no interrupt, 1 = interrupt pending
IRQD0	0 = no interrupt, 1 = interrupt pending
IRQD1	0 = no interrupt, 1 = interrupt pending

CNTL1 is read to determine the source of an interrupt request that originates from the IP Slots. If an interrupt request is processed by the host CPU originating from the PCI-40A, then the CPU should read it and CNTL2 to determine which interrupts are pending. If the IP requires access in the interrupt space then a read/write operation can be performed via the Interrupt space (see memory map) to create an INT space access to the IP slot in question. A1 is set by the address within the space. Access an even word [a1 =0] for INT0 and an odd word for INT1.

CNTL2: BAR2 [read only] offset 0x00000700 = control register 2 [CNTL2]

D7	D6	D5	D4	D3	D2	D1	D0
LINT	Auto_Int_Set	unused	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Definition [read only]
Auto_Int_Set	0 = no bus error time out, 1 = bus error interrupt pending
LINT	0 = no interrupt, 1 = interrupt pending to PLX

Auto_Int_Set
Auto_Int_Set indicates that a bus error has occurred and that Readyi# was asserted to prevent the system from hanging up. Please refer to CNTL0 for the control bits for Auto_Int_Set.

LINT
LINT is an active high version of LINT# input to the PCI 9080 and indicates that PCI-40A is requesting an interrupt when read as a "1".

I/O Connections

The four IP positions are referred to as slots and identified by the letters A, B, C, and D. Each slot's I/O connections are routed to a separate 50-pin IDC connector that allows the separate ribbon cables to be brought out through the front panel. Refer to the *I/O Wiring* section for more information.

Power

The PCI-40A provides protected, filtered +5V, +12V, and -12V supplies to each IP by means of passive "T" filters, capacitors, and fuses. The three terminal filters provide excellent RF rejection of power supply conducted noise. This permits use of precision analog IndustryPacks together with high-speed digital IndustryPacks in the same PCI-40A. The IP slots feature other power handling features such as separated ground planes to reduce conducted noise. For more information, see the Fuse Chart in Figure 6 in the *Other Features* section.

Programming

This section outlines key aspects in programming IPs installed on the PCI-40A.

The PCI-40A is normally programmed to occupy space above one megabyte. DOS, including Microsoft's MS-DOS and IBM's PC-DOS cannot access space above one megabyte. "32-bit" operating systems, such as Windows NT, OS-9000, and SCO Unix, can generally access space above 1 MByte. Some operating systems may require an intermediate piece of software to gain access to the hardware.

The PCI 9080 on the PCI-40A can be programmed to allocate space from the memory space below 1 MByte. SBS Technologies has not tested this configuration and does not recommend it.

Before use, the PCI-40A must have its Base Address set by the system. This is done via the PCI configuration registers. All accesses to the IndustryPacks on the PCI-40A are then relative to the Base Address. In general, computing an exact address of a register within an IP requires the addition of three numbers: the PCI-40A Base Address, the Offset of the IndustryPack's appropriate I/O space, and the Register Offset within the IP. Generally, C structures and C header files are used to perform these additions implicitly. The Offset of the IP's I/O space is shown in Figure 2 in the Addressing section. The Register Offset is specific to each IP, and is given in the User Manual for that IndustryPack.

The base address is determined during start-up by the PCI BIOS. Each device on the PCI bus is interrogated during start-up. The BIOS writes out all ones to the BAR, then reads it back. The card responds with zeroes in all the address bits it uses. From this, the BIOS determines how much space the device is requesting and assigns it a base address. It then writes this address back to the BAR.

The PCI 9080 used on the PCI-40A for a PCI interface has registers that are tested by the PCI BIOS during initialization. Based upon the results, two memory spaces and one I/O space are allocated to the PCI-40A. The first memory space is contained in BAR0 and is the address of the PCI-9080 PCI accessible registers referred to as the Local Configuration Registers, Runtime Registers, and Messaging Queue Registers in the PCI 9080 Datasheet. The second memory space is contained in BAR2 and is the address to use for accessing the IPs and PCI-40As Local Control registers. This is referred to as the Local Address Space 0 in the PCI-9080 Datasheet. The I/O space for the PCI 9080 accessible registers is contained in BAR1. Programming of the PCI 9080 registers from the I/O space is not recommended. The PCI-40A does not use the PCI-9080 BAR3 for Local Address Space 0. Figure 5 below shows a map of the PCI Configuration Registers. Refer to the PCI 2.1 Specification and the PLX PCI 9080 Data Sheet for definitions of these registers.

The PCI40A is identified by a Vendor and Subsystem Vendor ID of 0x124b, a Device ID of 0x0040 and a Subsystem ID of 0x9080.

PCI CFG Register Address	To ensure software compatibility with other versions of PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.				PCI Writable	Written by Serial EEPROM
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	Y
0x04	Status			Command	Y	N
0x 08	Class Code	Revision ID	Local	Y	Y[15:0]	N
0x 0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y	N
0x 10	PCI Base Address 0 for Memory Mapped Configuration Registers (BAR0)				Y	N
0x 14	PCI Base Address 1 for I/O Mapped Configuration Registers (BAR1)				Y	N
0x 18	PCI Base Address 2 for Local Address Space 0 (BAR2)				Y	N
0x 1C	PCI Base Address 3 for Local Address Space 1 (BAR3)				Y	N
0x 20	Unused Base Address (BAR4)				N	N
0x 24	Unused Base Address (BAR5)				N	N
0x 28	Cardbus CIS Pointer (Not Supported)				N	N
0x 2C	Subsystem ID Subsystem Vendor ID				N	Y
0x 30	PCI Base Address for Local Expansion ROM				Y	N
0x 34	Reserved				N	N
0x 38	Reserved				N	N
0x 3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y [7:0]	Y

Figure 5. PCI Configuration Registers

Programming the PCI 9080 Registers

At power on, or after a PCI bus reset, the PCI 9080 reads its configuration from a serial EEPROM to determine what responses to give to the BIOS. The following sections describe some of the modes that may be applicable to IndustryPacks. Please refer to the PCI 9080 Data Sheet for a complete description of the registers.

PCI 2.1 Mode

The PCI-9080 chip has two modes of operation - one in which it will hold on to the PCI bus during the entire IP read access and one in which it will issue an immediate retry on the PCI bus and continue issuing retries until the IP has responded. This second mode is the factory default and is compliant with the PCI 2.1 Specification that requires all targets to respond within 16 PCI clock cycles. For a 33 MHz PCI bus, this is equivalent to 485 ns. It is not possible for the PCI-40A to respond within this time period, even with a zero wait state 32 MHz IP. This mode may slow down the overall access to the IP as the master gives up ownership of the bus when it receives the retry and must arbitrate to get it back. In lightly loaded systems, or systems where the host is the only bus master, performance should not be affected. The 2.1 compliant mode only affects read cycles, as writes are always posted to the PCI-9080's internal write FIFO. The PCI-9080 terminates the PCI bus write cycle, then writes the data out to the local bus.

When not in the 2.1 compliant mode, the PCI-9080 uses a retry delay timer that will issue a retry when the timer expires. The factory default setting for the timer is the maximum allowed 128 PCI clock cycles, which is 3.8 usec for a 33 MHz PCI bus. This means that an IP must respond within 3.5 usecs to keep the timer from expiring, taking into account the overhead to translate the access to the IP bus. Some IPs may not be able to meet this requirement, particularly those IPs that read serial EEPROMs. Those IPs with processors with which the IP control hardware must arbitrate to gain access to the local bus may also have problems meeting this response time. This should not be a problem if it happens infrequently, though other cards on the PCI bus may suffer due to the loss of PCI bandwidth while the PCI-40A holds onto the bus.

The PCI 2.1 compliant mode is set with bits 24 and 26 in the Mode/Arbitration Register of the PCI 9080 chip. It gets loaded from the configuration EEPROM, but may be changed at run time. See the PLX PCI-9080 data sheet and the EEPROM Programming section for more information.

The PCI 9080 does not suffer from the bug in the PCI 9060 chip which caused it to read two words on a long word boundary on every read access to the local (IP) bus.

Read Ahead Mode

The PCI 9080 can operate in a read ahead mode, where it will prefetch the data from the next address on the IP. On subsequent reads, the data will be read from the PCI 9080's internal FIFO rather than from the IP. This is incompatible with most IPs. The default setting is to leave this mode disabled. The bit controlling this feature is the Memory Space 0 Prefetch Disable bit [8] in the Local Address Space 0/Expansion ROM Bus Region Descriptor Register. The Read Prefetch Count Enable bit [10] in the same register must be set to a "1" to disable the prefetch mode. See the PCI 9080 Data Sheet for more information.

Big/Little Endian Mode

The PCI bus is always little endian. The PCI 9080 can be set to convert to big endian data ordering on the local bus. This may be useful when using an IP with a Motorola style processor on it. The default is to leave the local bus side in little endian mode and pass data directly through to the IPs. To change to big endian mode, the Direct Slave Address Space 0 Big Endian Mode bit [2] in the Big/Little Endian Descriptor Register must be set to "1". Bit 4, the Big Endian Byte Lane Mode bit, must be set to "0" to maintain compatibility with the hardware. See the PCI 9080 Data Sheet for more information.

Interrupts

The PCI-40A maps all eight of the IP interrupts as well as its internal interrupts into the Local Interrupt In pin on the PCI 9080. These are routed in the PCI 9080 to the PCI bus INTA line. This is per the PCI 2.1 specification for single function devices. To enable interrupts, the INTEN bit, CNTL0 Bit[6], as well as both the PCI Interrupt Enable Bit[8] and the PCI Local Interrupt Enable Bit[11] in the PCI 9080 Interrupt Control/Status must be set to one. The PLX Interrupt Control/Status register is located at an offset of 0x68 from the address held in the BAR0. The following is an example of the steps and values to enable the IndustryPacks to interrupt the host CPU:

- Set CNTL0 to 0x007X. This value enables interrupts from the IndustryPacks to reach the PCI 9080, enables bus timeout on an access to an empty IndustryPack slot, and enables the bus timeout interrupt to reach the PCI 9080. The X value should be set to the proper clock speed bits for each IndustryPack slot. CNTL0 is relative to BAR2.
- Set PCI 9080 Interrupt Control/Status Register (INTCSR) to 0x000D0900. This value enables interrupts from the IndustryPacks or the bus timeout to reach the host CPU. INTCSR is relative to BAR0.

All IPs capable of generating interrupts must also supply an Interrupt Vector during an interrupt acknowledge (IACK) cycle. Since the PCI bus does not have an inherent IACK cycle, the PCI-40A has a separate address space for each IP which, when read, will create an IACK cycle. Reading from offset address 0x0 in the Interrupt Space will read the IntReq0* Interrupt Vector and address 0x2 will read the IntReq1* Interrupt Vector. The vector will normally be read inside the Interrupt Service Routine. The vector does not have to be read if the IP does nothing more with an IACK cycle than output the vector. Although this is the case with most IPs, review each IP's documentation. Some IPs require that the vector to be read to clear the interrupt.

Write Posting

The PLX PCI 9080 chip always posts writes to its internal write FIFO regardless of how the PCI 2.1 compliant bit in the Mode/Arbitration Register is set. This keeps the PCI bus access at a minimum, usually taking five PCI clocks, but can cause problems on the PCI-40A if the software is not aware of this feature. A problem can occur when a write is made to an IP that does not respond or is not present. The PCI bus transaction will complete normally. However, the local bus side of the PCI 9080 will hang, waiting for the IP to respond. The next access to the PCI-40A will then put the PCI bus in an infinite retry loop when the PCI 9080 issues a retry for the new access while waiting for the previous access to complete. The easiest way around this problem is to use the Auto Acknowledge feature, which automatically completes the local bus cycle if the IP does not respond within 3.2 usecs. See the IP Bus Time-Out and the Status and Control Register Bit Map sections in the *Hardware Overview* section of this manual.

SDpacK SDK for Windows NT

SDpacK SDK for Windows NT is available from SBS Technologies. This software development kit is designed for use with IndustryPacks in industrial data acquisition and control applications. Refer to the SDpacK SDK User Manual for more information. An electronic copy of the user manual is included in the SDpacK SDK diskette. The user manual is installed when the diskette is installed. You may view the user manual with Adobe Acrobat Reader.

SDpacK SDK includes support for the PCI-40A. However, a separate SDpacK Driver is required to access an IndustryPack. Check with your sales representative to see if an SDpacK Driver is available for the IndustryPack you desire.

Other Features

LED Indicators

There are four green LED indicators on the top long edge of the PCI-40A. These are labeled LED A, LED B, LED C, and LED D. Each time IP A is successfully accessed, the LED A indicator will turn on for one third of a second. A similar action occurs for the B, C, and D indicators. Accesses more frequent than three times a second will appear as a continuously illuminated indicator.

The LEDs respond to I/O, ID, memory, and interrupt vector ID accesses. Figure 6 shows the LED chart.

LED	Color	Function
LED A	green	IP A accessed
LED B	green	IP B accessed
LED C	green	IP C accessed
LED D	green	IP D accessed
–12V	red	Slot A –12 volt supply OK
+12V	red	Slot A +12 volt supply OK
+5V	red	Slot A +5 supply OK

Figure 6. LED Chart

The LEDs are driven by the acknowledge signal from the IPs. Thus, if the host software attempts to access an IP, but selects an unused location to which the IP does not respond, or a location that is empty, the indicator LED will not flash. The indicators do not show that the PCI-40A is being selected, but rather that the associated IP has completed an access. Similarly, the indicator LEDs do not show interrupts pending, but do show interrupt vector ID read cycles.

Fuses

Caution: PCI-40A has fuses added on the power inputs to all IP positions. This is consistent with safety-related requirements of some organizations. Current limitation imposed by these fuses are shown in Figure 7 below:

Supply	Applies To	Current	Fuse[a,b,c,d]
+5V	Per IP	1.5 amps total	F10,7,4,1
+12V	Per IP	1.0 amps total	F11,8,5,2
–12V	Per IP	1.0 amps total	F12,9,6,3

Figure 7. Fuse Chart

Blown fuses for Slot A may be detected visually by three red LEDs. These LEDs are mounted on the top of the long edge with distinct labels (+12V, -12V and +5V). A blown fuse has its corresponding LED off. Figure 7 shows the fuse chart. Other slots [B,C,D] have fuses but no LEDs. The fuses may be visually inspected and are located under each IP slot near the “logic connector”.

Installation of IndustryPacks

IndustryPacks are installed on the PCI-40A carrier board by simply snapping them in. Press the IP and the carrier board together with your fingers until the two pairs of mating connectors are flush. The connectors are keyed, so the IP can only be installed correctly. Proper anti-static handling procedures should be followed.

There are four locations for IPs. These are identified as IP A, IP B, IP C, and IP D. The silk screen lettering on the PCI-40A shows the location of each.

IndustryPacks A, B, C, and D mate with straight 50-pin flat cable receptacle connectors for their I/O. Pin 1 for each connector is identified on the silkscreen. Route the cables for IPs A, B, C, and D through the rear panel.

Many connector manufacturers are able to provide suitable receptacles. The following are recommended:

Adamtech	SC-50-B-A
Robinson Nugent	IDS-C50NPK-SR-TG

The following are recommended 50-pin IP connectors:

AMP	173279-3	Plug (situated on an IP)
AMP	173280-3	header (situated on a carrier board)

Cables are available from SBS Technologies.

After an IP has been installed, four stainless steel screws may be used to secure the IP to the carrier board. This is normally necessary only in high vibration or shock environments. Insert the screw through the IP and the two connectors. Attach the nut on the solder side of the PCI-40A. Tighten using small tools, taking care not to damage either the IP or the support board. The screws used are standard (metric) M2 x 18 stainless slotted flat head. The screws and nuts are supplied with each IP.

User I/O Wiring

Each of the 50 pins on each I/O connector for the four IndustryPack slots (A, B, C and D) connects to an identically numbered pin on the four corresponding flat cable connectors on the PCI-40A. The IndustryPack® I/O connector, the PCI-40A flat cable connectors, and the wires on the ribbon cables are all numbered identically from 1 to 50. Each connector is labeled as IP A I/O, IP B I/O, IP C I/O, and IP D I/O on the silkscreen.

Pin 1 on IP and PCI-40A connectors is marked with a square pad, observable from the solder side of the respective board. Pin 1 is also shown on the silkscreen for each connector.

Caution: This pin numbering system is not maintained with many mass-terminated connectors. Each type of connector has its own intrinsic pin numbering system. Systems integrators or users making their own cables must be certain which pin corresponds to which signal.

The pin assignment of the IP I/O connector is fixed by the connector manufacturer and repeated in the IndustryPack Specification. This assignment is shown in Figure 8 below.

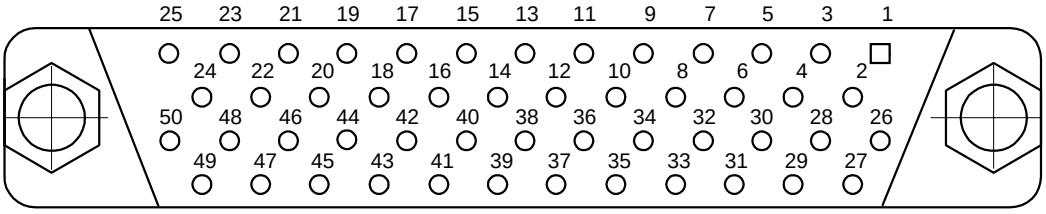

Figure 8. IndustryPack Connector Pin Numbering

Viewed from solder side of PCI-40A

The PCI-40A carrier board connects the mating I/O connector pins to a 50-pin flat cable connector. All pins from the IndustryPack go to identically numbered pins on these connectors. The pin numbering assignment of the four 50-pin front panel connectors is shown below in Figure 9. The wires in ribbon cables themselves are numbered sequentially across the flat cable starting with a red stripe on pin 1.

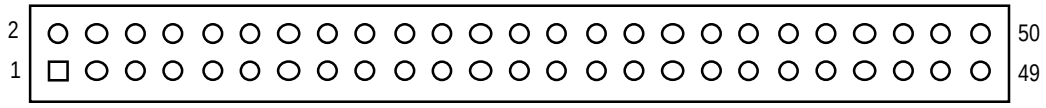

Figure 9. Flat Cable Connector Pin Numbering

Viewed from component side of PCI-40A

SBS Technologies offers cables and terminal blocks.

Interfacing to the outside world - the I/O cabling - remains the responsibility of the system integrator or end-user/engineer.

User Options

Shunts & Test Points

The PCI-40A has several shunts and test points available for configuration and debugging. The Test Points are labeled with the silk-screen. The page numbers refer to the schematic.

Shunts

J6 EEPROM PRE

The EEPROM PRE shunt and the J7 EEPROM PE shunt are used to enable programming of the EEPROM. The EEPROM PRE shunt connects the EEPROM Protect Register Enable (PRE) pin to VCC when installed. This allows programming of the EEPROM protect register. When removed, the PRE pin is pulled to GND by a 4.7KΩ resistor. This enables programming of the EEPROM data area and prevents programming of the protect register. This is the factory default.

J7 EEPROM PE

The EEPROM PE shunt and the J6 EEPROM PRE shunt are used to enable programming of the EEPROM. The EEPROM PE shunt connects the EEPROM Program Enable (PE) pin to VCC when installed. This allows programming of the EEPROM. When removed, the PE pin is pulled to GND by a 4.7KΩ resistor. This prevents any programming of the EEPROM. This is the factory default.

J8 SHORT

The SHORT shunt is used by the PCI 9080 to determine the size of the EEPROM. When removed, the PLX will only read the first five configuration registers and will not request any space for the PCI-40A IPs. When installed, all the configuration registers will be read. This is the factory default.

J11 Strobe

Each IndustryPack has one pin on the logic interface labeled "Strobe." This pin may be used for a digital strobe or clock signal related to the IPs functionality. On the PCI-40A, this pin from each of the four IP slots is connected to one of the pins on the J11 shunt. Wires may be added to connect combinations of the IP Strobe lines together. The factory default is to leave all these pins unconnected. The following table lists the connections.

Pin	IP Slot
1	Slot A
2	Slot B
3	Slot C
4	Slot D

J12 EEPROM Data Out

This shunt connects the EEPROM Data Out pin to the PLXPCI 9080 device. With it removed, the PLXPCI 9080 will power up with its factory defaults. It will not request any space for the IPs during the PCI BIOS configuration process. When inserted, the PLXPCI 9080 device will read the EEPROM after power up and use that information during the PCI BIOS configuration. This is the factory default. See schematic page 11.

DO NOT INSTALL THE FOLLOWING SHUNTS:

J3 PLL bypass – connects 8 and 32 MHz signals.
J9 Test.
J10 PLL bypass - single frequency operation

Test points are provided to aid in diagnosing and debugging IndustryPack logic interface problems. The test points labeled GNDx and TPx may be used to attach scope probes. J13 is a header style connector with standard .025”sq. posts for logic analyzer connection. This header is not factory installed. It is located under IP Slot D, and may be loaded on the back side of the board if an IP must be loaded in Slot D. SBS Technologies also has an IndustryPack extender card, IP-BusProbe, with test points on all of the signals on the logic connector. This can aid in troubleshooting problems interfacing to IPs.

Test Points

NAME	FUNCTION
GND1-3	Ground reference for test equipment
TP4	32 MHz. reference
TP5	8 MHz. reference
TP6	PLL Lock signal
J13-1	Ground reference
J13-2	clk8_32 - state machine clock reference
J13-3	ACKABCD - redefineable Altera internal test point - currently used for READYI#
J13-4	Reset Decode - signal that IP portion of State Machine is completed
J13-5	spare
J13-6	A - slot A decode active high
J13-7	INT space decode active high
J13-8	I/O space decode active high
J13-9	MEM space decode active high
J13-10	ID space decode active high

Figure 10. J13 Test Header Definition

Construction and Reliability

IndustryPacks and their carriers were conceived and engineered for rugged industrial environments. The PCI-40A is constructed out of 0.062-inch thick FR4 material. The six copper layers consist of a power plane, ground plane, and four signal planes. The power planes significantly reduce conducted and emitted RF noise. They also assist in heat dissipation. Solder mask covers exposed traces on both sides.

Components are a mix of surface-mount and through-hole. Programmable ICs are socketed in low profile gold-plated screw-machine pin sockets. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed component into the socket. The factory can build socket-free boards, as well as extended temperature range boards, on special order.

The IndustryPack connectors are keyed, shrouded and gold-plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is optionally secured to the carrier board with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications, they are not required.

IndustryPacks provide a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of standard IPs. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Most of the components on the PCI-40A are CMOS. Many IPs are also primarily CMOS. Nonetheless adequate cooling of the host system is strongly recommended.

The PCI-40A features independent three-terminal pi filters on all power lines to the IndustryPacks. This aggressive filtering of high frequency noise allows precision analog and high-speed digital IndustryPacks to be mixed in the same slot. The power line filters both block digital noise from elsewhere in the host system from entering an IP, and also block noise generated from an IP from entering the host system.

Specifications

Form Factor	PCI full-length slot
PCI	PCI Specification, Revision 2.1
PCI Controller	PLX 9080
Number of IndustryPack Slots	Four Supports up to two double-wide IndustryPacks
IndustryPack Bus Clock	Switchable 8/32 MHz per IndustryPack slot
IndustryPack Features Supported	I/O space, ID space, memory space, interrupt acknowledge cycles
IndustryPack Memory Size	8 MBytes per IndustryPack*
Carrier Board Memory Space	64 MBytes*
IndustryPack Interrupts Supported	Int0* and Int1* for each slot
PCI Bus Interrupts Generated	INTA# only
I/O Access	One 50-pin 0.1” ribbon cable header per IndustryPack slot One connector is rear-panel accessible
Indicators	One green LED per IndustryPack slot for CPU access One red LED per rail for power monitor
Fuses	1 A for 5 VDC each slot 1 A for +/-12 VDC each slot
Dimensions	4.2” x 12.2” (106.7 mm x 309.9 mm) PCI standard long card
Weight	0.21 kg (0.5 lb)
Power Requirements	+5V VDC, 250 mA typ +12 V DC, 10 mA typ –12 V DC, 10 mA typ Extra power required for IndustryPack modules
Environmental	Operating temperature: 0 to 70°C Humidity: 5 to 95% non-condensing Storage: -40 to +85°C

*A reduced memory map version of the PCI-40A is available by special order. Contact sales for more information.

References:

PCI BIOS
PCI Specification 2.1
ANSI/VITA 4-1995 IP Module Specification 1.0

PLX Technology PCI 9080 Data Sheet, Version 1.04.

Warranty and Repair

SBS Technologies, Inc. warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, SBS Technologies' sole responsibility shall be to repair or, at SBS Technologies' sole option, to replace the defective product. The product must be shipped, prepaid and insured, to SBS Technologies by the original customer. All replaced products become the sole property of SBS Technologies.

SBS Technologies' warranty of and liability for defective products is limited to that set forth herein. SBS Technologies disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchantability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

SBS Technologies' products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of SBS Technologies.

Service Policy

Before returning a product for repair, verify as soon as possible that the suspected unit is at fault; then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if it is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include the return address and telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service of SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

Out-of-Warranty Repairs

Out-of-warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is applied in addition to the minimum charge.

For service, contact:

SBS Technologies, Inc.
1284 Corporate Center Drive
St. Paul, MN 55121-1245
Tel: (651) 905-4700
FAX: (651) 905-4701
Email: support.commercial@sbs.com

Appendix A - DOS Extenders

DOS is not recommended with the PCI-40A because its native address space is limited to 1 MB. The PCI-40A can be located within this 1 MByte address space. However, this configuration has not been tested and is not recommended. The PCI-40A is normally located above the 1 MByte boundary where DOS cannot directly access. If your application requires a DOS environment then a DOS extender and a PC/AT platform with Intel 386SX/DX, 486SX/DX or higher processor are required.

A DOS Extender allows a user to access memory beyond the 1 MByte (extended memory) limit of DOS by running any application in the 16-bit protected mode of the Intel 80386, 486, or Pentium microprocessor. With a DOS Extender, an application can directly access up to 16 MBytes of memory in a PC/AT system running under DOS.

A user may access the extended memory with DOS 5.0 or 6.0 specific utility calls. Implementation of these utilities is beyond the scope of this user manual.

The user may contact the following DOS Extender vendors for any DOS Extender questions and literature:

PHAR LAP SOFTWARE, INC.
60 Aberdeen Avenue
Cambridge, MA 02138
Tel: (617) 661-1510

TENBERRY SOFTWARE, INC. (formerly RATIONAL SYSTEMS, INC.)
P.O. Box 20050
Fountain Hills, AZ 85269-0050
Tel: (480) 767-8868

ERGO COMPUTING, INC.
One Intercontinental Way
Peabody, MA 01960
Tel: (800) 633-1925