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GE
Intelligent Platforms

Hardware Reference

VMIVME-2533*

Differential Digital Output Board

Publication No: 500-002533-000 Rev. L

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Overview

Introduction

The VMIVME-2533* is a VMEbus Compatible Differential Digital Output Board with 32 differential outputs channels.

Features:

- 32 bits of differential voltage outputs
- RS485/422 compatible drivers
- 8-, 16-, or 32-bit data transfers
- Each data bit represents one discrete line pair
- Built-in-test
- Front panel with Fail LED
- Compatible with the VMIVME-9016 Intelligent I/O Controller

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Functional Description

The VMIVME-2533 transfers digital data from the VMEbus backplane to RS485/422 compatible differential output drivers. The board will support byte, word, and longword data transfers. A simplified functional block diagram of the board is illustrated in Figure 1 below.

The VMIVME-2533 is designed with extensive Built-in-Test electronics that enable the user to test most of the circuitry on the board. When the VMIVME-2533 is in test mode, data, which is written to the output registers, can be read back to verify proper operation. This can be done without driving the output cable, and without disturbing the field circuitry connected to the VMIVME-2533. Figure 2 below shows a simplified diagram of the Built-in-Test features of the VMIVME-2533.

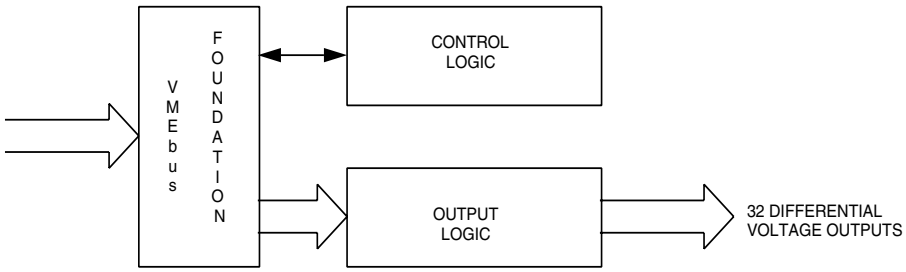


Figure 1 Basic Digital Board Functions

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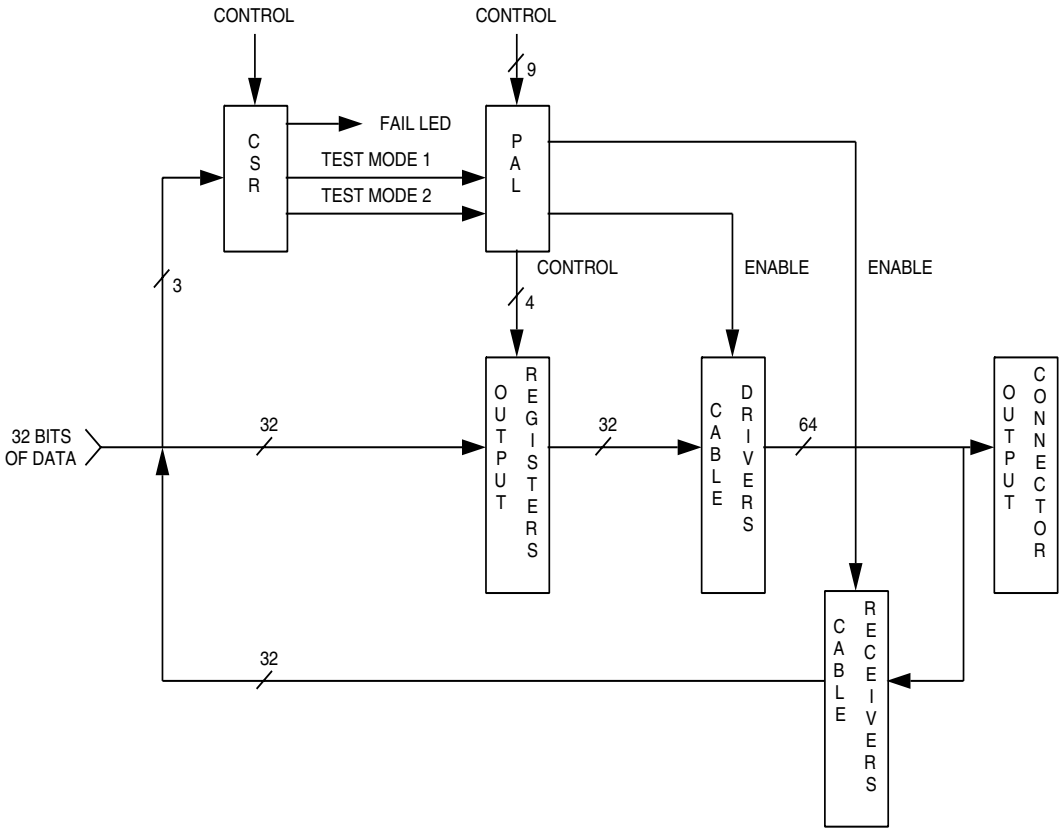


Figure 2 Simplified Built-in-Test Functional Block Diagram

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Functional Block Diagram

The VMIVME-2533 Differential Digital Output Board consists of VMEbus compatibility logic, four 8-bit output registers, eight 4-bit differential line drivers, a Control and Status Register, and eight 4-bit differential line receivers used by the Built-in-Test logic, as shown in Figure 3 below.

The VMEbus compatibility logic controls data transfer allowing 8-, 16-, or 32-bit VMEbus data transfers.

The four 8-bit output registers latch 32 bits of output data, which drives the eight RS485/422 compatible differential output voltage drivers to the field connector.

The Control and Status Register (CSR) contains three bits. One bit controls the on-board Fail LED, while the other two bits, along with some additional logic, control the test functions of the board.

Built-in-Test logic enables the output data to be read back without affecting the signals to the field. System reset puts the board into test mode for immediate loopback testing.

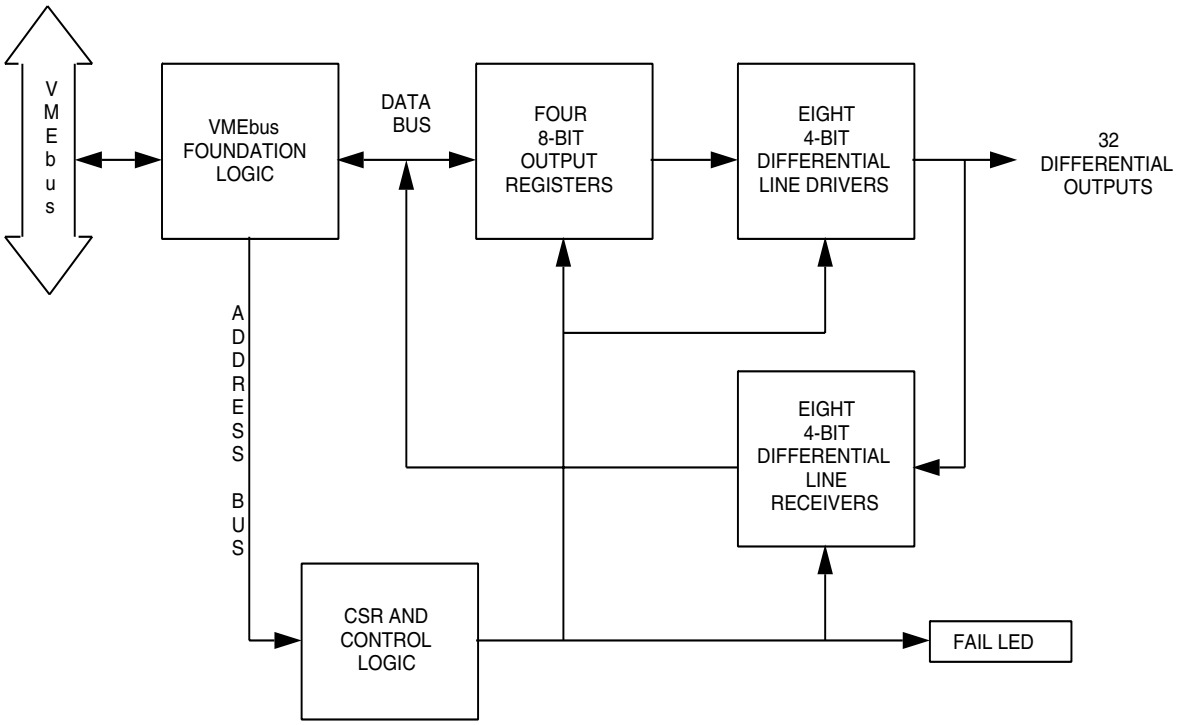


Figure 3 VMIVME-2533 Functional Block Diagram

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Reference Material List

For a detailed description of the VMEbus, refer to *The VMEbus Specification and Handbook* available from:

VMEbus International Trade Association (VITA)
7825 Gelding Dr. Suite No. 104
Scottsdale, AZ 85620-3415
(602) 951-8866
Fax: (602) 951-0720
e-mail: info@vita.com
Internet: www.vita.com

Physical Description and Specifications, refer to *Product Specification, 800-002533-000* available from:

GE
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308, USA
www.ge-ip.com

The following Application and Configuration Guides are available from GE to assist the user in the selection, specification and implementation of systems based on GE's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Low Level Analog I/O Configuration Guide	825-000000-001
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Application Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

GE assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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Safety Symbols Used in This Manual

STOP: This symbol informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: This sign denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: This sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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CHAPTER

1

Theory of Operation

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Introduction

This section of the manual presents detailed information concerning the hardware operation of the board.

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Operational Overview

The VMIVME-2533 consists of five primary sections as illustrated in Figure 1-1 below. These sections are described in more detail in the following sections.

To perform an output data transfer, data is written into Output Data Registers (ODRs) which latch the data. The latched data is used by the output driver stage of the board.

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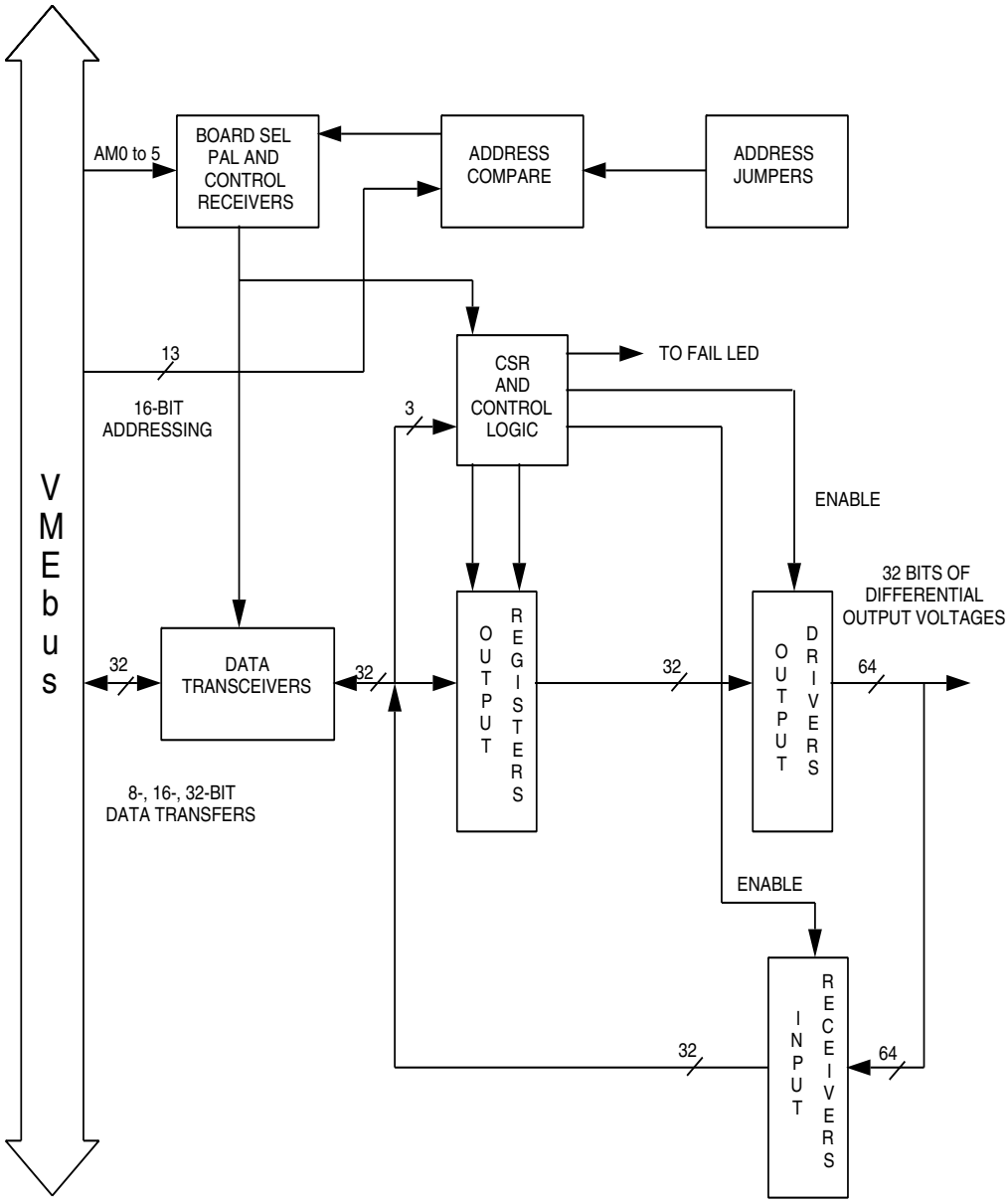


Figure 1-1 Functional Block Diagram

VMEbus Compatibility Logic

Typical VMEbus drivers, receivers, and control logic are shown in Figure 1-2 below. The DTACK generator shown in Figure 1-2 is designed to select the maximum data transfer speed.

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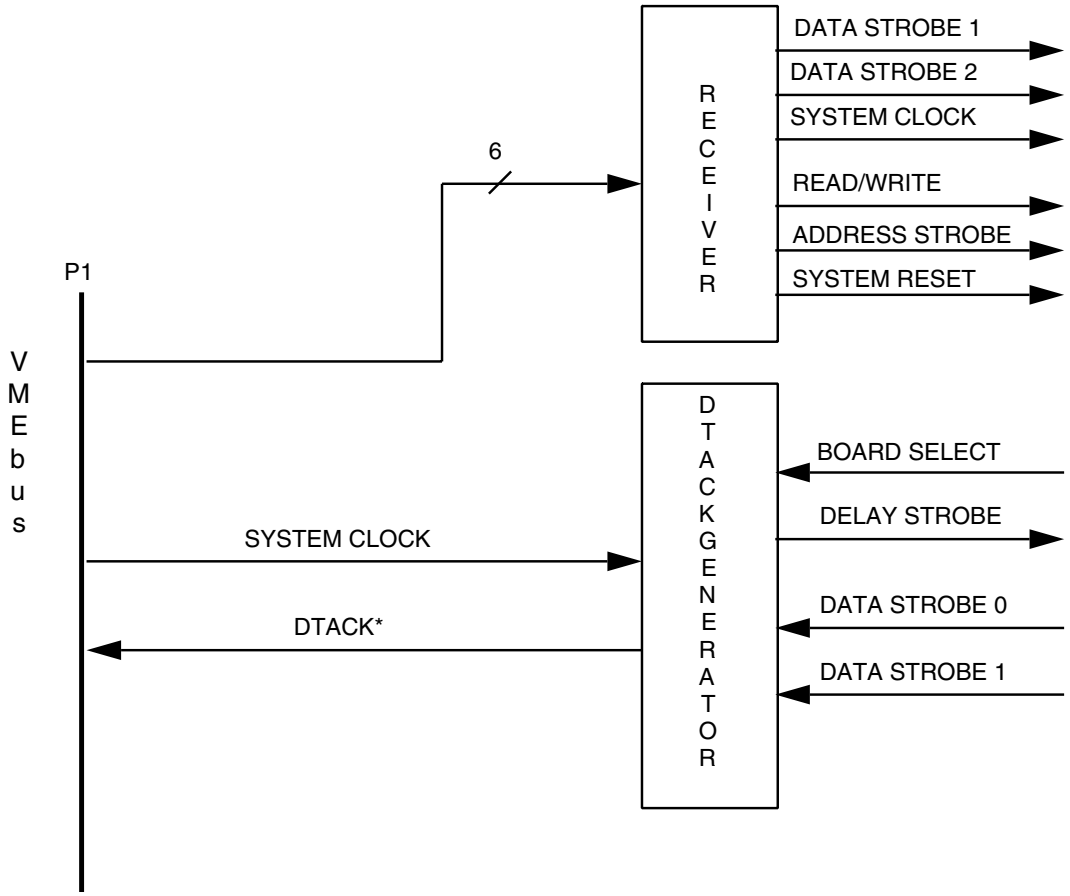


Figure 1-2 VMEbus Foundation Logic

Device Addressing

The VMIVME-2533 is designed to support data transfers in supervisory or non-privileged short I/O memory space or both. A jumper (AM02) is provided as shown in Figure 1-3 on page 18 (Address Decode Block Diagram) to allow user selection of either I/O access type or both. The jumper (AM02) is factory configured (jumper AM02 not installed) to respond to short supervisory I/O access. Refer to *Configuration and Installation* on page 22 for a detailed explanation of the address modifier jumper.

The VMIVME-2533 is designed with a set of board select jumpers and decode logic as shown in Figure 1-3 below to provide an efficient memory address map for CSR and output data addresses. The board is also designed to handle 8-, 16-, or 32-bit data transfers. Figure 1-4 on page 19 shows the block diagram of this circuitry.

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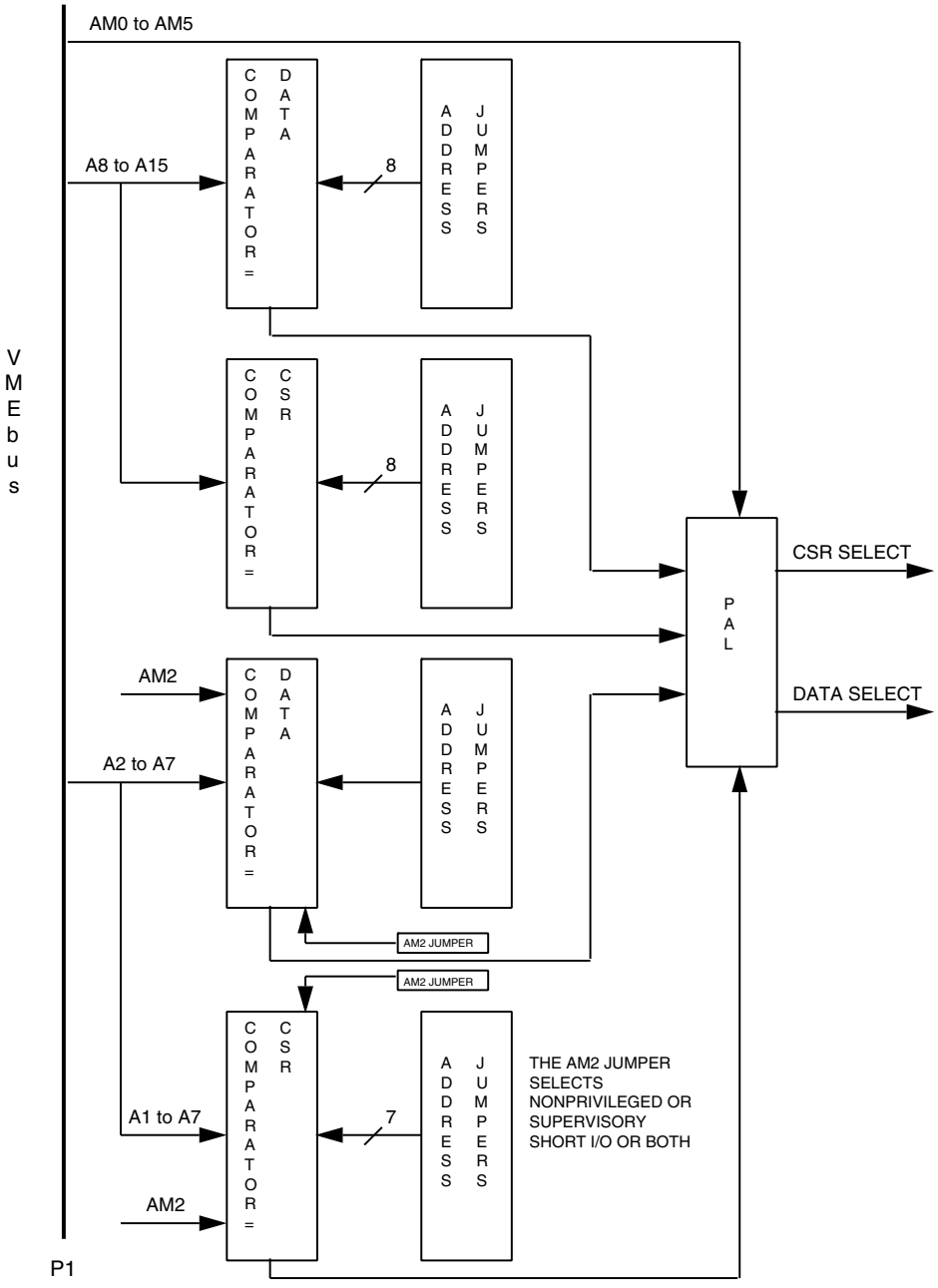


Figure 1-3 Address Decode Block Diagram

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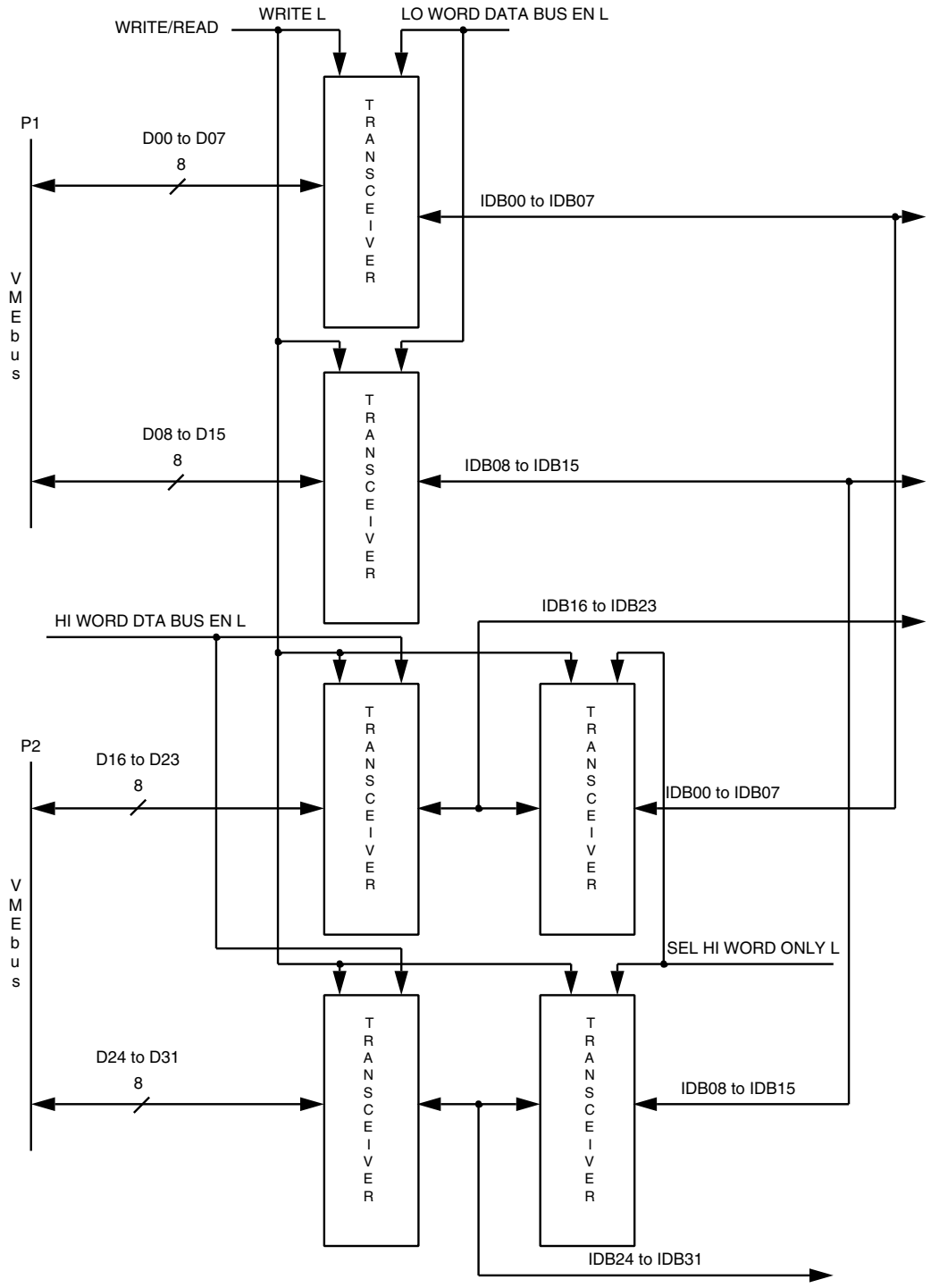


Figure 1-4 Data Transfer Block Diagram

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Control and Status Register (CSR)

The CSR controls the Test Mode (TM) Bits and the front panel Fail LED as shown in Figure 1-5 below. The TM bits enable the TRI-STATE outputs of four data latches and disables the output drivers to support Built-in-Test functions. The CSR is initialized active upon system reset such that the outputs to the cable are disabled and the front panel LED is illuminated.

The CSR uses only the upper nibble (bits 7 through 4) for controlling the test mode functions. The lower nibble (bits 3 through 0) can be setup by the user via jumper JA. These bits can define some function for the user to test in software.

The CSR also contains a board ID code register on the upper byte. Its value is 02 HEX. This register can be used by system software to do automatic system configuration.

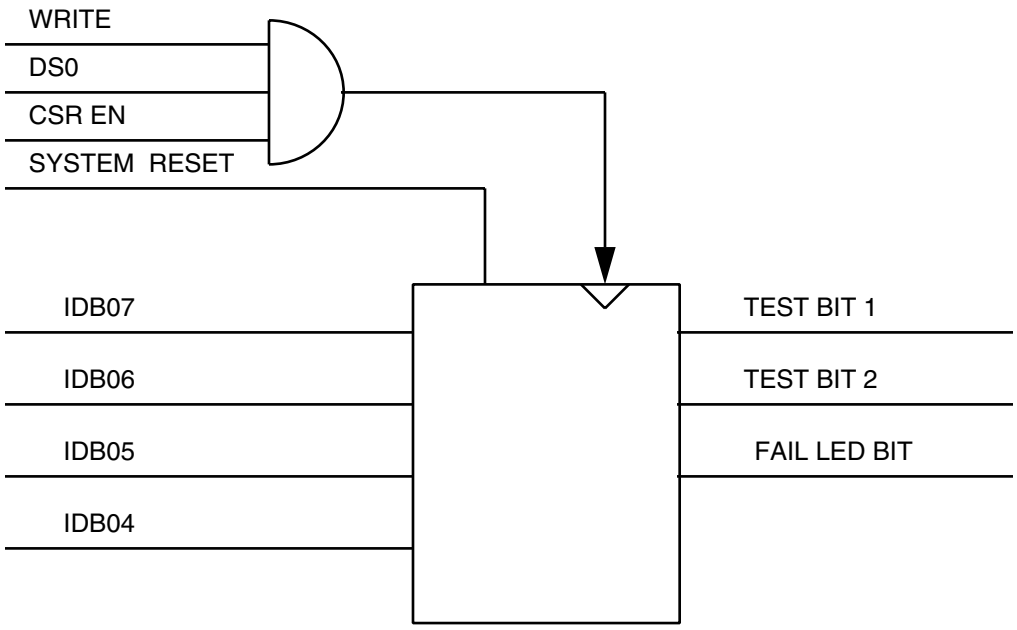


Figure 1-5 CSR Block Diagram

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Built-In-Test Description

The VMIVME-2533 test logic provides for two different modes of testing: an off-line test mode and a on-line test mode. Jumper JB can be used to disable this feature. Jumper JB is provided to accommodate future software advancements, and should not be moved from the ground position in which it was shipped.

Upon system reset, the CSR is cleared to all zeroes initializing the board in the off-line test mode. This mode of test disables all output drivers, enables the output registers and internal loopback registers to test the board circuitry without affecting off-board circuitry.

The on-line test mode is the normal mode of operation for the VMIVME-2533. In this mode the VMIVME-2533 has a differential line receiver dedicated to reading the differential outputs.

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CHAPTER 2

Configuration and Installation

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Address Modifiers 24
Data Registers Base Address 25
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Jumper Configuration

Figure 2-1 below shows the locations and factory configuration for the jumpers used on the VMIVME-2533. The following sections and figures give a detailed explanation of the use and set up of these jumpers.

Jumper A is read by the use of four bits of the CSR (Table 3-1 on page 33). Jumper JA can be used by the user for automatic software system set-up/configuration. The jumper JB is to be used for future enhancements and should not be moved from the G (ground pin) position.

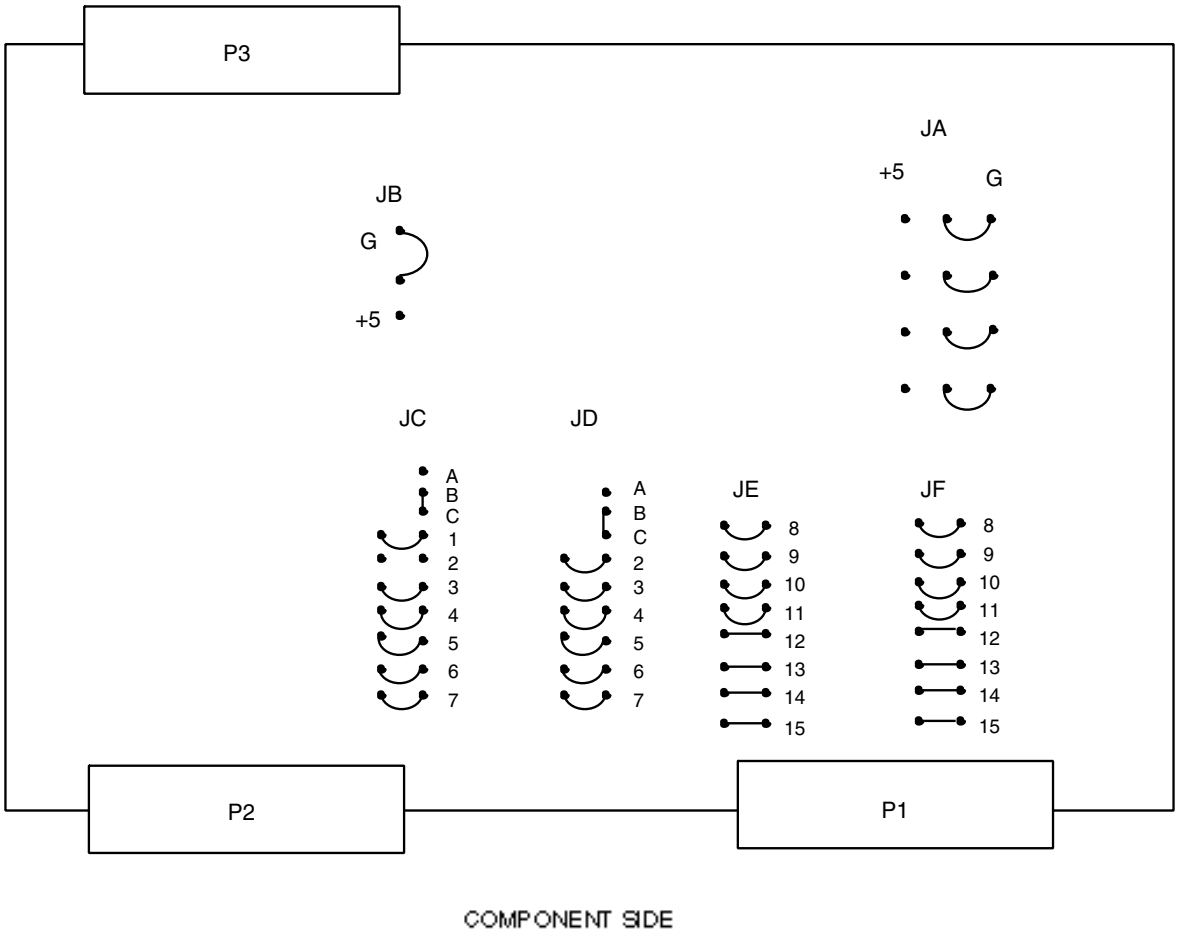
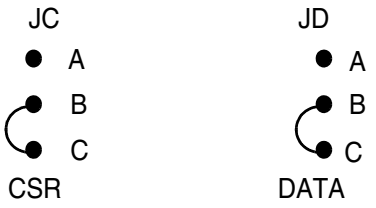


Figure 2-1 Jumper Locations

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Address Modifiers

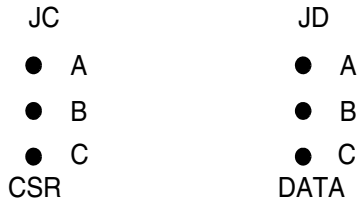
The VMIVME-2533 Board is configured at the factory to respond to short nonprivileged I/O access, (jumper AM2 installed). This can be changed by installing the AM2 jumpers to fit the need. There are two AM2 jumpers, one is for the data register's base address (jumper JD) and the other is for the CSR (jumper JC). There are also three possible selections for each of the AM2 jumpers. Figure 5.4-1 shows the three possible selections for AM2. Figure 2-2 below (a) shows the AM2 jumper for nonprivileged short I/O accesses only, while Figure 2-2 (b) shows the AM2 jumper set-up for either I/O access type. In this mode the data registers and/or the CSR will acknowledge either I/O access (short supervisory or non-privileged).



a. AM2 Jumpered for Short Nonprivileged I/O Access.



b. AM2 Jumpered for Either I/O Access.



c. AM2 Jumpered for Short Supervisory Access (no jumpers installed)

Figure 2-2 Address Modifier Positions

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Data Registers Base Address

The VMIVME-2533 Board occupies 4 bytes of the VMEbus short I/O address space. The base address of these bytes is configured by jumpers JD and JF. The factory sets up these headers to a base address of 0000 HEX, as shown in Figure 2-3 below.

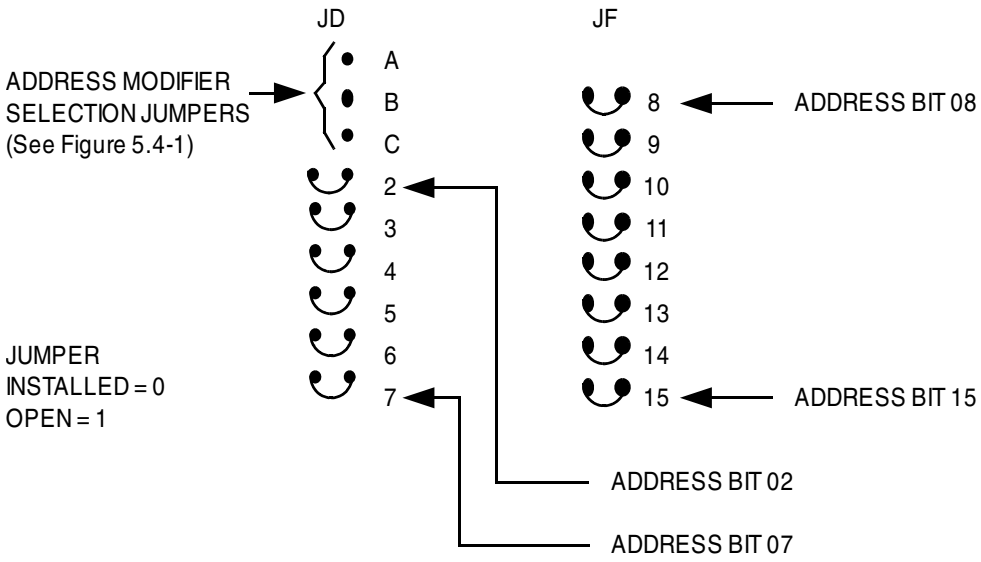


Figure 2-3 Data Registers Base Address Configuration

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CSR Base Address

The CSR of the VMIVME-2533 includes a byte for the board I.D. number. As such, the CSR occupies two bytes of the VMEbus short I/O address space. The CSR has its own set of address jumpers so the data and CSRs in a system can be stacked into separate but contiguous memory locations. The CSR jumpers JC and JE are configured at the factory to a base address of 0004 HEX, as shown in Figure 2-4 below.

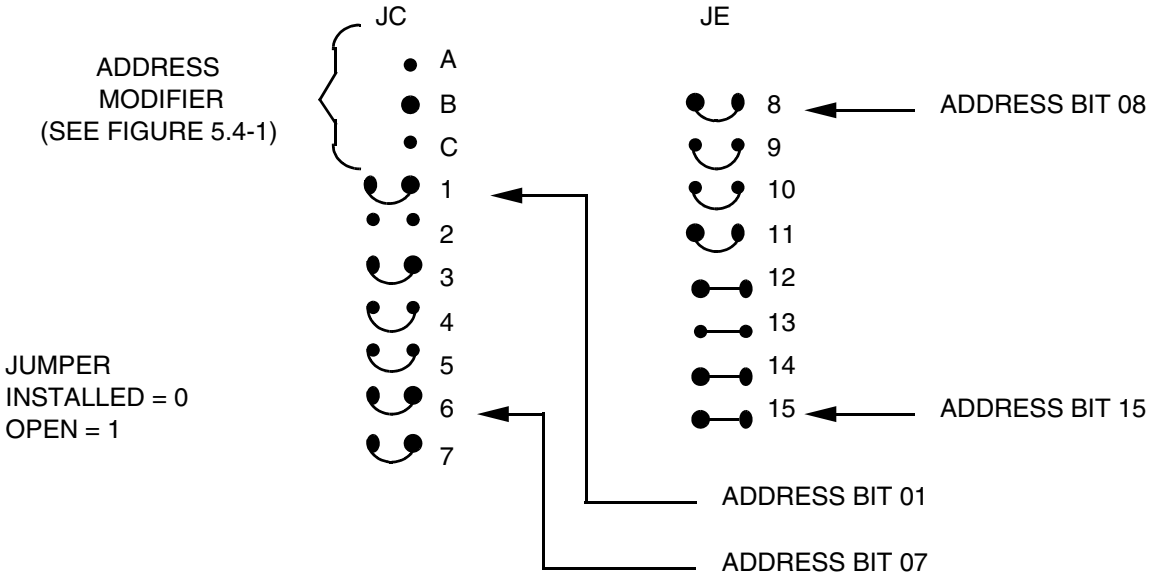


Figure 2-4 CSR Base Address Configuration

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I/O Cable and Front Panel Connector Configuration

The I/O connector (P3) is a 64-pin DIN standard and was selected because of its high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to GE's Connector and I/O Cable Application Guide (GE's Document No. 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning input connections are shown in Figure 2-5 below. Figure 2-5 has conductor number 1 shown at the bottom of the connector as it plugs into the header, due to pin number 1 of P3 being mounted as shown.

Connector pin assignments for the 32 output channels of the VMIVME-2533 are shown in Table 2-1 on page 29. The VMIVME-2533 is a differential output board, and so Pin "A" of each row is the output high side, and Pin "C" of each row is the low side of the assigned channel. The output connector pin configuration for P3 is shown in Figure 2-6 on page 28. Figure 2-7 on page 30 shows the pinout of the P1 and P2 connectors that connect the board to the VMEbus backplane.

A compatible flat-ribbon cable connector for the VMIVME-2533 is Panduit No. 120-964-435E, and the strain relief is Panduit No. 100-000-032.

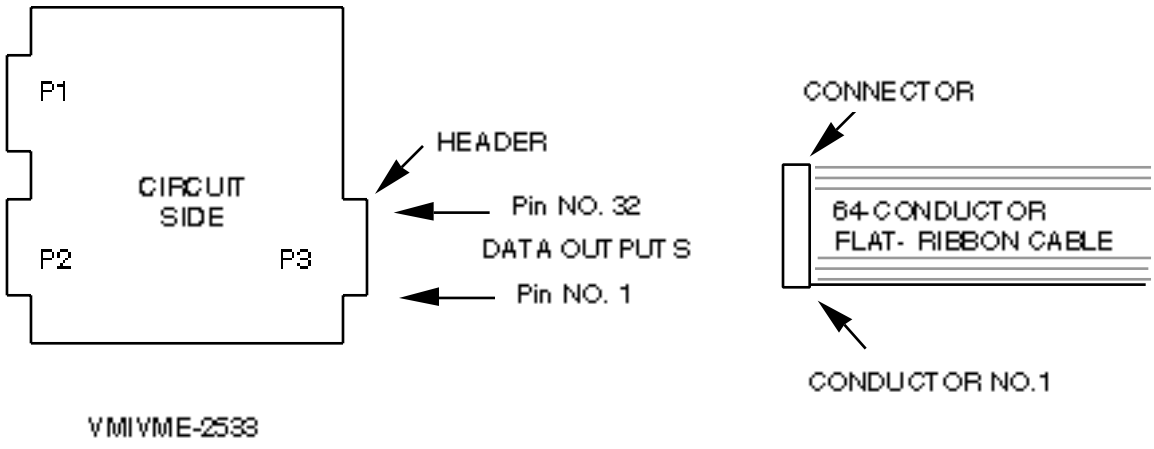


Figure 2-5 Cable Connector Configuration

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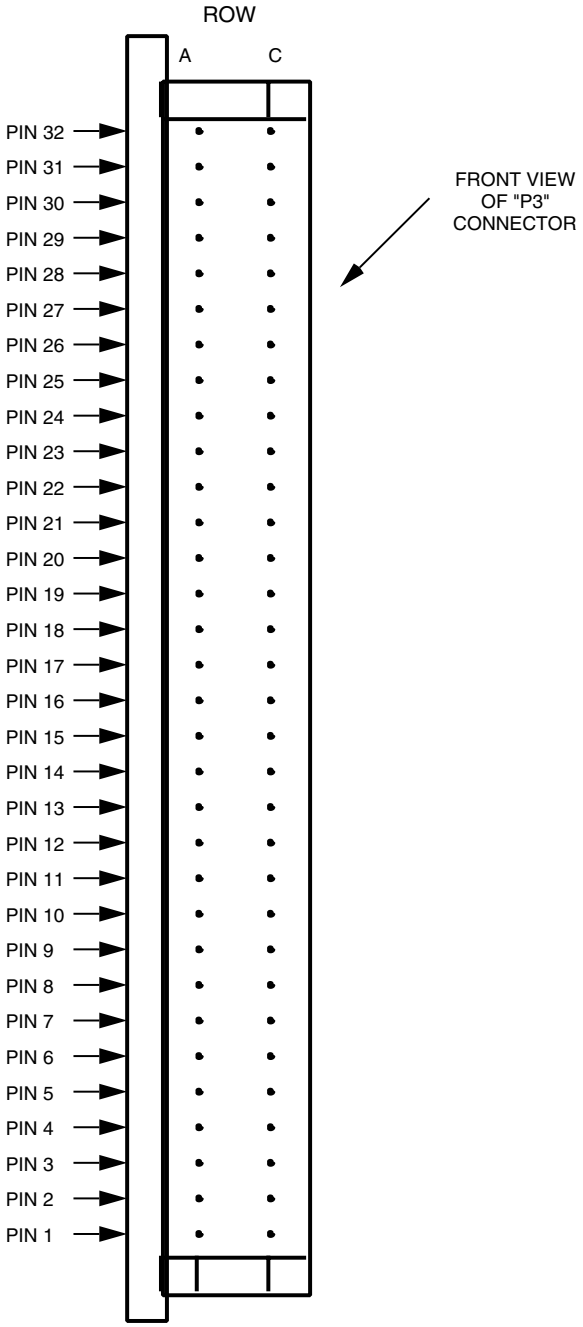


Figure 2-6 P3 Connector Pin Layout

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Table 2-1 P3 Output Connector Channel Assignments

P3		P3	
ROWS A & C PIN	CHANNEL NO.	ROWS A & C PIN	CHANNEL NO.
32	31	16	15
31	30	15	14
30	29	14	13
29	28	13	12
28	27	12	11
27	26	11	10
26	25	10	09
25	24	09	08
24	23	08	07
23	22	07	06
22	21	06	05
21	20	05	04
20	19	04	03
19	18	03	02
18	17	02	01
17	16	01	00

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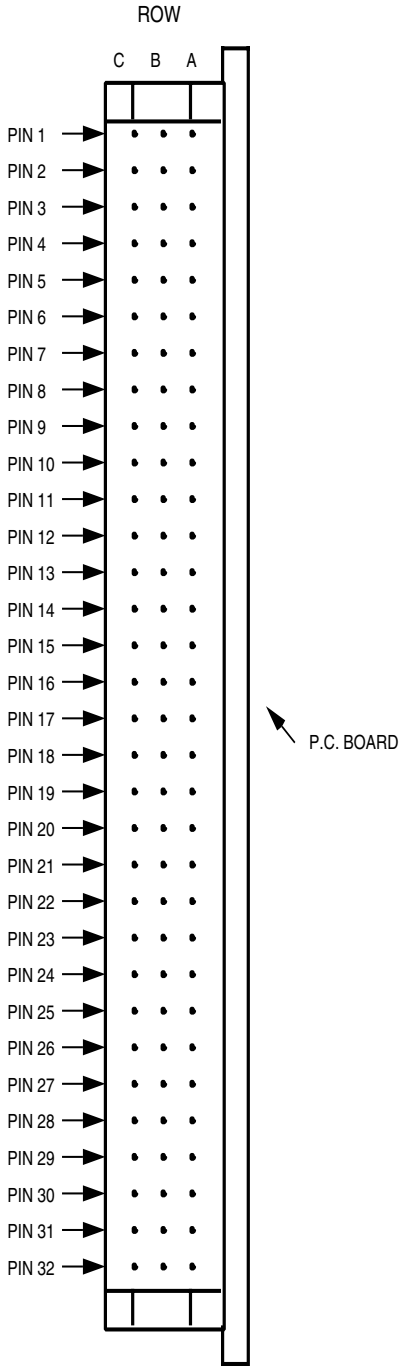


Figure 2-7 P1/P2 Connector Pin Layout

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CHAPTER
3

Programming

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Introduction

The VMIVME-2533 performs output transfers by writing data to the appropriate Output Data Registers (ODRs). The differential digital outputs are read by performing a read from differential data receivers. For programming simplicity differential receivers are mapped into the same address locations as the drivers. Therefore, the bits of each register correspond to an output channel when performing a write to that register, but the output data can be read back by performing a read cycle.

The base address required for accessing the VMIVME-2533 is selected by the address jumpers JD and JF referred to Chapter 2 *Configuration and Installation* on page 22. The on-board registers are selected by address bits A02, A01, DS1, and DS0.

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Data Output

A data output operation is initiated when the CPU executes an instruction that sends a board address that causes selection of the board. When the CPU executes an instruction to store data, VMEbus control signals cause the board to store the output data as transferred from the VMEbus. The format of the output data and the board address is shown in Table 3-1 on page 33.

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Data Loopback

A data loopback operation, used for loopback testing, is initiated when the CPU executes an instruction that sends a board address that causes the selection of the board. When the CPU executes an instruction to read data, VMEbus control signals cause the board to place a data input word on the VMEbus for transfer to the computer. The format of the input data and the board address are the same as the output data and is shown in Table 3-1 below.

Table 3-1 Address Register Bit Definitions

HEX ADDRESS	BINARY ADDRESS															
A15 to A4	A3	A2	A1	A0												
X X X	X	X	0	0	DATA PORT 0 (UPPER BYTE)											
					IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8				
					I/O 31	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	I/O 25	I/O 24				
X X X	X	X	0	1	DATA PORT 1 (MIDDLE UPPER BYTE)											
					IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0				
					I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16				
X X X	X	X	1	0	DATA PORT 2 (MIDDLE LOWER BYTE)											
					IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8				
					I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8				
X X X	X	X	1	1	DATA PORT 3 (LOWER BYTE)											
					IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0				
					I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0				
Y Y Y	Y	Y	Y	0	BD ID REGISTER											
					BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8				
					0	0	0	0	0	0	1	0				
Y Y Y	Y	Y	Y	1	CONTROL STATUS REGISTER											
					IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0				
					TM1	TM2	FAIL	NOT USED	USER-DEFINED							

CSR BIT DEFINITIONS

TM1* Set to a "zero" to disable output drivers. Set to a "one" to enable output drivers.

TM2* Set to a "zero" to enable internal registers. Set to a "one" to disable internal loopback registers.

FAIL* Fail mode LED bit. Fail LED is ON if bit is "zero", OFF if "one".

*0=Active State

X is for the DATA address select jumpers JD and JF

Y is for the CSR address select jumpers JC and JE

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Control and Status Register (CSR)

The CSR is a register that controls the Test Mode (TM) bits and the front panel Fail LED as shown in Figure 1-1 on page 16. Clearing both TM1 and TM2 disables the output differential line drivers but enables the internal data registers for off-line Built-in-Test. Setting TM1 to a logic "1", enables the output differential line drivers. These outputs can be read by differential line receivers for on-line Built-in-Test when TM1 is high.

The CSR address is selected by the address jumpers JC and JE. The format of the CSR data and address is shown in Table 3-1 on page 33. The CSR is initialized active upon system reset such that the outputs are disabled and the front panel LED is illuminated. Jumper JA can be used by the user for some automatic system set-up/configuration. This nibble is part of the CSR and is available to the user for this purpose.

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Maintenance

If a GE product malfunctions, please verify the following:

1. Software version resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return from Customer Care.**

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Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

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