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VMIVME-4105

8-CHANNEL 12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER BOARD

INSTRUCTION MANUAL

DOCUMENT NO: 500-004105-000 U

Revised July 21, 1995

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RECORD OF REVISIONS

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U	07/21/95	Cover, pages ii, vi, 4-3, 4-4, and Section 6	95-0449

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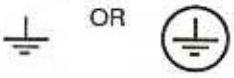
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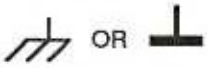
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Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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NOTE:

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VMIVME-4105
8-CHANNEL 12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER BOARD

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A Assembly Drawing, Parts List, and Schematic

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SECTION 1

VMIVME-4105 8-CHANNEL 12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER BOARD

1.1 INTRODUCTION

VMIVME-4105 8-Channel 12-Bit Multiplying Digital-to-Analog Converter (DAC) board delivers ±10 V outputs with positive true offset binary input coding and 0 to -10 V with unipolar straight binary. The DAC board features buffered data latches and buffered voltage outputs. The DAC board may be ordered with Built-in-Test hardware that can isolate the eight analog outputs from field connections during diagnostic tests. In the test mode analog outputs are multiplexed to an analog test bus on the VME P2 backplane (user I/0 pins) for analog-to-digital conversion by VMIC's VMIVME-3100 Analog-to-Digital Converter (ADC) board. A front panel Fail LED is provided for quick fault location identification. The DAC board is shown in Figure 1.1-1.

This document will primarily describe the operation of the DAC board, but some details of the VMIVME-3100 12-Bit ADC board and the VMIVME-3200 32-Channel Multiplexer board will be included for clarity. It is also intended to give the user a better understanding of the test capabilities of a data acquisition system using the DAC board in conjunction with the VMIC MUX Expander board, (VMIVME-3200) and the ADC board, (VMIVME-3100).

For a thorough understanding of the Built-in-Test and channel expansion capabilities, the reader should have access to the following documents:

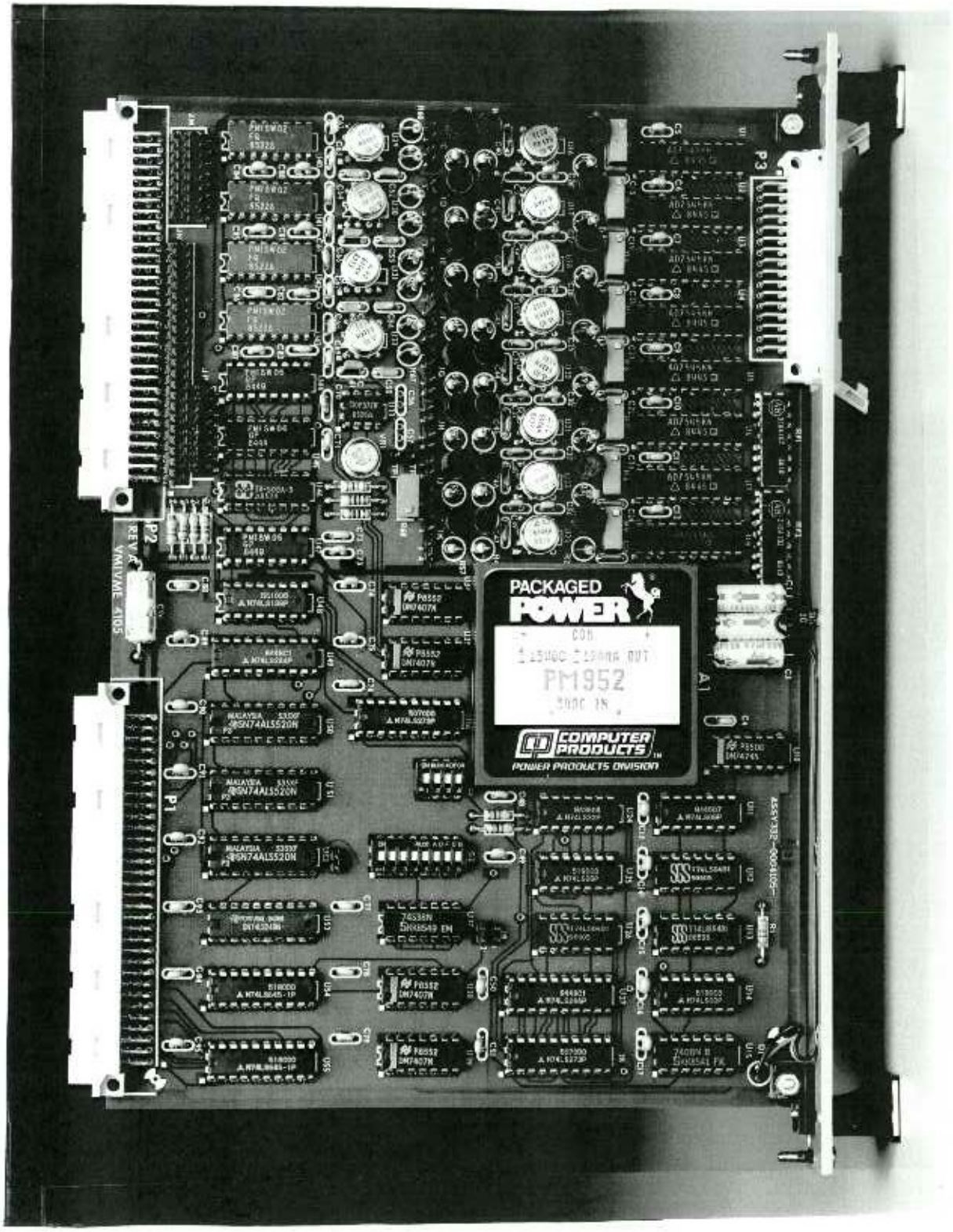
TITLE	DOCUMENT NUMBER
VMIVME-3200 32-Channel Analog Input Multiplexer Board Instruction Manual	500-003200-000
VMIVME-3100 12-Bit ADC Board Instruction Manual	500-003100-000

1.2 VMIVME-4105 OVERVIEW

The primary features of the VMIVME-4105 DAC board are as follows:

a. 8-Channel analog output
b. 12-bit resolution
c. ±10 V outputs

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M4105/F1.1-1

Figure 1.1-1. VMIVME-4105 Multiplying DAC Board

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d. 0 to -10 V option
e. Two or four quadrant multiplier option
f. Jumper option to select eight independent references from the P2 connector or one shared AC or DC voltage source reference from the P2 (VMEbus I/O) or P3 (front panel) connector
g. Software selectable internal precision +10 V reference
h. Built-in-Test hardware (requires VMIVME-3100)
i. Double Eurocard form factor
j. Front panel Fail LED
k. Outputs may be routed by jumpers to either the front panel P3 connector or the VMEbus user I/O P2 connector
l. 5 mA output drive current
m. Single +5 V supply operation

A unique feature of the VMIVME-4105 is the Built-in-Test logic that allows the testing of any one of the analog output channels through the use of an on-board multiplexer and the VMIVME-3100 ADC board. When in test mode, the field connections through connector P3 may be isolated and any of the eight channels may be routed to the 12-bit ADC board via VMIC's Analog Backplane (AMXbus™). At the A/D board under program control the analog signal may be converted to a 12-bit digital word and compared with the original 12-bit word written to the DAC board. In this manner each of the eight analog output channels may be verified without disturbing the field connected devices. The analog output channels may also be multiplexed to the Analog Test Bus simultaneously controlling the P3 connected field devices, and providing real-time fault detection of the outputs. If a board fails its self test a Fail LED on the front panel may be turned "ON" to indicate the board is in a FAILED condition. The complete operation and requirements for the self-test mode are explained in detail in this manual in Section 3, Theory of Operation, and Section 4, Programming.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Rd.
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based in VMIC's products.

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TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-00000-000
Change-of-State Application Guide	825-00000-002
Digital I/O (with Built-in-Test) Product Line Description	825-00000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-00000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-00000-005
Connector and I/O Cable Application Guide	825-00000-006

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-004105-000 DOCUMENT

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SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-4105 Digital-to-Analog Converter (DAC) board performs digital-to-analog conversion on 12-bit positive true offset binary coded words for ±10 V outputs and unipolar straight binary for 0 to -10 V outputs. Two's complement binary coding is available (jumper selectable) for ±10 V outputs.

The DAC board may use the on-board +10 V precision reference or an external AC reference may be selected under software control. When the external reference is used, the multiplying properties of the on-board DAC integrated circuits may be employed. A multiplying DAC, such as the one employed on the VMIVME-4105, is one in which the input reference voltage can be varied to produce an analog output which is the product of the input code and the input reference voltage.

Outputs are automatically updated when the DAC channel is written to, and data is latched into the corresponding DAC channel register. The DAC board allows the user to configure outputs out the P3 front panel connector or the VMEbus P2 connector. Each output has an associated GND wire output, allowing for flat twisted-pair cable connections. The DAC board block diagram is shown in Figure 3.1-1.

3.2 TEST MODE DESCRIPTION

The test mode hardware is optional (refer to Ordering Information, Section 2.3, for options) and is only needed when the VMIVME-4105 is used along with the VMIVME-3100 12-Bit Analog-to-Digital Converter (ADC) board as a minimum and possibly the VMIVME-3200 Multiplexer board. Both these boards support the Built-in-Test capabilities of the VMIVME-4105 and will be further explained here. A typical data acquisition configuration with Built-in-Test capabilities is shown in Figure 3.2-1. Up to 16 multiplexer boards or 16 DAC boards may be interconnected with one VMIVME-3100 ADC board. Thus, a single chassis system could accommodate 128 analog outputs, or up to 528 single-ended analog inputs.

If testing the accuracy of the analog output channels of the VMIVME-4105 is desired, then a VMIVME-3100 ADC board is required. These two boards must exist in the same VMIC (P2) analog backplane. VMIC has three low-noise

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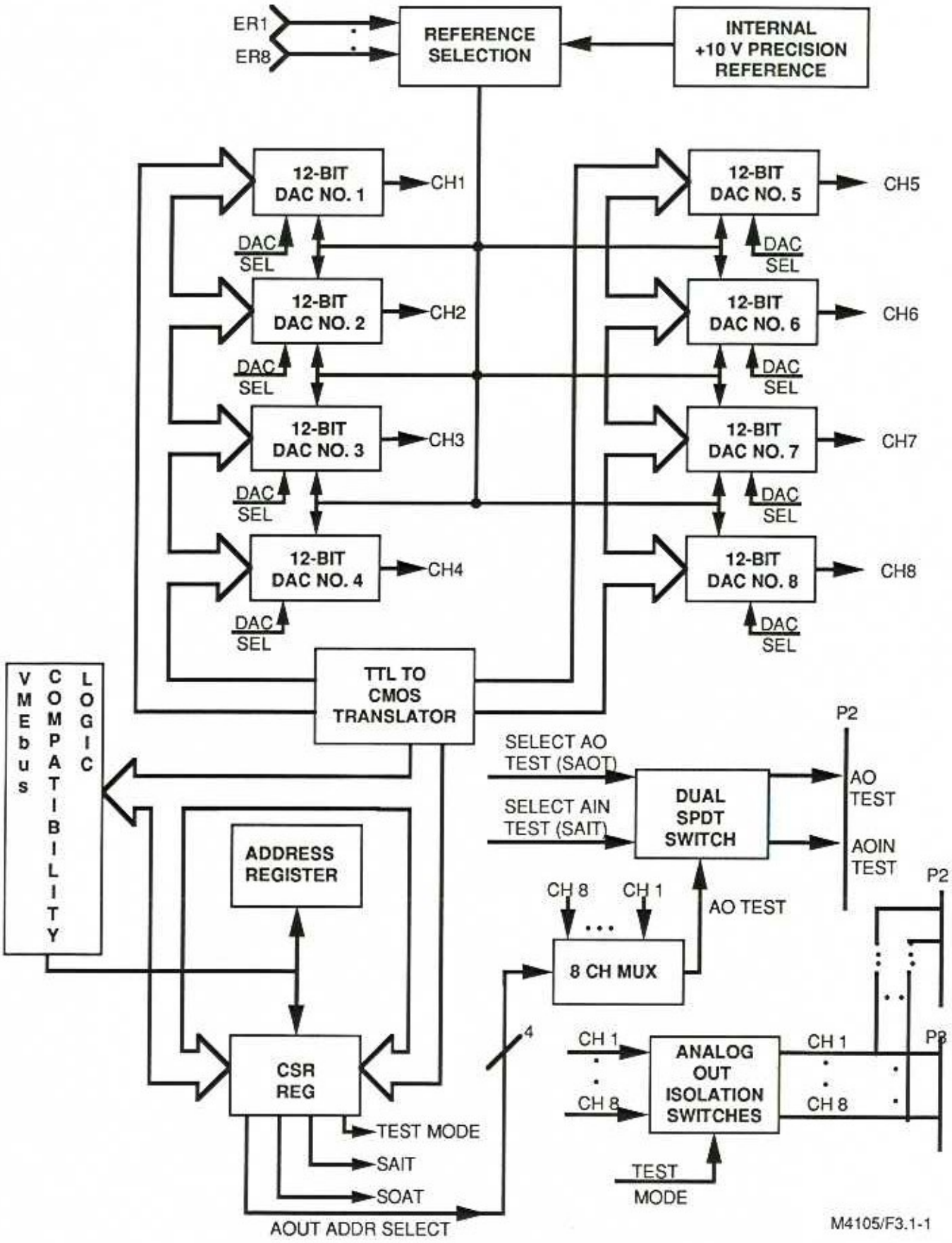


Figure 3.1-1. VMIVME-4105 Board

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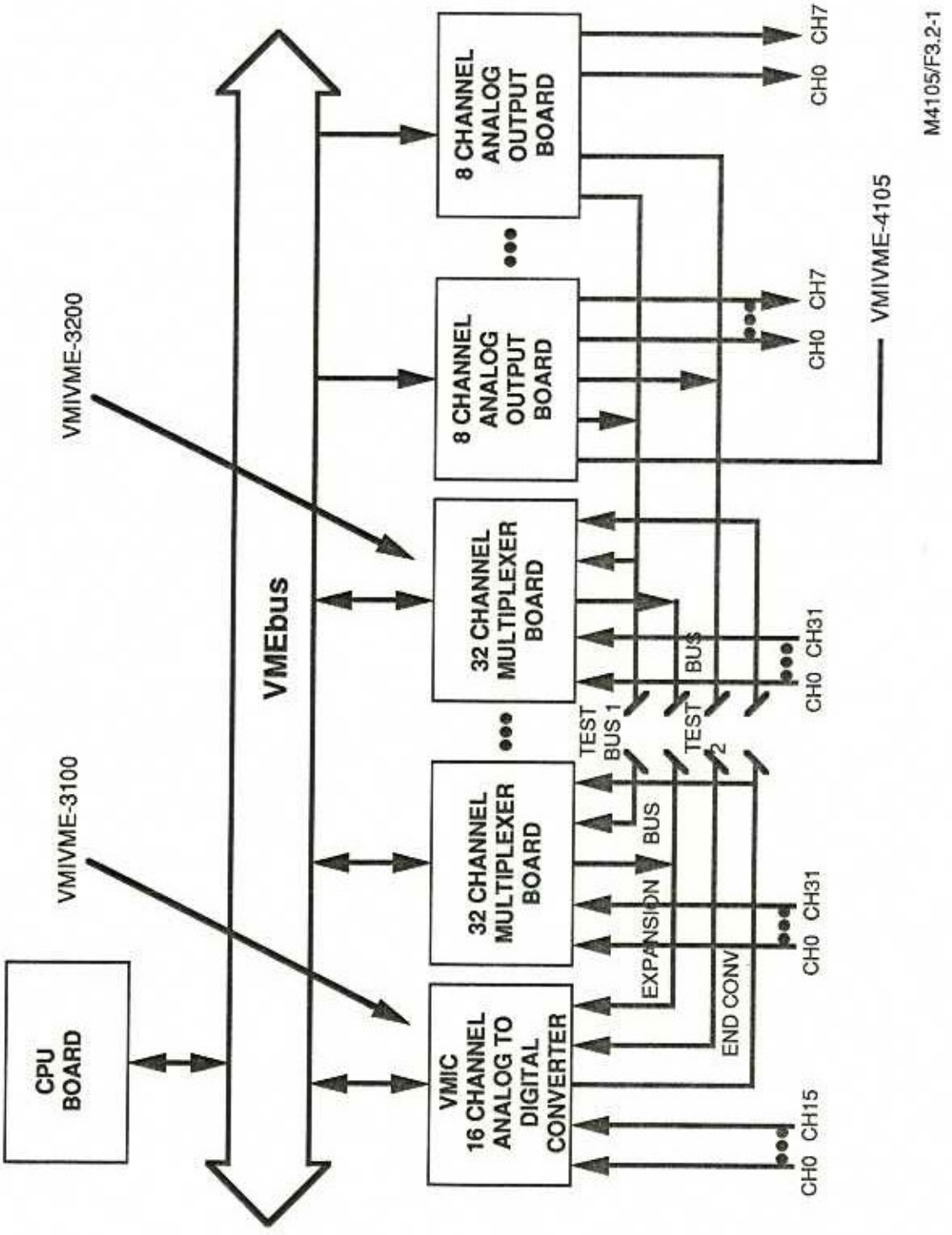


Figure 3.2-1. VMIC High Performance Analog Input/Output Configuration

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Analog Multiplexer Bus Backplanes (AMXbus™). They are available in 5-, 9-, 14- and 19-slot widths to accommodate different analog I/O sizing requirements.

The AMXbus™ allows DAC analog outputs to be routed to the VMIVME-3100 ADC board where they can be digitized and compared with the 12-bit word originally written to the DAC board. This digital-to-analog, back-to-digital wrapback test can be done with the field devices (at P3 or P2 connectors) connected or disconnected. This is accomplished by analog isolation switches (Figure 3.2-2) at the output of the DACs. These switches are turned on or off by the outputs of the on-board control/status register.

Each of the DAC outputs may be multiplexed one at a time via the test MUX shown in Figure 3.2-3. First, a control word must be written to the Control and Status Register (CSR) to determine whether the analog output is to be connected or disconnected from the P3 connector, and to which one of two test busses the output is to be routed. The DAC channel to be tested is written to in the immediate update mode. Address bits A01 through A03 are latched into the test address register. The output of this register selects, via the test MUX, the DAC channel that has just been updated. Test control information previously latched in the CSR passes the DAC output through the analog test switch to Test Bus 2.

Test Bus 2 is routed via the analog backplane (AMXbus™) to the input of the VMIVME-3100 ADC board where it is available for analog-to-digital conversion. When the VMIVME-3100 completes conversion, it sends an end-of-convert signal down the P2 backplane to the VMIVME-4105. This signal removes either of the two test bus outputs from the analog backplane. Along with the Test Bus 2 signal being sent to the ADC board, the analog ground (GND SEN) is switched out to the ADC board. This provides an input to the ADC board which is similar to a differential signal called pseudo differential. Pseudo differential solves some of the common mode error problems associated with single-ended signals. The input to the ADC board is referenced to the ground of the DAC board instead of the local ground at the ADC board, effectively cancelling out common mode errors associated with different ground potentials at each of the boards.

3.3 USING THE VMIVME-4105 TO TEST THE MULTIPLEXER CHANNELS OF THE VMIVME-3200

Similar to the way described in Section 3.2, any one of the DAC outputs can be selected via the test MUX and analog test switch (Figure 3.2-3), to be routed out a separate dedicated analog bus entitled Test Bus 1. This test bus is a dedicated input to any VMIVME-3200 that resides in the same VMIC analog backplane. This test bus can be used by the VMIVME-3200 board to verify each of the 32 multiplexer channels by muxing the test bus input one at a time throughout a selected channel of the VMIVME-3200 onto the VMIVME-3100 ADC board. Refer

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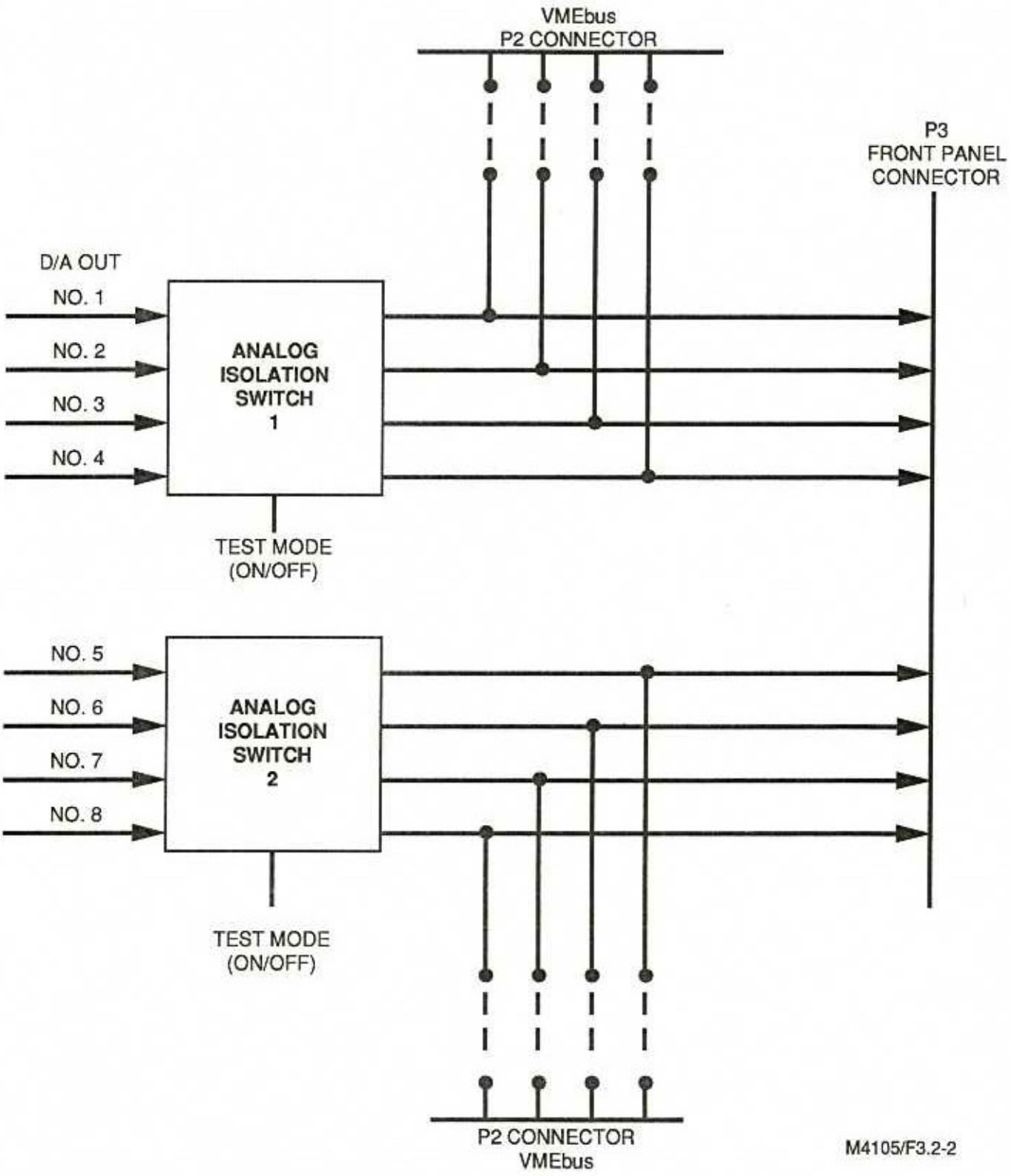


Figure 3.2-2. Analog Output Isolation Switches

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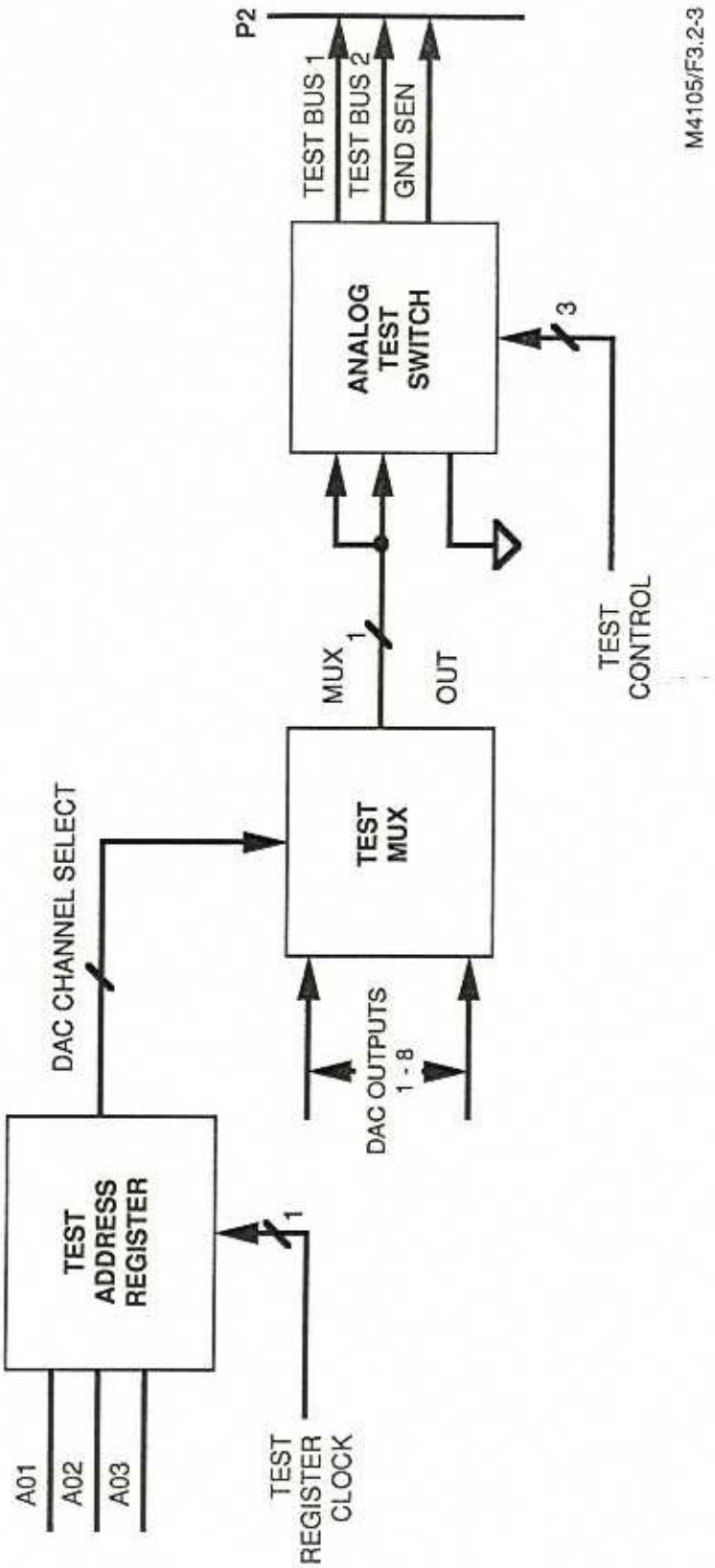


Figure 3.2-3. Test Bus Logic

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to the VMIVME-3200 Instruction Manual and the VMIC High Level Analog Data Acquisition System Manual for more details.

3.4 VMEbus INTERFACE DESCRIPTION

The VMEbus interface (Figure 3.4-1) contains the necessary logic to interface a slave board (VMIVME-4105) to the VMEbus. The VMIVME-4105 is memory mapped in the VMEbus short I/O address space. During a write cycle to the board, address bits A04 through A15 are compared with the previously selected board address. The board address is selected by DIP switches. If the address compares, then a board select signal is issued. This signal, along with the control signals received at the board, gate the data (D0 through D15) to a selected DAC or to the Control and Status Register (CSR) on the VMIVME-4105. Address bits A01 through A03 select one of the eight DAC channels when D15 is written low; data D0 through D11 is latched into the selected DAC register. When D15 is written high to the board, then data D08 through D14 is latched into the CSR.

The VMIVME-4105 circuitry requires +5 V, +15 V, and -15 V. The +5 V is supplied to the board via the P1 and P2 connectors. An on-board DC to DC converter generates the +15 V and -15 V for the analog circuitry, refer to Figure 3.4-2.

3.5 P2 CONNECTOR I/O SIGNAL DEFINITION

a. AINTESTBS (Test Bus 1). An analog test signal that originates from the DAC board and is optionally used by the VMIVME-3200 Multiplexer board to verify the multiplexer channels. Test Bus 1 may be multiplexed through each channel of the VMIVME-3200 MUX board to a VMIVME-3100 ADC board for conversion.

b. AOTESTBS (Test Bus 2). A second analog test bus from the DAC board used in conjunction with the VMIVME-3100 ADC board to verify the 16 analog output channels of the DAC board.

c. GND SEN. In test mode when Test Bus 2 is used, an analog ground from the DAC board is routed out the GND SEN line. The GND SEN line provides for a pseudo-differential input to a receiving ADC board.

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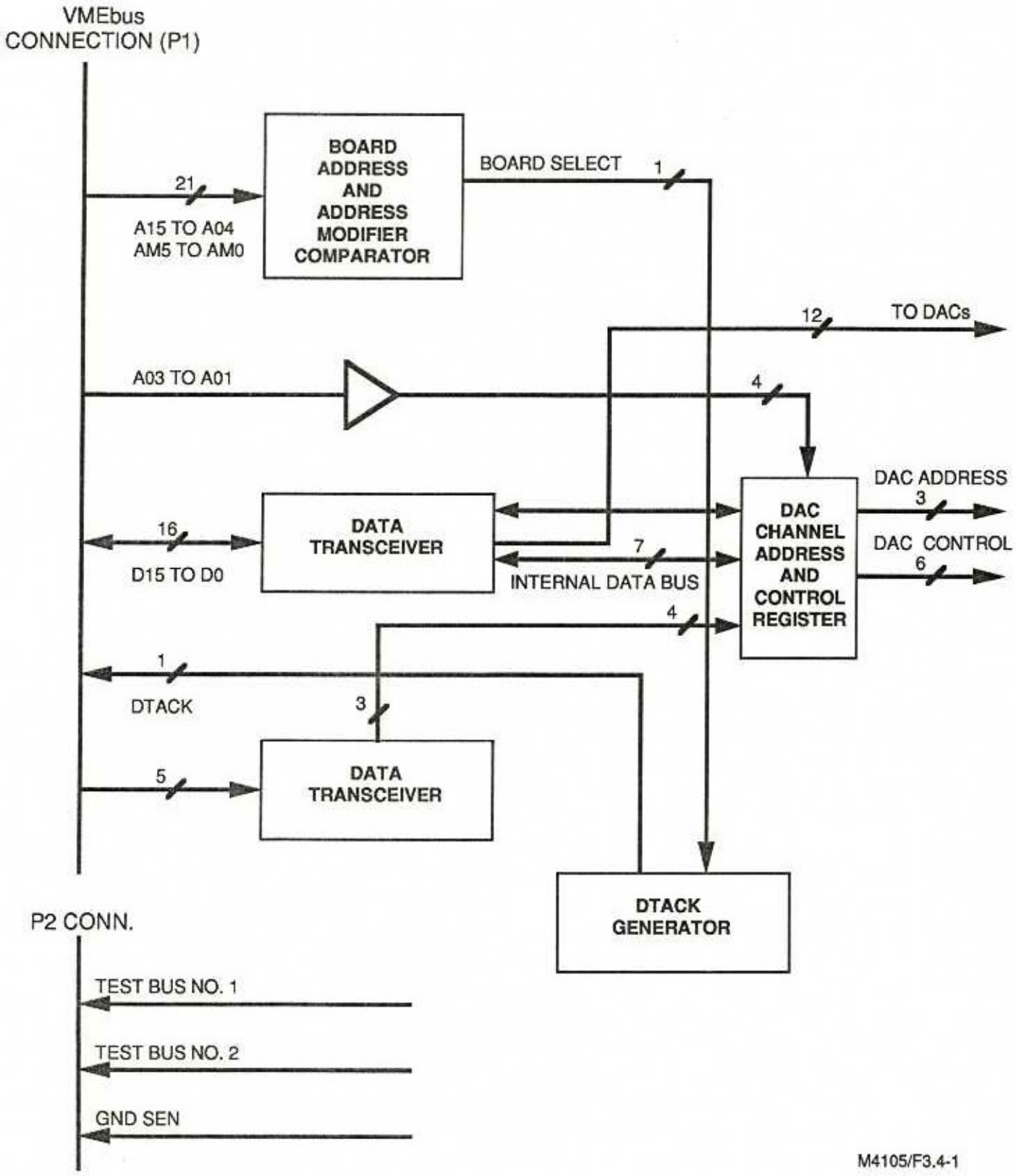


Figure 3.4-1. VMEbus Interface Logic and Interface Signals

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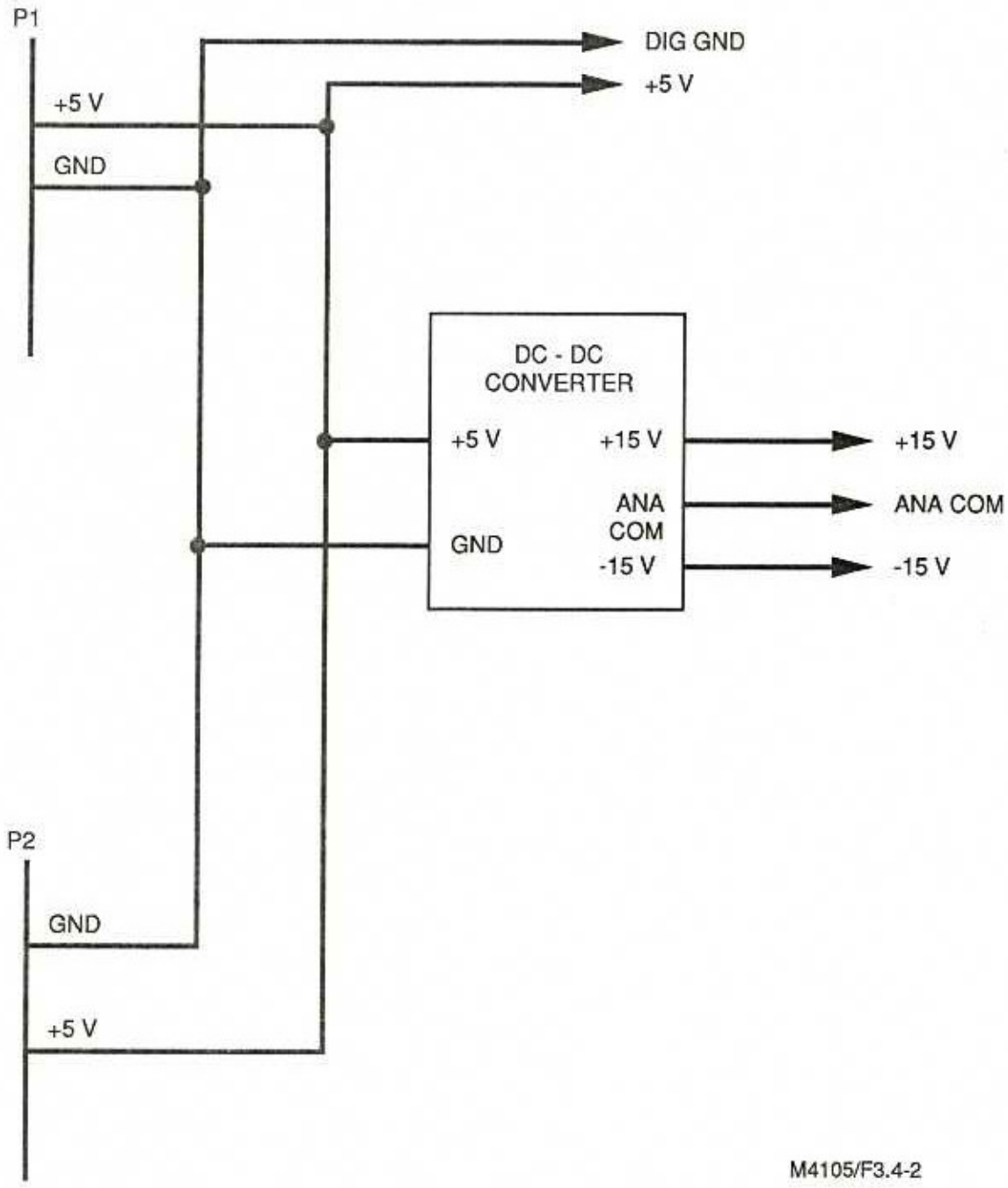


Figure 3.4-2. DAC Board Power

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SECTION 4

PROGRAMMING

4.1 PROGRAMMING

The Multiplying Digital-to-Analog Converter (DAC) board is memory mapped in the short I/O address space. The board occupies eight successive word locations in the VME short I/O address space of 65,535 bytes. The short I/O space is located from XXXX0000 HEX to XXXXFFFF HEX. Each write or read cycle must be a word transfer to an even address, due to the DAC output resolution of 12 bits. The board base address may be selected by DIP switches, as shown in Section 5.6. Table 4.1-1 represents the VMIVME-4105 address map assuming the factory set base address of XXXX0000 HEX. Note that the Control and Status Register (CSR) can be written to and read from any of the eight word locations that the board occupies. When the board is written to, the destination of the data is controlled by data bit 15. If data bit 15 is a "one" the word is written to the CSR; whereas, when data bit 15 is a "zero" the data is written to the DAC which is addressed. Reading any address on the board will return the status of the board.

4.2 PROGRAMMING THE CONTROL AND STATUS REGISTER

There are two types of on-board registers that must be written to for proper operation of the DAC board. There is a storage register for each DAC and there is a CSR that determines the operation of the board.

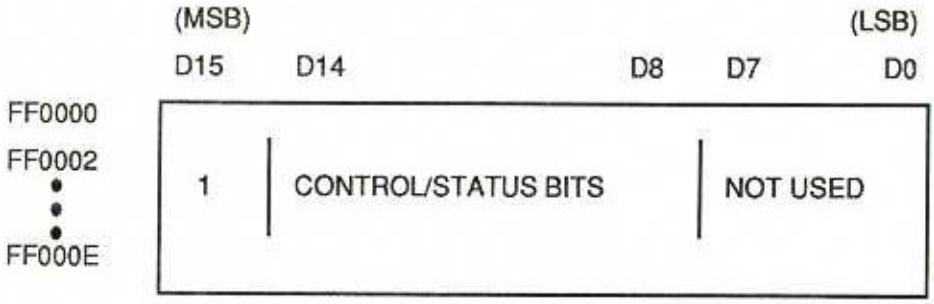
At power-up, the output isolation switches are disengaged. All eight analog output channels may then be initiated to the proper value by writing to the CSR to enable the multiplying DAC outputs P2/P3 connector. The CSR contents may be read at any time for board operational status. The CSR also contains test mode control information, controls the on/off selection of the Fail LED, and enables/disables the selection of the on-board +10 volt reference. The CSR bit definitions are shown in Tables 4.2-1 and 4.2-2.

4.3 PROGRAMMING THE MULTIPLYING DACs

The address map of the eight DACs was shown in Table 4.1-1. This section will describe the 12-bit data word that is written to the DAC to produce the desired analog output. The outputs are jumper selectable (as described in Section 5) between the unipolar outputs (0 V to -10 V) and bipolar (-10 V to +10 V).

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Table 4.1-1. CSR and DAC Channels Address Maps



CSR (READ/WRITE) ADDRESS

ADDRESS	(MSB) D15	D14	D13	D12	D11	(LSB) D0
FF0000	0	NOT USED				DAC OUT 0
FF0002	0	"				DAC OUT 1
FF0004	0	"				DAC OUT 2
FF0006	0	"				DAC OUT 3
FF0008	0	"				DAC OUT 4
FF000A	0	"				DAC OUT 5
FF000C	0	"				DAC OUT 6
FF000E	0	"				DAC OUT 7

DAC CHANNEL (0 TO 7) ADDRESS (WRITE ONLY)

NOTE: Jumper JB determines whether the board operates in short supervisory I/O access or short non-privileged I/O access. With the jumper installed, short non-privileged I/O access is selected.

M4105/T4.1-1

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Table 4.2-1. Control Register Data Format and Definitions

D15	D14	D13	D12	D11	D10	D09	D08	D07	D00
								NOT USED	

•D08 When written high, engages DAC outputs to the P3 connector. Disengages DAC outputs from P3 connector when written low. At power-up, this control bit is low. Note: P3 outputs can be jumpered to P2 outputs (see Table 5.3-1).

•D09 Reference select bit. When high, a user supplied external reference is selected. When low, an on-board +10 volt precision reference is engaged to the eight DACs. This control bit is low at power-up.

•D10 In test mode written high to clock channel address bits A01 through A03 into test register to select one of eight DAC channel outputs. Used in conjunction with D11, D12, and D13 to determine test modes.

•D11 When written high, engages analog outputs from DAC to one of two test buses. Used in conjunction with D12 and D13 to determine which test bus is selected. At power-up, this control bit is low which disengages the test busses.

•D12 A high state enables the selected test analog output to pass out the P2 connector on Test Bus 1 (AINTESTBS). At power-up, this control bit is low.

•D13 A high state enables the selected test analog output to pass out the P2 connector on Test Bus 2 (A0TESTBS). At power-up, this control bit is low.

•D14 A low state turns on the Fail LED. A high state turns it off. At power-up, this control bit is low.

•D15 This bit is used as a register select bit to determine which type of device is to be selected during a write cycle. D15 must be high when writing to the control register. Otherwise, D15 is low when writing to the DAC channels.

M4105/T4.2-1

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Table 4.2-2. Programming the CSR for Different Analog Output Variations - Bit Definitions

1. Analog Output over TEST BUS 1 (AINTESTBS)

D15	D14	D13	D12	D11	D10	D09*	D08
1	1	0	1	1	1	0 or 1	0

2. Analog Output over TEST BUS 2 (AONTESTBS)

D15	D14	D13	D12	D11	D10	D09*	D08
1	1	1	0	1	1	0 or 1	0

3. Analog Output over TEST BUS 2 and out P3 Connector to Field Connector Device (Used for Real-Time Fault Detection of DACs)

D15	D14	D13	D12	D11	D10	D09*	D08
1	1	1	0	1	1	0 or 1	1

4. Analog Output over P3 Connector Only

D15	D14	D13	D12	D11	D10	D09*	D08
1	1	0	0	0	0	0 or 1	1

*Refer to Table 4-2.

M4105/T4.2-2

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4.3.1 Unipolar Analog Outputs (Two Quadrant Multiplier)

A multiplying DAC, such as the one used on the VMIVME-4105 is one in which the input reference voltage can be varied to produce an analog output which is the product of the input code and the input reference voltage.

Data bits D0 (LSB) through D11 (MSB), when written to the desired DAC, along with the reference input, determine the analog output. Table 4.3.1-1 gives the digital input code versus the analog output for unipolar operation when the reference is at a fixed +10 volts.

Table 4.3.1-1. DAC Data Format Unipolar Analog Output vs Digital Input

DIGITAL INPUT CODE (MSB) D15	D14	D13	D12	D11		(LSB) D0	ANALOG OUTPUT VOLTAGE	
0	X	X	X	0000	0000	0000	0 Volts	Zero
0	X	X	X	0100	0000	0000	-2.5 Volts	1/4 Full Scale
0	X	X	X	1000	0000	0000	-5.0 Volts	1/2 Full Scale
0	X	X	X	1100	0000	0000	-7.5 Volts	3/4 Full Scale
0	X	X	X	1111	1111	1111	-9.997 Volts	Full Scale

M4105/T4.3.1-1

The general formula for calculating the analog output for any reference input is:

$$V_{OUT} = -V_{REF} \times \frac{\text{(Digital Input Code in Decimal)}}{4096}$$

Example: The analog output for a digital input of A00 HEX, assuming a fixed reference of 5.00 volts, would be:

(1) A00 decimal equivalent is 2560

(2) Analog out = $-5 \frac{(2560)}{4096} = -3.125$ Volts

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4.3.2 Bipolar Analog Outputs (Four Quadrant Multiplier)

In the bipolar operation, the user may select between the offset binary and two's complement input code. The codes are jumper selectable and the jumper configuration is shown in Section 5. In bipolar operation, the analog output range is from -10 volts to +10 volts. The digital coding for offset binary is represented in Table 4.3.2-1, and Table 4.3.2-2 represents two's complement operation.

Table 4.3.2-1. DAC Data Format Bipolar Analog Output vs Offset Binary Digital Input (±10 V Scale)

DIGITAL INPUT CODE (MSB) D15	D14	D13	D12	D11		(LSB) D0	ANALOG OUTPUT VOLTAGE	
0	X	X	X	0000	0000	0000	-10.000 V	-Full Scale
0	X	X	X	0100	0000	0000	-5.000 V	-1/2 Scale
0	X	X	X	1000	0000	0000	0.000 V	Zero
0	X	X	X	1000	0000	0001	+4.88 mV	+1 LSB
0	X	X	X	1100	0000	0000	+5.000 V	+1/2 Scale
0	X	X	X	1111	1111	1111	+9.9951 V	+Full Scale -1 LSB

M4105/T4.3.2-1

$$V_{OUT} = -V_{REF} + V_{REF} \left(\frac{\text{Digital Input Code in Decimal}}{4096}\right) \times 2$$

Example: The analog output for a digital input of A00 HEX, assuming a fixed reference of 5.00 volts, would be:

(1) A00 decimal equivalent is 2560

(2) Analog out = $-5 + 5 \left(\frac{2560}{4096}\right) \times 2$

$= -5 + (3.125 \times 2)$

$= 1.25$ volts

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Table 4.3.2-2. DAC Format Analog Output vs Two's Complement Digital Input (±10 V Scale)

DIGITAL INPUT CODE (MSB) D15	D14	D13	D12	D11		(LSB) D0	ANALOG OUTPUT VOLTAGE
0	X	X	X	0000	0000	0000	Zero
0	X	X	X	0100	0000	0000	+5.000 V
0	X	X	X	1000	0000	0000	-10.000 V
0	X	X	X	0000	0000	0001	4.88 MV
0	X	X	X	1100	0000	0000	-5.000 V
0	X	X	X	0111	1111	1111	+9.9951 V

M4105/T4.3.2-2

4.4 TEST MODE PROGRAMMING

As described in Section 3.2, any of the 16 DAC outputs may be selected to pass to a VMIVME-3100 ADC board over Test Bus 2 to verify the DAC outputs. If a VMIVME-3200 is present in the analog backplane, then any DAC output can be selected to go to that board for test purposes over the two test busses as follows:

First, a control word should be written to the CSR. In this control word, information as to which test bus the DAC output is to be routed and when the output is to be isolated or connected to the P3 connector is included (refer to Tables 4.2-1 and 4.2-2. The DAC to be updated is then loaded with a 12-bit word. The channel is updated and passes out the selected test bus.

The test modes can only be used if a VMIVME-3100 ADC board exists in the same VMIC analog (P2) backplane as the VMIVME-4100.

4.5 MC68000 ASSEMBLY LANGUAGE PROGRAMMING OF THE VMIVME-4105 MULTIPLYING DAC BOARD

Only a few assembly language statements are necessary to properly control and utilize the DAC board. It will be assumed that the base address of the card in this example is XXXX0060 HEX. The card address can be determined by referring to Sections 4.1 and 5.2.

This example will load all eight DACs with a full scale value of FFF HEX, giving an analog output over the P3 connector of 9.9951 volts, assuming a fixed reference of +10.000 volts. The DAC output value will be updated immediately upon being written to. The board must be jumpered to give bipolar outputs, as described

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in Section 5. The following program is intended as an instructional example only and may not be useful in the user's application. A flowchart of this example is shown in Figure 4.5-1, and the assembly language program is shown in Table 4.5-1.

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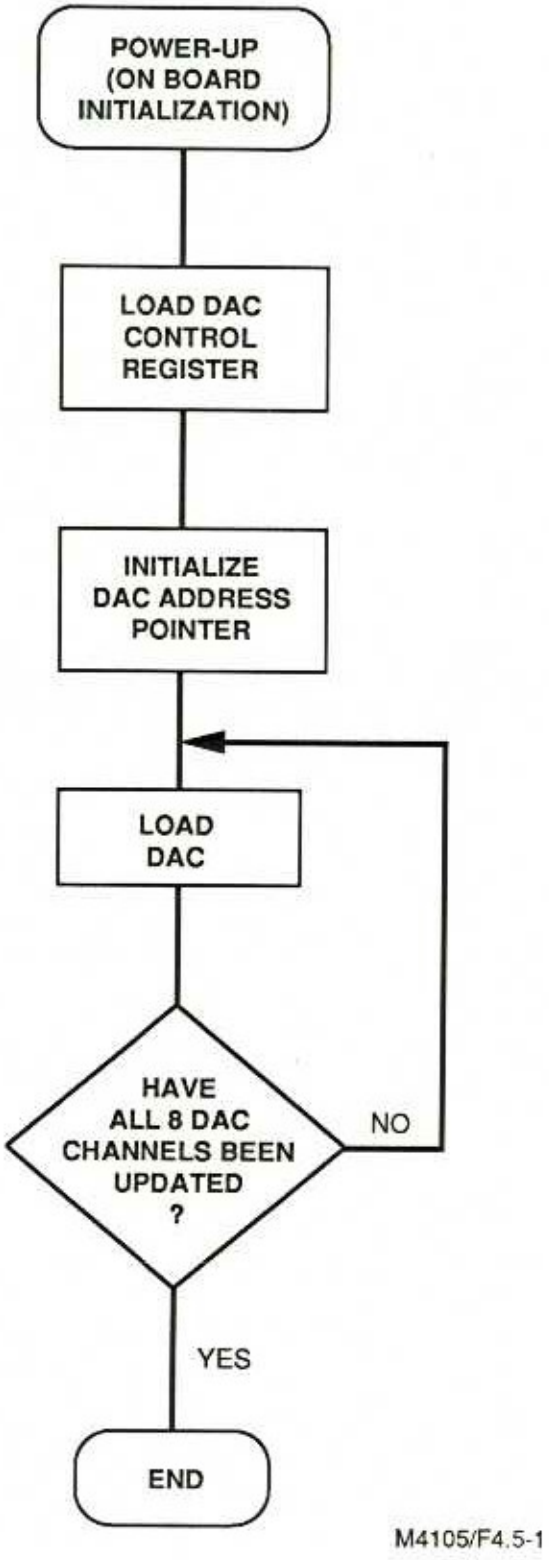


Figure 4.5-1. DAC Programming Sequence

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Table 4.5-1. Program Example

```
                                                    COMMENT
LDDACs      EQU         $
            MOVE.W      #0,D0                       1
            MOVE.W      #$C100,$FF0060              2
            LEA         $FF0060, A0                 3
LDNXT       MOVE.W      #$0FFF, (A0)+               4
            ADD.W       #1, D0                      5
            CMP.W       #$0008, D0                  6
            BNE         LDNXT                       7
            RTS                                     8
```

COMMENTS

1. Initialize register D0 (used as a counter) to 0
2. Load control register to enable DAC outputs to P3 connector
3. Load address of DAC channel no. 1 into address register A0
4. Load DAC channel with maximum value. Address pointer is automatically incremented to next DAC channel
5. Increment counter stored in D0
6. If all eight DAC channels have not been loaded, then go to step 7
7. Load next DAC channel
8. Else STOP

In comment 2, the control register was set to enable the analog outputs over the P3 connector. The outputs could have also been selected to pass out either of the two test busses or out the AOTESTBS and the P3 connector simultaneously by selecting the proper control word as determined from Table 4.2-2 and the HEX value for the different control words shown below in Table 4.5-2.

M4105/T4.5-1

Table 4.5-2. Analog Output Control in Immediate Update Mode

ANALOG OUT PATHWAY	CONTROL WORD (D15 TO D0) HEX VALUE
P3 CONNECTOR	C100
AOTESTBS (TEST BUS 2)	EC00
AINTESTBS (TEST BUS 1)	DC00
AOTESTBS & P3 CONNECTOR	ED00

M4105/T4.5-2

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, etc., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

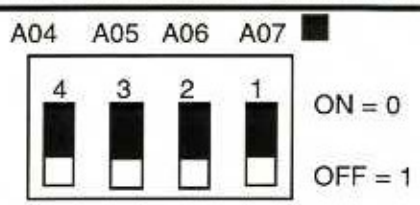
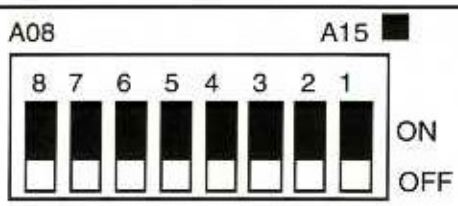
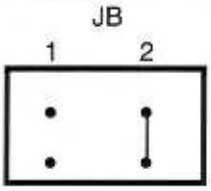
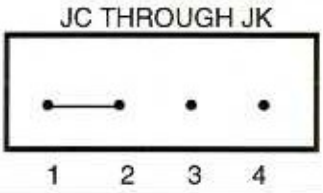
De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the card is properly aligned and oriented in the supporting card guides, slide the card smoothly forward against the mating connector until firmly seated.

5.3 INSTALLATION

This section describes the VMIVME-4105 Digital-to-Analog Converter (DAC) board setup procedure and jumper configuration. The board select base address and board jumper configuration are factory preset and shown in Table 5.3-1. The base address selection switches (S1 and S2) are all shown in the "on" position. This implies a base address for the board at XXXX0000H. Refer to the system specific documentation for the address information to substitute for the "XXXX_ _ _ _" to access system short I/O address space.

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Table 5.3-1. VMIVME-4105 Factory Set Jumpers and Address Switch Configurations

JUMPER	FUNCTION	FACTORY PRE-SET CONDITION
S1	BASE ADDRESS SELECTION SWITCH (A07 TO A04)	
S2	BASE ADDRESS SELECTION SWITCH (A15 TO A08)	
JA	DETERMINES ADDRESS MODIFIERS RESPONSE OF THE BOARD. FACTORY INSTALLED JUMPER SELECTS RESPONSE TO SHORT NON-PRIVILEGED I/O ACCESS	
JB	SELECTS OFFSET BINARY OR UNIPOLAR BINARY CODING WHEN CONNECTED ACROSS JB-2. SELECTS TWO'S COMPLEMENT BINARY CODING WHEN INSTALLED ACROSS JB-1.	
JC, JD, JE, JF, JG, JH, JJ, JK	JUMPER INSTALLED ACROSS PINS 1 & 2 GENERATES BIPOLAR OUTPUTS (±10 V). INSTALLED ACROSS PINS 3 AND 4 GENERATES UNIPOLAR OUTPUTS (0 TO - 10 V)	

M4105/T5.3-1

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Table 5.3-1. VMIVME-4105 Factory Set Jumpers and Address Switch Configuration (Concluded)

JUMPER	FUNCTION	FACTORY PRE-SET CONDITION
JN1	ROUTES ANALOG COMMON TO P2 A18	INSTALLED
JN2	ROUTES ANALOG COMMON TO P2 A16	INSTALLED
JN3	ROUTES ANALOG COMMON TO P2 C17	INSTALLED
JN4	ROUTES ANALOG COMMON TO P2 C15	INSTALLED
JN5	ROUTES ANALOG COMMON TO P2 A1	INSTALLED
JN6	ROUTES ANALOG COMMON TO P2 A2	INSTALLED
JN7	ROUTES ANALOG COMMON TO P2 A3	INSTALLED
JN8	ROUTES ANALOG COMMON TO P2 A4	INSTALLED
JN9	ROUTES ANALOG COMMON TO P2 A5	INSTALLED
JN10	ROUTES ANALOG COMMON TO P2 A6	INSTALLED
JN11	ROUTES ANALOG COMMON TO P2 A8	INSTALLED
JN12	ROUTES ANALOG COMMON TO P2 A10	INSTALLED
JN13	ROUTES ANALOG COMMON TO P2 C10	REMOVED
JN14	ROUTES ANALOG COMMON TO P2 C9	INSTALLED
JN15	ROUTES ANALOG COMMON TO P2 C8	REMOVED
JN16	ROUTES ANALOG COMMON TO P2 C7	INSTALLED
JN17	ROUTES ANALOG COMMON TO P2 C6	REMOVED
JN18	ROUTES ANALOG COMMON TO P2 C5	REMOVED
JN19	ROUTES ANALOG COMMON TO P2 C4	REMOVED
JN20	ROUTES ANALOG COMMON TO P2 C3	REMOVED
JN21	ROUTES ANALOG COMMON TO P2 C2	REMOVED
JN22	ROUTES ANALOG COMMON TO P2 C1	REMOVED
JP1	ROUTES DAC OUT 07 TO P2 A10 (JN12 MUST BE REMOVED)	REMOVED
JP2	ROUTES DAC OUT 06 TO P2 A10 (JN11 MUST BE REMOVED)	REMOVED
JP3	ROUTES DAC OUT 05 TO P2 A6 (JN10 MUST BE REMOVED)	REMOVED
JP4	ROUTES DAC OUT 04 TO P2 A5 (JN9 MUST BE REMOVED)	REMOVED
JP5	ROUTES DAC OUT 03 TO P2 A4 (JN8 MUST BE REMOVED)	REMOVED
JP6	ROUTES DAC OUT 02 TO P2 A3 (JN7 MUST BE REMOVED)	REMOVED
JP7	ROUTES DAC OUT 01 TO P2 A2 (JN6 MUST BE REMOVED)	REMOVED
JP8	ROUTES DAC OUT 00 TO P2 A1 (JN5 MUST BE REMOVED)	REMOVED
THE JUMPERS BELOW ARE USED TO ENABLE THE DESIRED EXTERNAL REFERENCE SELECTION		
JM1 (PIN B-C); JM2-JM8 (PINS A-B)	EXTERNAL REFERENCE FROM P2 CONNECTOR PIN A11 IS BROUGHT INTO THE BOARD AND TO EACH OF THE EIGHT DACs WHEN INSTALLED AND ENABLED BY SOFTWARE	THIS CONFIGURATION IS NOT INSTALLED AT FACTORY
JM1 TO JM8 (PINS A-B)	EXTERNAL REFERENCE FROM P3 CONNECTOR PIN A9 IS BROUGHT INTO THE BOARD AND TO EACH OF THE EIGHT DACs WHEN INSTALLED AND ENABLED BY SOFTWARE	THIS CONFIGURATION IS INSTALLED AT FACTORY
JM1 TO JM8 (PIN B-C)	THIS JUMPER CONFIGURATION BRINGS IN EIGHT INDIVIDUAL EXTERNAL REFERENCES TO THE EIGHT DACs VIA THE P2 CONNECTOR (JN1 AND JN2 MUST BE REMOVED WHEN CONFIGURING JUMPER JM5 AND JM6 B TO C)	THIS CONFIGURATION IS NOT INSTALLED AT FACTORY

M4105/T5.3-1

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5.4 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, go through the following checklist to verify the board is ready for the intended operation:

a. Have the sections on Theory and Programming of the DAC board, Sections 3 and 4, been read and applied to system requirements? √

b. Review Table 5.3-1 to verify the factory installed jumpers and board address switches are set to what is desired. _____

(1) To change DAC board Address Switches (S1 & S2), refer to Section 5.6.
(2) To change address modifier response jumper (JB), refer to Section 5.7.
(3) To change digital binary codes, refer to Section 5.8.
(4) To select either unipolar or bipolar outputs, refer to Section 5.9.
(5) To change external reference input selection, refer to Section 5.10.

c. To re-calibrate +10 volt precision reference, refer to Section 5.11 (not necessary when board is received from factory). _____

d. Has the cable, with proper mating connector, been connected to the analog output connector (P3)? Refer to Section 5.12. _____

e. When optional output isolation hardware is employed on the VMIVME-4105, review Section 5.13 for load impedance requirement. _____

f. If the outputs are to interface with the P2 and P3 connector, refer to Section 5.14. _____

g. To re-calibrate the gain of each DAC, refer to Section 5.15 (not necessary when board is received from factory). _____

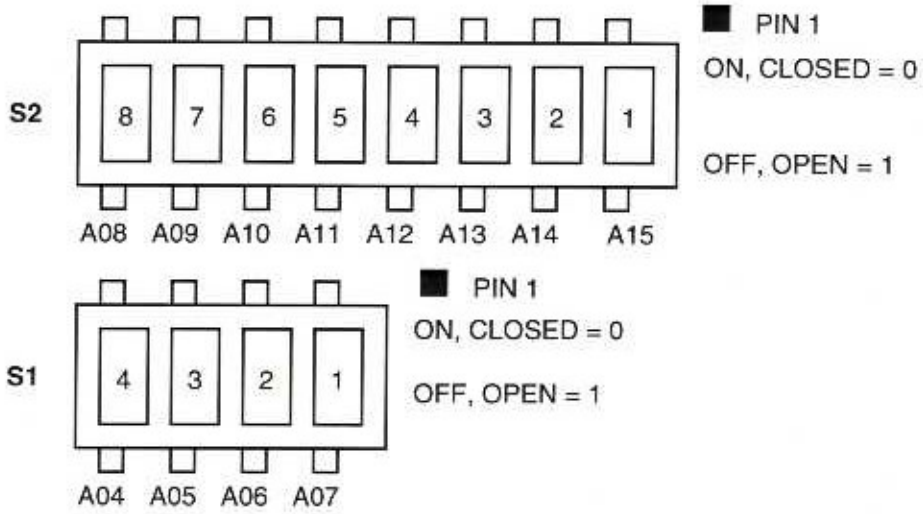
5.5 DAC BOARD INSTALLATION

After steps a through b have been reviewed in Section 5.4, then the DAC board may be installed in a VMEbus system. (Do not install or remove the board with power on). The DAC board may generally be installed in any slot position, except slot one which is usually reserved for the master processing unit.

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5.6 BOARD ADDRESS SELECTION - SWITCHES

There are two address select DIP switches on the VMIVME-4105 Board. Each individual switch corresponds to an address bit or is not used. If the switch is "ON", the corresponding address bit is compared to a logic "zero". All corresponding address bits must compare with the switch positions during a write/read of the DAC board. Figure 5.6-1 shows how each switch corresponds to the address bits. See Figure 5.6-2 for switch locations on the board.



Example: For the VMIVME-4105 to respond to a base address of XXXXFF00, the S1 and S2 switches would be set accordingly.

	1	2	3	4	5	6	7	8
S2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S1	ON	ON	ON	ON				

M4105/F5.6-1

Figure 5.6-1. DIP Switch Address Map

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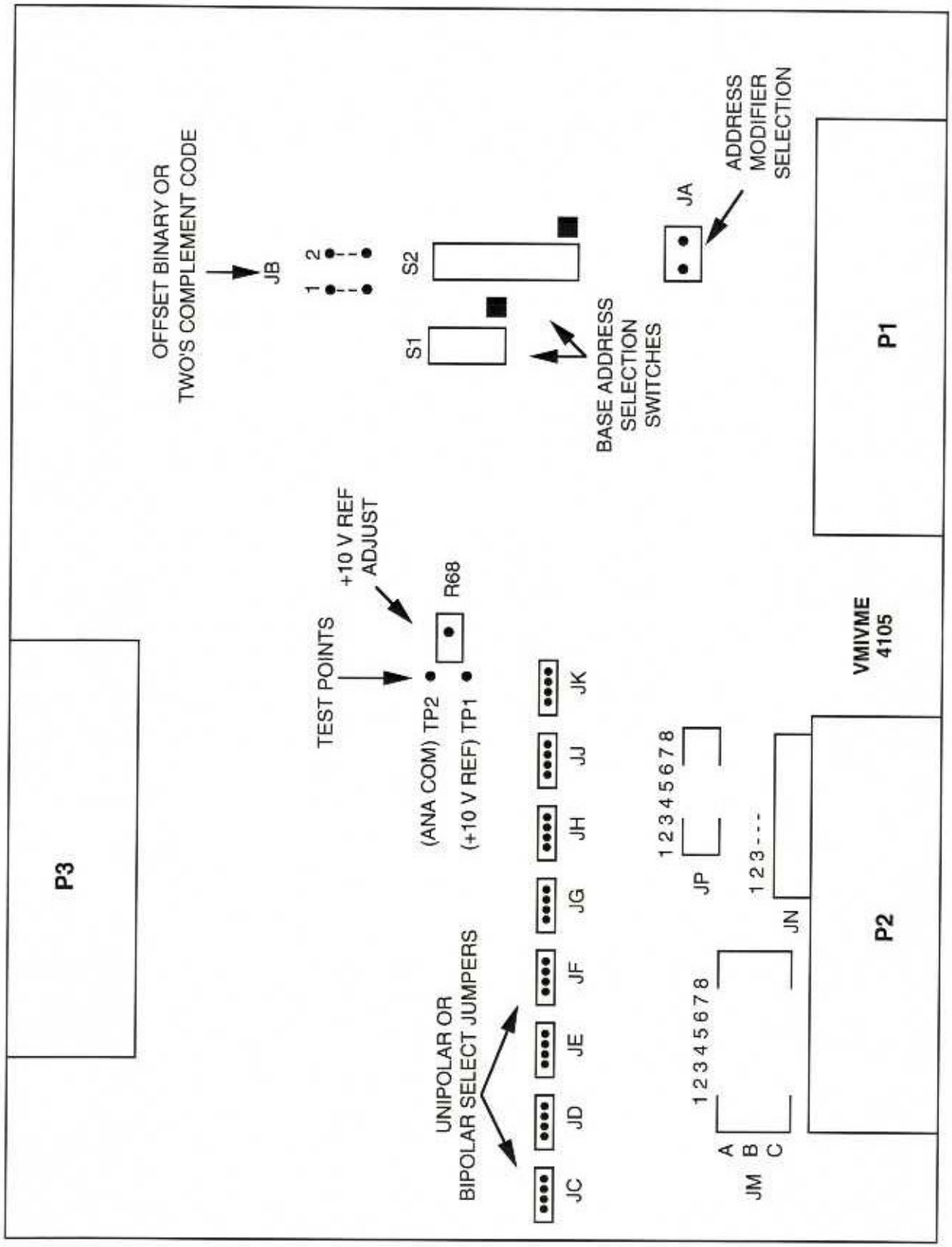


Figure 5.6-2. Jumper and Switch Locations on VMIVME-4105 (Component Side Shown)

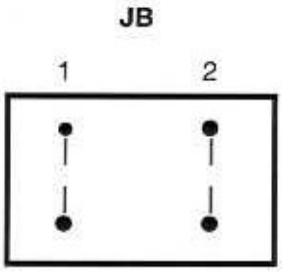
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5.7 ADDRESS MODIFIER RESPONSE SELECTION

The DAC board is memory mapped in the short I/O address space, as described previously in Section 4.1. The DAC board will respond to either of the two address modifier codes that may be issued to the DAC board by a CPU board during a write or read cycle. The DAC board is factory set to respond to supervisory short I/O access. To select non-privileged short I/O Access, install jumper at jumper location JA. See Figure 5.6-2 for jumper location.

5.8 DAC DIGITAL CODE SELECTION

The Most Significant Bit (MSB) (D11) written to the selected DAC channel may or may not be inverted by jumper JB. Inversion of D11 generates two's complement for bipolar operation (±10 V outputs). If D11 is not inverted, then digital coding is straight unipolar binary coding for unipolar outputs (0 to -10 V) and offset binary for bipolar outputs (±10 V). Figure 5.6-2 shows code selection using jumper JB. Figure 5.8-1 shows jumper JB.



JUMPER JB-2 FOR OFFSET BINARY OR UNIPOLAR BINARY

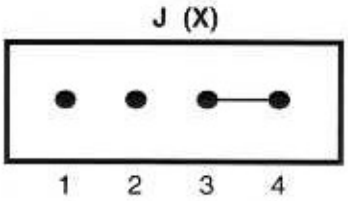
JUMPER JB-1 FOR TWO'S COMPLEMENT BINARY

M4105/F5.8-1

Figure 5.8-1. Digital Code Selection

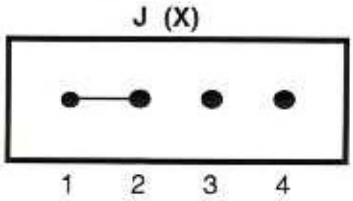
5.9 UNIPOLAR (0 to -10 V) OR BIPOLAR (±10 V) OUTPUT SELECTION

a. Unipolar outputs
(Jumpers JC, JD, JE, JF, JG, JH, JJ, JK Pins 3 to 4)



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b. Bipolar Outputs
(Jumpers JC, JD, JE, JF, JG, JH, JJ, JK Pins 1 to 2)

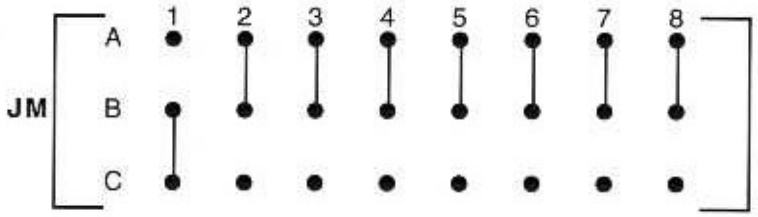


The JC, JD, JE, JF, JG, JH, JJ, JK jumper locations are shown in Figure 5.6-2.

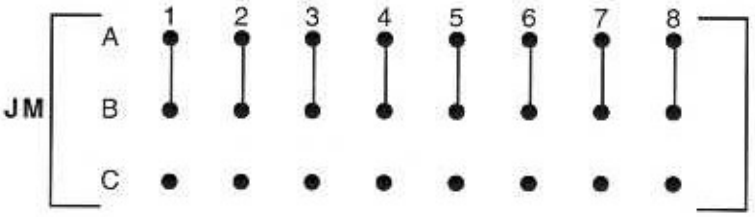
5.10 EXTERNAL DAC REFERENCES SELECTION

There are three different ways that one or more external references may be brought into the separate DAC reference inputs. This is determined by the JM jumper field. The JM jumper location is shown in Figure 5.6-2.

a. An external reference may be user supplied to P2 connector pin A11 (pin C11 is ANA GND) where, under software control, it is switched into all eight DAC reference inputs. The jumper configuration for this connection is as follows:



b. An external reference may be user supplied to the front panel P3 connector pin A9 (pin C9 is ANA GND) where, under software control, it is switched into all eight DAC reference inputs. The jumper configuration for this connection is as follows:

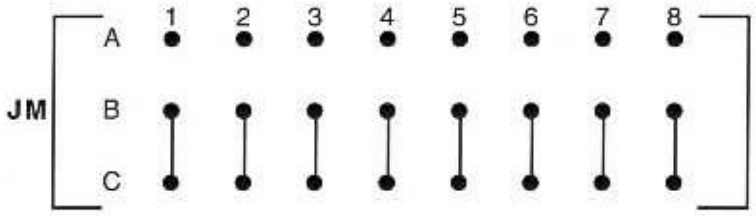


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c. Eight individual external references may be brought into each respective DAC via the P2 connector. To select this configuration, or any external reference configuration, the external reference select bit (D09) must be written high to the control register. The jumper configuration for this connection is as follows:

CAUTION

JUMPERS JN1 AND JN2 MUST BE REMOVED WHEN CONFIGURING JUMPER JM5 AND JM6 B TO C.



5.11 CALIBRATING THE +10 VOLT PRECISION REFERENCE

The +10 V precision reference has been adjusted at the factory and lock-tight has been applied to potentiometer adjustment to ensure no changes in shipping and handling. However, the adjustment is easily broken away for user adjustment, if necessary. Long term drift of the reference is very low (0.25 mV/1000 hrs). It is advised that after 6,000 hours of operation, or if the reference output (P2 connector) is being used by other devices, the reference voltage be checked with a 4-1/2 digit voltmeter. The procedure is as follows:

a. Remove any cable connected to the P3 connector.
b. Apply power to the board and let warm up 15 minutes.
c. Attach the negative lead of the voltmeter to Test Point 2.
d. Attach the positive lead of the voltmeter to Test Point 1.
e. If voltage is not within 1.0 mV of +10 V, then re-calibrate reference.
f. Re-calibrate reference by adjusting potentiometer R68 (board location shown in Figure 5.6-2) to +10 V (± 0.5 mV).

5.12 CONNECTOR DESCRIPTIONS

Two connectors P1 and P2 connect the DAC board to the VMEbus backplane. The connectors are 96-pin DIN type. The primary connector, P1, contains the address data and control lines, and all additional signals necessary to control data transfer and other bus functions. P2 connector carries the I/O lines necessary to join the DAC board with the optional VMIVME-3200 MUX Expander board and the VMIVME-3100 12-Bit ADC board. The P2 connector connects the DAC board with the Analog Multiplexer P2 Backplane (AMXbus™). The P2 connector may support the built-in-test signal which are routed to other VMIC

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analog boards. This is the case when the eight DAC channels are output via the front panel P3 connector only. This is referred to as the normal operating mode and the P2 signal assignments for normal operating mode are shown in Table 5.12-1. Figure 5.12-1 shows the P2 connector pin layout.

If the eight DAC channels are selected to go out the P2 connector (by jumper configuration shown in Section 5.14), the built-in-test signals which interface with the AMXbus™ are disengaged. The P2 signal assignments for this mode are shown in Table 5.12-2.

The external reference selection allows for one common external reference to be brought into the P2 connector (P2 EXTREF IN) or the P3 connector (P3 EXTREF IN) to be routed to all eight DAC channels. The external reference must supply an analog ground return to the board. For example, P2 EXTREF IN, according to Table 5.12-2 enters the board via P2 - A11. The external reference ground should connect the board analog common at P2 - C11. If all eight external references are selected, they must have a common ground, and that common ground should connect to at least one Row C ANA COM pin on the P2 connector.

If the test bus option is to be used in conjunction with other VMIC Analog I/O cards, then the user may use a VMIVME printed circuit Analog P2 Multiplexer Backplane (AMXbus™). These backplanes are available in different slot widths to accommodate almost any combination of boards.

The P3 connector is a Panduit 32-pin male connector type 120-332-053A. The matching Panduit connector for the input cable is a female connector type 120-332-455E. This connector handles the eight analog outputs, each with an associated analog ground wire. See Figure 5.12-3 and Table 5.12-3 for P3 connector assignment.

5.13 ANALOG OUTPUT ACCURACY WHEN OPTIONAL OUTPUT ISOLATION HARDWARE IS USED

The VMIVME-4105 is offered in several option configurations to the user, one of which is the use of Built-in-Test functions when used with other VMIVME boards, as discussed previously in Section 3.3.

The Built-in-Test hardware features analog output isolation switches for all eight channels that can be turned on/off by software commands. These switches are in series with the analog output and the user-connected device at the P3 connector. These switches have an "ON" resistance of approximately 100 ohms (max). If the user-connected load does not have a high impedance input, then a possible voltage division error is introduced. For example, if R(LOAD) is 10 kΩ, then a 1% error is introduced. R(LOAD) should be one megohm or greater for an error of .01% or less.

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Table 5.12-1. P2 Connector Signal Assignments Built-in-Test (BIT) Signals in Normal Operating Mode with Analog Outputs Going Out the P3 Connectors

PIN NO.	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	ANA COM*	+5 VOLTS	
2	ANA COM*	GND	
3	ANA COM*		
4	ANA COM*		
5	ANA COM*		
6	ANA COM*		
7	AINTESTBS		ANA COM*
8	ANA COM*		
9	AOTESTBS		ANA COM*
10	ANA COM*		
11			ANA COM
12	ANA COM	GND	ANA COM
13		+5 VOLTS	ANA COM
14	ANA COM		ANA COM
15	GND SEN		ANA COM*
16	ANA COM*		ANA COM
17	+10 VOLT REF		ANA COM*
18	ANA COM		ANA COM
19			ANA COM
20	ANA COM		ANA COM
21			
22	ANA COM	GND	
23	ANA COM		
24	ANA COM		
25			
26			
27			
28			
29			
30			
31		GND	
32		+5 VOLTS	

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*With jumper installed. See Table 5.3-1.

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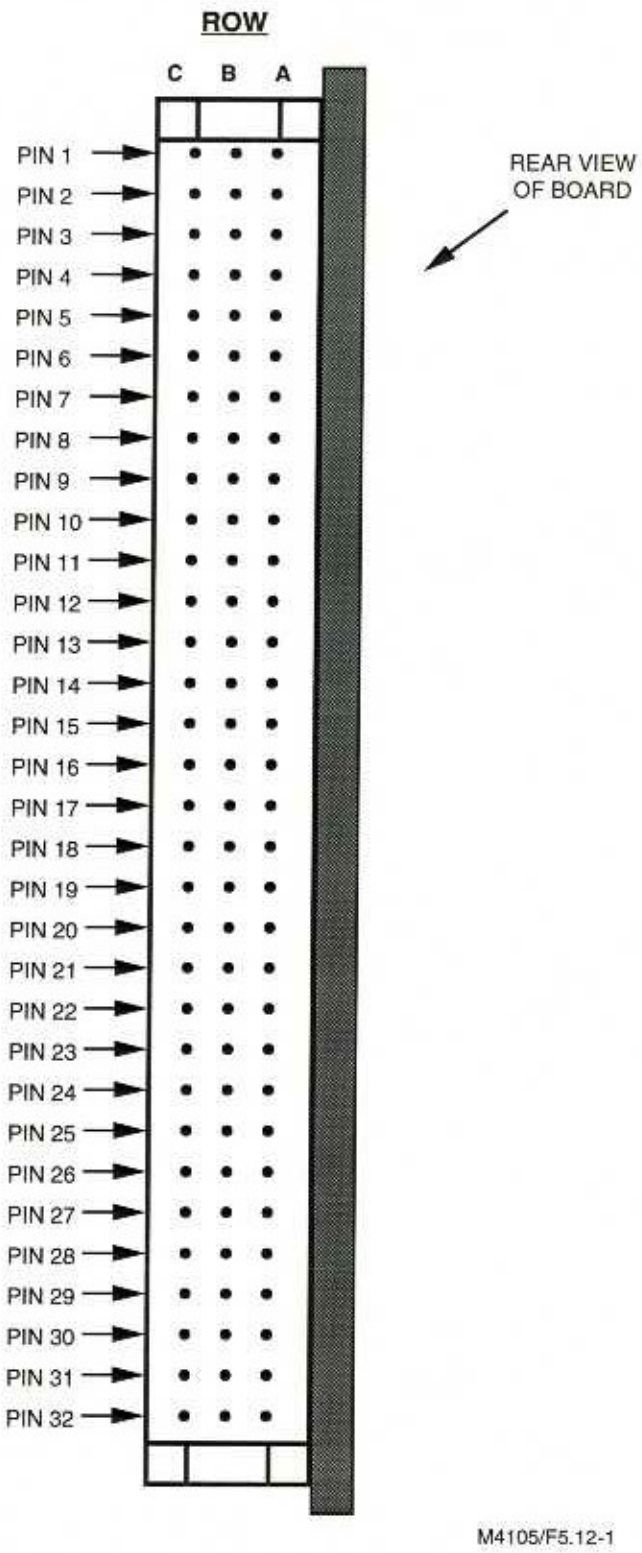


Figure 5.12-1. P2 Connector Pin Layout

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Table 5.12-2. P2 Connector Signal Assignments When Analog Outputs are Going Out the P2 Connectors

PIN NO.	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	ANO0 (CH1)*	+5 VOLTS	ANA COM*
2	ANO1 (CH2)*	GND	ANA COM*
3	ANO2 (CH3)*		ANA COM*
4	ANO3 (CH4)*		ANA COM*
5	ANO4 (CH5)*		ANA COM*
6	ANO5 (CH6)*		ANA COM*
7	AINTESTBS		ANA COM*
8	ANO6 (CH7)*		ANA COM*
9	AOTESTBS		ANA COM*
10	ANO7 (CH8)*		ANA COM*
11	P2 EXTREF IN		ANA COM
12	EXTREF 2	GND	ANA COM
13	EXTREF 3	+5 VOLTS	ANA COM
14	EXTREF 4		ANA COM
15	GND SEN*		ANA COM*
16	EXTREF 5		ANA COM
17	+10 VOLT REF		ANA COM*
18	EXTREF 6		ANA COM
19	EXTREF 7		ANA COM
20	EXTREF 8		ANA COM
21			
22		GND	
23			
24			
25			
26			
27			
28			
29			
30			
31		GND	
32		+5 VOLTS	

*With jumper installed. See Table 5.3-1.

M4105/T5.12-2

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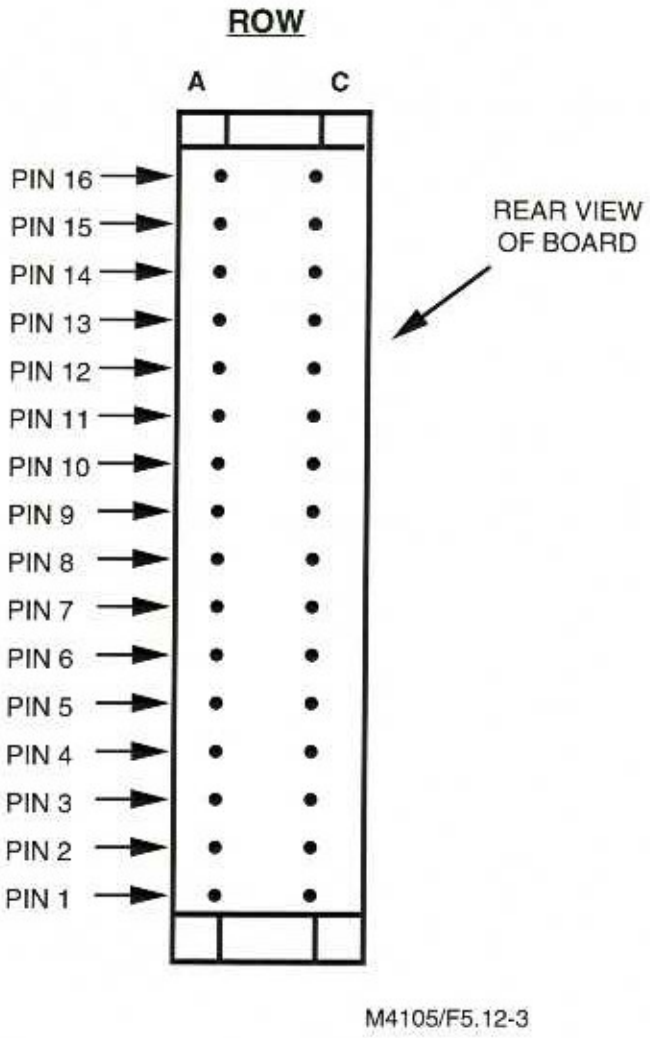


Figure 5.12-3. P3 Connector Pin Layout

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Table 5.12-3. P3 Connector Signal Assignments

PIN NO.	ROW A	ROW B	ROW C
1	ANO0 (CH1)		ANA COM
2	ANO1 (CH2)		ANA COM
3	ANO2 (CH3)		ANA COM
4	ANO3 (CH4)		ANA COM
5	ANO4 (CH5)		ANA COM
6	ANO5 (CH6)		ANA COM
7	ANO6 (CH7)		ANA COM
8	ANO7 (CH8)		ANA COM
9	P3 EXTREF IN		ANA COM
10	+10 V REF OUT		ANA COM
11			ANA COM
12	ANA COM		ANA COM
13	ANA COM		ANA COM
14	ANA COM		ANA COM
15	ANA COM		ANA COM
16	ANA COM		ANA COM

M4105/T5.12-3

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5.14 ROUTE ANALOG OUTPUTS TO P2 AND P3 CONNECTORS

The VMIVME-4105 offers the user the option of having the eight analog outputs routed to the front panel P3 connector (factory configured) or to both the P3 front panel connector and the VMEbus P2 connector (user configured). The jumper configuration for P2 connection is shown in Figure 5.14-1.

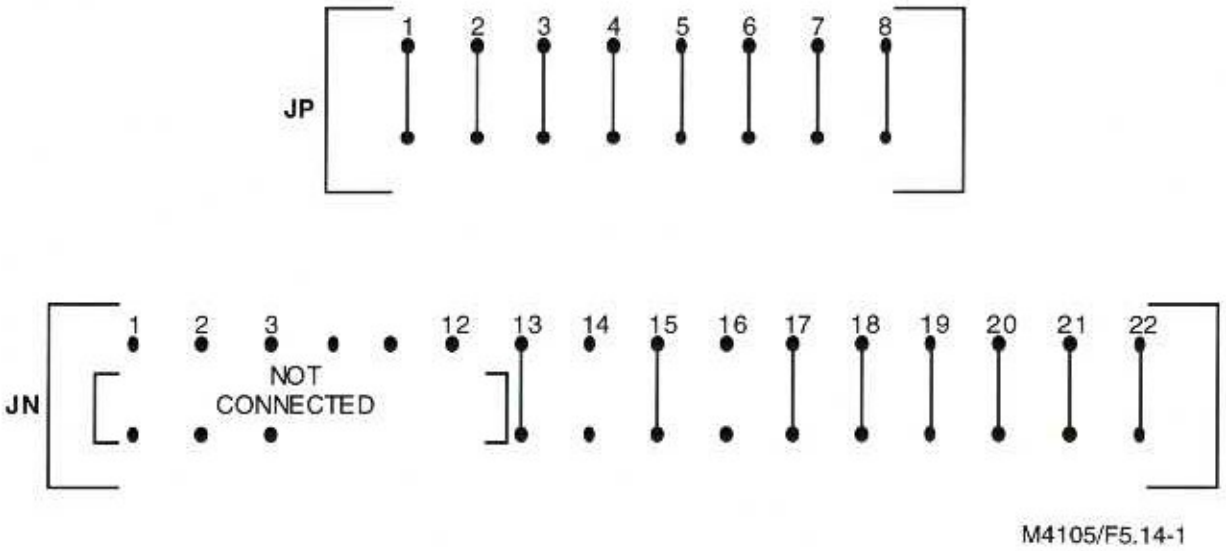


Figure 5.14-1. Jumper Configuration Analog Outputs Out P2 Connector

5.15 GAIN CALIBRATION

The gain potentiometers are precalibrated, and lock-tight is applied to the adjustments. Normally no calibration will be required by the user. If re-calibration is required, then it can be done with a 4-1/2 digit voltmeter. First, enable the outputs to the P3 connector for easier monitoring by a voltmeter probe at the connector pins. Connect the GND lead of the voltmeter to Row C, Pin 1 of P3 connector (see Figure 5.12-3). Write the maximum value FFF HEX to all eight channels. Connect the positive lead of the voltmeter to the pins as shown in Table 5.15-1. Adjust the corresponding potentiometer to read the reference DC voltage -1 Least Significant Bit (LSB). For example, for a +10 V reference, the maximum output for each channel is 9.9951 volts.

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Table 5.15-1. Gain Adjustment Procedure

READ VOLTAGE AT FOLLOWING PIN OF P3 CONNECTOR	ADJUST FOLLOWING POTENTIOMETER	ADJUST FOR FOLLOWING VOLTAGE (+10 Volt Ref.)
A1	R2	+9.9951 VDC
A2	R3	+9.9951 VDC
A3	R4	+9.9951 VDC
A4	R5	+9.9951 VDC
A5	R6	+9.9951 VDC
A6	R7	+9.9951 VDC
A7	R8	+9.9951 VDC
A8	R9	+9.9951 VDC

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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