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# IP-ENCODER-6

## Six Channel Quadrature IndustryPack® Manual

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**IP-ENCODER-6**
**Six Channel**
**Quadrature**
**IndustryPack®**

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# Product Description

The SBS IP-ENCODER-6 provides six channels of quadrature decoder inputs to an I/O subsystem built around any IndustryPack® host board. The Encoder-6 module is ideal for determining position, velocity and speed of rotational and linear moving objects which use bar-coding and optical detection; typical components in motion control applications.

Each channel has a dedicated quadrature decoder counter implemented using the HP HCTL-2020 integrated circuit. Each counter is 16 bits wide. When the counter overflows or underflows an interrupt is sent to one of the IndustryPack® interrupt request signals. This permits the software driver to maintain an infinitely wide counter.

The input to the counter is two waveforms with a maximum frequency of 1.3 MHz. The relative position of one waveform with respect to the other determines the direction of the count. The skew between each waveform must be greater than 125 ns. Each of the two waveforms is input via a differential line receiver designed to meet the specifications of RS-422-A and RS-423-A. An index input is available for each counter, the assertion of any causing the other IndustryPack® interrupt request signal to assert. The index input is normally used to initialize zero position or signal out of bounds conditions. Read only registers indicated which channels have overflowed, whether up or down, and index input assertion.

Revision B adds new functionality. A software programmable interrupt acknowledge vector allows the user to set bits d1 thru d7 of the vector; bit d0 is automatically set by the hardware depending on whether the interrupt selected is the overflow or index capture. A mask register is available for the overflow signals and for the index capture signals. Each of the six channels may be individually masked with the appropriate bit in the register. A channels mask bit prevents the logic from causing an interrupt for that channel but does not prevent the host from reading the overflow or index register status. Thus a polling of the register may still determine if there is an overflow or an index capture even if the mask is asserted. Revision B also implements a differential line receiver on the index capture input signals. The differential input will assert a channel's index capture when it goes low for a minimum of 125 ns.

The ID Prom on the board can be used for automatic configuration and conforms to the IndustryPack® standard.

The figure on the following page shows a block diagram of the module:



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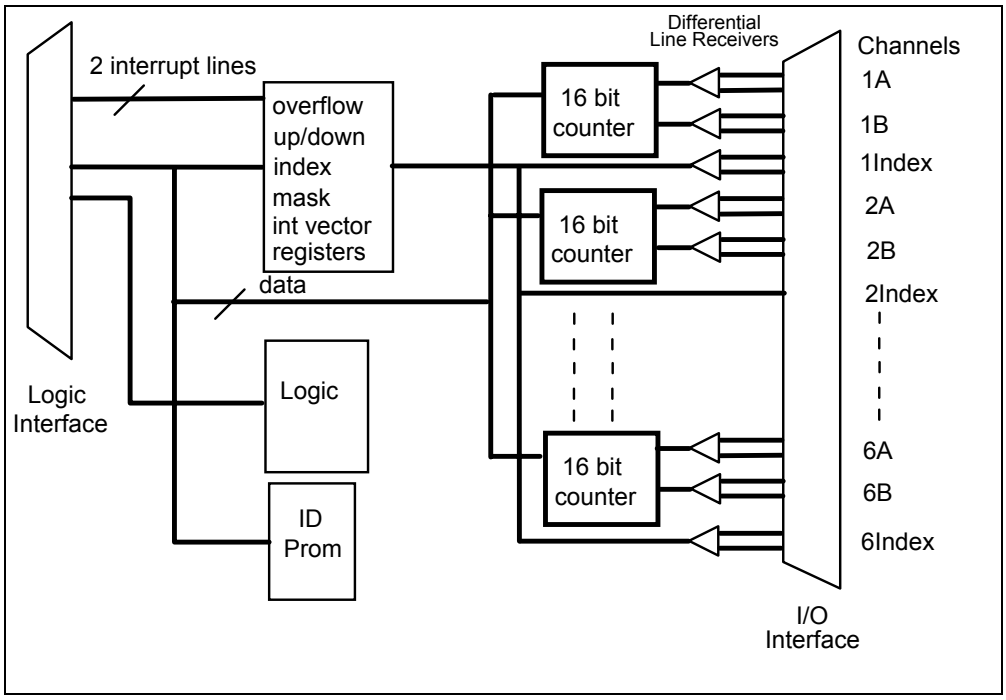



**Figure 1 Simplified Block Diagram of IP-ENCODER-6**



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# VMEbus Addressing

The Encoder-6 I/O module is accessed using the IndustryPack® I/O space. Each channel's count can be read with a 16 bit wide read access. A single read access resets all the channel counters. The overflow, index, and up/down registers can be read indicating the state of each channel. A write to the overflow and index register command clears the state of all channels. The interrupt vector can be programmed by writing the register bits d1 thru d7, (d0 is automatically determined by which of the two interrupts is active.) Each of the channels interrupts may be masked by setting the interrupt mask register; the overflow and index register will have the channel's bit latched asserted but will not cause an interrupt to the host.

The following table maps the address as an offset from the beginning of the modules I/O space:

| Offset (hex) | Width | Port | Read/Write |
|---|---|---|---|
| 00 | word | Counter channel 1 | read only |
| 02 | word | Counter channel 2 | read only |
| 04 | word | Counter channel 3 | read only |
| 06 | word | Counter channel 4 | read only |
| 08 | word | Counter channel 5 | read only |
| 0a | word | Counter channel 6 | read only |
| 0c | byte/word | Reset all channels | read only |
| | | | |
| 10 | word | overflow register | read only |
| 12 | word | index register | read only |
| 14 | word | up/down register | read only |
| 10 | word | clear overflow reg cmd | write only |
| 12 | word | clear index reg cmd | write only |
| 16 | byte | write the IRQ vector | write only |
| 18 | byte | write the IRQ overflow mask | write only |
| 1a | byte | write the interrupt index mask | write only |

Notes:
The overflow register has the following format:
d0 thru d5: channel 1 thru channel6: 0 - asserted, 1 - nonasserted
The index register has the following format:
d0 thru d5: channel 1 thru channel6: 0 - asserted, 1 - nonasserted
The up/down register has the following format:
d0 thru d5: channel 1 thru channel6: 0 - up, 1 - down
The interrupt mask register has the following format:
d0 thru d5: channel 1 thru channel6: 0 - unmask, 1 - masked

**Figure 2 VMEbus Register Map**



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# Programming

The Encoder-6 module will in general be programmed in the following manner:

1. At initialization the channels will be reset to zero by reading to offset 0x0C. Both the overflow and index registers should also be cleared. If a virtual counter of greater than 16 bits is desired, set up an interrupt service routine for INTRQ0 to increment or decrement the virtual counter upon receipt of the interrupt. If indexing is implemented, setup an interrupt service routine for INTRQ1 that saves the counter, or resets the counter upon receipt of the interrupt.

1.B (Rev B only) A vector can be set to respond to those carrier boards that implement the interrupt acknowledge, IntSel*, signal. A byte value should be placed on the low 8 bits of the IndustryPack® data bus using the I/O write access to the address specified in Table 1. The vector is presented on the bus when the IntSel* access is done with the value in the lowest bit, d0, indicating whether Int0 or Int1 is being requested; low for Int0 and high for Int1. For example, if the vector 0xaa is configured, then an acknowledgment of Int0 will yield the vector 0xaa, while an acknowledgment of Int1 will yield the vector 0xab.

1.C (Rev B only) The overflow and index capture mask registers should be set so that only channels required to interrupt the host have their bits unmasked.

2. To read a counter, do a word wide read of the desired channel.

3. If the virtual counter is implemented, the interrupt service routine upon receiving the interrupt, reads the overflow register to see which channel overflowed, reads the up/down register to see if it overflowed up or down, updates the virtual counter, and then clears the overflow register. Note that when reading the overflow register all channels should be checked as two or more channels may have overflowed at the same time.

4. If the index capture input is implemented, the interrupt service routine upon receiving the interrupt, reads the index register to see which channel or channels had its index input asserted, records or initializes the corresponding counter, and then clears the index register.

Notes:
- The overflow and index input capture signals are latched into their corresponding registers and thus the registers must be cleared in the interrupt service routine.
- The HCTL-2020 counters multiply the resolution of the input signals by four.



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# ID PROM

The Encoder-6 module is IndustryPack® compatible and includes an ID PROM. The ID PROM has a maximum size of 32 bytes not all of which contain significant information in the Encoder-6. The ID PROM permits software configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional.

Standard data in the ID PROM on the Encoder-6 module is shown in the table below. For more information on the IndustryPack® ID PROMs refer to the IndustryPack® Logic Interface Specification.

The ID information is accessed via the dedicated ID space. The data is available on the low 8 bits only. Thus sequential addressable locations on the PROM are in increments of two at even locations for little endian CPUs and at odd locations for big endian CPUs. The following table assumes little endian access modes.

| Address | Data | |
|---|---|---|
| 3E<br>\|\|<br>18 | Available for User<br>\|\|<br>Available for User | |
| 16 | Checksum | (1C) |
| 14 | Number of bytes used = 11dec | (0C) |
| 12 | Driver ID, high byte | (00) |
| 10 | Driver ID, low byte | (00) |
| 0E | Reserved | (00) |
| 0C | Revision Number A | (B1) |
| 0A | Model No Digital I/O | (AA) |
| 08 | Manufacturer ID Vigilant | (F0) |
| 06 | ASCII "C" | (43) |
| 04 | ASCII "A" | (41) |
| 02 | ASCII "P" | (50) |
| 00 | ASCII "I" | (49) |

**Figure 3 ID PROM Data (Hex)**



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# I/O Pin Assignment

The following table gives the pin assignments for the I/O connector:

| Pin Number | Channel | Function |
|---|---|---|
| 1 | GND | --- |
| 2 | Channel 6 | I+ (Index input capture) |
| 3 | Channel 6 | I- |
| 4 | Channel 6 | B+ |
| 5 | Channel 6 | B- |
| 6 | GND | --- |
| 7 | Channel 6 | A+ |
| 8 | Channel 6 | A- |
| 9 | GND | --- |
| 10 | Channel 5 | I+ |
| 11 | Channel 5 | I- |
| 12 | Channel 5 | B+ |
| 13 | Channel 5 | B- |
| 14 | GND | --- |
| 15 | Channel 5 | A+ |
| 16 | Channel 5 | A- |
| 17 | GND | --- |
| 18 | Channel 4 | I+ |
| 19 | Channel 4 | I- |
| 20 | Channel 4 | B+ |
| 21 | Channel 4 | B- |
| 22 | GND | --- |
| 23 | Channel 4 | A+ |
| 24 | Channel 4 | A- |
| 25 | GND | --- |
| 26 | GND | --- |
| 27 | Channel 3 | I+ |
| 28 | Channel 3 | I- |
| 29 | Channel 3 | B+ |
| 30 | Channel 3 | B- |
| 31 | GND | --- |
| 32 | Channel 3 | A+ |
| 33 | Channel 3 | A- |
| 34 | GND | --- |
| 35 | Channel 2 | I+ |
| 36 | Channel 2 | I- |
| 37 | Channel 2 | B+ |
| 38 | Channel 2 | B- |
| 39 | GND | --- |
| 40 | Channel 2 | A+ |
| 41 | Channel 2 | A- |
| 42 | GND | --- |
| 43 | Channel 1 | I+ |
| 44 | Channel 1 | I- |
| 45 | Channel 1 | B+ |
| 46 | Channel 1 | B- |
| 47 | GND | --- |
| 48 | Channel 1 | A+ |
| 49 | Channel 1 | A- |
| 50 | GND | --- |

**Figure 4 I/O Pin Assignment**



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# IndustryPack® Logic Interface Pin Assignment

Figure 5 below shows the pin assignments for the IndustryPack® logic interface. Pins that are marked with an "nc" are defined by the specification but not used by the Encoder-6 I/O module.

| Signals | | Pin Numbers | | |
|---|---|---|---|---|
| GND | GND | 1 | 26 | |
| CLK | +5V | 2 | | 27 |
| Reset* | R/W* | 3 | 28 | |
| D0 | IDSel* | 4 | | 29 |
| D1 | nc | 5 | 30 | |
| D2 | nc | 6 | | 31 |
| D3 | nc | 7 | 32 | |
| D4 | INTSel* | 8 | | 33 |
| D5 | nc | 9 | 34 | |
| D6 | IOSel* | 10 | | 35 |
| D7 | nc | 11 | 36 | |
| D8 | A1 | 12 | | 37 |
| D9 | nc | 13 | 38 | |
| D10 | A2 | 14 | | 39 |
| D11 | nc | 15 | 40 | |
| D12 | A3 | 16 | | 41 |
| D13 | INTRQ0* | 17 | 42 | |
| D14 | A4 | 18 | | 43 |
| D15 | INTRQ1* | 19 | 44 | |
| nc | A5 | 20 | | 45 |
| nc | nc | 21 | 46 | |
| nc | nc | 22 | | 47 |
| nc | ACK* | 23 | 48 | |
| +5V | nc | 24 | | 49 |
| GND | GND | 25 | 50 | |

**Figure 5 IP Logic Interface Pin Assignment**



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# Construction and Reliability

IndustryPack®s were conceived and engineered for rugged industrial environments. The IP-488 is constructed out of 0.062 inch thick FR4 material. The four copper layers consist of two signal layers on the top and bottom, and two internal layers for power distribution.

All components on the IP are surface mount components, except for the two 50 pin connectors and the two test points which are through hole. Surface mounting of components allows for high reliability and low cost.

The IndustryPack® connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack® provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.



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# Repair

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the factory for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS will not be responsible for damages due to improper packaging of returned items.



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# Specifications

| | |
|---|---|
| **Quadrature Decoder/Counter**: | Six HCTL-2020 ICs |
| **No. of Channels**: | 6 |
| **Encoder Inputs:** | differential: RS-422A, RS-423-A |
| **Index Capture Inputs**: | differential: RS-422A, RS-423-A |
| **Input Common Mode Voltage**: | ± 15V |
| **Input Differential Voltage**: | ± 25V |
| **Differential Input Threshold**: | Low: -0.2V<br>High: 0.2V |
| **Maximum Input Current**: | Low(0.5V): -100uA<br>High(5.25V): 40uA |
| **Input Impedance**: | 240 ohms |
| **Maximum Encoder Tracking Frequency**: | 1.3 MHz |
| **Maximum Encoder Counts**: | ± 32768 without interrupt,<br>± infinity with interrupts on overflow to virtual counter |
| **Data Transfer Modes**: | 16-bit I/O read/write accesses. |
| **Interrupts**: | INTRQ0 for overflow of one or more channels.<br>INTRQ1 for index input capture for one or more channels |
| **I/O Access Wait States**: | One |
| **Dimensions:** | 1.8 x 3.9 x 0.340 inches |
| **Power requirements**: | 200 mA @ 5V typ. no load |
| **Environmental**: | Operating Temperature:<br>0 to +70°C<br>Humidity:<br>5 to 95% non-condensing |



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