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PMC1553E Product Manual

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1 - Introduction

Radstone's PMC1553E forms part of an expansion board range complementing Radstone's latest generation of PMC-compatible, PowerPC-based single board computers, allowing dual 1553 functionality in a single VMEbus slot.

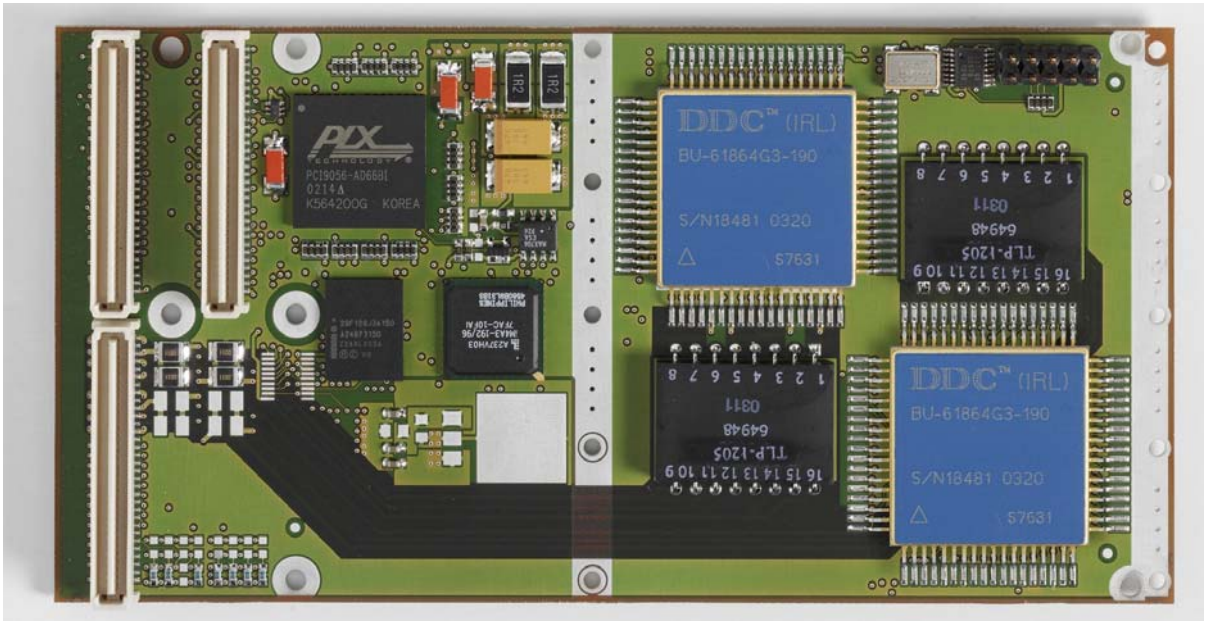
The PMC1553E provides up to two dual-redundant MIL-STD-1553B interfaces on a single PMC running at 66 MHz. Features such as hardware BC triggers and RT status lines allow the PMC1553E to control 1553 terminals. The PMC1553 also features an 8-bit TTL parallel I/O port.

Based on DDC Enhanced Mini-ACE devices, the PMC1553E meets the requirements of 1553A, 1553B Notice 2 and STANAG 3838. Bus Controller, Remote Terminal and Monitor Terminal modes are independently supported on each channel.

Available in a compatible range of increasingly more rugged build standards, the PMC1553E range provides the optimum solution for 1553 terminals at all levels of cost and ruggedization. In its air-cooled build levels, the PMC1553E conforms to the IEEE P1386.1 PMC standard, and in the conduction cooled build levels, it conforms to the ANSI/VITA 20-2001 Standard for Conduction Cooled PMCs.

The PMC1553E's form factor uses only one PMC slot on the host and can easily be plugged onto any host processor (VME or otherwise) that supports PMC and has appropriate drivers, for example, one of Radstone's PowerX family.

Figure 1-1. PMC1553E



Software Support

To simplify system integration of the PMC1553E, Radstone can also supply its comprehensive 1553 Library, which provides full support for all 1553 modes. Although the library only directly supports VxWorks, other operating systems such as Ada are easily supported via the 'C' source code package.

BIT compatible firmware is included with the PMC1553E. This provides power-up or primary diagnostics, and supports interactive operation.

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Objectives of this Manual

- To guide the reader through configuration, installation and power-up
- To provide the user with sufficient information to understand the operation of the PMC1553E hardware

Note: Software support (e.g. drivers, libraries etc.) is described in separate manuals.

Documentation Audience

This manual is written to cover, as far as possible, the range of people who will handle or use the PMC1553E including (but not limited to):

- Inspectors
- Installation technicians
- Hardware and software engineers
- System managers

While every effort has been made to keep the description of configuration, installation and power-up as simple and user-friendly as possible, a certain amount of background knowledge on these subjects is assumed.

In the Functional Description section, a higher degree of background knowledge is assumed on subjects including:

- Computer architecture
- Interfaces
- Peripherals
- PCI
- MIL-STD-1553B

There is a glossary provided at the back of this manual that explains some of the terms used and expands abbreviations.

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Scope of this Manual

This manual describes:

- All build standards of the PMC1553E
- All variants of the PMC1553E

This manual mentions, but does not describe in detail:

- The PMC host processor
- Carrier cards
- PMC1553E on-board firmware
- Software support (drivers etc.)
- Application software

Radstone's 1553 library is described in a separate manual as it is a generic product used across Radstone's range of MIL-STD-1553 cards. An overview of the library is given in Section 4.

Structure of this Manual

This manual is structured in a way that will reflect the sequence of operations from receipt of the PMC1553E up to getting it working with your host processor. Each topic is covered in a separate section, and each section begins with a brief introduction that tells you what the section contains. In this way, you can skip any sections that are not applicable, or with which you are already familiar.

The sections are:

Section 1 (this section) - gives a brief introduction, this manual's objectives, audience, scope, structure and conventions, safety notices, associated documentation and related web sites.

Section 2 - contains inspection instructions and describes product identification.

Section 3 - describes configuring the PMC1553E and fitting it to a PMC host

Section 4 - describes power-up and subsequent operation, including an overview of Radstone's 1553 interface library.

Section 5 - is a functional description.

Section 6 - describes the PMC1553E's connectors and signals used.

Section 7 - outlines how to obtain technical assistance.

Appendix A - is a board specification.

There are also a glossary and an index provided.

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Safety Notices

Safety Summary

Observe the following general safety precautions during operation of this equipment. Failure to comply with these precautions or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Radstone Limited trading as Radstone Technology assumes no liability for the user's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Radstone is aware. Take note of these warnings and take all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Equipment

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components

All Radstone circuit boards are manufactured by UL-recognized manufacturers and have a flammability rating of 94V-0.

CAUTION

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic inteference (EMI) if not installed and used in a cabinet with adequate EMI protection.

Only use the PMC1553E in PMC sites that supply power on both the P11 and P12 connectors

Radstone boards are designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

Radstone boards also comply with EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

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Conventions Used in this Manual

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'B' subscript. The prefix 0x shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_B

The multipliers 'M' and 'k' have their conventional scientific and engineering meanings of $*10^6$ and $*10^3$ respectively. The only exception to this is in the description of the size of memory areas, when 'M' and 'K' mean $*2^{20}$ and $*2^{10}$.

Note: When describing transfer rates, 'k' and 'M' mean $*10^3$ and $*10^6$, *not* $*2^{10}$ and $*2^{20}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follows the more familiar convention that bit 0 is the LSB and bit n is the MSB.

All data alignment in this manual refers to the PCI bus. How data appears to the processor depends entirely on the configuration of the host card and whether it is big- or little-endian.

Signal names ending with a tilde (~) denote active low signals; all other signals are active high.

This manual uses the following types of notice:

1) Notes call attention to important features or instructions, and are shown as follows:

Note: This is an example note entry.

2) Cautions call attention to actions that may cause system damage or loss of data, and are shown as follows:

CAUTION
This is an example caution entry.

3) Warnings call attention to actions that may cause risk of personal injury, and are shown as follows:

WARNING
This is an example warning entry.

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Related Documents

IEEE P1386 Draft Standard for a Common Mezzanine Card Family.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards.

ANSI/VITA 20-2001 Standard for Conduction Cooled PMCs.

Enhanced Miniature Advanced Communications Engine (ACE) Users Guide, MN-6186X-001.

PCI 9056 Data Book, PLX Technology 9056-SIL-DB-P1-091b.

IEEE 1149.1 Test Access Port and Boundary Scan Architecture.

MIL-STD-1553B.

Radstone PMC Installation Note, publication number HN4/3-99.

Radstone 1553 Library Manual, publication number RT5083.

Radstone 1553E BIT Release Notes, publication number 1553E-BIT-xHR.

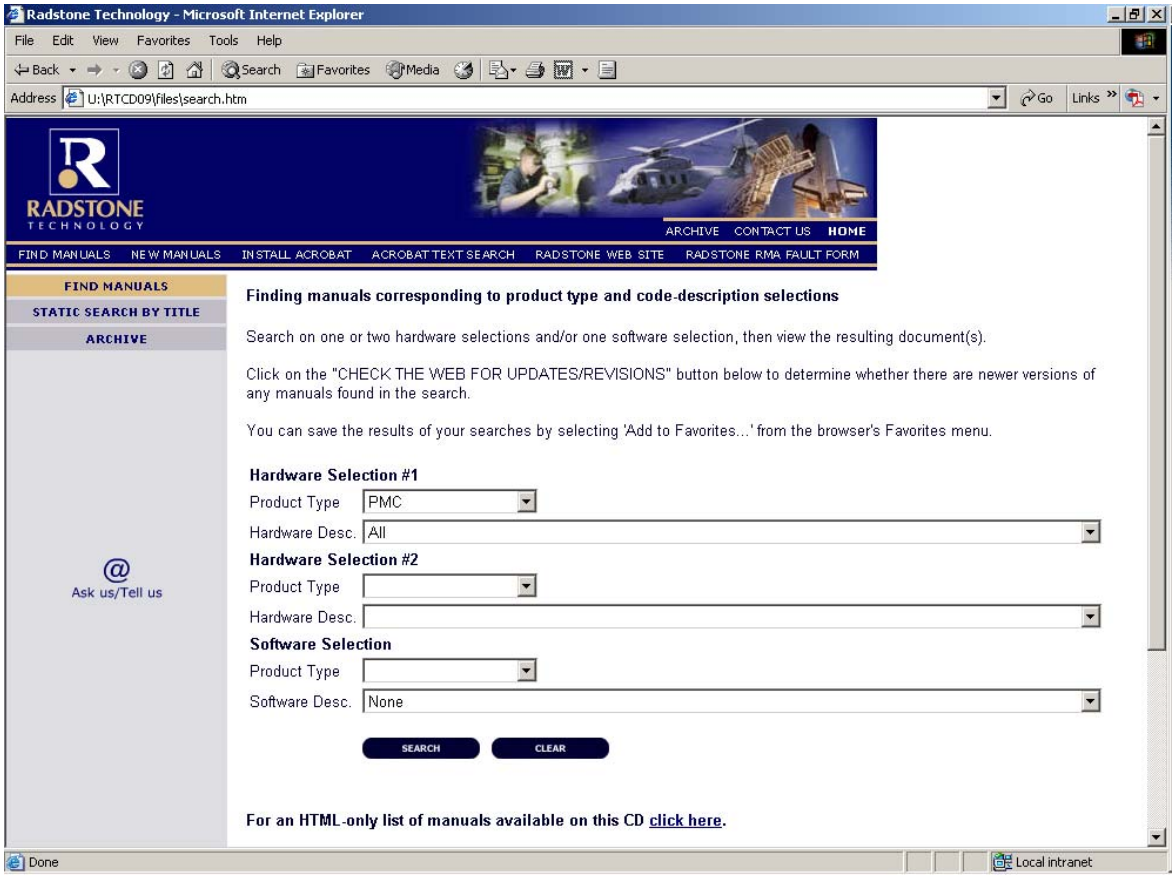
BIT on Radstone PPCx User Guide, publication number RT5107.

PMC1553 Coupler Box Manual, publication number 1553CPL-0HH.

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World Wide Web Sites

The Radstone Product Manuals CD-ROM allows privileged access to an Internet resource containing the latest updated documents. With the CD-ROM installed onto an Internet-connected compatible computer system, the following dialog box becomes available when the ‘FIND MANUALS’ button is clicked:



Other Radstone information is available at http://www.radstone.co.uk or http://www.radstone.com.

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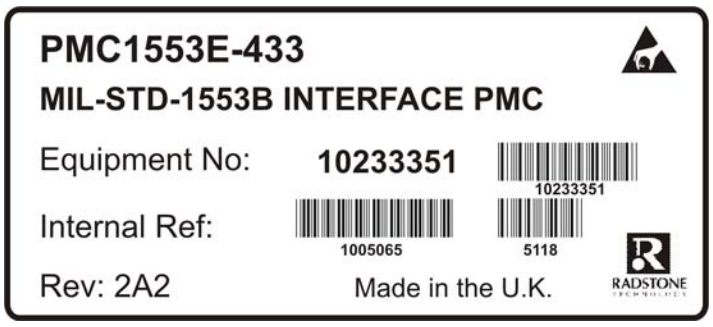
2 - Inspection

This section gives guidelines on inspecting the PMC1553E.

Product Identification

Radstone boards are identified by labels at strategic positions. You can cross-check these against the Advice Note provided as a separate note with your delivery.

On the outside of the shipping box, and the antistatic bag, there is a label similar to the following:



On the board within the antistatic bag, there is an identifying label similar to the following attached to the printed wiring board:

MADE IN UK	PMC1553E-433	REV
Equ No.	10233351	2A2

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Inspection

1) Using Figures 2-1 and 2-2, visually inspect the board for any damage, and loose or dislodged components.



CAUTION

Only handle the board by the edges or front panel

2) Report to Radstone any defects you detect.

3) There are no user-configurable link options on the PMC1553E.

Figure 2-1. Top Component Layout

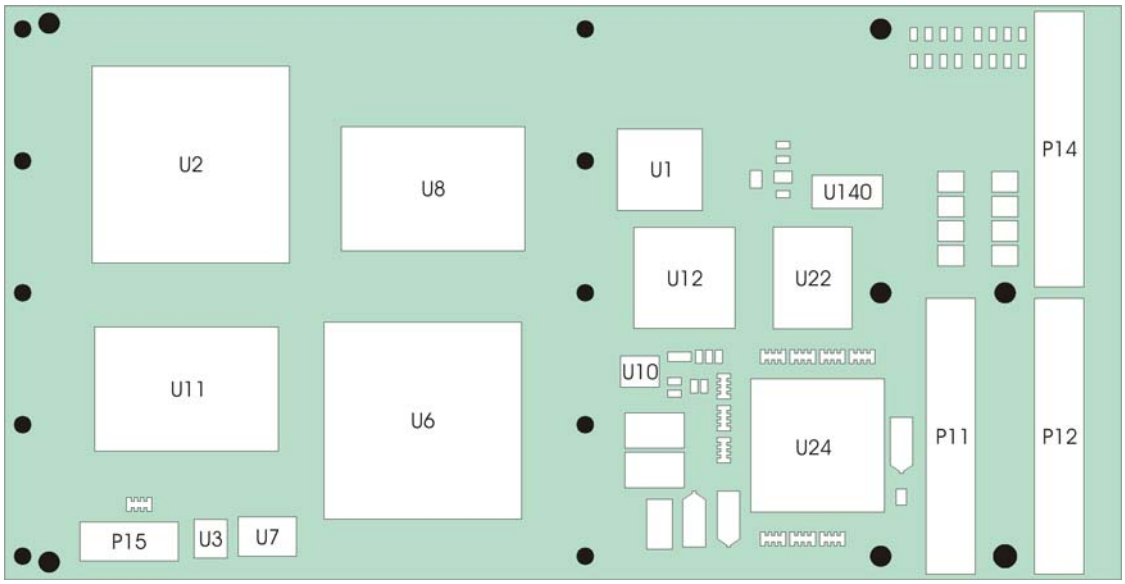
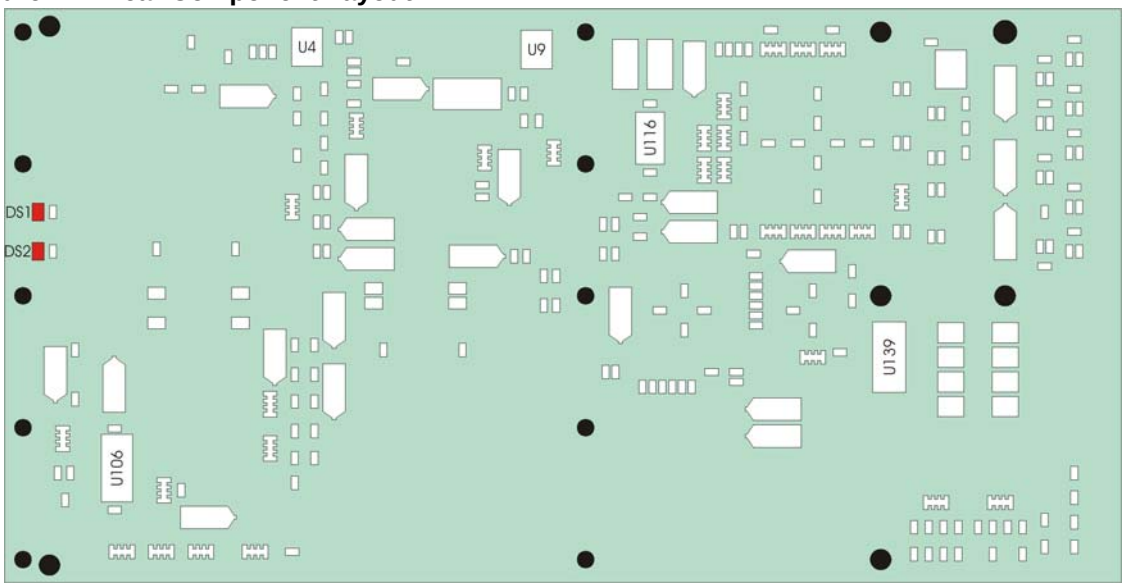


Figure 2-2. Rear Component Layout



Note: The above diagrams show the component placements for a dual-channel PMC1553E. For single channel versions, not all components shown are fitted.

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3 - Configuration and Installation

This section describes configuration of the PMC1553E and connection to an air- or conduction-cooled PMC host, e.g. one of Radstone's PowerX family of PowerPC-based Single Board Computers.



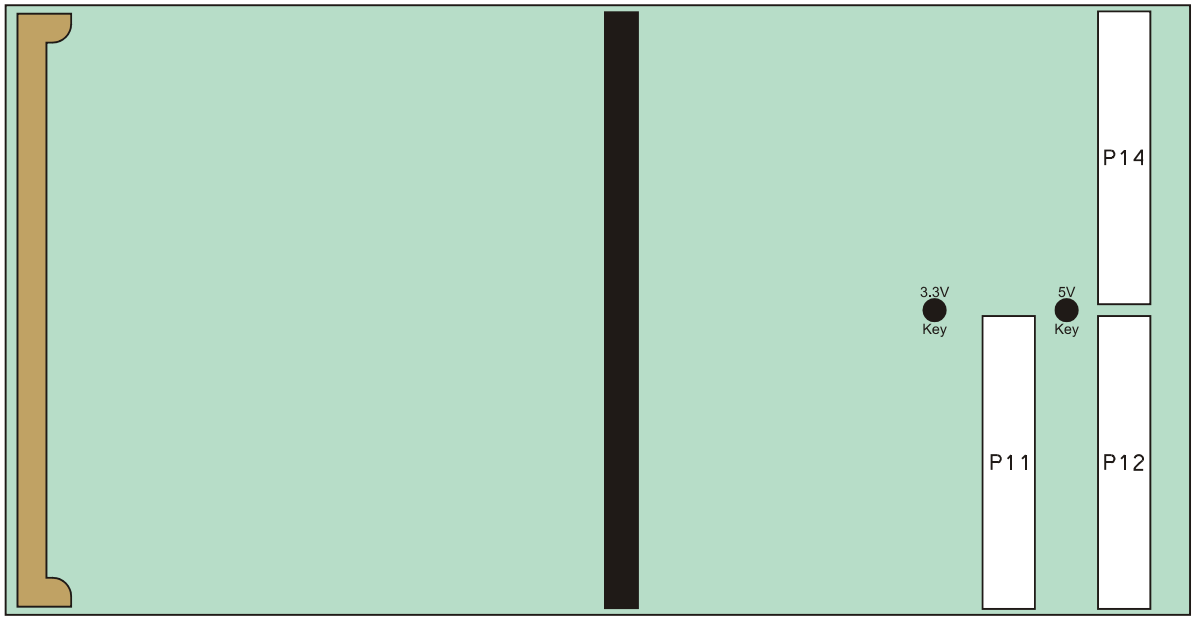


Configuration

There are no user configurable links on the PMC1553E. All configuration is defined by software or linking at the I/O interface. For special customer configuration-controlled variants, a predefined RT address can be incorporated during manufacture.

Installation

The PMC1553E conforms to the size/power requirements of a single PMC. It is designed to fit to any host card that is keyed to accept +5V or +3.3V PMC modules.



The PMC1553E is supplied with a full kit of parts for mounting it and fitting instructions. The installation of driver software or other firmware configuration may be required to achieve full functionality of a PMC module. PMC modules ordered with a Radstone host card can be supplied factory-fitted. Consult your Sales person for information.

To achieve compliance with the Rugged CMC specification, additional metalwork is required. This only affects level 3 product, where a half-height centre stiffening bar is supplied and, if ordered with a Radstone host card, is fitted at the factory. This bar interfaces between the PMC1553E and the metalwork on a host card. For level 1 and 2 PMC1553Es, the use of a half-height centre stiffening bar is not required. For level 4, the host card metalwork should be designed to accept rugged PMCs without the need for additional metalwork.

The PMC Installation application note, HN4/2-99, describes the fitting of any level to PMC to any level of host, including non-Radstone hosts.

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RT Address Selection

The RT address of each channel can be independently selected via hardware or software. Hard wiring at the I/O interface disables software programming of RT addresses. Section 5 describes software programming of RT addresses. Hardware configuration of RT addresses is described below. See Section 6 for connector pinouts.

CH0RTAD0 to CH0RTAD4/CH1RTAD0 to CH1RTAD4

These are the Channel 0/1 RT Address bits 0 to 4. They are used to set the address of an RT and are only valid in RT mode. Link the signal to 0V for a 0 bit or leave it open for a 1 bit. For example, for address 0xA, link CH0/1RTAD4, CH0/1RTAD2 and CH0/1RTAD0 to 0V. To enable software RT address selection, leave these signals and the CH0/1RTADPTY signal open.

CH0RTADPTY/CH1RTADPTY

This is the Channel 0/1 RT Address Parity and is only valid in RT mode. It must provide the odd parity sum with CH0/1RTAD0 to CH0/1RTAD4. Link the signal to 0V for a 0 bit or leave it open for a 1 bit. For example, for address 0xA (10_D), leave CH0/1RTADPTY open. To enable software RT address selection, leave this and the CH0/1RTAD0 to CH0/1RTAD4 signals open.

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4 - Power-up & Operational Description

This section describes power-up and subsequent operation of the PMC1553E.

Power-up

Having attached the PMC1553E to the PMC host, as described in Section 3, you can proceed with installing and powering it up as described in the relevant PMC host's Manual.

Initialisation and Self Test

As explained in the relevant PMC host's manual, on start-up, the host runs through a self-test diagnostic package called BIT that initialises all the on-board resources into their default conditions and interrogates them. PMC1553E's inclusion in these tests is described below.

Configuring the PPC Host

The board hosting the PMC1553E needs to be correctly configured to recognise the PMC if the BIT code is to run successfully. The BIT code is held in on-board FLASH. If this becomes corrupted in any way or needs to be upgraded, it can be reprogrammed from within VxWorks or LynxOS. See the 1553E BIT Release Notes, publication number 1553E-BIT-xHR, for more details.

To configure the PMC host to recognise the PMC1553E board:

1) Press any key on the terminal keyboard to stop the PMC host booting into VxWorks/LynxOS.

2) Select Option 1 to enter the SDE environment.

3) PMC1553E BIT is invoked by the PMC host processor by including a suitable entry in the System Description Table. From the BIT Options menu, select **System Description** and add a new entry as follows. Type:

```
> create 1↵
> mod n ciin=r1553e, routine=00080000, method=pmc_test, bus=B0S6↵
> mod n address=001411b5, length=8000, am=pmc ↵
> save↵
```

(where n is the number of the SDE entry created by the initial '`create`')

This results in the following output:

```
SDE CIIN   ROUTINE  ADDRESS  BUS    AM    METHOD      LENGTH   GRAN SKP TESTMASK
--- ----   -------  -------  ---    --    ------      ------   ---- --- --------
...
00n r1553e 00080000 001411b5 B0S6   PMC   PMC_TEST    00008000 0000 NO  00000000
```

Note: This example entry is for a PPC4 with a single PMC1553E fitted directly in slot 2. For other PowerX boards or where a carrier card is used, the bus and slot of the PMC need to be modified in the '`bus=`' entry. See the BIT on Radstone PPCx User Guide, publication number RT5107 for more details.

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Running BIT

Use BIT's Comprehensive level to verify the PMC1553E functionality. BIT is run as follows:

1) Press any key on the terminal keyboard to stop the PMC host booting into VxWorks.

2) Select Option 6 to enter the interactive BIT environment.

3) Type '**`mo 1f`**↵' for single shot mode (1 cycle through the tests) or '**`mo 2f`**↵' for continuous mode (continuous cycling through the tests).

4) Type '**`run`**↵' to start the tests.

The PMC1553E BIT tests, fail codes and fail data are described in the 1553E BIT Release Notes, publication number 1553E-BIT-xHR.

Operational Description

1553 Interface Library

This section gives an overview of Radstone's 1553 interface library.

Library Philosophy

Radstone's 1553 interface library works across Radstone's entire MIL-STD-1553 product range. The library provides a high-level interface that hides the handling of the specific card and maximises portability between products.

The library consists of several logical groups of functions:

- Those that handle the three modes - Bus Controller (BC), Remote Terminal (RT) and Monitor (PBM/MT) - of a MIL-STD-1553 channel. Only one of these three modes can be selected at a time
- The non-mode specific administration functions. These allow an application program to nominate the card, channel and channel mode. For each card, there is also a set of space allocation functions equivalent to the standard 'C' functions
- The interrupt handling functions, which work within the specific mode of a channel. These allow for the appropriate real-time response to particular events generated by the card

The library is fully described in the 1553 Library Manual, publication number RT5083.

Overview

The 1553 interface library provides a range of functions that the application code can use to control the operation of a PMC1553E card plugged onto a Radstone PowerPC-based host processor. The package runs under the VxWorks real time kernel.

Each library function provides detailed error reporting to assist in debugging of the code.

Usage

The library functions are used by including calls to them within application code. A series of ANSI C header files are supplied to provide the required definitions and function prototypes. Finally, the executable library files are combined with the application at the time of linking code modules into the executable image.

During the execution of library routines, certain data structures are set up and maintained with the card's status. To ensure integrity of this data, control of a PMC1553E card should be either entirely with, or entirely without, the library functions.

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Library Structure

The executable library routines are provided as one function per object module, enabling linkers to load only referenced functions. The object modules are collected within a library file, which should be passed to the linker being used as specified in the documentation related to the tool. The file format supplied is object modules in a GNU ar format library (e.g. PMC1553e.vx.a)

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5 - Functional Description

This section gives a functional description of the PMC1553E.

The PMC1553E board provides up to two dual redundant MIL-STD-1553A/B interfaces using the fully integrated BC/RT/MT BU61864G3-190 Enhanced Mini-ACE device with integral 64K words of RAM.

The RT address of each channel can be independently set either by hardwired linking on the I/O connector or by software programming. Hard wiring overrides software programming.

The PMC1553E also provides an 8-bit TTL parallel I/O port.

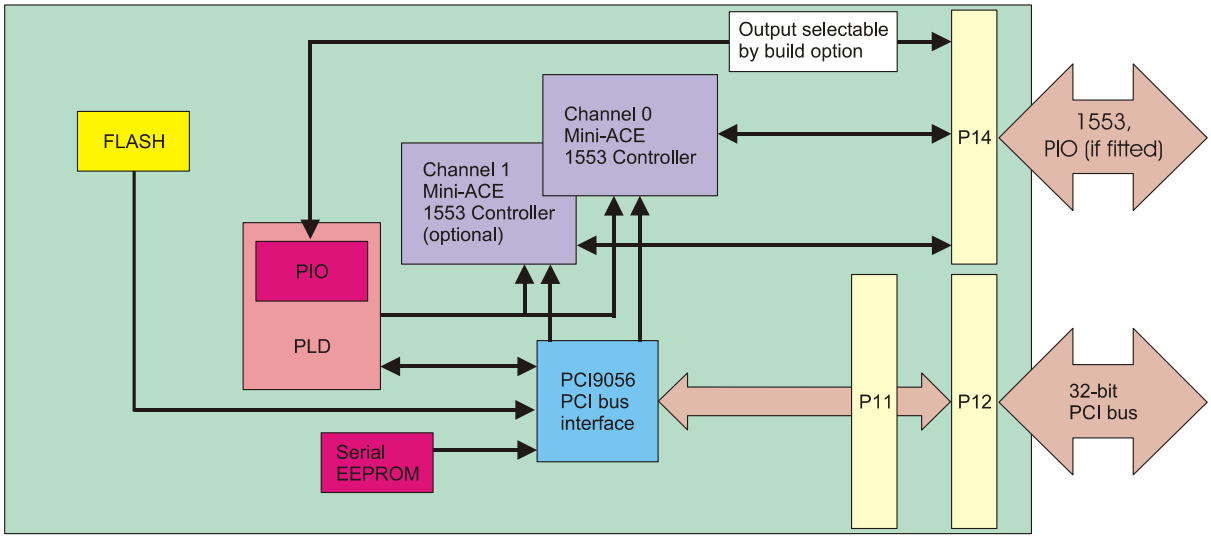
To provide full testability, the PMC1553E includes an IEEE 1149.1 JTAG port, and is delivered as standard with BIT. Compatible with the IEEE 1149.5 Module Test Maintenance bus, JTAG allows host device-independent testing of PMC1553E. BIT provides diagnostics to give confidence in the sub-system integrity at power-up, and the ability to interrogate the board from the host.

Features

- Two dual redundant MIL-STD-1553B bus interfaces (single interface option available)
- 1553A, 1553B Notice 2 and STANAG 3838 support
- 66 MHz PCI operation
- RT/BC/MT modes
- 64K words of SRAM per channel
- Transformer coupled or direct interfaces
- External BC trigger/RT status
- 8-bit TTL compatible parallel I/O port
- JTAG port
- BIT
- 1553B library with RT/BC/MT support
- Available in 5 build grades, from Standard to Rugged Conduction Cooled
- Hard-wired or software selectable RT addresses
- 16 Mbytes of Intel Strata FLASH memory

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Figure 5-1. PMC1553E Block Diagram



BC/RT/MT Operation

BU61864G3-190 devices provide full support for all modes of operation. Each channel includes 64K words of memory for configuration and data buffers.

BC mode includes advanced features such as automatic retries, programmable gap times and frame auto-repeat.

RT mode supports three message buffering schemes for optimum performance and includes programmable command illegalization and Busy.

MT mode allows word monitoring, selective message monitoring or simultaneous RT/monitor modes. This last mode is sometimes required for backup BC terminals.

Fully independent operation allows any combination of BC, RT and MT channels.

RT Addressing

The RT address of each channel on the PMC1553E may be set by software via the PCI interface, or by hard-wiring. Hardware setting of the address disables software setting.

BC Trigger/RT Status

An external trigger line is provided for each channel to allow hardware control of the BC. Messages may be pre-programmed, then sent on the trigger becoming active.

In RT mode, this line becomes a sub-system status line, used to indicate a failure within the sub-system. When active, all 1553 messages are tagged as suspect.

Parallel I/O

The PMC1553E includes an 8-bit TTL-compatible parallel I/O port. For maximum flexibility, each line is independently programmable as an input or output. As inputs, bits can be set to generate an interrupt on change of state.

Note: Due to pinout limitations, parallel I/O is not available from all PMC sites.

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Build Levels

The PMC1553E is available in Radstone's five electrically compatible build levels. These have two basic mechanical configurations:

- Air (convection)-cooled (build levels 1 to 3) in accordance with IEEE P1386 CMC Draft Standard, designed to be used in standard industrial chassis
- Conduction-cooled (build levels 4 and 5) in accordance with VITA 20 - 2001 CCPMC Standard, for use in Radstone or third party ATR-style enclosures

In addition to these COTS configurations, PMC1553E may be supplied to meet the mechanical and thermal requirements of specific platforms with the addition of mission specific, to-type mechanics.

Radstone uses advanced thermal and mechanical design in the PCB, metal work and assembly process to build-in the required levels of ruggedness. Each level is carefully tailored to a particular set of requirements and environments. Build level 2 and higher circuit card assemblies include conformal coating as standard.

All four styles fully support the power and versatility of PCI, so no matter how large or diversified your project, absolute compatibility is assured at all stages of development.

A brief description of each build style follows:

Level 1

Intended for use in benign environments, level 1 also provides the ideal cost effective method of complete system development. The level 1 assembly comprises an IEEE P1386 size assembly printed wiring board with high quality commercial (plastic encapsulated) components. As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to the target style only in the final stages of system integration.

Level 2

As Level 1, but tested in manufacture to provide an extended operating temperature range.

Level 3

Level 3 boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air-cooled, racking systems. These rugged boards comprise an IEEE P1386 size printed wiring board fitted with wide temperature range, industrial grade components.

Level 4

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments, the level 4 board features wide temperature range, industrial grade devices, an integral thermal management layer and incorporates a central stiffening bar for additional strength. Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. Level 4 boards are temperature characterised during manufacture.

Level 5

As Level 4, but tested in manufacture to provide an extended operating temperature range.

See Appendix A for more details of the environmental specifications of each build style.

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PCI Interface

The PMC1553E PCI bus interface is a PLX Technology PCI9056 device, which is PCI Rev 2.2 compliant and is capable of 32-bit operation at up to 66 MHz. On the PMC1553E, the PCI9056 operates in slave mode only.

The PMC1553E responds to the following PCI bus commands:

Memory Read; Memory Write; Configuration Read; Configuration Write; Memory Read Multiple (aliased to Memory Read); Memory Read Line (aliased to Memory Read); Memory Write and Invalidate (aliased to Memory Write)

PCI Configuration Space

Configuration Space provides a set of “hooks” for system configuration mechanisms. Support is provided for device relocation within the Host processor memory map; configuration of interrupt binding; device identification and consequently automatic installation and configuration of software support. The configuration space for the PMC1553E is detailed below. Shaded areas are not used by the PMC1553E and are not described. Registers from offset 0x40 onwards are not used by PMC1553E and are not shown. Default values are shown in brackets.

Address Offset	31 24	23 16	15 8	7 0
0x00	Device ID (0x0014)		Vendor ID (0x11B5)	
0x04	Status (0x02B0)		Command (0x0000)	
0x08	Class Code (0x068000)			Revision ID (0xAA)
0x0C	BIST (0x00)	Header Type (0x00)	PCI Bus Latency Timer (0x00)	Cache Line Size (0x00)
0x10	PCI Base Address 0 (Memory-mapped Configuration Registers) (0x00000000)			
0x14	PCI Base Address 1 (I/O-mapped Configuration Registers) (0x00000001)			
0x18	PCI Base Address 2 (Local Address Space 0) (0x00000000)			
0x1C	PCI Base Address 3 (Local Address Space 1) (0x00000000)			
0x20	PCI Base Address 4 (0x00000000)			
0x24	PCI Base Address 5 (0x00000000)			
0x28	Cardbus CIS Pointer (0x00000000)			
0x2C	Subsystem ID (0x0014)		Subsystem Vendor ID (0x11B5)	
0x30	PCI Base Address for Local Expansion ROM (0x00000000)			
0x34	Reserved (0x000000)			New Capability Pointer (0x40)
0x38	Reserved (0x00000000)			
0x3C	Max_Lat (0x00)	Min_Gnt (0x00)	Interrupt Pin (0x01)	Interrupt Line (0x00)

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On power-up, the PCI Configuration registers shown in the following table are loaded with the default values shown in parentheses in the previous table from a serial E^2PROM.

Some of the Configuration registers are not writeable from PCI. These are also shown in the following table:

Address	Default from E^2PROM	PCI Writeable
00	Yes	No
04	Yes	Yes
08	Yes (Class Code)	No
0C	No	Yes (Cache Line Size)
10	No	Yes
14	No	Yes
18	No	Yes
1C	No	Yes
20	No	Yes
24	No	Yes
28	No	No
2C	Yes	No
30	No	Yes
34	No	No
38	No	No
3C	Yes (Max_Lat, Max_Gnt)	Yes (Interrupt Line)

The registers are described below:

Vendor ID (PCI offset 0x00)

This 16-bit read-only register indicates that the vendor is Radstone Technology. The default value is 0x11B5.

Device ID (PCI offset 0x02)

This 16-bit read-only register indicates that the device is a 1553 module. The default value is 0x0014.

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Command Register (PCI offset 0x04)

This 16-bit read/write register is used to control PCI access to the PMC1553E. After power-up or reset, the default value of 0x0000 denies all PCI access except for configuration accesses.

In the following register layout, bits in parentheses can be written to, and the default value is shown:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	(0)	0	(0)	0	(0)	0	(0)	(0)	(0)

BITS	FUNCTION	READ/WRITE	MEANING
0	I/O Space	Read/Write	1 = PMC1553E can respond to I/O space accesses. 0 = PMC1553E cannot respond to I/O space accesses. ***Clear this bit***
1	Memory Space	Read/Write	0 = PMC1553E cannot respond to memory space accesses. 1 = PMC1553E can respond to memory space accesses. ***This bit must be set to allow access to the board***
2	Master Enable	Read/Write	Not Used. PMC1553E is slave only. ***Clear this bit***
3	Special Cycle	Read only	Not Supported
4	Memory Write/Invalidate	Read/Write	Not Used. ***Clear this bit***
5	VGA Palette Snoop	Read only	Not Supported
6	Parity Error Response	Read/Write	1 = PMC1553E asserts PERR~ on detection of a data parity error. 0 = PMC1553E does not assert PERR~ on detection of a data parity error, and continues normal operation. The Parity Error bit in the Status Register is always set on detection of a data parity error
7	Wait Cycle Control	Read only	Hardwired to 0 (device never does address/data stepping)
8	SERR~ Enable	Read/Write	1 = Enable SERR~ driver 0 = SERR~ driver disabled
9	Fast Back-to-Back	Read only	Hardwired to 0 (fast back-to-back transfers can only occur to the same agent as the previous cycle)
10 to 15	Reserved	Read only	Not Used

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Status Register (PCI offset 0x06)

This 16-bit read/write register holds status information on the PMC1553E. Writing to certain bits resets those bits.

In the following register layout, bits in parentheses can be written to, and the default value is shown:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
(0)	(0)	0	0	(0)	0	1	0	1	0	1	1	0	0	0	0

BITS	FUNCTION	READ/WRITE	MEANING
16 to 19	Reserved	Read only	Not used. These bits read 0
20	New Capability Functions Support	Read only	1 = New Capability Functions Supported
21	66 MHz Capable	Read only	1 = Device supports a 66MHz PCI clock environment
22	User Definable Functions Support	Read only	0 = User definable functions not supported
23	Fast Back-to-Back Capable	Read only	Hardwired to 1 (fast back-to-back cycles supported)
24	Master Data Parity	Read only	Not Used. Reads 0
25 and 26	DEVSEL~ Timing	Read only	Hardwired to 01 (PMC1553E asserts DEVSEL~ 2 clocks after the address phase)
27	Target Abort	Read/Write	0 = Transaction completed successfully. 1 = PMC1553E terminated a transaction with Target-Abort (i.e. a transaction to a non-existent device was attempted). This bit is cleared by writing a 1 to it
28	Received Target Abort	Read only	Not Used. Reads 0
29	Received Master Abort	Read only	Not Used. Reads 0
30	System Error	Read/Write	0 = No system error. 1 = PMC1553E signalled a system error. This bit is cleared by writing a 1 to it
31	Parity Error	Read/Write	0 = No parity error. 1 = PMC1553E detected a parity error (regardless of whether parity is enabled). This bit is cleared by writing a 1 to it

Revision ID (PCI offset 0x08)

This 8-bit read-only register shows the Silicon revision of the PCI 9056 device (0xAA or 0xAD – it may be useful to have this information to hand when contacting Customer Support).

Class Code (PCI offset 0x09)

This 24-bit read-only register is made up as follows:

Base class	Bridge device	0x06
Sub-class	Other bridge device	0x80
Interface	No interfaces defined	0x00

Header Type (PCI offset 0x0E)

This 8-bit read-only register holds a value of 0x00 showing that the PMC1553E is a single PCI function device with Configuration Layout type 0x0.

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PCI Base Address 0 (PCI offset 0x10)

This 32-bit read/write register is used to assign a segment of the PCI address space for memory access to the Local Configuration Registers. During initialisation, the host writes 0xFFFF FFFF to this register and then reads back 0xFFFF FF80, indicating that a space of 128 bytes is required.

In the following register layout, bits in parentheses can be written to, and the default value is shown:

31 ... 8	7	6	5	4	3	2	1	0
(0x000000)	0	0	0	0	0	0	0	0

Bits	Function	Read/Write	Meaning
0	Memory Space	Read only	Hardwired to 0 (register maps into PCI memory space)
1 and 2	Location	Read only	Hardwired to 00 (register may be located anywhere in 32 -bit memory address space)
3	Prefetchable	Read only	Hardwired to 0 (prefetching not supported)
4 to 7	Base Address	Read only	Hardwired to 0x0
7 to 31	Base Address	Read/Write	These bits of the Base Address may be written with any chosen value

PCI Base Address 1 (PCI offset 0x14)

By default, this 32-bit read/write register is disabled by bits 12 and 13 of the Local Control register. In the following register layout, bits in parentheses can be written to, and the default value is shown:

31 ... 7	6	5	4	3	2	1	0
(0x0000000)	0	0	0	0	0	0	1

Bits	Function	Read/Write	Meaning
0	I/O Space	Read only	This bit is fixed as 1 (register maps to I/O space)
1	Reserved	Read only	This bit always reads 0
2 to 6	Base Address	Read only	These bits of the Base Address are fixed as 00000_b
7 to 31	Base Address	Read/Write	These bits of the Base Address may be written with any chosen value

PCI Base Address 2 (PCI offset 0x18)

This 32-bit read/write register defines all memory accesses to the PMC1553E. In the following register layout, bits in parentheses can be written to, and the default value is shown:

31 ... 4	3	2	1	0
(0x0000000)	0	0	0	0

Bits	Function	Read/Write	Meaning
0	Memory Space	Read only	0 = Register maps to Memory Space
1 and 2	Location	Read only	00 = Register is located anywhere in 32-bit memory address space
3	Prefetchable	Read only	0 = Prefetching is not supported
4 to 31	Memory Base Address	Read/Write	These bits may be written with any chosen value

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PCI Base Address 3 (PCI offset 0x1C)

This 32-bit read/write register is used for access to Board Support registers, including PIO. In the following register layout, bits in parentheses can be written to, and the default value is shown:

31 … 4	3	2	1	0
(0x0000000)	0	0	0	0

Bits	Function	Read/Write	Meaning
0	Memory Space	Read only	0 = Register maps to Memory Space
1 and 2	Location	Read only	00 = Register is located anywhere in 32-bit memory address space
3	Prefetchable	Read only	0 = Prefetching is not supported
4 to 31	Memory Base Address	Read/Write	These bits may be written with any chosen value

Subsystem Vendor ID (PCI offset 0x2C)

This 16-bit read-only register holds the value 0x11B5 indicating Radstone Technology.

Subsystem ID (PCI offset 0x2E)

This 16-bit read-only register holds the value 0x0014, indicating a MIL-STD-1553B device.

PCI Base Address for Local Expansion ROM (PCI offset 0x30)

This 32-bit read/write register is used for access to FLASH. In the following register layout, bits in parentheses can be written to, and the default value is shown:

31 … 11	10 … 1	0
(0x000000)	0x000	0

Bits	Function	Read/Write	Meaning
0	Decode Enable	Read/Write	1 = Access enabled
1 to 10	-	Read only	Not used
11 to 31	Memory Base Address	Read/Write	These bits may be written with any chosen value

Interrupt Line (PCI offset 0x3C)

This 8-bit read/write register indicates the input of the system interrupt controller to which the PMC1553E's interrupt pin is connected.

Interrupt Pin (PCI offset 0x3D)

This 8-bit read-only register reads 0x01 to indicate that the PMC1553E interrupt uses INTA~.

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Local Configuration Registers

The PCI Base Address 0 (offset 0x10 of the PCI Configuration Registers) defines the base address of the Local Configuration Registers. These registers are used, among other things, to specify the ranges and re-mapping of Local Address Spaces, local bus width etc.

These registers are resident in the PCI9056 and are set to the default values shown in brackets by the serial E^2PROM on power-up or reset. For normal operation of the PMC1553E, you should not need to change them from their defaults.

If you do need to change any value from the default, see the PCI9056 Data Book, available at http://www.plxtech.com/products/9056/default.htm (you may need to register with PLX to access the data book.).

Address Offset	31 … 24	23 … 16	15 … 8	7 … 0
0x00	Local Address Space 0 Range (0xFFC0 0000)			
0x04	Local Address Space 0 Re-map (0x0000 0001)			
0x08	Mode/DMA Arbitration (0x0120 0000 – delayed read))			
0x0C	Local Miscellaneous Control 2 (0x00)	Serial EEPROM Write-protect Address Boundary (0x30)	Local Miscellaneous Control 1 (0x01)	Big/Little Endian Descriptor (0x00)
0x10	Local Expansion ROM Range (0xFC00 0000)			
0x14	Local Expansion ROM Re-map + BREQ Control (0xC000 0000)			
0x18	Local Bus Region Descriptors (Space 0 & Expansion ROM) (0x4041 0041)			
0x1C	Range for Master Access to PCI (not used)			
0x20	Local Base Address for Master Access to PCI Memory (not used)			
0x24	Local Base Address for Master Access to PCI I/O Configuration (not used)			
0x28	Re-map for Master Access to PCI (not used)			
0x2C	Configuration Address Register for Direct Master Access to PCI (not used)			
::				
0xF0	Local Address Space 1 Range (0xFFC0 0000)			
0xF4	Local Address Space 1 Re-map (0x8000 0001)			
0xF8	Local Bus Region Descriptors (Space 1) (0x0000 0040)			
0xFC	PCI Base Dual Address Cycle (Re-map) for Direct Master Access to PCI (not used)			
0x100	Reserved			PCI Arbiter Control (not used)
0x104	PCI Abort Address (not used)			

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Host Interface

Address Map

The PMC1553E address map is configurable via the PCI9056 registers. From PCI, the following address regions are accessible to the user:

Resource	Local Address Space	PCI Base Address (hex)	Organisation
Enhanced Mini-ACE0 SRAM	0	xx00 0000	64K x 16
Enhanced Mini-ACE0 Registers	0	xx10 0000	32K x 16 (plus 32 test registers)
Enhanced Mini-ACE1 SRAM	0	xx20 0000	64K x 16
Enhanced Mini-ACE1 Registers	0	xx30 0000	32K x 16 (plus 32 test registers)
Board Support Registers	1	xxxx xx00	11 x 32
FLASH Memory	Expansion ROM	xx00 0000	8M x 16

Access to the PMC1553E first requires the PCI Base Address registers to be set up as follows:

- PCI Base Address 2 (PCI Configuration Space offset 0x18) with the PCI address of Local Address Space 0
- PCI Base Address 3 (PCI Configuration Space offset 0x1C) with the PCI address of Local Address Space 1
- PCI Base Address for Local Expansion ROM (PCI Configuration Space offset 0x30) with the PCI address of Local Expansion ROM

The PCI Base Address registers are system dependent and cannot be written by the serial E^2PROM.

The PCI9056 Range and Re-map Local Configuration registers should then be set-up. These can be and are loaded from the serial E^2PROM on power-up (along with other registers). The default values are shown in parentheses in the Local Configuration Registers section.

The Local Address Space 0, Local Address Space 1 and Expansion ROM Range registers (offsets 0x00, 0xF0 and 0x10 respectively) should have a 1 written to each bit that is used for address decoding, with bits 31 to 4 of the Range register corresponding to bits 31 to 4 of the address (the least significant 4 bits of the Range register have a different use – see the PLX PCI9056 manual for a complete description).

The Local Address Space 0, Local Address Space 1 and Expansion ROM Range Re-map Registers (offsets 0x04, 0xF4 and 0x14 respectively) re-map the PCI addresses used to access these regions to the addresses used locally on the PMC1553E. This must comply with the Local Address Map. As shown below, Local Address bits 30 and 31 are used to define access to the ACE device(s), Board Support Registers and FLASH Memory, and Local Address bits 20 and 21 define access to ACE0/1 RAM/Registers:

Bit 31	Bit 30	Area		
1	1	FLASH Memory		
1	0	Board Support Registers and PIO Interface		
0	1	Not used		
0	0	ACE 0, ACE 1		
		Bit 21	Bit 20	Area
		1	1	ACE 1 Registers
		1	0	ACE 1 SRAM
		0	1	ACE 0 Registers
		0	0	ACE 0 SRAM

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Enhanced Mini-ACE

Both Enhanced Mini-ACEs are accessed via Local Address Space 0 as adjacent 16-bit half-words. The address is re-mapped so that the two most significant bits of Local Address are 00_B

The Enhanced Mini-ACE SRAM is organised as 64K x 16-bit half-words. The Enhanced Mini-ACE has 32 registers (some of which are test registers), and these are also 16-bit half-words. To maximise use of PCI bandwidth, data to/from the PMC1553E can be packed to use all 32 data bits of the PCI bus. A word access (4 bytes) on PCI results in two 2-byte accesses to the ACE. Byte ordering is big-endian by default so that the most significant half-word appears on word boundaries.

The Enhanced Mini-ACE is clocked at 20 MHz. This information is required for programming the Clock Frequency Selection bits of Configuration Registers 5 and 6.

Please refer to the Enhanced Mini-ACE User Guide for further information. This is available at http://www.ddc-web.com/products/Components/1553.asp.

RT Address Selection

RT Address selection is made either by hard-wiring the 5 address and 1 parity bits (RTAD0 to RTAD5 and RTADP) or by set-up of ACE registers.

The hardwired addresses are available on connector P14. If any one or more of these address lines is pulled low, the RT_AD_LAT signal to the ACE is held low and this forces the RT Address to follow the hard-wired inputs. If all hard-wired addresses are high (or open-circuit), then the RT_AD_LAT signal to the ACE is forced high and the RT Address is latched either from local data bits, LD0 to LD5 or from RTAD0 to RTAD5 and RTADPTY. Latching occurs on a write access to the ACE Config Register #5.

RT_AD_LAT (= 0 IF ANY HARD-WIRED ADDRESS IS PULLED LOW)	ACE CONFIG REG #5 BIT 3	ACE CONFIG REG #6 BIT 5	ACE CONFIG REG #3 BIT 15 (ENHANCED MODE)	RT ADDRESS SOURCE	MODE
0	X	X	X	Hard-wired address RTAD0-5, RTADPTY	Transparent
1	0	X	X	No effect	
1	1	0	X	Hard-wired address RTAD0-5, RTADPTYT	Latched
1	1	1	X	Local data LD0 to LD5	Latched

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Board Support Registers and PIO Interface

These registers are accessed via Local Address Space 1 as 32-bit words on word boundaries, where only the least significant byte is valid. All these registers are implemented in the Lattice M4A3 Programmable Logic Device. The address is re-mapped so that the two most significant bits of Local Address are 10_B

Board Support Registers

Address Offset	Name	Read/Write	Default
0x00	Board Rev/Code Rev	Read only	XX
0x04	Build Option	Read only	XX
0x08	Interrupt Status	Read only	XX
0x0C	Interrupt Mask	Read/Write	0x00
0x10	PIO Data	Read/Write	XX
0x14	PIO Direction	Read/Write	0x00
0x18	PIO Interrupt Status	Read/Write	0x00
0x1C	PIO Interrupt Mask	Read/Write	0x00
0x20	Control	Read/Write	0x04
0x24	ACE Inhibit Bus A	Read/Write	0x00
0x28	ACE Inhibit Bus B	Read/Write	0x00

Board Revision/Code Revision

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Board Revision				Code Revision			

The Board Revision is the hardware revision of the board. The Code Revision is incremented for every hardware change that has a major impact on software. Board Revision and Code Revision are independent.

Build Option

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	1 = ACE 1 fitted	1 = ACE 0 fitted	-

ACE 0 is always fitted; ACE 1 is a build option.

Interrupt Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	1 = ACE 1 interrupt active	1 = ACE 0 interrupt active	1 = PIO interrupt active

A logic 1 indicates an active interrupt. Interrupts are expected to be cleared at the source rather than via this register. The state of this register is not affected by the Interrupt Mask register.

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Interrupt Mask

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	1 = ACE 1 interrupt enabled	1 = ACE 0 interrupt enabled	1 = PIO interrupt enabled

The state of each interrupt mask bit is toggled by writing a 1 to that bit. Writing a 0 leaves the bit unchanged.

PIO Registers

See overleaf.

Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FLASH VPEN	EEPROM PRE✶	-	-	-	1 = LED2 ON	1 = LED1 ON	-

✶Bit 6 only has this function for Board Rev = 0; for subsequent boards, this bit is not used. EEPROM PRE is controlled from the USERo signal of the 9056.

Set bit 1 to logic 1 to illuminate LED DS1. Set bit 2 to logic 1 to illuminate LED DS2.

Set bit 7 to logic 1 to enable FLASH programming.

ACE Inhibit Bus A

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	1 = Inhibit Bus A Ch 1	1 = Inhibit Bus A Ch 0	-

This register is used to shut down activity on one of the 1553 buses in the event of catastrophic failure. Setting the appropriate bit disables the Enhanced Mini-ACE.

ACE Inhibit Bus B

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	-	1 = Inhibit Bus B Ch 1	1 = Inhibit Bus B Ch 0	-

This register is used to shut down activity on one of the 1553 buses in the event of catastrophic failure. Setting the appropriate bit disables the Enhanced Mini-ACE.

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PIO Interface

The PMC1553E supports an 8-bit, TTL-compatible, parallel I/O port. Each of the 8-bits operates independently and may be configured as input or output. The default on power-up or reset is for input. When configured as input, each bit can be set up to generate an interrupt on change of state.

There are four 8-bit registers associated with PIO.

PIO Data

The function of each bit of this register depends on the direction selected by the corresponding bit in the PIO Direction Register. If a PIO Direction Register bit is set for output, the corresponding PIO Data Register bit represents the value to which the output is set. Conversely, if a PIO Direction Register bit is set for input, a read of the PIO Data Register returns the corresponding register bit set to the value of the input.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIO 7	PIO 6	PIO 5	PIO 4	PIO 3	PIO 2	PIO 1	PIO 0

PIO Direction

This register defines each bit as either an input (default) or an output.

1 = Input

0 = Output

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIO Dir 7	PIO Dir 6	PIO Dir 5	PIO Dir 4	PIO Dir 3	PIO Dir 2	PIO Dir 1	PIO Dir 0

Each bit of this register is independent. Any number of bits can be set to either state.

PIO Interrupt Status

When configured as an input, a change of state on the input pin can be made to generate an interrupt, if enabled to do so by the PIO Interrupt Mask Register. This (PIO Interrupt Status Register) can be read to determine which input(s) caused the interrupt.

1 = Interrupt pending

0 = No interrupt

Writing a 1 to the appropriate bit(s) of this register clears the interrupt(s).

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Read	1 = PIO7 Interrupt Pending	1 = PIO6 Interrupt Pending	1 = PIO5 Interrupt Pending	1 = PIO4 Interrupt Pending	1 = PIO3 Interrupt Pending	1 = PIO2 Interrupt Pending	1 = PIO1 Interrupt Pending	1 = PIO0 Interrupt Pending
Write	1 = Clear PIO7 Interrupt	1 = Clear PIO6 Interrupt	1 = Clear PIO5 Interrupt	1 = Clear PIO4 Interrupt	1 = Clear PIO3 Interrupt	1 = Clear PIO2 Interrupt	1 = Clear PIO1 Interrupt	1 = Clear PIO0 Interrupt

Note: It is possible for an input to change more than once before the interrupt is acknowledged.

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PIO Interrupt Mask

When configured as an input, a change of state on the input pin can be made to generate an interrupt. This register allows/disallows interrupts on input pins as required. The default is for interrupts to be disabled.

1 = Interrupt enabled

0 = Interrupt masked

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 = PIO7 interrupt enabled	1 = PIO6 interrupt enabled	1 = PIO5 interrupt enabled	1 = PIO4 interrupt enabled	1 = PIO3 interrupt enabled	1 = PIO2 interrupt enabled	1 = PIO1 interrupt enabled	1 = PIO0 interrupt enabled

Writing a 1 to a bit set up for output has no effect.

Note: To generate an interrupt signal, bit 0 of the Interrupt Mask Register (offset 0x0C) must be set to 1.

FLASH Memory

Intel StrataFlash™ provides 16 Mbytes of non-volatile memory. FLASH is accessed as Expansion ROM space, is 16-bits wide and appears as packed data. Access is enabled for 8- and 16-bit width. The address is re-mapped so that the two most significant bits of Local Address are 11_B.

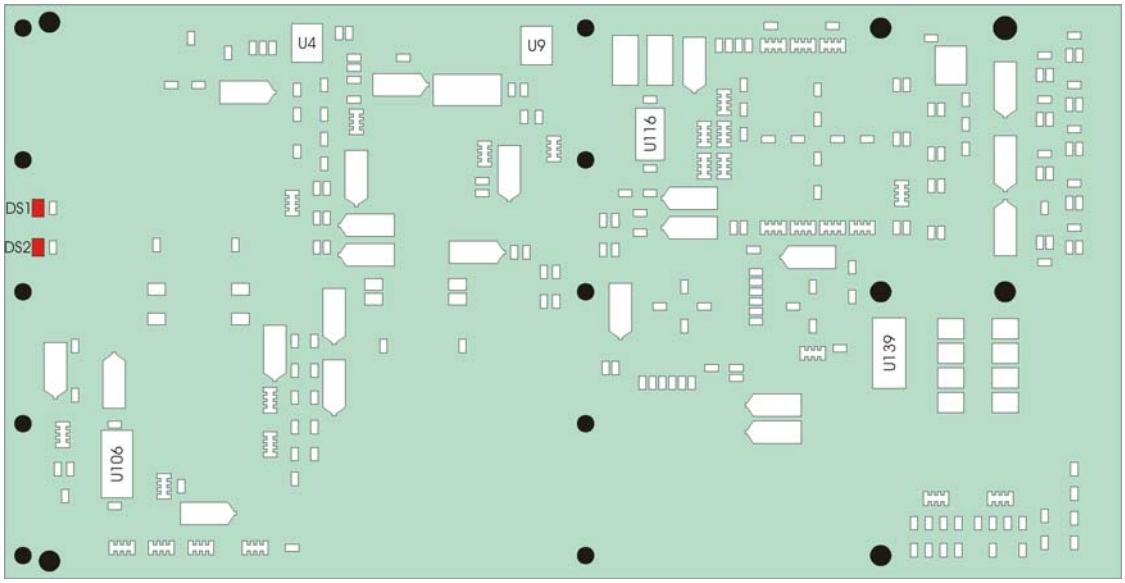
The FLASH memory holds board configuration data and Built-In-Test (BIT) code. BIT code is loaded into system RAM when BIT is run.

Writes to FLASH require assertion of the VPEN signal, bit 7 of the Board Support Control Register.

See http://www.intel.com/design/flcomp/datashts/290667.htm for more details on Intel StrataFlash™.

LEDs

There are two red LEDs on the back of the board, as shown below, visible when the PMC1553E is mounted on a PMC host. The LEDs indicate power-up/BIT status. After initial power-up, DS1 is off and DS2 is on; both LEDs are on while BIT is running and both LEDs go off when BIT is successfully completed. BIT failure results in DS1 on and DS2 off.



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Serial E^{2}PROM

The Serial E^{2}PROM (93CS56, 2Kbit, sequential read) is used to load certain PCI and Local Configuration Registers after power-up or reset. Under normal conditions, it is not necessary to change this set-up. The device has the following hardware protection signals:

PE (Program Enable)	Permanently pulled high, allows all accesses to Serial E^{2}PROM.
PRE (Program Register Enable)	On board rev = 0: controlled by bit 6 of the Board Support Control Register. Set bit 6 to logic 1 to allow access to protection registers. On board rev = 1 onwards: controlled by the USERo signal of the PCI9056 (inverted). Set USERo to logic 0 to allow access to protection registers **Note:** USERo defaults to logic 1 on power-up or reset.

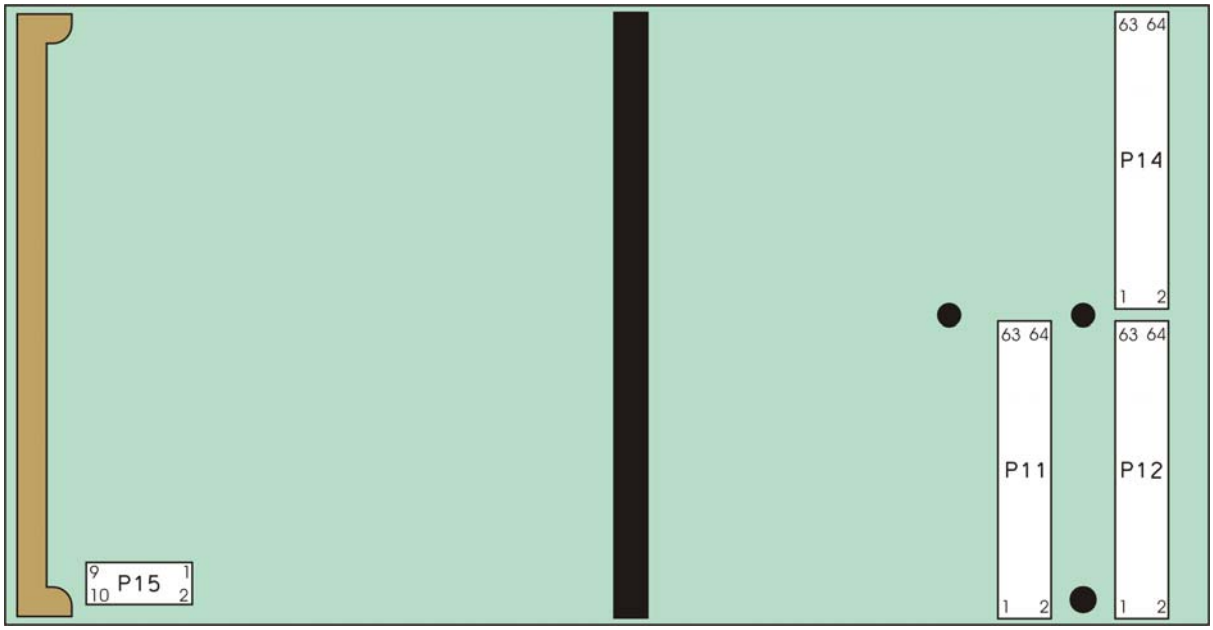
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6 - Connectors

This section gives the pinouts and signal descriptions for the connectors on the PMC1553E. The connectors have the following uses:

CONNECTOR	FUNCTION
P11, P12	32-bit PCI interface
P14	PMC rear I/O
P15	PLD programming

Figure 6-1. Connector Positions and Numbering



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PMC Connector Pinouts

P11

Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	GND	4	INTA~
5	INTB~	6	INTC~
7	BUSMODE1~	8	+5V
9	INTD~	10	PCI Reserved
11	GND	12	PCI Reserved
13	CLK	14	GND
15	GND	16	GNT~
17	REQ~	18	+5V
19	VIO	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3~
27	AD22	28	AD21
29	AD19	30	+5V
31	VIO	32	AD17
33	FRAME~	34	GND
35	GND	36	IRDY~
37	DEVSEL~	38	+5V
39	GND	40	LOCK~
41	SDONE~	42	SBO~
43	PAR	44	GND
45	VIO	46	AD15
47	AD12	48	AD11
49	AD09	50	+5V
51	GND	52	C/BE0~
53	AD06	54	AD05
55	AD04	56	GND
57	VIO	58	AD03
59	AD02	60	AD01
61	AD00	62	+5V
63	GND	64	REQ64~

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P12

Pin	Signal	Pin	Signal
1	+12V	2	TRST~
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	PCI Reserved
9	PCI Reserved	10	PCI Reserved
11	BUSMODE2~	12	+3.3V
13	RST~	14	BUSMODE3~
15	+3.3V	16	BUSMODE4~
17	PCI Reserved	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3V
25	IDSEL	26	AD23
27	+3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2~
33	GND	34	PMC Reserved
35	TRDY~	36	+3.3V
37	GND	38	STOP~
39	PERR~	40	GND
41	+3.3V	42	SERR~
43	C/BE1~	44	GND
45	AD14	46	AD13
47	M66EN (GND)	48	AD10
49	AD08	50	+3.3V
51	AD07	52	PMC Reserved
53	+3.3V	54	PMC Reserved
55	PMC Reserved	56	GND
57	PMC Reserved	58	PMC Reserved
59	GND	60	PMC Reserved
61	ACK64~	62	+3.3V
63	GND	64	REQ64~

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Signal Descriptions

Mnemonic	Description
AD0 to AD31	**Address/Data bits.** Multiplexed address and data bus
C_BE0 to C_BE3	**Command/Byte Enables.** During the address phase, these specify the type of cycle to carry out on the PCI bus. During the data phase, these are byte enables that specify the active bytes on the bus
FRAME~	**FRAME.** Driven low by the current master to signal the start and duration of an access
DEVSEL~	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE3
IRDY~	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	**LOCK.** Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE1~	**Bus Mode 1.** Driven low by a PMC if it supports the current bus mode
BUSMODE2~ to BUSMODE4~	**Bus mode.** Driven by the host to indicate the bus mode
RST~	**Reset.** Driven low to reset the PCI bus
TRDY~	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
PERR~	**Parity Error.** Driven low by a PCI agent to signal a parity error
SERR~	**System Error.** Driven low by a PCI agent to signal a system error
STOP~	**STOP.** Driven low by a PCI target to signal a disconnect or target-abort
INTA~, INTB~, INTC~	**Interrupt lines.** Level-sensitive, active-low interrupt requests
CLK	**Clock.** All PCI bus signals except RST~ are synchronous to this 33 MHz clock
REQ~	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
GNT~	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles
NC	**No connection**
REQ64~	**Request 64 Bit**. Driven low by a PCI master to request 64-bit transfer
M66EN	**66 MHz Operation.** Connected to GND for 33 MHz operation or left unconnected for 66 MHz
TCK	**Test Clock.** Clock for the PMC JTAG
TMS	**Test Mode Select.** Select Test Mode for PMC JTAG
TRST~	**Test Reset.** Reset any PMC JTAG devices
TDI	**Test Data In.** Input data for PMC JTAG chain
TDO	**Test Data Out.** Data from a PMC JTAG chain
5V	+5 Volts DC power
GND	The DC voltage reference for the system
VIO	Connects to VIO of the host card. 5V or 3.3V signaling are both supported
3.3V	+3.3 Volts DC power
–12V, +12V	No connection

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P14 I/O Connector

Pin	Signal	Pin	Signal
1	ITCSAN0	2	ITCSAP0
3	ISGNDA0	4	ISGNDA0
5	IDCSAN0	6	IDCSAP0
7	ITCSBN0	8	ITCSBP0
9	ISGNDB0	10	ISGNDB0
11	IDCSBN0	12	IDCSBP0
13		14	
15	ITCSAN1	16	ITCSAP1
17	ISGNDA1	18	ISGNDA1
19	IDCSAN1	20	IDCSAP1
21	ITCSBN1	22	ITCSBP1
23	ISGNDB1	24	ISGNDB1
25	IDCSBN1	26	IDCSBP1
27	GND	28	GND
29	CH0RTAD1	30	CH0RTAD0
31	CH0RTAD3	32	CH0RTAD2
33	CH0RTADPTY	34	CH0RTAD4
35		36	
37	CH0EXTTRIG	38	CH1EXTTRIG
39	CH1RTADPTY	40	CH1RTAD4
41	GND	42	CH1RTAD3
43	CH1RTAD0	44	CH1RTAD2
45	CH1RTAD1	46	
47	PIO0	48	PIO4
49	PIO1	50	PIO5
51	PIO2	52	PIO6
53	PIO3	54	PIO7
55		56	
57		58	
59		60	
61		62	
63		64	Reserved

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P14 Signal Descriptions

Mnemonic	Description
ITCSAN0, ITCSAP0	Bus A, channel 0 differential signals for use with transformer coupled stubs. ITCSAN0 is the negative connection and ITCSAP0 is the positive connection
ISGNDA0	Bus A channel 0 ground connections. Connected to the center tap of the secondary wiring of the isolation transformer and normally left open circuit. However, you can connect them to chassis ground for ESD or EMI/RFI considerations
IDCSAN0, IDCSAP0	Bus A channel 0 differential signals for use with direct coupled stubs. IDCSAN0 is the negative connection and IDCSAP0 is the positive connection
ITCSBN0, ITCSBP0	Bus B, channel 0 differential signals for use with transformer coupled stubs. ITCSBN0 is the negative connection and ITCSBP0 is the positive connection
ISGNDB0	Bus B channel 0 ground connections. Connected to the center tap of the secondary wiring of the isolation transformer and normally left open circuit. However, you can connect them to chassis ground for ESD or EMI/RFI considerations
IDCSBN0, IDCSBP0	Bus B channel 0 differential signals for use with direct coupled stubs. IDCSBN0 is the negative connection and IDCSBP0 is the positive connection
ITCSAN1, ITCSAP1	Bus A, channel 1 differential signals for use with transformer coupled stubs. ITCSAN1 is the negative connection and ITCSAP1 is the positive connection
ISGNDA1	Bus A channel 1 ground connections. Connected to the center tap of the secondary wiring of the isolation transformer and normally left open circuit. However, you can connect them to chassis ground for ESD or EMI/RFI considerations
IDCSAN1, IDCSAP1	Bus A channel 1 differential signals for use with direct coupled stubs. IDCSAN1 is the negative connection and IDCSAP1 is the positive connection
ITCSBN1, ITCSBP1	Bus B, channel 1 differential signals for use with transformer coupled stubs. ITCSBN1 is the negative connection and ITCSBP1 is the positive connection
ISGNDB1	Bus B channel 1 ground connections. Connected to the center tap of the secondary wiring of the isolation transformer and normally left open circuit. However, you can connect them to chassis ground for ESD or EMI/RFI considerations
IDCSBN1, IDCSBP1	Bus B channel 1 differential signals for use with direct coupled stubs. IDCSBN1 is the negative connection and IDCSBP1 is the positive connection
CH0RTAD0 to CH0RTAD4	Channel 0 RT Address bits 0 to 4. Used to set the address of an RT. Only valid in RT mode. Link the signal to 0V for a 0 bit or leave it open for a 1 bit †. To enable software RT address selection, leave these signals open.
CH0RTADPTY	Channel 0 RT Address Parity. Only valid in RT mode. It must provide the odd parity sum with CH0RTAD0 to CH0RTAD4. Link the signal to 0V for a 0 bit or leave it open for a 1 bit †. To enable software RT address selection, leave this signal open
CH0EXTTRIG	Channel 0 External Trigger/flag. A multi-functional input depending on the mode of operation. In RT mode, setting this line low sets the Subsystem Flag bit in the RT Status Word. In BC mode, if the external trigger has been enabled through software, a low-to-high transition on this line starts execution of the current BC frame
CH1EXTTRIG	As above, but for Channel 1
CH1RTAD0 to CH1RTAD4	Channel 1 RT Address bits 0 to 4. Used to set the address of an RT. Only valid in RT mode. Link the signal to 0V for a 0 bit or leave it open for a 1 bit †. To enable software RT address selection, leave these signals open.
CH1RTADPTY	Channel 1 RT Address Parity. Only valid in RT mode. It must provide the odd parity sum with CH1RTAD0 to CH1RTAD4. Link the signal to 0V for a 0 bit or leave it open for a 1 bit †. To enable software RT address selection, leave this signal open

† For example, for address 0xA (10_D), link CHzRTAD4, CHzRTAD2 and CHzRTAD0 to 0V and leave CHzRTPTY open (where z = channel 0 or channel 1 of the PMC1553E).

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Host P0 Connection

The following table shows the routing of the PMC1553E signals through the backplane P0 connector on PMC hosts such as Radstone's PowerX range. The PMC P14 pinout mapping to VME P0 is in accordance with VITA 35.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1						GND
2						GND
3				+5V	+5V	GND
4	IDCSAN0	ISGNDA0	ISGNDA0	ITCSAP0	ITCSAN0	GND
5	ISGNDB0	ISGNDB0	ITCSBP0	ITCSBN0	IDCSAP0	GND
6	ITCSAN1			IDCSBP0	IDCSBN0	GND
7	IDCSAP1	IDCSAN1	ISGNDA1	ISGNDA1	ITCSAP1	GND
8	IDCSBN1	ISGNDB1	ISGNDB1	ITCSBP1	ITCSBN1	GND
9						GND
10						GND
11						GND
12	CH0RTAD0	CH0RTAD1	GND	GND	IDCSBP1	GND
13		CH0RTAD4	CH0RTADPTY	CH0RTAD2	CH0RTAD3	GND
14	CH1RTDA4	CH1RTADPTY	CH1EXTTRIG	CH0EXTTRIG		GND
15	CH1RTAD1	CH1RTAD2	CH1RTAD0	CH1RTAD3	GND	GND
16	PIO5	PIO1	PIO4	PIO0		GND
17		PIO7	PIO3	PIO6	PIO2	GND
18						GND
19	+5V					GND

= Keying area on 80-way connectors

Note: PIO on rows 16 and 17 does not imply the availability of PIO on the PMC host board.

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Host P2 Connection

The following table shows the routing of the PMC1553E signals through the backplane P2 connector on hosts such as Radstone's PowerX range. The PMC P14 pinout mapping to VME P2 rows z and d is in accordance with VITA 35.

Pin	Row z	Row d
1	ITCSAP0	ITCSAN0
2		ISGNDA0
3	IDCSAN0	ISGNDA0
4		IDCSAP0
5	ITCSBP0	ITCSBN0
6		ISGNDB0
7	IDCSBN0	ISGNDB0
8		IDCSBP0
9		
10		ITCSAN1
11	ISGNDA1	ITCSAP1
12		ISGNDA1
13	IDCSAP1	IDCSAN1
14		ITCSBN1
15	ISGNDB1	ITCSBP1
16		ISGNDB1
17	IDCSBP1	IDCSBN1
18		GND
19	CH0RTAD1	GND
20		CH0RTAD0
21	CH0RTAD2	CH0RTAD3
22		CH0RTADPTY
23		CH0RTAD4
24		
25	CH1EXTTRIG	CH0EXTTRIG
26		CH1RTADPTY
27	GND	CH1RTAD4
28		CH1RTAD3
29	CH1RTAD2	CH1RTAD0
30		CH1RTAD1
31		
32		

See the P14 Signal Descriptions section for the meanings of the above signals.

Note: PIO is not usually available on P2.

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7 - Technical Assistance

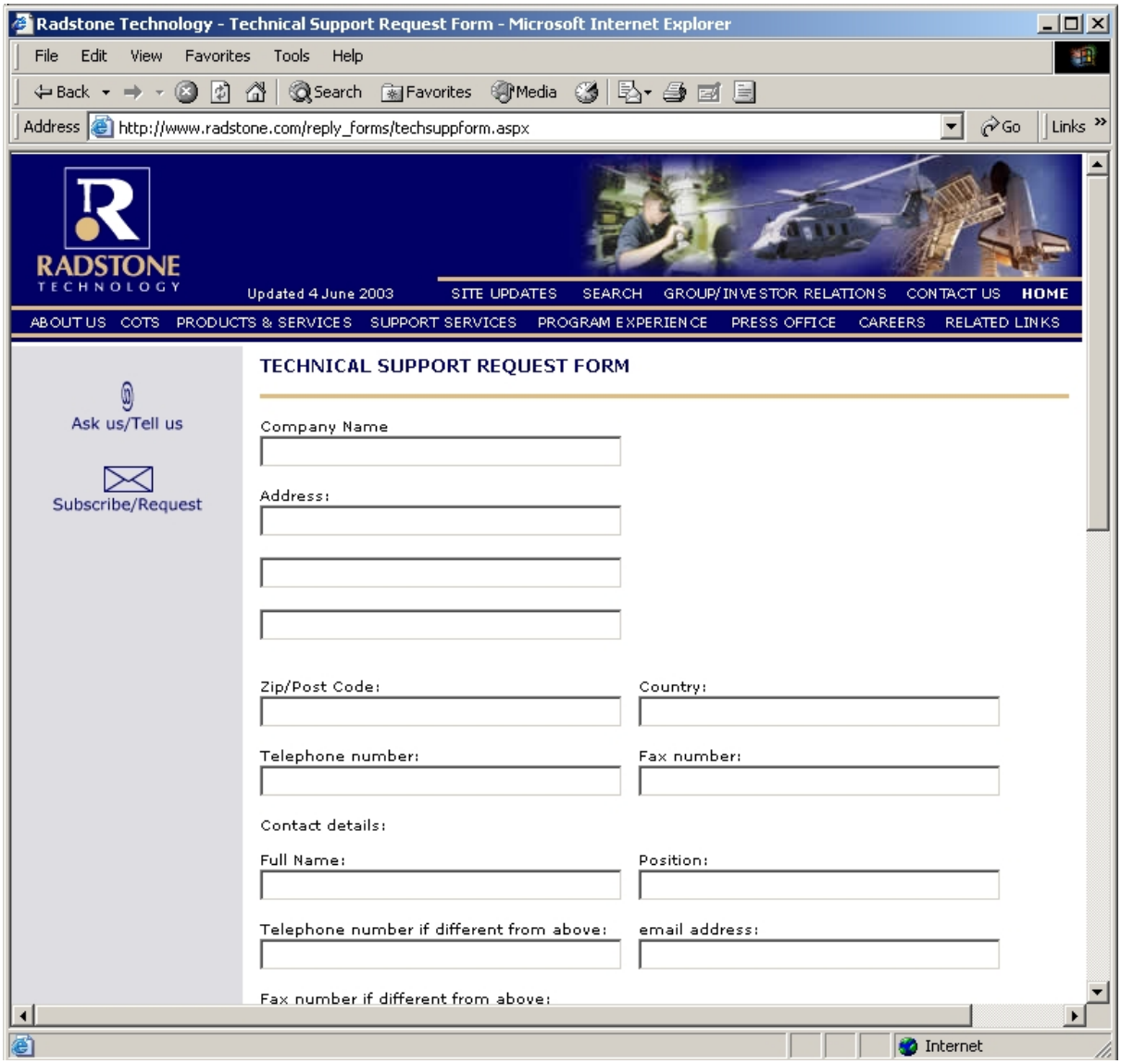
This section provides Radstone contact information (including details of information to have available when you call to report a problem) and some helpful hints for troubleshooting your PMC1553E.

Radstone Contact Information

Radstone does not anticipate that you will experience problems with your PMC1553E. However, in the unlikely event that you do have problems, for assistance please contact Radstone's Technical Help Line on:

+44 1327 359804 outside the UK
01327 359804 in the UK

Alternatively, you may register support requests using the Technical Support Request Form available through the Radstone web site at http://www.radstone.co.uk. This form looks like:



If you telephone for technical support, please be prepared to provide the same information as required in the above form.

Your query will be logged on Radstone's Technical Support database and allocated a unique Call Reference Number (CRN) for use in future correspondence.

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Troubleshooting

If you are experiencing a problem with your PMC1553E, there follow some general suggestions of actions you may take, which may resolve the problem without the need to contact Radstone's technical support.

First, ensure that it is not the host that is causing the problem, by checking that the host operates successfully in isolation (i.e. without the PMC1553E fitted).

If you have fitted the PMC1553E to a Radstone host or carrier card, you should also follow the suggestions in the Helpful Hints section in the appropriate host or carrier card's manual. By doing this, you can eliminate the host/carrier as being the source of the problem and narrow the scope to the PMC1553E itself or the PMC1553E to host/carrier connection.

Having satisfied yourself that the source of the problem is the PMC1553E, try the following suggestions.

- Ensure that there is no obvious damage to the PMC1553E (e.g. broken or missing components)
- Ensure that the PMC1553E is properly connected to the PMC host or carrier card, with the P11, P12 and P14 connectors properly located and firmly fitted. Ensure that the PMC1553E is firmly attached to the host/carrier and (conduction-cooled versions only) the centre stiffening bar
- Ensure that the PMC1553E is receiving power

These suggestions only apply if you are fitting the PMC1553E to a PMC host yourself. If Radstone has fitted your PMC1553E, it will have been extensively factory tested to provide correct operation. Please contact Radstone if this is not the case.

These suggestions mainly apply if you are fitting the PMC1553E to a Radstone PMC host. If you are fitting the PMC1553E to another manufacturer's PMC host, although the suggestions still apply in general, there may be different or additional requirements for the PMC1553E/PMC host combination. See the appropriate manufacturer's PMC host documentation for more details.

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Addendum

Following a Technical Update from PLX Technology Inc., the following additional Voltage Supply Requirements should be noted:

The +5V, +3.3V (if required by variant) and VIO supplies should all reach within 95% of their final value within 10mS of each other.

CAUTION

No PCI signals should be driven high to the PMC1553E before the VIO supply to the PMC1553E is established. Failure to comply with this requirement can result in damage to the PMC1553E.

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Appendix A - Specifications

This appendix gives a specification of the PMC1553E. It covers items such as the power requirements, the reliability, the general measurements etc., and lists the available variants.

Power Requirements

Power supplies and ground are shared between the connectors.

Current Consumption

1553 Transmitter Duty Cycle	Single Channel				Dual Channel			
	+3.3V Supply		+5V Supply		+3.3V Supply		+5V Supply	
	Typical	Maximum	Typical	Maximum	Typical	Maximum	Typical	Maximum
Idle	280 mA	450 mA	100 mA	150 mA	330mA	500mA	160mA	250mA
25%	280 mA	450 mA	200 mA	300 mA	330mA	500mA	330mA	500mA
50%	280 mA	450 mA	270 mA	400 mA	330mA	500mA	460mA	700mA
100%	280 mA	450 mA	450 mA	680 mA	330mA	500mA	730mA	1100mA

Notes:

1) The above table splits Current requirement between 3.3V and 5V. For 5V only variants (-x50 and –x55), these Current requirements must be combined.
2) Take care when using PMC modules as to how much current they require, especially from the +5V supply. The VME specification allows a maximum of 7.5 Watts to be drawn from the +5V supply in a single slot, over a host card's specified operating temperature range. It may not be possible to support all combinations within this limit.
3) The PMC1553E does not comprise the complete current load - some power is also dissipated on the 1553 bus.

Power Dissipation - 3.3V and 5V Supplies (For –b30 and –b33 Variants)

1553 Transmitter Duty Cycle	Single Channel		Dual Channel	
	Typical	Maximum	Typical	Maximum
Idle	1.7W	2.5W	2.2W	3.3W
25%	1.9W	2.8W	2.6W	3.8W
50%	2W	3W	2.9W	4.3W
100%	2.4W	3.5W	3.6W	5.3W

Power Dissipation - 5V Supply Only (For –b50 and –b55 Variants)

1553 Transmitter Duty Cycle	Single Channel		Dual Channel	
	Typical	Maximum	Typical	Maximum
Idle	2.2W	3.3W	2.8W	4.2W
25%	2.4W	3.6W	3.1W	4.7W
50%	2.5W	3.8W	3.4W	5.2W
100%	2.8W	4.3W	4.1W	6.2W

Voltage Supply Requirements

+5V ± 0.25V DC total excursion, including all transients.

Vripple (5V) = 50mV RMS (max) contained within the total excursion.

If applicable, +3.3V ± 0.165V DC total excursion, including all transients.

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PIO Characteristics

Parameter Symbol	Parameter Description	Test Conditions		Minimum	Maximum	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -100µA	V_{CC} – 0.2		V
			I_{OH} = -3.2mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = 100µA		0.2	
			I_{OH} = 24mA		0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW voltage for all Inputs		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6V, V_{CC} = Max			5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0V, V_{CC} = Max			-5	µA
I_{OZH}	Off-state Output Leakage Current HIGH	V_{OUT} = 3.6V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL}			5	µA
I_{OZL}	Off-state Output Leakage Current LOW	V_{OUT} = 0V, V_{CC} = Max $V_{IN} = V_{IH}$ or V_{IL}			-5	µA
I_{SC}	Output Short-circuit Current	V_{OUT} = 0.5V, V_{CC} = Max		-15	-160	mA

Note: The total current for all PIO outputs must not exceed 64mA.

EMC Regulatory Compliance and Safety

Air-cooled versions of PMC1553E are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction cooled versions are designed for integration into EMC hardened cabinets/boxes.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

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Reliability (MTBF)

The following table shows the calculated Mean Time Between Failures (MTBF) for the PMC1553E:

Environment	Fail Rate (Failures Per Million Hours)	Mean Time Between Failures (Hours)
Ground Benign 30°C	0.86088	1,161,602
Ground Fixed 40°C	2.35227	425,121
Ground Mobile 45°C	4.47023	223,702
Naval Sheltered 40°C	3.81861	261,875
Naval Unsheltered 45°C	7.17076	139,455
Airborne Inhabited Cargo 55°C	5.98706	167,027
Airborne Inhabited Fighter 55°C	6.54208	152,857
Airborne Uninhabited Cargo 70°C	10.65148	93,884
Airborne Uninhabited Fighter 70°C	17.10472	58,463
Airborne Rotary Wing 55°C	10.21622	97,884
Space Flight 30°C	0.80592904	1,240,804
Missile Flight 45°C	5.49418	182,011
Missile Launch 55°C	13.4171	74,532

These failure rates are based only on the components and connectors fitted to the board at delivery.

The failure rates used in this calculation are based on MIL-HDBK-217F Notice 1 with commercial or non-military quality level. Where a component did not comply with the MIL-HDBK, the closest equivalent, compliant component was used.

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Environmental Specification

The PMC1553E will operate and may be stored or transported without damage within the same limitations as the host board.

Convection-cooled Boards

Build Style	Temperature (°C)	Low Pressure (Feet)	Vibration	Shock	Humidity/ Salt Fog	Comments
Standard (Level 1)	**Operating:** 0 to +55 with airflow of 300 feet/minute. **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 15,000 **Storage:** 50,000	**Random:** 0.002g^2/Hz from 10 to 2000 Hz **Sine:** 2g from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating
Extended Temp (Level 2)	**Operating:** -20 to +65 with airflow of 300 feet/minute **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 15,000 **Storage:** 50,000	**Random:** 0.002g^2/Hz from 10 to 2000 Hz **Sine:** 2g from 5 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterised.
Rugged Air-cooled (Level 3)	**Operating:** -40 to +75 with airflow of 600 feet/minute **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 15,000 **Storage:** 50,000 **Rapid Decompression:** 0 to 50,000	**Random:** 0.04g^2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine:** 5g from 5 to 2000 Hz	20g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.

Conduction-cooled Boards

Build Style	Temperature (°C)	Low Pressure (Feet)	Vibration	Shock	Humidity/ Salt Fog	Comments
Rugged Conduction -cooled (Level 4)	**Operating:** -40 to +75 at the thermal interface **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 70,000 **Storage:** 70,000 **Rapid Decompression:** 0 to 70,000	**Random:** 0.1g^2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine:** 5g from 5 to 2000 Hz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

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Mechanical Specifications

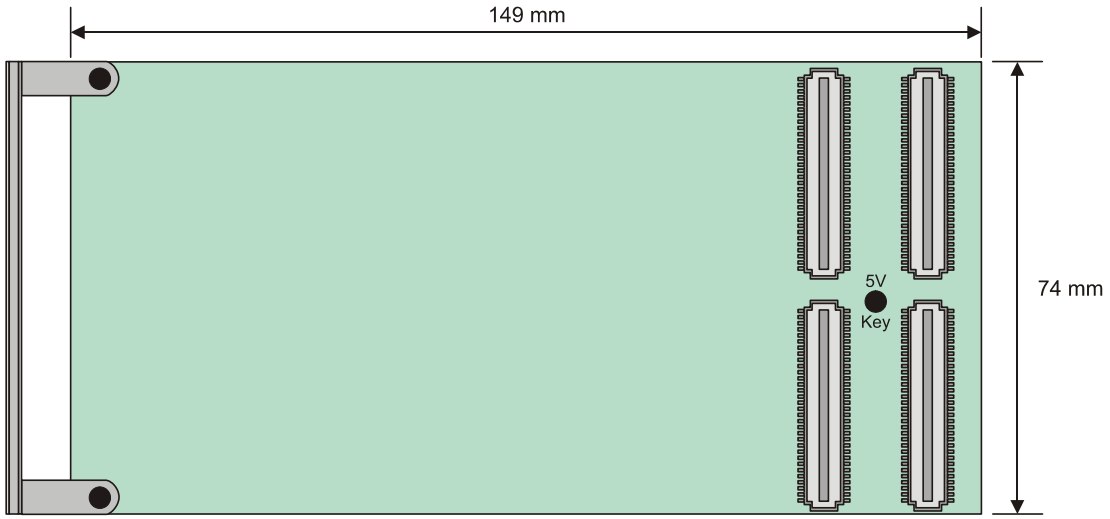
Weight

PMC1553E weighs approximately 100g for the single channel version.

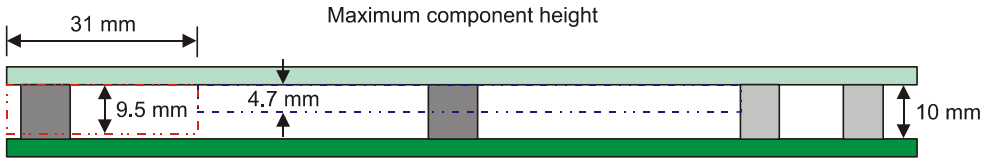
Dimensions

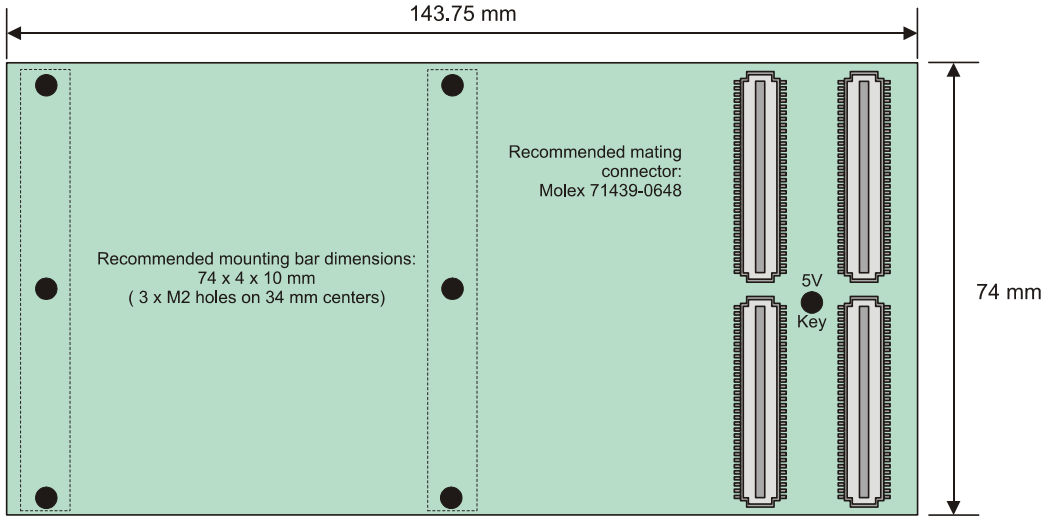
Build levels 1 to 3 of the PMC1553E conform to the IEEE P1386 PMC Specification, and level 4 conforms to the VITA 20-2001 Standard for Conduction Cooled PCI Mezzanine Cards (using primary thermal interface regions only). This allows all styles of assembly to be fitted to any PMC-compatible host.

The following diagrams show the overall dimensions, in millimeters, for general guidance only:



Air cooled PMC





Conduction cooled PMC

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Product Codes

The PMC1553E product codes are in the following form:

PMC1553E-bxx

where:

- b is the build level, which can be 1, 2, 3, 4 or 5
- xx is selected from the following table:

XX	DESCRIPTION
30	Single channel RT/BC/MT. 3.3V supplied on P12
33	Dual channel RT/BC/MT. 3.3V supplied on P12
50	Single channel RT/BC/MT. 3.3V regulator on-board
55	Dual channel RT/BC/MT. 3.3V regulator on-board

Preferred Build Variants are b50 and b55.

For example, PMC1553E-455 is a dual-channel RT/BC/MT in rugged conduction-cooled (level 4) build standard, with an 8-bit parallel port, rear I/O and an on-board 3.3V regulator.

All variants are delivered with the 1553 Library in VxWorks/GNU-C object code on CD-ROM.

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Glossary

Notes:

1) The PCI bus signals are explained in section 6.
2) This glossary only features terms special to this manual. Explanations of more general terms can be found in the Radstone Glossary, publication number RT5116.

ACE

Advanced Communications Engine from DDC.

BC

Bus Controller. One of the 1553 modes.

DDC

Data Device Corporation. A chip manufacturer.

MT

Monitor Terminal. One of the 1553 modes. Also sometimes called Passive Bus Monitor (PBM).

PIO

Parallel I/O.

PowerX

Radstone's PowerPC-based family of single board computers.

RT

Remote Terminal. One of the 1553 modes.

Serial EEPROM

EEPROM is usually a parallel device, i.e. the data is written-in or read-out in parallel on the 8 data lines. With Serial EEPROM, the data is read-out or written-in one bit at a time.

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