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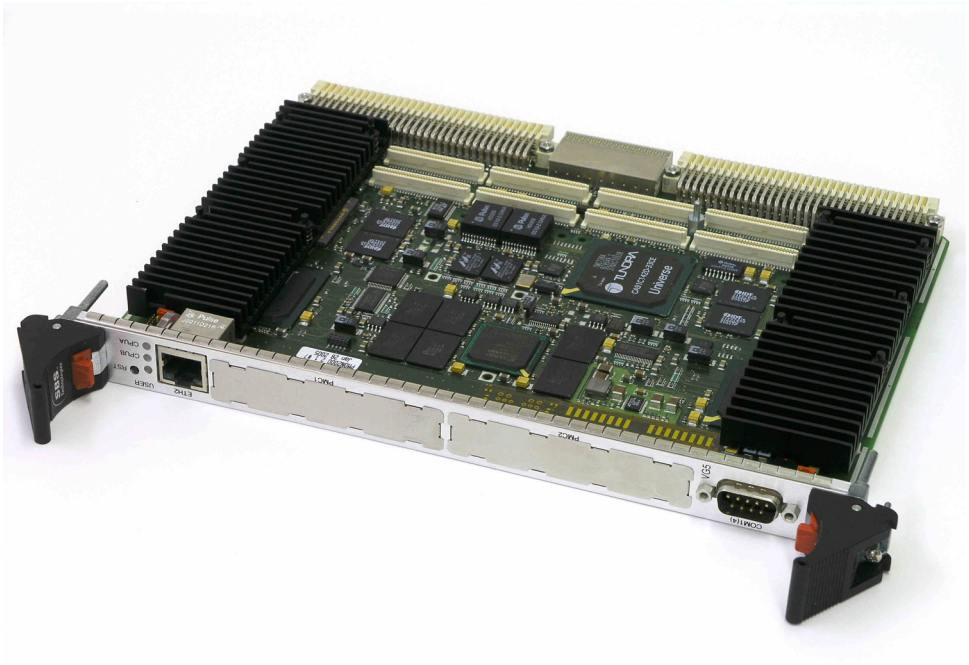
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GE
Intelligent Platforms

Hardware Reference Manual

VG5
Dual PowerPC™
6U VME SBC
First Edition

Publication No. HRMVG51E



imagination at work

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This manual applies to the VG 5 Dual PowerPC™ 6U VME Single Board Computer hardware revision 1.x and higher until superseded.

Document History

Edition	Date	By	Chapter	Comments
		HHS	All	Convert into current manual format
		TD	All	Added information regarding new VG5 V2.1 version
		HHS	All	Add and update boiler plates verify changes align tables and figures (centered) V-6: adapted format (left margin etc.) Change left margin to 2.5 cm resize tables & figures remove V.0x move specifications to new chapter 8
		MF	All	Minor cosmetic changes
		HHS	All	Add footnote Correct China address
		TD	Chap. 2, 7	Removed 5 ms power-up requirement for 5 V and 3.3V. Added: “Only for VG5 lower than version 2.x:”
		HHS	All	Minor cosmetic changes
		HHS	Support	Updated list of web site addresses
		HHS	Title	Change title, header and footer
		HHS	All	Cosmetic changes including unit symbol spelling
		HHS	Support Page 5	Insert info about PowerPC parameters for repair/return Insert Waste Disposal (WEEE) info
		HHS	Chap. 2 & 3	Update
		HHS		Insert Fig. 28 SATA LED
		HHS	Chap. 7	Specification: Revise electrical clearance parameter
		HHS	Chap. 3	Correct configuration paragraph
		HHS		Correct storage temperature values & styles (non-RoHS)
		TD	Table 81, Table 82	Power Consumption updated
		MF	Table of Content	Page numbers updated
		HHS	Chap. 3	Remove entries for keyboard & mouse; state that there is no battery; chapter start on odd pages; Change revision to edition on footer
		TD	Figure 7, Figure 8	Added placement for VG5 V3.x
			Chap. 4	Chapter FPGA and sub chapters restructured
			Chap. 7	Updated Chapter Thermal Behaviour
			all	Checked manual regarding V3.x
			Chap. 4	FPGA: Added remark regarding FPGA Version 0x0840 and WHOAMI bit in CNTRLSTAT register
		HHS	All	Cosmetic changes; replaced SBS with GE …; correct header styles; adjust page breaks
First	26 Apr 2010	HHS	Title page All	Insert photo; cosmetic changes replace Embedded Systems with Intelligent Platforms start chapters on odd page; add rear page

		Prepared for first release with new ‘GE style’
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HHS	p. 21	Reinsert 1 Gbit reference to System Controller
MF	All	Prepared for release
HHS	Title	Adjust vertical margins
HHS	All	Change front/rear page; add sales addresses change support chapter; remove Fanuc
HHS	All	Change tables to PDF-compatible format
HHS		More corrections

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Regulatory compliance

Products sold or transferred between companies or operated on company premises (factory floor, laboratory) do not need CE, FCC or equivalent certification. Boards or subsystems which cannot provide a useful function on their own do not need certification.

Certification can only be granted to complete and operational systems. There are authorized testing agencies, regulatory organizations and laboratories who will issue certificates of compliance after system testing.

GE Intelligent Platforms designs and tests all their products for EMI/EMC conformance. Where GE Intelligent Platforms supplies a complete/functional system for use by end users a certificate will be cited in the manuals/documents which are provided with the products.

Products manufactured by GE Intelligent Platforms should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign or additional filtering. However, the systems might not conform to specific regulations once assembled and used. The system integrator or installer must test for compliance as required in his country or by the intended application and certify this to the end user.

ESD/EMI issues

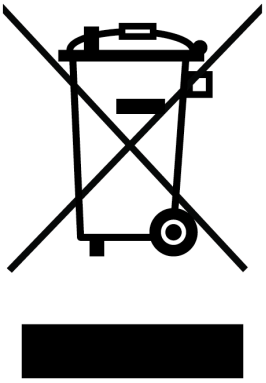
ESD (Electro-Static Discharge) and EMI (Electro-Magnetic Interference) issues may show up in complete and operational systems. There are many ways to avoid problems with these issues.

Any operational system with cables for I/O signals, connectivity or peripheral devices provides an entry point for ESD and EMI. If GE Intelligent Platforms does not manufacture the complete system, including enclosure and cables, it is the responsibility of the system integrator and end user to protect their system against potential problems. Filtering, optical isolation, ESD gaskets and other measures might be required at the physical point of entry (enclosure wall of box or rack). For example it is state-of-the-art that protection can not be done at the internal connector of an RTM if a cable is attached and routed outside the enclosure. It has to be done at the physical entry point as specified above.

Products manufactured by GE Intelligent Platforms should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign. However, the systems might be subject to problems and issues once assembled, cabled and used. The end user, system integrator or installer must test for possible problems and in some cases show compliance to local regulations as required in his country or by the intended application.

Waste Disposal

The mark or symbol on any electrical or electronic product shows that this product may not be disposed off in a trash bin. Such goods have to be returned to the original vendor or to a properly authorized collection point.



Electric waste disposal symbol with black bar as explained below

The black bar underneath the waste bin symbol shows that the product was placed on the market after 13 August 2005. Alternatively the date of 'placed on the market' is shown in place of the bar symbol.

CE conformance declaration

CE certification is required in EU countries for equipment which is used/operated by the end user. Products sold or transferred between companies or operated on company premises (factory floor, laboratory) do not need CE certification.

CE certification can only be granted to complete and operational systems. Boards or subsystems which cannot provide a useful function on their own do not need CE certification.

GE Intelligent Platforms designs and tests all their products for EMI/EMC conformance. Products manufactured by GE Intelligent Platforms should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign or additional filtering. The system integrator or installer must, in any case, test for CE compliance and certify this to the end user.

Where GE Intelligent Platforms supplies a complete/functional system for use by end users in EU countries a CE certificate will be cited in the manuals/documents which are provided with the products. The CE (and year of certification) symbol is shown on the equipment, typically on the type or S/N label or close to the power cable entry.

GE Intelligent Platforms have tested their boards using their own card cages (chassis). Test results of these tests are available upon request.

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For contact and other information (service, warranty, support etc.) see address list in chapter: 'Support, Service'.

Welcome

The VG5 6U VME Single Board Computer is a fully PowerPC compatible stand-alone computer equipped with numerous functions and add-on features on a minimized board size. This board is a member of the GE Intelligent Platforms VME family which includes a variety of different VME type boards, carriers and systems. This technical manual is designed to provide information regarding the general use and application of the VG5 6U VME Single Board Computer, as well as details of the hardware design. Software methods and programming information are also provided.

Chapter 1 gives a brief overview of the functions and features of VG5
Chapter 2 illustrates unpacking and inspection procedures
Chapter 3 provides installation procedures
Chapter 4 describes all function blocks
Chapter 5 explains the VTM20 Transition Module
Chapter 6 has Tips and Tricks
Chapter 7 details the specifications
Chapter 8 shows a Glossary
Chapter 9 provides warrant, repair and support information

Please observe all safety instructions when handling GE Intelligent Platforms products as outlined in the unpacking and installation chapters.

The following documents also cover items relevant to the VG5 Single Board Computer. All documents are included as files on the Technical Product Information CD-ROM or they are part of the software package.

- Integrity Board Support Package for VG5: INT5-BVG5 User's Manual
- VxWorks Board Support Package for VG5: VXWx-BVG5 Software User's Manual

Typographic Conventions

This manual uses the following notation conventions:

- *Italics* (sometimes additional in *blue* color) emphasize words in text or documentation or chapter titles or web addresses if underlined.
- Hexadecimal values (base 16) are represented as digits followed by "h", for example: 0C**h**.
- Hexadecimal values (base 16) are represented as digits preceded by "H", for example: **H**0C.
- Hexadecimal values (base 16) are represented as digits preceded by "$", for example: **$**0C.
- Binary values (base 2) are represented as digits followed by "b", for example 01**b**
- The use of a "#" (hash) suffix to a signal name indicates an active low signal. The signal is either true when it is at a logic zero level (voltage close to 0 V) or the signal initiates actions on a high-to-low transition.
- The use of a "\" (backslash) prefix to a signal name indicates an active low signal. The signal is either true when it is at a logic zero level (voltage close to 0 V) or the signal initiates actions on a high-to-low transition.
- Text in `Courier` font indicates a command entry or output from an GE Intelligent Platforms embedded PC product using the built-in character set.
- Notes, warning symbols and cautions call attention to essential information.

Product Properties

Certification

The product or products described in this technical manual cannot be operated by themselves. They are components for integration into operational systems or add-ons to such systems. The products have been designed to meet relevant regulatory standards like FCC and CE. As mandated by these standards conformance to these standards can only be certified for complete operational systems. This has to be done by the end-user or by the systems integrator in their operational systems. GE Intelligent Platforms have tested some products in their own systems. Upon request information is available which products have been tested and about the specific environment under which GE Intelligent Platforms has tested these components.

Altitude

Altitude, air pressure and ambient temperature influence the thermal operation of the components described in this manual. They have been developed and tested at about 500 m (1650 ft.) above sea level at a typical ambient temperature of 20 °C (68 °F). Because of only marginal variations within a limited range of altitudes these products operate as specified within altitudes from sea level to 1000 m (3300 ft.). GE Intelligent Platforms can assist the user of these components in planning operation outside this altitude range upon request.

Options

This manual describes the basic product plus all options. Your product may not have all options implemented. Please verify with your purchase contract which options are implemented. Descriptions of options which are not implemented obviously do not apply to your product.

Support, Service and Warranty

The manufacturer grants the original purchaser of GE Intelligent Platforms products a warranty of 24 months from the date of delivery. For details regarding this warranty refer to the Terms & Conditions of the initial sale.

Please see chapter “Support, Service, and Warranty” for further details on repairs and product support.

For support on the web and product information, visit our website at
http://www.ge-ip.com

Table of Contents

Legal Information....5
Legal Disclaimers....5
Regulatory compliance....6
ESD/EMI issues....6
Waste Disposal....7
CE conformance declaration....7
Corporate addresses....8

Welcome....9

Typographic Conventions....10
Product Properties....10
Certification....10
Altitude....10
Options....10
Support, Service and Warranty....11
Table of Contents....13
List of Tables....17
List of Figures....19

CHAPTER 1 **General Information....21**

Features....21

CHAPTER 2 **Unpacking and Inspection....25**

Delivery Volume....25
Available Accessories....25
ESD....26
Electrostatic Discharge Notice....26
Warning....26
Initial Inspection....27
Unpacking....27
Handling....28

CHAPTER 3 **Hardware Installation....31**

Installation preparation....31
General Advisories....31
Caution....32
Required items....32
Backplane and Power Supply....32
Advice on Batteries....32
Installation of a plug-in board....33
Block Diagram Dual Node....34
Block Diagram Single Node....34
Placement Plan VG5 Board Version V1.x....35
Top Side VG5 V1.x....35
Bottom Side VG5 V1.x....36
Placement Plan VG5 Board Version V2.x....37

Top Side VG5 V2.x....37
Bottom Side VG5 V2.x....38
Placement Plan VG5 Board Version V3.x....39
Top Side VG5 V3.x....39
Bottom Side VG5 V3.x....40
Front Panel....41
Socket Installation....41
VME Reset Jumper....41
Bootselect Jumper....43
VG5 Version V1.x and higher....44
Watchdog Jumper....45
VG5 Version V1.x and higher....45
Flash Write Protect Jumpers (Resistors)....46
VG5 Version V1.x and higher....47
Clocking....47
Interfaces and Connectors on the VG5....49
Pin Description for the following tables:....49
VMEbus Connector P1 (P7100)....49
VMEbus Connector P2 (P7200)....51
VMEbus Connector P0 (P7000)....53
PMC Slot 1 connectors (P7101, P7102, P7103)....53
PMC Slot 2 connectors (P7201, P7202)....54
PMC-IO connector (P7104 and P7204)....56
COP Interface Connectors (P1100, P1150)....56
VG5 Version V1.x and higher....58
JTAG Interface....59
PCI-IDSEL....59
Interrupts....60
Reset....63
Hard and Fast Reset....64

CHAPTER 4 **Function Blocks....67**

PowerPC Processor....67
L3 Cache....67
Chipset....67
DDR-SDRAM Memory....67
Flash ROM....67
FPGA....68
FPGA Overview (Block Diagram)....68
FPGA Overview (Registers)....71
FPGA Dual Port RAM....72
FPGA Interrupt Controller A....73
FPGA Interrupt Controller B....76
FPGA Address decoder A/B....77
FPGA Control and Status Register A/B_CNTRLSTAT....78
FPGA Test Register A/B....81
FPGA Watchdog Timer A/B....81
FPGA Watchdog A/B (Registers detailed)....84
FPGA System IO....85
FPGA User General Purpose IO (UGPIO)....88

FPGA in single Node VG5 Version 91
PCI Buses 92
Asynchronous Serial Ports COM1, COM4 92
Serial Communication Interface COM2, COM3, COM5, COM6 93
Extra Baud Rate Generator Clocks in VG5 V2.x (and above) 95
Counter and Timer 97
Real Time Clock 97
COP Interface 98
PMC Interfaces 98
PMC Power Requirements 98
Serial ATA 98
Ethernet Interfaces 99
VMEbus Interface 100
Two-Wire-Serial-Interface (TWSI) Devices 101
Chipset Init EEPROM 101
SPD and Factory EEPROM 101
NVRAM - User Serial EEPROM 101
Temperature Sensor 102
Non-volatile Switches 102
Analog Digital Converter (VG5 2.x and above) 104
LED 105
Reset Button 106

CHAPTER 5 **Transition Module VTM20** **107**

VTM20 V1.x 108
VTM20 V1.x 109
Connectors 110
Backplane Connectors P0/P2 110
Power Supply 112
Card Fail LED and Boot Select Jumper 112
Reset Button 112
Ethernet Interfaces 113
COP Debug and JTAG Interfaces P2000, P2001, P6000 115
Serial Interfaces COM1...COM6 P100x 117
PMC-IO connectors 120
Miscellaneous Connector P8100 123
Serial ATA Connector P9000 123
User General Purpose IO +5 V P8000 124

CHAPTER 6 **VG5 Tips and Tricks** **125**

Adapter Cables 125
Serial Port cables (RS232) 125

CHAPTER 7 **Specifications** **129**

Specification 129
Power Requirements 129
External Battery Voltage for RTC 131
Electrical clearance 131
Thermal Behaviour 133
Thermal Condition Air Cooled Styles (C-, I-, 1-, 3-Styles) 133

Thermal Condition Conduction Cooled Styles (N-, 8-Style) 136

CHAPTER 8 **Glossary** **139**

CHAPTER 9 **Support, Service and Warranty** **141**

Technical Support 141
Support on the Web 142
Warranty 142
Error Report 142

List of Tables

Table 1: Serial COM Ports 23
Table 2: VME Reset Jumper J7300 (VG5 V1.0 - V1.2) 41
Table 3: VME Reset Jumper J7300 (VG5 V1.3 and higher) 42
Table 4: Bootselect Jumper J2520, J2521 43
Table 5: Watchdog Jumpers J2500, J2501 45
Table 6: P1 Connector 50
Table 7: P2 Connector 52
Table 8: P0 Connector 53
Table 9: PMC Slot 1 Connectors 54
Table 10: PMC Slot 2 Connectors 55
Table 11: PMC1/2 IO Connector 56
Table 12: P1100 A-COP, P1101 B-COP 57
Table 13: COP Terminations 57
Table 14: a-e: PCI-IDSEL 60
Table 15: IRQ inputs Node A (MPP of Chipset A) 62
Table 16: IRQ inputs Node B (MPP of Chipset B) 62
Table 17: Reset Sources 63
Table 18: FPGA Register touched by Fast Reset 65
Table 19: Overview FPGA Registers (Node A and B) 71
Table 20: A_IRQ_CAUSE Register 74
Table 21: VMEbusErr, Thermo_A/B/C IRQs 74
Table 22: A_IRQ_MASK Register 75
Table 23: B_IRQ_CAUSE Register 76
Table 24: VMEbusErr, Thermo_A/B/C IRQs 77
Table 25: B_IRQ_MASK Register 77
Table 26: A_CNTRLSTAT Register 79
Table 27: B_CNTRLSTAT Register 80
Table 28: Test register A/B 81
Table 29: A/B_WDGCOMP0/1 84
Table 30: A/B_WDGDATA + Service 84
Table 31: Watchdog A Control-Bits 84
Table 32: Watchdog B Control-Bits 85
Table 33: SYS_IN Register 86
Table 34: A_SYS_OUT Register 87
Table 35: B_SYS_OUT Register 88
Table 36: UGPIO at P2 (P7200) 89
Table 37: UGPIO Registers 90
Table 38: a-b: UGPIO Electrical Specification 91
Table 39: a-b: COM1+4 Pin assignments at P2 and front connector P2710 93
Table 40: COM2 Signals at P2 and front connector P2720 94
Table 41: COM3 Signals at P2 94
Table 42: COM5 Signals at P2 94
Table 43: COM6 Signals at P2 95
Table 44: ConfigBit settings for Extra Baud Rate Oscillators in SysIn-Register 96
Table 45: HDLC scenario's 97
Table 46: PMC Power Requirements 98
Table 47: Ethernet LED indicators 99
Table 48: TWSI Devices Node A and B Addresses 101
Table 49: Non-volatile switches in V1.3 and higher 104
Table 50: ADC 105
Table 51: LEDs and their registers 106
Table 52: TM P0 Connector P7000 110

Table 53: TM P2 Connector P7200 111
Table 54: TM Power Ratings 112
Table 55: TM Boot Select jumper 112
Table 56: VG5 Ethernet Variants 113
Table 57: TM Gigabit RJ45 Jacks 113
Table 58: TM Fast Ethernet RJ45 Jack 114
Table 59: TM Fast Ethernet Header 115
Table 60: matching VTM variant for use of Link Status LEDs 115
Table 61: TM COP A Header 116
Table 62: TM COP B Header 116
Table 63: TM JTAG Header 117
Table 64: TM COM1 117
Table 65: TM COM2 118
Table 66: TM COM3 118
Table 67: TM COM4 118
Table 68: TM COM5 119
Table 69: TM COM6 119
Table 70: RS422 / 485 Termination Resistors 119
Table 71: TM PIM1 connector 120
Table 72: TM PMC1 IO header 121
Table 73: TM PIM2 connector 122
Table 74: TM PMC2 IO header 123
Table 75: TM Misc Connector 123
Table 76: TM Serial ATA connector 124
Table 77: TM UPGIO 5 V header 124
Table 78: Simple Null Modem 125
Table 79: Simple Null Modem for VG5D at P2710 (COM1/4) 126
Table 80: Splitter Cable for VG5D P2710 (Front, COM1/4) 127
Table 81: Power Consumption VG5 V1.x 130
Table 82: Power Consumption VG5 V2.x and above 130
Table 83: Environment 132
Table 84: Product ID Position 13 (Environments) 132
Table 85: Operating Temperature Range –7457 Dual Node VG5 V1.x Air Cooled (C-, 1-Style) 135
Table 86: Operating Temperature Range: VG5 V1.x I-, 3-Style at 3 m/s airflow 135
Table 87: Operating Temperature Range: VG5 V2.x and V3.x C-, 1-Style at 3 m/s airflow 136
Table 88: Operating Temperature Range: VG5 V1.x Conduction Cooled Styles (N-/ 8-Style) 137
Table 89: Operating Temperature Range: VG5 V2.x and V3.x Conduction Cooled Styles (N/ 8-Style) 138

List of Figures

Figure 1: VG5 Block Diagram (Dual Node) 34
Figure 2: VG5 Block Diagram (Single Node) 34
Figure 3: Placement Top Side (VG5 V1.x) 35
Figure 4: Placement Bottom Side (VG5 V1.x) 36
Figure 5: Placement Top Side (Vg5 V2.x) 37
Figure 6: Placement Bottom Side (VG5 V2.x) 38
Figure 7: Placement Top Side (VG5 V3.x) 39
Figure 8: Placement Bottom Side (VG5 V3.x) 40
Figure 9: Front Panel with one PMC site 41
Figure 10: Front Panel with two PMC sites 41
Figure 11: Location of VME-Reset Jumper J7300 (VG5 V1.0-V1.2) 42
Figure 12: Location of VME-Reset Jumper J7300 (VG5 V1.3 and higher) 43
Figure 13: Location of Node A Bootselect Jumper J2520 , (VG5 V1.x and higher) 44
Figure 14: Location of Node B Bootselect Jumper J2521 , (VG5 V1.x and higher) 44
Figure 15: Location of Node A Watchdog Jumper J2500 , (VG5 V1.x and higher) 45
Figure 16: Location of Node B Watchdog Jumper J2501 , (VG5 V1.x and higher) 46
Figure 17: Location of Write Flash Protection Jumpers (SMD Resistors) (VG5 V1.x and higher) 47
Figure 18: Main Clock Tree 48
Figure 19: PCI Bus Clocks 48
Figure 20: COP A P1100 Connector Location (VG5 v1.x and higher) 58
Figure 21: COP B P1150 Connector Location (+Opt. P1101,P1151) (VG5 V1.x and higher) 59
Figure 22: Reset Structure 64
Figure 23: FPGA Block Diagram Dual Node 69
Figure 24: FPGA Block Diagram Single Node 70
Figure 25: IRQ Cause Register Structure 75
Figure 26: Memory Write Protection Areas 78
Figure 27: Watchdog Block Diagram 82
Figure 28: Watchdog Timing Diagram 83
Figure 29: Baud Rate Generator for MPSCs 95
Figure 30: Location of SATA LED D1800 99
Figure 31: Blockdiagram: Non-volatile switches in V1.0-V1.2 103
Figure 32: Blockdiagram: Non-volatile switches and J7300 in V1.3 and higher 103
Figure 33: Placement Plan Top Side (VTM20 V1.x) 108
Figure 34: Placement Plan Bottom Side (VTM20 V1.x) 109
Figure 35: RJ45 Jack pinning and LEDs 114
Figure 36: ΔTemperature of VG5 Single Node C-, 1-Style 134
Figure 37: Definition of Card Edge 136

CHAPTER 1 General Information

Chapter Scope

This manual applies to the VG5 single board computer version 1.x and 2.x until superseded.

Features

Microprocessor

Single or dual Freescale® PowerPC™
Freescale® PowerPC™ MPC7455 processor 800 MHz -1000 MHz
Freescale® PowerPC™ MPC7457 processor 800 MHz-1266 MHz

Cache RAM

On chip 32 kBytes instruction + 32 kBytes data first level cache
On chip 256 kByte or 512 kByte second level cache
external 2 MByte third level cache for each processor node

DRAM

One bank for each system controller,
256 MByte or 512 MByte per bank,
memory interface with 133 MHz,
memory banks are ECC controlled and on-board soldered.

NVRAM

NVRAM build with a 1 Mbit Serial EEPROM for Node A and the same for Node B

Flash

Each Node has up to 128 MByte (256 MByte from V3.0) Flash which includes a Boot Program

System Controller

Discovery II Marvell® MV64360 system controller for each processor node for independent operation
Up to 133 MHz CPU bus frequency
DDR SDRAM Controller supports up to 1 Gbit devices
Two 64-bit PCI-X buses
Separate device bus interface

Two integrated Gigabit Ethernet MAC controllers
Two Multi Protocol Serial Controllers (MPSC)

Single/Dual Node

In a Dual Node configuration each node has CPU, System Controller,
DDR SDRAM bank, PMC site, flash banks and system devices.
Interconnection of the two Nodes is with a 64-bit PCI-X bus and via FPGA dual port SRAM
In a Single Node configuration there are one CPU, System Controller,
DDR SDRAM bank, PMC site, and flash banks. The second PMC site is connected via a jumper bridge

Real Time Clock

MC146818 compatible RTC only with external battery voltage supply and 114 byte non-volatile SRAM

Watchdog

A Watchdog for each CPU activates reset under software control

Timer/Counter

8 timers each 32-bit wide for system timing and periodic interrupt

FPGA

Field Programmable Gate Array for internal logic, provides additional 1 kByte Dual Port SRAM for message interchange and also 32 user programmable IO signals
50 % of the FPGA is free for user defined features

PMC slots

Two 64-bit PCI mezzanine connectors for standard PMC as well as for rugged PMC. IO signals available at the rear connectors. PMC1 is usable with PCI 33/66 MHz. PMC2 is limited to 33 MHz. In Dual Node configuration PMC1 is bound to Node A and PMC2 is bound to Node B.

Ethernet

Each Node has one Gigabit Ethernet and one Fast Ethernet channel coming directly from the MV64360 System Controller.
These Ethernet channels are either front or rear (Node A) available or only rear (Node B).

Serial IO

Up to six serial interfaces, three for Node A and three for Node B:
For each node one async. 16550 compatible full duplex RS-232 channel with a transfer rate of up to 115.2 kBaud
For each node there are two Multi Protocol Interface RS-422/485 channels available for transfer rates of up to 10 Mbit/s. One of the Node A serial channels is software selectable RS-232 or RS-422/485 (115 kbit/s, 250 kbit/s)
Serial interfaces are available at rear or front

Table 1: Serial COM Ports

Port	Type	max. Speed	Front IO	Rear IO	Dual Node	Single Node
COM1	RS232 UART	115.2 kbit	Yes	Yes [1]	A	Yes
COM2	RS232/422 MPSC	250 kbit	Option [3]	Yes	A	Yes
COM3	RS422 MPSC	10 Mbit	No	Yes	A	Yes
COM4	RS232 UART	115.2 kbit	Yes [1, 2]	Yes [1]	B	Yes
COM5	RS422 MPSC	10 Mbit	No	Yes	B	No
COM6	RS422 MPSC	10 Mbit	No	Yes	B	No

Notes:
1) only TxD and RxD signals
2) only for Dual Node VG5 (SUBD-9pin shared with COM1)
3) if used then no PMC2 available

General Purpose IO
32-bit general purpose IOs individually programmable for input, output or edge triggered interrupt. IO signals are available at rear IO (shared with PMC IO)

VMEbus
PCI bus to VMEbus bridge (Tundra Universe IID) ,
up to 60 MByte/s transfer rates
Big endian / Little endian conversion control
FIFOs for write posting, DMA controller with linked list support
Master and Slave transfer modes:
BLT, ADOH, RMW, LOCK, RETRY
A32 / A24 / A16 and D64 (MBLT) / D32 / D16 / D8
Full VMEbus system controller

Serial ATA
PCI to SATA Bridge (SIL3112); new = SIL3512 with version V3.0: One channel SATA interface available at rear (shared with PMC1 IO).
Need new BSP (VxW2-BVG5 V1.2/6), driver and software for SIL 3512

COP Interfaces
Processor debug interface for external emulator for each node. Available at rear or on-board

JTAG Interface
JTAG interface for all devices with JTAG interface. Optionally available at rear (shared with PMC IO and COP interface)

LED Indicators
CPU Fail LEDs for each node and one User LED

Temperature Sensors
Three sensors (LM75) show the temperature of the system board near both CPUs and in the board centre, software readable in 0.5 °C increments from -55 °C to +125 °C

Front Panel

Two PMCs, one DSUB9 Serial Connector, RJ45 Fast Ethernet Jack, LEDs and Reset Button
Optional RJ45 Gigabit Ethernet Jack, and DSUB9 Serial Interface

Backpanel IO

COM1-6 [1)], GPIO [2)], Serial ATA [3)], reset, watchdog [2)], PMC1 IO [3)],
PMC2 IO [2)], Ethernet [1)], Boot Select, JTAG [2)], COP [2)]

[1)] depends on configuration: Single /Dual Node VG5
[2)] depends on P2 row a+c configuration (PMC2 rear or front IO)
[3)] depends on P1 configuration (S-ATA only possible with limited PMC2 rear IO)

Transition module VTM20 available for compatible connectors

Power

Dual Power Supply +5 V and +3.3 V.

Conduction Cooling

Conduction Cooling available

Conformal Coating

The board can optionally be conformal coated to protect against humidity and fungus

CHAPTER 2 Unpacking and Inspection

Chapter Scope

This chapter covers the suggested inspection and preparation considerations and background information necessary prior to using the VG5. Unpacking, initial inspection, and first-time operation of the VG5 are covered. Following the procedures given in the chapter is recommended, since they will verify proper operation after shipping and before the product is integrated into your system.

Delivery Volume

Please check that the delivered package contains the following items:

Qty.	Item	Purpose
1	VG5	Dual PowerPC 6U VME Single Board Computer
1	CDROM	Technical Product Information with driver software and manuals in Adobe Acrobat (PDF) format

The manual files are also available through the World Wide Web from our Web-Server:
http://www.ge-ip.com

Available Accessories

The following table lists accessory options which are available for the board or module:

Item	Purpose
	no accessories defined

Please contact the sales department or your sales representative for latest information on options and accessories.

Accessories are subject to change without notice.

ESD

Electrostatic Discharge Notice

The discharge of static electricity, known as Electro Static Discharge or ESD, is a major cause of electronic component failure. The board has been packed in a static-safe bag which protects the board from ESD while the board is in the bag. Before removing the board or any other electronic product from its static-safe bag, be prepared to handle it in a static-safe environment.



You should wear a properly-functioning antistatic strap and ensure you are fully grounded. Any surface upon which you place the unprotected board should be static-safe, usually facilitated by the use of antistatic mats. From the time the board is removed from the anti static bag until it is in the card cage and functioning properly, extreme care should be taken to avoid 'zappin' the board with ESD. You should be aware that you could 'zap' the board without you knowing it; a small discharge, imperceptible to the eye and touch, can often be enough to damage electronic components. Extra caution should be taken in cold and dry weather when static easily builds up.

Only after ensuring that both you and the surrounding area are protected from ESD, carefully remove the board or module from the shipping carton by grasping it by the front panel and the connectors. Place the board, in its antistatic bag, flat down on a suitable surface. You may then remove the board from the anti static bag by tearing the ESD warning labels.

Warning

This is a Class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

Notes:
Drain static electricity before you install or remove any parts. Installing or removing modules without observing this precaution could result in damage to this and/or other modules in your system.

Initial Inspection

After unpacking the board or module, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socket components), contact GE Intelligent Platforms for additional instructions. Depending on the severity of the damage, it may need to be returned to the factory for repair**. DO NOT apply power to the board if it has visible damage.** Doing so may cause further, possibly irreparable damage, as well as introduce a fire or shock hazard.

Since some of the boards or modules incorporate a number of socketed components, including the CPU, memory, etc., these should be inspected to make sure they are seated fully in their sockets.

Note
Please observe all safety procedures to avoid damaging system and protect operators and users.

Unpacking

1. Please read this manual carefully before unpacking the module or fitting it into your system. This will certainly save time and avoid trouble.
2. Please observe the precautions for electrostatically sensitive modules.
3. If the product contains batteries, please do not place the board on conductive surfaces or anti-static plastic or sponge, which can cause shorts and lead to battery or board trace damage.
4. Please do not exceed the specified operational temperatures. Please note that batteries might have temperature restrictions.
5. Keep all original packaging material for future storage or warranty shipments of the board.

Although the board or module is carefully packaged to protect it against the rigors of shipping, it is still possible that shipping damages can occur. Careful inspection of the shipping carton should reveal some information about how the package was handled by the shipping service. If evidence of damage or rough handling is found, you should notify the shipping service and GE Intelligent Platforms as soon as possible.

Retain all packing material in case of future need.

Note
Before installing or removing any board, please ensure that the system power and external supplies have been turned off.

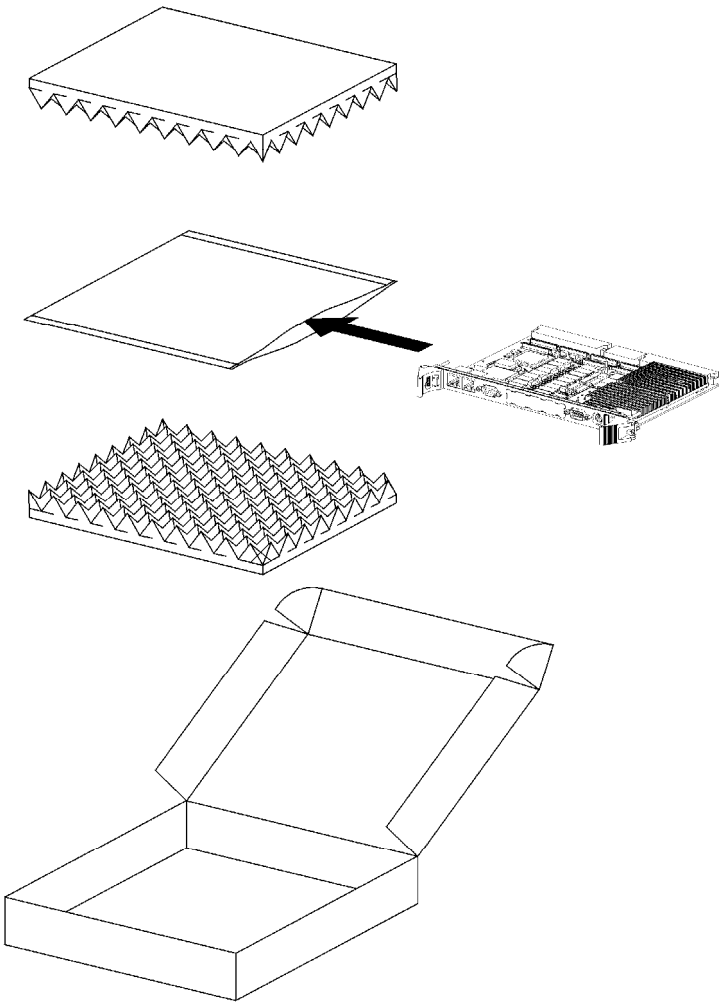


Figure 1: Board packaging

Handling

Proper handling of the board or module is critical to ensure proper operation and long-term reliability. When unpacking the board, and whenever handling it thereafter, be sure to hold the board by the front panel as shown. Do not hold the board by the circuit card edges, the heat sink, or the connectors.

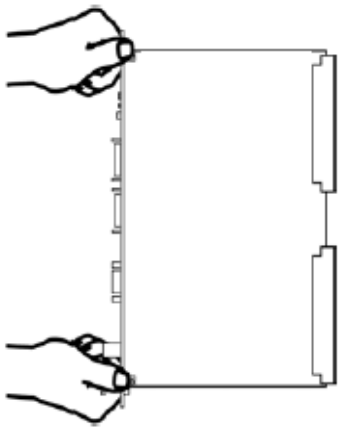


Figure 2: Handling a 6U VME board

CHAPTER 3 Hardware Installation

Chapter Scope

The VG5 is a single slot VME controller equipped with either dual PowerPC 7455/57 or single PowerPC 7455/57 processors. It is equipped with all functions which a conventional system controller can only offer with several add-on cards. Extension boards can be connected via the VME interface and 2 PMC interfaces. The minimized board size and the large number of interfaces and functions enable the VG5 for use in many applications.

Installation preparation

Use the following steps to install your GE Intelligent Platforms hardware.

General Advisories

1. Before installing or removing any board, please ensure that the system power and external supplies have been turned off.
2. Check that the jumpers and piggybacks are correctly configured for your application.
3. Mount the board/piggyback/transition module very carefully. See also additional advisories for VMEbus and CompactPCI products below.
4. Connect all IO cables.
5. Once you are certain that all modules are correctly fitted into the system and all connections have been made properly, restore the power.

General Advisories

Before installing or removing any board, please ensure that the system power and external supplies have been turned off.

Check that jumpers and mezzanines are correctly configured for your application. Mount the board, mezzanine, or transition module very carefully. See also sections on additional advisories below.

Do not restore power until you are sure that all modules are fitted correctly and all connections have been made properly.

Advisories for VMEbus products

On a standard VMEbus backplane, remove the jumpers on the IACKIN - IACKOUT interrupt daisy-chain (1 jumper) and on the BGxIN - BGxOUT busgrant daisy-chains (4 jumpers) for the slot where the board is to be mounted. The daisy-chain jumpers on the VMEbus backplane should be mounted on all free slots.

Setting jumpers is not necessary for the GE Intelligent Platforms Auto-Daisy-Chain VMEbus backplane (order number: VBUSxxAD). Please read additional advisories within the manual.
A board with system controller functionality must be fitted at slot 1 (for GE Intelligent Platforms products, see additional notes within the manual).

The backplane must supply +3.3 V and +5 V.

Because the board is available in several options the description in this chapter is related to the standard configuration.

Caution



Requirement for the used power supply:
Only for VG5 lower than version 2.x:
5 V and 3.3 V must be powered on / off simultaneously (<5 ms)

Required items

The following items are required to start the board in a standard configuration:

Backplane and Power Supply

You will need a standard CompactPCI or VMEbus backplane wired into a regulated power supply capable of providing stable low noise +5 V, + 3.3 V and +12 V sources. Make sure that the supply is capable of meeting the total power requirements of the board. Please refer to chapter ‘Specifications’ for details.

Some CPCI boards feature Full Hot Swap capabilities according to the PCI Hot Plug specification PICMG 2.1. This allows orderly insertion and extraction of the board from the system host (backplane) without having to power down the system. Please note that this feature requires that Hot Swap functions are also available on the backplane. See chapter ‘Hot Swap’ for details.

Initially, you may plug the board into your 3U or 6U system slot of your CPCI or VMEbus system. Optionally, when used as an intelligent peripheral board, this board can also be used in a non-system slot. In case that the board is used in a non-system slot you have to have an additional CPU board in the system slot for providing system clock, arbiter function and more. Please make sure that you do not have the power supply turned ON when the board is plugged into your backplane.

Advice on Batteries

There is no battery on this board.

Installation of a plug-in board

Boards are installed in a CPCI or VMEbus chassis by carefully sliding them into the guide rails, inserting them all the way until the handles can be operated to seat and lock the board in place. Handles typically have a lock (snap lever) to unlock them when extracting a board. Older boards may have screws instead of handles to secure the board in place.

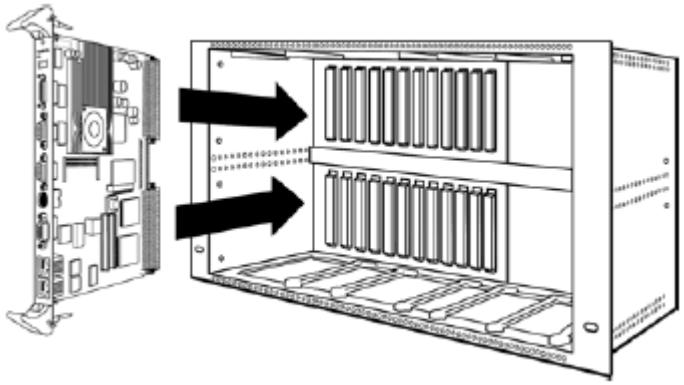


Figure 3: 6U board insertion into VMEbus system box

Block Diagram Dual Node

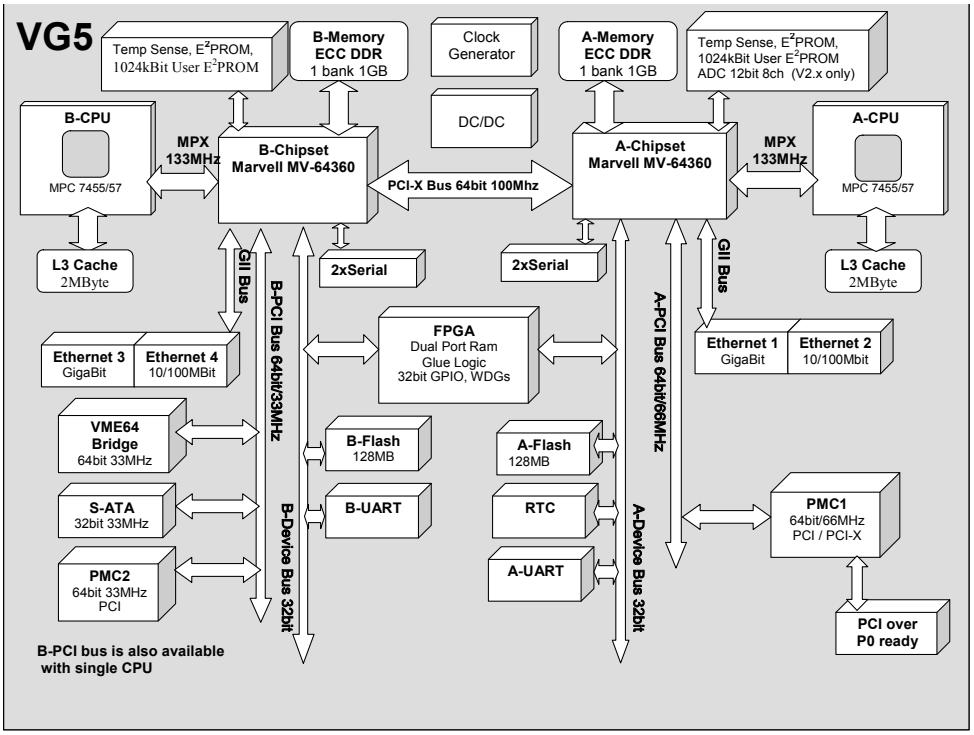


Figure 1: VG5 Block Diagram (Dual Node)

Block Diagram Single Node

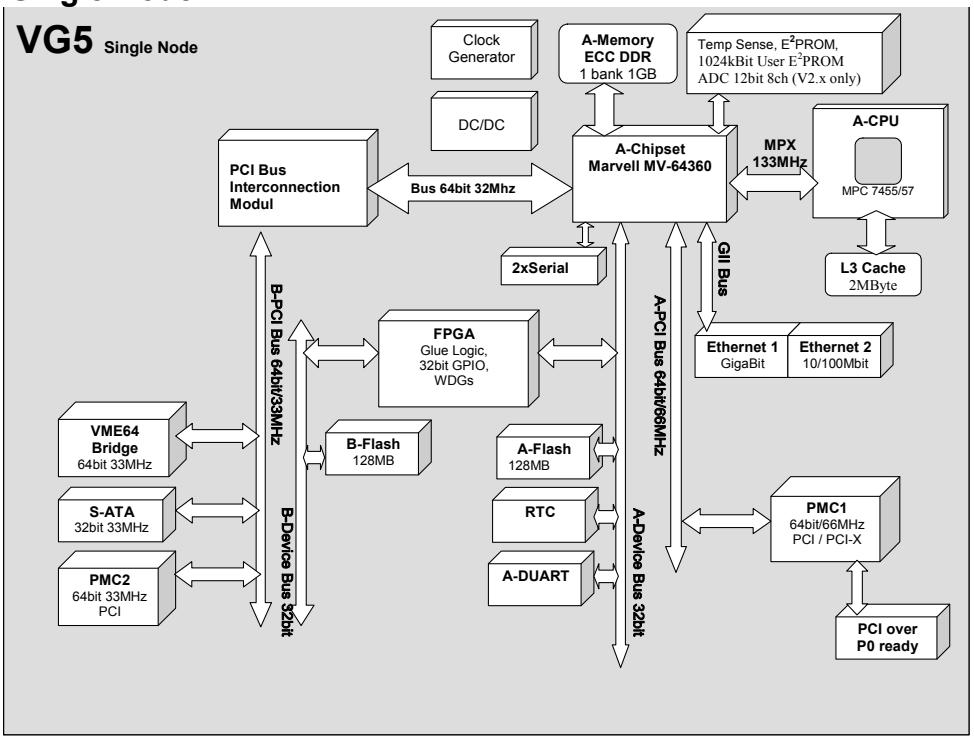


Figure 2: VG5 Block Diagram (Single Node)

Placement Plan VG5 Board Version V1.x

Top Side VG5 V1.x

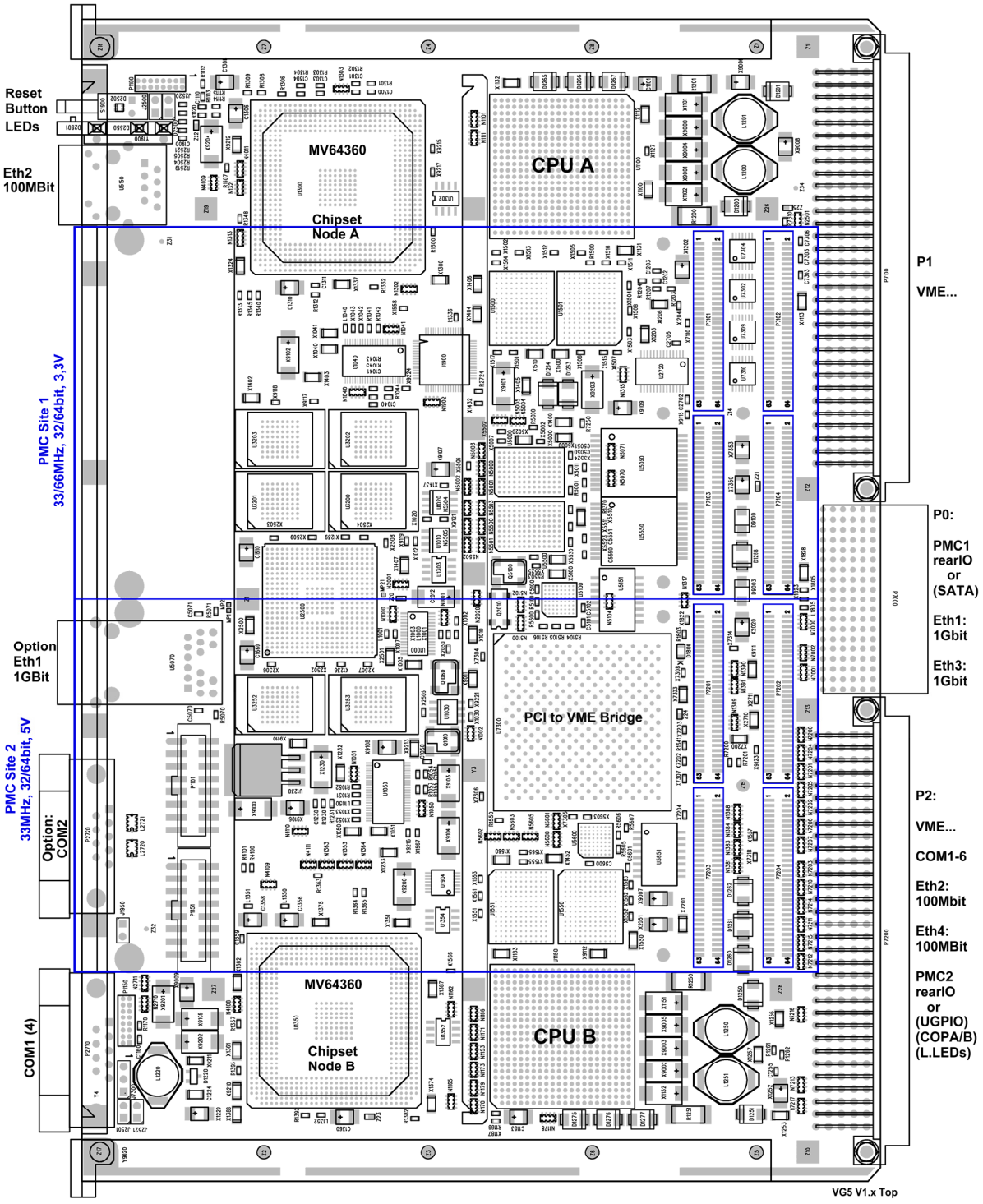


Figure 3: Placement Top Side (VG5 V1.x)

Bottom Side VG5 V1.x

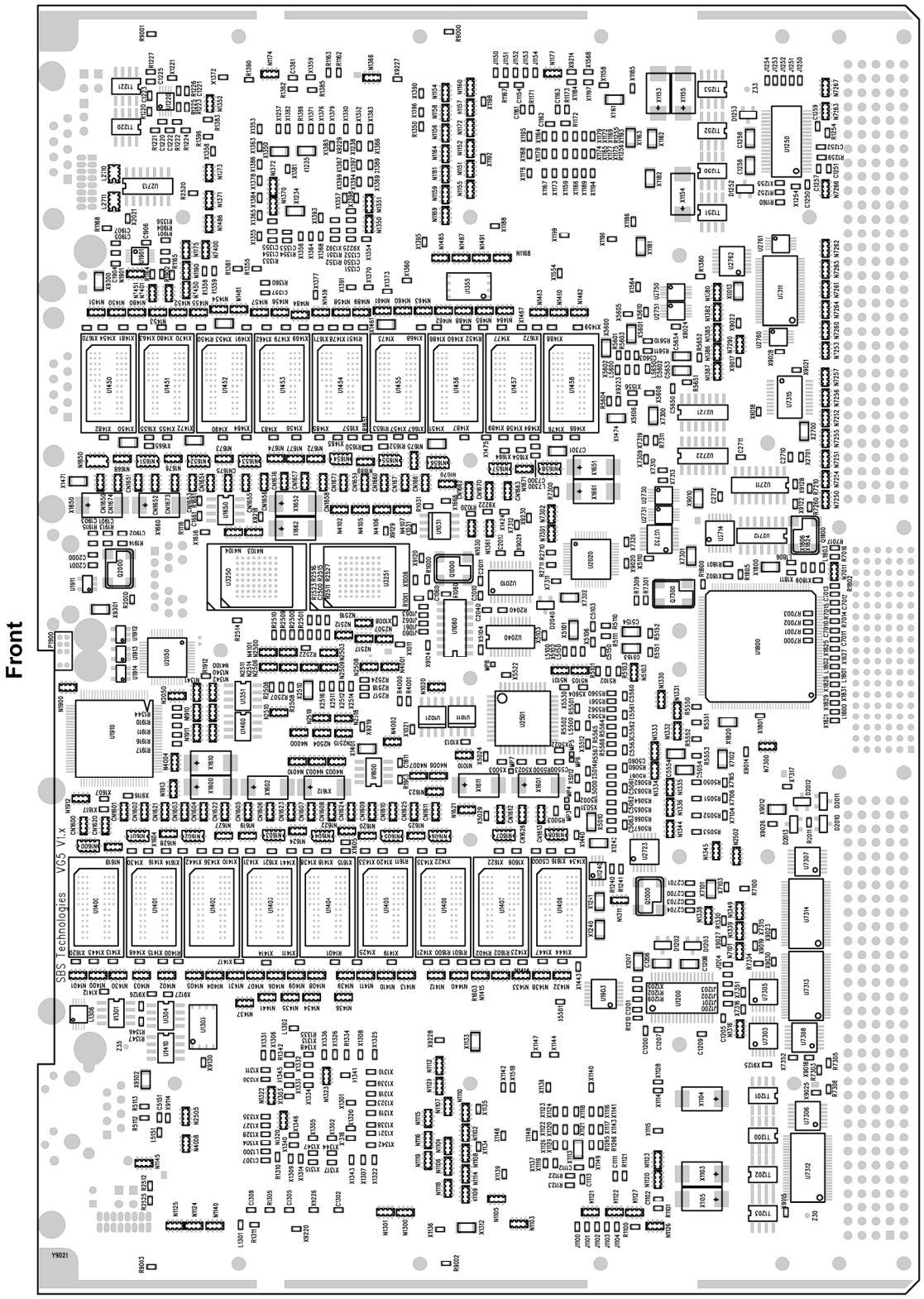


Figure 4: Placement Bottom Side (VG5 V1.x)

Placement Plan VG5 Board Version V2.x

Top Side VG5 V2.x

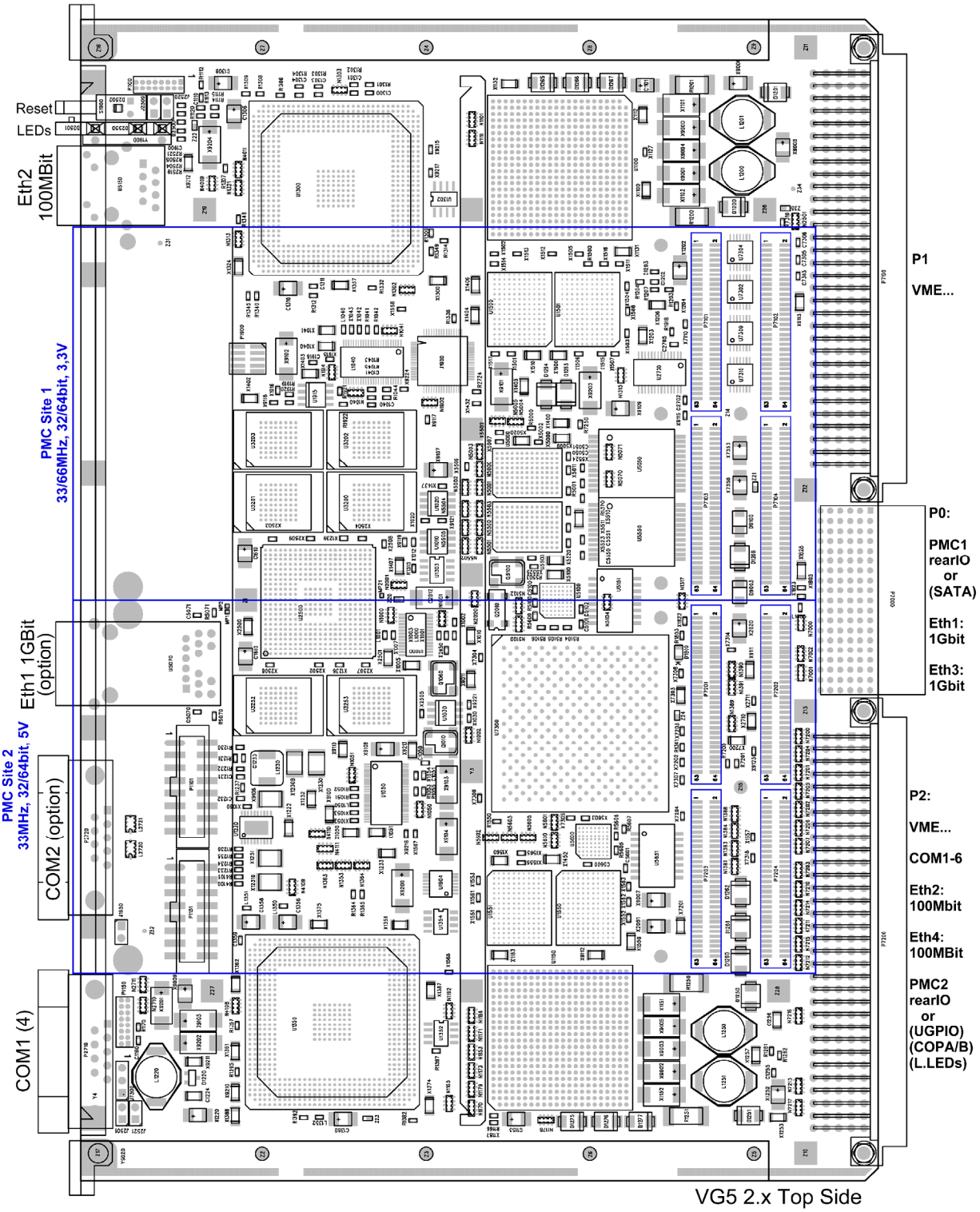
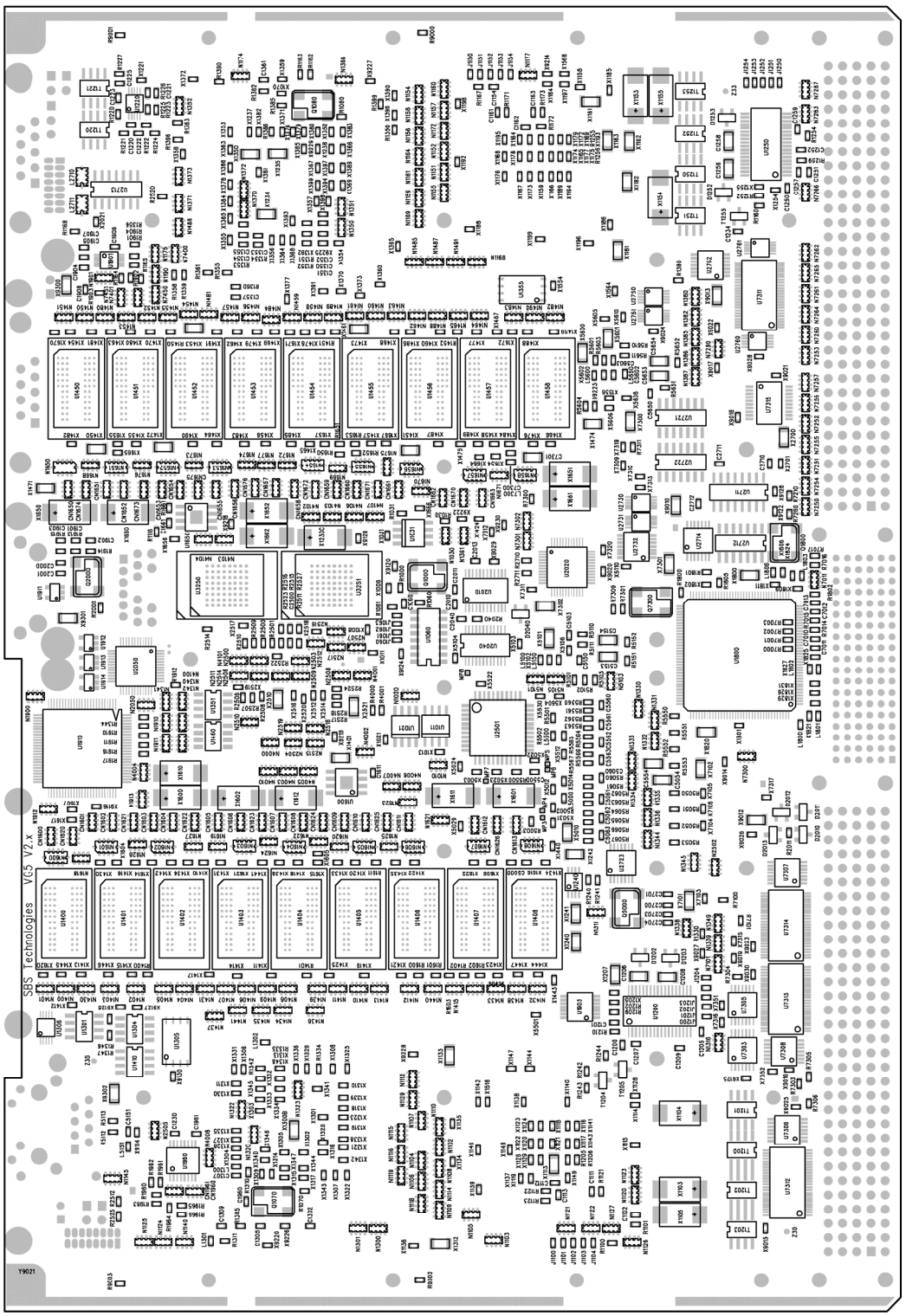


Figure 5: Placement Top Side (Vg5 V2.x)

Bottom Side VG5 V2.x



VG5 2.x Bottom Side

Figure 6: Placement Bottom Side (VG5 V2.x)

Placement Plan VG5 Board Version V3.x

Top Side VG5 V3.x

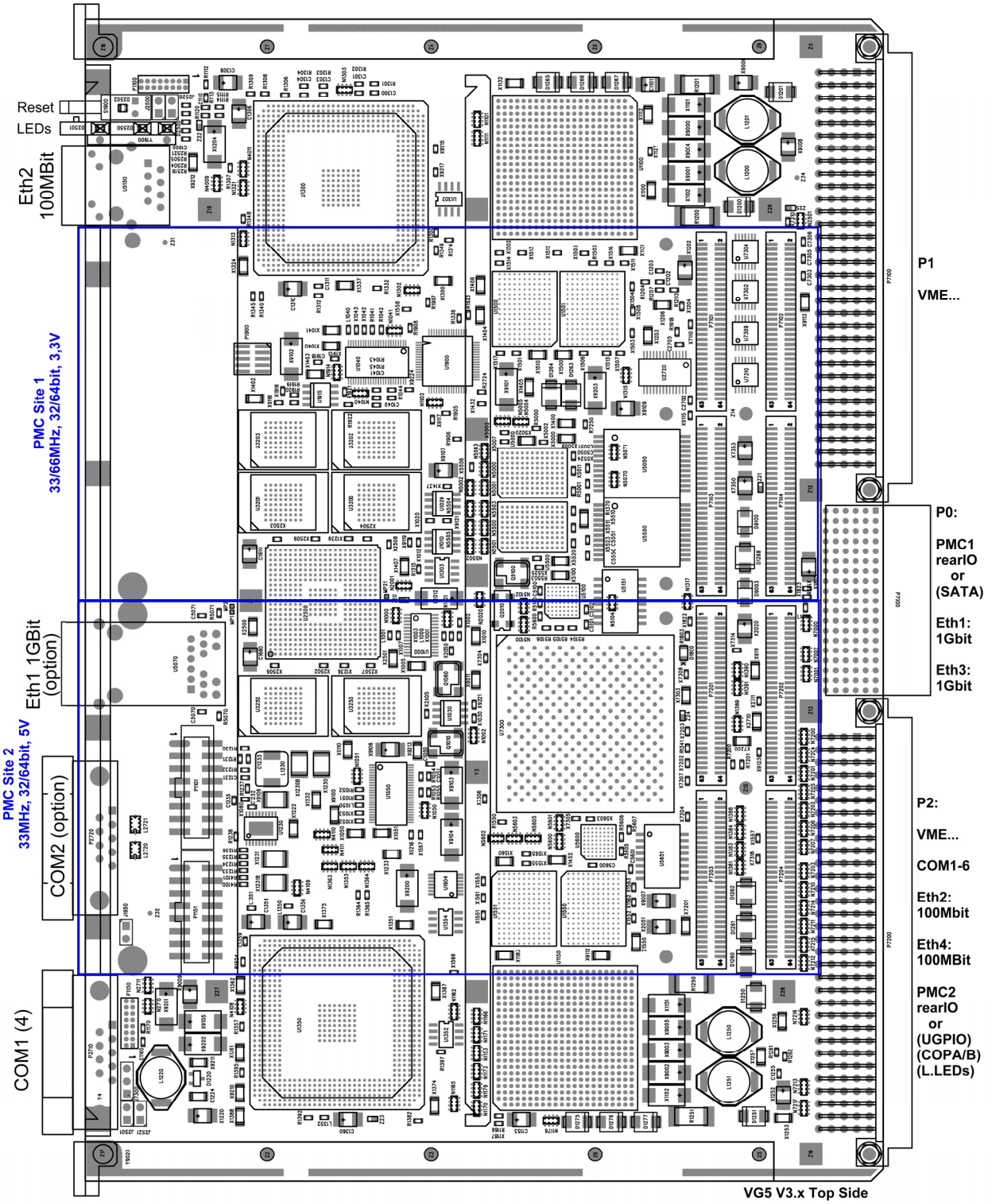


Figure 7: Placement Top Side (VG5 V3.x)

Bottom Side VG5 V3.x

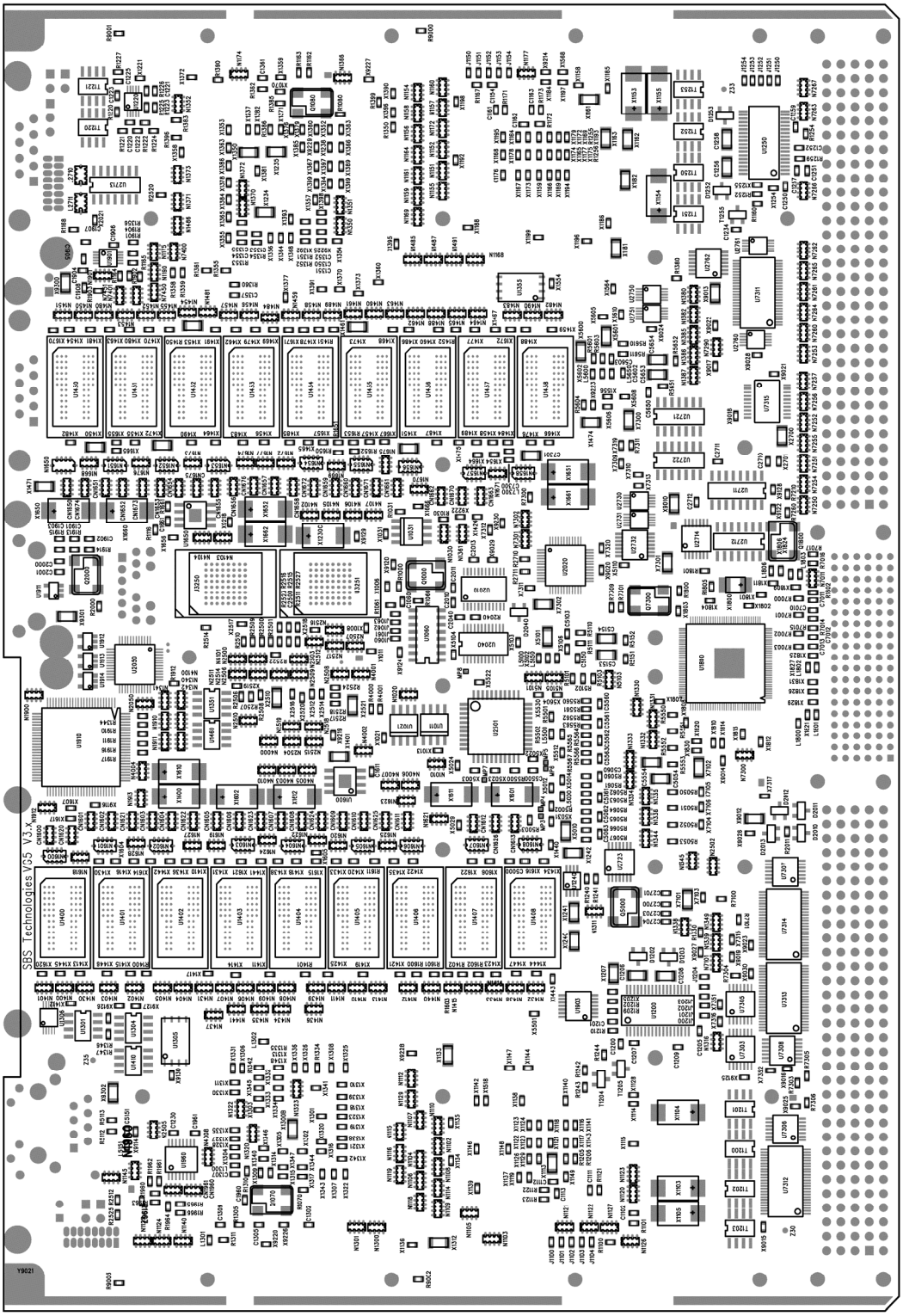


Figure 8: Placement Bottom Side (VG5 V3.x)

Front Panel

VG5 with two front Ethernet ports, two front COM ports and one PMC site:

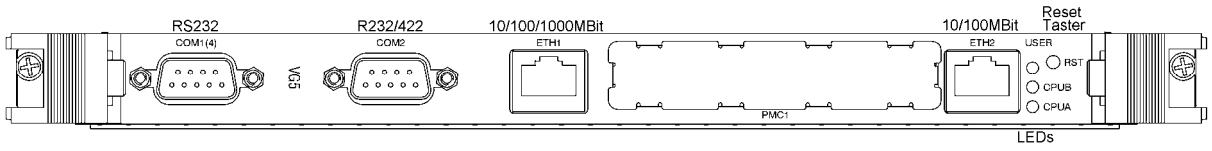


Figure 9: Front Panel with one PMC site

VG5 with one front Ethernet port, on front RS232 COM port and two PMC sites:

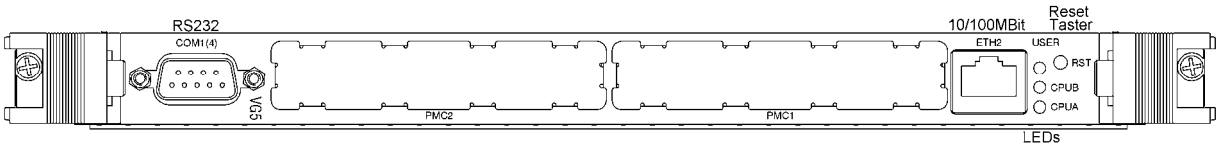


Figure 10: Front Panel with two PMC sites

Socket Installation

There are several accessible jumpers on the VG5.

VME Reset Jumper

The jumper J7300 defines the strategy for VMEbus resets.
See also chapter Non-volatile Switches for further details.

Table 2: VME Reset Jumper J7300 (VG5 V1.0 - V1.2)

For VG5 V1.0 – V1.2

J7300 1-2	J7300 2-3	J7300 open
"Software Mode" Via Software Command programmable, if VME reset is *always* or *never* generated by VG5	VMEbus reset always generated (factory default setting)	VMEbus reset is never generated

Usage in "Software Mode":

At PMON (Version up to #6) command prompt:

With command: `vmerstsw [on | off]`

`on` enables the VME Reset by VG5

`off` disables the VME Reset by VG5

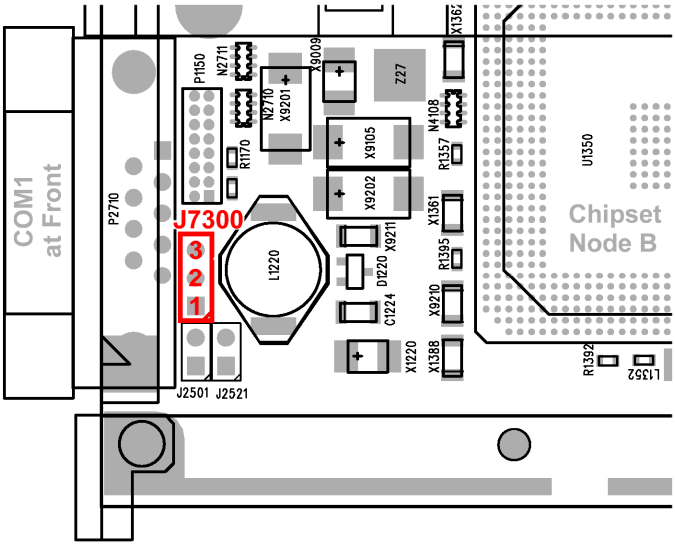


Figure 11: Location of VME-Reset Jumper J7300 (VG5 V1.0-V1.2)

Hint:
If you are using PMON#7 in a V1.0 - V1.2 board, the `vmerstsw` or `vmesysclk` commands will not be available in PMON – the J7300 software mode will not be available.

Use the J7300 command instead of `vmesysclk`. Be aware, that this is a workaround.

If the VG5 is the system controller (located in slot 0) type `J7300 close12` at pmon#7 prompt.
The VG5 will provide the VMESYSCLK.
Then set the reset strategy with the J7300 Hardware jumper (see Table 2: 2-3 closed or open)

If the VG5 is not the system controller (another board is plugged in slot 0, e.g. if there are multiple VG5 in one rack) then type: `J7300 open` at pmon#7 prompt.

The VG5 will then not provide a VMESYSCLK.
Then set the reset strategy with the J7300 Hardware jumper (see Table 2: 2-3 closed or open)

The VG5 V1.0-V1.2 boards can also be easily upgraded to V1.3 at the GE Intelligent Platforms factory.
See also chapter Non-volatile Switches for more details.

Table 3: VME Reset Jumper J7300 (VG5 V1.3 and higher)

J7300 1-2	J7300 2-3	J7300 open
"Software Mode" default (soldered bridge in 1-2)		

For VG5 V1.3 and higher

Usage in "Software Mode":

At PMON (Version #7 and higher) command prompt:

With command:
`J7300 [close12 | close23 | open]`

`close12` VG5 can generate VME reset if it is the system controller (first populated VME slot)

`close23` VG5 can always generate a VME reset

`open` disables the VME reset by VG5

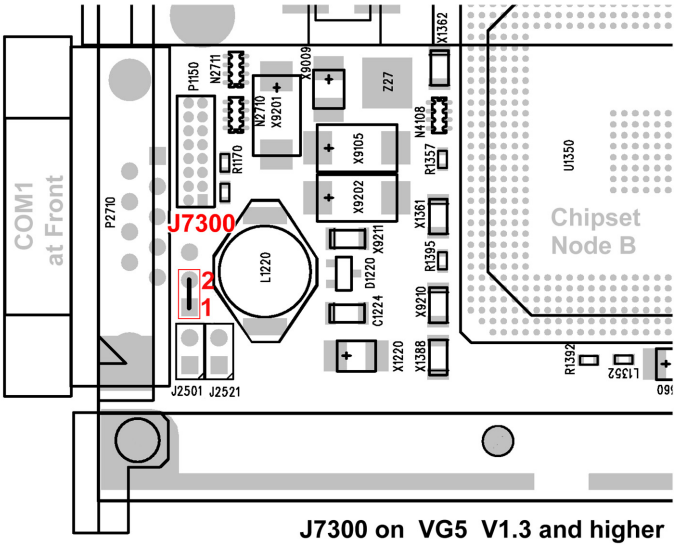


Figure 12: Location of VME-Reset Jumper J7300 (VG5 V1.3 and higher)

See also chapter Non-volatile Switches for more details.

Bootselect Jumper

The jumpers J2520 and J2521 select the booting source of Node A and B. Not mounted in conduction cooled version (N-, 8-style). Both Bootselect jumpers are available at rear IO too. The boot behaviour depends on the software installed in the emergency boot flash (Flashbank 1). The boot software is responsible for the evaluation of the BOOTSEL jumper.
Due to limited pins at P0/P2 the boot select signals share the function with the card fail LEDs of CPU A and CPU B. If a jumper is closed the program will read the status of the boot select function, after this read function the signal will be an output and controls the card fail LEDs. That means if a jumper is closed the LED is in on-state as long as the jumper is installed. The LED output is protected against this short circuit.

Table 4: Bootselect Jumper J2520, J2521

J2520 open	**J2520 closed**
Booting from user boot source for CPU A	Booting from emergency boot source for CPU A
J2521 open	**J2521 closed**
Booting from user boot source for CPU B	Booting from emergency boot source for CPU B

VG5 Version V1.x and higher

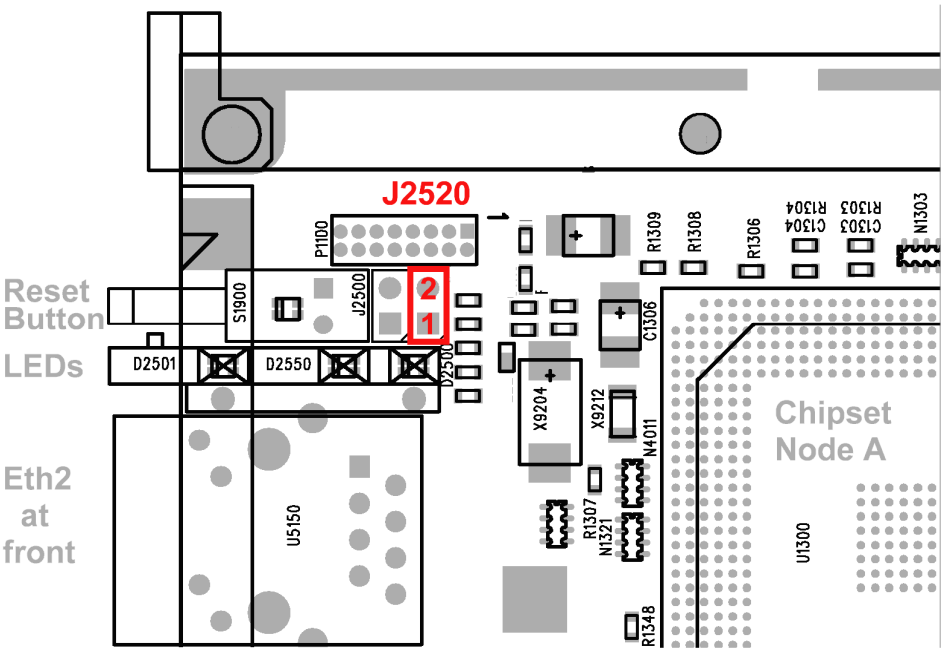


Figure 13: Location of Node A Bootselect Jumper J2520 , (VG5 V1.x and higher)

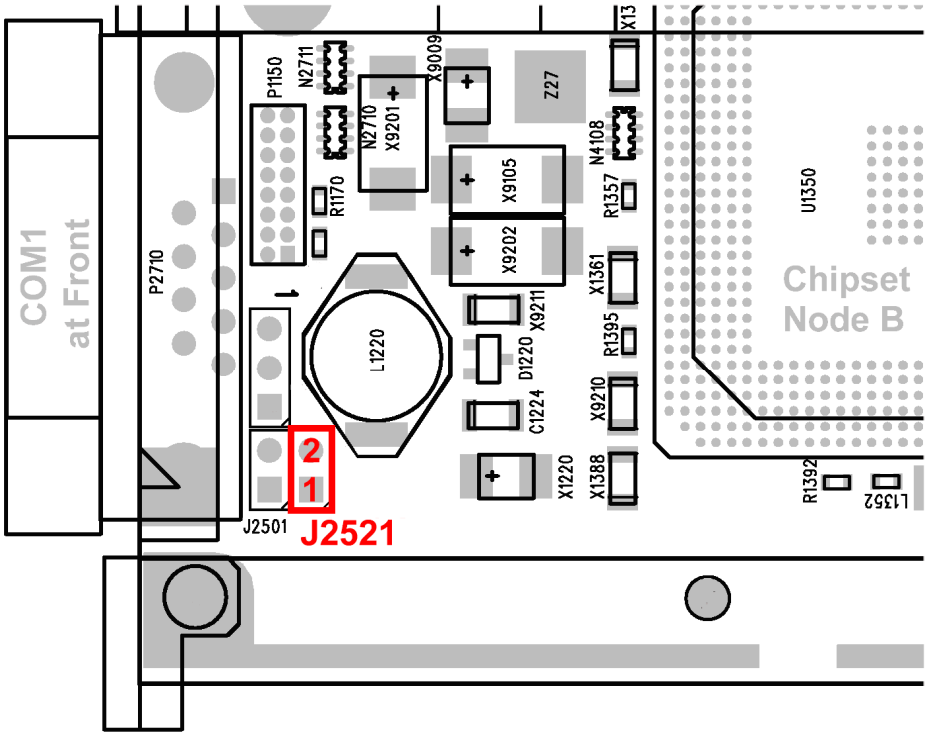


Figure 14: Location of Node B Bootselect Jumper J2521 , (VG5 V1.x and higher)

Watchdog Jumper

Jumpers J2500 and J2501 define the Watchdog functions.
They are not mounted in conduction cooled versions (N-, 8-style).

Table 5: Watchdog Jumpers J2500, J2501

J2500 open	**J2500 closed**
Watchdog-Reset for Node A is enabled after hard reset (factory default setting)	Watchdog-Reset for Node A is disabled after hard reset and can not be activated by software
J2501 open	**J2501 closed**
Watchdog-Reset for Node B is enabled after hard reset (factory default setting)	Watchdog-Reset for Node B is disabled after hard reset and can not be activated by software

See chapter (Watchdog Timer A/B) for more details on watchdogs.

VG5 Version V1.x and higher

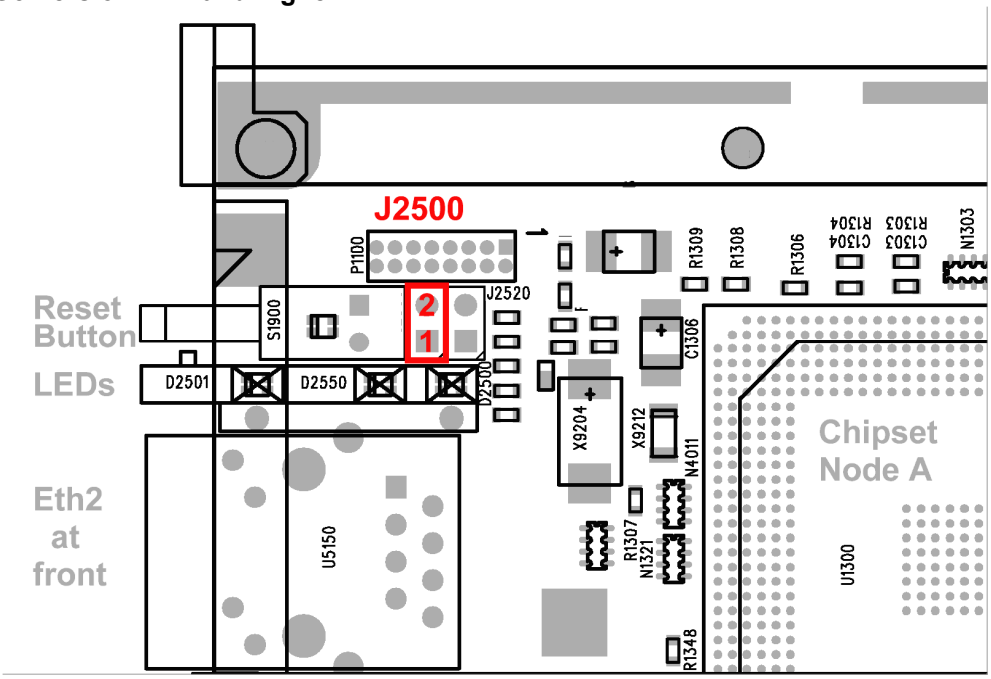


Figure 15: Location of Node A Watchdog Jumper J2500 , (VG5 V1.x and higher)

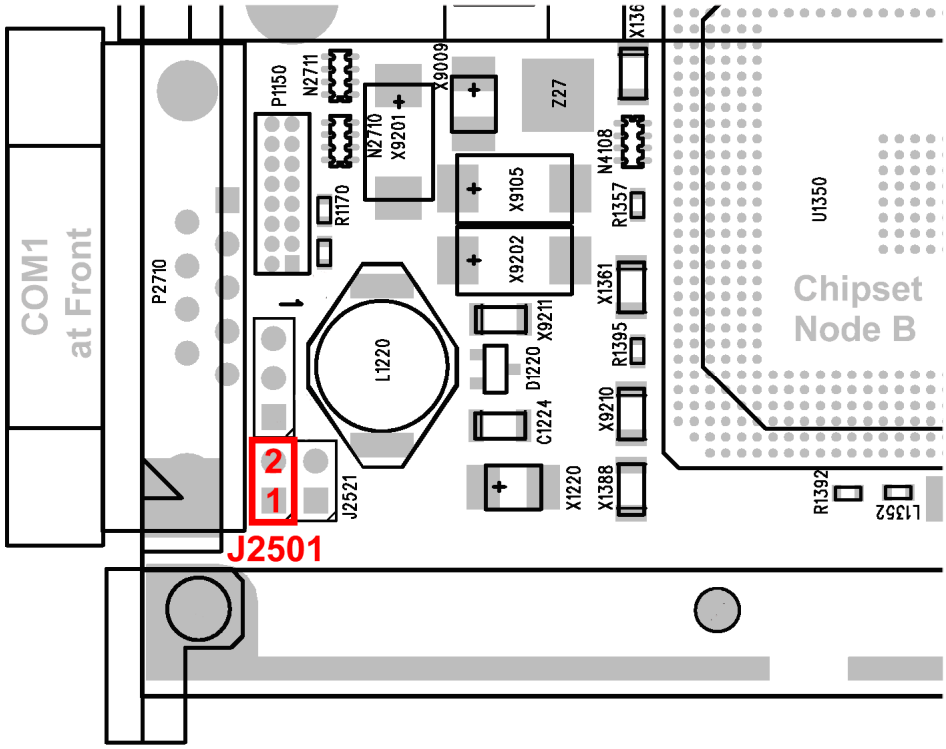


Figure 16: Location of Node B Watchdog Jumper J2501 , (VG5 V1.x and higher)

Flash Write Protect Jumpers (Resistors)

The following jumper resistors (0 Ω) are generally mounted.

Then the software can remove the hardware flash write protection for the boot block or the system block of flash bank1 by clearing the write protection bits FB1_BootWP or FB1_SysWP in the A/B_CNTRLSTAT registers.

After reset or power-on the write protection is switched on.

If the resistors are not mounted the software can never remove the write protection.

The hardware write protection is created with the FPGA. The FPGA checks the device bus for addresses located in the boot block or the system block. If the write protection is on, write accesses to these blocks are not performed.

Be aware that the hardware write protection only works for flash bank1 and only helps against *sector write* or *sector erase* commands. If you perform a *chip erase* command you can delete the flash bank, because the command does not put a sector address on the address bus, which can be detected by the FPGA.

In addition to the hardware write protection you have of course the standard software flash protection. It is very unlikely that a random byte sequence is exactly the command sequence for writing or erasing a sector or the entire chip.

The main danger is that the processor jumps accidentally (because of a software error) in the area were the flash routines are stored – and then writes or erases a sector or even the entire chip.

If you have no chip erase routine in the memory (Flash or DDR-SDRAM), which could be used accidentally, the hardware write protection is quite safe.

R2506 When mounted, the software can remove the write protection of boot block of Node A (upper 1 MByte, see Figure 26)
(see also Table 26: A_FB1_BootWP bit in A_CNTRLSTAT Register)

R2507 When mounted, the software can remove the write protection of the system block of Node A (upper 8 MByte, see Figure 26)
(see also Table 26: A_FB1_SysWP bit in A_CNTRLSTAT Register)

R2508 When mounted, the software can remove the write protection of the boot block of Node B (upper 1 MByte, see Figure 26)
(see also Table 27: B_FB1_BootWP bit in B_CNTRLSTAT Register)

R2509 When mounted, the software can remove the write protection of the system block of Node B (upper 8 MByte, see see Figure 26)
(see also Table 27: B_FB1_SysWP bit in B_CNTRLSTAT Register)

VG5 Version V1.x and higher

Bottom side of VG5 board, near centre:

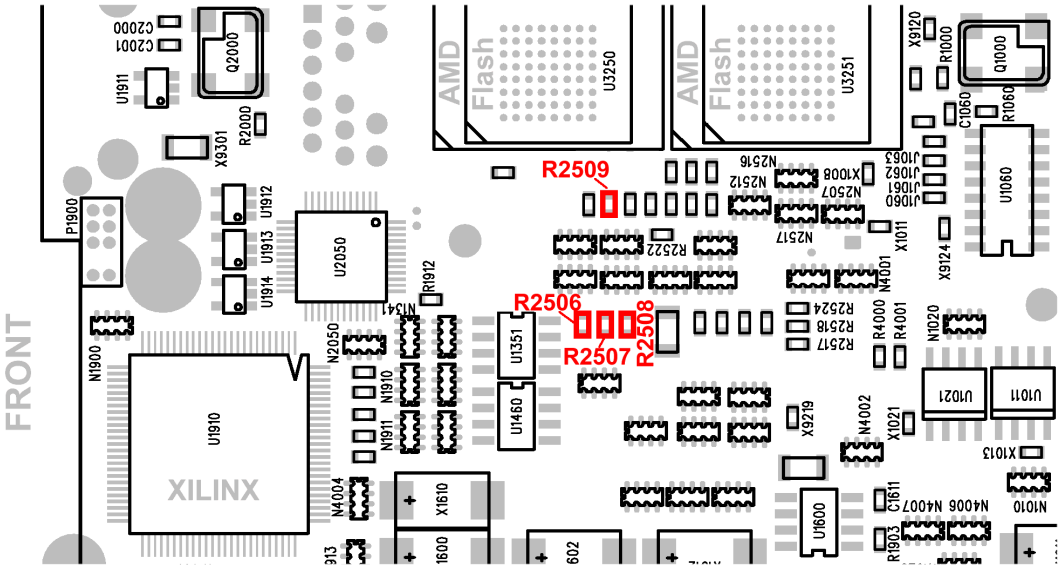


Figure 17: Location of Write Flash Protection Jumpers (SMD Resistors) (VG5 V1.x and higher)

Clocking

The clock scheme of the VG5 is very flexible. The main clock is a 133 MHz clock for CPU, CPU bus, and device bus with FPGA and DDR memory. The CPU core clock is a multiple of the main clock.

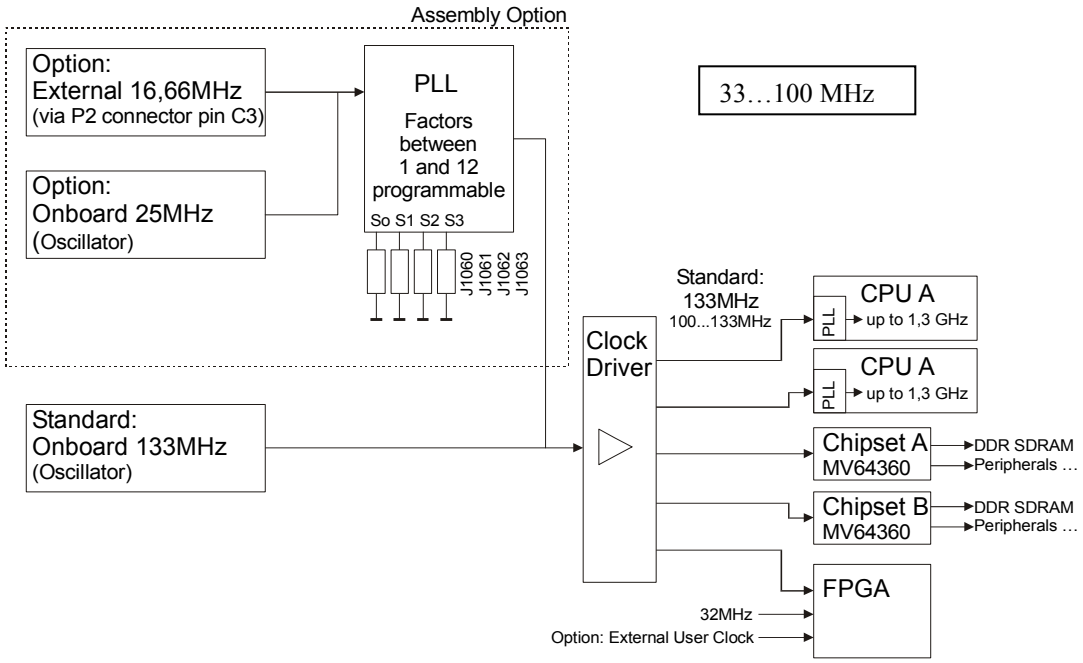


Figure 18: Main Clock Tree

Each PCI bus has its own clock which is completely independent from the other PCI bus or the main clock. The frequencies of the PCI buses are self-selectable (depending on the used configuration and PMC card) in steps between 33..133 Mhz.

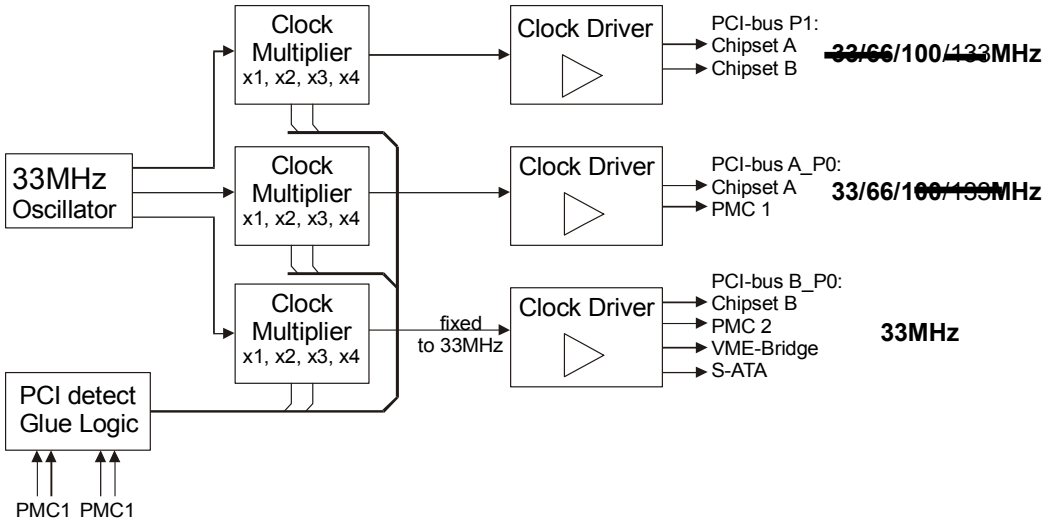


Figure 19: PCI Bus Clocks

Interfaces and Connectors on the VG5

The connectors P0, P1 and P2 carry the signals for the VMEbus as well as all the IO signals of the VG5. For easy connection of the IO signals to standard connectors a transition module is available from GE Intelligent Platforms. The order number for the transition module is "VTM20".

Pin Description for the following tables:

Signal groups:

PMC IO signals of Slot 1:	PMC1_IO…
PMC IO signals of Slot 2:	PMC2_IO…
COM1, COM2, ... signals:	C1....., C2.....,
User General Purpose IO	UGpio_...
Node A Gigabit Ethernet signals:	Eth1_…
Node A Fast Ethernet signals:	Eth2_…
Node B Gigabit Ethernet signals:	Eth3_…
Node B Fast Ethernet signals:	Eth4_…

VME signals: VME....
Serial ATA channel: ATA_...

Remarks to the Gigabit LAN-Port signal names:
Gigabit Ethernet has 4 differential pairs per Port, e.g. for Eth1:

Eth1_DA ±	used in 100 Mbit mode as	TxD± located on P0
Eth1_DB ±	used in 100 Mbit mode as	RxD±
Eth1_DC ±		
Eth1_DD ±		
Eth1_LED	link LED	located on P2

Gigabit Ethernet has 4 differential pairs per Port, e.g. for Eth3:

Eth3_DA ±	used in 100 Mbit mode as	TxD± located on P0
Eth3_DB ±	used in 100 Mbit mode as	RxD±
Eth3_DC ±		
Eth3_DD ±		
Eth3_LED	link LED	located on P2

VMEbus Connector P1 (P7100)

The following table lists the pin assignments of connector P1. The connector is compatible to the P1 connector of the VMEbus specification VME64 VITA 1-1994 and VME64 Extension VITA 1.1-1997.

Table 6: P1 Connector

	z	a	b	c	d
1	rsv	D00	BBSY#	D08	+5 V (VPC)
2	GND	D01	BCLR#	D09	GND
3	rsv	D02	ACFAIL#	D10	rsv
4	GND	D03	BG0IN#	D11	rsv
5	rsv	D04	BG0OUT#	D12	rsv
6	GND	D05	BG1IN#	D13	rsv
7	rsv	D06	BG1OUT#	D14	rsv
8	GND	D07	BG2IN#	D15	rsv
9	rsv	GND	BG2OUT#	GND	GAP#
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#
11	rsv	GND	BG3OUT#	BERR#	GA1#
12	GND	DS1#	BR0#	SYSRESET#	+3,3 V
13	rsv	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	+3,3 V
15	rsv	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	+3,3 V
17	rsv	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	+3,3 V
19	rsv	GND	AM3	A19	rsv
20	GND	IACK#	GND	A18	+3,3 V
21	rsv	IACKIN#	rsv	A17	rsv
22	GND	IACKOUT#	rsv	A16	+3,3 V
23	rsv	AM4	GND	A15	rsv
24	GND	A07	IRQ7#	A14	+3,3 V
25	rsv	A06	IRQ6#	A13	rsv
26	GND	A05	IRQ5#	A12	+3,3 V
27	rsv	A04	IRQ4#	A11	rsv
28	GND	A03	IRQ3#	A10	+3,3 V
29	rsv	A02	IRQ2#	A09	rsv
30	GND	A01	IRQ1#	A08	+3,3 V
31	rsv	-12 V	+5 V STDBY	+12 V	GND
32	GND	+5 V	+5 V	+5 V	+5 V (VPC)

☞ If the ACFAIL* function is not driven by the power supply, ACFAIL* should be strapped to VCC on the VMEbus backplane to avoid spurious interrupts caused by cross talking.

☞ For explanation of signals see VMEbus specification.

VMEbus Connector P2 (P7200)

The following table lists the pin assignments of connector P2. Row b of the connector is compatible to connector P2 of the VMEbus specification VME64 VITA 1- 1994 and VME64 Extension VITA 1.1-1997. Row a and c complies to VITA 35-2000 PMC-P4 to VME-P2 rows a and c (P4V2-64ac), optionally row a and c may alternatively be used by VG5 specific signals.

Table 7: P2 Connector

☞ See chapter Pin Description for the following tables: for pin name description

	z	a PMCIO or VG5 function::		b	c PMCIO or VG5 function:			d user defined
		VG5_Func.	PMC2_IO		VG5_Func.		PMC2_IO	
1	C2_DCD/TXD-	Eth1_LED	PMC2_IO02	+5 V	Eth3_LED		PMC2_IO01	Eth2_TxD-
2	GND	Eth2_LED	PMC2_IO04	GND	Eth4_LED		PMC2_IO03	Eth2_TxD+
3	C2_DSR/TXD+	CPUVIO	PMC2_IO06	rsv	WDG_REL	EXT16.66 MHz	PMC2_IO05	Eth2_RxD-
4	GND	ACOP_HRST#	PMC2_IO08	VMEA24	BCOP_HRST#		PMC2_IO07	Eth2_RxD+
5	LED A#/BOOTSEL	ACOP_SRST#	PMC2_IO10	VMEA25	BCOP_SRST#		PMC2_IO09	C2_CTS/RXC-/CTS-
6	GND	ACHKSTP_OUT#	PMC2_IO12	VMEA26	BCHKSTP_OUT#		PMC2_IO11	C2_TXD/RXC+/CTS+
7	LED B#/BOOTSEL	ACOP_TCK	PMC2_IO14	VMEA275	BCOP_TCK	JTAG_TCK	PMC2_IO13	C2_RXD/TXC-/RTS-
8	GND	ACOP_TDI	PMC2_IO16	VMEA28	BCOP_TDI	JTAG_TDI	PMC2_IO15	C2_RTS/TXC+/RTS+
9	C1_RxD	ACOP_TMS	PMC2_IO18	VMEA29	BCOP_TMS	JTAG_TMS	PMC2_IO17	C2_RXD-
10	GND	ACOP_TRST	PMC2_IO20	VMEA30	BCOP_TRST#	JTAG_TRST#	PMC2_IO19	C2_DTR/RXD+
11	C1_TxD	ACOP_TDO	PMC2_IO22	VMEA31	BCOP_TDO	JTAG_TDO	PMC2_IO21	Eth4_TxD-
12	GND	AQREQ#	PMC2_IO24	GND	BQREQ#		PMC2_IO23	Eth4_TxD+
13	C4_RxD	AQACK#	PMC2_IO26	+5 V	BQACK#		PMC2_IO25	Eth4_RxD-
14	GND	ACHKSTP_IN#	PMC2_IO28	VMED16	BCHKSTP_IN#		PMC2_IO27	Eth4_RxD+
15	C4_TxD	-	PMC2_IO30	VMED17	-		PMC2_IO29	C3_RxD-
16	GND	-	PMC2_IO32	VMED18	-		PMC2_IO31	C3_RxD+
17	C6_RxD-	UGPIO0	PMC2_IO34	VMED19	UGPIO16		PMC2_IO33	C3_RXC-/CTS-
18	GND	UGPIO1	PMC2_IO36	VMED20	UGPIO17		PMC2_IO35	C3_RXC+/CTS+
19	C6_RxD+	UGPIO2	PMC2_IO38	VMED21	UGPIO18		PMC2_IO37	C3_TXC-/RTS-
20	GND	UGPIO3	PMC2_IO40	VMED22	UGPIO19		PMC2_IO39	C3_TXC+/RTS+
21	C6_RXC-/CTS-	UGPIO4	PMC2_IO42	VMED23	UGPIO20		PMC2_IO41	C3_TxD-
22	GND	UGPIO5	PMC2_IO44	GND	UGPIO21		PMC2_IO43	C3_TxD+
23	C6_RXC+/CTS+	UGPIO6	PMC2_IO46	VMED24	UGPIO22		PMC2_IO45	C5_RXC-/CTS-
24	GND	UGPIO7	PMC2_IO48	VMED25	UGPIO23		PMC2_IO47	C5_RXC+/CTS+
25	C6_TXC-/RTS-	UGPIO8	PMC2_IO50	VMED26	UGPIO24		PMC2_IO49	C5_TXC-/RTS-
26	GND	UGPIO9	PMC2_IO52	VMED27	UGPIO25		PMC2_IO51	C5_TXC+/RTS+
27	C6_TXC+/RTS+	UGPIO10	PMC2_IO54	VMED28	UGPIO26		PMC2_IO53	C5_TxD-
28	GND	UGPIO11	PMC2_IO56	VMED29	UGPIO27		PMC2_IO55	C5_TxD+
29	C6_TxD-	UGPIO12	PMC2_IO58	VMED30	UGPIO28		PMC2_IO57	C5_RxD-
30	GND	UGPIO13	PMC2_IO60	VMED31	UGPIO29		PMC2_IO59	C5_RxD+
31	C6_TxD+	UGPIO14	PMC2_IO62	GND	UGPIO30		PMC2_IO61	GND
32	GND	UGPIO15	PMC2_IO64	+5 V	UGPIO31		PMC2_IO63	+5 V (VPC)

VMEbus Connector P0 (P7000)

The pin assignment of the Gigabit Ethernet signals complies with VITA31.1-2000 (Giga Ethernet on VME64 backplanes). The mapping of PMC IO follows the VITA 35 2000 (PMC-P4 Pin Out Mapping To VME-P0 and VME64x-P2) as long as not violated by VITA 31.1.
That means PMC 1_IO 01...PMC1_ IO25 doesn't comply with VITA 35. Optionally some PMC1 IO pins may alternatively be used by Serial ATA signals (unique to VG5).

Table 8: P0 Connector

	a	b		c		d		e		f
1	GND	GND		GND		GND		GND		GND
2	**ETH1_DA+**	**ETH1_DA-**		GND		**ETH1_DC+**		**ETH1_DC-**		GND
3	**ETH1_DB+**	**ETH1_DB-**		GND		**ETH1_DD+**		**ETH1_DD-**		GND
4	**ETH3_DA+**	**ETH3_DA-**		GND		**ETH3_DC+**		**ETH3_DC-**		GND
5	**ETH3_DB+**	**ETH3_DB-**		GND		**ETH3_DD+**		**ETH3_DD-**		GND
6	GND	GND		GND		GND		GND		GND
7	PMC1_IO05	PMC1_IO04		PMC1_IO03		PMC1_IO02		PMC1_IO01		GND
8	PMC1_IO10	PMC1_IO09		PMC1_IO08		PMC1_IO07		PMC1_IO06		GND
9	PMC1_IO15	PMC1_IO14		PMC1_IO13		PMC1_IO12		PMC1_IO11		GND
10	PMC1_IO20	PMC1_IO19		PMC1_IO18		PMC1_IO17		PMC1_IO16		GND
11	PMC1_IO25	PMC1_IO24		PMC1_IO23		PMC1_IO22		PMC1_IO21		GND
12	PMC1_IO30	PMC1_IO29		PMC1_IO28		PMC1_IO27		PMC1_IO26		GND
13	PMC1_IO35	PMC1_IO34		PMC1_IO33		PMC1_IO32		PMC1_IO31		GND
14	PMC1_IO40	PMC1_IO39		PMC1_IO38		PMC1_IO37		PMC1_IO36		GND
15	PMC1_IO45	PMC1_IO44		PMC1_IO43		PMC1_IO42		PMC1_IO41		GND
16	PMC1_IO50	PMC1_IO49		PMC1_IO48		PMC1_IO47		PMC1_IO46		GND
17	PMC1_IO55	P1_IO54	GND	P1_IO53	GND	P1_IO52	GND	P1_IO51	GND	GND
18	PMC1_IO60	P1_IO59	GND	P1_IO58	ATA_TX+	P1_IO57	GND	P1_IO56	ATA_RX-	GND
19	RST_BUT#	P1_IO64	GND	P1_IO63	ATA_TX-	P1_IO62	GND	P1_IO61	ATA_RX+	GND

☞ See chapter Pin Description for the following tables: for pin name description

PMC Slot 1 connectors (P7101, P7102, P7103)

The following table lists the pin assignments of the onboard PMC1 connector. The PMC slot is 64-bit and can operate at PCI-33, PCI-66 and is connected to the first PCI bus of Node A. The PMC is electrically and mechanically compliant to the specification IEEE 1386 and IEEE 1386.1 with enhancements to the Processor PMC Standard VITA 32-199x. The VG5 enhancements provide pins for a second device (IDSELB and REQB/GNTB), but doesn't support a monarch PMC card.

Table 9: PMC Slot 1 Connectors

P7101	P7102	P7103	Pin	Pin	P7101	P7102	P7103
TCK	+12 V	rsv	**01**	**02**	-12 V	TRST#	GND
GND	TMS	GND	**03**	**04**	A_INTB#(inta#)	TDO	C/BE7#
A_INTC# (intb#)	TDI	C/BE6#	**05**	**06**	A_INTD#(intc#)	GND	C/BE5#
PRESENT#	GND	C/BE4#	**07**	**08**	+5 V	rsv	GND
A_INTA# (intd#)	rsv	V(IO)	**09**	**10**	rsv	rsv	PAR64
GND	PUP	AD63	**11**	**12**	+3.3 Vaux	+3.3 V	AD62
PCICLK	PCIRST#	AD61	**13**	**14**	GND	PDN	GND
GND	+3.3 V	GND	**15**	**16**	GNT1#	PDN	AD60
REQ1#	PME#	AD59	**17**	**18**	+5 V	GND	AD58
V(IO)	AD30	AD57	**19**	**20**	AD31	AD29	GND
AD28	GND	V(IO)	**21**	**22**	AD27	AD26	AD56
AD25	AD24	AD55	**23**	**24**	GND	+3.3 V	AD54
GND	AD30(idsel)	AD53	**25**	**26**	C/BE3#	AD23	GND
AD22	+3.3 V	GND	**27**	**28**	AD21	AD20	AD52
AD19	AD18	AD51	**29**	**30**	+5 V	GND	AD50
V(IO)	AD16	AD49	**31**	**32**	AD17	C/BE2#	GND
FRAME#	GND	GND	**33**	**34**	GND	AD29(idselb)	AD48
GND	TRDY#	AD47	**35**	**36**	IRDY#	+3.3 V	AD46
DEVSEL#	GND	AD45	**37**	**38**	+5 V	STOP#	GND
PCIXCAP	PERR#	V(IO)	**39**	**40**	LOCK#	GND	AD44
rsv	+3.3 V	AD43	**41**	**42**	rsv	SERR#	AD42
PAR	C/BE1#	AD41	**43**	**44**	GND	GND	GND
V(IO)	AD14	GND	**45**	**46**	AD15	AD13	AD40
AD12	M66EN	AD39	**47**	**48**	AD11	AD10	AD38
AD9	AD8	AD37	**49**	**50**	+5 V	+3.3 V	GND
GND	AD7	GND	**51**	**52**	C/BE0#	REQ2#	AD36
AD6	+3.3 V	AD35	**53**	**54**	AD5	GNT2#	AD34
AD4	rsv	AD33	**55**	**56**	GND	GND	GND
V(IO)	rsv	V(IO)	**57**	**58**	AD3	EREADY	AD32
AD2	GND	rsv	**59**	**60**	AD1	RESETOUT#	rsv
AD0	ACK64#	rsv	**61**	**62**	+5 V	+3.3 V	GND
GND	GND	GND	**63**	**64**	REQ64#	rsv	rsv

nc	Not connected
rsv	Reserved. Do not connect anything
V(IO)	IO Voltage, connected to +3,3 V
+12 V/-12 V	Only available if connected at the VME backplane
PUP	Weak 10 kΩ pull-up to VIO
PDN	Weak 10 kΩ pull-down to GND

PMC Slot 2 connectors (P7201, P7202)

PMC2 is only available without the front Ethernet and/or front COM2 (P2720) connector.
The following table lists the pin assignments of the onboard PMC2 connector. The PMC slot is 64-bit and PCI 33 MHz capable and is connected to the first PCI bus of Node B. In single node configuration this bus is connected to the second PCI bus of Node A. The PMC is electrically and mechanically compliant to the specification IEEE 1386 and IEEE 1386.1 with enhancements to the Processor PMC Standard VITA 32-199x. The enhancements provide pins for a second device (IDSELB and REQB/GNTB) but don't support a monarch PMC card.

Table 10: PMC Slot 2 Connectors

P7201	P7202	P7203	Pin	Pin	P7201	P7202	P7203
TCK	+12 V	rsv	**01**	**02**	-12 V	TRST#	GND
GND	TMS	GND	**03**	**04**	B_INTC#(inta#)	TDO	C/BE7#
B_INTD# (intb#)	TDI	C/BE6#	**05**	**06**	B_INTA#(intc#)	GND	C/BE5#
PRESENT#	GND	C/BE4#	**07**	**08**	+5 V	rsv.	GND
B_INTB# (intd#)	rsv	V(IO)	**09**	**10**	rsv	rsv	PAR64
GND	PUP[1)]	AD63	**11**	**12**	+3.3 Vaux	+3.3 V	AD62
PCICLK	PCIRST#	AD61	**13**	**14**	GND	PDN	GND
GND	+3.3 V	GND	**15**	**16**	GNT1#	PDN	AD60
REQ1#	PME#	AD59	**17**	**18**	+5 V	GND	AD58
V(IO)	AD30	AD57	**19**	**20**	AD31	AD29	GND
AD28	GND	V(IO)	**21**	**22**	AD27	AD26	AD56
AD25	AD24	AD55	**23**	**24**	GND	+3.3 V	AD54
GND	AD29(idsel)	AD53	**25**	**26**	C/BE3#	AD23	GND
AD22	+3.3 V	GND	**27**	**28**	AD21	AD20	AD52
AD19	AD18	AD51	**29**	**30**	+5 V	GND	AD50
V(IO)	AD16	AD49	**31**	**32**	AD17	C/BE2#	GND
FRAME#	GND	GND	**33**	**34**	GND	AD29(idselb)	AD48
GND	TRDY#	AD47	**35**	**36**	IRDY#	+3.3 V	AD46
DEVSEL#	GND	AD45	**37**	**38**	+5 V	STOP#	GND
GND	PERR#	V(IO)	**39**	**40**	LOCK#	GND	AD44
rsv	+3.3 V	AD43	**41**	**42**	rsv	SERR#	AD42
PAR	C/BE1#	AD41	**43**	**44**	GND	GND	GND
V(IO)	AD14	GND	**45**	**46**	AD15	AD13	AD40
AD12	M66EN	AD39	**47**	**48**	AD11	AD10	AD38
AD9	AD8	AD37	**49**	**50**	+5 V	+3.3 V	GND
GND	AD7	GND	**51**	**52**	C/BE0#	REQ2#	AD36
AD6	+3.3 V	AD35	**53**	**54**	AD5	GNT2#	AD34
AD4	rsv	AD33	**55**	**56**	GND	GND	GND
V(IO)	rsv	V(IO)	**57**	**58**	AD3	EREADY	AD32
AD2	GND	rsv	**59**	**60**	AD1	RESETOUT#	rsv
AD0	ACK64#	rsv	**61**	**62**	+5 V	+3.3 V	GND
GND	GND	GND	**63**	**64**	REQ64#	rsv	rsv

nc	Not connected
rsv	Reserved. Do not connect anything
V(IO)	IO Voltage, connected with +5 V
+12 V/-12 V	Only available if connected at the VME backplane.
PUP	Weak 10 kΩ pull-up to VIO
PDN	Weak 10 kΩ pull-down to GND

PMC-IO connector (P7104 and P7204)

The VG5 provides all PMC IO of both PMC slots at the rear connector. These PMC IO signals can be accessed via connectors at the transition module VTM20 (see CHAPTER 5 Transition Module VTM20, depends on VG5 configuration). The pinning of PMC1 IO and PMC2 IO are the same for both.

Table 11: PMC1/2 IO Connector

Pin	P7104/P7204 (Pn4)		Pin
01	PMCx_IO01	PMCx_IO02	02
03	PMCx_IO03	PMCx_IO04	04
05	PMCx_IO05	PMCx_IO06	06
07	PMCx_IO07	PMCx_IO08	08
09	PMCx_IO09	PMCx_IO10	10
11	PMCx_IO11	PMCx_IO12	12
13	PMCx_IO13	PMCx_IO14	14
15	PMCx_IO15	PMCx_IO16	16
17	PMCx_IO17	PMCx_IO18	18
19	PMCx_IO19	PMCx_IO20	20
21	PMCx_IO21	PMCx_IO22	22
23	PMCx_IO23	PMCx_IO24	24
25	PMCx_IO25	PMCx_IO26	26
27	PMCx_IO27	PMCx_IO28	28
29	PMCx_IO29	PMCx_IO30	30
31	PMCx_IO31	PMCx_IO32	32
33	PMCx_IO33	PMCx_IO34	34
35	PMCx_IO35	PMCx_IO36	36
37	PMCx_IO37	PMCx_IO38	38
39	PMCx_IO39	PMCx_IO40	40
41	PMCx_IO41	PMCx_IO42	42
43	PMCx_IO43	PMCx_IO44	44
45	PMCx_IO45	PMCx_IO46	46
47	PMCx_IO47	PMCx_IO48	48
49	PMCx_IO49	PMCx_IO50	50
51	PMCx_IO51	PMCx_IO52	52
53	PMCx_IO53	PMCx_IO54	54
55	PMCx_IO55	PMCx_IO56	56
57	PMCx_IO57	PMCx_IO58	58
59	PMCx_IO59	PMCx_IO60	60
61	PMCx_IO61	PMCx_IO62	62
63	PMCx_IO63	PMCx_IO64	64

COP Interface Connectors (P1100, P1150)

Each of the two CPUs has its own COP interface for debugging.
P1100 is dedicated to CPU A and P1150 to CPU B.

P1100 and P1150 are 16 pin connectors (1.27 mm pitch) but only accessible on the board – not at the VG5 front panel . For connecting a compatible 2.54 mm pitch connector an adapter is necessary.

The used connector is a Samtec FTSH-108-01-L-D, check www.samtec.com for available counterparts.

Optionally, if the PMC Site 2 is not assembled, there are the connectors P1101 and P1151 with 2.54 mm pitch and equal pin assignments as their relatives with 1.27 mm pitch.

Table 12: P1100 A-COP, P1101 B-COP

Signal	P1100 (opt. P1101)		Signal
ACOP_TDO	1	2	A_QACK#
ACOP_TDI	3	4	A_COP_TRST#
A_QREQ#	5	6	VIO Sense (2.5 V)
ACOP_TCK	7	8	CHKSTOP_IN#
ACOP_TMS	9	10	NC
A_COP_SRESET#	11	12	NC
A_COP_HRESET#	13	14	NC (Key)
A_CHKSTOP_OUT#	15	16	GND

Signal	P1150 (opt. P1151)		Signal
BCOP_TDO	1	2	B_QACK#
BCOP_TDI	3	4	B_COP_TRST#
B_QREQ#	5	6	VIO Sense (2.5 V)
BCOP_TCK	7	8	CHKSTOP_IN#
BCOP_TMS	9	10	NC
B_COP_SRESET#	11	12	NC
B_COP_HRESET#	13	14	NC (Key)
B_CHKSTOP_OUT#	15	16	GND

The COP interface signals are also available at the P2 connector but are shared with other signals, please see P2 pin listing in Table 7 for configuration.

➔ No COP-Signals are available on P2, when the VG5 is configured with a PMC2 rear IO.

COP interface pull-up and pull-down resistors are provided on the VG5 board. The following table list the used resistor values.

Table 13: COP Terminations

Signal	Resistor Value, pull-up or pull down
\COP_HRESET	1 kΩ, pull-up 2.5 V
\COP_SRESET	1 kΩ, pull-up2.5 V
COP_TMS	10 kΩ, pull-up 2.5 V
COP_TCK	10 kΩ, pull-up 2.5 V
\COP_TRST	1 kΩ, pull-down GND
COP_TDI	10 kΩ, pull-up 2.5 V
\CHKSTOP	10 kΩ, pull-up 2.5 V
VIO Sense	100 Ω serial resistor to 2.5 V

VG5 Version V1.x and higher

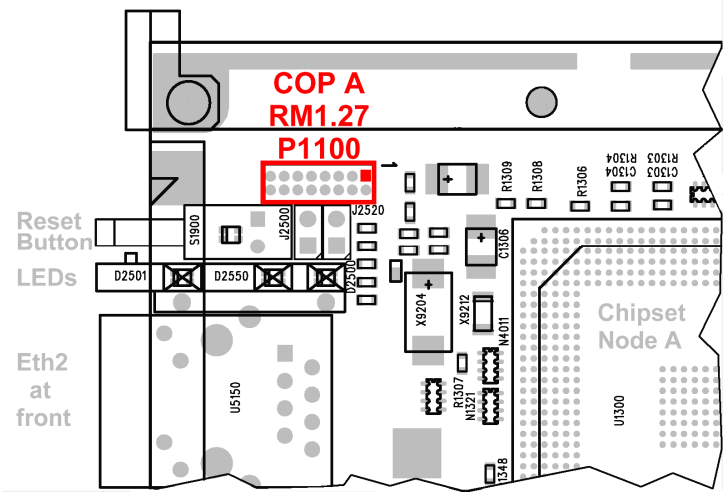


Figure 20: COP A P1100 Connector Location (VG5 v1.x and higher)

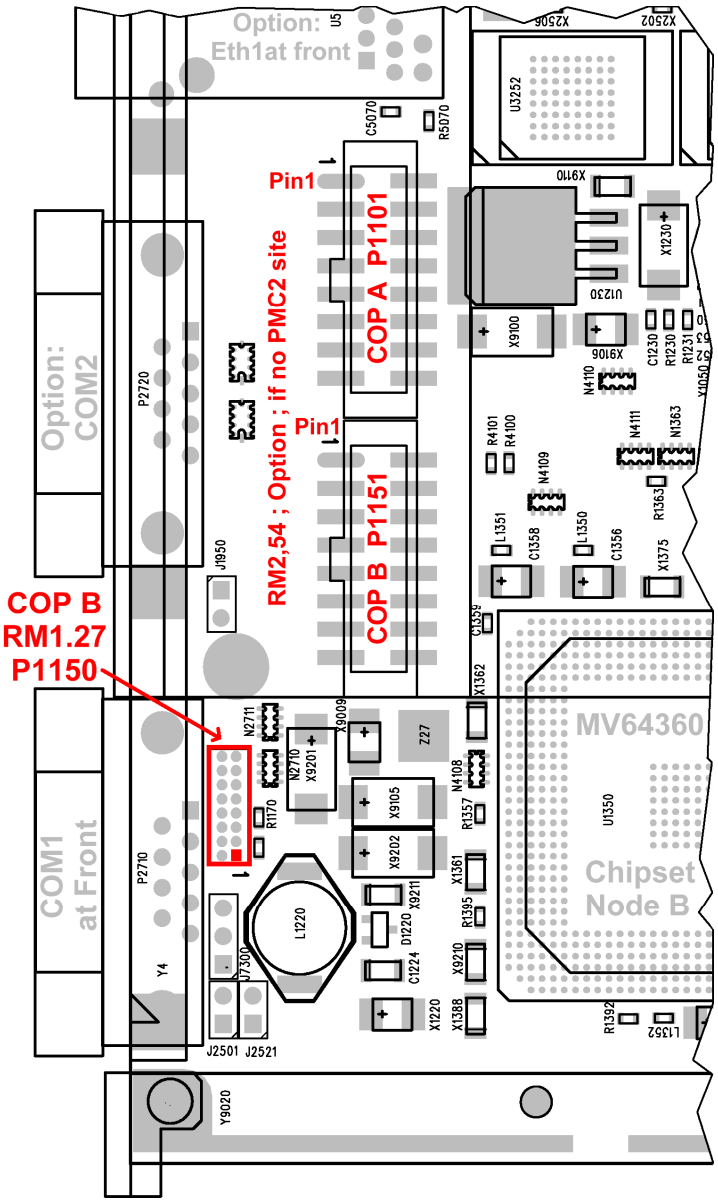


Figure 21: COP B P1150 Connector Location (+Opt. P1101,P1151) (VG5 V1.x and higher)

JTAG Interface

A JTAG interface is available for testing the connected devices according to IEEE1149.1. Please call the factory for details of how to order board-specific JTAG software.
The JTAG interface signals are available at the P2 connector but are shared with other signals (see P2 pin listing).

PCI-IDSEL

Each PCI device has a unique PCI address/data signal connected to the IDSEL input. The following table provides the IDSEL on the VG5 board for the three separate PCI buses (dual

node) respectively two PCI buses (single node). First or second IDSEL are designated **idsel** or **idselb** respectively

Table 14: a-e: PCI-IDSEL

Dual Node PCI 0 of Node A:

IDSEL	Device
AD31	Chipset PCI 0 Controller of Node A
AD30	First IDSEL of PMC1 (**idsel**)
AD29	Second IDSEL of PMC1 (**idselb**)

Dual Node PCI 1 Interconnection Node A/B:

IDSEL	Device
AD31	Chipset PCI 1 Controller of Node A
AD30	Chipset PCI 1 Controller of Node B

Dual Node PCI 0 of Node B:

IDSEL	Device
AD31	Chipset PCI 0 Controller of Node B
AD30	VMEbus Controller
AD29	First IDSEL of PMC2 (**idsel**)
AD28	Second IDSEL of PMC2 (**idselb**)
AD27	SATA Controller

Single Node PCI 0 of Node A:

IDSEL	Device
AD31	Chipset PCI 0 Controller of Node A
AD30	First IDSEL of PMC1 (**idsel**)
AD29	Second IDSEL of PMC1 (**idselb**)

Single Node PCI 1 of Node A:

IDSEL	Device
AD31	Chipset PCI 1 Controller of Node AB
AD30	VMEbus Controller
AD29	First IDSEL of PMC2 (**idsel**)
AD28	Second IDSEL of PMC2 (**idselb**)
AD27	SATA Controller

Remark:
IDSEL is driven High during a Configuration Access – so for a Configuration Read on e.g. the VMEbus Controller, AD30 of PCI0 Node B has to be set to logic 1 during the address phase, when C/BE# = CFG-RD,
see PCI Spec. for details.

Interrupts

On the VG5 board two chip devices perform interrupt handling with integrated interrupt controllers, these are the MV64360 chipsets and the FPGA. The master IRQ controller is the chipset for each node. The FPGA has a small IRQ controller for each node included, which extends the IRQ controller of the chipset. Sources of interrupts may be any of the following:

MV64360 Chipset Intern:
CPU, DRAM, Device Interface, integrated SRAM, PCI0/1, Ethernet0/1, IDMA, Timers, Serial Communication controllers (MPSC0/1), SDMA, Baud Rate Generators, GPP, TWSI

MV64360 Chipset extern:
PCI buses INTA/B/C/D, VME Bridge, S-ATA, FPGA-IRQ

managed by FPGA:
RTC, UGPIO, Thermo Sensor A/B/C, UART, Watchdog, Dual Port RAM Mailbox IRQ, VMEbus Error IRQ.

The IRQ cause can be determined by querying at first the Main Interrupt Cause Register and then the next in the tree structure of cause registers:

MV64360 Interrupt Cause registers (per Node)
• CPU Cause register
• CPU Doorbell register
• DRAM Cause register
• Device Interface Cause register
• Integrated SRAM Cause register
• PCI0 Cause register
• PCI0 Inbound Cause register
• PCI0 Outbound Cause register
• PCI1 Cause register
• PCI1 Inbound Cause register
• PCI1 Outbound Cause register
• Ethernet Unit Cause register
• Ethernet0 Cause register
• Ethernet1 Cause register
• IDMA Cause register
• Timers Cause register
• Comm Unit Cause register
• MPSC0 Cause register
• MPSC1 Cause register
• SDMA Cause register
• BRG Cause register
• GPP Cause register
• TWSI Cause register

FPGA Cause register:
• A_IRQ_CAUSE register (Node A)
• B_IRQ_CAUSE register (Node B)
• UGPIO: A_IRQEVENT register (Node A)
• UGPIO: B_IRQEVENT register (Node B)

See also the MV64360 datasheet and chapter Interrupt Controller A and Interrupt Controller B and Figure 25.

The MV64360 datasheet is directly available from Marvell, but you have to sign an NDA with Marvell.

Usage of Chipset (MV64360) MPP input pins for interrupts:

Node A: (Dual and Single Node Board)

Table 15: IRQ inputs Node A (MPP of Chipset A)

Chipset A MPP bit	Interrupt Function	Remark
MPP20	A_FPGA_IRQ	Input for normal interrupts coming from FPGA IRQ-Controller A (for example UART, RTC, GPIO...)
MPP16	-	VG5 V1.x: Reserved
	AG0_INT	VG5 V2.x, V3.x : Interrupt Input for Gigabit-Ethernet PHY A
MPP21	AG0_INT	VG5 V1.x : Interrupt Input for Gigabit-Ethernet PHY A
	A_BClkIn	VG5 V2.x, V3.x : Extra input clock for baud rate generator
MPP22	P1_INTA	PCI bus 1 Interrupt A (only for link of Nodes)
MPP23	P1_INTB	PCI bus 1 Interrupt B (only for link of Nodes)
MPP24	A_INTA	Node A PCI bus 0 Interrupt A (PMC1 slot)
MPP25	A_INTB	Node A PCI bus 0 Interrupt B (PMC1 slot)
MPP26	A_INTC	Node A PCI bus 0 Interrupt C (PMC1 slot)
MPP27	A_INTD	Node A PCI bus 0 Interrupt D (PMC1 slot)
MPP28	B_INTA	Node B PCI bus 0 Interrupt A (single node only)
MPP29	B_INTB	Node B PCI bus 0 Interrupt B (single node only)
MPP30	B_INTC	Node B PCI bus 0 Interrupt C (single node only)
MPP31	B_INTD	Node B PCI bus 0 Interrupt D (single node only)

Node B: (Dual Node Board)

Table 16: IRQ inputs Node B (MPP of Chipset B)

Chipset B MPP bit	Interrupt Function	Remark
MPP20	B_FPGA_IRQ	Input for normal interrupts coming from FPGA IRQ-Controller B (for example UART, GPIO...)
MPP16	-	VG5 V1.x: Reserved
	BG0_INT	VG5 V2.x, V3.x : Interrupt Input for Gigabit-Ethernet PHY B
MPP21	BG0_INT	VG5 V1.x : Interrupt Input for Gigabit-Ethernet PHY B
	B_BClkIn	VG5 V2.x, V3.x : Extra input clock for baud rate generator
MPP22	P1_INTB	PCI bus 1 Interrupt A (only for link of Nodes)
MPP23	P1_INTA	PCI bus 1 Interrupt B (only for link of Nodes)
MPP24	-	not used
MPP25	-	not used
MPP26	-	not used
MPP27	-	not used
MPP28	B_INTA	Node B PCI bus 0 Interrupt A (dual node only)
MPP29	B_INTB	Node B PCI bus 0 Interrupt B (dual node only)
MPP30	B_INTC	Node B PCI bus 0 Interrupt C (dual node only)
MPP31	B_INTD	Node B PCI bus 0 Interrupt D (dual node only)

See also chapter FPGA Interrupt Controller A and B and Figure 25 for details to A/B_FPGA_IRQ.

Attention:
Other MPP pins are used for other functions, like MPSC inputs.

Reset

The VG5 has five different sources of reset.

- Power-on reset
- Reset switch
- Watchdog Timer reset
- Reset from the COP debug interface
- VMEbus SYSRESET* signal

The affected devices of the various reset types are listed in the table below:

Table 17: Reset Sources

	Processor Node A	**Chipset Node A**	**PCI Node A**	**Processor Node B**	**Chipset Node B**	**PCI Node B**	**VME bus [1)]**
Power Monitor reset	X	X	X	X	X	X	X
Reset switch	X	X	X	X	X	X	X
Watchdog reset Node A [2)]	X	X	X				
Reset COP interface Node A	X	X	X				
Watchdog reset Node B [2)]				X	X	X	X
Reset COP interface Node B				X	X	X	X
VME SYSRESET	X	X	X	X	X	X	X

1) Depends on VME Reset Strategy configured by J7300 , see chap. VME Reset Jumper.

2) The type of watchdog reset depends on bits A/B_WDGRSTMODE[1:0] in register A/B_CNTRLSTAT
(see chapter Control and Status Register A/B and Watchdog Timer A/B and especially the following sub chapter)

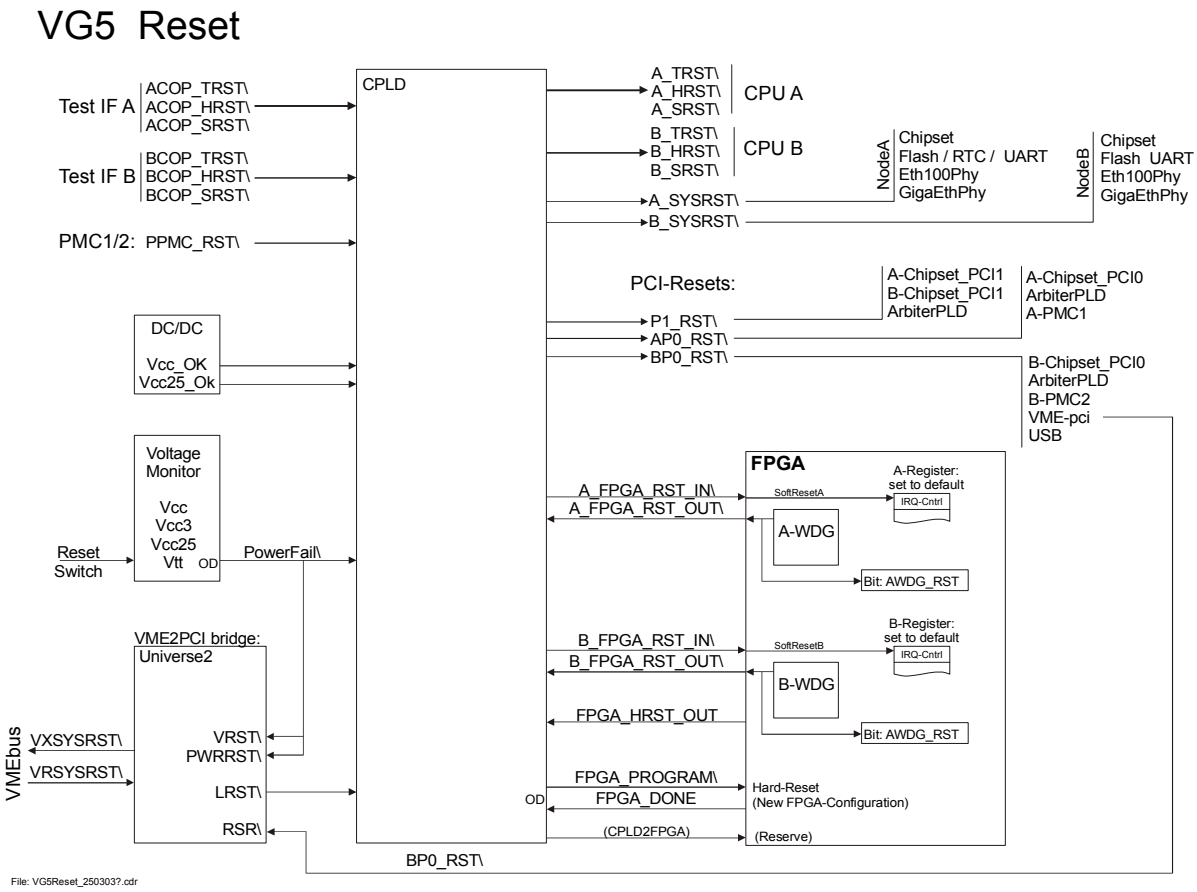


Figure 22: Reset Structure

Hard and Fast Reset

There are two kinds of reset built into the VG5 reset logic: *Hard Reset* and *Fast Reset*

The *Hard Reset* is performing a total board reset – it is like a Power On-Off-On cycle.
The VG5 FPGA is initialized and all its registers are set to default.
In a dual node VG5 both nodes always get the reset. Node A starts after reset automatically – Node B is still in reset until the software on Node A has set the bit A_RESETB in register A_CNTRLSTAT to zero, releasing the reset on Node B (see chapter FPGA Control and Status Register A/B).
The *Hard Reset* takes about 260 ms (200k FPGA) due to the initialization of the FPGA.
At power-on the VG5 is always doing a *hard reset*.

The *Fast Reset* is like the Hard Reset, with the exceptions that the FPGA is not re-initialized and so the reset can be performed in only 1,5...2ms. The next advantage is, that in a dual node VG5 each node (A or B) can be reset individually by the *Fast Reset* (*Fast Reset* A or B).
When using *Fast Reset* the software can recognize, if a reset was generated by a watchdog, by inspecting the expire bits "A/B_WDG1A/B_EXP" in the SYS_IN register (see Table 33).
The *Fast Reset* can only be released by WatchdogA/B built in the FPGA (see chapter FPGA Watchdog Timer A/B).

The software can select between Hard and Fast Reset by setting the A/B_WDGRSTMODE[1:0] bits in the A/B_CNTRLSTAT register (see FPGA Control and Status Register A/B).

Table 18: FPGA Register touched by Fast Reset

A_CNTRLSTAT (Control&Status Register Node A) see Table 26 for all details

Bit	Name	Default	Remark
0	A_WDGRSTMODE0		00 = No reset when Watchdog A expires 01 = A_WDG generates Fast-Reset A when Watchdog A expires
1	A_WDGRSTMODE1	*	10 = A_WDG generates Fast-Reset A and Fast-Reset B 11 = A_WDG generates a hard reset (including FPGA)

B_CNTRLSTAT (Control&Status Register Node B) see Table 27 for all details

Bit	Name	Default	Remark
0	B_WDGRSTMODE0		00 = No reset when Watchdog B expires 01 = B_WDG generates Fast-Reset B when Watchdog B expires
1	B_WDGRSTMODE1	*	10 = B_WDG generates Fast-Reset B and Fast-Reset A 11 = B_WDG generates a hard reset (including FPGA)

Fast Reset A resets all Node A Devices: CPU A, Chipset A, UART A, AP0 PCIbus (PMC1), P1 PCIbus, Eth1/2 Phy,		
The following Node A FPGA registers are touched by Fast Reset :		
FPGA Node A Register	**Value**	**Remark**
A_IRQ_MASK	0x0000	All interrupts in FPGA IRQ Controller A are disabled.
A_CNTRLSTAT	only bits: Bit A_RESETB =0 Bit A_FB1_BootWP =1 Bit A_FB1_SysWP =1	
Fast Reset B resets all Node B Devices: CPU B, Chipset B, UART B, BP0 PCIbus (PMC2), P1 PCIbus, Eth3/4 Phy,		
The following Node B FPGA registers are touched by Fast Reset B:		
FPGA Node B Register	**Value**	**Remark**
B_IRQ_MASK	0x0000	All interrupts in FPGA IRQ Controller B are disabled.
B_CNTRLSTAT	only bits: Bit A_FB1_BootWP =1 Bit A_FB1_SysWP =1.	

CHAPTER 4 Function Blocks

PowerPC Processor

The VG5 board provides the usage of MPC7455 and MPC7457 PowerPC processors. With frequencies from 800 MHz to +1300 MHz and core voltage supplies from 1.75 V down to 0.6 V. The VG5 can support either one or two CPUs. Each CPU has its own chipset and memory for independent operation.

L3 Cache

The L3 cache of 2 MByte (PowerPC MPC7455) or 4 MByte (PowerPC MPC7457 with 2 MByte cache and 2 MByte conventional SRAM) has a direct interface to the CPU and works with a maximum clock rate of 166 MHz. It consists of a Synchronous Pipelined Burst SRAM with an access time of <3,5 ns. The L3 cache is ECC protected.

Chipset

The VG5 uses the Marvell MV64360 chipset. This is a highly integrated system controller which provides a PowerPC CPU bus interface, memory controller, device controller (direct connection to standard logic), 2 PCI bus interfaces, two Ethernet MAC controllers and two Multi-Protocol Serial Controllers as the main features. Each Processor Node has one chipset for independent operation. For a complete description see the Marvell MV64360 datasheet.

DDR-SDRAM Memory

The VG5 provides at each chipset one bank of 64-bit wide Double Data Rate SDRAM memory with a 133 MHz memory clock. It is controlled by the MV64360 chipset controller with ECC single-bit error correction and double-bit error detection. The size of each bank can be 256 MByte or 512 MByte.

Flash ROM

The VG5 contains for each node two banks of Flash memory. This provides 64 MByte (one bank) or 128 MByte (two banks) of Flash memory capacity for each node - so the maximum Flash memory per board is 256 MByte.

Version V3.0 and up:
The VG5 contains for each node two banks of Flash memory. This provides 128 MByte (one bank) or 256 MByte (two banks) of Flash memory capacity for each node - so the maximum Flash memory per board is 512 MByte. This version requires new BSP (VxW2-BVG5 V1.2/6). VxWorks kernel has to be recompiled to create new memory map, if 256 MB of memory per node is used.

The Flash memory contains the boot program and the emergency boot program, theses two blocks are individually write protected by hardware jumpers. Additionally the BOOTSEL jumpers select the boot process either from the normal boot or from the emergency boot program. For erase and reprogramming the Flash device and boot behavior please refer to the software manual which is part of the BSP.

FPGA

FPGA Overview (Block Diagram)

The FPGA is connected to the device buses of Node A and Node B. The device bus is a 32-bit wide multiplexed address/data bus. The device buses of Node A and B are independent and only coupled through the dual port RAM inside the FPGA. The FPGA is a Xilinx Spartan2e type. The base address of the FPGA address decoding is the programmed value of DevCS1 in the chipsets. The default base address after reset is 0x1C80_0000.

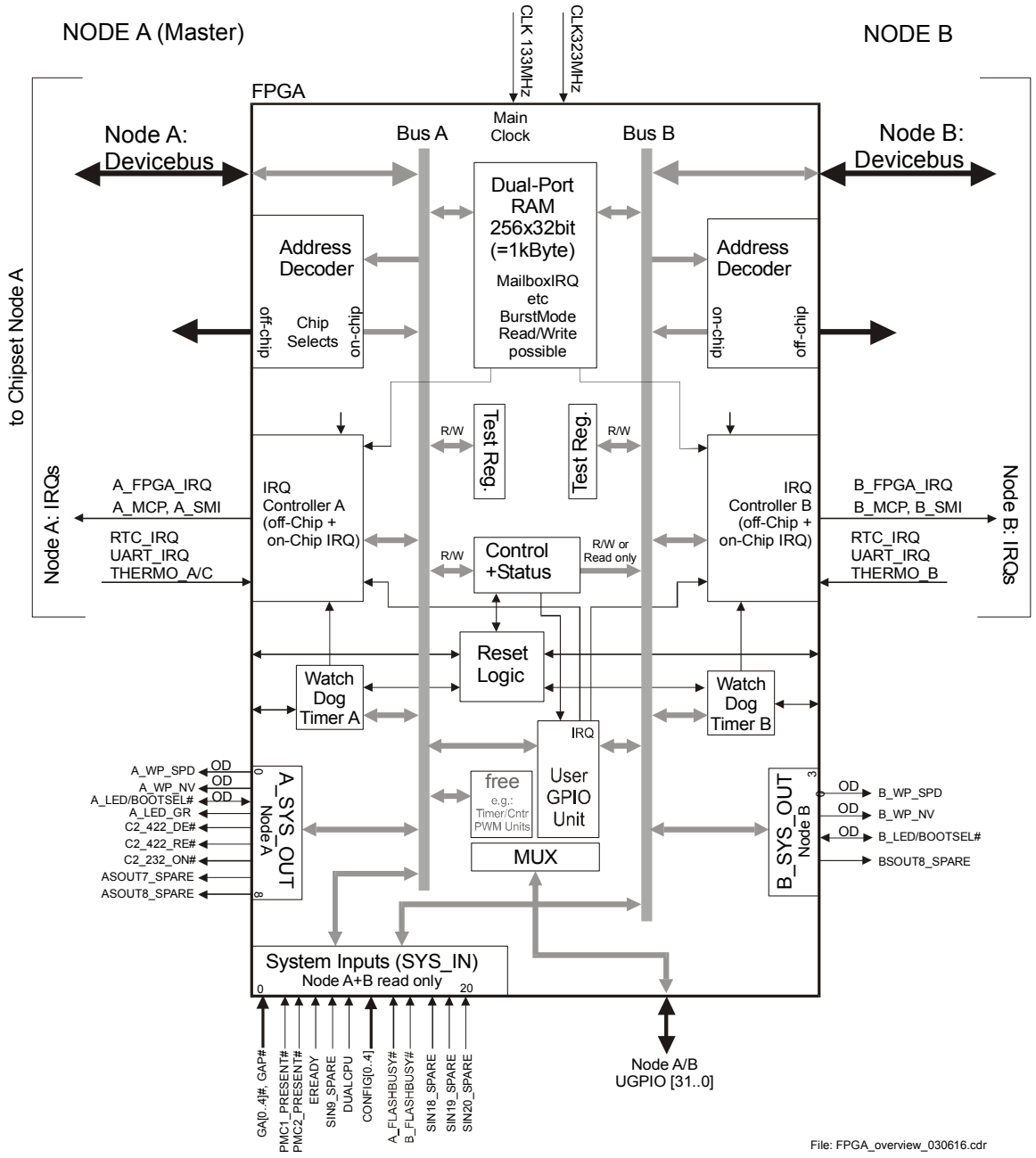


Figure 23: FPGA Block Diagram Dual Node

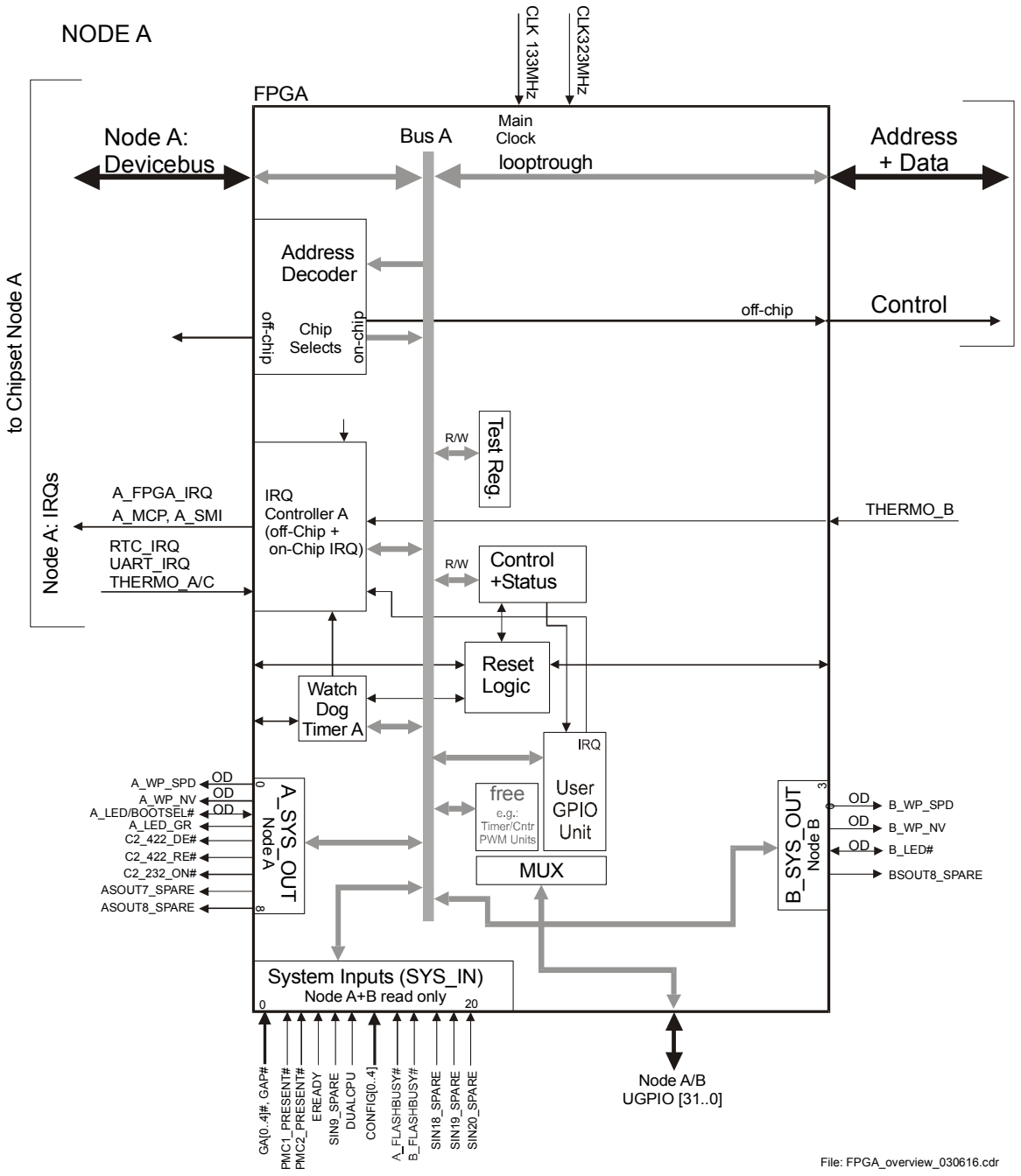


Figure 24: FPGA Block Diagram Single Node

FPGA Overview (Registers)

Table 19: Overview FPGA Registers (Node A and B)

Register	Offset	Accessible by Node	Kind of Access	Remarks
Dual-Port-RAM				(for details see chapter FPGA Dual Port RAM)
A_DPRAM B_DPRAM	0-0x3FF	A B	R/W R/W	1 kByte Dual Port RAM simultaneously accessible by Node A and B
A_DPCNTRL	0x8000	A B	W R	Write Access generates DPRAM_IRQ Interrupt on B-Node side. B-Node can read the written value.
B_DPCNTRL	0x8000	B A	W R	Write Access generates DPRAM_IRQ Interrupt on A-Node side. A-Node can read the written value.
On-board IO Registers				(for details see chapter FPGA System I/O)
A_SYS_OUT	0x8104	A	R/W	Outputs for special onboard functions. Only accessible by Node A. (for details see Table 34)
B_SYS_OUT	0x8104	B	R/W	Outputs for special onboard functions. Only accessible by Node B (for details see Table 35)
SYS_IN	0x8100	A + B	R(W)	Inputs for special onboard functions. Readable for Node A and B (for details see Table 33)
IRQ-Controller Node A				(for details see chapter FPGA Interrupt Controller A)
A_IRQ_CAUSE	0x8300	A	R/W	Node A Interrupt cause register (for details see Table 20)
A_IRQ_MASK	0x8304	A	R/W	Node A Interrupt mask register (for details see Table 22)
IRQ-Controller Node B				(for details see chapter FPGA Interrupt Controller B)
B_IRQ_CAUSE	0x8300	B	R/W	Node B Interrupt cause register (for details see Table 23)
B_IRQ_MASK	0x8304	B	R/W	Node B Interrupt mask register (for details see Table 25)
UGPIO				(for details see chapterFPGA UPGIO)
UGPIO_CONFIG	0x8600	A B	R/W R (WProt)	User GPIO configuration register. Selects which Node a UGPIO bit belongs. Only writeable by Node A (Master) – both nodes can read simultaneously. Write Protection!
UGPIO_MUX	0x8518	A	R/W R/W	For Future extension: Selects between UGPIO function and a secondary funct.(depends on settings in UGPIO_CONFIG)
UGPIO_DIR	0x8504	A B	R/W R/W	Selects if a UGPIO-bit is Input or Output (depends on settings in UGPIO_CONFIG)
UGPIO_IN	0x8500	A+B	R	UGPIO Input register (readable by both nodes)
UGPIO_OUT	0x8500	A B	W W	UGPIO Output register: writeability depends on settings in GPIO_CONFIG
UGPIO_IRQMASK1	0x8508	A B	R/W R/W	Interrupt Mask Register1: Setup for UGPIO[0..15] (depends on settings in UGPIO_CONFIG)
UGPIO_IRQMASK2	0x8510	A B	R/W R/W	Interrupt Mask Register2: Setup for UGPIO[16..31] (depends on settings in UGPIO_CONFIG)
A_IRQEVENT	0x8514	A	R/W	UGPIO IRQ Event register Node A.
B_IRQEVENT	0x8514	B	R/W	UGPIO IRQ Event register Node B.

Watchdog A				(for details see chapter FPGA Watchdog Timer A/B)
A_WDGCOMP1/0	0x8200	A	R/W	Watchdog A Compare Register: COMP1: Compare value for Reset (High Word) COMP0: Compare value for A_MCP Interrupt (Low Word)
A_WDGDATA +(Service)	0x8204	A	R(W)	Read: High Word of the 32 bit A_WDG-Counter. Write 0x2A: Service for Watchdog A
Watchdog B				(for details see chapterFPGA Watchdog Timer A/B)
B_WDGCOMP1/0	0x8200	B	R/W	Watchdog B Compare Register: COMP1: Compare value for Reset (High Word) COMP0: Compare value for B_MCP Interrupt (Low Word)
B_WDGDATA +(Service)	0x8204	B	R(W)	Read: High Word of the 32 bit B_WDG-Counter. Write 0x2A: Service for Watchdog B
Others				
A_CNTRLSTAT	0x8008	A	R/W (WProt)	Node A Control and Status bits including write protection for CNTRLSTAT and UGPIO_CONFIG register (for details see Table 26)
B_CNTRLSTAT	0x8008	B	R/W (WProt)	Node B Control and Status bits including write protection for B_CNTRLSTAT register (for details see Table 27: B_CNTRLSTAT Register)
A_TEST	0x8004	A	R/W	Node A Test Register (for details see chapter FPGA Test Register A/B)
B_TEST	0x8004	B	R/W	Node B Test Register (for details see chapter FPGA Test Register A/B)

Remarks

- FPGA Register names starting with 'A_' are Node A registers.
- FPGA Register names starting with 'B_' are Node B registers.
- Some registers are read/write for Node A and read only for Node B.
- All registers are located on long word boundaries, so all addresses are divisible by four.
- All registers are 32-bit wide but some registers use not all bits.
- The UGPIO_CONFIG register controls to which node the UGPIO register bits belong.
- The register address map is identical as seen from the Node A or node B side.
- The registers on the node B side have some functions less than their counterparts on the node A side.
- The register address is calculated : FPGA Base Address + Offset.
- The FPGA Base Address is set in the DEVCS1base Register (0x228) in the Node A or B Chipset.
  The page size has to be 64 kByte (DEVCS1SIZE (0x230) = 0)

FPGA Dual Port RAM

The FPGA has a built-in true Dual Port Memory organised as 256 x 32 bit (=1 kByte).
The address area is base address+0000h to 03FFh.
With two mailbox registers interrupts can be generated on the other node.

A_DPCNTRL Register: Mailbox A → B
32-bit register; Node A write only; Node B read only
a write on side A causes a B_DPRAM_IRQ on side B

B_DPCNTRL Register: Mailbox B → A
32-bit register; Node B write only; Node A read only
a write on side B causes a A_DPRAM_IRQ on side A

Performance: max peak read/write rate to the Dual Port RAM is about 100 MByte/s.

FPGA Interrupt Controller A

Each Node has its own independent Interrupt Controller in the FPGA.
The FPGA Interrupt Controller A extends the huge interrupt capabilities of the Chipset of Node A.

Interrupt Controller for Node A has the following sources:

- FPGA external:
  A_RTC_IRQ Real Time Clock
  A_UART_INTA UART A, Channel A
  A_UART_INTB UART A, Channel B(only used in Single Node VG5)
  VME_BERR VMEbus error
  THERMO_A Thermo sensor near CPU-A
  THERMO_B Thermo sensor near CPU-B (used by Node B)
  THERMO_C Thermo sensor Centre of board

- FPGA internal
  A_DPRAM_IRQ Mailbox Interrupt from Dual Port RAM
  A_GPIO_IRQ Interrupt caused by User General Purpose IO (GPIO)
  A_WDG_IRQ Watchdog A MCP step reached (causes high Priority MCP IRQ)
  B_WDG_IRQ caused by a Fast Reset on Node B side due to Watchdog B

The Interrupt Controller A has the following outputs:

- A_FPGA_IRQ Standard IRQ, connected to the MPP20 pin of chipset A
- A_SMI System Management Interrupt, high Priority IRQ, directly connected to CPU A
- A_MCP Machine Check Interrupt, high Priority IRQ, directly connected to CPU A

Table 20: A_IRQ_CAUSE Register

A_IRQ_CAUSE Register: This register shows pending IRQs.						Address: Base Address + 8300h
		Bit	**IRQ-Name**	**routed to IRQ output**	**Read/ Write**	**Remark**
A_IRQ CAUSE-Register	external IRQs	0	A_RTC_IRQ	A_FPGA_IRQ	R	
		1	A_UARTA	A_FPGA_IRQ	R	
		2	A_UARTB	A_FPGA_IRQ	R	
		3	-	-	R=0	Reserve for future off chip IRQ source
		4	VME_BERR	A_MCP	R/W	latched [1) 3)]
		5	THERMO_A	A_SMI	R	[2)]
		6	THERMO_B	A_SMI	R	also connected to Node B IRQ Controller[2) 3)]
		7	THERMO_C	A_SMI	R	[2)]
	internal IRQs	8	-	-	R=0	Reserve for future on-chip IRQ source
		9	-	-	R=0	Reserve for future on-chip IRQ source
		10	-	-	R=0	Reserve for future on-chip IRQ source
		11	-	-	R=0	Reserve for future on-chip IRQ source
		12	A_DPRAM_IRQ	A_FPGA_IRQ	R/W	latched [1)]
		13	A_GPIO_IRQ	A_FPGA_IRQ	R	see A_GPIO IRQ Event Register
		14	A_WDG_IRQ	A_MCP	R/W	latched [1)]
		15	B_WDG_IRQ	A_FPGA_IRQ	R/W	latched [1)]

Notes:

1) to reset IRQs that are latched a '1'-bit must be written at the bit in the A_IRQ_CAUSE register, all other IRQs are cleared in the source chip of the IRQ (e.g. RTC chip).

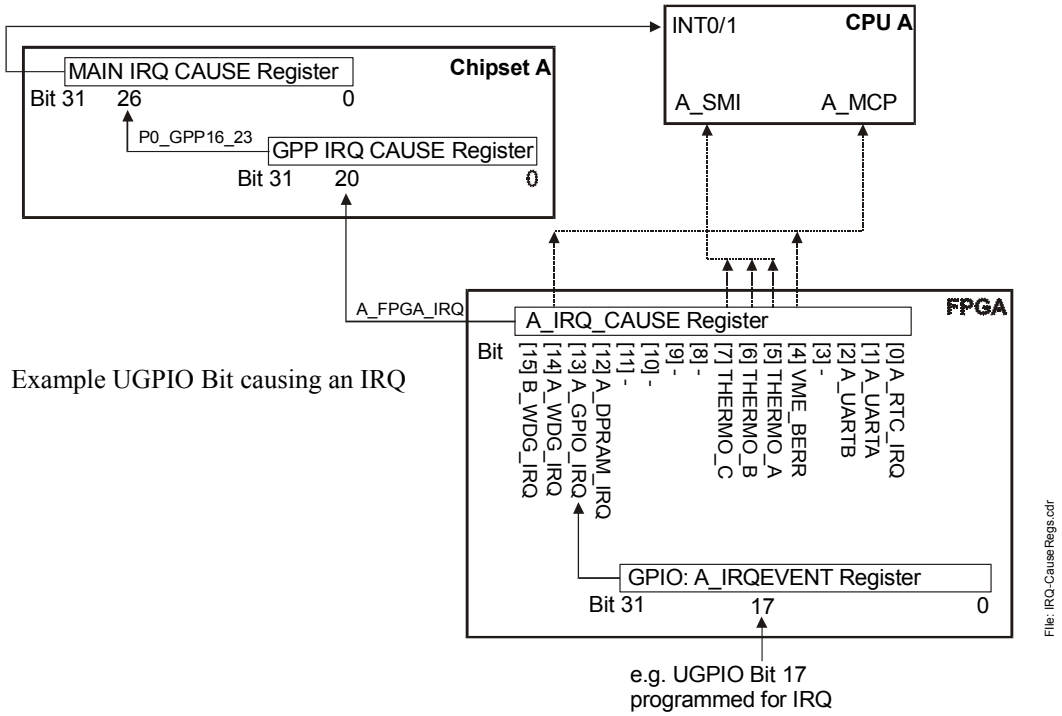
2) THERMO_A/B/C IRQs are connected to the LM75 Temperature sensors. The LM75 must be programmed for interrupt mode. (see LM75 Datasheet). A pending IRQ at the THERMO_A/B/C is cleared by reading any register of the corresponding LM75.

3) In dual node configuration VME-BusERR and THERMO_B are also connected to Node B. Software has to select through the IRQ-Mask which node is servicing the IRQ. In dual node configuration GE Intelligent Platforms BSPs use Interrupt Controller B; in single node configuration Interrupt Controller A is used (there is no Interrupt Controller B). See figures 21 and 22:

Table 21: VMEbusErr, Thermo_A/B/C IRQs

Interrupt	DualCPU	SingleCPU (only Node A)
VME-BusErr	Node B	Node A
THERMO_A	Node A	Node A
THERMO_B	Node B	Node A
THERMO_C	Node A	Node A

IRQ Cause Register Structure in VG5:



Example UGPIO Bit causing an IRQ

Figure 25: IRQ Cause Register Structure

Table 22: A_IRQ_MASK Register

A_IRQ_MASK Register:			Address: Base Address + 8304h
		Bit	**Mask for...**
A_IRQ_MASK Register	external IRQs	0	A_RTC_IRQ#
		1	A_UARTA
		2	A_UARTB
		3	-
		4	VME_BERR#
		5	THERMO_A#
		6	THERMO_B#
		7	THERMO_C#
	internalal IRQs	8	-
		9	-
		10	-
		11	-
		12	A_DPRAM_IRQ
		13	A_GPIO_IRQ
		14	A_WDG_IRQ
		15	B_WDG_IRQ

After a reset the MASK Register is set 0x0000, all IRQs are disabled.

FPGA Interrupt Controller B

The FPGA Interrupt Controller B extends the huge interrupt capabilities of the Chipset of Node B. It's structure is identical to Interrupt Controller A, but has fewer external interrupt sources.

Interrupt Controller for Node B has following IRQ sources:

- FPGA external:
  B_RTC_IRQ Real Time Clock
  B_UART_INTA UART B, Channel A
  VME_BERR VMEbus error
  THERMO_B Thermo sensor near CPU-B (also connected to Node A)

- FPGA internal
  B_DPRAM_IRQ Mailbox Interrupt from Dual Port RAM
  B_GPIO_IRQ Interrupt caused by User General Purpose IO (UGPIO)
  B_WDG_IRQ Watchdog B MCP step reached (causes high Priority MCP IRQ)
  A_WDG_IRQ caused by a soft reset on Node A side due to Watchdog A

The Interrupt Controller B has following IRQ outputs:

- B_FPGA_IRQ Standard IRQ, connected to the MPP20 pin of chipset B (GPIO of Chipset)
- B_SMI System Management Interrupt, high Priority IRQ, directly connected to CPU B
- B_MCP Machine Check Interrupt, high Priority IRQ, directly connected to CPU B

Table 23: B_IRQ_CAUSE Register

B_IRQ_CAUSE Register: This register shows pending IRQs. Address: Base address + 8300h						
		Bit	**IRQ-Name**	**routed to IRQ output**	**Read/ Write**	**Remark**
B_IRQ_CAUSE-Register	external IRQs	0	-		R=0	-
		1	B_UARTA	B_FPGA_IRQ	R	
		2	-	-	R=0	-
		3	-	-	R=0	Reserve for future off chip IRQ source
		4	VME_BERR	B_MCP	R/W	latched [1) 3)]
		5	-	-	R=0	-
		6	THERMO_B	B_SMI	R	also connected to Node A IRQ Controller[2) 3)]
		7	-	-	R=0	-
	internal IRQs	8	-	-	R=0	Reserve for future on-chip IRQ source
		9	-	-	R=0	Reserve for future on-chip IRQ source
		10	-	-	R=0	Reserve for future on-chip IRQ source
		11	-	-	R=0	Reserve for future on-chip IRQ source
		12	B_DPRAM_IRQ	B_FPGA_IRQ	R/W	latched [1)]
		13	B_GPIO_IRQ	B_FPGA_IRQ	R	see B_GPIO IRQ Event Register
		14	B_WDG_IRQ	B_MCP	R/W	latched [1)]
		15	A_WDG_IRQ	B_FPGA_IRQ	R/W	latched [1)]

Notes:

1) to reset IRQs that are latched a '1'-bit must be written at the bit in the B_IRQ_CAUSE register, all other IRQs are cleared in the source chip of the IRQ (e.g. UART chip).

2) THERMO_B IRQ is connected to the LM75 Temperature sensors. The LM75 must be programmed for interrupt mode. (see LM75 Datasheet). A pending IRQ at the THERMO_B is cleared by reading any register of the corresponding LM75.

3) VME-BusERR and THERMO_B are also connected to Node B. Software has to select through the IRQ-Mask which node is servicing the IRQ. This feature is also important for the single node VG5 version. The default is:

Table 24: VMEbusErr, Thermo_A/B/C IRQs

Interrupt	DualCPU	SingleCPU (only Node A)
VME-BusErr	Node B	Node A
THERMO_A	Node A	Node A
THERMO_B	Node B	Node A
THERMO_C	Node A	Node A

Table 25: B_IRQ_MASK Register

B_IRQ_MASK Register:			Address: Base address + 8304h
		Bit	**Mask for...**
B_IRQ_MASK Register	external IRQs	0	-
		1	B_UARTA
		2	-
		3	-
		4	VME_BERR#
		5	-
		6	THERMO_B#
		7	-
	internal IRQs	8	-
		9	-
		10	-
		11	-
		12	B_DPRAM_IRQ
		13	B_GPIO_IRQ
		14	B_WDG_IRQ
		15	A_WDG_IRQ

After a reset the MASK Register is set to 0x0000, all IRQs are disabled.

FPGA Address decoder A/B

The device bus address decoder for Node A generates all control signals for RTC, A_UART and the two Flash Memory banks and also for all FPGA internal resources seen from Node A.

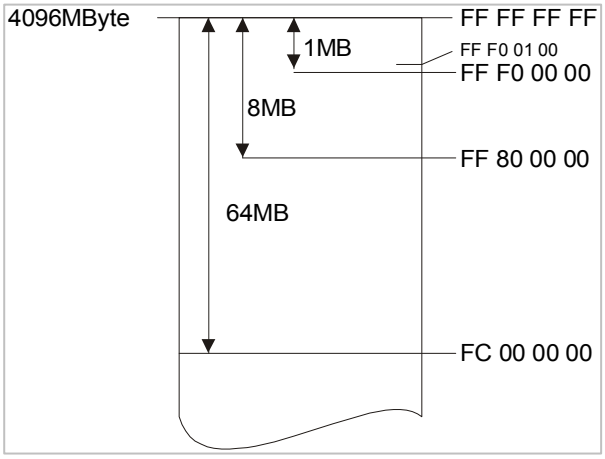


Figure 26: Memory Write Protection Areas

Note:
Change 64 MB to 128 MB and FC 00 00 00 to F8 00 00 00 in the figure above for version V3.0 and above

The device bus address decoder for Node B generates all control Signals for B_UART and the two Flash Memory banks and also for all FPGA internal resources seen from Node B.

Special function of the address controller is the Flash Write Protect function for some areas of the Flash Memory Bank 1 (Boot Node A/B).

Flashbank 1 is located at the upper boundary of the 4 GByte address space. The entrance point after Reset or Power-Up is in the upper 1 MByte where the boot loader is located.
This area is hardware write protected by the FPGA.
The upper 8 MByte are per default write protected by the FPGA, but this write protection can be switched off via the A/B_FB1_SYSWP bits in the A/B_CNTRLSTAT register.

Of course the standard Software Write Protection of the Flash Memory devices can be also used to protect Bank1 and Bank2.

FPGA Control and Status Register A/B_CNTRLSTAT

In the Node A Control/Status register A_CNTRLSTAT the following bits can be found:

Table 26: A_CNTRLSTAT Register

A_CNTRLSTAT (Control&Status Register A)					Address: Base address + 8008h
	Bit	**Name**	Read/ Write	Default	**Remark**
Byte 0	0	A_WDGRSTMODE0 [1]	R/W [2]	11	00 = No reset when Watchdog A expires [1] (but an MCP can be generated) 01 = A_WDG generates Fast-Reset A when Watchdog A expires
	1	A_WDGRSTMODE1 [1]	R/W [2]		10 = A_WDG generates Fast-Reset A and Fast-Reset B [3] 11 = A_WDG generates a hard reset (including FPGA)
	2	A_RESETB	R/W [2]	1	0 = Node B normal operation 1 = Node B is held in Reset (if used, Node A software has to control that minimum reset duration of B is 1.1ms)
	3	A_FB1_BootWP	R/W [2]	1	0= no write protection 1= Write-Protect for Flashbank 1 (boot area) on
	4	A_FB1_SysWP	R/W [2]	1	0= no write protection 1= Write-Protect for Flashbank 1 (system area) on
	5	-	-	0	-
	6	-	-	0	-
	7	WHOAMI	R	0	Node A reads always 0 [5]
Byte 1	8	A_RWP[0]	R/W	1	**Write protection** for A_CNTRLSTAT and UGPIO_CONFIG register: Write to this registers is only possible with the magic constant in A_RWP[7:0] = 0b0010'1010=42. This sets A_RWP[0]=0 and the write protection is disabled. Then the next access to A_CNTRLSTAT can be a successful write access. After this access A_RWP[0] is set to one again and the write protection is on again.
	9	A_RWP[1]	W		
	⋮	⋮	⋮		
	15	A_RWP[7]	W		
Byte3+2	16	16Bit FPGA-Version [4]	R	-	Bit 31..28: min. required VG5 PCB (0.x=0, 1.x=1, 2.x=2,...) Bit 27: Single/DualNode FPGA (0=Single / 1=Dual) Bit 26..20: Standard-FPGA-Version (1=Betas, 2,3,4...) Bit 19..16: Reserve (0000)
	⋮				
	31				

Notes
Node B
B_CNTRLSTAT register is identical to A_CNTRLSTAT, but has some functions missing:
Bit 2 is not used. (A_RESETB is here located in A_CNTRLSTAT, there is no B_RESETA)
Bit 7: WHOAMI reads always 1
Bit15..8: B_RWP[7:0] is only write protection for B_CNTRLSTAT (but not for UGPIO_CONFIG).

Table 27: B_CNTRLSTAT Register

B_CNTRLSTAT (Control&Status Register B)					Address: Base address + 8008h
	Bit	**Name**	Read/ Write	Default	**Remark**
Byte 0	0	B_WDGRSTMODE0 [1]	R/W [2]		00 = No reset when Watchdog B expires [1] (but an MCP can be generated) 01 = B_WDG generates Fast-Reset B when Watchdog B expires
	1	B_WDGRSTMODE1 [1]	R/W [2]	11	10 = B_WDG generates Fast-Reset B and Fast-Reset A [3] 11 = B_WDG generates a hard reset (including FPGA)
	2	-	-	-	-
	3	B_FB1_BootWP	R/W [2]	1	0= no write protection 1= Write-Protect for Flashbank 1 (boot area) on
	4	B_FB1_SysWP	R/W [2]	1	0= no write protection 1= Write-Protect for Flashbank 1 (system area) on
	5	-	-	0	-
	6	-	-	0	-
	7	WHOAMI	R	0	Node B reads always 1 [5]
Byte 1	8	B_RWP[0]	R/W	1	**Write protection** for B_CNTRLSTAT Register: Write to this registers is only possible with the magic constant in B_RWP[7:0] = 0b0010'1010=42. This sets B_RWP[0]=0 and the write protection is disabled. Then the next access to B_CNTRLSTAT can be a successful write access. After this access B_RWP[0] is set to one again and the write protection is on again.
	9	B_RWP[1]	W		
	⋮	⋮	⋮		
	15	B_RWP[7]	W		
Byte3+2	16 ⋮ 31	16Bit FPGA-Version [4]	R	-	Bit 31..28: min. required VG5 PCB (0.x=0, 1.x=1, 2.x=2,...) Bit 27: Single/DualNode FPGA (0=Single / 1=Dual) Bit 26..20: Standard-FPGA-Version (1=Betas, 2,3,4...) Bit 19..16: Reserve (0000)

Notes:

1) If the A or B_WDG_Off_Jumper is set, A/B_WDGRSTMODE[1:0] is always 00, so Watchdog Reset A/B is off

2) Write protected by A/B_RWP[7:0]

3) A/B_WDGRST bits located in SYS_IN register are set when a Fast-Reset A/B occurs. See also chapter FPGA System I/O.

4) Remark regarding 16-Bit FPGA version register

FPGA-Beta-Versionen (Single/Dual) 0x1010

Single Node

PCB0.x, first FPGA-version with new version register:
0000'0000'0010'0000 = 0x0020
e.g.: further SingleNode FPGA-Versions 0x0030, 0x0040, 0x0050, ... 0x07F0

Dual Node PCB0.x, first FPGA-version with new version register:
0000'1000'0010'0000 = 0x0820
e.g.: further DualNode FPGA-Versionen 0x0830, 0x0840, 0x0850, ... 0x0FF0

E.g.: A future FPGA-Version (with a changed pinout), which would require a special VG5-PCB version (e.g. PCB 2.x and higher), would have the dual-version : e.g.: 0x2830 = PCB2.x,Dual,FPGA3

5) Unfortunately due to an errata in the FPGA Node B reads the WHOAMI-bit also as 0 (as Node A) – so the software can't identify Node B in this way – use RTC instead: No RTC → Node B.

or UGPIO instead: UGPIO_Config Register read-only → Node B
This errata is fixed in the FPGA revision 0x0840 (VG5 V2.4 or VG5 V3.4)

FPGA Test Register A/B

The test register A/B is only used for factory testing

Table 28: Test register A/B

Test-Register Node A/B			Address: Base address + 8004h
Name	Bit	Read/Write	Remark
A/B_TEST	32 bit width	R/W	the written long word will be read inverted

FPGA Watchdog Timer A/B

For the security of application software, the VG5 offers a software controlled hardware watchdog capable of issuing a reset signal if its time-out interval expires. To prevent the watchdog from generating a reset signal, it must be serviced within a programmable interval by writing a magic constant to the watchdog register WDGDATA.

There is one for Node A Watchdog A and for Node B Watchdog B. Each watchdog is exclusively bound to its Node.

The Watchdog consists of a 32-bit counter using the 133 MHz system clock as its input clock. The upper 16 bit of the counter are compared against the 16-bit registers COMP0 and 1, and if equal a MCP is caused by COMP0 and a reset by COMP1.
So the Watchdog expiry time is programmable in steps of 492 µs up to the max. time of 32.29 s using the standard 133 MHz system clock.
(at 100 MHz system clock 656 µs up to 43 s)
Watchdog A has the following registers:

- A_WDGCOMP0 and A_WDGCOMP1
- A_WDGDATA (+ service)
- A_WDGRSTMODE[1:0] bits located in A_CNTRLSTAT register
- A_WDG1A/B_EXP bits located in SYS_IN register

Watchdog B has following registers:

- B_WDGCOMP0 and B_WDGCOMP1
- B_WDGDATA (+ service)
- B_WDGRSTMODE[1:0] bits located in B_CNTRLSTAT register
- B_WDG1B/A_EXP bits located in SYS_IN register

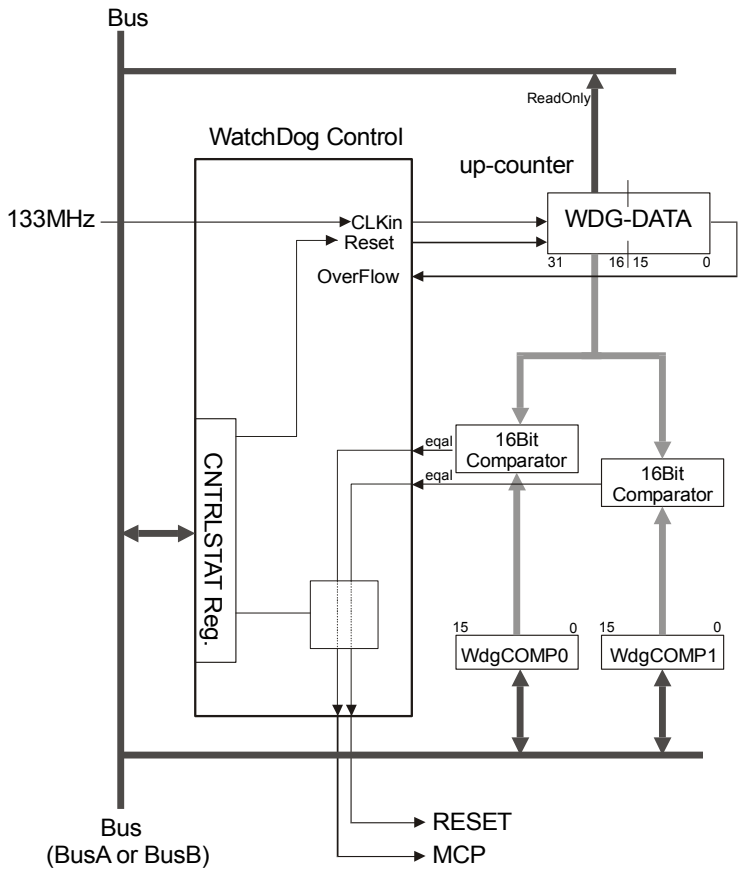


Figure 27: Watchdog Block Diagram

The Figure below shows some different working examples of the Watchdog:

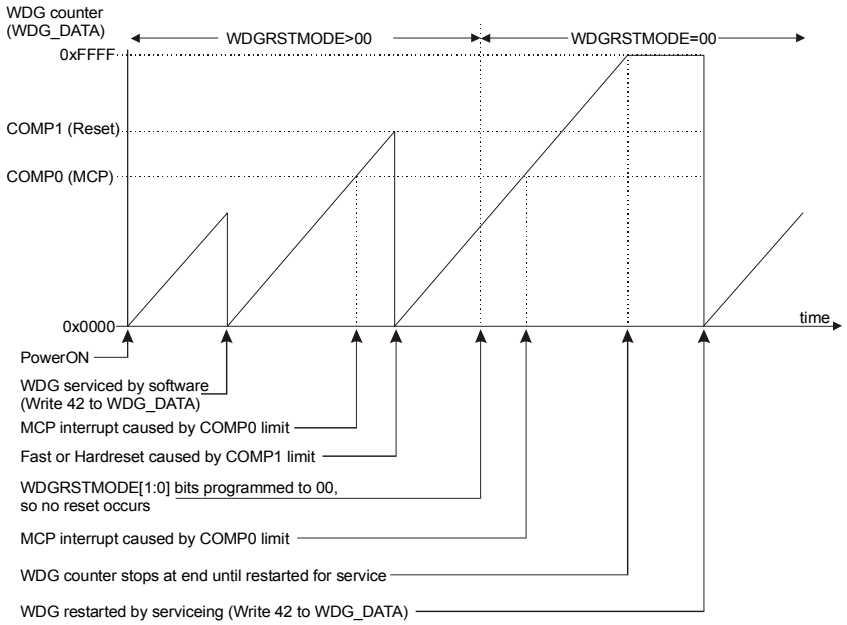


Figure 28: Watchdog Timing Diagram

Warning:
The watchdog's MCP interrupt feature (Machine Check Exception) is only usable for some last actions before doing a software controlled reset. It is possible e.g.:

- to set the UGPIO outputs to a safe state
- or to give the other node a message via the Dual Port RAM
- or to do error logging to the console port.

The return from the MCP exception crashes, when the system was working in an interrupt service routine (ISR) when the MCP exception comes up.
It is successfully when the system was not in an ISR or exception handler when the MCP occurs.

Please see the excerpt of the Freescale 745x processor manual below:

> *The machine check exception is usually unrecoverable in the sense that execution cannot resume in the context that existed before the exception. If the condition that caused the machine check does not otherwise prevent continued execution, MSR[ME] is set by software to allow the processor to continue execution at the machine check exception vector address. Typically, earlier processes cannot resume; however, operating systems can use the machine check exception handler to try to identify and log the cause of the machine check condition.*

See also the VxWorks SPR# 116794 from Wind River describing the problem.

Its also possible to use the watchdog's MCP interrupt feature in a stand alone program (no operating system) without other active exception and interrupt handler – but this will be a rare case.

FPGA Watchdog A/B (Registers detailed)

Table 29: A/B_WDGCOMP0/1

Watchdog A/B Compare Register (0+1)			Address: Base address + 8200h
Name	Bit	Read/Write	Remark
A/B_WDGCOMP0	Bit[15..0] (Low Word)	R/W	These 16 bit set the limit, where a A/B_MCP interrupt is generated. Default after PowerOn: 0x27B3 = 5s
A/B_WDGCOMP1	Bit[31..16] (High Word)	R/W	These 16 bit set the limit where, depending on the A/B_WDGRSTMODE[1:0] bits, a Fast or hard reset is generated Default after PowerOn: 0x2FA3 = 6sec

Table 30: A/B_WDGDATA + Service

The value of A/B_WDGCOMP0 should be normally lower than A/B_COMP.

Watchdog A/B_WDGDATA Register			Address: Base address + 8204h
Name	Bit	Read/Write	Remark
A/B_WDGDATA +(Service)	Bit[15..0]	R/W	Read: The actual value of the watchdog counter high word can be read. The value can change during read – so the software has to read it multiple times in less than 492 µs and check the value for correctness. Write: The watchdog will be serviced (reset), when writing the magic constant 0b0010'1010=42 into the A/B_WDG_DATA register

Table 31: Watchdog A Control-Bits

Watchdog A Control-Bits located in A_CNTRLSTATregister			Address: Base address + 8008h
Bit	Name	Read/Write	Remark
in A_CNTRLSTAT-Register (see also chapter FPGA Control and Status Register A/B)(see chapter H			
0	A_WDGRSTMODE0 [1)]	R/W [2)]	00 = No reset when Watchdog A expires [1)] (but an A_MCP can be generated) 01 = A_WDG generates Fast-Reset A when Watchdog A expires Node B will get an A_WDG_IRQ for information
1	A_WDGRSTMODE1 [1)]	R/W [2)]	10 = A_WDG generates Fast-Reset A and Fast-Reset B [3)] 11 = A_WDG generates a hard reset (including reload of FPGA)
in SYS_IN-Register			
26	A_WDG1A_EXP	R/W	=0 after Hardreset, (default) =1 if A_WDG ≥ A_WDGCOMP1 (WDG_A expired → Fast Reset) Only Node A can clear the bit by writing '0'. Node B can only read.
27	A_WDG1B_EXP	R/W	=0 after Hardreset, (default) =1 if B_WDG ≥ B_WDGCOMP1 (WDG_B expired → Fast Reset) Only Node A can clear the bit by writing '0'. Node B can only read.

Table 32: Watchdog B Control-Bits

Watchdog B Control-Bits located in B_CNTRLSTAT register Address: Base address + 8008h			
Bit	Name	Read/Write	Remark: (see chapter Hard and Fast Reset for Hard/Fast Reset)
in B_CNTRLSTAT-Register (see also chapter FPGA Control and Status Register A/B)			
0	B_WDGRSTMODE0 [1)]	R/W [2)]	00 = No reset when Watchdog B expires [1)] (but an B_MCP can be generated) 01 = B_WDG generates Fast-Reset B when Watchdog B expires Node A will get an B_WDG_IRQ for information
1	B_WDGRSTMODE1 [1)]	R/W [2)]	10 = B_WDG generates Fast-Reset B and Fast-Reset A [3)] 11 = B_WDG generates a hard reset (including reload of FPGA)
in SYS_IN-Register			
28	B_WDG1B_EXP	R/W [3)]	=0 after Hardreset (default) =1 if B_WDG ≥ B_WDGCOMP1 (WDG_B expired → Fast Reset) Only Node B can clear the bit by writing '0'. Node A can only read.
29	B_WDG1A_EXP	R/W [3)]	=0 after Hardreset, (default) =1 if A_WDG ≥ A_WDGCOMP1 (WDG_A expired → Fast Reset) Only Node B can clear the bit by writing '0'. Node A can only read.

Notes:

1) If the A or B_WDG_Off_Jumper is set, A/B_WDGRSTMODE[1:0] is always 00, so Watchdog Reset A/B is off
2) Write protected by A/B_RWP[7:0]
3) A/B_WDG1A/B_EXP bits located in SYS_IN register are set when a Fast-Reset A/B occurs. See also Table 33: SYS_IN Register.

FPGA System IO

The System IOs are used for VG5 on-board IO. They consist of three registers:

In SYS_IN all onboard Inputs are located. Node A and B can read simultaneously.
In A_SYS_OUT there are Node A Outputs. Only Node A can read and write this register.
In B_SYS_OUT there are Node B Outputs located. Only Node B can read and write this register.

See detailed register information below.

Table 33: SYS_IN Register

Register SYS_IN (readable by Node A and B)				Address: Base address + 8100h	
	Pin-Name	**Function**	**Bit**	**Register –Bit**	**Default / Remark**
Byte 0 (extern)	GA[4..0]#	VME Geographical Addressing	4..0		Static during PowerOn
	GAP#	VME Geographical Addressing Parity	5		Static during PowerOn
	PMC1_PRESENT#	PMC1 Site populated when Low	6	=0 populated =1 empty	Static during PowerOn
	PMC2_PRESENT#	PMC2 Site populated when pin Low	7	=0 populated =1 empty	Static during PowerOn
Byte 1 (extern)	EREADY	PMC1/2: Processor of PMC ready	8	=0 =1 Ready	
	SIN9_SPARE	Reserve	9	-	
	DUALCPU	High-active Input	10	=0 one CPU =1 dual CPU	Static during PowerOn
	Config[4..0]#	Configuration Pins	15..11	=0 Pull-down R set =1	
Byte 2 (extern)	A_FLASHBUSY#	Low if Node A Flashbank 1 or 2 is busy	16	=0 Busy =1 Ready	
	B_FLASHBUSY#	Low if Node B Flashbank 1 or 2 is busy	17	=0 Busy =1 Ready	
	SIN18_SPARE	Reserve	18	-	
	SIN19_SPARE	Reserve	19	-	
	SIN20_SPARE	Reserve	20	-	
	-		21		
	-		22		
	-		23		
Byte 3 (intern)	-		24		
	-		25		
	A_WDG1A_EXP	Bit: read (A/B) write (A) Info for Node A: WDG_A has reached the limit of A_WDGCOMP1.	26	Details see Table 31	
	A_WDG1B_EXP	Bit: read (A/B) write (A) Info for Node A: WDG_B has reached the limit of B_WDGCOMP1.	27	Details see Table 31	
	B_WDG1B_EXP	Bit: read (A/B) write (B) Info for Node B: WDG_B has reached the limit of B_WDGCOMP1.	28	Details see Table 32	
	B_WDG1A_EXP	Bit: read (A/B) write (B) Info for Node B: WDG_A has reached the limit of A_WDGCOMP1.	29	Details see Table 32	
	-		30		
	-		31		

Table 34: A_SYS_OUT Register

Register: A_SYS_OUT (only readable by Node A)			Address: Base address + 8104h	
Pin-Name	**Function**	**Bit**	**Bit Description**	**Default / Remark**
A_WP_SPD	Write-Protect Serial SPD-EEPROM Node A	0	=0 Write Enabled =1 Write Protected	Default: 1 Protected
A_WP_NV	Write-Protect Serial NV-EEPROM Node A	1	=0 Write Enabled =1 Write Protected	Default: 1 Protected
A_LED/BOOTSEL	Output: Open-Drain A_LED: Red Node A LED	2	=0 LED On =1 LED Off	Default: 0 = LED On
	Input: BootSelect: Flashbank 1/2		=0 Jumper set =1 Jumper not set	Read: The external pin status will be read, so it can be detected if the A_Bootselect-Jumper is set or not. To be able to detect the external pin status, the Output has to be set to one (LED off)
A_LED_GR#	LED Green, User	3	=1 LED Off =0 LED on	Default: 1 = LED Off
C2_422_DE#	Com2 RS422 Transmitter Data Enable	4	=0 Enabled =1 Disabled	Default: 1 Disabled
C2_422_RE#	Com2 RS422 Receiver Enable	5	=0 Enabled =1 Disabled	Default: 1 Disabled
C2_232_ON#	Com2 RS232 Enable	6	=0 Enabled =1 Disabled	Default: 1 Disabled
ASOUT7_SPARE	Output; Reserve	7	-	-
ASOUT8_SPARE	Output; Reserve	8	-	-
	Only for Single Node Version:			
B_WP_NV	High-active Output; Open-Drain Write-Protect Serial NV-EEPROMS Node B	16	=0 Write Enabled =1 Write Protected	Default: 1 Protected
B_LED #	Low-active Output; Open-Drain B_LED: Red Node B LED	17	=0 LED On =1 LED Off	Default: 1 LED Off

Table 35: B_SYS_OUT Register

Register: B_SYS_OUT (only readable by Node B)			Address: Base address + 8104h	
Pin-Name	**Function**	**Bit**	**Bit Description**	**Default / Remark**
B_WP_SPD	Write-Protect Ser. SPD-EEPROM Node B	0	=0 Write Enabled =1 Write Protected	Default: 1 Protected
B_WP_NV	Write-Protect Serial NV-EEPROM Node B	1	=0 Write Enabled =1 Write Protected	Default: 1 Protected
B_LED/BOOTSEL	Output: Open-Drain B_LED: Red Node B LED	2	=0 LED On =1 LED Off	Default: 0 = LED On
	Input: BootSelect: Flashbank 1/2		=0 Jumper set =1 Jumper not set	Read: The external pin status will be read, so it can be detected if the B_Bootselect-Jumper is set or not. To be able to detect the external pin status, the Output has to be set to one (LED off)
BSOUT3_SPARE	Output, Reserve	3		

FPGA User General Purpose IO (UGPIO)

The VG5 provides 32 General Purpose IOs (UGPIO). The UGPIOs are controlled by the FPGA logic.
Each of these UGPIO bits is separately programmable by the user as input, output and with rising/falling/any edge sensitive interrupt.
All 32 bits are available at rear IO but shared with PMC2 IO signals:

'VG5x xxxx x0xx x'	no PMC2 ,	UGPIO available.
'VG5x xxxx x1xx x'	PMC2 rearIO ,	no UGPIO available.
'VG5x xxxx x2xx x'	no PMC2 rearIO ,	UGPIO available.

Node A as the Master can configure which UGPIO bits belong to Node A or B.
(see register UGPIO_CONFIG)

Table 36: UGPIO at P2 (P7200)

IO Signal	P2 Connector	IO Signal	P2 Connector
UGPIO00	A17	UGPIO16	C17
UGPIO01	A18	UGPIO17	C18
UGPIO02	A19	UGPIO18	C19
UGPIO03	A20	UGPIO19	C20
UGPIO04	A21	UGPIO20	C21
UGPIO05	A22	UGPIO21	C22
UGPIO06	A23	UGPIO22	C23
UGPIO07	A24	UGPIO23	C24
UGPIO08	A25	UGPIO24	C25
UGPIO09	A26	UGPIO25	C26
UGPIO10	A27	UGPIO26	C27
UGPIO11	A28	UGPIO27	C28
UGPIO12	A29	UGPIO28	C29
UGPIO13	A30	UGPIO29	C30
UGPIO14	A31	UGPIO30	C31
UGPIO15	A32	UGPIO31	C32

Attention:
The UGPIO are not 5 V tolerant at P2 connector (high voltage 3,3 V ; see chap. FPGA UPGIO – Electrical Specification
When using the VTM20 transition module level translators (‘Quickswitches’) are provided.
At P8000 the UGPIO signals are 5 V capable.

Table 37: UGPIO Registers

Register	Function
UGPIO_CONFIG Base address + 8600h	Selects for each UGPIO bits (and the belonging bits in other configuration registers), if it is writeable by Node A or Node B. Only Node A (Master) can set this register. 0 = Node A, 1 = Node B PowerON Default: 0xFFFF 0000 Node A: Read/Write Node B: Read only **Write protected** by A_CNTRLSTAT (see Table 26)
UGPIO_MUX Base address + 8518h	Foreseen for future use, if a special function module is included in the FPGA, that shares IOs with the UGPIO function block. This register is shared by between Node A and B, depending of the configuration in the UGPIO_CONFIG register. 0= UGPIO-Function 1= Special function PowerON Default: 0x0000 0000 Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
UGPIO_DIR Base address + 8504h	Selects the direction of a UGPIO bit. Node A or B can select the direction (Input or Output), depending of the settings in UGPIO_CONFIG. The direction for Node A bits can only be set by Node A and also only Node B can set the direction for Node B bits. 0 = Input 1 = Output PowerON Default: 0x0000 0000 Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
UGPIO_IN Base address + 8500h	Input data from 32 UGPIO inputs. Can be read simultaneously by Node A and B. Node A: read only Node B: read only
UGPIO_OUT Base address + 8500h	Shared between Node A and B for data Output. PowerON Default: 0x0000 0000 Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
UGPIO_IRQMASK1 Base address + 8508h UGPIO_IRQMASK2 Base address + 8510h	Configuration of the edge recognition. These registers are shared by between Node A and B, depending of the configuration in the UGPIO_CONFIG register. Two neighbouring bits set the edge recognition mode of the belonging UGPIO_IN bits. 00= IRQ off (default) PowerON Default: 0x0000 0000 01= IRQ on falling Edge 10= IRQ on rising Edge 11= IRQ on Edge (rising or falling) Node A: Read and depending from UGPIO_CONFIG (Bit=0) Write Node B: Read and depending from UGPIO_CONFIG (Bit=1) Write
A_IRQEVENT Base address + 8514h	32-bit edge detection event register for Node A stores UGPIO_IN edge events, if the belonging UGPIO bit is configured for Node A. A detected event will be stored as ‘1’ in the event register. It can only be cleared by Node A by writing a ‘1’ onto this bit in the A_IRQEVENT register. Bits that are configured to Node B are always read as 0. Multiple event bits can be set in the A_IRQEVENT register. If minimum one event bit is set, the A_GPIO_IRQ is set active in the A_IRQ-Controller.
B_IRQEVENT Base address + 8514h	32-bit edge detection event register for Node B stores UGPIO_IN edge events, if the belonging UGPIO bit is configured for Node B. A detected event will be stored as ‘1’ in the event register. It can only be cleared by Node B by writing a ‘1’ onto this bit in the B_IRQEVENT register. Bits that are configured to Node A are always read as 0. Multiple event bits can be set in the B_IRQEVENT register. If minimum one event bit is set, the B_GPIO_IRQ is set active in the B_IRQ-Controller.

Base address = FPGA base address. Base and size of page is set in the Chipset see MV64360 Datasheet , DevCS[1]# Base Address (Offset: 0x228). The VxWorks Board Support Package has a system function returning the FPGA base address: fpgaBasePtr.

UGPIO – Electrical Specifications

Table 38: a-b: UGPIO Electrical Specification

Absolute maximum ratings

Parameter	Condition	min.	typ.	max.
Input clamp current I_{IC}	V_{IH} < 0 V			±10 mA
Input voltage range VI (input range)		-0.5 V		4 V
Output source or sink current I_O	V_O > -0.5 V, VO <4.0 V			±24 mA

Remarks:

VI (input range) should not exceed V_{CCO}=0 V (power) by more than 3.6 V over extended periods of time (e.g., longer than a day). Maximum DC overshoot must be limited to either V_{CCO} + 0.5 V or 10 mA, and undershoot must be limited to –0.5 V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0 V or overshoot to V_{CCO} +2.0 V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

Operating

Parameter	Condition	min	typ	max
Input voltage high V_{IH}		2.0 V		
Input voltage low V_{IL}				0.8 V
Input voltage VI		0 V		3.6 V
Input transition rise or fall time				250 ns
Input capacitance CI			8 pF	
Output voltage high V_{OH}	I_{OH} = 8 mA	2.4 V		
Output voltage low V_{OL}	I_{OL} = 8 mA		0.4 V	0.5 V

Remarks:

The IO standard used for the UGPIO pins is LVTTL (3,3 V) with 8 mA cells.
5 V IOs can be connected to the UGPIO-Pins when using the VG5 transition module VTM20. Take care to use the UGPIO-5 V connector on the transition module.

FPGA in single Node VG5 Version

The FPGA in the VG5 single Node configuration is nearly the same as in dual node configuration.

The following differences exist:

- Dual Port RAM not included
- Only Node A specific modules included (e.g. no B_IRQ-Controller or B_WDG)
- Node B Flashbank 1/2 can be used for Node A (as Node A Flashbank3). Node A bus is routed completely through FPGA to reach the Node B flash banks. So now up to 128 MB+128 MB Flash Memory are possible in single node configuration. Slight read/write performance impact for the B-Flash Memories has to be taken into account.
- Register Layout compatible to dual node configuration. Some registers have to be initialized for Node A only usage. (e.g. UGPIO_CONFIG=0x00000000 etc)
- A_SYS_OUT Register has inherited some bits of Node B B_SYS_OUT Register.(see Table 34)

PCI Buses

The VG5 has in dual Node version three PCI buses. Each chipset provides two 64-bit PCI buses, one of each is dedicated to PCI devices like PMC, VME Controller etc, and the other PCI bus interconnects both chipsets to access the resources of the other node respectively to communicate between the two CPUs. Each PCI bus is theoretically 133 MHz PCI-X capable, but due to electrical and timing restrictions this is not possible.

Node A: PCI bus 0 has a maximum clock rate of 66 MHz (PCI)
Node A/B: PCI bus 1 has a maximum clock rate of 100 MHz (PCI-X)
Node B: PCI bus 0 has a maximum clock rate of 33 MHz (PCI)

In single node version the VG5 has only one chipset with two PCI buses. In this version the interconnection PCI bus will be short circuited with the Node B PCI bus via a device which simply connects the traces of these two buses. The speed of this PCI bus stays at PCI 33 MHz.

Asynchronous Serial Ports COM1, COM4

The VG5 supports two asynchronous serial ports. The serial ports are fully compatible with the NS16450 and NS16550. Address area: offset + 0000h to 0007h. Offset is the programmed value of DevCS2 in the chipset.
The UARTs have programmable baud rate generators capable of 50 to 115200 baud.
The asynchronous ports are COM1 and COM4 and are dedicated for the command terminal of each CPU node. In single node configuration COM4 can be controlled by Node A, too. The address area is offset + 0008h
The signals are buffered through EIA-232-D drivers and receivers and routed to the P2 connector and to the front IO at a SUBD-9pin (P2710) connector. At the rear connector (P2) only the receive and transmit signals are connected, at the front SUBD connector COM1 has additional status signals and COM4 uses pins of this connector for the transmit/receive line. To use two terminals a split cable is necessary to separate the RS-232 signal of both interfaces. In single node version COM4 is only connected to rear IO and the freed pins at P2710 are used by additional COM1 status signals.
(see also Table 1)

Table 39: a-b: COM1+4 Pin assignments at P2 and front connector P2710

Signal COM1	**P2 connector**
C1_RXD	Z9
C1_TXD	Z11
Signal COM4	**P2 connector**
C4_RXD	Z13
C4_TXD	Z15

Signal (VG5S, Single Node)	**Signal (VG5D, Dual Node)**	**P2710 (Front) (SUBD 9pin, male)**
C1_DCD	*C4_RXD*	1
C1_RXD	C1_RXD	2
C1_TXD	C1_TXD	3
C1_DTR	*C4_TXD*	4
GND	GND	5
C1_DSR	C1_DSR	6
C1_RTS	C1_RTS	7
C1_CTS	C1_CTS	8
C1_RI	C1_RI	9

Notes:
C1 = Serial Port COM1
C4 = Serial Port COM4
TxD = Transmit Data
RxD = Receive Data
GND = Signal Ground
RTS = Request To Send
CTS = Clear To Send
DCD = Data Carrier Detect
DSR = DCE Ready
DTR = DTE Ready
RI = Ring Indicator

Remark:
Don't use a standard Null Modem Cable with full handshake on a VG5D, because the VG5D C4_RXD / C4_TXD Signals will irritate your PC.

See appendix Serial Port cables (RS232) for detailed information regarding splitter and null modem cables

Serial Communication Interface COM2, COM3, COM5, COM6

Each of the Marvell MV64360 chipset contains two high performance Multi-Protocol Serial Controllers which support HDLC, BISYNC, UART (sync/async), and Transparent protocols. On the VG5 theses channels are COM2, COM3 (Node A) and COM5, COM6 (Node B) with RS-232 up to 115 kBaud and/or RS-422/485 driver/receivers up to 10 Mbit/s (COM2 limited to 250 kbit/s). COM2 is a software selectable RS-232 or RS-422/485 interface, COM3, COM5, and COM6 are RS-422/485 only.
The signals of all four serial interfaces are available at rear IO P2 and additionally there is a version with COM2 front IO at P2720 but this will restrict the usage of the second PMC site.

Table 40: COM2 Signals at P2 and front connector P2720

Signal COM2			**P2 connector**	**9-pin SUBD P2720**
RS-232 Signal (max 115 kbit)	RS-422/485 sync (max 250 kbit)	RS-422/485 async (max 250 kbit)		
C2_CTS	C2_ RXC-	C2_CTS-	D5	8
C2_TXD	C2_ RXC+	C2_CTS+	D6	3
C2_RXD	C2_TXC-	C2_RTS-	D7	2
C2_RTS	C2_TXC+	C2_RTS+	D8	7
Not used	C2_RXD-	C2_RXD-	D9	9
C2_DTR	C2_RXD+	C2_RXD+	D10	4
C2_DCD	C2_TXD-	C2_TXD-	Z1	1
C2_DSR	C2_TXD+	C2_TXD+	Z3	6
GND	GND	GND	-	5

Table 41: COM3 Signals at P2

Signal COM3 (max 10 Mbit)		**P2 Connector**
RS-422/485 sync	RS-422/485 async	
C3_ RXC-	C3_CTS-	D17
C3_ RXC+	C3_CTS+	D18
C3_TXC-	C3_RTS-	D19
C3_TXC+	C3_RTS+	D20
C3_RXD-	C3_RXD-	D15
C3_RXD+	C3_RXD+	D16
C3_TXD-	C3_TXD-	D21
C3_TXD+	C3_TXD+	D22

see also Table 1

Table 42: COM5 Signals at P2

Signal COM5 (max 10 Mbit)		**P2 Connector**
RS-422/485 sync	RS-422/485 async	
C5_ RXC-	C5_CTS-	D23
C5_ RXC+	C5_CTS+	D24
C5_TXC-	C5_RTS-	D25
C5_TXC+	C5_RTS+	D26
C5_RXD-	C5_RXD-	D29
C5_RXD+	C5_RXD+	D30
C5_TXD-	C5_TXD-	D27
C5_TXD+	C5_TXD+	D28

Table 43: COM6 Signals at P2

Signal COM6 (max 10 Mbit)		P2 Connector
RS-422/485 sync	RS-422/485 async	
C6_RXC-	C6_CTS-	Z21
C6_RXC+	C6_CTS+	Z23
C6_TXC-	C6_RTS-	Z25
C6_TXC+	C6_RTS+	Z27
C6_RXD-	C6_RXD-	Z17
C6_RXD+	C6_RXD+	Z19
C6_TXD-	C6_TXD-	Z29
C6_TXD+	C6_TXD+	Z31

Extra Baud Rate Generator Clocks in VG5 V2.x (and above)

VG5 Version 2.x and higher have the possibility of using a new oscillator (Node A: Q1070 and Node B: Q1080) as clock source for the baud rate generators, that supply the MPSCs in the MV64360 chipset.

The default clock for these oscillators is 80 MHz.

With this clock it is possible to select the maximum baud rate of 10 Mbit for the MPSCs COM3,COM5 and COM6. Each MPSC can be configured with a different baud rate clock.

Be aware that 12 Mbit is the maximum speed for the RS422 transceivers of COM3/5/6 and – so the maximum transmittable TxC/RxC is 6 MHz (→12 Mbit). 10 Mbit are only possible without using TxC and RxC and with configuring the baud rate generator and the used MPSC to clock recovery.
(See also the *Test Report: HDLC on VG5* Doc. Ref. VG5-007.)

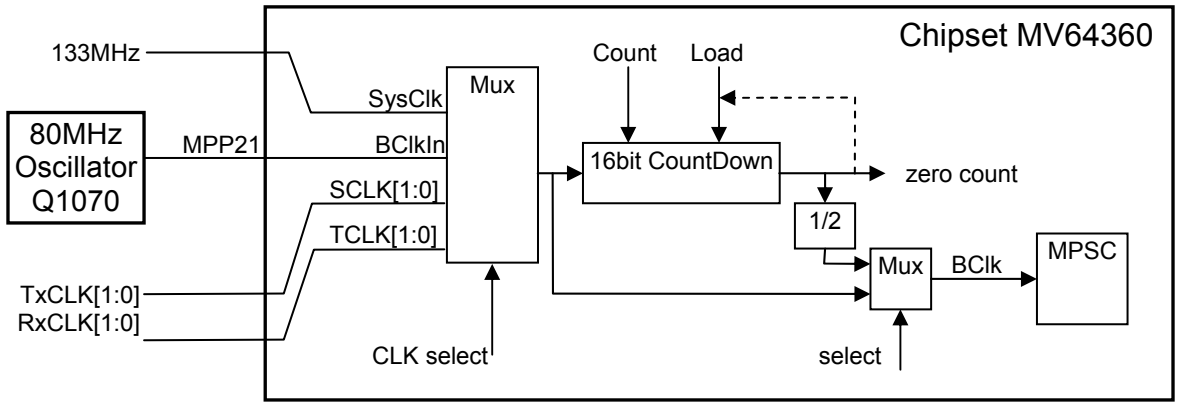


Figure 29: Baud Rate Generator for MPSCs

Attention: A termination resistor (typ. 120 Ω, 1 W) shall be foreseen when COM3,5,6 (and COM2 in RS422 mode) are used with high data rates or long cables. On the VTM20 transition module termination resistors can be mounted. See Table 70 and Figure 34 for details

The software (e.g VxWorks) determines by the Config Bits in the SysIN Register what Extra Baud Rate Generator clock is mounted. (see also Table 33)

Table 44: ConfigBit settings for Extra Baud Rate Oscillators in SysIn-Register

Node A					**Function of Q1070**
FPGA SysIn-Register [13:11]			mounted resistor		
Config2	Config 1	Config 0	R2501	R2500	
Rsv (1)	0	0	mounted	mounted	as VG5 V1.x no Extra Baud rate Clock (Q1070 not available)
Rsv (1)	0	1	mounted	n.m.	Q1070= 14,7456 MHz Custom W-Number, ask factory
Rsv (1)	1	0	n.m.	mounted	**Q1070= 80 MHz (Default for VG5 V2.x)**
Rsv (1)	1	1	n.m.	n.m.	Custom W-Number, ask factory (→ Frequency is stored in SPD E^2PROM)
Node B					**Function of Q1080**
FPGA SysIn-Register [15:14]			mounted resistor		
Config4	Config3		R2511	R2510	
0	0		mounted	mounted	as VG5 V1.x no Extra Baud rate Clock (Q1080 not available)
0	1		mounted	n.m.	Q1070= 14,7456 MHz Custom W-Number, ask factory
1	0		n.m.	mounted	**Q1070= 80 MHz (Default for VG5 V2.x)**
1	1		n.m.	n.m.	Custom W-Number, ask factory (→ Frequency is stored in SPD E^2PROM)

The following HDLC scenarios in NRZ coding are supported by the VG5 on COM3,5 and 6: (Remark: COM2 has a maximum baud rate of 250 kbit in RS422 mode)

Table 45: HDLC scenario's

data bit rate Mbps	RxClk line, TxClk line	clock recovery (oversampling, no RxClk used)
133 MHz system clock source		
all higher	-[1]	-[1,2]
16.625	-[1]	-[1]
8.3125	-[1]	✓
4.15625	✓	✓
all lower	✓	✓
80 MHz BCLKIN clock source, Q1070/Q1080 (standard for VG5 V2.1 and later)		
all higher	-[1]	-[1,2]
10	-[1]	✓
5	✓	✓
all lower	✓	✓

Notes:
1) Limiting factor 12 Mb/s throughput for RS422 transceivers as specified in Maxim's MAX1484 datasheet.
2) not possible because of minimum over sampling factor of 8 as given in Marvell's MV64360 datasheet.

Counter and Timer

There are four 32-bit wide timer/counters in each MV64360 chipset.
So the Dual Node VG5 configuration has 8 timer/counters in total, the Single Node configuration has 4 timer/counters in total.
Each timer/counter can be selected to operate as a timer or as a counter. Each timer/counter increments with every System Clock rising edge (System Clock=100 MHz or 133 MHz).
In Counter mode, the counter counts down to terminal count, stops, and issues an interrupt.
In Timer mode, the timer counts down, issues an interrupt on terminal count, reloads itself to the programmed value, and continues to count. Reads from the counter or timer are done from the counter itself, while writes are to its register. This means that read results are in the counter's real time value.
See details in the MV64360 datasheet, which is available from Marvell under NDA.

Additional to the Counters in the chipset the A/B watchdog counters in the FPGA can be used to generate an A/B_MCP interrupt after a given time. The A/B_WDGRSTMODE bits have to be set to 00 or a reset will occur after the watchdog expired. The time can be set with the A/B_WDGCOMP0
16-bit register in steps of 492 µs between 492 µs and about 32,3s. See details in chapter FPGA Watchdog Timer A/B.

Real Time Clock

The VG5 has a Real Time Clock (RTC) chip on-board at address offset + 00010h for address index and offset+0020h for data index. Offset is the programmed value of DevCS2 in the chipset.
The RTC provides a 100-year calendar with alarm function, a timer with periodic interrupt and 114 bytes of general purpose SRAM. In power-off state the RTC can be supplied from the VMEbus via the +5 VSTDBY (+4.85 V to 5,25 V) voltage. The maximum battery supply current is 3 µA (typ 1 µA).

COP Interface

The COP (Common On-chip Processor) interface of the PowerPC processor provides a serial interface for boundary scan and special interface for debug and control. The VG5 has for each CPU node a separate COP interface. Both COP interfaces are connected as follows:

- Access COP A via 16-pin connector P1100 with 1.27 mm grid near the front or via optional P1101 with 2.54 mm grid in the PMC2 area.
- Access COP B via 16-pin connector P1150 with 1.27 mm grid near the front or via optional P1151 with 2.54 mm grid in the PMC2 area.
- Both COP interfaces are wired to the P2 connector but shared with PMC2 IO signals

PMC Interfaces

The VG5 allows the installation of up to two additional PMC modules with user defined IO routed to P0 for PMC1 and P2 for PMC2. Some PMC1 IO signals and all PMC2 IO signals are shared with other signals see section PMC Slot 1 connectors (P7101, P7102, P7103), PMC Slot 2 connectors (P7201, P7202) for pin assignment.
Both PMCs are 64 bit, PMC1 is connected to Node A and has a maximum performance of PCI 66 MHz. PMC2 belongs to Node B (or in single node it is connected to the second PCI bus of Node A) and has a maximum PCI 33 MHz performance.
PMC1 (64 bit 33/66 MHz) is keyed for +3.3 V VIO and PMC2 (64 bit 33 MHz) is keyed for +5 V VIO.

PMC Power Requirements

The VG5 board provides +5 V, +3.3 V, and +/-12 V to the PMC connectors. The +5 V and + 3.3 V is limited by the max possible power consumption of PMC module to 7.5 W each. +/-12 V is limited by the thickness of the power traces. The VME backplane has to provide +5 V, +3.3 V and +/-12 V.
The maximal current for each voltage is defined in the table below.

Table 46: PMC Power Requirements

Voltage	Max. current for single PMC	Max. current for both PMCs
+5 V	1.5 A	3.0 A
+3.3 V	2.3 A	4.6 A
+12 V	0.5 A	0.5 A
-12 V	0.5 A	0.5 A

Serial ATA

The VG5 has implemented one serial ATA channel to support one serial ATA device and has following features.
• Integrated Serial ATA Link and PHY logic
• Compliant with Serial ATA 1.0 specifications
• Supports Serial ATA Generation 1 transfer rate of 1.5 Gb/s.
• Supports Spread Spectrum in receiver
• Programmable drive strengths for Backplane applications

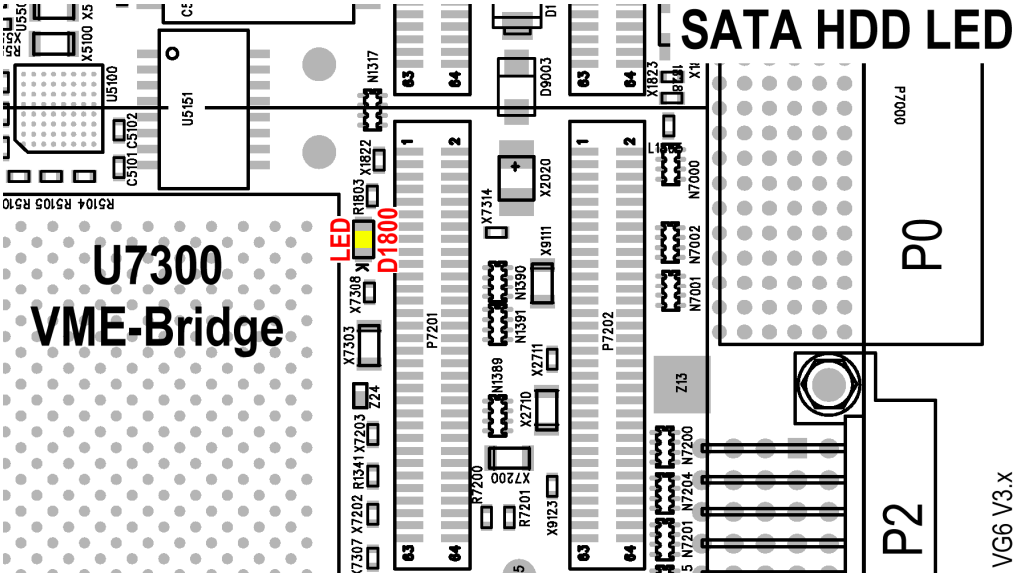


Figure 30: Location of SATA LED D1800

The SATA LED is bright yellow when the SATA hard disk is accessed. It is located on the board component side close to VME bridge and P0, P2 connector edges (see figure above).

The serial ATA signals are available at P0 and are shared with some of the PMC1 IO signals.

Ethernet Interfaces

Each of the Marvell Chipsets has two Ethernet MAC controllers, which have Gigabit Ethernet capability. On the VG5 each node implements a Fast Ethernet and Gigabit Ethernet PHY Transceiver. The MAC addresses of the Ethernet ports are stored in the SPD serial EEPROM.

All Ethernet signals are available at the rear IO connector P0 and P2, alternatively both Ethernet ports of Node A are also available at the front IO via RJ45 connectors.

The link status of all 4 Ethernet channel is available at the rear IO of P2, but these signals are shared with PMC2 IOs. At the front RJ-45 connectors each interface has two LEDs to indicate link and speed status.

Table 47: Ethernet LED indicators

Eth1	Green LED	Yellow/green LED
	on: Link	yellow: 1000 Mbit
	off: no Link	green: 100 Mbit
	blink: TX/RX activity	off: 10 Mbit or none

Eth2	Green LED	Yellow LED
	on: 10 Mbit	on: Link
	off: 100 Mbit	off: no Link

VMEbus Interface

The VG5 provides the UniverseII VMEbus interface chip. It contains a complete high performance 64-bit VMEbus interface with 64-bit PCI master/slave capability. Furthermore a system controller is implemented to allow the VG5 to reside in slot 1 without the necessity of an extra system controller.
The VME controller is controlled by the Node B PCI-bus (dual node) but may also controlled via the interconnection PCI bus by Node A.

Universe Register

All of the controlling registers are located in the UniverseII. The registers are memory mapped and after Power-On the base address is assigned dynamically by the software. 64 kBytes address space is reserved but only the first 4 kBytes are used.

Universe PCI bus Address Space

By default the VMEbus interface is disabled. In this case the PCI address space reserved for the VMEbus is available. If the VG5 needs to access the VMEbus, the VMEbus logic must be enabled and the PCI address spaces must be defined. Multiple PCI to VMEbus address space mappings with different attributes (A16, A24, D16, D32, User, ...) are possible.

Universe VMEbus Address Space

VMEbus address space may be defined when an other VMEbus master needs to access internal memory. Any location accessible over the PCI bus can be used.

Local Interrupt

UNIVERSE Interrupt line LINT 0 may be assigned by Setup to one free internal interrupt. Interrupt sharing with other PCI devices may be allowed when all interrupt lines support level driven mode (typical for PCI devices) and all interrupt service handler are known of this feature. The other seven interrupt lines LINT 1 .. LINT 7 are not connected.

Features

- Fully compliant, 64-bit, 33 MHz PCI local bus interface
- Fully compliant, high performance 64-bit VMEbus interface
- Integral FIFOs for write posting to maximize bandwidth utilization
- Programmable DMA controller with linked list support
- VMEbus transfer rates of 60 MBytes/sec
- Complete suite of VMEbus address and transfer modes
- A32/A24/A16 master and slave
- D64 (MBLT)/D32/D16/D8 master and slave
- BLT, ADOH, RMW, LOCK
- Flexible register set, programmable from both the PCI and VMEbus ports
- Full VMEbus system controller functionality

Programming

For detailed information about programming the UNIVERSE refer to 'VMEbus Interface Components Manual UNIVERSE' available from Tundra Semiconductor Corporation. This manual can be downloaded from the Tundra web site (http://www.tundra.com) in PDF-Format. The web site also contains sample code for the first initialisation.

GE Intelligent Platforms also recommends reading carefully the device errata available on the VG5 utility disk.

Two-Wire-Serial-Interface (TWSI) Devices

The VG5 uses two (dual node) or one (single node) Two-Wire-Serial-Interface TWSI to communicate with several onboard devices. The TWSI master is the corresponding chipset of Node A or B.

Table 48: TWSI Devices Node A and B Addresses

Device Node A (dual node)		**VG5 TSWI address**
Chipset Init 8 kByte EEProm		1010 000X b
SPD and Factory 512 Byte EEProm		1010 10YX b
U1305: NVRAM User EEProm: 128 kByte		1010 01YX b
Near CPU A Temperature sensor	(ThermoA)	1001 111X b
Centre board Temperature sensor	(ThermoC)	1001 101X b
DS3905 non volatile switch, EEPoti		1010 110X b
U1960 ADS7828 8channel ADC 12 bit	V2.x and higher	1001 001X b
Device Node A (single node) in addition to Devices Node A (Dual)		
Near CPU B Temperature sensor	(ThermoB)	1001 110X b
Device Node B (dual node)		
Chipset Init 8 kByte EEProm		1010 000X b
SPD 512 Byte EEProm		1010 100X b
NVRAM User EEProm	128 kByte	1010 01YX b
Near CPU B Temperature sensor	(ThermoB)	1001 110X b

Notes:
Y = bit in address not hardwired – set by software
X = Read or Write bit
b = the number before is binary
x = version number

Chipset Init EEPROM

Each chipset has an serial EEPROM of 8 kByte for storage of pre-initialisation values for the chipset. These values are read and stored in the appropriate chipset register after reset. Chipset Init and Factory/SPD EEPROM are protected by an output port for unintentional writes.

SPD and Factory EEPROM

For storage of factory SDRAM data a serial EEPROM is implemented on the VG5 board. This 512 Byte EEPROM stores the data according to the PC SDRAM Serial Presence Detect (SPD) Specification and also factory data like MAC addresses, serial number, variants are stored in this device. Chipset Init and Factory/SPD EEPROM are protected by an output port for unintentional writes. Reprogramming is not permitted.

NVRAM - User Serial EEPROM

The NVRAM is build with a serial EEPROM and is used for storage of user data. The size depends on VG5 Board Version: up to 128 kByte at each Node. These devices are protected by an output port against unintentional writes.

Bit A_WP_NV in register A_SYS_OUT protects the NVRAM for Node A and bit B_WP_NV in register B_SYS_OUT protects the NVRAM for Node B. See Table 34 and Table 35).

Temperature Sensor

Three National Semiconductors LM75 temperature sensor are implemented on the VG5 board. The sensors are located close to the CPUs and one in mid board area and show the board temperature at this locations. The sensor has an over-temperature output integrated, which can be used to take actions like reducing the CPU power.

See temperature sensor locations in Table 48:

Thermo A: U1302 near CPU A
Thermo B: U1352 near CPU B (only mounted on dual node boards)
Thermo C: U1303 centre of VG5

Non-volatile Switches

For VG5 V1.0 – V1.2

The three programmable resistors of a Dallas DS3905 (U1306) are used as non-volatile switches:

H0 controls the function of the VMEbus Reset. It depends also of the setting of Jumper J7300.

J7300:

1-2 set "Software Mode"
If H0 = Low (0) then VG5 cannot generate resets on the VMEbus
If H0 = High-Z (1) then VG5 can generate resets on the VMEbus

2-3 set Independent of H0 VG5 can always generate resets on the VMEbus (default)

non set VMEbus reset is never generated

H1 controls the direction of the VME System Clock :

H1= Low (0): clock coming from VMEbus
H1= High-Z (1): VG5 supplies clock (default)

Attention:
the VME clock is normally supplied by the VME system controller board in the VME-bus rack – if you have the VG5 as a second CPU board in the rack and not in the first populated slot, you have to set H1=0 , or the VME-Clock is possibly driven by 2 boards.
This 'feature' is removed in VG5 V1.3 , In VG5 V1.3 the clock is only supplied by the VG5, when it is VME system controller (in the first populated slot).

H2 is not used (reserved)

☞ See the API description in the VxWorks Board Support Package anual for using this VG5 features.

☞ This Feature (U1306, J7300 Auto Mode) is only available with VG5 version 1.0-1.2

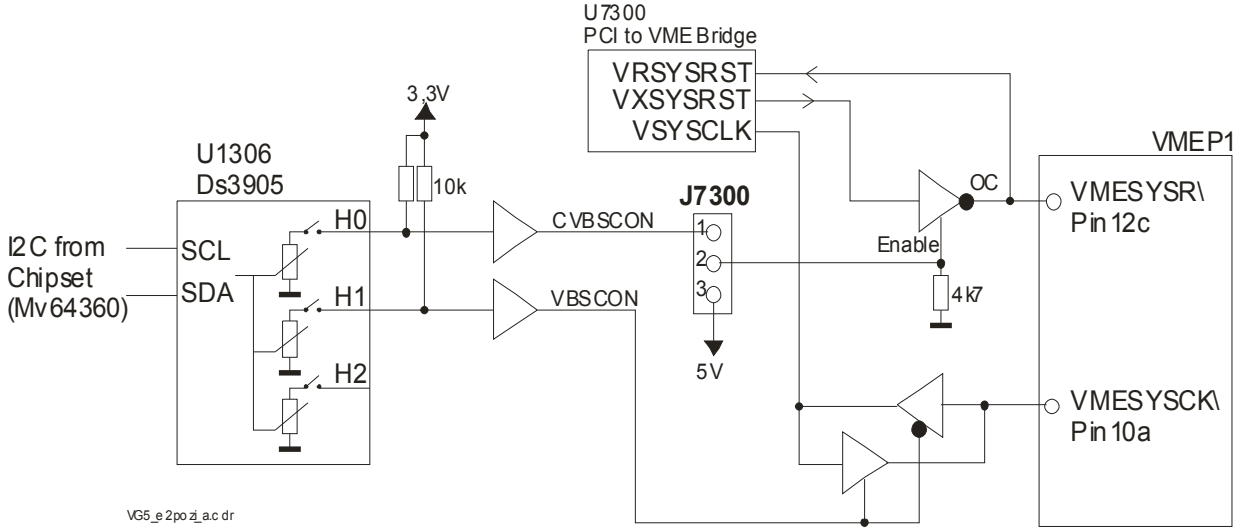


Figure 31: Blockdiagram: Non-volatile switches in V1.0-V1.2

See also chapter VME Reset Jumper.

For VG5 V1.3 and higher

The three programmable resistors of a Dallas DS3905 (U1306) are used as non-volatile switches:

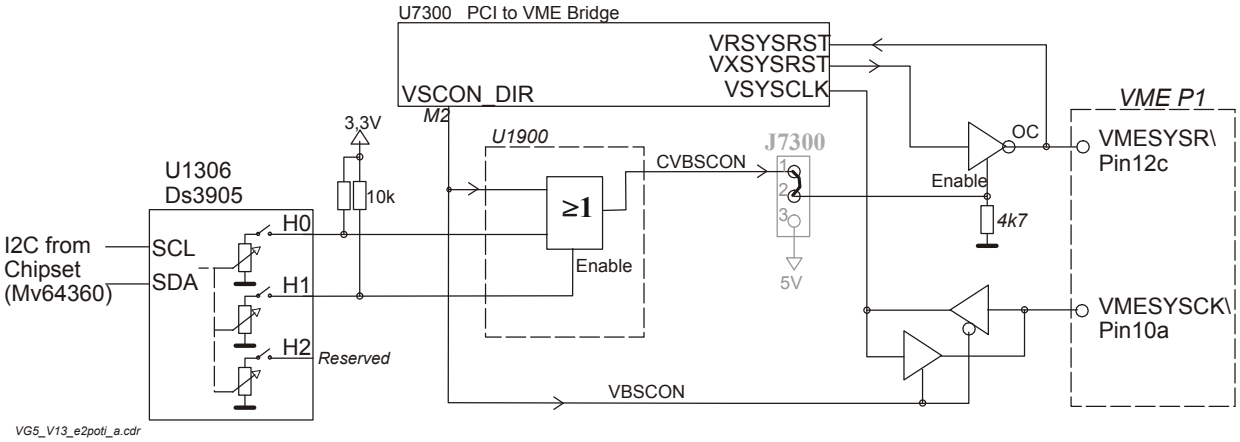


Figure 32: Blockdiagram: Non-volatile switches and J7300 in V1.3 and higher

H0 and H1	outputs of the U1306 control the VMEbus reset strategy of the VG5.
H2	is reserved for future use

Table 49: Non-volatile switches in V1.3 and higher

U1306 pin H1	U1306pin H0	Function
Low	Low	VG5 will never generate a VME-Reset
Low	High-Z	VG5 will never generate a VME-Reset
High-Z	Low	If VG5 is VME system controller, a VME Reset can be generated
High-Z	High-Z	VG5 can always generate a VME-Reset

☞ See the API description in the VxWorks Board Support Package Manual for using this VG5 features.

With PMON2000 V2.1#7 easy setting of J7300 is possible:

At PMON command prompt: type h and you will get a help screen
The command J7300 can be found under 'GE Intelligent Platforms VG5 hardware specific'.

Syntax: `J7300 [close12 | close 23 | open ]`
`J7300 close12` VMEbus reset will be generated if master (system controller)
`J7300 close23` VMEbus reset will be generated regardless if master
`J7300 open` no VMEbus reset will be generated

See also chapter VME Reset Jumper.

Analog Digital Converter (VG5 2.x and above)

The Analog Digital Converter (ADC) a has 12 bit resolution and eight channels.
The used ADC is a ADS7828 (Texas Instruments, BurrBrown). The internal reference voltage of 2.5 V is used.

Table 50: ADC

ADC-Channel	Measured Voltage	Readout for nom. voltage in Hex	Voltage Divider	Precision	Remark
0	+5 V	0xAAA	/ 3	1.33 %	Off board generated
1	+3.3 V	0xA8F	/ 2	1 %	Off board generated
2	+2,5 V	0x800	/ 2	1 %	DDR-SDRAM, L3-CacheIO, …
3	+1,8 V	0xB85	n/a	12 bit	MV64360 and FPGA Core Voltage
4	V_{TTA}=1,25 V	0x800	n/a	12 bit	DDR-SDRAM A Termination
5	V_{CCPA}=1,1 V V_{CCPA}=1,3 V	0x851 0x70A	n/a	12 bit	Node A: CPU-Core Voltage: 7457 up to 1 GHz all 7455 and 7457 1266 MHz
6	V_{CCPB}=1,1 V V_{CCPB}=1,3 V	0x851 0x70A	n/a	12 bit	Node B: CPU-Core Voltage: 7457 up to 1 GHz all 7455 and 7457 1266 MHz
7	1.2 V	0x7AE	n/a	12 bit	Gigabit PHY core voltage

A 12-bit ADC has decimal Values 0..4095 or 0x0..0xFFF

LED

The VG5 has three LED indicators at the front panel. The two red LEDs are Card Fail of CPU A and/or B. After reset, the LEDs are turned on by hardware and turned off if the boot loader sequence was performed successfully. (E.g.: The Card Fail LED of CPU A will be on if the boot flash will be corrupt and no boot code could be loaded)
During application these LEDs can be used for any user-defined purpose. Both red LEDs are also available at the rear connector P2 (z5 and z7). The both card fail LEDs are used by the BOOTSEL jumpers too, if a boot selector jumper is closed the LED will always lit.
The third LED is a green LED for user purposes. After reset it is off and can be used by any application.

Table 51: LEDs and their registers

LED Front	Owner	Pin Name	Register/Bit Name/Bit No.	Remark
CPU A Red	Node A	A_LED/Bootsel	A_SYS_OUT / A_LED / 2	See Table 34 in chapter FPGA System I/O
CPU B Red	Node B (Dual Node VG5)	B_LED/Bootsel	B_SYS_OUT / B_LED / 2	See Table 35 in chapter FPGA System I/O
	Node A (Single Node VG5)		A_SYS_OUT / B_LED / 17	See Table 34 in chapter FPGA System I/O
Green	Node A	A_LED_GR	A_SYS_OUT / A_LED / 3	See Table 34 in chapter FPGA System I/O

Reset Button

A push button at the front of the VG5 will release a hard reset. The reset signal is active for all subsystems of the VG5. Additionally the reset signal RST_BUT (open collector) at P0-a19 can release a reset from the backplane. (RST_BUT connected to GND will release a RESET).

The hard reset can also be released by the reset button on the VTM20 transition module.

See also chapter Reset for more details on reset.

CHAPTER 5 **Transition Module VTM20**

Chapter Scope

The VTM20 is a transition module which is used to route IO signals from the VG5 Single Board Computer to interface to external peripherals. The transition module is a 6U x 80 mm rear IO module which has to be plugged into the VG5 slot with the backplane in between. Make sure that your selected chassis supports this type of rear IO transition module. Please notice that many IO signals have alternative functions, so the interface signals are only available if the corresponding interface signals are provided by the VG5 board.
The VTM20 transition module is compliant with IEEE 1101.11-1998.

The +5 V and +3,3 V power available at connectors are protected by over current circuits.
The +12 V and –12 V power (if needed by PIM modules) must be protected by the user, e.g. with a 1 A fuse (fast type).

Overview of available connectors on this module :
(depending on the configuration not all connectors may be available).

Transition Module front panel connectors
- Three Ethernet RJ45 connectors with LED's for link status
- Reset button
- Slot opening for two PMC IO Modules (PIM)

Transition Module onboard connectors
- COM1 to COM6 10-pin headers
- Ethernet 2 10-pin header
- COP A and COP B Interface 16-pin header
- PMCIO IO connectors of PMC1 and PMC2 with 64-pin header
- General Purpose IO +5 V tolerant at a 34 pin header
- Serial ATA connector compliant to SATA specification
- Miscellaneous 10-pin header
- JTAG interface at a 10 pin header
- +12 V, -12 V and GND terminals for external power supply

The following chapters describe the connectors and interfaces in detail.

VTM20 V1.x

Top Side

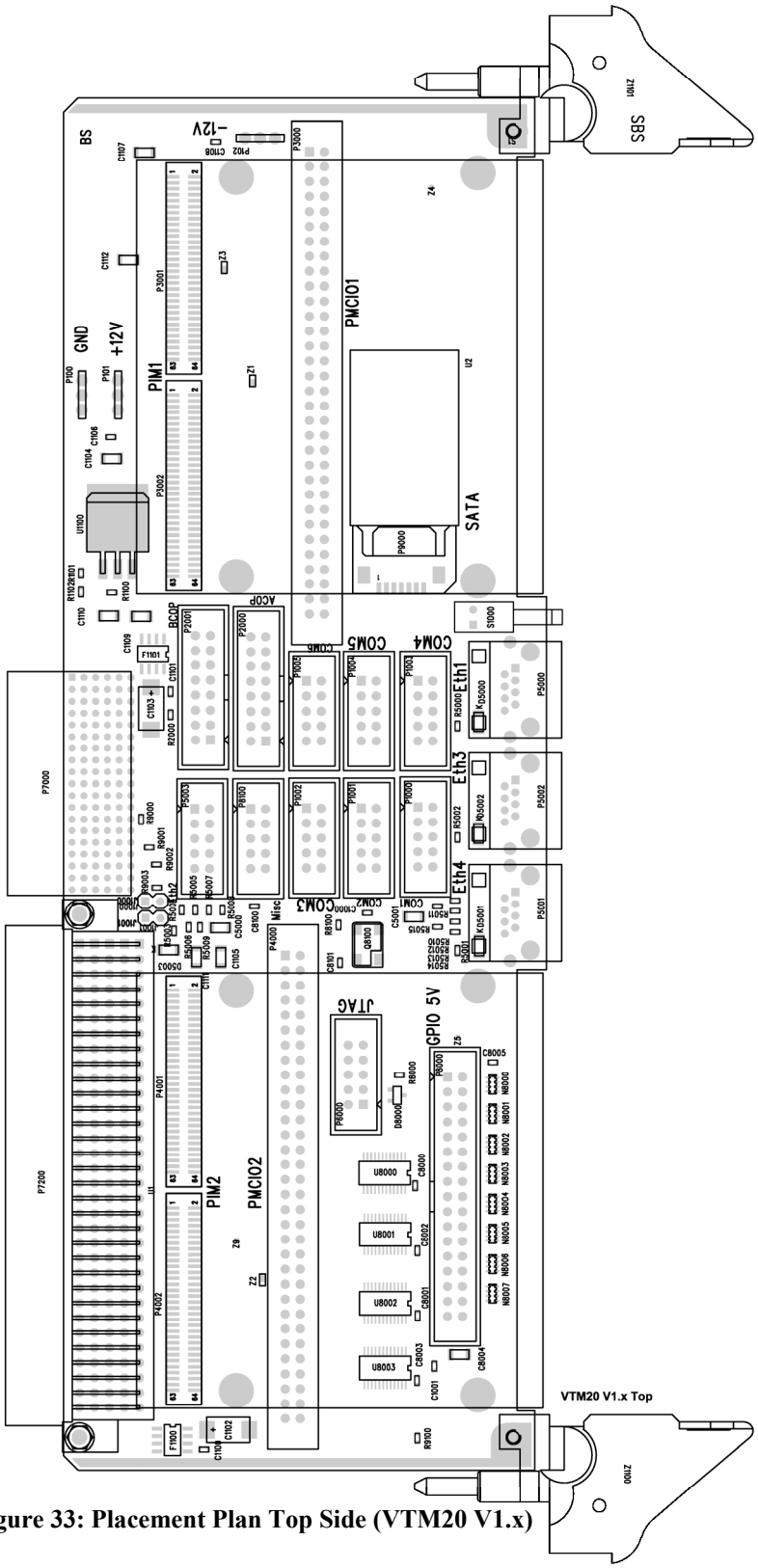


Figure 33: Placement Plan Top Side (VTM20 V1.x)

VTM20 V1.x

Bottom Side

See Chapter Serial Interfaces COM1...COM6 P100x RS422/RS485 Termination "RS422 / RS485 Termination" for details to resistor R7000-R7007.

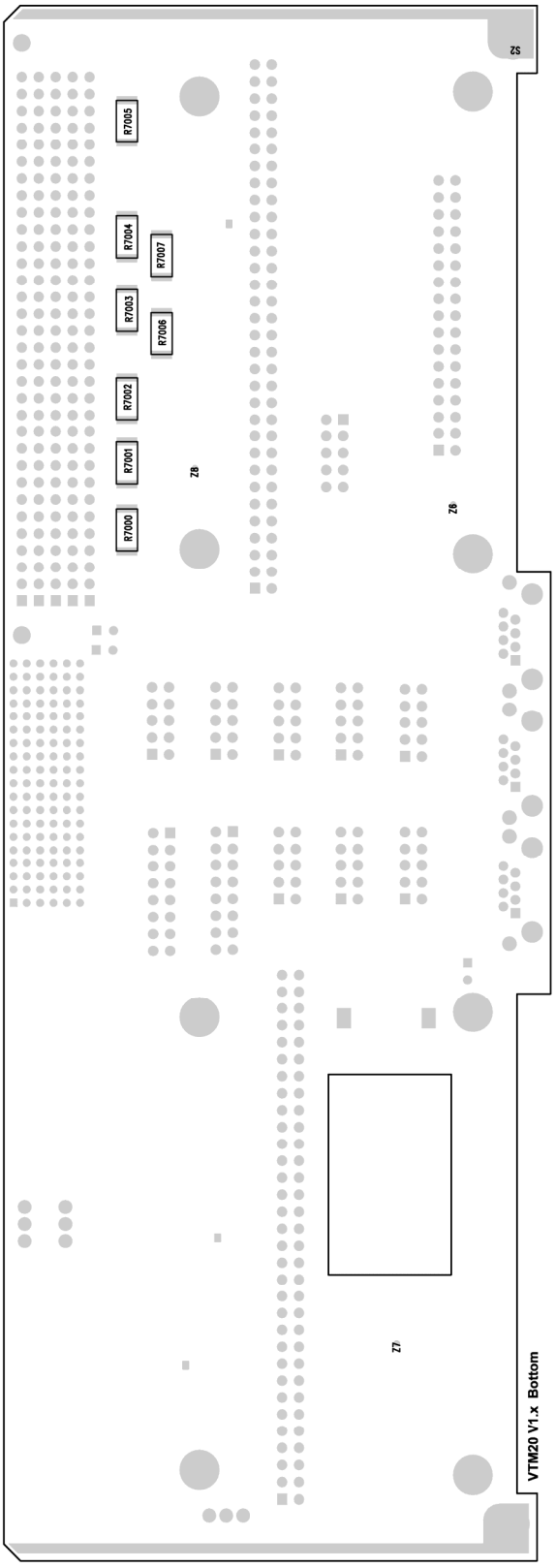


Figure 34: Placement Plan Bottom Side (VTM20 V1.x)

Connectors

Backplane Connectors P0/P2

The transition module can be connected to a VME64 backplane using the user defined pins at P0 and P2.

P0 Connector P7000

Table 52: TM P0 Connector P7000

	a	b	c	d	e	f
1	GND	GND	GND	GND	GND	GND
2	**ETH1_DA+**	**ETH1_DA-**	GND	**ETH1_DC+**	**ETH1_DC-**	GND
3	**ETH1_DB+**	**ETH1_DB-**	GND	**ETH1_DD+**	**ETH1_DD-**	GND
4	**ETH3_DA+**	**ETH3_DA-**	GND	**ETH3_DC+**	**ETH3_DC-**	GND
5	**ETH3_DB+**	**ETH3_DB-**	GND	**ETH3_DD+**	**ETH3_DD-**	GND
6	GND	GND	GND	GND	GND	GND
7	PMC1_IO05	PMC1_IO04	PMC1_IO03	PMC1_IO02	PMC1_IO01	GND
8	PMC1_IO10	PMC1_IO09	PMC1_IO08	PMC1_IO07	PMC1_IO06	GND
9	PMC1_IO15	PMC1_IO14	PMC1_IO13	PMC1_IO12	PMC1_IO11	GND
10	PMC1_IO20	PMC1_IO19	PMC1_IO18	PMC1_IO17	PMC1_IO16	GND
11	PMC1_IO25	PMC1_IO24	PMC1_IO23	PMC1_IO22	PMC1_IO21	GND
12	PMC1_IO30	PMC1_IO29	PMC1_IO28	PMC1_IO27	PMC1_IO26	GND
13	PMC1_IO35	PMC1_IO34	PMC1_IO33	PMC1_IO32	PMC1_IO31	GND
14	PMC1_IO40	PMC1_IO39	PMC1_IO38	PMC1_IO37	PMC1_IO36	GND
15	PMC1_IO45	PMC1_IO44	PMC1_IO43	PMC1_IO42	PMC1_IO41	GND
16	PMC1_IO50	PMC1_IO49	PMC1_IO48	PMC1_IO47	PMC1_IO46	GND
17	PMC1_IO55	P1_IO54 GND	P1_IO53 GND	P1_IO52 GND	P1_IO51 GND	GND
18	PMC1_IO60	P1_IO59 GND	P1_IO58 ATA_TX+	P1_IO57 GND	P1_IO56 ATA_RX-	GND
19	RSTBUT#	P1_IO64 GND	P1_IO63 ATA_TX-	P1_IO62 GND	P1_IO61 ATA_RX+	GND

P2 Connector P7200

Table 53: TM P2 Connector P7200

	z	a PMCIO or VG5 function::		b	c PMCIO or VG5 function:			d user defined
		VG5_Func.	PMC2_IO		VG5_Func.		PMC2_IO	
1	C2_DCD/TXD-	Geth1_LED	PMC2_IO02	+5 V	Geth3_LED		PMC2_IO01	Eth2_TxD-
2	GND	Eth2_LED	PMC2_IO04	GND	Eth4_LED		PMC2_IO03	Eth2_TxD+
3	C2_DSR/TXD+	CPUVIO	PMC2_IO06	-	WDG_REL	EXT16.66 MHz	PMC2_IO05	Eth2_RxD-
4	GND	ACOP_HRST#	PMC2_IO08	-	BCOP_HRST#		PMC2_IO07	Eth2_RxD+
5	LED A#/BOOTSEL	ACOP_SRST#	PMC2_IO10	-	BCOP_SRST#		PMC2_IO09	C2_CTS/RXC-/CTS-
6	GND	ACHKSTPOUT#	PMC2_IO12	-	BCHKSTP_OUT#		PMC2_IO11	C2_TXD/RXC+/CTS+
7	LED B#/BOOTSEL	ACOP_TCK	PMC2_IO14	-	BCOP_TCK	JTAG_TCK	PMC2_IO13	C2_RXD/TXC-/RTS-
8	GND	ACOP_TDI	PMC2_IO16	-	BCOP_TDI	JTAG_TDI	PMC2_IO15	C2_RTS/TXC+/RTS+
9	C1_RxD	ACOP_TMS	PMC2_IO18	-	BCOP_TMS	JTAG_TMS	PMC2_IO17	C2_RXD-
10	GND	ACOP_TRST#	PMC2_IO20	-	BCOP_TRST#	JTAG_TRST#	PMC2_IO19	C2_DTR/RXD+
11	C1_TxD	ACOP_TDO	PMC2_IO22	-	BCOP_TDO	JTAG_TDO	PMC2_IO21	Eth4_TxD-
12	GND	AQREQ#	PMC2_IO24	GND	BQREQ#		PMC2_IO23	Eth4_TxD+
13	C4_RxD	AQACK#	PMC2_IO26	+5 V	BQACK#		PMC2_IO25	Eth4_RxD-
14	GND	ACHKSTP_IN#	PMC2_IO28	-	BCHKSTPIN#		PMC2_IO27	Eth4_RxD+
15	C4_TxD		PMC2_IO30	-			PMC2_IO29	C3_RxD-
16	GND		PMC2_IO32	-			PMC2_IO31	C3_RxD+
17	C6_RxD-	UGPIO0	PMC2_IO34	-	UGPIO16		PMC2_IO33	C3_RXC-/CTS-
18	GND	UGPIO1	PMC2_IO36	-	UGPIO17		PMC2_IO35	C3_RXC+/CTS+
19	C6_RxD+	UGPIO2	PMC2_IO38	-	UGPIO18		PMC2_IO37	C3_TXC-/RTS-
20	GND	UGPIO3	PMC2_IO40	-	UGPIO19		PMC2_IO39	C3_TXC+/RTS+
21	C6_RXC-/CTS-	UGPIO4	PMC2_IO42	-	UGPIO20		PMC2_IO41	C3_TxD-
22	GND	UGPIO5	PMC2_IO44	GND	UGPIO21		PMC2_IO43	C3_TxD+
23	C6_RXC+/CTS+	UGPIO6	PMC2_IO46	-	UGPIO22		PMC2_IO45	C5_RXC-/CTS-
24	GND	UGPIO7	PMC2_IO48	-	UGPIO23		PMC2_IO47	C5_RXC+/CTS+
25	C6_TXC-/RTS-	UGPIO8	PMC2_IO50	-	UGPIO24		PMC2_IO49	C5_TXC-/RTS-
26	GND	UGPIO9	PMC2_IO52	-	UGPIO25		PMC2_IO51	C5_TXC+/RTS+
27	C6_TXC+/RTS+	UGPIO10	PMC2_IO54	-	UGPIO26		PMC2_IO53	C5_TxD-
28	GND	UGPIO11	PMC2_IO56	-	UGPIO27		PMC2_IO55	C5_TxD+
29	C6_TxD-	UGPIO12	PMC2_IO58	-	UGPIO28		PMC2_IO57	C5_RxD-
30	GND	UGPIO13	PMC2_IO60	-	UGPIO29		PMC2_IO59	C5_RxD+
31	C6_TxD+	UGPIO14	PMC2_IO62	GND	UGPIO30		PMC2_IO61	GND
32	GND	UGPIO15	PMC2_IO64	+5 V	UGPIO31		PMC2_IO63	+5 V (VPC)

Power Supply

The VTM20 is supplied from the backplane with +5 V only. This +5 V is used to generate +3.3 V via an intern linear voltage regulator. If +12 V and –12 V voltages are necessary these voltage has to be supplied to the transition module via terminals P100, P101, P102.

P100 GND
P101 +12 V
P102 -12 V

Power Supply Electrical Specification

The user must not exceed the current in the Transition Module as listed below.

Table 54: TM Power Ratings

Voltage	Maximum Current
+5 V	3.0 A
+3.3 V	1.0 A
+12 V	1.0 A
-12 V	1.0 A

Card Fail LED and Boot Select Jumper

The VTM20 has two jumper positions J1000 and J1001. The jumpers select the booting source of Node A and B. The boot behavior depends on the software installed in the boot flash (Flashbank 1). The boot software is responsible for the evaluation of the BOOTSEL jumper.

Due to limited pins at P0/P2 connector the boot select signals share the function with the card fail LEDs of CPU A and CPU B. If a jumper is closed the program will read and store the status of the boot select function, after this read function the signal will be an output and controls the card fail LEDs. That means if a jumper is closed the LED is in on-state as long the jumper is installed. The LED output is protected against this short circuit.
To connect a LED use a 680Ω serial resistor to +3.3 V.

Table 55: TM Boot Select jumper

J1000 open	**J1000 closed**
Node A will boot from default boot loader. The A_LED (CPU A, red) can be controlled by software	Node A will boot from emergency boot loader. The A_LED (CPU A, red) will be on and can not be controlled by software
J1001 open	**J1001 closed**
Node B will boot from default boot loader. The B_LED (CPU B, red) can be controlled by software	Node B will boot from emergency boot loader. The B_LED (CPU B, red) will be on and can not be controlled by software

Reset Button

A push button at the front of the VTM20 will release a hard reset. This reset button has the same function as the reset button at the VG5 front.

Ethernet Interfaces

The VG5 has a maximum of four Ethernet interfaces. Three of these four interface can be accessed via RJ45 8-pin connectors mounted at the transition module's front panel, the fourth interface via a 10 pin header.

Remark:
Eth1 (Node A, 100 Mbit) and Eth2 (Node A, 1000 Mbit) on the VTM20 have no function, if the VTM20 transition module is used in conjunction with a VG5 with Eth1 and/or Eth2 as front IO.

Table 56: VG5 Ethernet Variants

VG5 Variant with	VGTM20
no Ethernet	Eth1, Eth2, (Dual Node VG5: Eth3, Eth4) not functional
with Eth1 and Eth2 rear	both functional
with Eth1 front Eth2 rear	Eth2 port is functional
with Eth1 rear Eth2 front	Eth1 port is functional
with Eth1 front Eth2 front	Eth1 and Eth2 port are not functional
with Eth3 and Eth4 rear	Eth3 and Eth4 are available only on dual node VG5
with PMC2 rear IO	Ethernet LED function for Eth1-4 is not available on VTM20
with no PMC2 rear IO but GPIO, COP and Eth-LEDs	Ethernet LED function for Eth1-4 is available on VTM20

Gigabit Ethernet Connectors P5000, P5002

These two Ethernet connectors are Gigabit Ethernet (10/100/1000BaseTX) capable. The Ethernet interface at P5000 corresponds to the Node A and has the number Eth1, the Ethernet interface at P5002 correspond to Node B and has the number Eth3.

Note:
Pin assignments listed in brackets on P5000 and P5002 are possible assignments if this port is used in Fast Ethernet mode.

Table 57: TM Gigabit RJ45 Jacks

Name	**Ethernet1** P5000 **Ethernet3** P5002
ETHx_DA+ (TxD+)	1
ETHx_DA- (TxD-)	2
ETHx_DB+ (RxD+)	3
ETHx_DC+	4
ETHx_DC-	5
ETHx_DB- (RxD-)	6
ETHx_DD+	7
ETHx_DD-	8
FGND	9&10 Frame Ground

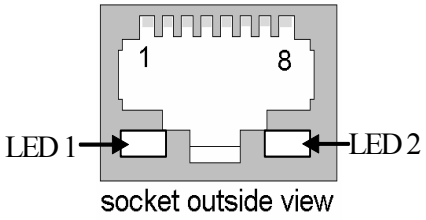


Figure 35: RJ45 Jack pinning and LEDs

LED1:	green	= link active
	off	= no link
LED2:	green	= 1000 Mbit link speed
	yellow	= 100 Mbit link Speed
	off	= 10 Mbit speed

Fast Ethernet Connectors P5001, P5003

These two Ethernet connectors are only Fast Ethernet (10/100BaseTX) capable. The Ethernet interface at P5001 corresponds to the Node A and has the number Eth4, the Ethernet interface at P5003 corresponds to Node B and has the number Eth2. Eth4 at P5001 is an RJ45 connector at the front panel and Eth2 at P5003 is available as a 10 pin header. The unused pin pairs are terminated with a resistor network.

Table 58: TM Fast Ethernet RJ45 Jack

Name	**Ethernet2** P5001
E4_TxD+	1
E4_TxD-	2
E4_RxD+	3
Term	4
Term	5
E4_RxD-	6
Term	7
Term	8
FGND	9&10 Frame Ground

Table 59: TM Fast Ethernet Header

Ethernet Signals	P5003
E2_TXD+	1
E2_TXD-	2
Term	3
Term	4
E2_RXD+	5
E2_RXD-	6
Term	7
Term	8
nc	9
nc	10

Link Status LEDs

Front IO option (Eth1, Eth2):

A green Link Status LED (LED1) and a green/yellow Link Speed LED (LED2) are integrated into the RJ45 Ethernet jack. (See Figure 35)

Rear IO option (via VTM20 Transition Module)

Eth1, Eth3, Eth4: Only the green Link LED (LED1, see Figure 35) is integrated in the RJ45 Ethernet jack. A Link Speed LED is not available.

Eth2: Ethernet signals are located on a 10 pin header (P5003). The Link LED (D5000) is located on the Transition Module PCB next to P5003. A Link Speed LED is not available.

Important: All four Link status signals are shared with PMC IOs (see P2 pin assignment: Table 7). Depending on the VG5 variant and the matching VTM20 variant the LEDs are available. The customer has to take care of using the matching VTM20 transition module to his VG5. See table below.

Table 60: matching VTM variant for use of Link Status LEDs

VG5 variant with	matching VTM20 variant with
no PMC2, no PMC2 rear IO, with COM2 front, with COPA/B, GPIO, **Eth-LEDs**	no PIM2, GPIO, partly PMCIO2
PMC2 full rear IO, without COPA/B, GPIO, Eth-LEDs	no PIM2, no GPIO, full PMCIO2 **or** PIM2, no GPIO, no PMCIO2
PMC2 no rear IO with COPA/B, UGPIO, **Eth-LEDs**	no PIM2, GPIO, partly PMCIO2

Warning:
If you use a VG5 with PMC2 rear IO capability and a VTM20 with GPIO/COP functionality I/Os of the VTM20 or the PMC in PMC site 2 may be damaged or PMC-rear IO signals may be disturbed !

COP Debug and JTAG Interfaces P2000, P2001, P6000

Two 16pin headers P2000 and P2001 provide the COP debug interfaces for both PowerPC processors of the VG5. The COP A and B signals are shared with the PMC2_IO and JTAG interface. The VG5 variant determines which signal group is valid.

Table 61: TM COP A Header

A COP Interface	P2000	Remarks
PMC2_IO22/**ACOP_TDO**	1	
PMC2_IO26/**AQACK#**	2	
PMC2_IO16/**ACOP_TDI**	3	
PMC2_IO20/**ACOP_TRST#**	4	
PMC2_IO24/**AQREQ#**	5	
PMC2_IO06/**CPUVIOSense**	6	220 Ω to 2.5 V
PMC2_IO14/**ACOP_TCK**	7	
PMC2_IO28/**ACHKSTPIN#**	8	
PMC2_IO18/**ACOP_TMS**	9	
nc	10	
PMC2_IO10/**ACOP_SRST**#	11	
GND	12	
PMC2_IO08/**ACOP_HRST#**	13	
Key	14	
PMC2_IO12/**ACHKSTOPOUT#**	15	
GND	16	

Table 62: TM COP B Header

B COP Interface	P2001	Remarks
PMC2_IO21/JTAG_TDO/**BCOP_TDO**	1	
PMC2_IO25/**BQACK#**	2	
PMC2_IO15/JTAG_TDI/**BCOP_TDI**	3	
PMC2_IO19/JTAG_TRST/**BCOP_TRST#**	4	
PMC2_IO23/**BQREQ#**	5	
PMC2_IO06/**CPUVIOSENSE**	6	220 Ω to 2.5 V
PMC2_IO13/JTAG_TCK/**BCOP_TCK**	7	
PMC2_IO27/**BCHKSTPIN#**	8	
PMC2_IO17/JTAG_TMS/**BCOP_TMS**	9	
nc	10	
PMC2_IO09/**BCOP_SRST**#	11	
GND	12	
PMC2_IO07/**BCOP_HRST#**	13	
nc Key	14	
PMC2_IO11/**BCHKSTOPOUT#**	15	
GND	16	

Table 63: TM JTAG Header

JTAG Interface	P6000
PMC2_IO13/**JTAG_TCK**/BCOP_TCK	1
GND	2
PMC2_IO21/**JTAG_TDO**/BCOP_TDO	3
nc	4
PMC2_IO19/**JTAG_TRST**/BCOP_TRST#	5
PMC2_IO17/**JTAG_TMS**/BCOP_TMS	6
nc	7
nc	8
PMC2_IO15/**JTAG_TDI**/BCOP_TDI	9
GND	10

Serial Interfaces COM1...COM6 P100x

The signals of the six (6) serial interfaces are available at 10-pin headers P1000..P1005 .

COM1 and COM4 are RS232 only interfaces with transmit/receive capability. COM3, COM4 and COM5 are RS422/485 (sync/async) interfaces and additionally COM2 can be either RS232 (sync/async) or RS422/485 (sync/async). The function of these interfaces is determined by the VG5.
Some COM interface headers have a +5 V voltage (VCC) at pin 10. This power supply is fused by a 2 A electronic fuse and should not exceed 100 mA per interface.

COM1 P1000

COM1 is an RS232 interface at P1000.

Table 64: TM COM1

COM1	P1000	Remarks
-	1	
-	2	
C1_RXD	3	
-	4	
C1_TXD	5	
-	6	
-	7	
-	8	
GND	9	
VCC	10	Fused VCC

COM2 P1001

COM2 is a software selectable RS422/485 (sync/async) or RS232 (async) interface at P1001.

Table 65: TM COM2

COM2	P1001	RS-232 async	RS-422/485 async	RS-422/485 sync
C2_DCD/TXD-	1	DCD	TXD-	TXD-
C2_DSR/TXD+	2	DSR	TXD+	TXD+
C2_RXD/TXC-/RTS-	3	RXD	RTS-	TXC-
C2_RTS/TXC+ /RTS+	4	RTS	RTS+	TXC+
C2_TXD/RXC+/CTS+	5	TXD	CTS+	RXC+
C2_CTS/RXC-/CTS-	6	CTS	CTS-	RXC-
C2_DTR/RXD+	7	DTR	RXD+	RXD+
C2_RXD-	8	-	RXD-	RXD-
GND	9			
VCC	10	Fused VCC		

COM3 P1002

COM3 is an RS422/485 sync/async interface at P1002.

Table 66: TM COM3

COM3	P1002	RS-422/485 async	RS-422/485 sync
C3_TXD-	1	TXD-	TXD-
C3_TXD+	2	TXD+	TXD+
C3_TXC-/RTS-	3	RTS-	TXC-
C3_TXC+ /RTS+	4	RTS+	TXC+
C3_RXC+/CTS+	5	CTS+	RXC+
C3_RXC-/CTS-	6	CTS-	RXC-
C3_RXD+	7	RXD+	RXD+
C3_RXD-	8	RXD-	RXD-
GND	9		
VCC	10	Fused VCC	

COM4 P1003

COM4 is an RS232 interface at P1003.

Table 67: TM COM4

COM4	P1003	Remarks
-	1	
-	2	
C4_RXD	3	
-	4	
C4_TXD	5	
-	6	
-	7	
-	8	
GND	9	
VCC	10	Fused VCC

COM5 P1004

COM5 is an RS422/485 sync/async interface at P1004.

Table 68: TM COM5

COM5	P1004	RS-422/485 async	RS-422/485 sync
C5_TXD-	1	TXD-	TXD-
C5_TXD+	2	TXD+	TXD+
C5_TXC-/RTS-	3	RTS-	TXC-
C5_TXC+ /RTS+	4	RTS+	TXC+
C5_RXC+/CTS+	5	CTS+	RXC+
C5_RXC-/CTS-	6	CTS-	RXC-
C5_RXD+	7	RXD+	RXD+
C5_RXD-	8	RXD-	RXD-
GND	9		
VCC	10	Fused VCC	

COM6 P1005

COM6 is an RS422/422 sync/async interface at P1005.

Table 69: TM COM6

COM6	P1005	RS-422/485 async	RS-422/485 sync
C6_TXD-	1	TXD-	TXD-
C6_TXD+	2	TXD+	TXD+
C6_TXC-/RTS-	3	RTS-	TXC-
C6_TXC+ /RTS+	4	RTS+	TXC+
C6_RXC+/CTS+	5	CTS+	RXC+
C6_RXC-/CTS-	6	CTS-	RXC-
C6_RXD+	7	RXD+	RXD+
C6_RXD-	8	RXD-	RXD-
GND	9		
VCC	10	Fused VCC	

RS422 / RS485 Termination

There are provisions on the VTM20 transition module's bottom side (LS marked side) to terminate the RS-485 differential inputs RXC/CTS and RXD with 120 Ω (1 W SMD 2512 size) termination resistors.

Table 70: RS422 / 485 Termination Resistors

Termination Resistor	COM Port , Signal (sync/async)
R7000	C2 , RXC / CTS
R7001	C2 , RXD
R7002	C3 , RXD
R7003	C3 , RXC / CTS
R7004	C5 , RXC / CTS
R7005	C5 , RXD
R7006	C6 , RXD
R7007	C6 , RXC / CTS

See Figure 34 for placement of these resistors on VTM20.

PMC-IO connectors

The PMC IO signals of both PMC slots are either available at 64-pin male headers (P3000/P4000) or via VITA36 compliant PIM (PMC IO Module) connectors (P3001/P3002 and P4001/P4002). The availability of a PIM interface or 64-pin header is mutually exclusive.
The PMC IOs of PMC1 are shared with serial ATA signals, so either the PMCIO1 or the SATA function is available at the pins.

PMC1-IO connectors P300x
The following table lists the pin assignments of the onboard PIM1 P3001 and P3002 connectors.

Table 71: TM PIM1 connector

P3001	P3002	Pin	Pin	P3001	P3002
	PMC1_IO01	**01**	**02**	+12 V [3]	PMC1_IO02
	PMC1_IO03	**03**	**04**		PMC1_IO04
+5 V [1]	PMC1_IO05	**05**	**06**		PMC1_IO06
	PMC1_IO07	**07**	**08**		PMC1_IO08
	PMC1_IO09	**09**	**10**	+3.3 V [2]	PMC1_IO10
	PMC1_IO11	**11**	**12**		PMC1_IO12
GND	PMC1_IO13	**13**	**14**		PMC1_IO14
	PMC1_IO15	**15**	**16**		PMC1_IO16
	PMC1_IO17	**17**	**18**	GND	PMC1_IO18
	PMC1_IO19	**19**	**20**		PMC1_IO20
+5 V [1]	PMC1_IO21	**21**	**22**		PMC1_IO22
	PMC1_IO23	**23**	**24**		PMC1_IO24
	PMC1_IO25	**25**	**26**	+3.3 V [2]	PMC1_IO26
	PMC1_IO27	**27**	**28**		PMC1_IO28
GND	PMC1_IO29	**29**	**30**		PMC1_IO30
	PMC1_IO31	**31**	**32**		PMC1_IO32
	PMC1_IO33	**33**	**34**	GND	PMC1_IO34
	PMC1_IO35	**35**	**36**		PMC1_IO36
+5 V [1]	PMC1_IO37	**37**	**38**		PMC1_IO38
	PMC1_IO39	**39**	**40**		PMC1_IO40
	PMC1_IO41	**41**	**42**	+3.3 V [2]	PMC1_IO42
	PMC1_IO43	**43**	**44**		PMC1_IO44
GND	PMC1_IO45	**45**	**46**		PMC1_IO46
	PMC1_IO47	**47**	**48**		PMC1_IO48
	PMC1_IO49	**49**	**50**	GND	PMC1_IO50
	PMC1_IO51 [4]	**51**	**52**		PMC1_IO52 [4]
+5 V [1]	PMC1_IO53 [4]	**53**	**54**		PMC1_IO54 [4]
	PMC1_IO55	**55**	**56**		PMC1_IO56 [4]
	PMC1_IO57 [4]	**57**	**58**	+3.3 V [2]	PMC1_IO58 [4]
	PMC1_IO59 [4]	**59**	**60**		PMC1_IO60
-12 V [3]	PMC1_IO61 [4]	**61**	**62**		PMC1_IO62 [4]
	PMC1_IO63 [4]	**63**	**64**		PMC1_IO64 [4]

[1] +5 V fused supplied via VG5, max 2A
[2] +3.3 V generated from +5 V via a linear voltage regulator and fused max. 1 A
[3] +12 V, -12 V supplied via the terminal from external power connector P101, P102 max current 500 mA each
[4] not available with SATA option

The following table lists the pin assignment of the PMC1 IO signals of the 64-pin header P3000.

Table 72: TM PMC1 IO header

PMC1	P3000		PMC1
PMC1_IO01	1	2	PMC1_IO02
PMC1_IO03	3	4	PMC1_IO04
PMC1_IO05	5	6	PMC1_IO06
PMC1_IO07	7	8	PMC1_IO08
PMC1_IO09	9	10	PMC1_IO10
PMC1_IO11	11	12	PMC1_IO12
PMC1_IO13	13	14	PMC1_IO14
PMC1_IO15	15	16	PMC1_IO16
PMC1_IO17	17	18	PMC1_IO18
PMC1_IO19	19	20	PMC1_IO20
PMC1_IO21	21	22	PMC1_IO22
PMC1_IO23	23	24	PMC1_IO24
PMC1_IO25	25	26	PMC1_IO26
PMC1_IO27	27	28	PMC1_IO28
PMC1_IO29	29	30	PMC1_IO30
PMC1_IO31	31	32	PMC1_IO32
PMC1_IO33	33	34	PMC1_IO34
PMC1_IO35	35	36	PMC1_IO36
PMC1_IO37	37	38	PMC1_IO38
PMC1_IO39	39	40	PMC1_IO40
PMC1_IO41	41	42	PMC1_IO42
PMC1_IO43	43	44	PMC1_IO44
PMC1_IO45	45	46	PMC1_IO46
PMC1_IO47	47	48	PMC1_IO48
PMC1_IO49	49	50	PMC1_IO50
PMC1_IO51 [1)]	51	52	PMC1_IO52 [1)]
PMC1_IO53 [1)]	53	54	PMC1_IO54 [1)]
PMC1_IO55	55	56	PMC1_IO56 [1)]
PMC1_IO57 [1)]	57	58	PMC1_IO58 [1)]
PMC1_IO59 [1)]	59	60	PMC1_IO60
PMC1_IO61 [1)]	61	62	PMC1_IO62 [1)]
PMC1_IO63 [1)]	63	64	PMC1_IO64 [1)]

[1)] not available with SATA option

PMC2-IO connectors P400x

The PMC IO of PMC2 is shared with other signals so either the PMC2-IO or the other function is available at the pins.

The following table lists the pin assignments of the onboard PIM2 P4001/P4002 connector.

Table 73: TM PIM2 connector

P4001	P4002	Pin	Pin	P4001	P4002
	PMC2_IO01/Geth3_LED	01	02	+12 V [3]	PMC2_IO02/Geth1_LED
	PMC2_IO03/Eth4_LED	03	04		PMC2_IO04/Eth2_LED
+5 V [1]	PMC2_IO05/WDG_REL/EXT16.66 MHz	05	06		PMC2_IO06/CPUVIO
	PMC2_IO07/BCOP_HRST#	07	08		PMC2_IO08/ACOP_HRST#
	PMC2_IO09/BCOP_SRST#	09	10	+3.3 V [2]	PMC2_IO10/ACOP_SRST#
	PMC2_IO11/BCHKSTPOUT#	11	12		PMC2_IO12/ACHKSTPOUT#
GND	PMC2_IO13/BCOP_TCK/JTAG_TCK	13	14		PMC2_IO14/ACOP_TCK
	PMC2_IO15/BCOP_TDI/JTAG_TDI	15	16		PMC2_IO16/ACOP_TDI
	PMC2_IO17/BCOP_TMS/JTAG_TMS	17	18	GND	PMC2_IO18/ACOP_TMS
	PMC2_IO19/BCOP_TRST#/JTAG_TRST#	19	20		PMC2_IO20/ACOP_TRST#
+5 V [1]	PMC2_IO21/BCOP_TDO/JTAG_TDO	21	22		PMC2_IO22/ACOP_TDO
	PMC2_IO23/BQREQ#	23	24		PMC2_IO24/AQREQ#
	PMC2_IO25/BQACK#	25	26	+3.3 V [2]	PMC2_IO26/AQACK#
	PMC2_IO27/BCHKSTPIN#	27	28		PMC2_IO28/ACHKSTPIN#
GND	PMC2_IO29	29	30		PMC2_IO30
	PMC2_IO31	31	32		PMC2_IO32
	PMC2_IO33/UGPIO16	33	34	GND	PMC2_IO34/UGPIO0
	PMC2_IO35/UGPIO17	35	36		PMC2_IO36/UGPIO1
+5 V [1]	PMC2_IO37/UGPIO18	37	38		PMC2_IO38/UGPIO2
	PMC2_IO39/UGPIO19	39	40		PMC2_IO40/UGPIO3
	PMC2_IO41/UGPIO20	41	42	+3.3 V [2]	PMC2_IO42/UGPIO4
	PMC2_IO43/UGPIO21	43	44		PMC2_IO44/UGPIO5
GND	PMC2_IO45/UGPIO22	45	46		PMC2_IO46/UGPIO6
	PMC2_IO47/UGPIO23	47	48		PMC2_IO48/UGPIO7
	PMC2_IO49/UGPIO24	49	50	GND	PMC2_IO50/UGPIO8
	PMC2_IO51/UGPIO25	51	52		PMC2_IO52/UGPIO9
+5 V [1]	PMC2_IO53/UGPIO26	53	54		PMC2_IO54/UGPIO10
	PMC2_IO55/UGPIO27	55	56		PMC2_IO56/UGPIO11
	PMC2_IO57/UGPIO28	57	58	+3.3 V [2]	PMC2_IO58/UGPIO12
	PMC2_IO59/UGPIO29	59	60		PMC2_IO60/UGPIO13
-12 V [3]	PMC2_IO61/UGPIO30	61	62		PMC2_IO62/UGPIO14
	PMC2_IO63/UGPIO31	63	64		PMC2_IO64/UGPIO15

[1] +5 V fused supplied via VG5 max 2A

[2] +3.3 V generated from +5 V via a linear voltage regulator and fused max. 1A

[3] +12 V, -12 V supplied via the terminal from external power connectors P101 and P102 max current 500 mA each

The following table lists the pin assignment of the PMC2IO signals of the 64pin header P4000.

Table 74: TM PMC2 IO header

P4000	Pin	Pin	P4000
PMC2_IO01/Geth3_LED	01	02	PMC2_IO02/Geth1_LED
PMC2_IO03/Eth4_LED	03	04	PMC2_IO04/Eth2_LED
PMC2_IO05/WDG_REL/EXT16.66 MHz	05	06	PMC2_IO06/CPUVIO
PMC2_IO07/BCOP_HRST#	07	08	PMC2_IO08/ACOP_HRST#
PMC2_IO09/BCOP_SRST#	09	10	PMC2_IO10/ACOP_SRST#
PMC2_IO11/BCHKSTP_OUT#	11	12	PMC2_IO12/ACHKSTPOUT#
PMC2_IO13/BCOP_TCK/JTAG_TCK	13	14	PMC2_IO14/ACOP_TCK
PMC2_IO15/BCOP_TDI/JTAG_TDI	15	16	PMC2_IO16/ACOP_TDI
PMC2_IO17/BCOP_TMS/JTAGTMS	17	18	PMC2_IO18/ACOP_TMS
PMC2_IO19/BCOP_TRST#/JTAG_TRST#	19	20	PMC2_IO20/ACOP_TRST#
PMC2_IO21/BCOP_TDO/JTAG_TDO	21	22	PMC2_IO22/ACOP_TDO
PMC2_IO23/BQREQ#	23	24	PMC2_IO24/AQREQ#
PMC2_IO25/BQACK#	25	26	PMC2_IO26/AQACK#
PMC2_IO27/BCHKSTPIN#	27	28	PMC2_IO28/ACHKSTPIN#
PMC2_IO29	29	30	PMC2_IO30
PMC2_IO31	31	32	PMC2_IO32
PMC2_IO33/UGPIO16	33	34	PMC2_IO34/UGPIO0
PMC2_IO35/UGPIO17	35	36	PMC2_IO36/UGPIO1
PMC2_IO37/UGPIO18	37	38	PMC2_IO38/UGPIO2
PMC2_IO39/UGPIO19	39	40	PMC2_IO40/UGPIO3
PMC2_IO41/UGPIO20	41	42	PMC2_IO42/UGPIO4
PMC2_IO43/UGPIO21	43	44	PMC2_IO44/UGPIO5
PMC2_IO45/UGPIO22	45	46	PMC2_IO46/UGPIO6
PMC2_IO47/UGPIO23	47	48	PMC2_IO48/UGPIO7
PMC2_IO49/UGPIO24	49	50	PMC2_IO50/UGPIO8
PMC2_IO51/UGPIO25	51	52	PMC2_IO52/UGPIO9
PMC2_IO53/UGPIO26	53	54	PMC2_IO54/UGPIO10
PMC2_IO55/UGPIO27	55	56	PMC2_IO56/UGPIO11
PMC2_IO57/UGPIO28	57	58	PMC2_IO58/UGPIO12
PMC2_IO59/UGPIO29	59	60	PMC2_IO60/UGPIO13
PMC2_IO61/UGPIO30	61	62	PMC2_IO62/UGPIO14
PMC2_IO63/UGPIO31	63	64	PMC2_IO64/UGPIO15

Miscellaneous Connector P8100

A 10-pin header P8100 provides miscellaneous interface signals.

Table 75: TM Misc Connector

	P8100		
A_LED#/BOOTSEL#	1	2	B_LED#/BOOTSEL#
PMC2_IO29	3	4	PMC2_IO30
PMC2_IO31	5	6	PMC2_IO32
RST_BUT#	7	8	WDG_REL/EXT16.66/PMC2_IO05
Fused VCC3	9	10	GND

Serial ATA Connector P9000

The VTM20 provides one serial ATA compliant connector to support one SATA hard disk drive. The SATA signal are shared with PMC1IO signals, therefore this interface can only be used if the VG5 has the SATA option.

Table 76: TM Serial ATA connector

P9000	Pin
GND	1
ATA_TX+/PMC1_IO58	2
ATA_TX-/PMC1_IO63	3
GND	4
ATA_RX-/PMC1_IO56	5
ATA_RX+/PMC1_IO61	6
GND	7

User General Purpose IO +5 V P8000

At this connector the 32 User General Purpose IO (UGPIO) signals are available. The normal GPIO signals are available (shared with PMC2-IO) at connector P4000, but at this stage the GPIO is not 5 V tolerant (max 3,3 V).
Between P4000 and P8000 are bi-directional voltage level converters inserted for 5 V tolerant signals at the P8000 connector.

Table 77: TM UPGIO 5 V header

Name	P8000		Name
UGPIO00	1	2	UGPIO01
UGPIO02	3	4	UGPIO03
UGPIO04	5	6	UGPIO05
UGPIO06	7	8	UGPIO07
UGPIO08	9	10	UGPIO09
UGPIO10	11	12	UGPIO11
UGPIO12	13	14	UGPIO13
UGPIO14	15	16	UGPIO15
UGPIO16	17	18	UGPIO17
UGPIO18	19	20	UGPIO19
UGPIO20	21	22	UGPIO21
UGPIO22	23	24	UGPIO23
UGPIO24	25	26	UGPIO25
UGPIO26	27	28	UGPIO27
UGPIO28	29	30	UGPIO29
UGPIO30	31	32	UGPIO31
Fuse VCC	33	34	GND

CHAPTER 6 VG5 Tips and Tricks

Adapter Cables

Serial Port cables (RS232)

Connecting a PC as a Terminal to a VG5

Minimum necessary signals
(works at VG5 COM1 on P2710, and for COM1, 2 and 4 on the VTM20 transition module):

Table 78: Simple Null Modem

SUBD 9pin female (VG5 Side)		SUBD 9pin female (PC-side)	
Signal	**Pin**	**Pin**	**Signal**
RxD (in)	2	2	RxD (in)
TxD (out)	3	3	TxD (out)
Signal Ground	5	5	Signal Ground
Shield	-	-	Shield

Shield (recommended for better EMI)

Recommended cable length 3 m (at 115 kbit)

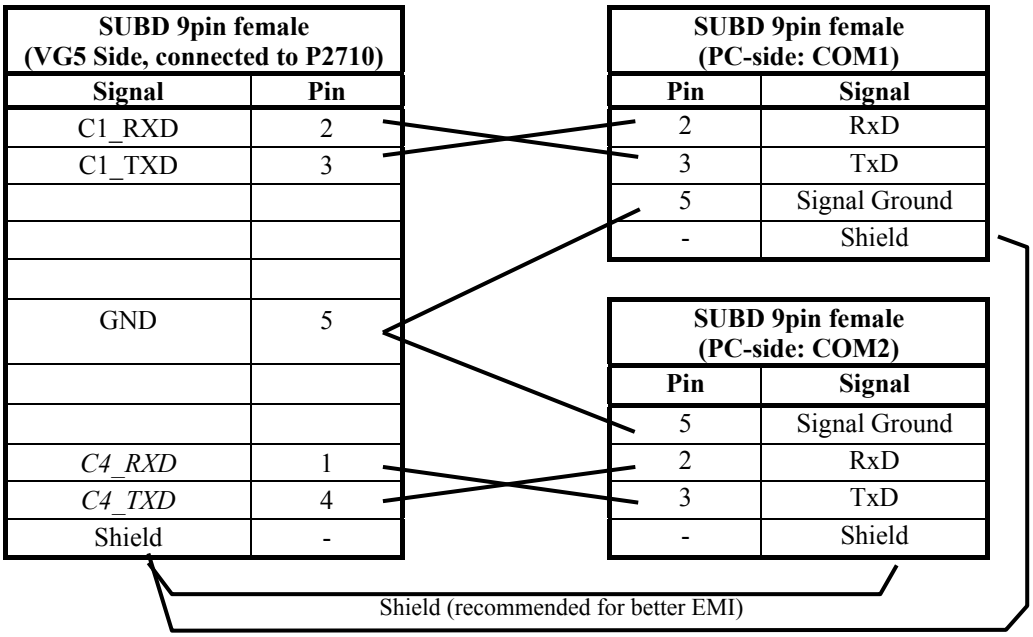
Legend:

C1	= Serial Port COM1	C2	= Serial Port COM2	C4	= Serial Port COM4
TxD	= Transmit Data	RxD	= Receive Data	GND	= Signal Ground
RTS	= Request To Send	CTS	= Clear To Send	DCD	= Data Carrier Detect
DSR	= DCE Ready	DTR	= DTE Ready	RI	= Ring Indicator

Connecting a PC as two Terminals to a VG5D (Dual Node) at P2710 (Front)
Necessary signals for a Splitter Cable with Null Modem included.
VG5 COM1 and COM2 connected directly to two PC COM Ports.

Recommended cable length 3m (at 115 kbit)

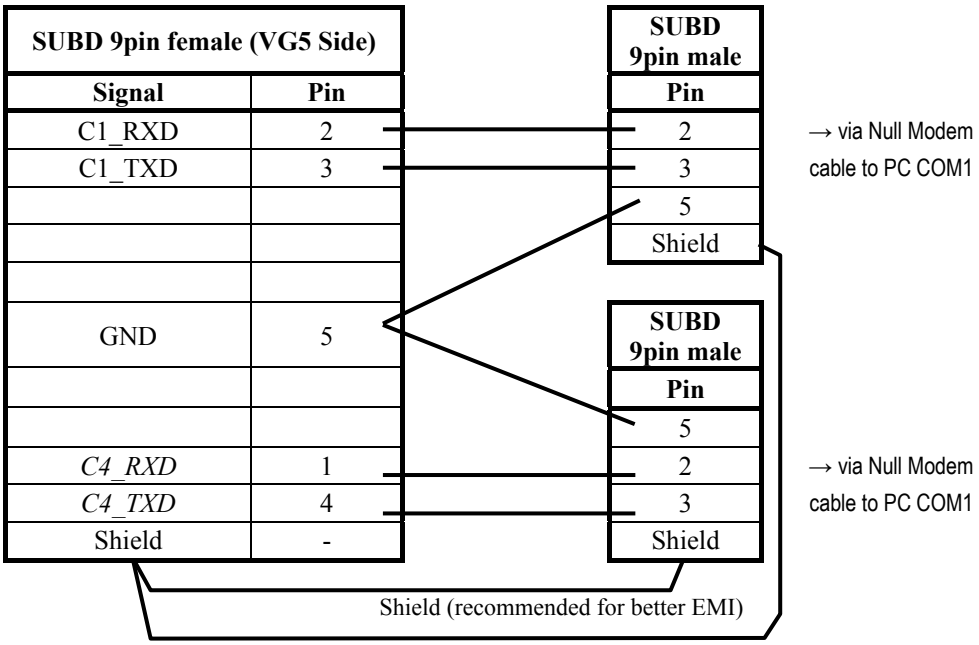
Table 79: Simple Null Modem for VG5D at P2710 (COM1/4)



Short Splitter Cable as an adapter to connect standard Null Modem cables.

Recommended cable length 0,2 m

Table 80: Splitter Cable for VG5D P2710 (Front, COM1/4)



CHAPTER 7 Specifications

Chapter Scope

This chapter contains information regarding specifications of the VG 5 product and variations.

Specification

PCB
FR4 Multilayer

Size
Total size: 1 board : 6U, 4HP

Dimensions
PCB: 233.35 mm x 160 mm x 20 mm

Weight:

VG5 single node C-, I- or 1-, 3-Style	440 g	(with frontpanel, heatsink)
VG5 dual node C-, I- or 1-, 3-Style	516 g	(with frontpanel, 2x heatsink)
VG5 N-, 8-Style single node	650 g	
VG5 N-, 8-Style dual node	675 g	(VG5DJ8II2231N)

Power Requirements

+5 V min 4.875 V max 5.25 V
+3.3 V min 3.25 V max 3.45 V
Requirement only for VG5 lower than version 2.x:
5 V and 3.3 V must be powered on/off simultaneously (<5 ms)
Max Power at VMEbus connectors: 1.25 A/pin @ 60 °C ambient:
+3.3 V with 10 pins at VME backplane can supply nominal 41 W
+5 V with 9 pins at VME backplane can supply nominal 56 W

Power Consumption
The table below helps customers to calculate the power consumption of a VG5 system. For measurement, the VG5 is mounted on a VME backplane, without any other IO interfaces. During

measurement, the power consumption of the backplane is ignored. The power is measured during VxWorks prompt when no application software is running.

Table 81: Power Consumption VG5 V1.x

Order No.	Typical current @ +5 V	Typical current @ +3.3 V	Typical total Power Consumption [4]	Remarks
VG5S J7xx xxxx x	3.3 A	2.4 A	25.0 W [1]	Single Node CPU 7455, 1000 MHz @ 133 MHz FSB 256 MB DDR-SDRAM
VG5S I7xx xxxx x	2.8 A	2.2 A	22.7 W [1]	Single Node CPU 7455, 800 MHz @ 133 MHz FSB 256 MB DDR-SDRAM
VG5S L7xx xxxx x	3.6 A	3.0 A	28.0 W [1]	Single Node CPU 7457, 1266 MHz @ 133 MHz FSB 256 MB DDR-SDRAM
VG5D J8xx xxxx x	5.8 A	5.6 A	47.5 W [2]	Dual Node CPU 7455, 1000 MHz @ 133 MHz FSB 2 x 512 MB DDR-SDRAM
VG5D N7xx xxxx x	3.5 A	5.66 A	36.2 W [2]	Dual Node CPU 7457, 867 MHz @ 133 MHz FSB 2 x 256 MB DDR-SDRAM
VG5D K7xx xxxx x	4.3 A	5.7 A	40.3 W [2]	Dual Node CPU 7457, 1000 MHz @ 133 MHz FSB 2 x 256 MB DDR-SDRAM
VG5D L7xx xxxx x	6.8 A	5.7 A	52.8 W [2]	Dual Node CPU 7457, 1266 MHz @ 133 MHz FSB 2 x 256 MB DDR-SDRAM

Table 82: Power Consumption VG5 V2.x and above

Order No.	Typical current @ +5 V	Typical current @ +3.3 V	Typical total Power Consumption [4]	Remarks
VG5S L8xx xxxx x	3.6 A	3.0 A	28.0 W [1]	Single Node CPU 7457, 1266 MHz @ 133 MHz FSB 512 MB DDR-SDRAM
VG5D L8II 2231 x	6.95 A	4,9 A	51 W [2]	Dual Node CPU 7457, 1266 MHz @ 133 MHz FSB 2 x 512 MB DDR-SDRAM
VG5D K8xx xxxx x	4.29 A	4.9 A	37.7 W [2]	Dual Node CPU 7457, 1000 MHz @ 133 MHz FSB 2 x 512 MB DDR-SDRAM
VG5D x8II 2231 x	3.24 A	4.9A	30.5 W [2]	Dual Node CPU 7457, 800 MHz @ 133 MHz FSB 2 x 512 MB DDR-SDRAM
VG5D x8II 2231 x	2.57 A	4.3A	27.1 W [3]	Dual Node CPU 7457, 600 MHz @ 100 MHz FSB 2 x 512 MB DDR-SDRAM no S-ATA Link, only 2x 100 MBit Link

Notes:

1) Node A VxWorks Prompt; eth1 100 Mbit link, eth2 1 Gbit link
(add for VME-Backplane (5slot) and VTM20 transition module ~1.7 A (5 V))
2) Node A+B: VxWorks Prompt; eth1,3 100 Mbit link, eth2,4 1 Gbit link
(add for VME-Backplane (5slot) and VTM20 transition module ~1.7 A (5 V))
3) Node A+B: VxWorks Prompt; eth1,3 100 Mbit link, eth2,4 no Gbit link
(add for VME-Backplane (5slot) and VTM20 transition module ~1.7 A (5 V))
4) at ambient conditions 25 °C, approximately 20% more Power at 85 °C

For these tests only the idle task is running (CPU load high, periphery load low).

External Battery Voltage for RTC

input range 4.875 V – 5.25 V, max. current @ 5.0 V, 3 µA
External battery connected via '+5 V STDBY' at P1 pin 31b. Typically the RTC will work down to 4 V at '+5 V STDBY'. Typically single voltage breakdowns up to 5 min at '+5 VSTDBY' won't cause loss of RTC settings.

Electrical clearance

Starting with board version 3.0 certain rules on spacing between conductors on individual layers of the printed circuit board (PCB) apply. The boards starting with version V3.x are designed to meet the parameters as listed below.

Voltage between conductors (DC or AC peaks) of 51 V – 100 V require a spacing of

- **0.6 mm for type B2 conditions**

external conductors, uncoated, sea level to 3050 m.

These rules are in accordance with IPC-2221 requirements.

Table 83: Environment

Environment	C-, 1-Style	I-, 3-Style	R-, 6-Style	N-, 8-Style
High Temperature [°C]				
Operating [1]:	←	see note below	→	see note below
Storage:	+85 °C	+85 °C	+105 °C	+105 °C
	← derating above 1 km altitude →			
☞ Note 1: Please refer to section **Thermal Behaviour** for more information.				
Low Temperature				
Operating	+0 °C	-40 °C	-40 °C	-40 °C
Storage	-40 °C	-40 °C	-55 °C	-55 °C
Rel. Humidity				
Operating		up to 95 % @ 40 °C, non-condensing		
Storage		up to 95 % @ 40 °C, non-condensing		
Altitude				
Operating	4.5 km	4.5 km	4.5 km	vacuum (ask factory)
Storage	12 km	12 km	12 km	vacuum (ask factory)
☞ Note: 4.5 km (15 000 ft.), 12 km (40 000 ft.)				
Shock				
Amplitude	12 g	12 g	20 g	100 g / 40 g
Duration	6 ms	6 ms	6 ms	6 ms / 11 ms
☞ Note: half sine (peak), 3 axis up & down, 5 hits / direction				
Vibration (operating)				
Spectrum	5 to 100 Hz	5 to 100 Hz	5 to 2000 Hz	5 to 2000 Hz
Acceleration	2 g_{rms}	2 g_{rms}	2 g_{rms}	14 g_{rms}
☞ Note: random, 30 min., 3 axis				

Table 84: Product ID Position 13 (Environments)

VG5 can come in some additional variants were the VG5 is coated.

Pos. 13 in Product ID Environm. Variant	Remark	Style-family	Type of cooling	Temperature # [°C]
C	C	C-, 1-Styles	Airflow	0…70 °C
D	Like C + Coating		Airflow	0…70 °C
E*	Like C + Stiffener		Airflow	0…70 °C
I	I	I-, 3-Styles	Airflow	-40 °C … 85 °C
H*	Like I + Coating		Airflow	-40 °C … 85 °C
R	Like I + Stiffener		Airflow	-40 °C … 85 °C
N	N	N-, 8-Style	Conduction Cooled	-40 °C … 85 °C

Note:

\# upper temperature limit depends on airflow (C-, I-, 1-, 3-Styles) and type of CPU

* like C + improved shock and vibration resistance

Thermal Behaviour

This section describes in short the thermal behavior of the VG5 boards. For more detailed information, please check the thermal report document of the VG5 (Doc Ref TR-HW-006 as well as the Addendum Doc Ref TR-HW-10, ask GE Intelligent Platforms Sales).

Thermal Condition Air Cooled Styles (C-, I-, 1-, 3-Styles)

The thermal condition of the C-, I-, 1-, 3-Style VG5 is for use in an airflow cooled environment. This means the maximum ambient temperature can only be achieved with sufficient airflow. The diagram below gives the maximal ambient temperature of the CPU (hottest spot) related to the forced airflow under worst case power condition.

☞ **Note:** Please note that the airflow must be valid for the complete board surface (front and rear side)
A mounted PMC Module changes the thermal behaviour of the VG5 board.

It is not recommended to operate the VG5 system without sufficient airflow. As the thermal situation depends on the actual power consumption and a defined airflow, which may be difficult to determine, there are some hints to determine the maximum operating temperature.

One hot spot at the VG5 board is the CPU under the heatsink. Under worst case power consumption the heatsink surface shall not exceed the specified value, which can be found in the figure below.
The curves show the delta temperature between CPU or Heatsink hotspot and ambient temperature.
E.g: with no PMCs : ambient = 50 °C; airspeed = 1.5 m/s → heatsink = 70 °C → CPU = 82 °C, 105 °C is the absolute maximum for the CPU – so we have a reserve of 105 °C - 82 °C = 23 K which is OK

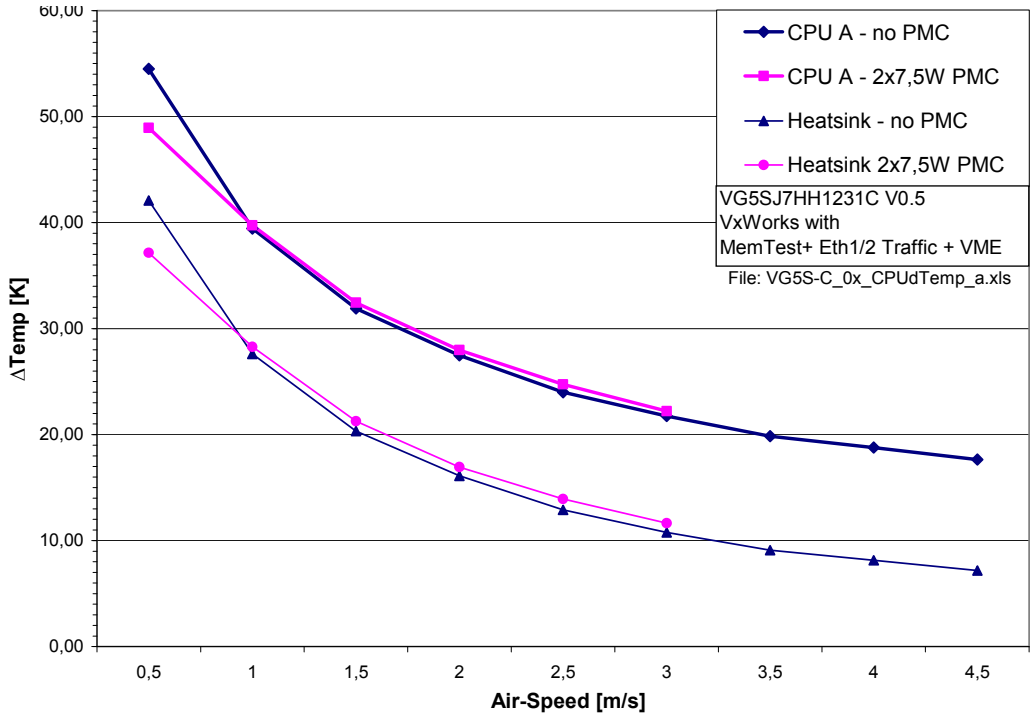


Figure 36: ΔTemperature of VG5 Single Node C-, 1-Style

As can be seen in the above figure the impact of two PMCs (each with 7.5 W) plugged on a VG5S is relatively low at higher airflow speed.

To determine the maximum possible ambient temperature (T_{amax}) the user shall take the maximum heatsink temperature ($T_{heatsinkmax}$) from Figure 36 above and measure the current ambient temperature (T_{ameas}) and the heatsink surface hotspot temperature ($T_{heatsinkmeas}$) under typical applications and actual airflow in the system rack.
The maximum ambient temperature is then calculated with the following formula.

$$T_{amax} > T_{heatsinkmax} - T_{heatsinkmeas} + T_{ameas}$$

☞ Tip: The board has a better MTBF with low heatsink or board temperature, so better cooling gives longer operating life.

Table 85: Operating Temperature Range –7457 Dual Node VG5 V1.x Air Cooled (C-, 1-Style)

Board	Processor	typ. Max temperature at airflow inlet [°C] *CPU-A Temp [°C]*				Remark
		3 m/s	2 m/s	1.5 m/s	1 m/s	
VG5D C-, 1-Style	Dual 7457 @ 800 MHz	**82** *93*	**75** *92*	**69** *91*	**59** *90*	measured V1.4 Board
VG5D C-, 1-Style	Dual 7457 @ 866 MHz	**82**	**75**	**69**	**59**	similarity to 800 MHz
VG5D C-, 1-Style	Dual 7457 @ 1000 MHz	**81**	**75**	**68**	**58**	measured V1.4 Board

According to the formula below Figure 36 the maximum possible ambient temperature at the input is shown in bold (e.g. 82 °C) and the resulting CPU-A temperature (e.g. 93 °C) is shown in italics for a given airflow rate (e.g. 3 m/s).

Table 86: Operating Temperature Range: VG5 V1.x I-, 3-Style at 3 m/s airflow

Product ID	Processor	Typical Operating Temperature Range at 3 m/s airflow	Remark
Dual Node VG5:			
VG5D Ixxx xxxx I	Dual 7455 800 MHz	-40 °C ….81 °C	Estimated
VG5D Jxxx xxxx I	Dual 7455 1000 MHz	-40 °C ….75 °C	Estimated
VG5D _xxx xxxx I	**Dual 7457 800 MHz**	**-40 °C ….82 °C**	**Measured**
VG5D Nxxx xxxx I	Dual 7457 867 MHz	-40 °C ….82 °C	Similarity to Dual 7457 800 MHz
VG5D Kxxx xxxx I	**Dual 7457 1000 MHz**	**-40 °C ….81 °C**	**Measured**
VG5D Lxxx xxxx I	Dual 7457 1266 MHz	-40 °C ….75 °C	Estimated
Single Node VG5:			
VG5S Ixxx xxxx I	Single 7455 800 MHz	-40 °C ….82 °C	Estimated
VG5S Jxxx xxxx I	Single 7455 1000 MHz	-40 °C ….78 °C	Estimated
VG5S _xxx xxxx I	Single 7457 800 MHz	-40 °C ….82 °C	Derived from Dual measurement
VG5S Nxxx xxxx I	Single 7457 867 MHz	-40 °C ….82 °C	similarity to Single 7457 800 MHz
VG5S Kxxx xxxx I	Single 7457 1000 MHz	-40 °C ….82 °C	Derived from Dual measurement
VG5S Lxxx xxxx I	Single 7457 1266 MHz	-40 °C ….77 °C	Derived from Dual measurement

Remark:
VG5 C-, 1-style boards are all 0 °C…70 °C at 3m/s airflow

Table 87: Operating Temperature Range: VG5 V2.x and V3.x C-, 1-Style at 3 m/s airflow

Product ID	Processor	Typical Operating Temperature Range at 3 m/s airflow	Remark
Dual Node VG5:			
VG5D Nxxx xxxx I	Dual 7457 867 MHz	-40 °C ….85 °C	similarity to Single 7457D 1 GHz
VG5D Kxxx xxxx I	**Dual 7457 1000 MHz**	**-40 °C ….85 °C**	**Measured**
VG5D Lxxx xxxx I	Dual 7457 1266 MHz	-40 °C ….75 °C	Estimated (as V1.x)
Single Node VG5:			
VG5S Nxxx xxxx I	Single 7457 867 MHz	-40 °C ….85 °C	similarity to Single 7457D 1 GHz
VG5S Kxxx xxxx I	Single 7457 1000 MHz	-40 °C ….85 °C	similarity to Single 7457D 1 GHz
VG5S Lxxx xxxx I	Single 7457 1266 MHz	-40 °C ….75 °C	Estimated (as V1.x)

Thermal Condition Conduction Cooled Styles (N-, 8-Style)

The thermal condition of the N-, 8-Style VG5 is for use in a conduction cooling environment. This means the base is not related to the ambient temperature but to the maximum card edge temperature.

☞**Note:** Please note that a mounted PMC Module will change the thermal behaviour of the VG5 board	☞**Note:** See photo for definition of CardEdge measurement point.

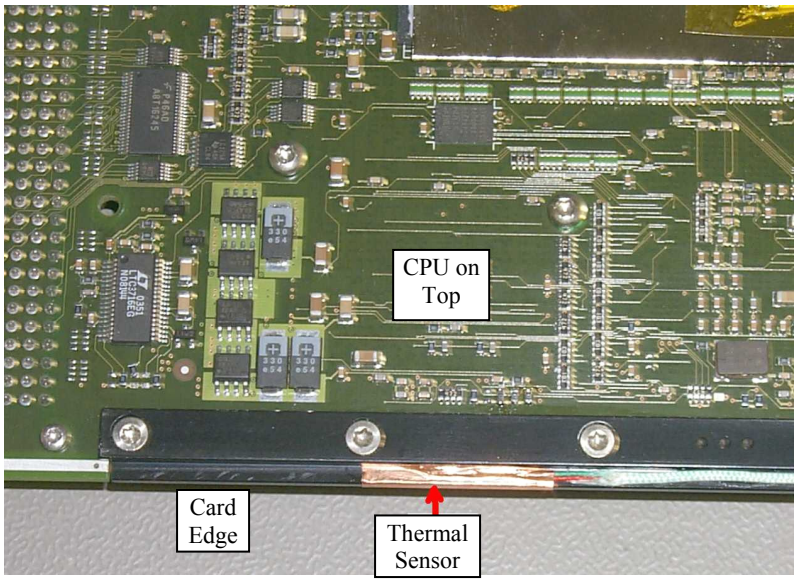


Figure 37: Definition of Card Edge

Table 88: Operating Temperature Range: VG5 V1.x Conduction Cooled Styles (N-/ 8-Style)

valid for VG5D V1.3 and above (no PMCs mounted)

Product ID	Processor	Typical Operating Temperature Range	Remark
Dual Node:			
VG5D Ixxx xxxx N	Dual 7455 800 MHz	-40 °C ….74 °C	Estimated
VG5D Jxxx xxxx N	**Dual 7455 1000 MHz**	**-40 °C …. 74 °C**	**Measured**
VG5D _xxx xxxx N	**Dual 7457 800 MHz**	**-40 °C ….75 °C**	**Measured**
VG5D Nxxx xxxx N	Dual 7457 867 MHz	-40 °C ….75 °C	Similarity to Dual 7457 800 MHz
VG5D Kxxx xxxx N	**Dual 7457 1000 MHz**	**-40 °C ….74 °C**	**Measured**
VG5D Lxxx xxxx N	**Dual 7457 1266 MHz**	**-40 °C ….70 °C**	**Measured**
Single Node:			
VG5S Ixxx xxxx N	Single 7455 800 MHz	-40 °C ….82 °C	Estimated
VG5S Jxxx xxxx N	Single 7455 1000 MHz	-40 °C ….80 °C	Derived from Node A of Dual Board
VG5S _xxx xxxx N	Single 7457 800 MHz	-40 °C ….82 °C	Derived from Node A of Dual Board
VG5S Nxxx xxxx N	Single 7457 867 MHz	-40 °C ….82 °C	Similarity to Single 7457 800 MHz
VG5S Kxxx xxxx N	Single 7457 1000 MHz	-40 °C ….82 °C	Derived from Node A of Dual Board
VG5S Lxxx xxxx N	Single 7457 1266 MHz	-40 °C ….78 °C	Derived from Node A of Dual Board

The limiting factors for the Dual Node VG5 V1.x are some devices on the bottom side, due to the fact that they are not directly bound to the cooling stiffener:

1. Node B: DDR-SDRAM Bank U145x:
   It is heated by the 1.8 V Linear Regulator and so seeing higher temperatures as Node A DDR-SDRAM Bank.
2. Node B DDR-Termination Regulator U1650
   It is also heated by the 1.8 V Voltage Regulator on the top side – if very many memory read/write transfers have zero as data, the highest temperature will be reached – it is very unlikely to happen in applications – but up to 39 K were measured with special test software.

The limiting factors for the Single Node VG5 are some devices on the bottom side, due to the fact that they are not directly bound to the cooling stiffener:

1. DDR-SDRAM Bank U140x: Bottom side
2. DDR-Termination Regulator U1600
   If very many memory read/write transfers (10secs) have zero as data, the highest temperature will be reached – it is very unlikely to happen in applications, we achieved these high temperatures only with specially designed test software.
3. For the 1266 MHz speed grade the CPU is also a limiting factor

Table 89: Operating Temperature Range: VG5 V2.x and V3.x Conduction Cooled Styles (N/ 8-Style)

(no PMCs mounted)

Product ID	Processor	Typical Operating Temperature Range	Remark
Dual Node:			
VG5D _xxx xxxx N	Dual 7457 800 MHz	-40 °C ….85 °C	Similarity to Dual 7457 1000 MHz
VG5D Nxxx xxxx N	Dual 7457 867 MHz	-40 °C ….85 °C	Similarity to Dual 7457 1000 MHz
VG5D Kxxx xxxx N	**Dual 7457 1000 MHz**	**-40 °C ….85 °C**	**Measured**
VG5D Lxxx xxxx N	**Dual 7457 1267 MHz**	**-40 °C ….76 °C**	**Measured**
Single Node:			
VG5S _xxx xxxx N	Single 7457 800 MHz	-40 °C ….85 °C	Derived from Dual measurement
VG5S Nxxx xxxx N	Single 7457 867 MHz	-40 °C ….85 °C	Derived from Dual measurement
VG5S Kxxx xxxx N	Single 7457 1000 MHz	-40 °C ….85 °C	Derived from Dual measurement
VG5S Lxxx xxxx N	Single 7457 1267 MHz	-40 °C ….78 °C	Estimated

Remarks:
A VG5D consumes about 12% more power when the card edge is at 85 °C in comparison to 40 °C

CHAPTER 8 Glossary

TBD	to be defined
TBC	to be confirmed
SBC	Single Board Computer
Node A	Unit on VG5 made of Chipset A, CPU A, L3 Cache A, DDR RAM A, FLASH A.
Node B	Unit on VG5 made of Chipset B, CPU B, L3 Cache B, DDR RAM B, FLASH B.
Devicebus	A 32-bit bus from the Chipset (MV64360) used for connecting Flash Memory, UART, RTC and FPGA. Each node has an independent Devicebus.
FPGA	Field Programmable Gate Array
MPSC	Multi Protocol Serial Controller (Unit of MV64360)
MPP	Multi Purpose Port (Unit of MV64360)
MTBF	Mean Time Between Failures
NDA	Non Disclosure Agreement
SPD	Serial Presence Detect

CHAPTER 9 Support, Service and Warranty

Chapter Scope

The following section describes GE Intelligent Platforms' product support program. There are two regional support headquarters and regional customer centers. In this chapter you will find information about our product warranty terms and details about what action to take if you experience a problem with the product.

Geographical Regions

World-wide headquarter of GE Intelligent Platforms, Inc. is at

GE Intelligent Platforms, Inc.
2500 Austin Drive
Charlottesville, VA 22911
U.S.A.

Web: http://www.ge-ip.com

GE Intelligent Platforms, Inc. uses two regional headquarters for the purpose of support, service, RMA returns and other functions.

Regional areas:

WW	world-wide
EU	Germany: Augsburg UK: Towcester
US	Americas & Pacific Rim (Japan, Korea, China, Philippines, AUS, NZ)

Technical Support

If you should have a problem with an GE Intelligent Platforms product: Free technical support is available by phone, fax or email. Telephone support is available at main locations or at the regional center where the product was bought.

Germany	US
Monday through Thursday 8:00 – 17:00 (CET) Friday 8:00 – 16:00 (CET)	Monday through Friday 8:30 AM – 5:30 PM (Eastern Time)
Phone +49-821-5034-170	Phone +1-800-322-3616
Fax +49-821-5034-119	Fax +1-
E-Mail: support.augsburg.ip@ge.com	E-Mail: support.huntsville.ip@ge.com

Support on the Web

For support and information, visit our website at
www.ge.com

Information for components, corresponding driver software, etc. can also be found at the following locations:

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Warranty

For detailed warranty information, visit our website at
http://www.ge-ip.com

Error Report

For error reports and RMA (Return Material Authorization) forms contact these email addresses:
repairs.augsburg.ip@ge.com
repairs.huntsville.ip@ge.com

In case of difficulties provide at least the information listed below to an appropriate support center or on their web site as listed above:

- RMA Number, if applicable
- Product & Serial Number
- Part Number
- Version
- Contact: Name & Phone Number
- Detailed Description of the Problem/Defect

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