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VMIPCI-5579
13.4 Mbyte/s Fiber-Optic Reflective Memory with Interrupts

Product Manual

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Huntsville, Alabama 35803-3308, USA
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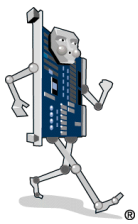
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Overview

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Introduction

The VMIPCI-5579 is a member of VMIC's high-performance, daisy-chained fiber-optic network family of Reflective Memory. Data is transferred around the network by writing to on-board global RAM. The data is automatically sent to the corresponding location in memory on all Reflective Memory boards on the network. The Reflective Memory network may consist of any of VMIC's family of VMIxxx-5579 boards.

The VMIPCI-5579 Reflective Memory board has several useful and unique features:

- High-speed, easy-to-use fiber-optic network (270 Mbaud serially)
- Data written to memory in one node is also written to memory in all nodes on the network
- Up to 1,000 meters between nodes
- Up to 256 nodes per network
- Network data transferred at 13.4 Mbyte/s (without redundant transfer)
- Network data transfer rate of 6.7 Mbyte/s (with redundant transfer)
- Redundant transmission mode for suppressing errors
- Any node on the network can generate an interrupt in any other node on the network or in all network nodes with a single command
- Error detection
- No software overhead for basic operation
- No processor involvement in the operation of the network
- Up to 64 Mbyte of Reflective Memory
- D32, D16, and D8 memory access
- Configurable endian conversions, to support multiple CPU architectures on the same network

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Functional Description

Figure 1 on page 15 shows the block diagram of the Reflective Memory board. Note that the FIFO memory is on the same bus as the RAM memory. The user sees only the memory and is not aware of the FIFO memory, which does the actual bus transfer to the other boards. The Reflective Memory board appears to the user as standard RAM memory and can be used as such. Due to the presence of the communications bus, the only effect noticeable to the user is that the RAM takes slightly longer to acknowledge when the receive FIFO is also writing to RAM.

Software Requirements

Upon power up, the Reflective Memory board is able to establish the board-to-board link without any software intervention. Furthermore, the basic operation of the board requires no software interaction. However, if an alternate mode of endian byte swapping, address offsetting, or memory block protection is desired, a software initialization routine will be required.

If network and / or status interrupts are desired, a software routine must be resident which can initialize and service these interrupts through a group of Control and Status Registers. Several on-board sources may be enabled to generate a single PCI interrupt to the host system. Upon power up, all sources of the PCI interrupt are disabled with the exception of a manual interrupt.

The VMIPCI-5579 does not contain an imbedded self-diagnostic mechanism. However, it does contain several Control and Status registers, which support both board and system level diagnostics. If desired, the host system will require software routines to activate and use the diagnostic features.

Hardware Requirements

The VMIPCI-5579 contains user configurable jumpers, which should be configured prior to installation of the board. One bank of eight jumpers are used to define the Network Node ID. Each board within the network must have its own unique Node ID ranging from 0 through 255. The nodes can be physically located in any order.

Besides the Node ID jumpers, the board also contains a jumper which selects either single or redundant mode. A set of three rogue packet control jumpers also exist. The descriptions of these jumpered features are discussed in later sections of this document.

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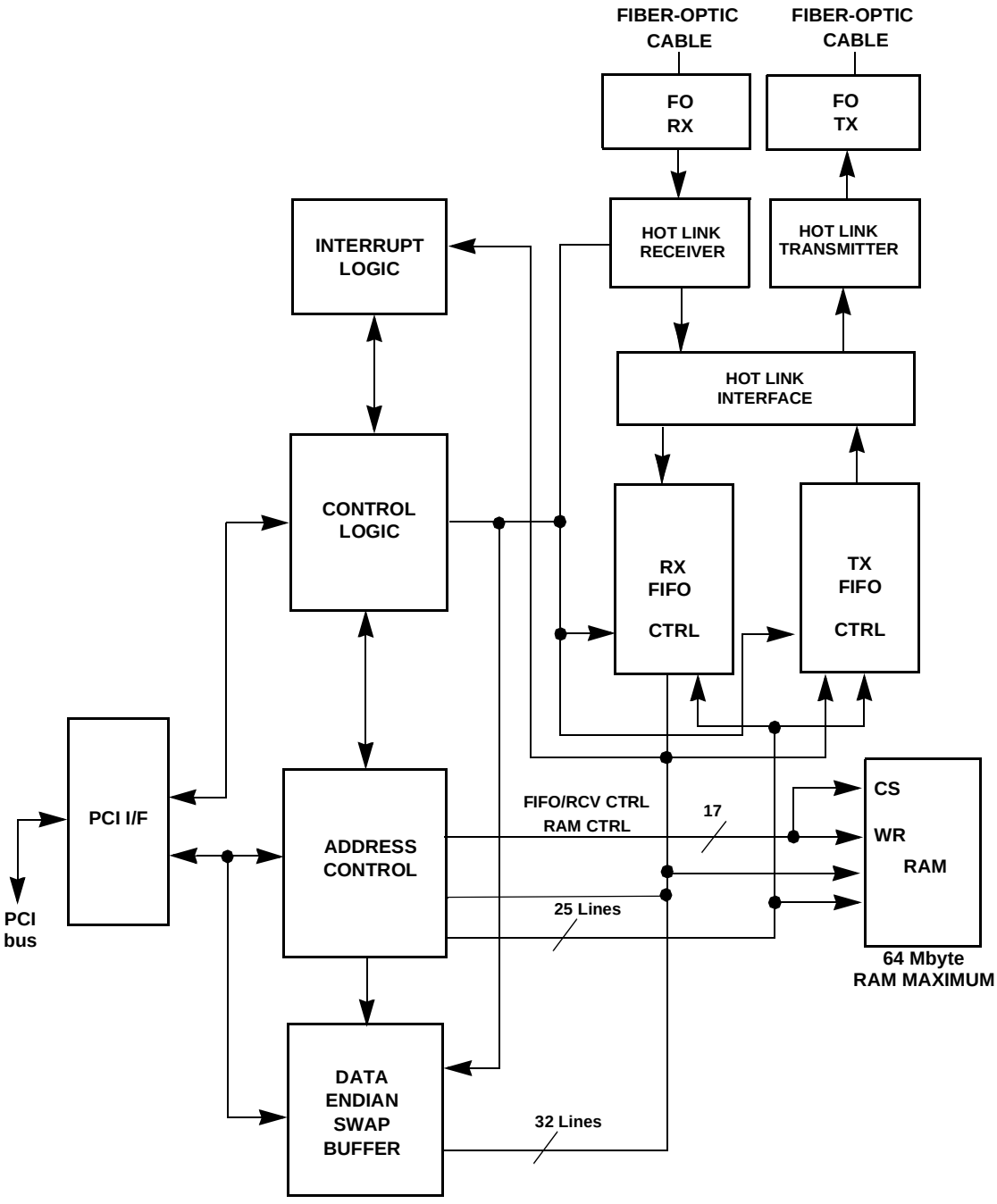


Figure 1 VMIPCI-5579 Functional Block Diagram

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Reference Material List

Refer to *PCI Local Bus Specification* for a detailed explanation of the PCI Local bus. The PCI Local bus Specification is available from the following source:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
U.S.: (800) 433-5177
International: (503) 797-4207
FAX: (503) 234-6762

Physical Description and Specifications

Refer to Product Specification, 800-855579-000 available from:

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.



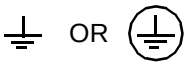
Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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Safety Symbols Used in This Manual



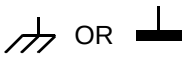
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).



The STOP symbol informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.



The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.



The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.



The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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CHAPTER 1

Theory of Operation

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Introduction

The VMIPCI-5579 is a single slot PCI board that implements a high-performance, daisy-chained PCI-to-Reflective Memory network. Data is transferred to each node on the network by writing to on-board global RAM. Data written to any node appears in all other nodes without programming or other intervention by the user. The link between the nodes is two fiber-optic cables which pass Node ID, data, and if enabled, interrupt information between adjacent boards on the link.

The VMIPCI-5579 allows a user to read or write the RAM address space at will. All memory writes are stored in RAM on the board and also put in a FIFO to be broadcast to all other nodes. An interrupt command may also be written to any or all nodes by writing a data word into a specific location. The data value written dictates which node(s) will receive the interrupt. The interrupt is sent out in the order the data was received from the PCI bus. If a block of data was written to the board before the interrupt command is sent, then the data is broadcast to all boards before the interrupt command is broadcast.

A data packet received by a local node is decoded and checked for validity. Then, if the packet data is valid and did not originate at this local node, it is written into a receive FIFO. If invalid data is received, it is discarded and a status register fault flag is set. From the receive FIFO, the data packet is written to the local RAM at the earliest convenience and also transferred into the transmit FIFO to be sent to the next node on the link.

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Memory Configuration

The VMIPCI-5579 provides memory size options of 32, and 64 Mbytes. As with any PCI bus product, the host's Basic Input Output System (BIOS) automatically allocates memory space on the PCI bus, which is equal to the board memory option. Likewise, the host's BIOS sets the Base Address from which this memory space starts. All the on-board memory contained on the VMIPCI-5579 is fully read / write accessible by the host system, with the exception of the first 40 (HEX) bytes. The first $40 memory bytes have been replaced with Control and Status Registers. Several bits within the Control and Status Registers are either read-only or write-only.

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Network Configuration

The VMIPCI-5579 system is a fiber-optic daisy-chained ring as shown in Figure 1-1 on page 22. Each transfer is passed from node-to-node, until it has gone all the way around the ring and reaches the originating node. Each node retransmits all transfers that it receives, except those that it originated. Nodes are allowed to insert transfers between transfers passing through.

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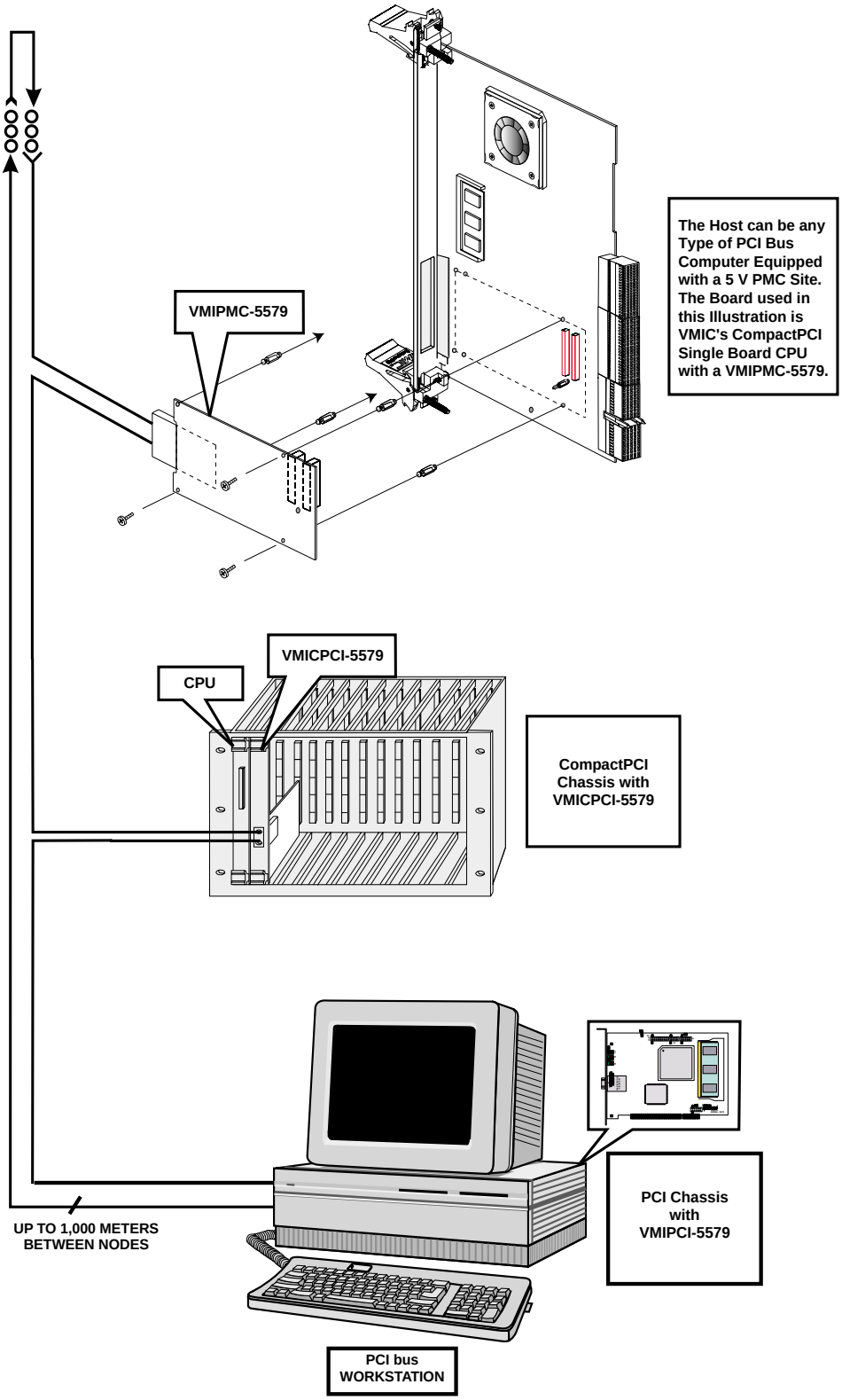


Figure 1-1 Network Example Using Reflective Memory System

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Interrupt Transfers

In addition to transferring data between nodes, the VMIPCI-5579 will allow any host processor in any node to generate an interrupt on any other node. These interrupts would generally be used to indicate to the receiving node that new data has been sent and is ready for processing. These interrupts are also used to indicate that processing of old data is completed and the receiving node is ready for new data.

Three interrupts are available. The user can define the function for each interrupt. In addition, any processor on the network can generate an interrupt on all nodes on the network. Interrupts are generated by simply writing to a single VMIPCI-5579 register. All data and interrupt command transfers contain the node ID of the node that originated the transfer. This information is used primarily so the originating node can remove the transfer from the network after the transfer has traversed the ring. The node identification is also used by nodes receiving interrupt commands. When a node receives an interrupt command, it places the identification number (node ID) of the originating node in a FIFO. Each of the three interrupts has a separate associated FIFO. Up to 63 interrupts can be stacked in each of the three FIFOs. During the interrupt service routine, the sender node ID of the interrupting node can be read from the FIFO.

In addition to storing the sender node ID in the three interrupt FIFOs, the VMIPCI-5579 also stores flags bits, and stores up to 21 bits of data. The three flag bits indicate if the interrupt was global, and verify its type (1, 2, or 3). The 21 interrupt data bits are user defined.

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Addressing Features

The VMIPCI-5579 is offered with two memory options: 32 and 64 Mbyte(s). Upon power up, the host PCI system BIOS automatically allocates a memory space equal to the physical memory available on the board. Not all nodes on a network have to be configured with the same memory size.

Standard and Extended Addressing Modes

Currently the maximum amount of on-board memory that can be located on a single VMIPCI-5579 is 64 Mbyte. However, the relative address passed by the VMIPCI-5579 on the network is 128 Mbyte wide to provide network compatibility with future expanded products.

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Node Latency

If the fiber-optic data bandwidth has not been exceeded, data latency is typically 1.5 µs to 1.8 µs per node in single transfer mode. Longer latencies result if data input rates exceed 13.4 Mbyte/s sustained. The PCI bus can burst data into the transmit FIFO and RAM at up to 33 Mbyte/s until the TX FIFO becomes full at which time the PCI bus interface would generate a STOP so that data is not lost in the TX FIFO.



The actual burst rate depends on the PCI bus speed of the host system. The 33 Mbyte/s assumes the maximum PCI bus clock rate of 33 MHz.

DMA Capabilities

The VMIPCI-5579 supports DMA read and write operations. The DMA sequence is initialized by control register writes to the VMIPCI-5579 issued by the host. Immediately following this, the VMIPCI-5579 becomes a PCI initiator, and moves the specified block of data without further host intervention. The PCI architecture ensures that the VMIPCI-5579 does not monopolize the PCI bus. The DMA engine of the VMIPCI-5579 automatically breaks large blocks into small bursts. The VMIPCI-5579 can be programmed to issue a PCI interrupt upon completion of the DMA process. Although the DMA engine can do both DMA reads and DMA writes, it cannot perform both simultaneously. In the DMA mode, the VMIPCI-5579 can burst data on the PCI bus at a maximum rate of 132 Mbyte/s and 22 Mbyte/s sustained with a 33 MHz clock frequency.

Error Management

Errors are detected by the VMIPCI-5579 using the error detection facilities of the Hot Link encoder/decoder, and with additional interlaced parity encoding and checking. The error rate of the VMIPCI-5579 is a function of the rate of errors produced in the optical portion of the system. This optical error rate depends on the length and type of fiber-optic cable. Assuming the typical optical error rate is 10^{-12}, the error rate of the VMIPCI-5579 is 1.6×10^{-10} erroneous transfers. However, the rate of undetectable errors is less than 2.56×10^{-20} erroneous transfers. When a node detects an error, the erroneous transfer is not written into memory but removed from the network and a PCI interrupt is generated if enabled.

The VMIPCI-5579 can be operated in a redundant transfer mode in which each data packet is transmitted twice. In this mode, the first of two transfers is used unless an error is detected, in which case the second transfer is evaluated and used if valid. In the event that an error is detected in both transfers, the board removes the packet from the network. The probability of both transfers containing an error is 2.56×10^{-20}, or about an error every 1,470,000 years at the maximum data rate.

$$Bit_ERR := 10^{-12} \qquad Bit := 128 \cdot \frac{5}{4}$$

$$Op_ERR := \frac{1}{(Bit_ERR \cdot Bits)^2} \qquad Op_ERR = 3.906 \cdot 10^{19}$$

$$Bit_ERR \cdot Bits = 1.6 \cdot 10^{-10}$$

$$Data_Rate := \frac{270 \cdot 10^6}{2 \cdot Bits} \qquad \text{(Dual Packet Time/Transfer)}$$

$$Time := \left(\frac{1}{Data_Rate}\right) \cdot \frac{Op_ERR}{(60 \cdot 60 \cdot 24 \cdot 365)}$$

$$Time = 1.468 \cdot 10^6 \qquad \text{(Years/Dual Packet Error)}$$

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Data Endian Conversion

Data lane steering can be configured through a control register to allow the host processors of different architectures, and endian convention to transfer data transparently. The available endian conventions include byte swap, word swap, byte and word swap and swap-on-size. Endian conversion is transparent to received or transmitted data.

Diagnostic Features

The VMIPCI-5579 contains several Control and Status Registers, which can serve to indicate the configuration and status of various circuits on the board. One such Status Register contains an “OWN DATA” flag which is asserted high when a node detects its own data returning on its receiver. The “OWN DATA” flag can be used to verify that data is traversing the ring (that is the daisy-chained network ring is not broken) and can be used to measure network latency. The VMIPCI-5579 contains several diagnostic features which are not present in prior VMIC products such as the VMIxxx-5588 series. They are intended to aid in both local and network-level diagnostics. These features are described in the following paragraphs:

***Monitor Mode*:** Once the Monitor Mode is activated by a control register write, the host will be prohibited from writing to on-board memory and from initiating data packet writes to other nodes. Access of the on-board memory by the other nodes is unaffected and data pass through to the other nodes is not effected. The host will only be able to monitor network activity by reading the on-board memory.

***Disconnect Mode*:** The Disconnect Mode is activated through a control register write, the on-board memory will be disconnected from the network. In this mode, the host can perform on-board memory tests without affecting other nodes on the network. At the same time, the other nodes can pass data through the board without affecting the local memory.



The VMIPCI-5579 contains registers that are similar to those found on the VMIPCI-5588 Reflective Memory boards.

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Configuration Space

This portion of the theory of operation defines the programming model, and usage rules for the configuration register space in PCI-compliant devices. The intent of the PCI configuration space definition is to provide an appropriate set of configuration *hooks* which satisfies the needs of current and anticipated system configuration mechanisms. As a general rule, accesses to this information is required only to find where the VMIPCI-5579 is located in I/O space, memory space, and the interrupt table. Figure 1-2 below is the organization of the PCI Configuration Space Header.

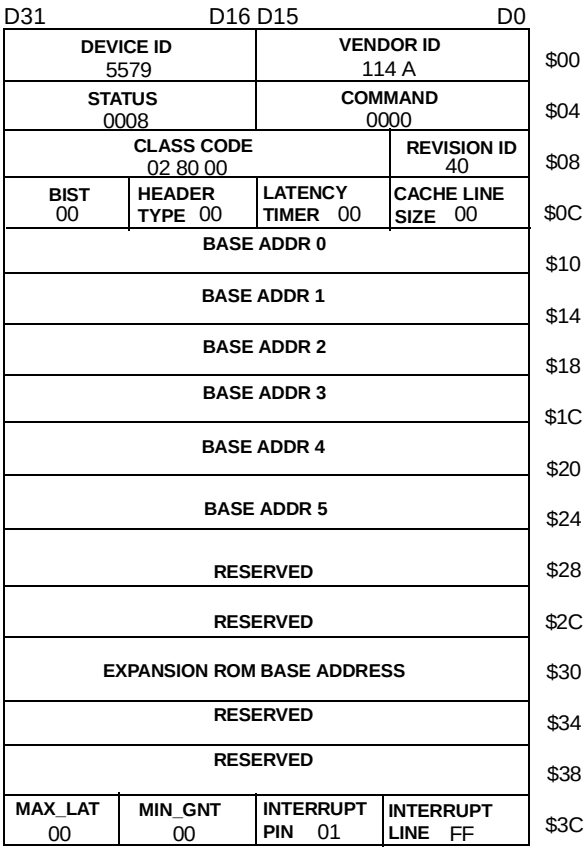


Figure 1-2 Configuration Space Header

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CHAPTER 2

Configuration and Installation

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Fiber-Optic Link Configuration 34

Introduction

This chapter describes the setup and configuration of the board, depending on your particular need. Jumper configuration, fiber-optic link configuration, and board layout are also addressed in this chapter.

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Unpacking Procedures



Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation



Do not install or remove the board while power is applied.

Host systems containing PCI card sites vary widely in appearance and board installation procedures. VMIC recommends examining the host system installation guides prior to installing this board. Also prior to installing this board, set the user configurable jumpers described on pages 31 and 32.

1. Remove the host system’s cover or access panels according to the unit’s hardware guide.
2. Remove the blank PCI cover bracket corresponding to the slot into which this board is to be installed.
3. Insert this board firmly into the desired PCI motherboard slot.
4. Install the screw that fastens the board’s PCI bracket to host’s support panel.

The VMIPCI-5579 installation is complete.

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Jumper Installation

Figure 2-1 shows the layout of user-configurable jumpers on the Reflective Memory board. Jumpers E1 and E4 are for factory use only

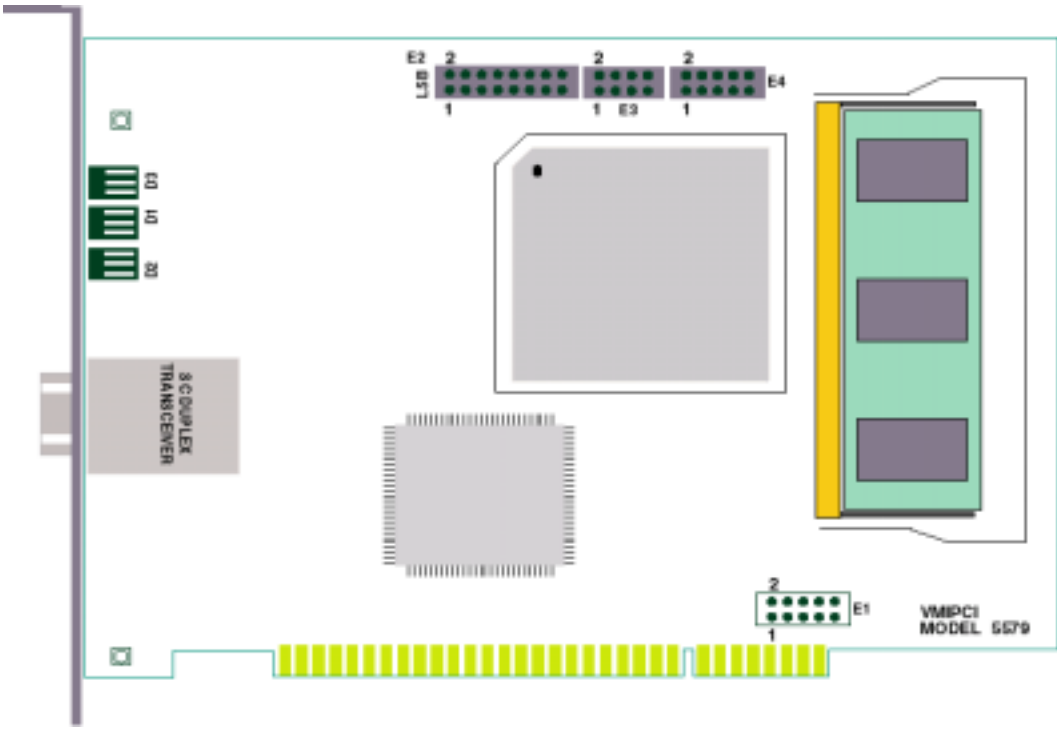


Figure 2-1 VMIPCI-5579 Jumper Locations

Board Node ID Field (E2)

The Board Node ID Field identifies each board on the memory link. No ID may be used more than once on the link. Jumper field E2 provides 8 bits to define the board node ID. An installed jumper sets the corresponding bit to zero. There is no relation between the node number and the physical position on the link. Nodes may be physically located in any order.

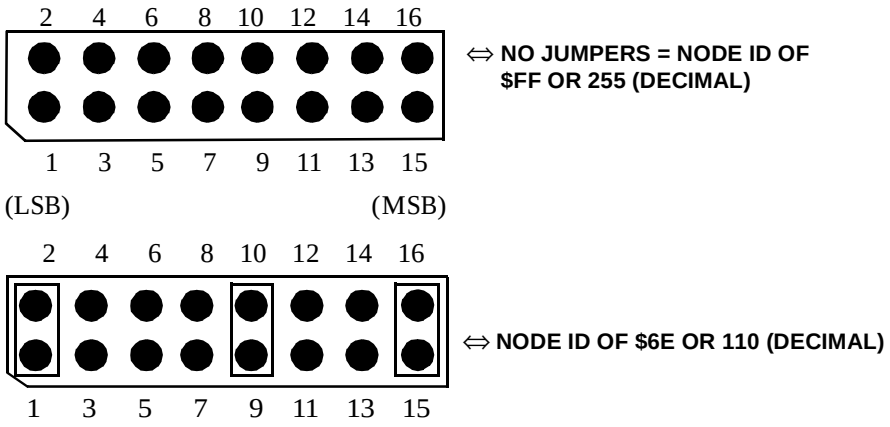


Figure 2-2 Example of Node ID Field Jumper E2

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Fast/Rogue Packet Jumper Field (E3)

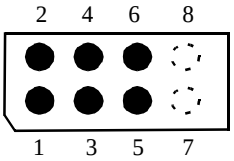
A Rogue Packet is a packet that has become corrupted in such a manner that it passes all the data integrity checks including parity. Rogue Packets are packets that do not contain the ID of an active node. Without a node to eliminate it from the ring, the Rogue Packet will continue to circulate. The odds of this happening are extremely small as shown in the calculation of undetectable errors (see page 25). There are situations where broken hardware can generate a Rogue Packet. The VMIPCI-5579 incorporates a scheme where a Rogue Packet Master (RPx) tags all micropackets passed on the fiber-optic network. If the Rogue Packet Master sees a packet that was previously tagged, the Rogue Packet Master will remove that packet from the ring.

The Rogue Packet Master is jumper selectable using jumper header E3. There can be up to three Rogue Packet Master (RP0, RP1, and RP2) on the ring. It is not necessary to use this feature when running the board. Running this feature does not hamper the performance of the network. Each Rogue Packet Master must be unique, since it tags a specific bit in the micropacket, and no other Rogue Packet Master can use this bit. See figure below for configuring the Rogue Packet Master feature.

Note

When configuring the VMIPCI-5579 Rogue Packet feature, care must be taken to ensure that each Rogue Packet Master is unique, that is no two Rogue Packet Masters can have the same jumper removed (active).

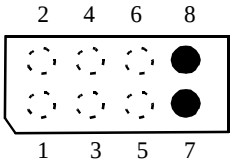
Jumper E3 (Rogue Packet Master Field - Pins 1 through 6)



Pins 1 and 2 = RP0 - REMOVED IS ACTIVE STATE
Pins 3 and 4 = RP1 - REMOVED IS ACTIVE STATE
Pins 5 and 6 = RP2 - REMOVED IS ACTIVE STATE

Rogue Packet Masters tag all traffic that passes around the ring, and removes the traffic that has passed through more than once. There can only be three RP masters in a ring (RP0, RP1, and RP2). Each with a unique RP jumper, this jumper must be removed to enable that particular RP master.

Jumper E3 (Fast Jumper Field - Pins 7 and 8)



Pins 7 and 8, INSTALLED = REDUNDANT MODE
Pins 7 and 8, OMITTED = FAST MODE

Note

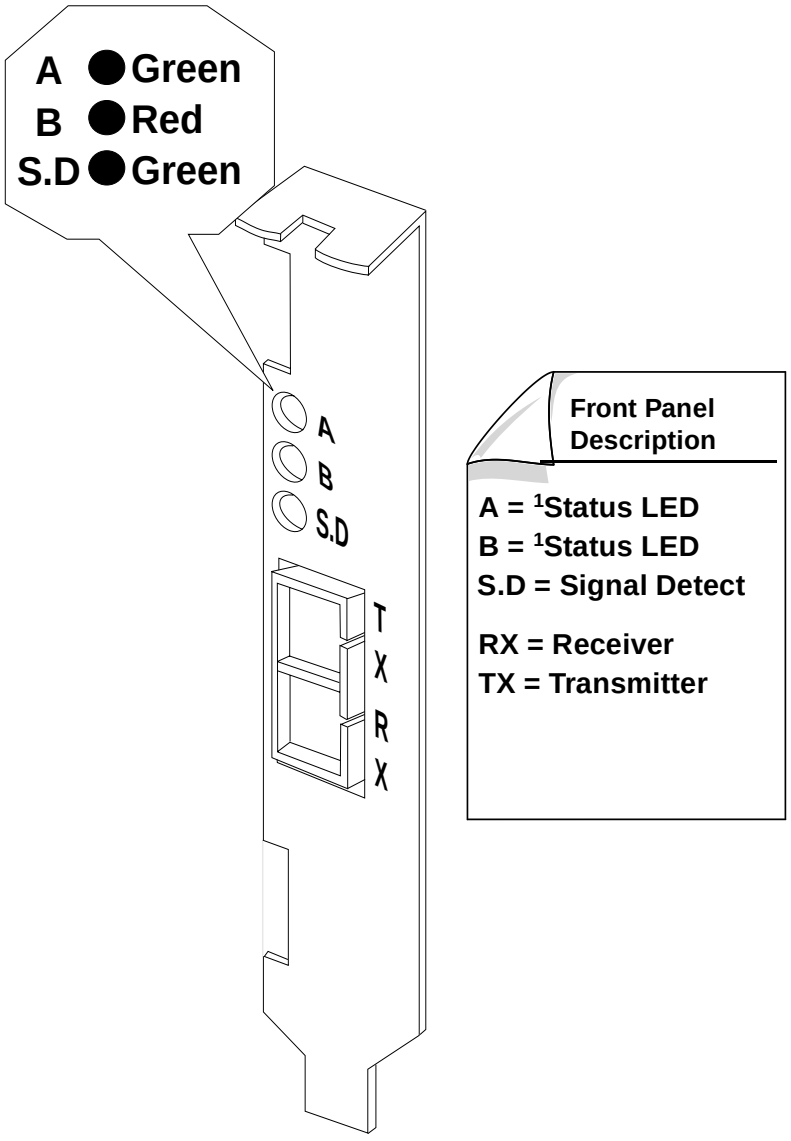
When the jumper is installed, all transmissions are redundant. All nodes in a system must be setup the same (either redundant or fast mode).

Figure 2-3 Configuring Fast/Rouge Packet Jumper E3

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Status LEDs

The VMIPCI-5579 has three status LEDs located on the front panel above the fiber-optic transceiver. The LEDs are labelled ‘A, B, and S.D. A and B are green and red respectively, and are status LED’s, that are controlled by the user. S.D, is the Signal Detect LED that indicates light is present at the fiber-optic receiver.



Note

[1]The A and B LEDs are user defined status LEDs.

Figure 2-4 VMIPCI-5579 Front Panel View, and Description of LEDs

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Fiber-Optic Link Configuration

A VMIPCI-5579 ring is formed by connecting the transmitter of board A into the receiver of board B. Board B's transmitter is then connected to the receiver of board C, and so on. The last board in the ring has its transmitter connected back to board A's receiver to close the ring. The VMIPCI-5579 uses 'SC' type multi-mode fiber-optic cables as shown in Figure 2-5. See Product Specification for ordering information. Cable Specifications:

- Simplex, multi-mode, graded index glass fiber
- Core diameter = 62.5 ±3 µM
- Cladding diameter = 125 ±2 µM
- Jacket outer diameter = 3.0 mm ±.1mm
- Attenuation: 4.0 dB/Km (max) at 850nm, 1.75dB/Km (max) at 1300nm
- Bandwidth: 160 to 300 MHz-Km (min) at 850nm, 300 to 700 MHz-Km (min)at 1300 nm
- UL type OFNR, CSA type OFN FT4

Connector Specification:

- Compatible with NTT SC standard and JIS C 5973 complaint
- Ceramic ferrule
- Insertion loss: 0.35 dB (max) multi-mode
- Fiber clad diameter: 125 µM
- Jacket diameter: 3.0 mm
- Temperature range: -20 °C to +85 °C



Figure 2-5 'SC' Type Fiber-Optic Cable

When data has been sent around the ring, and has returned to the originating node, two things happen. First, the data is removed from the ring by comparing the data packet's ID to the local node's ID. If they match, the data packet is removed from the ring. Second, the OWN DATA bit is set in the CSR1. Loop data latency can be measured by writing a zero (0) to the OWN DATA bit in the CSR1, and polling until it returns to a one (1) state. This test assumes there is no other data originated by the local node on the ring before the latency test is initiated. The data written to the Control and Status Registers, located in the first $40 memory-mapped locations, is passed around the ring as regular traffic but does not affect the status of any other node's CSRs.

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CHAPTER 3

Programming

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Following established conventions, a group of data bits 16 bits wide is simply called a **Word**, while 32-bit wide data is called a **Longword** or **Lword**. In other sections of this manual and / or other VMIC manuals, 32-bit wide data may be called **Double Word** or **Dword**.

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Programming

The VMIPCI-5579 Reflective Memory board has three sets of registers associated with it. The first is the PCI Configuration registers, these registers can only be accessed with configuration cycles over the PCI bus. The PCI Configuration registers are automatically configured by the PC BIOS on power up. The registers are defined by the PCI specification, and will be initialized automatically (by an on-board state machine, no software is required) during the powerup sequence, from an on-board EPROM. The address map of the PCI Configuration Space Header is shown below. Detailed bit information is in the section title Configuration Space Organization on page 37.

D31		D16 D15	D0	
DEVICE ID 5579		**VENDOR ID** 114 A		$00
STATUS 00 08		**COMMAND** 0000		$04
CLASS CODE 02 80 00		**REVISION ID** 40		$08
BIST 00	**HEADER TYPE** 00	**LATENCY TIMER** 00	**CACHE LINE SIZE** 00	$0C
BASE ADDR #0 (I/O - PCI I/F IC) 64 byte Requested				$10
BASE ADDR #1 (Memory and Board Control) 32 or 64 Mbyte Requested				$14
BASE ADDR #2 (Not Used)				$18
BASE ADDR #3 (Not Used)				$1C
BASE ADDR #4 (Not Used				$20
BASE ADDR #5 (Not Used)				$24
RESERVED = 0				$28
RESERVED = 0				$2C
EXPANSION ROM BASE ADDRESS				$30
RESERVED = 0				$34
RESERVED = 0				$38
MAX_LAT 00	**MIN_GNT** 00	**INTERRUPT PIN** 01	**INTERRUPT LINE** FF	$3C

Figure 3-1 PCI Configuration Space Header

The second set of registers is the Control Registers which are associated with the PCI Interface Chip used on the board. This set of registers is used to enable and configure the PCI interrupts and to Control DMA functions. This address area is mapped as 16 consecutive Dword registers located at the address space (I/O) specified by the Base Address register 0 (as shown in Figure 3-1.) The register map for this address space is shown in Table 3-4, “PCI bus Operation Register Map,” on page 47. These registers are accessed with PCI I/O cycles.

The third set of registers are those associated with the internal board operations and are located in the lower $00 bytes of memory. These registers must be accessed with PCI memory cycles.

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Configuration Space Organization

This section defines the organization of configuration space registers and imposes a specific record structure, or template of the 256-byte space. This space is divided into a predefined header region, and a device dependent region. Devices implement only the necessary and relevant registers in each region. A device's configuration space must be accessible at all times, not just during system boot. The predefined header region has a size of 64 bytes and every device must support the register layout of this region. This region consists of fields that uniquely identify the device and allow the device to be generically controlled. See Figure 3-1 on page 36.

All compliant devices must support the Vendor ID, Device ID, Command and Status fields in the header. Implementation of other registers is optional (i.e., they can be treated as reserved registers) depending on the device functionality. If a device supports the function that the register is concerned with, the device must implement it in the defined location and with the defined functionality.

Configuration Space Functions

PCI has the potential for greatly increasing the ease in which systems may be configured. To realize this potential, all PCI devices must provide certain functions that system configuration software can utilize. This section also lists the functions that need to be supported by PCI devices by way of registers defined in the predefined header portion of the configuration space. The exact format of these registers (i.e., number of bits implemented) is device-specific. However, some general rules must be followed. All registers must be capable of being read back and the data returned must indicate the value that the device is actually using.

Configuration space is intended for configuration, initialization, and catastrophic error handling functions; its usage should be initialization software and error handling software. All operational software must continue to use I/O and/or memory space accesses to manipulate device registers.

Device Identification

Five fields in the predefined header deal with device identification. All PCI devices are required to implement these fields. Generic configuration software will be able to easily determine what devices are available on the system's PCI bus(es). All of these registers are read-only.

Vendor ID This field identifies the manufacturer of the device. Valid vendor identifiers are allocated by the PCI SIG to ensure uniqueness. $114A is VMIC's vendor ID.

Device ID This field identifies the particular device. This identifier is allocated by the vendor. The Device ID for the VMIPCI-5579 is 5579.

Revision ID This register specifies a device-specific revision identifier. The value is chosen by the vendor. This field should be viewed as a vendor-defined extension to the Device ID. For VMIPCI-5579, the revision code shall be $40 and up.

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Header Type This byte identifies the layout of bytes $10 through $3F in configuration space and also whether or not the device contains multiple functions. Bit 7 in this register is used to identify a multifunction device. If the bit is 0, then the device has multiple functions. Bits 6 through 0 specify the layout of bytes $10 through $3F. One encoding, $00, is defined and specifies the layout shown in Figure 3-1 on page 36.

Class Code The Class Code register is read-only and is used to identify the generic function of the device. The register is broken into three byte-size fields. The upper byte (at offset $0B) is a base class code which broadly classifies the type of function the device performs. The middle byte (at offset $0A) is a subclass code which identifies more specifically the function of the device. The lower byte (at offset $09) identifies a specific register-level programming interface (if any) so that device independent software can interact with the device. The VMIPCI-5579 class code is $28000.

Device Control

The Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero (0) is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command register may or may not be implemented depending on a device's functionality. For instance, devices that do not implement an I/O space probably will not implement a writable element at bit location zero (0) of the Command register. Devices typically come up with all zeros in this register. Figure 3-2 shows the layout of the register and Table 3-1 on page 39 explains the definitions of the different bits in the Command register.

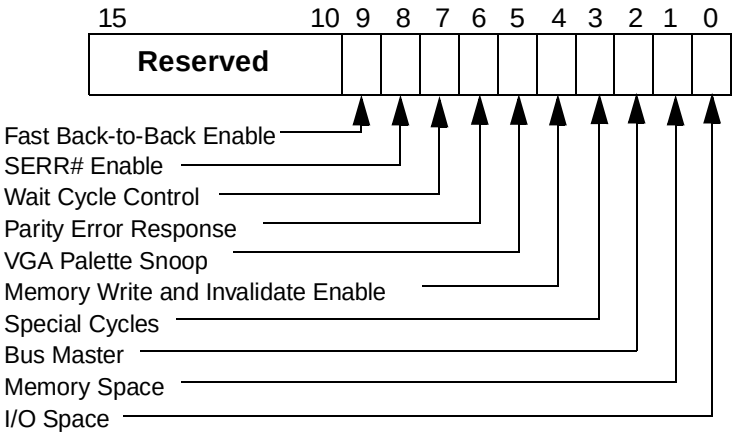


Figure 3-2 Command Register Layout

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Table 3-1 Command Register Bits

Bit Name	Bit Location	Bit Definitions
I/O Space	0	Controls a device's response to I/O space accesses. A value of zero disables the device response. A value of one allows the device to respond to I/O space accesses.
Memory Space	1	Controls a device's response to memory space accesses. A value of zero disables the device response. A value of one allows the device to respond to memory space accesses.
Bus Master	2	Controls a device's ability to act as a master on the PCI bus. A value of zero disables the device from generating PCI accesses. A value of one allows the device to behave as a bus master.
Special Cycles	3	Controls a device's action on Special Cycle Operations. A value of zero causes the device to ignore all Special Cycle Operations. A value of one allows the device to monitor Special Cycle Operations.
Memory Write and Invalidate Enable	4	This is an enable bit for using the Memory Write and invalidate command. When this bit is one, masters can generate the command. When this bit is zero, Memory Write must be used instead. State after RST# is zero. This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
VGA Palette Snoop	5	This bit controls how VGA-compatible devices handle accesses to their palette registers. When this bit is set, special palette snooping behavior is enabled (i.e., device must not respond). When the bit is reset, the device should treat palette accesses like all other accesses. VGA-compatible devices should implement this bit.
Parity Error Response	6	This bit controls the device's response to parity errors. When the bit is set, the device must take its normal action when a parity error is detected. When the bit is reset, the device must ignore any parity errors that it detects and continue normal operation. This bit must be set to zero after RST#. Devices that check parity must implement this bit. Devices are still required to generate parity even if parity checking is disabled.
Wait Cycle Control	7	This bit is used to control whether or not a device does address/ data stepping. Devices that never do stepping must hardwire this bit to zero. Devices that always do stepping must hardwire this bit to one. Devices that can do either, should make this bit read/write and have it initialize to one after RST#.
SERR# Enable	8	This bit is an enable bit for the SERR# driver. A value of zero disables the SERR# driver. A value of one enables the SERR# driver. This bit's state after reset is zero. All devices that have a SERR# pin must implement this bit. This bit (and bit 6) must be ON to report address parity errors.
Fast Back-to-Back Enable	9	This optional read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of one means the master is allowed to generate fast back-to-back transactions to different agents. A value of zero means fast back-to-back transactions are only allowed to the same agent.
Reserved	10 through 15	Reserved

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Device Status

The Status Register is used to record status information for PCI bus-related events. The definition of each of the bits is given in Table 3-2 on page 41, and the layout of the register is shown in Figure 3-3 below. Devices would not need to implement all bits, depending on device functionality. For instance, a device that acts as a target but will never signal target-abort, would not implement bit 11.

Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one (1). For instance, to clear bit 14 and not affect any other bits, write the value 0100_0000_0000_0000b to the register.

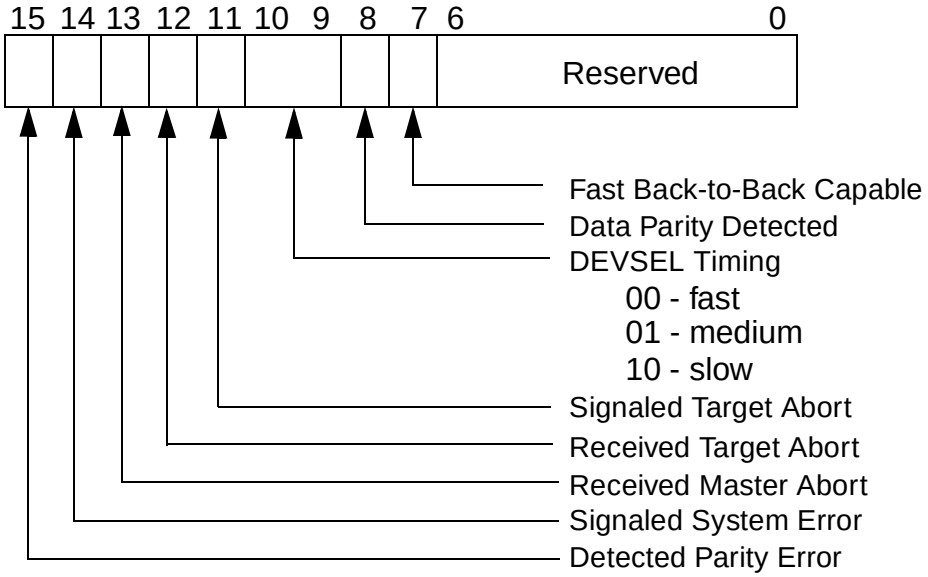


Figure 3-3 Status Register Layout

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Table 3-2 Status Register Bits

Bit Name	Bit Location	Descriptions
Reserved	0 through 6	Reserved
Fast Back-to-Back Capable	7	This optional read-only bit indicates whether or not the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent. This bit can be set to one (1) if the device can accept these transactions, and must be set to zero (0) otherwise.
Data Parity Detected	8	This bit is only implemented by bus masters. It is set when three conditions are met: 1) the bus agent asserted PERR# itself or observed PERR# asserted; 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; and 3) the Parity Error Response bit (Command register) is set.
DEVSEL Timing	9 and 10	These bits encode the timing of DEVSEL#. The bits are encoded as 00b for fast, 01b for medium, and 10b for slow (11b is reserved). These bits are read-only and must indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.
Signal Target Abort	11	This bit must be set by a target device whenever it terminates a transaction with target-abort. All master devices must implement this bit.
Received Target Abort	12	This bit must be set by a master device whenever its transaction is terminated with target-abort. All master devices must implement this bit.
Received Master Abort	13	This bit must be set by a master device whenever its transaction (except for Special Cycle) is terminated with master-abort. All master devices must implement this bit.
Signaled System Error	14	This bit must be set whenever the device asserts SERR#. Devices which will never assert SERR# do not need to implement this bit.
Detected Parity Error	15	This bit must be set by the device whenever it detects a parity error, even if parity error handling is disabled as controlled by bit 6 in the Command register.

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Miscellaneous Functions

This section describes the registers that are device independent, and only need to be implemented by devices that provide the described function.

Interrupt Line

The Interrupt Line register is an 8-bit register used to communicate interrupt line routing information. The register is read / write and must be implemented by any device (or device function) that uses an interrupt pin. Power On Seft-Test (POST) software will write the routing information into this register as it initializes and configures the system.

The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin is connected to. Device drivers and operating systems can use this information to determine priority and vector information. Values in this register are system architecture specific.[1]

Note

[1] For x86-based PCs, the values in this register corresponds to IRQ numbers (0 through 15) of the Standard Dual 8259 Configuration. The value 255 is defined as meaning ***unknown*** or ***no connection*** to the interrupt controller. Values between 15 and 255 are reserved.

Interrupt Pin

The Interrupt Pin register tells which interrupt pin the device (or device function) uses. A value of one (1) corresponds to INTA#. A value of two (2) corresponds to INTB#. A value of three (3) corresponds to INTC#. A value of four (4) corresponds to INTD#. Devices (or device functions) that do not use an interrupt pin must put a zero (0) in this register. This register is read-only.

Latency Timer

The Latency Timer Register (LAT) is an 8-bit wide register located in the PCI configuration space at offset $0D. Bits 7 through 3 are read and write accessible, while bits 2, 1, and 0 are read-only. This register initializes to 00.

The Latency Timer Register has meaning only when the VMIPCI-5579 PCI I / F is used as a bus master (DMA enabled) and pertains to the number of PCI bus clocks that this master will be guaranteed. The nonzero value is internally decremented after this device has been granted the bus and has asserted FRAME#. Prior to this latency timer count reaching zero, this device can ignore the removal of the bus grant and may continue to use the bus for data transfers. This PCI configuration register is used to ensure that no resource dominates the PCI bus and that bus arbitration occurs on a regular basis. The VMIPCI-5579 will request the PCI bus when the DMA process is enabled and the VMIPCI-5579 is ready to move data. The complete transfer block size may be broken into smaller burst automatically by the PCI I / F since the VMIPCI-5579 must release the bus at regular intervals. The maximum value the user can write to this register is $F0. The user only has to write this value one time; this value is then used by the counter on all master cycles.

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Base Addresses

One of the most important functions for enabling superior configurability and ease-of-use is the ability to relocate PCI devices in the address spaces. At system powerup, device independent software must be able to determine what devices are present, build a consistent address map, and determine if a device has an expansion ROM. Each of these areas are covered in the following sections.

Each of the six Base Address Registers are used in a similar but independent manner. The bit definitions and procedures for using the registers is outlined in the following section.

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Address Maps

Power-up software needs to build a consistent address map before booting the machine to an operating system. This means it has to determine how much memory is in the system, and how much address space the I/O controllers in the system require. After determining this information, power-up software can map the I/O controllers into reasonable locations and proceed with system boot. In order to do this mapping in a device independent manner, the base registers for this mapping are placed in the predefined header portion of configuration space.

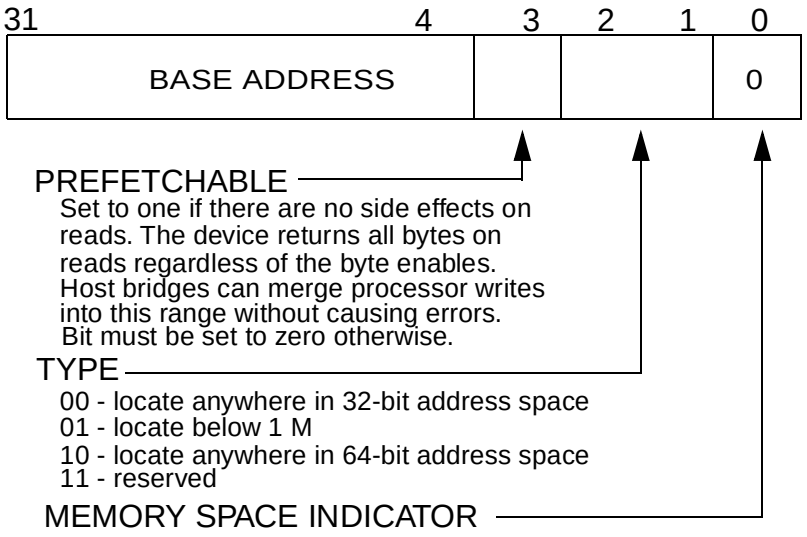


Figure 3-4 Base Address Register for Memory

Bit 0 in all base registers is read-only and used to determine whether the register maps into Memory or I/O space. Base registers that map to Memory space must return a zero (0) in bit 0. Base registers that map to I/O space must return a one (1) in bit 0.

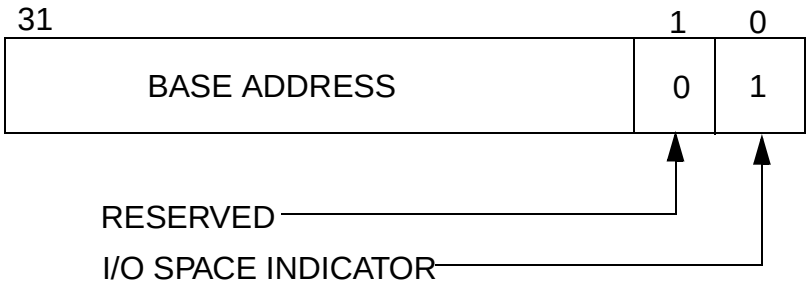


Figure 3-5 Base Address Register for I/O

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Base registers that map into I/O space are always 32 bits with bit 0 hardwired to a one (1), bit 1 is reserved and must return zero (0) on reads, and the other bits are used to map the device into I/O space[1].

Base registers that map into memory space (see Figure 3-5 on page 44) can be 32 bits wide to support mapping into a 64-bit address space) with bit 0 hardwired to a zero (0). For memory base registers, bits 2 and 1 have an encoded meaning as shown in Table 3-3 below. Bit 3 should be set to one (1) if the data is prefetchable, and reset to zero (0) otherwise. A device can mark a range as prefetchable[2]: if there are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and host bridges can merge processor writes into this range[2] without causing errors. Bits 0 through 3 are read-only.

Table 3-3 Bits 2/1 Encoding

Bits 2/1	Definition
00	Base register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
01	Base register is 32 bits wide but must be mapped below 1 Mbyte in memory space.
10	Base register is 64 bits wide and can be mapped anywhere in the 64-bit address space.
11	Reserved

The number of upper bits that a device actually implements depends on how much of the address space the device will respond to. A device that wants a 1 Mbyte memory address space (using a 32-bit base address register) would build the top 12 bits of the address register hardwiring the other bits to zero (0).

Powerup software can determine how much address space the device requires by writing a value of all ones to the register and then reading the value back. The device will return zeros in all don't care address bits, effectively specifying the address space required.

This design implies that all address spaces used are a power of two in size, and are naturally aligned. Devices are free to consume more address space than required, but decoding down to a 4 Kbyte space for memory and 256 bytes for I/O is suggested for devices that need less than those amounts. Devices that do consume more address space than they use are not required to respond to the unused portion of that address space.

Six DWORD locations are allocated for Base Address registers starting at offset $10 in configuration space. The first Base Address register is always located at offset $10. The second register may be at offset $14 or $18 depending on the size of the first. The offsets of subsequent Base Address registers are determined by the size of previous Base Address registers.

A typical device will require one memory range for its control functions. Some graphics devices may use two ranges, one for control functions and another for a frame buffer. A device that wants to map control functions into both memory and I/O space at the same time must implement two base registers (one Memory, one I/O). The driver for that device might only use one space in which case the other space will

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be unused. Devices should always allow control functions to be mapped into memory space.

Note

[1]The I/O address will have 01b in the least significant bits, but the base is at 00b. If, for example, the configuration places the I/O address at $FF00 in the I/O space, the base address register will read $FF01.

Note

[2]Any device that has a range that behaves like normal memory, but doesn't participate in PCI's caching protocol, should mark the range as prefetchable. A linear frame buffer in a graphics device is an example of a range that should be marked prefetchable.

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PCI bus Operation Registers

The PCI bus operation registers are mapped as sixteen consecutive Lword registers located at the address space (I/O) specified by the Base Address Register 0. Table 3-4 below lists the PCI bus Operation Registers.

Table 3-4 PCI bus Operation Register Map

Offset	Descriptions	Mnemonic	Access Mode
$00	I/O Mailbox 1	OMB1	Lword (R/W)
$04	I/O Mailbox 2	OMB2	Lword (R/W)
$08	I/O Mailbox 3	OMB3	Lword (R/W)
$0C	I/O Mailbox 4	OMB4	Lword (R/W)
$10	Incoming Mailbox 1	IMB1	Lword (Read Only)
$14	Reserved	----	----
$18	Reserved	----	----
$1C	Reserved	----	----
$20	Reserved	----	----
$24	Master Write Address Register	MWAR	Lword (R/W)
$28	Master Write Transfer Count Register	MWTC	Lword (R/W)
$2C	Master Read Address Register	MRAR	Lword (R/W)
$30	Master Read Transfer Count Register	MRTC	Lword (R/W)
$34	Reserved	----	----
$38	Interrupt Control and Status	INTCSR	Lword (R/W)
$3C	Bus Master Control/Status	MCSR	Lword (R/W)

The PCI I/F IC has other functions that are not utilized in this implementation. Reserved bits should be zero (0) when written to and ignored when read.

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User I/O Outgoing Mailboxes (OMB1, OMB2, OMB3, OMB4)

The lowest four Lwords of I/O space on the board contain four user mailbox registers. These mailboxes are 32-bit R/W locations that are accessible to the user for any purpose. The access time for each of these registers is faster than a single memory-mapped access. These registers are not reflected across the network.

Register Name:	User I/O Outgoing Mailboxes 1-4
Address Offset	0h, 4h, 8h, Ch
Power-up Value:	xxxxxxxxh
Attribute:	Read/Write
Size:	32 bits

Figure 3-6 User I/O Outgoing Mailbox Registers

Incoming Mailbox (IMB1)

32-bit, Read only, located at I/O offset $10.

IMB1 will never contain useful information, but due to the architecture of the PCI I/F and the way the PCI interrupts are generated this register must be read during some of the interrupt service routines. The interrupt convention involving the read of this register is defined in the section entitled *Using Interrupts* on page 83.

Register Name:	Incoming Mailbox
Address Offset	10h
Power-up Value:	xxxxxxxxh
Attribute:	Read Only
Size:	32 bits

Figure 3-7 Incoming Mailbox Register

Master Write Address Register (MWAR)

This register is used to establish the PCI address for data moving from the VMIPCI-5579 to the PCI bus during DMA write operations. It consists of a 30-bit counter with the lowest two bits hardwired as zeros. (See Figure 3-8 on page 49.)

The Master Write Address Register is continually updated during the transfer process and will always be pointing to the next unwritten location. Reading of this register during a transfer process is permitted and can be used to monitor the progress of the transfer. During the address phase for bus master write transfers, the two least significant bits presented on the PCI bus pins AD[31:0] will always be zero. This

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identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium® processor cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the S593X controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation.

Register Name:	Master Write Address
Address Offset:	24h
Power-up Value:	00000000h
Attribute:	Read/Write
Size:	32 bits

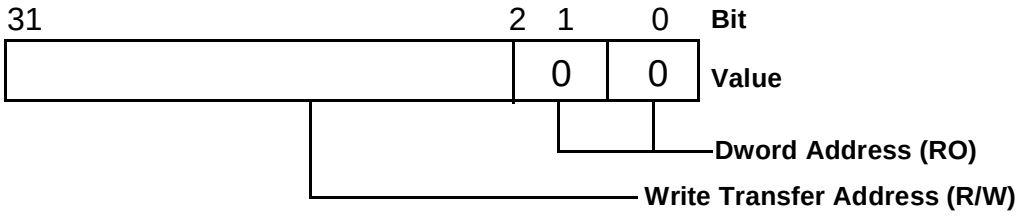


Figure 3-8 Master Write Address Register

Master Write Transfer Count Register (MWTC)

The Master Write Transfer Count Register is used to convey to the PCI DMA controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI write operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated. Figure 3-9 is an illustration of the MWTC register.

Register Name:	Master Write Transfer Count
Address Offset:	28h
Power-up Value:	00000000h
Attribute:	Read/Write
Size:	32 bits

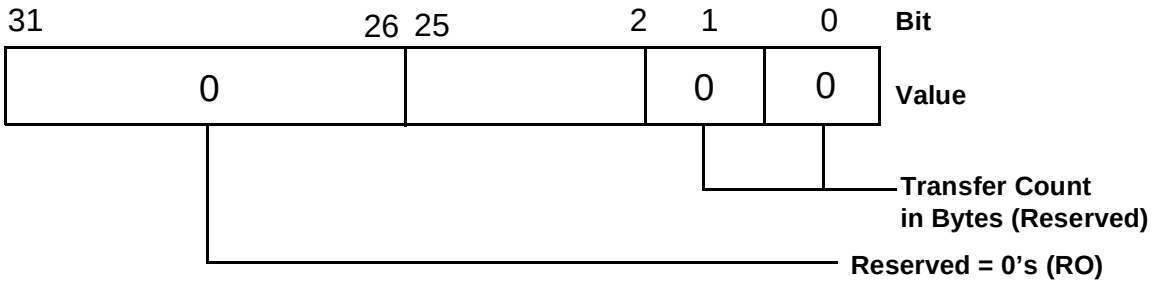


Figure 3-9 Master Write Transfer Count Register

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Master Read Address Register (MRAR)

This register is used to establish the PCI address for data moving to the VMIPCI-5579 from the PCI bus during DMA read operations. It consists of a 30-bit counter with the low-order two bits hardwired as zeros.

The Master Read Address Register is continually updated during the transfer process and will always be pointing to the next unread location. Reading of this register during a transfer process is permitted and may be used to monitor the progress of the transfer. During the address phase for bus master read transfers, the two least significant bits presented on the PCI bus AD[31:0] will always be zero. This identifies to the target memory that the burst address sequence will be in a linear order rather than in an Intel 486 or Pentium® processor cache line fill sequence. Also, the PCI bus address bit A1 will always be zero when this controller is the bus master. This signifies to the target that the controller is burst capable and that the target should not arbitrarily disconnect after the first data phase of this operation. Figure 3-10 is an illustration of this register.

Register Name:	Master Read Address
Address Offset:	2Ch
Powerup Value:	00000000h
Attribute:	Read/Write
Size:	32 bits

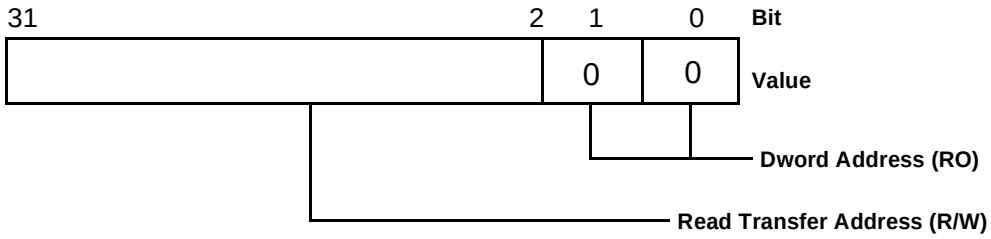


Figure 3-10 Master Read Address Register

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Master Read Transfer Count Register (MRTC)

The Master Read Transfer Count Register is used to convey to the PCI DMA controller the actual number of bytes that are to be transferred. The value in this register is decremented with each bus master PCI read operation until the transfer count reaches zero. Upon reaching zero, the transfer operation ceases and an interrupt may be optionally generated. Figure 3-11 is an illustration of this register.

Register Name:	Master Read Transfer Count
Address Offset:	30h
Powerup Value:	00000000h
Attribute:	Read/Write
Size:	32 bits

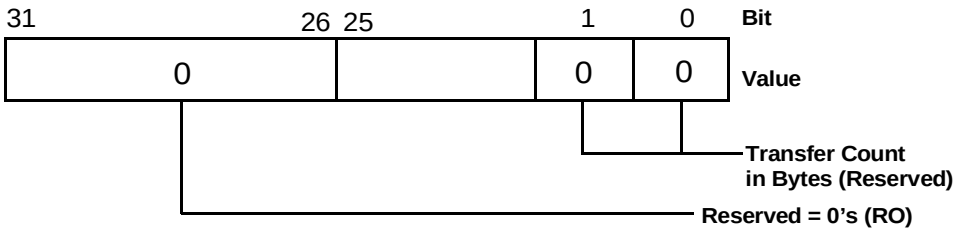


Figure 3-11 Master Read Transfer Count Register

Interrupt Control and Status Register (INTCSR)

This register provides the method for choosing which conditions are to produce an interrupt on the PCI bus interface, a method for viewing the cause of the interrupt, and a method for acknowledging (removing) the interrupt's assertion.

Register Name:	Interrupt Control/Status (INTCSR)
Address Offset:	38h
Powerup Value:	00000000h
Attribute:	Read/Write Read/Write_One_Clear
Size:	32 bits

Figure 3-12 Interrupt Control/Status Register

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The VMIPCI-5579 contains a single physical interrupt line with which to interrupt the host system and many sources within the VMIPCI-5579 can assert this line. To accommodate the many interrupt sources, the interrupt circuitry is configured in a two tiered fashion. The INTCSR register, which is described in this section, comprises the first or primary tier of interrupts. A secondary tier of interrupts are defined in a related register '*Extended Interrupt Status (EIS) Register* on page 77.' All secondary tier interrupts are funneled into the single Incoming Mailbox Interrupt (Bit 17) of this INTCSR register.

Table 3-5 Interrupt Control and Status Register Bit Map

Interrupt Control and Status Register (INTCSR): Relative Offset $38 Read/Write, Lword							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
0	0	0	0	0	0	0	0

Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
INT Asserted	0	Target Abort	Master Abort	Read Transfer	Write Transfer	Incoming Mailbox INT	0

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Interrupt on Read COMP	Interrupt on Write COMP	0	Incoming Mailbox Enable	Reserved			

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	0

Interrupt Control and Status Register Bit Definitions

Bits 31 through 24: **Reserved -** Always zero.

Bit 23: **Interrupt Asserted** - This read-only status bit indicates that one or more of the five possible interrupt conditions is present. This bit is the logical OR of the interrupt conditions described by bits 21 through 17 of this register.

Bit 22: **Reserved -** Always zero.

Bit 21: **Target Abort** - This bit signifies that an interrupt has been generated due to the VMIPCI-5579 encountering a target abort during a PCI bus cycle while the VMIPCI-5579 was the current bus master. This bit operates as read or write one clear. A write to this bit with the data of **one** will cause this bit to be reset; a write to this bit with the data of **zero** will not change the state of this bit.

Bit 20: **Master Abort -** This bit signifies that an interrupt has been generated due to the VMIPCI-5579 encountering a Master Abort on the PCI bus. A master abort occurs when there is no target response to a PCI bus cycle. This bit operates as read or write one clear. A write to this bit with the data of one (1) will cause this bit be reset; a write to this bit with the data of zero (0) will not change the state of this bit.

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Bit 19: **Read Transfer Complete -** This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data from the PCI bus to the add-on. This interrupt will occur when the Master Read Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of one (1) will cause this bit to be reset; a write to this bit with the data of zero (0) will not change the state of this bit.

Bit 18: **Write Transfer Complete -** This bit signifies that an interrupt has been generated due to the completion of a PCI bus master operation involving the transfer of data to the PCI bus from the add-on. This interrupt will occur when the Master Write Transfer Count register reaches zero. This bit operates as read or write one clear. A write to this bit with the data of one (1) will cause this bit to be reset; a write to this bit with the data of zero (0) will not change the state of this bit.

Bit 17: **Incoming Mailbox Interrupt -** This bit is set when the mailbox selected by bits 12 through 8 of this register are written by the add-on interface. This bit operates as read or write one clear. A write to this bit with the data of one (1) will cause this bit to be reset; a write to this bit with the data as zero (0) will not change the state of this bit.

This bit functions as the common access point for all secondary tier interrupts, which are controlled by the '*Extended Interrupt Status (EIS) Register* on page 77.' Assertion of any secondary tier interrupt will also result in bit 17 of this register being asserted.

Bit 16: **Reserved -** Write to zero.

Bit 15: **Interrupt on Read Transfer Complete -** This bit enables the generation of an interrupt when the read transfer count reaches zero. This bit is read / write.

Bit 14: **Interrupt on Write Transfer Complete -** This bit enables the generation of an interrupt when the write transfer count reaches zero. This bit is read / write.

Bit 13: **Reserved -** Write to zero.

Bit 12: **Incoming Mailbox Enable -** This bit allows the VMIPCI-5579 to produce a PCI interrupt when an interrupt is received over the Reflective Memory network. This bit is read / write.

Bits 11 Through 0: **Reserved -** Write to zero**.**

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Bus Master Control and Status Register (MCSR)

This register provides for overall control of the VMIPCI-5579 PCI I/F. It is used to enable bus mastering for both data directions as well as providing a method to perform software resets.

Register Name:	Bus Master Control/Status (MCSR)
Address Offset:	3Ch
Powerup Value:	000000E6h
Attribute:	Read/Write, Read Only, Write Only
Size:	32 bits

Figure 3-13 Bus Master Control and Status Register

Table 3-6 on page 55 shows the bit definitions for this register. The following PCI bus controls are available:

- Write Transfer Enable
- Write master requests on four or more DMA FIFO words available (full)
- Read transfer enable
- Read master requests on four or more DMA FIFO available (empty)
- Assert reset to VMIPCI-5579
- Reset VMIPCI-5579 to PCI DMA FIFO flags
- Reset PCI to VMIPCI-5579 DMA FIFO flags
- Reset mailbox empty full status flags

The following PCI interface status flags are provided:

- PCI to VMIPCI-5579 DMA FIFO FULL
- PCI to VMIPCI-5579 DMA FIFO has four or more empty locations
- PCI to VMIPCI-5579 DMA FIFO EMPTY
- VMIPCI-5579 to PCI DMA FIFO FULL
- VMIPCI-5579 to PCI DMA FIFO has four or more words loaded
- VMIPCI-5579 to PCI DMA FIFO EMPTY
- PCI to VMIPCI-5579 Transfer Count = Zero
- VMIPCI-5579 to PCI Transfer Count = Zero

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Table 3-6 Bus Master Control and Status Register Bit Map

Bus Master Control and Status Register (MCSR) Relative Offset $3C, Read/Write, Lword							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
0				RC3	RC2	RC1	RC0

Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved 0000 0000							

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 08**
0	Read Transfer Enable	Read FIFO Management Scheme	0	0	Write Transfer Enable	Write FIFO Management Scheme	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
PCI-5579 to PCI Transfer Count	PCI to PCI-5579 Transfer Count	PCI-5579 to PCI FIFO Empty	PCI-5579 to PCI 4+ Space	PCI-5579 to PCI FIFO Full	PCI to PCI-5579 FIFO Empty	PCI to PCI-5579 FIFO 4+ Spaces	PCI to PCI-5579 FIFO Full

Bus Master Control and Status Register Bit Definitions

Bits 31 through 28: **Reserved** - Write to zero.

Bit 27: **Mailbox Flag (Reset Control (RC3) -** Writing a one to this bit causes all mailbox status flag to become reset (EMPTY). It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.

Bit 26: **VMIPCI-5579 to PCI FIFO Status (Reset Control (RC2) -** Writing a one to this bit causes the VMIPCI-5579 to PCI (bus master memory writes) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus word flag to reset. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.

Bit 25: **PCI to VMIPCI-5579 FIFO Status (Reset Control (RC1) -** Writing a one to this bit causes the PCI to VMIPCI-5579 (bus master memory reads) FIFO empty flag to set indicating empty and the FIFO FULL flag to reset and the FIFO Four Plus words available flag to set. It is not necessary to write this bit as zero because it is used internally to produce a reset pulse. Since reading of this bit will always produce zeros, this bit is write only.

Bit 24: **VMIPCI-5579 Pin (Reset Control (RC0) -** Writing a one (1) to this bit resets the entire VMIPCI-5579 Reflective Memory board. All registers will be put in their default condition. Writing a zero (0) to this bit is necessary to remove the assertion of the reset. This register bit is read / write.

Bits 23 through 15: **Reserved:** Write to zero.

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Bit 14: **Read Transfer Enable:** This bit must be set to a one (1) for VMIPCI-5579 PCI bus master read transfers to take place. Writing a zero (0) to this location will suspend an active transfer. An active transfer is one in which the terminal count is not zero.This bit actually initiates the DMA transfer which has been setup in the MRAR (Master Read Address Register) and MRTC (Master Read Transfer Count) registers.

Bit 13: **Read FIFO Management Scheme:** When set to a one (1), this bit causes the controller to refrain from requesting the PCI bus unless it has four or more vacant FIFO locations to fill. Once the controller is granted the PCI bus or is in possession of the bus due to the write channel, this constraint is not meaningful. When this bit is zero (0), the controller will request the PCI bus if it has at least one vacant FIFO word.

Bits 12 and 11: **Reserved:** Write to zero.

Bit 10: **Write Transfer Enable:** This bit must be set to a one (1), for PCI bus master write transfers to take place. Writing a zero (0) to this location will suspend an active transfer. An active transfer is one in which the terminal count is not zero. This bit initiates the DMA write transfer which has been setup in the MWAR (Master Write Address Register) and MWTC (Master Write Transfer Count) registers.

Bit 9: **Write FIFO Management Scheme:** When set to a one (1) this bit causes the controller to refrain from requesting the PCI bus unless it has four or more FIFO locations filled. Once the VMIPCI-5579 controller is granted the PCI bus or is in possession of the bus due to the write channel, this constraint is not meaningful. When this bit is zero (0) the controller will request the PCI bus if it has at least one valid FIFO word.

Bit 8: **Reserved:** Write to zero.

Bit 7: **VMIPCI-5579 to PCI Transfer Count Equal Zero (RO):** This bit is a one (1) to signify that the write transfer count is all zeros.

Bit 6: **PCI to VMIPCI-5579 Transfer Count Equals Zero (RO):** This bit is a one (1) to signify that the read transfer count is all zeros.

Bit 5: **VMIPCI-5579 to PCI DMA FIFO Empty:** This bit is a one (1) when the VMIPCI-5579 to PCI bus DMA FIFO is completely empty.

Bit 4: **VMIPCI-5579 to PCI 4+ Words:** This bit is a one (1) when there are four or more FIFO words valid within the VMIPCI-5579 to PCI bus DMA FIFO.

Bit 3: **VMIPCI-5579 to PCI DMA FIFO Full:** This bit is a one (1) when the VMIPCI-5579 to PCI bus DMA FIFO is completely full.

Bit 2: **PCI to VMIPCI-5579 DMA FIFO Empty:** This bit is a one (1) when the PCI bus to VMIPCI-5579 DMA FIFO is completely empty.

Bit 1: **PCI to VMIPCI-5579 DMA FIFO 4+ Space:** This bit signifies that there are at least four empty words within the PCI to VMIPCI-5579 DMA FIFO.

Bit 0: **PCI to VMIPCI-5579 DMA FIFO Full -** This bit is a one (1) when the PCI bus to VMIPCI-5579 DMA FIFO is completely full.

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VMIPCI-5579 Reflective Memory-Mapped Control Registers

The third set of control registers are those that have more direct control over the Reflective Memory board. Although the VMIPCI-5579 Reflective Memory board is software transparent on power up, some registers are present to facilitate user information and interrupt generation. Table 3-7 below shows the memory map of the VMIPCI-5579.

Table 3-7 VMIPCI-5579 Register Map

Offset	Descriptions	Mnemonic	Access Mode
$0	Reserved	----	----
$1	Board ID	BID	Byte (R)
$2 and $3	Reserved	----	----
$4	Node ID	NID	Byte (R)
$5 through $7	Reserved	----	----
$8	INT and Receiver Status	IRS	Byte (R/W)
$9	Control and Status 1	CSR 1	Byte (R/W)
$A and B	Reserved	----	----
$C	Control and Status 2	CSR 2	Byte/Word (R/W)
$D	Control and Status 3	CSR 3	Byte/Word (R/W)
$E and $F	Reserved	----	----
$10	Command Node	CMDN	Byte, Word, Lword (W)
$11	Command	CMD	Byte, Word, Lword (W)
$12 and $13	Command Data Registers	CMDD	Byte, Word, Lword (W)
$14	INT Control and Status	ICSR	Byte/Word (W)
$15 Through $17	Reserved	----	----
$18	INT1 Sender ID	SID1	Lword (R/W)
$19	INT1 Flag Register	IFR1	Lword (R)
$1A and $1B	INT1 Data Registers	IDR1	Lword (R)
$1C	INT2 Sender ID	SID2	Lword (R/W)
$1D	INT2 Flag Register	IFR2	Lword (R)
$1E and $1F	INT2 Data Registers	IDR2	Lword (R)
$20	INT3 Sender ID	SID3	Lword (R/W)
$21	INT3 Flag Register	IFR3	Lword (R)
$22 and $23	INT3 Data Registers	IDR3	Lword (R)
$24 through $27	DMA Start Address	DADD	Lword (W)
$28	Extended Interrupt Status	EIS	Byte (R/W)
$29	Extended Control and Status 3	ECSR3	Byte/Word (R/W)
$2A	Manual Interrupt Control and Status	MICS	Byte (R/W)
$2B and $2C	Reserved	----	----
$2D	Memory Access Control Register	MACR	Byte (W)
$2E through $3F	Reserved	----	----

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Table 3-7 VMIPCI-5579 Register Map (Continued)

Offset	Descriptions	Mnemonic	Access Mode
$40	Start of RAM		Byte, Word, Lword (R/W)
$00FFFFF	End of 1 Mbyte RAM		Byte, Word, Lword (R/W)
$03FFFFF	End of 4 Mbyte RAM		Byte, Word, Lword (R/W)
$07FFFFF	End of 8 Mbyte RAM		Byte, Word, Lword (R/W)
$0FFFFFF	End of 16 Mbyte RAM		Byte, Word, Lword (R/W)
$1FFFFFF	End of 32 Mbyte RAM		Byte, Word, Lword (R/W)
$3FFFFFF	End of 64 Mbyte RAM		Byte, Word, Lword (R/W)

Note

Two bytes can be accessed as a word if they are contiguous, and on an even word boundary. Two words can be assecced as a Lword if they are contiguous, and on an even Lword boundary.

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Board Identification (BID) Register

The Board Identification (BID) Register is read-only and will be assigned a fixed value. This will allow the user to verify the presence of the Reflective Memory board. This register may be considered redundant on the VMIPCI-5579 since a Device ID is present in the PCI configuration memory on this board. The board ID for the VMIPCI-5579 is $60.

Table 3-8 Board ID Register Bit Map

Board Identification Register (BID): Relative Offset $01, Read-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	1	1	0	0	0	0	0

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Node Identification (NID) Register

The Node ID Register contains the 8-bit node ID (0 to 255) which is used over the network. This is set by the Node ID jumpers of (E2) on the board.

Table 3-9 Node ID Register Bit Map

Node Identification Register (NID): Relative Offset $04, Read-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Node ID							

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Interrupt and Receiver Status (IRS) Register

Table 3-10 Interrupt and Receiver Status Register Bit Map

Interrupt and Receiver Status Register (IRS): Relative Offset $08, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
RCVR SYNC'D Low	Latched SYNC Loss	Bad Data Received	RCVR FIFO Half-Full Low	Reset Node Received	INT3 Pending	INT2 Pending	INT1 Pending

Interrupt and Receiver Status Register Bit Definitions

Bit 7: **RCVR SYNC'D, Low -** A logical zero (0) in this bit location indicates the fiber-optic receiver is currently synchronized to incoming data. This bit is read-only and immediate status only.

Bit 6: **Latched SYNC Loss** - A one (1) in this bit location indicates that the receiver has lost synchronization with incoming data one or more times since the last time this register was cleared. This bit is cleared by writing a zero (0) to this bit location in the register.

Bit 5: **Bad Data Received** - A transfer error has occurred. This bit is cleared by writing a zero (0) to this register. 1 = bad data received.

Bit 4: **RCVR FIFO Half-Full, Low** - The receiver FIFO is not half-full. Writes have no effect on this register (immediate status only). 1 = FIFO not more than half-full.

Bit 3: **Reset Node Received** - A one (1) in this bit location indicates that the board has received a Reset Node Command from the network. This bit is cleared by writing a zero (0) to this location in the register. In compliance with the PCI Specification, the host must perform the actual reset function. This bit is only an indicator. This is not a hard reset, it is an interrupt that is in keeping with the VME version of reflective memory products. The reset is a software controlled interrupt.

Bit 2: **INT3 Pending** - A one (1) in this bit location indicates that at least one level 3 interrupt has been received (receiver interrupt FIFO3 is not empty). Writes have no effect on this bit location (Immediate Status only).

Bit 1: **INT2 Pending** - A one (1) in this bit location indicates that at least one level 2 interrupt has been received (receiver interrupt FIFO2 is not empty). Writes have no effect on this bit location (immediate status only).

Bit 0: **INT1 Pending** - A one (1) in this bit location indicates that at least one level 1 interrupt has been received (receiver interrupt FIFO1 is not empty). Writes have no effect on this bit location (immediate status only).

Note

The IRS register of the VMIPCI-5579 is identical to that of the VMIPCI-5588 to maintain backward software compatibility. To access the extended interrupt functions use the Extended Interrupt Status (EIS) register at relative offset $28.

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Control and Status Register 1 (CSR1)

The CSR contains local node state information and is mapped as follows.

Table 3-11 Control and Status Register 1 Bit Map

Control and Status Register 1 (CSR1): Relative Offset $09 Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
RCVR SIG DET Low	RCVR FIFO Half Full Low	TX FIFO Half Full Low	TX FIFO Empty Low	DMA Write Enable	Own Data	DMA Read Enable	Fast Mode

Control and Status Register 1 Bit Definitions

Bit 07: **RCVR SIG DET, Low -** When this bit is zero (0), the fiber-optic receiver is currently receiving a signal that is either data or SYNC patterns (Read-Only). The green Signal Detect LED will also be **ON** when a signal is present.

Bit 06: **RCVR FIFO Half-Full, Low -** When this bit is one (1), the receive FIFO is less than half-full (Read-Only).

Bit 05: **Transmit FIFO Half-Full, Low** - When this bit is zero (0), the transmit FIFO on the local node is half full (Read-Only).

Bit 04: **Transmit FIFO Empty, Low-** When this bit is one (1), the transmit FIFO on the local node is not empty (Read-Only).

Bit 03: **DMA Write Enable -** When this bit is set to a one (1), internal data transfers are allowed between memory and PCI DMA FIFO. This bit should not be set if bit 1 (Read DMA Enable bit) is set. This bit initiates the DMA write transfer which has been setup in the MWAR (Master Write Address Register) and MWTC (Master Write Transfer Count) registers.

Bit 02: **Own-Data -** When this bit is set to one (1), a data packet that this node sent has been received. Writing a zero (0) to this bit will clear it. The act of writing a zero (0) will generate a packet on the network. Therefore, it will be set back to one (1) as soon as the packet goes around the ring.

Bit 01: **DMA Read Enable -** When this bit is set to a one (1), internal data transfers are allowed between the PCI DMA FIFO and memory. This bit should not be set if bit 3 (DMA Write Enable bit) is set. This bit actually initiates the DMA transfer which is setup in the MRAR (Master Read Address Register) and MRTC (Master Read Transfer Count) registers.

Bit 00: **Fast Mode** - When this bit is set to a one (1), Fast mode is enabled. Fast mode transmits each data transfer once on the fiber-optic link. This bit indicates the status of the Fast jumper and is read-only.

1= Jumper omitted (Fast Mode)
0= Jumper Installed (Redundant Mode)

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Control and Status Register 2 (CSR2)

CSR2 is an additional board control register. The bit map and bit definitions are shown below.

Table 3-12 Control and Status Register 2 Bit Map

Control and Status Register 2 (CSR2): Relative Offset $0C, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
FAIL LED (Status B LED)	Node Bypass	ADDR Offset	Reserved				

Control and Status Register 2 Bit Definitions

Bit 7: **FAIL LED (Status B LED) -** When this bit is set to one (1), the red FAIL LED is OFF. The LED is ON after power up. The host system must manually write a one (1) to this bit to turn the Fail LED OFF. This is the red LED, “B” on the front panel.

Bit 6: **Node Bypass -** Writing a one (1) to this bit enables this board to work in conjunction with a Node Bypass board by shutting off the Transmitter optics if the Receiver loses the optical signal.

Bit 5: **Address Offset** - This bit is used for 32 Mbyte boards **only**. The Offset Address bit can be used to map the 32 Mbyte board into the upper 32 Mbytes of a 64 Mbyte board, if one is installed on the network.

1 = Upper 32 Mbytes - Shifts Address of Fiber-Optic
0 = Lower 32 Mbytes - Data Transmissions

Bits 4 through 0: **Reserved -** These bits are currently reserved, and should not be used.

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Control and Status Register 3 (CSR3)

CSR3 is mainly a board control register, it should not be used for VMIPCI-5579 board control. This is a legacy register that is used for boards going in older systems that used VMIxxx-5588 Reflective Memory boards. The VMIPCI-5579 software should use the information in extended CSR3 at offset $29.

Table 3-13 Control and Status Register 3 Bit Map

Control and Status Register 3 (CSR3): Relative Offset $0D, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Flag A	Reserved 1, 1, 0			User Flag B	Endian Control EC2	Endian Control EC1	Endian Control EC0

Control and Status Register 3 Bit Definitions

Bit 7: **User Flag A -** This bit is a read / write user-defined flag.

Bits 6, 5, and 4: **Reserved -** These bits are currently reserved, and should not be used. The bits are read only bits, and read 1, 1, 0 respectfully. This signifies that it is a 16 Mbyte board in previous reflective memory products.

Bit 3: **User Flag B** - This bit is a read / write user-defined flag.

Bits 2, 1, and 0: **Endian Control EC[2:0] -** These bits are for big-endian / little-endian conversions between PCI and any VMEbus machines. Because of endian swaps between VMEbus and PCI bus, swap on size function swaps bytes and words for 32-bit access. Swapping bytes for 16-bit access does nothing for byte accesses. The simplest way of using the VMIPCI-5579 hardware to take care of the byte-ordering problem is to configure it to swap according to size (see Table 3-14). Figure 3-14 on page 65 is an illustration of Endian conversion.



This register is identical to that of the VMIPCI-5588 to maintain software compatibility. For extended functions see the Extended Control and Status Register 3 at relative offset $29.



Endian control affects only read / write to the reflected portion of the memory - control register access and on-board memory is not affected.

Table 3-14 Size Swap for Endian Conversions

EC[2..0] States	Endian Conversion Applied
000	No Swap, straight through (*Default*)
100	Byte Swap
101	Word Swap
110	Byte and Word Swap
111	Swap on Size
Note: All other values are illegal, and are not used.	

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The Endian conversion mode Swap on Size reacts to the data based on its size and follows the convention:

1. If the data is a Lword (32 bits) then swap the bytes and words.
2. If the data is a Word (16 bits) then swap the bytes.
3. If the data is a Byte (8 bits) then do not swap.

Note

Dword is the name convention used in PCI manuals for 32-bit wide data transfers. Other places in this and other VMIC manuals can use the name convention Lword or longword for 32-bit wide data.

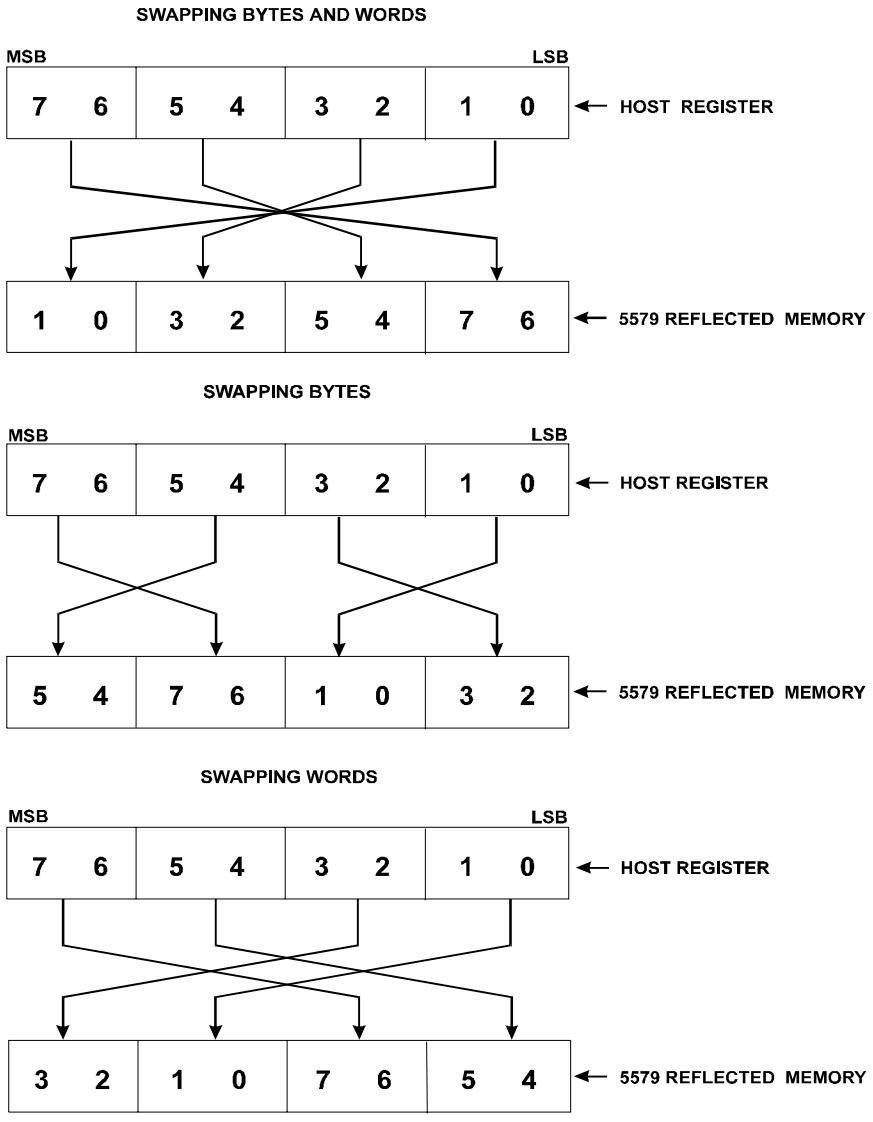


Figure 3-14 Example of Size Swap Endian Conversion

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Command Node (CMDN) Register

The CMDN register contains the Node ID of the node that is to receive the command in the Command (CMD) Register. See Table 3-16 on page 67 for the CMD bit map.

Table 3-15 Command Node Register Bit Map

Command Node Register (CMDN): Relative Offset $10, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CMD Target Node ID (0 TO 255)							

The Command Node (CMDN) register can be written in conjunction with the Command (CMD) register as a 16-bit word or, it can be written in conjunction with the Command (CMD) register plus the Command Data (CMDD 0 and CMDD1) registers as a 32-bit Lword.

Note

The Command Node register (CMDN) can be written repeatedly without invoking an interrupt at the receiving node.

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Command Register (CMD)

The VMIPCI-5579 can generate an interrupt to one or all other chassis through the use of the Command Register. Valid choices for interrupts are 1, 2, and 3. Table 3-17 shows all possible combinations. The interrupts are processed just like data so all words sent previous to the interrupt command are present on the receiving board's memory before the interrupt is issued to the receiving board. See Figure 3-15 on page 68 for an illustration of interrupt

Table 3-16 Command Register Bit Map

Command Register (CMD): Relative Offset $11, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data Bits	All Nodes	User Data Bits				L1	L2

Command Register Bit Definitions

Bits 7, 5, 4, 3, and 2: **User Defined Data Bits -** These bits are only valid for the VMIPCI-5579 products, and are not supported by the VMIxxx-5588 Reflective Memory products.

Bit 6: **ALL Nodes -** Writing a one (1) to this bit location causes all nodes on the ring to receive the command. A zero (0) in this bit position allows a specific node to receive commands, identified in the CMDN.

Bits 1 and 0: **Interrupt Level[1:0] -** When set these bits determine the level of interrupt to sent to the other nodes.

Table 3-17 Interrupt Levels

L1	L2	Function
0	0	Reset Node Interrupt
0	1	Interrupt 1 is generated
1	0	Interrupt 2 is generated
1	1	Interrupt 3 is generated

Note

Only the act of writing to the CMD Register actually invokes the interrupt at the receiving node.

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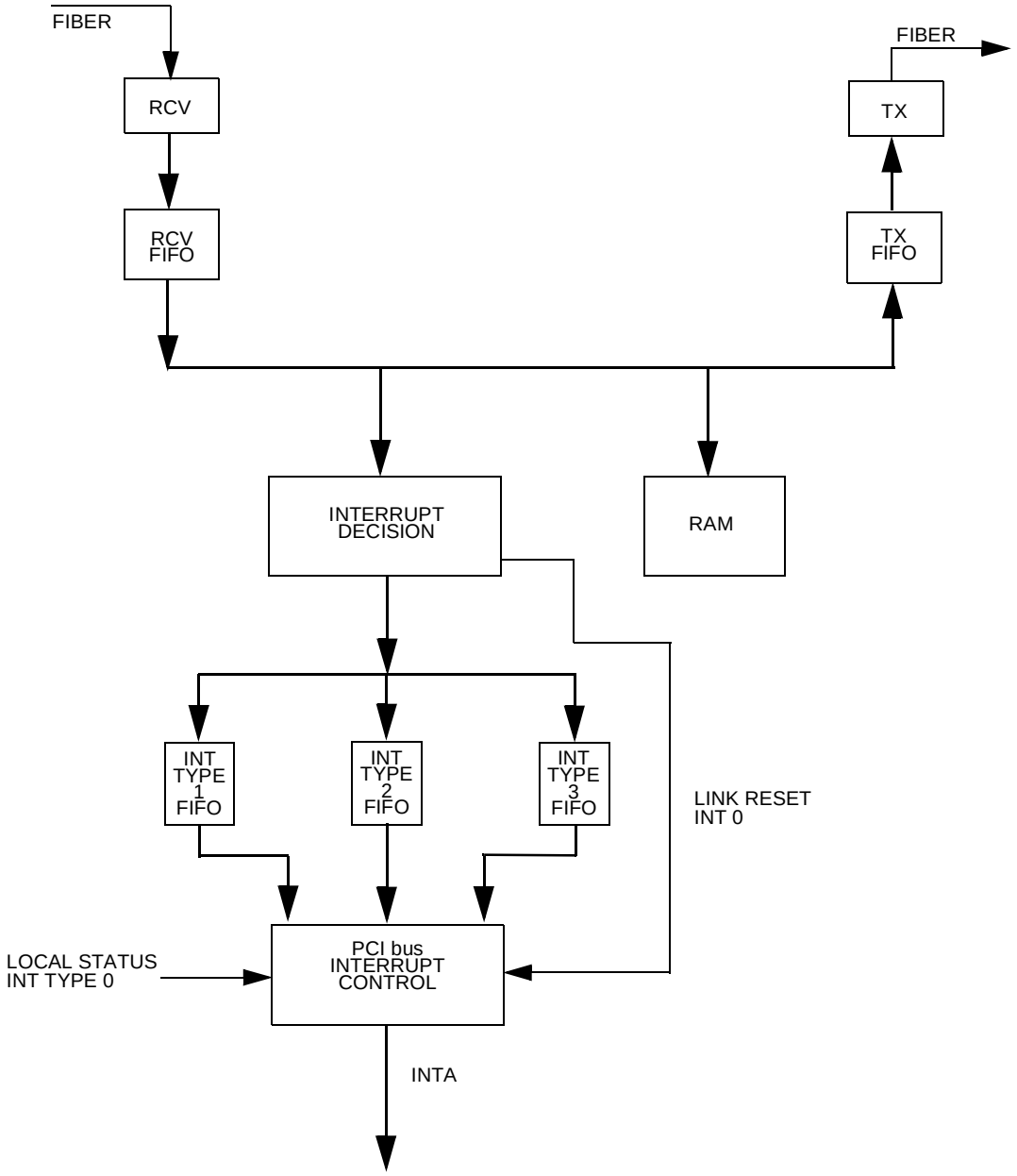


Figure 3-15 Interrupt/Data Receive Path

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Command Data Registers 0 and 1

The Command Data registers are actually write-only ports and the bits are not registered. In order for either of the Command Data registers to be stored in the receiving node's FIFO, they must be written in conjunction with the CMD register. Data register 0 (offset $12) can be written along with the CMD register (offset $11) as a 16-bit word. Likewise, the Data register 1 (offset $13), the Data register 0 (offset $12), the CMD register (offset $11) and the Command Node register (offset $10) can all be written together as one Lword. Any data written to these registers is transferred with the command packet to the receiving nodes.

Table 3-18 Command Data Registers 0 and 1 Bit Map

Command Data Register 0 (CMDD0): Relative Offset $12, Write-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data							

Command Data Register 1 (CMDD1): Relative Offset $13, Write-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data							

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Interrupt Control and Status Register (ICSR)

The ICSR register controls the secondary tier of interrupts. The assertion of any secondary tier interrupt shall also assert the primary level interrupt referred to as the Incoming Mailbox Interrupt.

Table 3-19 Interrupt Control and Status Register Bit Map

Interrupt Control and Status Register (ICSR): Relative Offset $14, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved	Global INT EN	EN INT Bad Data Received	EN INT RCVR FIFO HF	EN INT Reset Node Received	EN INT INT3 Pending	EN INT INT2 Pending	EN INT INT1 Pending

Interrupt Control and Status Register Bit Definitions

Bit 7: **Reserved -** This bit is currently reserved, and should not be used.

Bit 6: **Global INT Enable -** Writing a one (1) to this bit location enables individual bits 5 through 0. This bit is cleared after each time the PCI bus is interrupted and must be rearmed if more interrupts are desired.

Note The Global INT Enable bit, enables only secondary tier interrupts controlled by the ICSR register.

Bit 5: **EN INT, Bad Data Received -** This bit is an enable bit which allows interrupts to be generated if bad data is received. A one (1) equals Bad Data Interrupt Enabled. Bit 6 must be set to enable interrupts.

Bit 4: **EN INT, RCVR FIFO Half-Full -** This bit is an enable bit, that when set to a one (1) allows the RCVR FIFO half-full flag to generate an interrupt. A one (1) equals RCVR FIFO half-full interrupt enabled. Bit 6 must be set to enable interrupts.

Bit 3: **Enable Interrupt Reset Node Received -** This bit enables a PCI interrupt when a Reset Node Command is received. A one (1) is enabled. Bit 6 must also be a one (1).

Bit 2: **EN INT, INT3 Pending -** When this bit is set to one (1), an interrupt is generated if there is a level 3 INT pending and the global INT EN is active.

Bit 1: **EN INT, INT2 Pending -** When this bit is one (1), an interrupt is generated if there is a level 2 INT pending and the global INT EN is active.

Bit 0: **EN INT, INT1 Pending -** When this bit is set to one (1), an interrupt is generated if there is a level 1 INT pending and the global INT EN is active.

Note The IRS register must be read to determine who generated an interrupt if more than one source is enabled.

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Receiver Interrupt Registers Overview

The VMIPCI-5579 contains a set of Receiver Interrupt Registers, for each of the three attention interrupts that can be passed over the network. Each set of interrupt registers is actually constructed as a 32-bit wide by 63 deep FIFO. The least significant 8 bits of each FIFO are defined as the Sender ID Register. The Sender ID Registers have the same relative offsets and bit assignments as those of the VMIPCI-5588 to maintain a degree of backward compatibility. These Sender ID Registers contain the Node ID of the board that initiated the interrupt.

In addition to the Sender ID, the next 8 bits of each receiver interrupt FIFO are defined as an Interrupt Flag Register. If accessed as part of a 32-bit Lword, the Interrupt Flag register would correspond to bits D8 through D15, where the LSB is D8. The Interrupt Flag register is a copy of the CMD register of the node that initiated the interrupt. Therefore, the Interrupt Flag Registers contain three predefined bits that are considered status flags and five user defined data bits.

The most significant 16 bits of each receiver interrupt FIFO are defined as two Interrupt Data Registers. These data registers copy the contents of the CMDD0 and CMDD1 registers of the node that initiated the interrupt. The interrupt data is user-defined.



When reading the contents of the receiver FIFOs, some rules should be observed. The key rule is that the FIFO pointer increments when the Sender ID portion is read. As with any FIFO, once the pointer has moved, the contents previously directed by the pointer cannot be read again. This has a definite impact on the order in which portions of the receive FIFO should be read. The combination of Sender ID, Interrupt Flags, and Interrupt Data can all be read together as one 32-bit Lword. In this case, the FIFO pointer will increment with each read. If however, the host cannot perform Lword reads or if Lword reads are not desired, the content of the Interrupt Flag Register and Interrupt Data Registers must be read before reading the Sender ID register. Otherwise, the FIFO pointer will be pointing to the wrong flags and data. Actually, the flag and data registers can be read multiple times without affecting the FIFO pointer.



When bits 1 and 0 of the initiator's CMD registers are zero (0), a reset node command is issued. Unlike the three interrupts, the reset node command is not stored in a FIFO. Rather, it will set bit 3 in the IRS register, and will assert a PCI interrupt if enabled in the ICSR register.

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Interrupt Sender ID Registers

These registers contain the ID of the node that send the local node interrupt types 1 through 3.

Table 3-20 Interrupt Sender ID Register Bit Map

Interrupt Sender ID Register (INT1): Relative Offset $18 Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
INT1 Sender ID							

Interrupt Sender ID Register (INT2): Relative Offset $1C Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
INT2 Sender ID							

Interrupt Sender ID Register (INT3): Relative Offset $20 Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
INT3 Sender ID							

Interrupt Sender ID Registers, Bit Definitions

Bits 7 through 0: **INT1 Sender ID:** Contains the ID of the node that sent the local node INT Type 1. A write to this location clears all pending INT1 interrupts.

Bits 7 through 0: **INT2 Sender ID:** Contains the ID of the node that sent the local node INT Type 2. A write to this location clears all pending INT2 interrupts.

Bits 7 through 0: **INT3 Sender ID:** Contains the ID of the node that sent the local node INT Type 3. A write to this location clears all pending INT3 interrupts.

In the interrupt handling sequence, the user should perform only one read of the Sender ID per interrupt cycle.

Each Sender ID register is implemented with a FIFO. When the user reads a sender ID, all of the data sent with that particular interrupt is removed from the FIFO. If the user attempts to read the sender ID again, the output will be the next interrupt in the FIFO. However, if the FIFO is empty, the output is indeterminate. Therefore, do not key on the presence of any value in the Sender ID register to indicate a pending interrupt. Instead, use the Interrupt and Receive Status register. The depth of the Sender ID register in the VMIPCI-5579 is 64 locations.

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Interrupt Flag Registers (IFR1, IFR2, IFR3)

The IFR1, IFR2, and IFR3 registers are 8-bit subsections of the receiver interrupt FIFOs. They are used to pass three flags and five user-defined data bits from the CMD register of interrupt initiating node to the receiving node's interrupt FIFO. If read in conjunction with the Sender ID Register as a 16-bit word or 32-bit Lword, the IFRx register would correspond to data bits D8 through D15.

Table 3-21 Interrupt Flag Registers Bit Map

Interrupt Flag 1 (IFR1): Relative Offset $19 Read-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data	Global Flag	User Data				INT Level 1	INT Level 0

Interrupt Flag 2 (IFR2): Relative Offset $1D Read-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data	Global Flag	User Data				INT Level 1	INT Level 0

Interrupt Flag 3 (IFR3): Relative Offset $21 Read-Only, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data	Global Flag	User Data				INT Level 1	INT Level 0

Interrupt Flag Bit Definitions

Bits 7, 5, 4, 3, 2: **User Data** - These bits are user-defined. They contain a copy of data written into the corresponding bits of the CMD register of the node that initiated the interrupt.

Bit 6: **Global Flag** - A one (1) in this bit location indicates the current interrupt was issued globally to all nodes of the network.

Bits 1 and 0 **INT Level 1 and 0** - These bit locations match the contents of the corresponding bits of the CMD register of the node that initiated the interrupt. Since in the CMD register these bits dictate which level this interrupt is to be, they should read as ***01*** in the IFR1 register, ***10*** in the IFR2 register and ***11*** in the IFR3 register. Any other bit patterns would indicate that the interrupt FIFO is actually empty or the interrupt circuitry has malfunctioned.

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Interrupt Data Registers (IDR1, IDR2, IDR3)

The IDR1, IDR2, and IDR3 registers are 16-bit subsections of the receiver interrupt FIFOs. They are used to pass 16 user defined data bits from the CMDD0 and CMDD1 registers of interrupt initiating node to the receiving node's interrupt FIFO. The IDRx registers can be read as two separate bytes or as a 16-bit word. Furthermore, they can be read as the most significant 16 bits of a Lword when read in conjunction with the Sender ID and IFRx registers.

Table 3-22 Interrupt Data Registers Bit Map

Interrupt Data Register 1 (IDR1): Relative Offset $1A and $1B Read-Only, Byte/Word/Lword							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
User Data							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data							

Interrupt Data Register 2 (IDR2): Relative Offset $1E and $1F Read-Only, Byte/Word/Lword							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
User Data							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data							

Interrupt Data Register 3 (IDR3): Relative Offset $22 and $23 Read-Only, Byte/Word/Lword							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
User Data							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
User Data							

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DMA Start Address Register (DADD)

This register is initialized with the internal address pointer for DMA transfers. Once loaded it will count every DMA transfer.

Register Name:	DMA Start Address
Address Offset:	24h
Powerup Value:	000000h
Attribute:	Write Only
Size:	26 bits

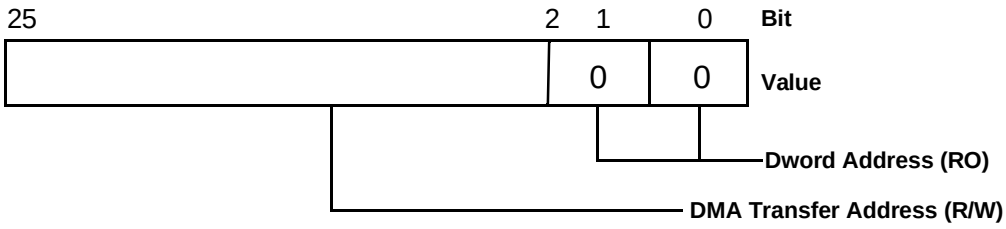


Figure 3-16 DMA Start Address Register

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Extended Control and Status Register Set

In the relative offset range of $28 through $3F, the VMIPCI-5579 contains a series of control and status registers which are used to access the extended features not present on the VMIxxx-5588 series boards. To the extent possible, the original register set in the relative offset $00 through $27 is the same as the VMIPCI-5588. This approach allows the user to substitute a VMIPCI-5579 for a VMIPCI-5588 with little or no software impact.

Two of the extended registers have many bit functions that are redundant to their original register counter parts. Only those bit functions necessary to access the extended features were changed. The Extended Interrupt Status Register (EIS) is similar to the Interrupt and Receiver Status Register (IRS) and the Extended Control and Status Register 3 is similar to the Control and Status Register 3 (CSR3).

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Extended Interrupt Status (EIS) Register

The Extended Interrupt Status Register contains eight separate secondary tier conditions that can cause a PCI interrupt to the host, provided the appropriate bits in the Interrupt Control and Status Register (ICSR) are set. Normally, a host interrupt service routine accesses this register to determine the cause of the PCI interrupt. This register is functionally the same as the original IRS register (offset $08) except bit 7 changed from *RCVR SYNC'D Low* to *Reserved* and bit 6 changed from *Latched SYNC Loss* to *Bad RCVR FIFO Cycle*.

Table 3-23 Extended Interrupt Status Register Bit Map

Extended Interrupt Status (EIS): Offset $28, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved	Bad RCVR FIFO Cycle	Bad Data Received	RCVR FIFO Half-Full Low	Reset Node Received	INT3 Pending	INT2 Pending	INT1 Pending

Extended Interrupt Status Register Bit Definitions

Bit 7: **Reserved** - This bit is currently reserved, and should not be used.

Bit 6: **Bad RCVR FIFO Cycle** - A one (1) in the bit location indicates that bad data has occurred due to an error in the receiver FIFO operation rather than an error in data at the receiver. Bit 6 is read-only. Like the original Bad Data bit 5 convention, any bad data due to receiver FIFO operation shall also be removed from the network. Bit 6 is cleared when bit 5 (Bad Data Received) is cleared by writing bit 5 to zero (0). It's designed this way so that existing VMIPCI-5588 software will still clear the fault even though it will not distinguish between bad data from the receiver or FIFO.

Bit 5: **Bad Data Received** - A one (1) in this bit location indicates that bad data was detected and removed by the receiver circuitry. Once set, this bit will remain set until it is cleared by writing a zero (0) to this bit location.

Bit 4: **RCVR FIFO Half-Full Low** - A one (1) in this bit location indicates that the receiver FIFO has reached or exceeded the half-full point at least once. Once set to one by the receiver half-full condition, it remains a one until cleared by writing a zero (0) to this bit location.(See Note below)

Note

Unlike the VMIxxx-5588 when this bit is set to one (1) by the assertion of the receiver FIFO half-full signal, it remains one (1) until overwritten by the host (just like bad data or reset node bits). Therefore, if a momentary assertion of receiver FIFO causes a PCI interrupt, the host has a way of determining the cause.

Bit 3: **Reset Node Received** - A one (1) in this bit location indicates that the board has received a Reset Node Command form the network. This bit is cleared by writing a zero (0) to this bit location in the register. In compliance with the PCI specification, the host must perform the actual reset function. This bit is only an indicator.

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Bit 2: **INT3 Pending** - A one (1) in this bit location indicates that at least one level 3 interrupt has been received (the receiver interrupt FIFO in not empty). Writes to this bit location have no effect (immediate status only).

Bit 1: **INT2 Pending** - A one (1) in this bit location indicates that at least one level 2 interrupt has been received (the receiver interrupt FIFO is not empty). Writes to this bit location have no effect (immediate status only).

Bit 0: **INT1 Pending** - A one (1) in this bit location indicates that at least one level 1 interrupt has been received (the receiver interrupt FIFO is not empty). Writes to this bit location have no effect (immediate status only).

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Extended Control and Status Register 3 (ECSR3)

The Extended Control and Status Register 3 is similar to the original CSR3 register, except the bit function of bits 7 through 3 have been modified to represent the extended address range of the VMIPCI-5579.

Table 3-24 Extended Control and Status Register 3 Bit Map

Extended Control and Status Register 3 (ECSR3): Offset $29, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CONFIG 3	CONFIG 2	CONFIG 1	CONFIG 0	Reserved	Endian Control EC2	Endian Control EC1	Endian Control EC0

Extended Control and Status Register 3 Bit Definitions

Bits 7 through 4: **CONFIG[3:0]** - These bits indicate the memory configuration of the board as defined by the table below. These bits are read-only.

Table 3-25 Memory Configuration

CONFIG[3..0]	MEM Size	CONFIG[3..0]	MEM Size
0000	256 Kbyte (not used)	1000	32 Mbyte
0001	512 Kbyte (not used)	1001	64 Mbyte
0010	1 Mbyte (not used)	1010	Reserved
0011	2 Mbyte (not used)	1011	Reserved
0100	4 Mbyte (not used)	1100	Reserved
0101	8 Mbyte (not used)	1101	Reserved
0110	16 Mbyte (not used)	1110	Reserved
0111	No Memory	1111	Reserved

Bit 3: **Reserved** - This bit is currently reserved, and should not be used.

Bits 2 through 0: **Endian Control[2:0]** - These three bits select the endian conversion that is applied to the data as it is transferred between the PCI bus host and the memory (and the network). Several conversion options are provided to accommodate both big-endian and little-endian host architectures with various data word sizes. Bits 2, 1, and 0 of the Extended Control and Status Register are a redundant way of accessing the same three flip flops controlled by bits 2, 1, and 0 of the CSR3 register. Changing these bits in either register will give the same results and changing these bits in either register will change the corresponding bits in the other register. Table 3-26 on page 80 defines the type of endian conversion that are applied.

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Table 3-26 Endian Conversion Modes

EC[2..0] States	Endian Conversion Applied
000	No Swap, straight through (*Default*)
100	Byte Swap
101	Word Swap
110	Byte and Word Swap
111	Swap on Size
Note: All other values are illegal, and are not used.	

The Endian Conversion mode swap on size reacts to the data based on its size and follows the Convention:

1. If the data is a Lword (32 bits) then swap the bytes and words.
2. If the data is a Word (16 bits) then swap the bytes.
3. If the data is a Byte (8 bits) then do not swap.

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Manual Interrupt Control and Status Register (MICS)

The MICS register is only used to control the green LED “A” on the VMIPCI-5579.

Table 3-27 Manual Interrupt Control and Status Register’s Bit Map

Manual Interrupt Control and Status Register (MICS): Offset $2A, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved			Green LED Status	Reserved			

Manual Interrupt Control and Status Register Bit Definitions

Bits 7 through 5, and 3 through 0:Reserved - These bits are currently reserved and should not be used.

Bit 4: **Green LED (Status)** - This is a user defined LED, 1 = ON, 0 = OFF

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Memory Access Control Register (MACR)

The Memory Access Control Register is used to enable or disable three modes of memory access. The ***Disconnect Mode*** and the ***Monitor Mode*** are intended for diagnostic testing. While in the ***Disconnect Mode***, the PCI bus host can write and read to the on-board RAM without generating data packets on the network. Likewise, data packets from other nodes can pass through this board without effecting the on-board memory.

While in the ***Monitor Mode***, the PCI host is neither able to write to the on-board RAM nor able to initiate a data packet to other nodes. Access to the on-board RAM by other nodes is not effected. The host is only able to monitor network activity by reading the on-board RAM.

Table 3-28 Memory Access Control Register Bit Map

Memory Access Control Register (MACR): Offset $2D, Read/Write, Byte							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Key Bit 7	Key Bit 6	Key Bit 5	Key Bit 4	Loop_EN	Disconnect Mode ENA	Monitor Mode ENA	Reserved

Memory Access Control Register Bit Definitions

Bits 7 through 4: **Key Bit[7:4]** - The key bits 7 through 4 must be written with the key pattern $A to enable any access mode. The key bits 7 through 4 must be written with the key pattern $C to disable any access mode. Writing to the MACR register with any other bit pattern in the key bits will have no effect. This implementation reduces the likelihood of inadvertent writes placing this board in an undesired access mode. The key bits are write-only.

Bit 3: **Loop_EN** - When this bit is set the Signal Detect (S.D) signal is not used, and the signal is looped back on itself. This is used to test the Hot Link chipset. The key pattern must be used to access this bit.

Bit 2: **Disconnect Mode Enable** - Writing a one (1) to this bit location in addition to the key pattern $A in the key bits will enable the Disconnect Mode. Writing a zero (0) to this bit location in addition to the key bit pattern $C in the key bits will disable the Disconnect Mode.

Bit 1: **Monitor Mode Enable** - Writing a one (1) to this bit location in addition to the key pattern $A in the key bits will enable the Monitor Mode. Writing a zero (0) to this bit location in addition to the key bit pattern $C in the key bits will disable the Monitor Mode.

Bit 0: **Reserved** - This bit is currently reserved, and should not be used. Write to a zero (0).

Note

Bits 2 and 1 can be read by the PCI host to verify the current memory access mode(s).

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Using Interrupts

Due to the architecture of the VMIPCI-5579 board, the interrupts are enabled and handled in a tiered fashion. The PCI interface chip is used to generate the PCI interrupts and other logic is used to tell the PCI interface chip when and what to do. The control registers in the PCI interface chip are different from the main board control registers. Therefore, both PCI I/O and memory accesses are required to use interrupts. The proper sequence of events is outlined below:

Enabling Interrupts

1. Select what sources can enable interrupts and enable the interrupt process by writing to the ICSR (memory base + $14) as outlined in the programming section (for example, 43 would enable interrupts for INT1 or INT2 pending). If the manual interrupt is used, the MICS register must also be written.
2. Enable the PCI Interface Chip by writing H"0000:1000" to the PCI INTCSR control register (I/O base + $38).

Disabling Interrupts

To disable both primary and secondary interrupts disable the PCI Interface Chip from generating interrupts by writing H"0000:0000" to the PCI Interface Chip Control register. To disable only the secondary tier interrupts write a zero (0) to bit 6, Global Interrupt Enable, of the ICSR.

Servicing Secondary Tier Interrupts

1. To verify the PCI interrupt, the PCI Interface Chip INTCSR will have bit 17 set to a (logical one) (optional); if a secondary tier source is the cause. Bit 17 is the Incoming Mailbox Interrupt.
2. Read PCI I/F (I/O base + $10) and discard data - this clears the cause of the interrupt. The Incoming Mailbox register is located at I/O base + $10
3. A write to the PCI Interface Chip's INTCSR with a H"0002:0000" will clear the interrupt off the PCI bus. Bit 17 is set when the interrupt is generated by the board's secondary tier of sources.
4. To determine the cause of the PCI interrupt, read either the IRS register (relative offset $08) or the EIS register (relative offset $28). The EIS should be used if any extended features are activated. In addition, if the manual interrupt is used, the MICS register (relative offset $2A should be read). It is possible for multiple events to occur while an interrupt is being generated and as such multiple flags could be set.
5. The act of reading the ISR register or EIS register does not clear any interrupt flags. However, writing a zero (0) to the ISR or EIS register will clear all the interrupt flags in bit positions 7 through 3 but will not clear the interrupt flags in bit positions 2, 1 or 0. The EIS or ISR bit positions 2, 1, and 0 correspond to the INT3 pending, INT2 pending, and INT1 pending. Each of these network interrupts flags is cleared by reading the associated Sender ID register until the receiver interrupt FIFO is emptied. Alternatively, the act of writing any value to

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a Sender ID register will reset the associated receiver interrupt FIFO, and clear the pending flag in the ISR or EIS registers.

6. To re-arm the interrupts, write to the ICSR register (relative offset $14) a data pattern in which the desired individual enables are set to one (1), plus the Global Enable in bit position 6 is set to one (1). If any interrupts are still pending, as indicated by the IRS register or the EIS register, re-arming the interrupt enables will immediately result in an new PCI interrupt once the PCI Interface Chip is also re-armed. Each time a PCI interrupt is generated, the Global Enable in bit position 6, is automatically reset to zero to allow only one PCI interrupt to occur. Global Enable must be re-written to a one (1) to allow an additional PCI interrupt.
7. The PCI Interface Chip must be rearmed by writing H"0000:1000" to the INTCSR.

Generating Interrupts on Other Nodes

To generate an interrupt on the local bus of another node, the local bus interrupt enable(s) must first be set by the host of that node. If the other node is a VMIPCI-5579, this is done through the other node's ICSR register and PCI Interface Chip (INTCSR) register. (See the previous section titled "*Using Interrupts*".) Regardless of whether the local bus interrupt of the other node is enabled, each node can store a network interrupt in the receiver interrupt FIFO of the other node and a pending interrupt flag in the other node will be asserted. If the other node is of the type VMIxxx-5588, the only information that can be stored in the interrupt FIFO of that node is the Sender ID (that is... the node ID of the node issuing the interrupt). If, however, the other node is of the type VMIxxx-5579, three flag bits, and up to 25 bits of data can be stored in the interrupt FIFO in addition to the Sender ID.

Example 1: The destination node is of the type VMIxx-5579, and its node ID is $20. The node ID of this node is $A0. The desired interrupt level is INT3, and the interrupt is to be received by that node alone. In addition to the Sender ID, the data pattern $55 is to be stored in the destination node's interrupt FIFO.

The steps to perform to issue the interrupt are:

1. Perform a byte write of data $20 (destination node ID) to the CMDN registers at relative offset $10.
2. Perform a word write of data $5503 to the CMD and CMDD0 registers starting at relative offset $11.

If performed separately, the Command Node (CMDN) write must proceed the Command (CMD) write or the interrupt will be issued to the wrong node. Alternatively, the above two steps can be performed with a single Lword write of data $00550320 to relative offset $10

At the destination node the interrupt service routine can perform the following steps to service the interrupt:

1. Perform a byte read of the EIS register at relative offset $28 and get the binary data of XXXXX1XX where for this example "X" bits are don't care. The "1" in bit 2 indicates the INT3 is pending and its FIFO is not empty.
2. Perform a word read of IDR3 register at relative offset $22 and get the data

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pattern $0055, which is the sender's user defined data.

3. Perform a byte read of the Interrupt Flag Register 3 (IFR3) at relative offset $21 and get the data pattern $03, which indicates a non-global level 3 interrupt.
4. Perform a byte read of the Interrupt Sender ID 3(INT3) register at relative offset $20 and get the data pattern $A0, which is the senders node ID.

If read separately, the IDR3 and IFR3 registers must be read before the SID3 register or the resulting data would be invalid. Alternatively, steps 2, 3, and 4 can be performed as a single Lword read of relative offset $20.

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DMA Features

The VMIPCI-5579 can be set-up as a DMA Initiator on the PCI bus. This feature is initialized by another PCI Initiator, who wishes to offload the process of moving blocks of data to or from the VMIPCI-5579 to another memory location. This is very useful for moving large blocks of data to or from system memory, and relieving the processor from this time consuming activity. The VMIPCI-5579 can move data blocks up to 1 Mbyte at burst rates over 22 Mbyte/s. Large blocks of data are broken into smaller blocks by the VMIPCI-5579 so that the PCI bus is not monopolized. The VMIPCI-5579 will request the PCI bus when it needs to move data. The period of time, in PCI clock cycles, that the VMIPCI-5579 will use the bus once the bus is granted is programmable. The VMIPCI-5579 will move as much data as possible during this time, and then relinquish the bus, and request the bus again if more data needs to be moved. The VMIPCI-5579 can be configured to generate a PCI interrupt upon completion of a DMA cycle, or the board can be polled to see if the DMA process is complete, or how many more bytes are remaining to be transferred. The VMIPCI-5579 PCI interface contains FIFOs that are utilized during the DMA process to quicken the data transfer. During a DMA write, these FlFOs are being filled even before the VMIPCI-5579 is granted the bus. This allows some burst to be at the maximum PCI data rate of 132 Mbyte/s, but only about ten Lwords (40 bytes). For a 33 MHz host PCI bus, the maximum sustained rate can drop to 22 Mbytes/s for longer burst. During DMA reads, these FlFOs can be filled at the maximum of 132 Mbyte/s but, once filled, the data rate will be slowed to 22 Mbyte/s. The 22 Mbyte/s will be further throttled to 13.4 Mbyte once the Reflective Memory transmit FIFOs are filled. An illustration of the DMA data path is shown in Figure 3-17 below.

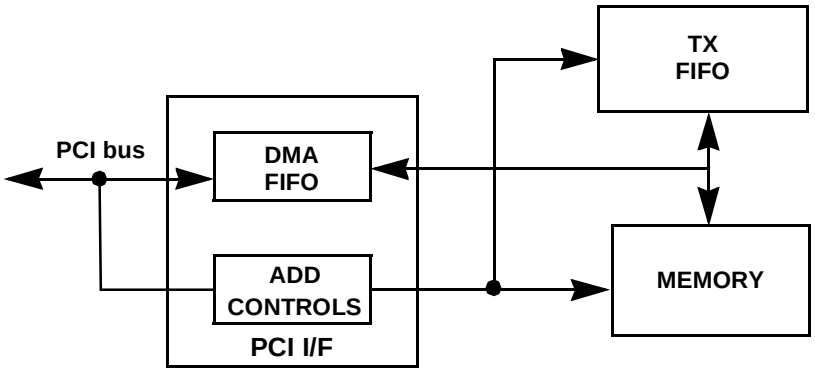


Figure 3-17 DMA Data Path

DMA Write Procedure

The following is the procedure that must be followed to perform DMA Writes (from the VMIPCI-5579 to a PCI target device):

1. Clear PCI I/F DMA Write FIFO, I/O write to offset $3C with value $04000000.
2. Initialize Target address, I/O write to offset $24 the target address (R/W 32-bit).
3. Initialize Transfer Byte Count, I/O Write to offset $28 total bytes (R/W 32-bit).

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4. Initialize VMIPCI-5579 Initiator address, Memory-Mapped Control Register at offset $24.
5. Enable the VMIPCI-5579 DMA Write bit, Memory-Mapped CSR1 bit 3.
6. Enable VMIPCI-5579 PCI bus Master, I/O Write long to offset $3C value of $400.
7. After DMA cycle is complete, disable bus mastership, offset $3C value of $0.
8. Disable internal DMA control CSR1 bit 3.

Example DMA Write

The DMA Write procedure is done by following the instructions to perform a DMA write from a VMIPCI-5579 to system memory. The VMIPCI-5579 board is mapped at $F000 0000 for memory and $6100 for I/O. The following procedure will move 40(H) bytes, 10(H) Lwords from the block $F000 0040 to $F000 007C to the block $100000 to $10003C.

1. IWL 613C 04000000 ;Clear DMA FIFO
2. IWL 6124 100000 ;Initialize Target Address
3. IWL 6128 40 ;Initialize Transfer Byte Count
4. MWL F0000024 F0000040 ;Initialize Initiator Address
5. MWB F0000009 8 ;Enable VMIPCI-5579 capability
6. IWL 613C 400 ;Enable VMIPCI-5579 to become PCI Initiator
7. IRL 6128 ;Poll to verify the DMA process is complete
   = 0 ;(Interrupts can also flag the DMA termination)
   IWL 613C 0 ;Disable VMIPCI-5579 from requesting bus
8. MWB F0000009 0 ;Disable internal DMA data movement.

DMA Read Procedure

The following is the procedure that must be followed to perform a DMA Read (from the PCI target Device to the VMIPCI-5579):

1. Clear DMA FIFO, I/O Write to offset $3C value $02000000.
2. Initialize Target address, I/O Write to offset $2C the target address (R/W 32-bit).
3. Initialize Transfer Byte Count, I/O Write to offset $30 total bytes (R/W 32-bit).
4. Initialize VMIPCI-5579 Initiator address, Memory-Mapped Control Register at offset $24.
5. Enable the VMIPCI-5579 DMA Read bit, Memory-Mapped CSR1 bit 1.
6. Enable VMIPCI-5579 PCI bus Master, I/O Write long to offset $3C value of $4000.
7. After DMA cycle is complete, disable bus mastership, offset $3C value of $0.
8. After DMA cycle is complete, disable internal movements by clearing CSR1 bit 1.

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Example DMA Read

The DMA Read procedure is done by following the instructions to perform a DMA read from system memory to a VMIPCI-5579. The VMIPCI-5579 board is mapped at $F000 0000 for memory, and $6100 for I/O. The following procedure will move 40(H) bytes, 10(H) Lwords from the block $100000 to $10003C to the VMIPCI-5579 at the block $F000 0040 to $F000 007C.

1. IWL 613C 02000000 ;Clear DMA FIFO
2. IWL 612C 100000 ;Initialize Target Address
3. IWL 6130 40 ;Initialize Transfer Byte Count
4. MWL F0000024 F0000040 ;Initialize Initiator Address
5. MWB F0000009 2 ;Enable VMIPCI-5579 DMA capability
6. IWL 613C 4000 ;Enable VMIPCI-5579 to become PCI Initiator
   IRL 6130 ;Poll to verify the DMA process is complete
   = 0 ;(Interrupts can also flag the DMA termination)
   IRL 613C ;Make sure internal data movements are complete
   bit 2 = 1
7. IWL 613C 0 ;Disable VMIPCI-5579 from requesting bus
8. MWB F0000009 0 ;Disable internal DMA movements.

DMA Interrupts

The VMIPCI-5579 can generate a PCI interrupt upon completion of a DMA transfer. The procedure is slightly different for reads and writes, but it is generally the same. The I/O mapped register INTCSR at offset $38 is used to enable interrupts. This is the same register that is used by other Reflective Memory interrupts. A method to determine why the interrupt has occurred is also in this register. The bit map for this register is below.

Bit 23	Interrupt Asserted	(From any cause, Read Only)
Bit 21	Target Abort	(A Target Abort occurred while VMIPCI-5579 was Initiator)
Bit 20	Master Abort	(A Master Abort occurred while VMIPCI-5579 was Initiator)
Bit 19	DMA Read Complete	(Offset $30 = 0, end of DMA read cycle)
Bit 18	DMA Write Complete	(Offset $28 = 0, end of DMA write cycle)
Bit 17	Mailbox Int	(Standard Reflective Memory interrupt pending)

Bits 17- 21 Read/Write One to Clear type.

Bit 15 Interrupt on Read Transfer Complete Enable (enable set to 1)

Bit 14 Interrupt on Write Transfer Complete Enable (enable set to 1)

Bit 12 Interrupt on Incoming Mailbox Enable (enable set to 1)

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To arm the interrupts for use with the DMA procedure, the transfer count must first be loaded into the appropriate register before the interrupt is enabled. This would normally be done immediately before the VMIPCI-5579 is enabled to become a PCI initiator (refer to step 5 in the procedures section).

DMA Restrictions

The following restrictions apply to VMIPCI-5579 DMA activities. There are no restrictions on target accesses while the VMIPCI-5579 is enabled as a PCI Initiator in DMA mode.

1. All DMA cycles move 32-bit wide data words.
2. The maximum byte transfer count is 16 Mbyte.
3. The DMA capability can be used for both DMA reads and DMA writes, but not both simultaneously. The user should only enable one at a time in the control registers.
4. Data rates: The VMIPCI-5579 can do a DMA read at rates of 132 Mbyte/s maximum and 24 Mbyte/s sustained. This data rate will be further throttled down to the 13.4 Mbyte/s, the Reflective Memory network speed, after the transmit FIFOs are full. This allows all data written to the board to be broadcast out on the Reflective Memory network. This ensures no data will be lost.
5. To abort any DMA process, the transfer count should be written to four (4) so that the PCI I/F will terminate normally after the next transfer. This is due to an errata in the PCI I/F.

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Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

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Maintenance Prints

User level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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Troubleshooting Hints

The following pages list problems you can have when using the VMIPCI-5579. The list also contains the possible causes and solutions for those problems.

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SYMPTOM	POSSIBLE CAUSES
Communications lost after power down of one or more nodes on the link.	1) The VMIPCI-5579 is a ring architecture network and all data must be repeated at each node. If a node is powered down, the ring is opened at that point. The fiber-optic cable may be moved to complete the ring again or a fiber-optic bypass switch may be used to automatically complete the ring.
Data written to one node does not appear in other nodes.	1) The VMIPCI-5579 is available in several memory size options. In addition, the control register offset can add an offset to any relative address on the network. Either or both of the above conditions can result in memory accesses outside a board's actual memory space. 2) The sending node ID is the same as another node on the ring. Each node must have a unique node ID, otherwise data originated on one node will be removed by the other node of the same ID. 3) Open or defective connection to fiber-optic cable. 4) Defective FIFO module on either receiving node or transmitting node (the bad board may be found by checking memory on other nodes to see if they received data correctly). 5) Mixed nodes on the link (redundant and single transfer nodes on link). All nodes must be in either redundant or single transmission mode. 6) Multiple Rouge Packet Masters with same RP control number (i.e.,. two or more boards in the ring with the same jumper removed.)

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SYMPTOM	POSSIBLE CAUSES
Data is wrong in one node and is correct in all other nodes.	1) Possible write to same memory location in two or more boards (in separate nodes) at the same time (this must be prevented in software). 2) Damaged local node.
Fiber-optic errors commonly seen on local node.	1) Defective fiber-optic cable. It may have insufficient length-bandwidth or simply be broken. Light loss error budget has been exceeded. 2) Damaged fiber-optic transmitter or receiver. 3) Damaged node on ring (if parity errors are seen on a node, the failing node is either the local node or the node sending data to the local node).

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