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V469 Single Board Computer
"Patriot"

Ultra High Performance, Single Slot, Dual Redundant, Pentium® M VME Server



User's Manual

Revision B

July 10, 2007

General Micro Systems, Inc.

"Redefining Embedded Real-Time Computer Design"
Since 1979

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1. USER INFORMATION

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CAUTION !

Always use proper Electrostatic Discharge (ESD) protection when handling printed circuit boards to avoid seriously damaging components.

Product handlers must always be properly grounded.

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- National Semiconductor is a registered trademark of National Semiconductor Corporation.
- Texas Instruments is a registered trademark of Texas Instruments Corporation.
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This General Micro Systems Embedded Module product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, General Micro Systems will at its discretion decide to repair or replace defective products.

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The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

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Before contacting General Micro Systems Embedded Modules technical support please consult our Website at **www.gms4sbc.com** for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone at (800) 307-4863 or (909) 980-4863 Extension 206, or Email **fae@gms4sbc.com**.

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1.8.1 Product Repairs

RMA Information

To expedite assistance for problems, be able to provide the following information:

- Your name, Phone number, Company, Division and City.
- Product with which you are having trouble.
- Serial Number and Revision (located on the board).
- Operating system you are running.
- Last software used.
- Detailed description of your problem and any error messages that have appeared on the screen.

Depending on the circumstances of the problem, it may be deemed necessary to return the products to General Micro Systems (GMS) for repair. In order to return the product for repair, the following step is necessary:

1. Obtain a Return Material Authorization Number (RMA#) from GMS Customer Service via the GMS website or phone.

Obtaining an RMA Number

To obtain a product RMA number, you should call our Customer Service department through our main number or the numbers previously mentioned in this manual.

Shipping the Product

Any product returned to GMS should be in its original shipping carton if possible. Otherwise, the product should be carefully packaged in a conductive packing material and placed in a cushioned corrugated carton suitable for shipping. Please mark the shipping label with the RMA number and return it to:

Customer Service Department
ATT: RMA# (*put RMA number here*)
General Micro Systems
8358 Maple Place,
Rancho Cucamonga, Ca
91730 USA

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Providing a Product Defect Report

When you are returning a product for repair, it is very important to include a written report that details the nature of the problem in order to expedite the repair. Ensure the following information is included:

- RMA Number.
- Product.
- Serial Number.
- Contact.
- Phone Number.
- Description of the Problem/Defect using standard terminology (i.e. port not working etc).

Warranty Repairs

Any product returned and found to be under warranty will be repaired or replaced at the discretion of GMS.

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2. TABLE OF CONTENTS

1. USER INFORMATION 2
1.1 Thank You 2
1.2 Unpacking and Handling 2
1.3 Copyright 3
1.4 About This Manual 3
1.5 Trademark Acknowledgement 3
1.6 Standards 4
1.7 Warranty Information 4
1.8 Technical Support 4
1.8.1 Product Repairs 5
2. TABLE OF CONTENTS 7
3. FIGURES 10
4. LIST OF TABLES 11
5. PRODUCT INFORMATION 13
5.1 Highlights 13
5.2 Functional Description 15
6. BLOCK DIAGRAM 18
7. FEATURES and SPECIFICATIONS 19
7.1 Features 19
7.2 Mechanical Specifications 24
7.2.1 Dimensions 24
7.3 Electrical Specifications 24
7.3.1 Power Consumption 24
7.4 Environmental Specifications 25
7.4.1 Air Flow 26
8. MAJOR COMPONENTS 27
8.1 CPU 27
8.2 Server-Works™ CMIC-LE Bridge 28
8.3 Server-Works™ C10B-X2 Dual PCI-X 30
8.4 Server-Works™ CSB5 South Bridge 30
8.5 Tundra® (CA91C142) PCI to VME Bridge 31
8.6 Intel® (82559ER) Ethernet Controller 32
8.6 Intel® (82546GB) Dual Port Gigabit Ethernet Controller 32
8.8 TI (1394b) High Performance Link Layer Controller 33

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8.9 TI (TSB81BA3) IEEE P1394b S800 Three-Port Cable Transceiver/Arbiter 34
8.10 EXAR (ST16C2550) Dual UART with 16-Byte Transmit and Receive FIFOs 35
8.11 NEC (PD720101) USB 2.0 Host Controller 36
8.12 ATI Technologies Mobility Radeon™ 9000 Graphics Controller 37
8.13 National Semiconductor® PC87417 LPC Servo Ultra I/O 39
8.14 LSI (53C1020) Ultra320 SCSI Controller 40
8.15 M-Systems (MD2811) Disk-On-Chip 42
8.16 National Semiconductor® (LM81) Microprocessor System Monitor 43
8.17 MAXIM (MAX1617) Temperature Sensor 44
8.18 Atmel® (AT93C46/AT93C66), 3-Wire Serial CMOS EEPROM 45
8.19 Atmel® (AT24C256) 2-Wire Serial EEPROM 46
8.20 Atmel® (AT24C16) Serial EEPROM 47
8.21 Intersil™ (ISL6115CB) Controller 48
8.22 Micrel (MIC2505-2) Power Switch 49
8.23 Transpower Technologies (RJ-714-CL2) 10/100 Magnetics 49
8.24 St Microelectronics (M29W040B) 4 Mbit Flash Memory 50
8.25 St Microelectronics (M29W400BT) 4 Mbit Flash Memory 50
8.26 LSI Logic (LSI FC 929 X) Fibre Channel Controller 51
8.27 Intersil™ (ISL6520) Single Synchronous Buck PW Modulation Controller 52
8.28 Serial Ports 53
8.29 Keyboard and Mouse 53
8.30 3-Volt Lithium Battery 53
8.31 Power Distribution 54
8.32 Heatsinks 55
APPENDIX A 56
A.1 Front Panel 56
A.2 Connector Pin Assignments 57
APPENDIX B 85
B.1 Rear Transition Module 85
B.2 Rear Transition Module Pin Assignments 87
APPENDIX C 96
C.1 Default Jumper Settings 96
APPENDIX D 97
D.1 POST/Status LEDs 97
D.2 LED Description and Procedures 99
D.3 Ethernet Default Configuration and Ethernet VITA41 Configuration 101
D.4. BIOS 102

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

D.4.1 Bootblock Initialization Code Checkpoints 102
D.4.2 Bootblock Recovery Code Checkpoints 103
D.4.3 POST Code Checkpoints 104
D.4.4 DIM Code Checkpoints 106
D.4.5 ACPI Runtime Checkpoints 107
APPENDIX E 108
E.1 Installing Operating Systems using Fibre Channel 108
APPENDIX F 109
F.1 Making Hardware Upgrades or Changes – General Procedure 109
APPENDIX G 110
G.1 Document – Revision History 110

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3. FIGURES

Figure 1. V469 Single Board Computer (Top) 13
Figure 2. V469 Single Board Computer (With Memory) 14
Figure 3. V469 Block Diagram 18
Figure 4. Two Way Multiprocessing Server Configuration 29
Figure 5. PC87417 Advanced I/O Block Diagram 39
Figure 6. LSI 53C1020 Implementation Block Diagram 41
Figure 7. Power Distribution Block Diagram 54
Figure 8. Passive Processor Heatsink Top/Side View 55
Figure 9. Passive North Bridge (BGA) Heatsink Top/Side View 55
Figure 10. V469 SBC Front Panel 56
Figure 11. Rear Transition Module 85
Figure 12. Rear Transition Module Block Diagram 86
Figure 13. Rear Transition Module Front Panel 86
Figure 14. POST/STATUS A and B LEDs (on Front Panel) 98
Figure 15. Ethernet Default Configuration 101
Figure 16. Ethernet VITA41 Configuration 101

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4. LIST OF TABLES

Table A.1. A-USB2 Connector J5 Pin Assignments 57
Table A.2. A-SAM-3 Expansion Bus Connector J6 Pin Assignments 58
Table A.3. B-USB2 Connector J7 Pin Assignments 59
Table A.4. A-ENET1 RJ-45 Connector J8 Pin Assignments 60
Table A.5. A-USB1 Connector J10 Pin Assignments 61
Table A.6. B-USB1 Connector J11 Pin Assignments 61
Table A.7. Programming Header Connector J12 Pin Assignments 62
Table A.8. A-VGA Connector J13 Pin Assignments 62
Table A.9. B-VGA Connector J14 Pin Assignments 63
Table A.10. A-COM1 RJ-45 Connector J15 Pin Assignments 63
Table A.11. A-DDR Module Connector J17 Part 1 of 3 Pin Assignments 64
Table A.11. A-DDR Module Connector J17 Part 2 of 3 Pin Assignments 65
Table A.11. A-DDR Module Connector J17 Part 3 of 3 Pin Assignments 66
Table A.12. A-DDR Module Connector J18 Part 1 of 3 Pin Assignments 67
Table A.12. A-DDR Module Connector J18 Part 2 of 3 Pin Assignments 68
Table A.12. A-DDR Module Connector J18 Part 3 of 3 Pin Assignments 69
Table A.13. B-DDR Module Connector J19 Part 1 of 3 Pin Assignments 70
Table A.13. B-DDR Module Connector J19 Part 2 of 3 Pin Assignments 71
Table A.13. B-DDR Module Connector J19 Part 3 of 3 Pin Assignments 72
Table A.14. B-DDR Module Connector J20 Part 1 of 3 Pin Assignments 73
Table A.14. B-DDR Module Connector J20 Part 2 of 3 Pin Assignments 74
Table A.14. B-DDR Module Connector J20 Part 3 of 3 Pin Assignments 75
Table A.15. A-IDE Connector J22 Pin Assignments 76
Table A.16. B-COM1 RJ-45 Connector J24 Pin Assignments 77
Table A.17. B-SAM-3 Expansion Bus Connector J25 Pin Assignments 78
Table A.18. A-ENET2 RJ-45 Connector J26 Pin Assignments 79
Table A.19. B-ENET2 RJ-45 Connector J27 Pin Assignments 79
Table A.20. B-IDE Connector J28 Pin Assignments 80
Table A.21. B-ENET1 RJ-45 Connector J29 Pin Assignments 81
Table A.22. VME P0 VITA 41.3 J23 Connector Pin Assignments 82
Table A.23. VME P1 Connector Pin Assignments 83
Table A.24. VME P2 Connector Pin Assignments 84
Table B.1. Rear Transition Module VME Connector J2 Pin Assignments 87
Table B.2. Rear Transition Module B-USB4 Connector J3 Pin Assignments 88

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Table B.3. Rear Transition Module BUSB3 Connector J4 Pin Assignments 88
Table B.4. Rear Transition Module B-COM2 (RJ-11C) Connector J5 Pin Assignments 89
Table B.5. Rear Transition Module A-USB4 Connector J6 Pin Assignments 89
Table B.6. Rear Transition Module A-USB3 Connector J7 Pin Assignments 90
Table B.7. Rear Transition Module A-COM2 (RJ-11C) Connector J8 Pin Assignments 90
Table B.8. Rear Transition Module B-IDE Connector J9 Pin Assignments 91
Table B.9. Rear Transition Module B-IDE Connector J10 Pin Assignments 92
Table B.10. Rear Transition Module A-IDE Connector J11 Pin Assignments 93
Table B.11. Rear Transition Module A-IDE Connector J12 Pin Assignments 94
Table B.12. Rear Transition Module PIM Jn4 Mezzanine User I/O Conn. J13 Pin Assign. 95
Table C.1. Default Jumper Settings 96
Table D.1. A-POST/Status LED Common Circuits 97
Table D.2. B-POST/Status LED Common Circuits 97
Table D.3. BIOS Bootblock Initialization Code Checkpoints 102
Table D.4. Bootblock Recovery Code Checkpoints 103
Table D.5. POST Code Checkpoints 105
Table D.6. DIM Code Checkpoints 106
Table D.7. ACPI Runtime Checkpoints 107
Table F.1. Hardware Upgrades or Changes 109
Table G.1. Document – Revision History 110

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5. PRODUCT INFORMATION

5.1 Highlights

The V469 “Patriot" (Figure 1) is a single slot (4HP) 6U VXS Single Board Computer (SBC) specifically designed to provide the ultimate server functionality in a VME card cage. This ultra high performance, low power requirement server is true dual processor architecture, with each processor sharing absolutely NOTHING with the other processor, as if they were in two different VME slots. The two processors are linked together with the Gigabit Ethernet or may be linked via VITA 41.3 VXS, thus providing a massive server density unlike ANY other technology. To provide even more processing power at lower power, the new dual core processors will be used (Q3-06) to provide QUAD-processing capabilities.

This ultimate processing power per VME site and per watt makes the Patriot an ideal solution for systems requiring massive parallel processing for intensive floating point/integer calculations. No other Pentium® or PowerPC® based SBC can match the performance and the low power consumption of the V469 for Mil/Aero and server applications.

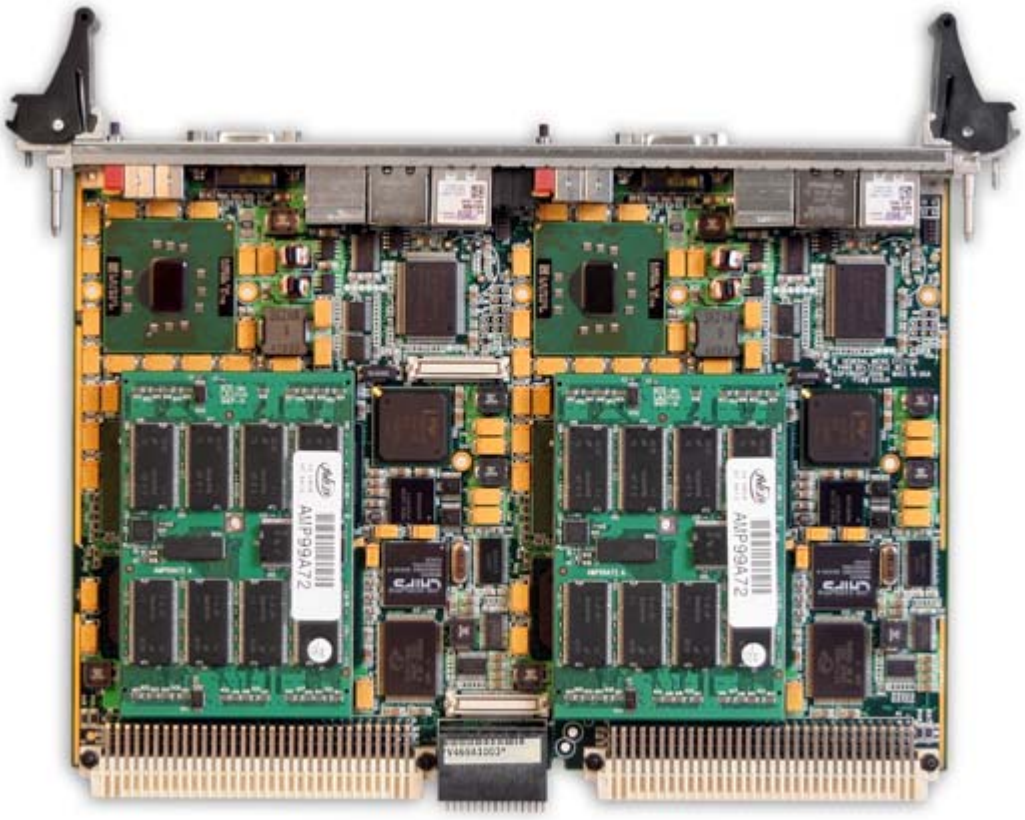


Figure 1. V469 Single Board Computer (Top)

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The V469 utilizes two of the new M-760 Pentium-M processors, each operating at 2.0-GHz with 2-MB of L2 Cache and 533-MHz FSB. Each processor is 100% decoupled from the other processor and they do not share any functions, including power supplies and I/O. Each Pentium® processor has it own memory and I/O controllers and they communicate with each other over Gigabit Ethernet port or via VME VITA 41.3 VXS. The two sides (Side A and B) are 100% identical including the mechanicals, thus all the inner-connects can be duplicated.

Note: The V469 SBC with memory is shown in Figure 2 below:



Figure 2. V469 Single Board Computer (With Memory)

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The V469 provides up to 8-GB of 266-MHz RDDR memory with ECC configured in **128-bit wide,** compared to the standard 64-bit wide, DDR 200-MHz of all other Pentium® M designs. This unique memory design of the Patriot supports the fastest DMA operations between the system memory and high-speed I/O devices. The onboard high-speed devices such as dual Gigabit Ethernet ports, Fibre Channel and the two PMC sites take full advantage of this added bandwidth and provide unmatched performance without any degradation when all I/O devices are used simultaneously.

Standard I/O functions of each side of Patriot included are: dual Gigabit Ethernet ports with Copper or Fiber interface, 2-Gbit, full duplex Fibre Channel with 2-MB of SRAM buffer and Flash BIOS to support Boot capabilities, quad USB 2.0, dual Serial ports, XVGA Video, UDMA IDE interface. An optional I/O interface module allows one Compact Flash and one USB-2.0 device to be added to each side. This Compact Flash may be used to Boot the Operating System or to store user data while the USB device may support 802.11b/g wireless Ethernet or any other USB functions.

For additional I/O functions, each side is connected to a Special Application Module (SAM-III™). This open architecture, interface provides the equivalent of dual 100-MHz, 64-bit PCI bus throughput. User may connect to this bus directly via FPGA or may utilize existing silicon to convert to dual PCI-X buses for user I/O functions. GMS plans for several I/O functions for this SAM-III™ interface, including dual PMC module. Consult factory for the latest offering.

5.2 Functional Description

Memory and System Architecture

Note: *Since the V469 is a true dual processor (A side and B Side), each function below is duplicated for both sides.*

To facilitate such incredible CPU performance and to guarantee that the memory and I/O devices have the full CPU bandwidth, which is an astounding 4.2 Gigabytes/s, tremendous attention was given to the systems architecture. The Patriot utilizes a Hub Technology for CPU bandwidth distribution. The CPU Front Side Bus (FSB), which operates at 533-MHz, is connected to a four port Hub. Three links of the Hub are capable of taking full advantage of the CPU performance.

The first link, Link-0 (see Block Diagram) is connected to a memory module via two high speed, high reliability connectors, which may be used to add up to 8-GB of ECC protected memory to each processor. This memory is configured as **128-bit wide and dual interleaved** to provide maximum performance, and it is field upgradeable module to take advantage of the highest density memory design while providing technical stability for rugged applications.

The second link, Link-1, provides the onboard I/O functions with dual PCI-X buses for high-speed system I/O devices. This link provides data transfers to/from the system memory at 3.2-GB/s ensure no bottleneck even when both PCI-X buses are active at the same time. This link is also used for system I/O functions on the baseboard.

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The third link, Link-2, is connected to the Special Application Module III, (SAM-III™) which is an expansion connector. SAM-III™ is a third generation I/O expansion bus from GMS, which was designed to provide ultra high speed (3.2-GB/s) I/O, without bottlenecking the onboard System I/O or memory. This bus is also connected to custom I/O or the optional dual PMC expansion module.

The fourth Link, Link-3, is a 266-MB/s bus which is used for the low speed I/O devices onboard. This balanced four-port Hub is the ultimate in memory and I/O performance and presents the user with the ability to architect systems, which until now, was not possible.

System I/O

Two independent PCI-X buses are provided on the Patriot for high speed I/O via Link-1. The first PCI-X bus is connected to the dual Gigabit Ethernet ports, while the other PCI-X is connected to a Fibre Channel port. This dual PCI-X design provides the best Gigabit and Fibre Channel performance possible. The Gigabit supports full TCP/IP Offloading Engine (TOE) and best Gigabit performance possible with very little CPU utilization. The Fibre channel provides up to 2-Gbit full duplex data transfers, and has a BIOS flash to support system boot. To further enhance the Fibre Channel performance a 2-MB of high speed SRAM is provided to buffer the data from the controller. This SRAM is Parity protected and used only by the Fibre Channel controller.

Link-2 of the Hub is connected to the Special Application Module (SAM-III™) Bus, which is used to add additional high-speed I/O devices to the Patriot module on the expansion module, which occupies 2nd VME slot. The SAM-III™ bus delivers over eight times the performance (3.2 GB/s) of a PMC expansion bus (533-MB/s @ 64-bit, 66-MHz) with fewer pins and a much simpler interface.

The Systems I/O functions are provided via Link-3 of the Hub. This link provides the system with a 33-MHz/32-bit PCI-bus, X-bus, LPC-bus, SMB-bus, and dual Ultra DMA-100 IDE buses. One of the IDE buses, along with LPC bus and one USB port are connected to the I/O expansion connector for additional onboard I/O; such as Compact Flash, Wireless Ethernet, Serial Ports etc. yet still occupying a single slot. The 2nd IDE bus and two USB ports are connected to VME P2. The low speed PCI-bus is connected to a USB 2.0 controller and to a XVGA video controller.

The supper I/O controller is connected to the LPC bus, provides 2-Serial ports, RTC and CMOS RAM. One of the Serial ports out of the super I/O is available at the front panel while the other Serial port is connected to rear I/O.

The X-bus is connected to a 512-KB Flash device. This Flash is used as the system BIOS device and also may be used to store user data.

The SMB-bus is used as an I^2C bus to configure system memory via the memory modules. Additionally, the I^2C bus is connected to a 2-Kbit of Serial EEPROM for VxWorks® Boot parameters or as an FRU device and to communicate with the system health monitors.

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Status and Alarms

The CPU and baseboard temperatures (for each side) along with all voltages are constantly monitored and may be read/set in BIOS. Alarms are provided to the Operating System/user application to alert when the critical level has been reached. AMI BIOS and Power-On-Self-Test (POST) or Built-In-Test (BIT) is standard with Extended BIT (EBIT) as optional to provide detail system testing. Two binary displays on the front panel indicate the status of each test performed upon power on. BIT diagnostic tests cover over 60% of the board's functions, while EBIT tests over 90% of the functionality of the Patriot. A Real Time Clock (RTC) with a field replaceable battery, four 32-bit timers, and a watchdog timer are all standard.

VXS Interface and Software Offering

The VXS interface for the V469 is provided via VITA 41.3 interface. This high speed Switched Gigabit Ethernet provides the ultimate backplane connectivity without the need for ANY custom I/O drivers. This technology also eliminates the Big Endian /Little Endian issues and fully supported under any OS which has TCP/IP support.

Air Flow

The V469 SBC may be plugged into any 5 rows VME card cage that has no P0 connector without the need for any modifications. Extensive attention has been given to the cooling which is supplied via a passive heat sink. This allows the Patriot to operate at up to 55^{o} C with a standard 400 LFM airflow. The V469 requires +5V, 3.3V and +/-12V.

Operating Systems

The Patriot is supported under Windows® /2000/XP, VxWorks®, Solaris® x86, QNX®, and Linux®. Board Support Packages (BSP) supports almost every function right out of the box. However, some custom drivers are required to take full advantage of all the I/O functions under VxWorks®, Linux®, and Solaris. Check with your local GMS representative to see which of the latest I/O drivers are either required or available.

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6. BLOCK DIAGRAM

A simplified perspective of the V469 Block Diagram is illustrated in Figure 3. The following subsections provide an overview of the Major Components comprising the V469 architecture. Zoom to 150% for clarity.

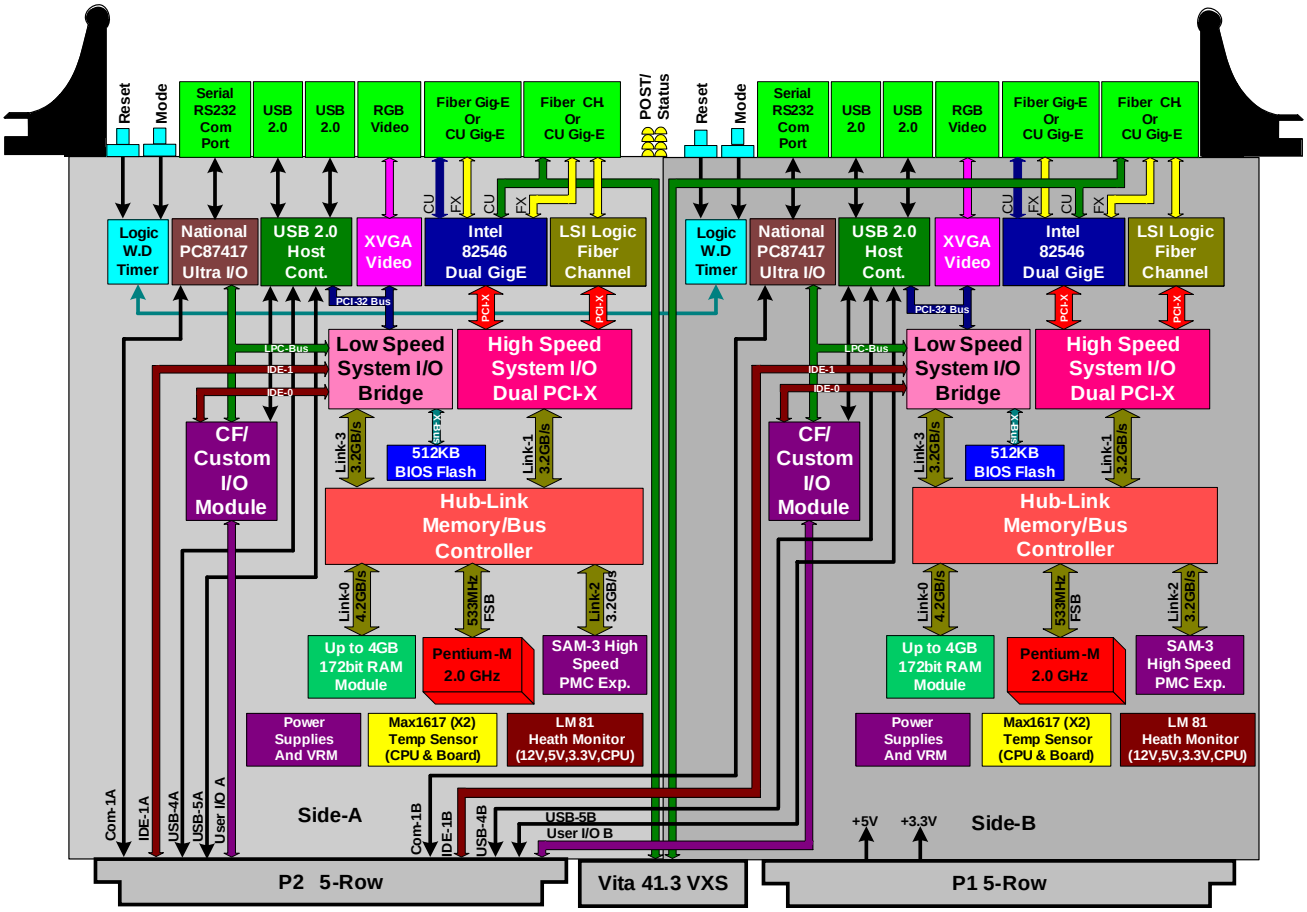


Figure 3. V469 Block Diagram

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7. FEATURES and SPECIFICATIONS

7.1 Features

- True Dual Redundant Server with 100% “Share Nothing”. Each server with:
- 2.0-GHz Pentium® M processor with 2-MB of L2 Cache.
- Up to 8-GB of ECC, RDDR-266 memory via upgradeable module.
- 533-MHz Front Side Bus (FSB), with two independent PCI-X busses.
- Dual GigE ports with TCP/IP Offloading Engine.
- Support for Fiber or Copper Ethernet ports to front/rear I/O panel.
- Fibre Channel with 2-Gbit full duplex operation.
- 2-MB of SRAM memory to buffer Fibre Channel data.
- Ultra-low power consumption, as low as 65W (both sides).
- Dynamic speed stepping for lowest power possible in stand-by mode.
- Boots from Fibre Channel, Network or IDE/USB devices.
- Quad USB-2.0 ports and dual COM ports.
- XVGA RGB Video for console work.
- Optional up to 16-GB Compact Flash for Boot/storage.
- Optional dual PMC module carrier (2nd Slot).
- Supports VITA 41.3 VXS for Switched Backplane Topology
- 512-KB BIOS Flash with Power-On-Self-Test (POST) functions.
- Full Health monitoring for safe system operation.
- Built In Test (BIT) and Extended BIT (EBIT).
- Front panel LEDs for POST code and Status display.
- All major I/O is connected to front panel, no RTM is required.
- Supports Windows®2000/XP, VxWorks®, Solaris®x86, QNX® and Linux®.
- Available in standard, 0º C to +60º C or extended temperature -20º C to +80º C.

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Computer 1 Specifications Table:

Feature	Description
Processor	Intel Pentium-M (760), 2.0-GHz, 2-MB L2 cache. - 533-Front Side Bus (FSB).
System Controller	ServerWorks Grand Champion CMIC-LE: - 533-MHz FSB. - 144-bit DDR interface, 200/266 MHz, with ECC. - 2 high speed (3.2-GB/Sec) Inter-Module Buses. - 1 200-MB/Sec Inter-Module Bus for South Bridge.
Main Memory	Proprietary Memory Module supporting up to 8 Gbytes. - Configured as 128-MBx144 bits, ECC support included. - DDR PC2100 (266-MHz) Registered. - SPD Function provided (GMS defined contents.)
Boot Flash / BIOS	- STMicro 4-Mbit Flash, M29F400BT. - AMI BIOS 8 core. - Serial Video Re-direct supported. - Boot over Fibre Channel Supported.
I/O Controller	ServerWorks Champion South Bridge CSB5: - 200-MB/Sec Inter-Module Bus Interface to System Controller. - PCI Interface: PCI 32-bit/33-MHz. - IDE Controller: 2 UDMA-100 channels, support for 4 drives. - Low Pin Count (LPC) interface. - X-Bus for System BIOS Flash access. - 16 PCI Interrupts supported. - SMBus Host / GPIOs.
PCI-X Bridge	Server Works Champion I/O Bridge/PCI-X CIOBX2: - 3.2-GB/Sec. Inter-Module Bus Interface to system controller. - 2 PCI-X buses, 64-bit, 66/100/133-MHz
Super I/O	National Semiconductor PC87417 Ultra I/O Controller: - LPC Bus Interface. - Battery backed CMOS for BIOS configuration settings. - Real Time Clock (RTC). - 2 Serial Ports.
Gigabit Ethernet	Intel 82546GB dual port MAC/PHY: - 1 Gigabit port at the front Panel (Copper of Fiber). - Second port routed to Computer 2. - Option to route the Second Port to VITA 41.3 Rear I/O Interface.
Fibre Channel	LSILogic LSI FC 919X PCI-X to Fibre Channel Controller. - 2-GB/s data rate. - Stratos Optical RJ Format Multimode Optical Transceiver Connector at F.P.
Video	Asilisant 69030 Video Controller: - VGA connector at front panel. - On 32-Bit 33-MHz PCI Bus.
USB	5 USB 2.0 ports from NEC USB Controller. - 2 port to front panel. - 2 ports to RTM. - 1 port on optional daughter card expansion.
COM Ports	2 RS232 Serial I/O ports: - 1 serial port via RJ-45 at front panel. - 1 serial port on RTM.

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SAM-3 Expansion	3.2-GB/Sec Inter-Module Bus for system expansion. - Connector for future expansion boards.
Hardware Monitor	- LM81 hardware monitor. - MAX1617 Temp sensor / processor thermal diode interface. - Serial EEPROM for Vital Product Data.
Expansion Card	Custom Expansion card: - 1 IDE port for Compact flash. - 1 USB 2.0 port. - LPC bus for expansion.
Status / Diagnostic Indicators	Support for diagnostic LEDs: POST.
Voltage Regulators	On-board regulation for voltages: - VRM9.1 for CPU Core. - FSB Voltage Regulator (1.05V). - 2.5V for Chipset and DDR Memory Module. - 1.5V for Chipset & Dual Gigabit Ethernet Controller. - 1.25V for memory termination.
Reset/Power Good	- Separate power good circuit - Separate Reset switch for each computer - Common VME reset

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Computer 2 Specifications:

Feature	Description
Processor	Intel Pentium-M (760), 2.0-GHz, 2-MB L2 cache. - 533-Front Side Bus (FSB).
System Controller	ServerWorks Grand Champion CMIC-LE: - 533-MHz FSB. - 144-bit DDR interface, 200/266-MHz, with ECC. - 2 high speed (3.2GB/Sec) Inter-Module Buses. - 1 200-MB/Sec Inter-Module Bus for South Bridge.
Main Memory	Proprietary Memory Module supporting up to 8-Gbytes: - Configured as 128-MBx144-bits, ECC support included. - DDR PC2100 (266-MHz) Registered - SPD Function provided (GMS defined contents.)
Boot Flash / BIOS	- STMicro 4-Mbit Flash, M29F400BT: - AMI BIOS 8 core. - Serial Video Re-direct supported. - Boot over Fibre Channel Supported.
I/O Controller	ServerWorks Champion South Bridge CSB5: - 200-MB/Sec Inter-Module Bus Interface to System Controller. - PCI Interface: PCI 32-bit/33-Mhz. - IDE Controller: 2 UDMA-100 channels, support for 4 drives. - Low Pin Count (LPC) interface. - X-Bus for System BIOS Flash access. - 16 PCI Interrupts supported. - SMBus Host / GPIOs.
PCI-X Bridge	Server Works Champion I/O Bridge/PCI-X CIOBX2: - 3.2-GB/Sec. Inter-Module Bus Interface to system controller. - 2 PCI-X buses, 64-bit, 66/100/133-MHz.
Super I/O	National Semiconductor PC87417 Ultra I/O Controller: - LPC Bus Interface. - Battery backed CMOS for BIOS configuration settings. - Real Time Clock (RTC). - 2 Serial Ports.
Gigabit Ethernet	- 1 Gigabit port at the front Panel (Copper of Fiber). - Second port routed to Computer 1. - Option to route the Second Port to VITA 41.3 Rear I/O Interface.
Fibre Channel	LSILogic LSI FC 919X PCI-X to Fibre Channel Controller: - 2-GB/s data rate. - Stratos Optical RJ Format Multimode Optical Transceiver Connector at F.P.
Video	Asilisant 69030 Video Controller: - VGA connector at front panel. - On 32-Bit 33-MHz PCI Bus.
USB	5 USB 2.0 ports from NEC USB Controller. - 2 port to front panel - 2 ports to RTM. - 1 port on optional daughter card expansion.
COM Ports	2 RS-232 Serial I/O ports: - 1 serial port via RJ-11 at front panel. - 1 serial port on RTM.

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SAM-3 Expansion	3.2-GB/Sec Inter-Module Bus for system expansion. - Connector for future expansion boards.
Hardware Monitor	- LM-81 hardware monitor. - MAX1617 Temp sensor / processor thermal diode interface. - Serial EEPROM for Vital Product Data.
Expansion Card	Custom Expansion card: - 1 IDE port for Compact flash. - 1 USB 2.0 port. - LPC bus for expansion.
Status / Diagnostic Indicators	Support for diagnostic LEDs: POST.
Voltage Regulators	On-board regulation for voltages: - VRM 9.1 for CPU Core. - FSB Voltage Regulator (1.05V). - 2.5V for Chipset and DDR Memory Module. - 1.5V for Chipset & Dual Gigabit Ethernet Controller. - 1.25V for memory termination.
Reset/Power Good	- Separate power good circuit: - Separate Reset switch for each computer. - Common VME reset.

Common Specifications:

Feature	Description
Mechanical	- 6U/4HP VME Form Factor. - Convection Cooled.
VME Backplane Interface	No VME Bus interface on P1 & P2. P1 & P2 provide Power (5 row connectors with +5v & +3.3V). P2 user I/O for RTM access. Optional P0 for VITA 41.3 Interface.

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7.2 Mechanical Specifications

7.2.1 Dimensions

- 233.35mm x 160mm (9.187” x 6.299”).
- Height approximately. 13.20mm (.519”).

7.3 Electrical Specifications

7.3.1 Power Consumption

Configuration

- Processor: Pentium-M 760, 2.0GHz with 2-MB Cache and 533-MHz FSB.
- Memory: 2-GB of 266-MHz DDR SDRAM.
- **Nominal: 79W (61W 5V, 18W 3V),**
- **Maximum: 104W (81W 5V, 18W 3.3V).**

- These values are measured running Windows-XP on both CPUs. Maximum value is with CPU at 100% loading.

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7.4 Environmental Specifications

The Environmental Specifications for the V469 SBC are covered in the tables below:

Commercial

Temperature, Humidity & Altitude		
	Operating	**Non-Operating:**
Temperature:	0º C to +60º C	-40º C to +85º C
Humidity:	0% to 95% non-condensing @ 40ºC	0% to 95% non-condensing @ 40º C
Altitude:		
Coin battery used	15,000 Feet	40,000 Feet
Coin battery not used	50,000 Feet 1. Based on adequate enclosure 2. Cooling is ensured in system level	50,000 Feet
Vibration & Shock		
Vibration:	Spectrum [Hz]	5-2000
	Acceleration (RMS)	2g
	Duration	30 minutes per axis
Shock:	Amplitude	20g
	Duration	6ms
	Hits	5 per axis
Salt & Fog		
When conformal coated, the product will withstand 5% salt (NaCl) atmosphere at 95° F for minimum of 48 hours.		

Extended Temperature

Temperature, Humidity & Altitude		
	Operating	**Non-Operating:**
Temperature:	-40º C to +85º C	-40º C to +85º C
Humidity:	0% to 95% non-condensing @ 40º C	0% to 95% non-condensing @ 40º C
Altitude:		
Coin battery used	15,000 Feet	40,000 Feet
Coin battery not used	50,000 Feet 1. Based on adequate enclosure 2. Cooling is ensured in system level	50,000 Feet
Vibration & Shock		
Vibration:	Spectrum [Hz]	5-2000
	Acceleration (RMS)	6g
	Duration	30 minutes per axis
Shock:	Amplitude	35g
	Duration	6ms
	Hits	5 per axis
Salt & Fog		
When conformal coated, the product will withstand 5% salt (NaCl) atmosphere at 95° F for minimum of 48 hours.		

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Extended Temperature, Ruggedized

Temperature, Humidity & Altitude			
	Operating	**Non-Operating:**	
Temperature:	-40º C to +80º C	-40º C to +85º C	
Humidity:	0% to 95% non-condensing @ 40º C	0% to 95% non-condensing @ 40º C	
Altitude:			
Coin battery used	15,000 Feet	40,000 Feet	
Coin battery not used	50,000 Feet 1. Based on adequate enclosure 2. Cooling is ensured in system level	50,000 Feet	
Vibration & Shock			
Vibration:	Spectrum [Hz]	5-2000	
	Acceleration (RMS)	15g	
	Duration	30 minutes per axis	
Shock:	Amplitude	100g	40g
	Duration	6ms	11ms
	Hits	5 per axis	5 per axis
Salt & Fog			
When conformal coated, the product will withstand 5% salt (NaCl) atmosphere at 95° F for minimum of 48 hours.			

7.4.1 Air Flow

- 400 Linear Feet per Minute LFM (Minimum).
- This airflow must be kept across the CPU Heat Sink to guarantee CPU performance.

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8. MAJOR COMPONENTS

8.1 CPU

The Intel® Pentium® M processor is a high performance, low power mobile processor with several micro-architectural enhancements over existing Intel mobile processors.

The Intel® Pentium® M processor is manufactured on Intel's advanced 0.13 micron process technology with copper interconnects. The processor maintains support for MMX™ technology and Internet Streaming SIMD instructions and full compatibility with IA-32 software. The high performance core features architectural innovations like Micro-op Fusion and Advanced Stack Management that reduce the number of micro-ops handled by the processor. This results in more efficient scheduling and better performance at lower power. The on-die 32-KB level I instruction and data caches and the 1-MB Level 2 cache with Advanced Transfer Cache Architecture enable significant performance improvement over existing mobile processors. The processor also features a very advanced branch prediction architecture that significantly reduces the number of mispredicted branches. The processor's Data Prefetch Logic speculatively fetches data to the L2 cache before L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance.

The Streaming SIMD Extensions 2 (SSE2) enable break through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Part Number: **RJ80535GC0251M**.

Additional Features:

- Supports Intel Architecture with Dynamic Execution.
- High performance, low-power core.
- On-die, primary 32-kbyte-instruction cache, and 32-kbyte write-back data cache.
- Advanced Branch Prediction and Data Pre-fetch Logic.
- Streaming SIMD Extensions 2 (SSE2).
- 400-MHz, Source Synchronous processor system bus.
- Advanced Power Management features including Enhanced Intel SpeedStep® technology.
- Micro-FCBGA Packaging Technologies.

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8.2 Server-Works™ CMIC-LE Bridge

The Grand Champion LE utilizes the IMB to connect the host bridge to a variety of south bridges and I/O bridges. This building block approach, common across all Server-Works System I/O solutions, offers OEMs ease of platform migration and reconfiguration by leveraging existing designs. The Two Way Multiprocessing Server Configuration is shown in Figure 4.

The Grand Champion LE is targeted at the volume 2 Way server market. It's a highly scaleable System I/O solution for the Pentium IV and Pentium IV XEON™ family of processors, and can be configured to meet OEMs needs for a variety of product segments.

The Grand Champion LE is the highest performance 2 Way Pentium IV System I/O solutions on the market. With dual memory channels capable of supporting up to 16-GB of DDR200 memory the GC-LE provides 3.2-GB/s of memory bandwidth. I/O and processor bandwidth complement the memory bandwidth. Two IMB buses provide support for up to 4, independent PCI-X buses, with 6.4-GB/s of bandwidth between them. The Front Side Bus (FSB) provides 3.2-GB/s of bandwidth, a 3-fold increase over the Pentium III generation. The high bandwidth, low latency data paths on all interfaces provide the performance next generation enterprise servers require.

The GC-LE is an extremely robust platform from a Reliability, Availability and Scalability (RAS) perspective. With a multi-bit memory ECC algorithm, memory scrubbing and Chip-kill™ you can be assured that your data integrity is maintained. If a failure does occur the GC-LE supports Spare Memory configurations so any failure will be invisible to the end user. The managers can then replace the memory module at their convenience. Additional RAS features are provided on the I/O interfaces. The IMB is CRC protected.

The GC-LE utilizes the IMB to connect the host bridge to a variety of south bridges and I/O bridges. This building block approach, common across all ServerWorks System I/O solutions, offers OEMs ease of platform migration and reconfiguration by leveraging existing designs.

Part Number: **SWC-NB7465-P03**.

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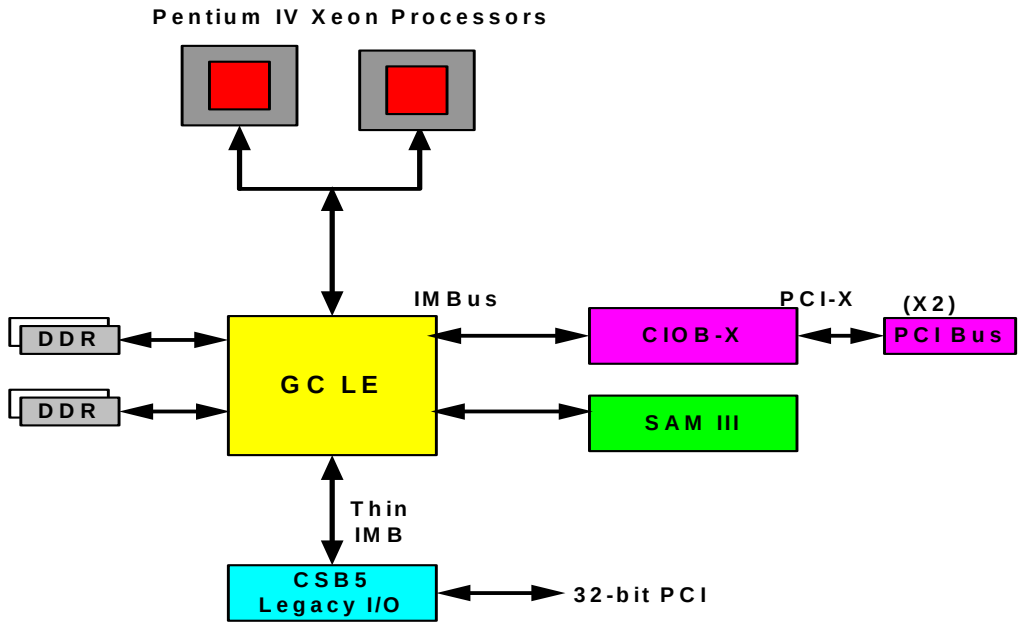


Figure 4. Two Way Multiprocessing Server Configuration

Additional Features:

- Processor Interface.
  - Two-way Pentium IV XEON™.
  - 400-MHz FSB; 3.2-GB/s FSB Bandwidth.
- Memory Controller.
  - Dual DDR200 Channels.
  - 16-GB of memory, two-way Inter-leaved.
  - 3.2-GB/s of memory Bandwidth.
- I/O Bridge Interface.
  - 2 Inter-Module Buses (IMB) 3.2-GB/s per bus.
  - One Thin IMB bus to CSB-5 South Bridge.

RAS Features:

- ECC – 128-bit algorithm; 16-bit detection; 8-bit correction.
- Memory Scrubbing, Chip-kill™.
- Spare Memory.
- Fault Isolation.
- Extensive error reporting.

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8.3 Server-Works™ C10B-X2 Dual PCI-X

The Server-Works™ C10B-X2 Dual PCI-X is the I/O Bridge between the CMIC-LE and the PCI buses.

Part Number: **SWC-IB-7425-P03**.

Additional Features:

- Dual PCI-X Buses; Supports PCI 2.2.
- 64-bit; 66/100/133-MHz.

8.4 Server-Works™ CSB5 South Bridge

Server-Works™ CSB5 (Legacy I/O) South Bridge interfaces with the GC-LE via a Thin IMB. It is a 32-bit PCI Bridge.

Part Number: **SWC-SB-7440=P01**.

Additional Features:

- PCI 2.2 32-bit/33-MHz.
- Legacy functions (8237DMA, 8259PIC, 8254Timer).
- PCI to LPC Bridge.
- XIO-APIC for multiprocessor systems.
- 4 Port USB 1.0 interface.
- ACPI power management and event detection support.
- Dual Channel hard disk controller.

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8.5 Tundra® (CA91C142) PCI to VME Bridge

The Universe II™ PCI-to-VME bus interface controller (CA91C142) is a member of Tundra's growing line of Openbus Interface Components (OIC), and provides a reliable, high performance 64-bit VME bus interface in one device. The Universe II is ideally suited for a CPU board acting as either master or slave in the VME bus system, and is particularly fitted for PCI local systems.

Universe II™ bridges VME platforms to PCI-based applications. Bridging is accomplished via a powerful decoupled architecture with independent FIFOs for inbound, outbound, and DMA traffic. With this architecture, throughput is maximized without sacrificing bandwidth on either bus.

A zero-wait state implementation, with multi-beat transactions and support for bus parking, ensures that Universe II™ is never the bottleneck on the PCI bus. On VME, a rich set of features ensures that the device fits within a wide range of applications. A full suite of addressing and data modes is implemented, including BLT and MBLT support. In addition, a fully featured system controller, interrupter, interrupt handler, and Linked-List DMA make Universe II features include location monitors, mailboxes, and semaphores.

Part Number: **CA91C142D-33CE**.

Additional Features:

- Industry-proven, high performance 64-bit VMEbus interface.
- Fully compliant, 32-bit or 64-bit, 33 MHz PCI bus interface.
- Integral FIFOs for write posting to maximize bandwidth utilization.
- Programmable DMA controller with Linked-List mode (Scatter/Gather) support.
- Flexible interrupt logic.
- Sustained transfer rates up to 60-70 Mbytes per second.
- Extensive suite of VMEbus address and data transfer modes.
- Automatic initialization for slave-only applications.
- Flexible register set, programmable from both the PCI bus and VMEbus ports.
- Full VMEbus system controller functionality.
- Support for RMWs, ADCH, PCI LOCK # cycles, and semaphores.
- Commercial, industrial, and extended temperatures.
- IEEE 1149.1 JTAG testability support.
- Available in 361-pin dimpled ceramic BGA (DBGA) and 313-pin plastic BGA packages.

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8.6 Intel® (82559ER) Ethernet Controller

The Intel® 82559ER has an integrated physical layer interface for 10/100 Mbps to provide full support of 100BASE-TX and 10BASE-T operation on the V469 SBC.

The 82559ER controller contains a 32-bit PCI bus master interface optimized to fully utilize the high bandwidth available to PCI bus masters. The bus master interface can eliminate the 'intermediate copy' step in receive and transmit frame copies, resulting in faster processing and less dependence on the host CPU.

Part Number: **GD82559ER**.

Additional Features:

- Glue-less 32-bit PCI bus master interface.
- Compliance with Advanced Configuration and Power Interface and PCI Power Management specifications.
- Support for wake-up on interesting packets and link status change.

8.6 Intel® (82546GB) Dual Port Gigabit Ethernet Controller

The Intel® 82546GB Dual Port Gigabit Ethernet Controller is a single, compact component with two full Gigabit Ethernet MAC and PHY layer functions and Serializer/Deserializer (SerDes) on a single, compact component. Packaged in a 21x21 mm PBGA, the Intel 82546GB Dual Port Gigabit Ethernet controller provides dual port functionality without additional board space requirements for the component and enables a dual port Gigabit Ethernet implementation in a very small area.

The Intel® 82546GB's onboard SMBus port enables enhanced manageability and system health monitoring via the LAN. With SMBus, management packets can be routed to or from a management processor. The SMBus port enables industry standards such as Intelligent Platform Management Interface (IPMI) to be implemented with the Intel 82546GB. In addition, ASF 1.0 (Alert Standard Format) standard circuitry provides alerting and remote control capabilities with standardized interfaces.

Part Number: **82546GB**.

Additional Features:

- PCI Rev 2.2, 32/64-bit, 33/66-MHz.
- Dual 64-KB configurable RX and TX packet FIFOs per port.
- IEEE 802.3x compliant flow control support with software controllable threshold.

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8.8 TI (1394b) High Performance Link Layer Controller

The TSB82AA2 OHCI-Lynx is a discrete 1394b link-layer device, which has been designed to meet the demanding requirements of today's 1394 bus designs. The TSB82AA2 device is capable of exceptional 800M bits/s performance; thus, providing the throughput and bandwidth to move data efficiently and quickly between the PCI and 1394 buses. This device also provides outstanding ultra-low power management capabilities. The device provides IEEE 1394 link function and is compatible with 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s serial bus data rates.

The TSB82AA2 OHCI-Lynx operates as the interface between a 33-MHz/64-bit or 33-MHz/32-bit PCI local bus and a compatible 1394b PHY-layer device (such as the TSB81BA3 device) that is capable of supporting serial data rates at 98.304M, 196.608M, 393.216M, or 786.432M bits/s (referred to as S100, S200, S400, or S800 speeds, respectively). When acting as a PCI bus master, the TSB82AA2 device is capable of multiple cache line bursts of data, which can transfer at 264M bytes/s for 64-bit transfers or 132M bytes/s for 32-bit transfers after connecting to the memory controller.

Part Number: **TSB82AA2**.

Additional Features:

- Single 3.3V supply (1.8V internal core voltage with regulator).
- 3.3V and 5V PCI signaling environments.
- Serial bus data rates of 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s.
- Physical write posting of up to three outstanding transactions.
- Serial ROM or boot ROM interface supports 2-wire serial EEPROM devices.
- 33-MHz/64-bit and 33-MHz/32-bit selectable PCI interface.
- Programmable asynchronous transmit threshold.
- Isochronous receive dual-buffer mode.
- Out-of-order pipelining for asynchronous transmits requests.
- Register access fail interrupt when the PHY SYSCLK is not active.
- Initial Bandwidth available and initial channels available registers.
- Digital video and audio performance enhancements.
- Fabricated in advanced low-power CMOS process.
- Packaged in 144-terminal LQFP (PGE).

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8.9 TI (TSB81BA3) IEEE P1394b S800 Three-Port Cable Transceiver/Arbiter

The TSB81BA3 Transceiver/Arbiter provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB81BA3 is designed to interface with a Link-Layer Controller (LLC), such as the TSB82AA2.

The TSB81BA3 is powered by dual voltage supplies, such as a 3.3V supply for I/O and a core voltage supply. The core voltage supply is supplied to the PLLVDD-1.8 and DVDD- 1.8 terminals to the requirements in the recommended operating conditions.

The TSB81BA3 requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal Phase-Locked Loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two devices and is used for resynchronization of the received data when operating the PHY-link interface in compliance with the IEEE 1394a-2000 standard. A 98.304-MHz clock signal is supplied to the associated LLC for synchronization of the two devices when operating the PHY-link interface in compliance with the IEEE P1394b standard. The Power Down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

Part Number: **TSB81BA3**.

Note:

The BMODE terminal does not select the cable interface mode of operation. The BMODE terminal selects the PHY-link interface mode of operation and affects the arbitration modes on the cable. When the BMODE terminal is de-asserted, BOSS arbitration is disabled.

Additional Features:

- Fully supports provisions of IEEE P1394b Revision 1.33+ at 1- Gigabit Signaling Rates.
- Fully Interoperable with Firewire™, i.LINK™, and SB1394™, Implementation of IEEE Std 1394.
- Provides Three Fully Backward Compatible, (1394a-2000 Fully Compliant) Bilingual P1394b Cable Ports at up to 800 Megabits per Second (Mbits/s).
- Power-Down features to conserve energy in battery powered applications.
- Low-Power Sleep Mode.
- Interoperable with Link-layer Controllers using 3.3V Supplies.
- Interoperable with other 1394 Physical Layers (PHYs) using 1.8V, 3.3V, and 5V Supplies.
- Low cost, high performance 80-pin TQFP (PFP) Thermally Enhanced Package.

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8.10 EXAR (ST16C2550) Dual UART with 16-Byte Transmit and Receive FIFOs

The ST16C2550 is a Dual Universal Asynchronous Receiver and Transmitter (UART). The ST16C2550 is an improved version of the NS16C550 UART with higher operating speed and power access time. The ST16C2550 provides enhanced UART functions with 16 byte FIFOs, a modem control interface, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. System interrupts and modem control features may be tailored by external software to meet specific user requirements. An internal loop- back capability allows onboard diagnostics. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50 Bps to 1.5 Mbps. The Baud rate generator can be configured for either crystal or external clock input.

The 2550 are available in a 40-pin plastic-DIP, 44-pin PLCC, and 48-pin TQFP packages. The 40-pin package does not offer TXRDY and RXRDY pins (DMA Signal monitoring). Otherwise the three package versions are the same. The 2550 are functionally compatible with the 16C2450. The 2550 are fabricated in an advanced CMOS process to achieve low drain power and high-speed requirements.

Part Number: **STC2550CQ48**.

Additional Features:

- Dual UART device.
- Up to 4 Mbps with external clock of 64-MHz.
- Up to 1.5 Mbps data rate with a 24-MHz crystal frequency.
- 16-byte transmit FIFO to reduce the bandwidth requirement of the external CPU.
- 16-byte receive FIFO with error flags to reduce the bandwidth requirement of the external CPU.
- Independent transmit and receive UART control.
- Status Report register.
- Crystal or external clock input.
- TTL compatible inputs, outputs.
- 3.3V or 5V supply operation.

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8.11 NEC (PD720101) USB 2.0 Host Controller

The USB 2.0 Host Controller PD720101 complies with the Universal Serial Bus Specification Revision 2.0 and Open Host Controller Interface Specification for full/low speed signaling and Intel's Enhanced Host Controller Interface Specification for high-speed signaling and works up to 480 Mbps. The PD720101 is integrated 3 host controller cores with PCI interface and USB2.0 transceivers into a single chip.

Part Number: **µPD720101F1-EA8.**

Additional Features:

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data rate 1.5/12/480 Mbps).
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a.
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 1.0.
- PCI multi-function device consists of two OHCI host controller cores for full/low speed signaling and one EHCI host controller core for high speed signaling.
- Root hub with 5 (max) downstream facing ports, which are shared by OHCI and EHCI host controller cores.
- All downstream facing ports can handle high-speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps).
- Configurable number of downstream facing ports (2 to 5).
- 32-bit 33-MHz host interface compliant to PCI Specification release 1.1.
- PCI bus master access.
- Legacy support for all downstream facing ports. Legacy support features allow easy migration for motherboard implementation.
- 3.3V power supply, PCI signal pins have 5V tolerance circuit.

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8.12 ATI Technologies Mobility Radeon™ 9000 Graphics Controller

The Mobility Radeon™ 9000 provides the fastest and most advanced 2D, 3D, and multimedia graphics performance for the latest applications in full 32-bit color. Its architecture introduces the latest achievements in the graphics industry, which enable the use of the progressive new features in upcoming applications, but without compromising performance. ATI's exclusive support of DirectX® 8.1 features, highly optimized OpenGL® support, and flexible memory configurations allow implementations targeted at both gaming enthusiast and workstation platforms.

Part Number: **M9-CSP64**.

Additional Features:

- SMARTSHADER™ - Advanced Shader Technology.

  - Provides complete hardware-accelerated support for the new DirectX® 8.1 programmable shader model, enabling more complex and realistic texture and lighting effects than ever before.

  - Offers full support for this feature in OpenGL® 1.3 applications.

- SMOOTHVISION™ – Flexible Anti-Aliasing.

  - The most flexible and efficient anti-aliasing implementation available to date.

  - Better visual quality with minimal performance degradation.

  - Supports DirectX® 8.1 multisampling and related effects, including motion blur and depth-of-field.

- High Performance Memory Support.

  - Incorporates support for DDR SDRAM/SGRAM at up to 220-MHz.

  - Boosts effective memory bandwidth by over 20%.

- Dual Display Support.

  - Leading edge technology, fully optimized with HYDRA VISION™, flexibly supports multiple combinations of traditional CRT monitors, flat panel displays and TV.

  - Improved RAMDAC speed of 400-MHz.

- CHARISMA ENGINE™ II.

  - CHARISMA ENGINE™ II, the MOBILITY RADEON 9000 geometry engine, delivers on average 45 million transformed, clipped, and lit triangles/second processing capability. Additionally, the engine implements a fully compliant DirectX® 8.1 Programmable Vertix Shader.

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- PIXEL TAPESTRY™ II.

  - PIXEL TAPESTRY™ II, the MOBILITY RADEON 9000 3D rendering engine, utilizes 4 parallel pipelines each capable of handling up to 6 textures in a single pass, delivering an incredible 1.0 gigatexels per second fill rate for maximum 32 bit color performance at the highest resolutions.

- VIDEO IMMERSION™ II.

  - VIDEO IMMERSION™ II technology allows integration of industry leading digital video features; including advanced de-interlacing and frame rate conversion algorithms for unprecedented video quality and integrated digital TV decode capability. It also Includes programmable, independent gamma control for the video overlay.

- Ideal for Windows 2000 and Windows XP.

  - MOBILITY RADEON 9000 provides comprehensive support for all new Windows 2000 and Windows XP display-oriented features, including acceleration of new GDI extensions like Alpha BLTs, Transparent BLTs, and Gradient Fills, as well as exclusive, patent-pending hardware alpha cursor support.

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8.13 National Semiconductor® PC87417 LPC Servo Ultra I/O

The National Semiconductor® PC87417 is a highly integrated Advanced I/O. The PC87417 is targeted for a wide range of servers and workstations that use the Low Pin Count (LPC) bus for the host interface.

Part Number: **PC87417-ICK/VLA**.

The PC87417 advanced I/O block diagram is shown in Figure 5.

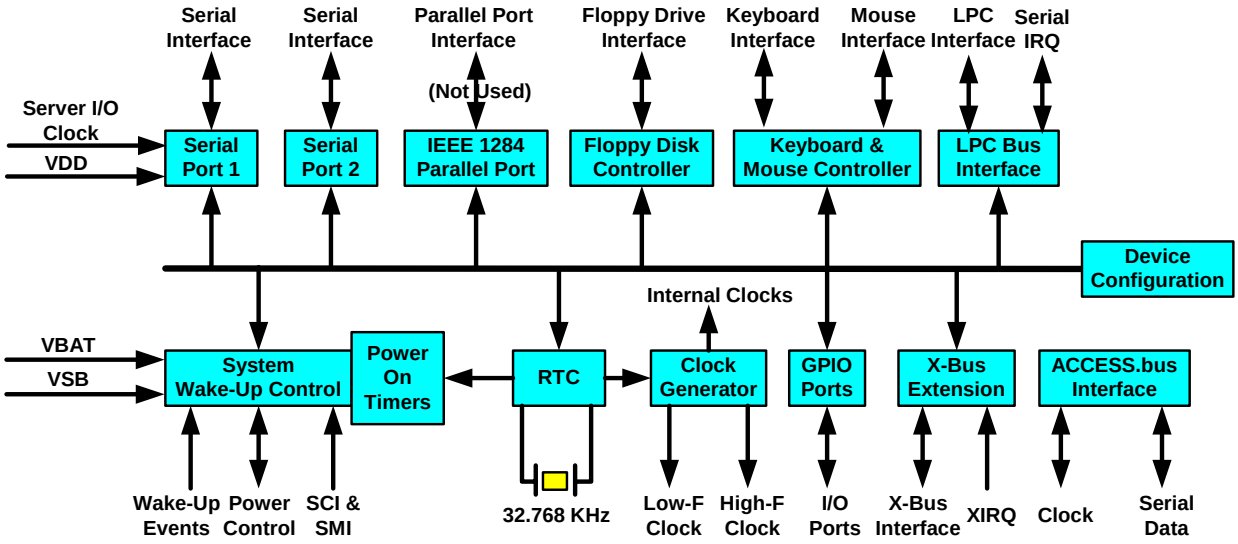


Figure 5. PC87417 Advanced I/O Block Diagram

Additional Features:

- LPC Interface, based on Intel's LPC Interface Specification, Revision 1.0.
- X-Bus Extension for memory and I/O.
- Servo I/O modules:
  - FDC,
  - Two Serial Ports (UART),
  - Keyboard and Mouse Controller.
- RTC with 242 bytes of RAM.
- 51 GPIO ports with a variety of wake-up events.
- Extremely low current consumption in Battery Backup mode.
- 128-pin PQFP package.

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8.14 LSI (53C1020) Ultra320 SCSI Controller

The LSI53C1020 is an extremely high performance, intelligent PCI-X to Single Channel Ultra320 Controller. The LSI53C1020 is compliant with the SPI-4 SCSI draft specification, and provides additional features to ensure robust system operation. LSI Logic's Fusion-MPT™ (Message Passing Technology) architecture provides unparalleled performance, binary compatibility of host software with LSI Logic's Fiber Channel products, and significantly reduced software development time. With this advanced architecture, the LSI Logic product family can be quickly adapted to respond to emerging I/O interfaces.

Part Number: **LSI53C1020**.

ULTRA320 SCSI Features

Paced transfers and double transition clocking enable throughput of up to 320 MBps. Both the data and clock frequencies are doubled. Because of the faster data and clock speeds, Ultra320 SCSI introduces skew compensation and InterSymbol Interference (ISI) compensation. Skew compensation adjusts for timing differences between data and clock signals caused by cabling, board traces, etc. ISI compensation enhances the first pulse after a change in state to ensure data integrity.

PCI-X Interface

The host PCI-X interface complies with the PCI Local Bus Specification Revision 2.2, and the PCI-X addendum, Revision 1.0. It implements a 100-MHz, 64-bit bus and is backward compatible with 33/66-MHz, 32/64-bit PCI. Support for 64-bit addressing with Single Address Cycle (DAC) is provided.

SCSI Cores

The LSI 53C1020 Controller supports wide Ultra320 SCSI synchronous transfer rates up to 320 MBps on a LVD SCSI bus. Integrated LVDlink™ transceivers support both LVD and single-ended signals with no external transceivers required. The LSI53C1020 Controller supports all fast SCSI, Ultra SCSI, Ultra2 SCSI, Ultra 160 SCSI, and Ultra320 SCSI.

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Memory Interfaces

Expansion ROM is implemented on local memory bus.

The LSI53C1020 Ultra320 SCSI Controller implementation block diagram is shown in Figure 6.

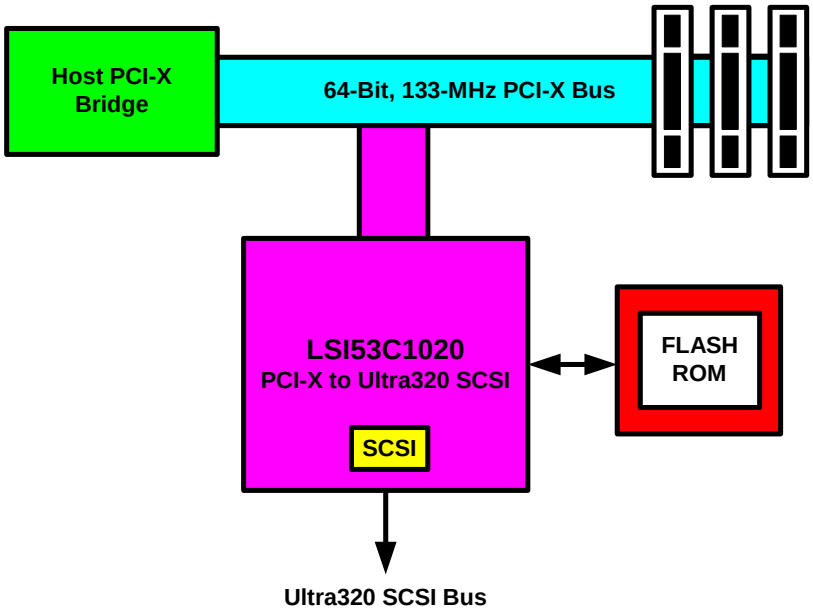


Figure 6. LSI 53C1020 Implementation Block Diagram

Additional Features:

- 100-MHz, 64-bit PCI-X Interface.
- Supports Ultra320 with:
  - Double transition clocking for 320-MBps throughputs.
  - Packetized protocol.
  - Quick Arbitrate and Select (QAS).
  - Skew compensation.
  - InterSymbol Interference (ISI) compensation.
  - Domain validation, including margining.
- Performance optimized architecture.
- SCSI Interrupt Steering Logic (SISL) provides alternate interrupt routing for RAID applications.
- Packaged in a 456 EPBGA.

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8.15 M-Systems (MD2811) Disk-On-Chip

The Disk-On-Chip (DOC) 2000 TSOP 16-MB (MD2811-D16-V3) is based on M-Systems patented DOC technology. The DOC is a flash disk that provides full hard disk emulation using solid-state flash memory technology. The MD2211 combines a disk controller with flash memory in a single chip providing a complete, easily integrated, flash disk solution. In addition, the DOC is a multi-function device. It provides both mass data storage and code storage with eXecute In Place (XIP) capabilities.

The DOC is based on state of the art NAND flash technology. NAND flash features exceptional write and erase performance, providing the optimal data storage solution. Additionally, NAND technology is known for its high density and small die size. Thus providing a cost effective solution.

A programmable boot block (1-KB) provides XIP capability. This means, that the DOC can replace a boot ROM, functioning as the only non-volatile memory onboard. Eliminating the need for an additional boot ROM on the motherboard not only reduces cost, but also saves programming effort, reduces logistics costs, reduces board real estate, and simplifies PCB layout and more. Although the XIP area is only 1-KB, larger boot code images can be executed by swapping in multiple code pages from the flash memory.

The DOC is optimized for use where minimum weight, space, and low power consumption are essential. Furthermore, the DOC has no moving parts, resulting in significantly decreased power consumption and increased reliability. It is easy to use and reduces integration overhead.

Part Number: **MD2811-D32-V3**.

Additional Features:

- Flash Disk – full hard emulation.
- 16-MB (128Mbit) capacity.
- Single-chip, based on state of the art NAND flash technology.
- Small form factor – standard 48-pin TSOP-I package.
- High Reliability – on the fly EDC/ECC.

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8.16 National Semiconductor® (LM81) Microprocessor System Monitor

The LM81 is a highly integrated data acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor-based system. In a V469, the LM81 is used to monitor power supply voltages, temperatures, and fan speeds. Actual values for these inputs can be read at any time. Programmable WATCHDOG limits in the LM81 activate a fully programmable and maskable interrupt system with two outputs (INT# and T_CRIT_#).

The LM81 has an on-chip, digital output temperature sensor with a 9-bit or 12-bit resolution. Additionally, the LM81 has six analog inputs ADC with 8-bit resolution and an 8-bit DAC. The DAC, with a 0 to 1.25V output voltage range, can be used for fan speed control. Additional inputs are provided for Chassis Intrusion detection circuits, and VID monitor inputs. The LM81 has a Serial Bus interface that is compatible with SMBus™.

Part Number: **LM81BIMT-3**.

Additional Features:

- Temperature sensing.
- Six positive voltage inputs with scaling resistors to monitor +5V, +12V, +3.3V, +2.5V, VCC Power supplies directly.
- WATCHDOG comparison of all monitored values.
- SMBus™ 1.0 (LM81C) and 1.1 (LM81B) Serial Bus interface compatibility.
- LM81B has improved voltage-monitoring accuracy.

GMS provides software support for this function under NT™, Windows® 2000 and VxWorks®.

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8.17 MAXIM (MAX1617) Temperature Sensor

The MAXIM MAX1617 is used to measure the die temperature of the V469 main processor via an SMBus serial interface.

The MAX1617 is a precise digital thermometer that reports the temperature of both a remote sensor and its own package. The remote sensor is a diode-connected transistor. Remote accuracy is a +/- 2°C for multiple transistor manufacturers, with no calibration needed.

The MAX1617 is available in a small, 16-pin QSOP surface-mount package.

Part Number: **MAX1617AMEE**.

Additional Features:

- Two channels: Measures both Remote and Local Temperatures.
- No calibration required.
- SMBus 2-Wire Serial Interface.
- Programmable Under/Over temperature Alarms.
- Supports SMBus Alert Response.
- 3µA (typical) Standby Supply Current.
- L70µA (max) Supply Current in Auto-Convert Mode.
- +3V to +5.5V Supply Range.
- Small, 16-Pin QSOP Package.

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8.18 Atmel® (AT93C46/AT93C66), 3-Wire Serial CMOS EEPROM

The ATMEL® AT93C46 and AT93C66 provide 1024/2048/4096 bits of serial EEPROM organized as 64/128/256 words of 16-bits each, when the ORG Pin is connected to VCC and 128/256/512 words of 8-bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46 and AT93C66 are available in space saving 8-pin PDIP and 8-pin JEDEC and EIAJ SOIC packages.

The **AT93C46** is a **1K (64X16)** 3-Wire Serial EEPROM and the **AT93C66** is a **4K (256X16)** 3-Wire Serial EEPROM.

The AT93C46 and AT93C66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift ClocK (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE/ ENABLE State. When CS is brought “high” following the initiation of a WRITE cycle, the DO pin outputs the READ/BUSY status of the part.

Additional Features:

- AT93C46 – 1K: 128 x 8 or 64 x 16.
- AT93C66 – 4K: 512 x 8 or 256 x 16.
- 3-Wire Serial Interface.
- 2-MHz Clock Rate (5V) Compatibility.
- Self-Timed Write Cycle (10 ms max).
- High Reliability.
  - Endurance: 1 Million Cycles.
  - Data Retention: 100 Years.
- 8-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages.

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8.19 Atmel® (AT24C256) 2-Wire Serial EEPROM

The AT24C256 provides 131,072/262, 144-bits of serial Electrically Erasable and Programmable Read Only Memory (EEPROM) organized as 16,384/32,768 words of 8 bits each.

Additional Features:

- Low-Voltage and Standard-Voltage Operation.
  - 2.7 (VCC=2.7V to 5.5V).
- Internally Organized 16,384 x 8 and 32,768 x 8.
- 2-Wire Serial Interface.
- Write Protect Pin for Hardware and Software Data Protection.

The EEPROM is located on the I²C bus at address 1010, 011 x 'B'.

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8.20 Atmel® (AT24C16) Serial EEPROM

The AT24C16 provides 16384-bits of serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 2048 words of 8-bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT24C16 is accessed via a 2-Wire serial interface.

Part Number: **AT24C16**.

Additional Features:

- Low-voltage and Standard-voltage operation.
  - 2.7 (VCC = 2.7V to 5.5V).
  - 1.8 (VCC = 1.8V to 5.5V).
- Internally Organized 2048 x 8 (16K).
- 2-Wire Serial Interface.
- Schmitt Trigger, Filtered Inputs for Noise Suppression.
- Bi-Directional Data Transfer Protocol.
- 100-KHz (1.8V, 2.5V, 2.7V) and 400-KHz (5V) Compatibility.
- Write Protect Pin for Hardware Data Protection.
- 8-byte Page (1K, 2K) 16-byte Page (16K) writes modes.
- Partial Page Writes are allowed.
- Self-timed Write Cycle (10-ms max).
- High reliability.
  - Endurance: 1 Million Write Cycles.
  - Data Retention: 100 Years.
- Automotive Grade and Extended Temperature Devices Available.
- 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead TAP and 8-lead TSOP Packages.

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8.21 Intersil™ (ISL6115CB) Controller

The ISL6115CB Controller is a Hot Swap Power controller. It is targeted for +12 Volts control applications. The ISL6115CB has a hard wired Under Voltage (UV) monitoring and reporting threshold level ~17% lower than the nominal +12V and +5V.

The ISL6115CB has an integrated charge pump allowing control of up to +16V using an external N-channel MOSFET. It also features programmable Over Current (OC) detection, Current Regulation (CR) with time delay to latch off and soft start.

The significant differentiation is in the functionality of the PGOOD feature, how and when it reports an UV condition. The PGOOD featured on the HIP devices are disabled during turn-on of the external MOSFET until the GATE pin voltage has reached a particular voltage. PGOOD is defaulted to VDD during this disabled period.

Part Number: **ISL6115CB**.

Additional Features:

- Hot Swap Single Power Distribution Control for +12 Volts.
- Over Current Fault Isolation.
- Programmable Current Regulation Level.
- Programmable Current Limit Time to Latch-Off.
- Rail to Rail Common Mode Input Voltage Range.
- Internal Charge Pump allows the use of N-Channel MOSFET.
- Under Voltage and Over Current Latch Indicators.
- Adjustable Turn-On Ramp.
- Protection during Turn On.
- Two Levels of Over Current Detection Fast Response to Varying Fault Conditions.
- 1µ's Response Time to Dead Short.

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8.22 Micrel (MIC2505-2) Power Switch

The Micrel MIC2505-2 is a high-side power switch that consists of TTL compatible control/enable inputs, a charge pump, and protected N-channel MOSFET. The MIC2505-02 can be used instead of separate high-side drivers and MOSFET in many low-voltage applications.

The MIC2505-2 can deliver at least 2A continuous current. A slow turn-on feature prevents high inrush current when switching capacitive loads. MIC2505-2 is tailored to Universal Serial Bus (USB) applications and do not include open-load detection.

Part Number: **MIC2505-2BM**.

Additional Features:

- 2.7V to 7.5V input.
- 110µA typical on-state supply current.
- 1µA typical off-state supply current.
- Output can be forced higher than input (off-state).
- Current limit.
- Thermal shutdown.
- 2.5V Under Voltage Lock Out (UVLO).
- 5ms (slow) turn-on and fast turnoff.
- Logic-level control/enable input.

8.23 Transpower Technologies (RJ-714-CL2) 10/100 Magnetics

The Transpower Technology 10/100 Magnetics is a Single Port Through Hole (TH).

Part Number: **RJ-714-CL2**.

Additional Features:

- Meets IEEE 802.3 and ANSI X3.263 Requirements.
- Includes integrated LEDs. LED signal leads are isolated from the Ethernet signal leads to reduce EMI.
- Signal Routing is designed for NIC applications.
- LEDs are Yellow and Green.

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8.24 St Microelectronics (M29W040B) 4 Mbit Flash Memory

The M29W040B is a 4-Mbit (512KB x 8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

Part Number: **M29W040B90N1**.

Additional Features:

- Single 2.7 to 3.6V Supply Voltage for program, erase and read operations.
- Access Time: 55ns.
- Programming Time: 10µs per byte typical.
- Unlock Bypass Program Command.
- 100,000 Program/Erase Cycles per Block.
- 20-Year Data Retention.
- Electronic Signature.

8.25 St Microelectronics (M29W400BT) 4 Mbit Flash Memory

The M29W400BT is a 4 Mbit (512KB x 8 or 256KB x 16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power up, the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

Part Number: **M29F400BT70N1**.

Additional Features:

- Single 2.7 to 3.6V Supply Voltage for program, erase and read operations.
- Access Time: 55ns.
- Programming Time: 10µs per byte typical.
- 11 Memory Blocks.
  - 1 Boot Block (Top or Bottom Location).
  - 2 Parameter and 8 Main Blocks.
- 100,000 Program/Erase Cycles per Block.
- 20-Year Data Retention.

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8.26 LSI Logic (LSI FC 929 X) Fibre Channel Controller

The LSI FC 919X is a high performance, intelligent I/O processor that simultaneously supports mass storage protocols on a full duplex FC link. From the host CPUY perspective, the LSI FC 919X manages the FC link at the exchange level for mass storage (FCP) protocols. The LSI FC 919X is a highly efficient NL_Port that supports point-to-point, public and private loop topologies, and the FC switch/attach topology defined in the ANSI X3T11 FC-PH standard.

The LSI FC 919X supports a 64-bit, 133-MHz PCI-X interface and is backward compatible with 32-bit, 33-MHz PCI systems. The LSI FC 919X supports a dual channel, 2-Gbit/s full duplex Fibre Channel link.

Part Number: **LSI FC 929 X**.

Additional Features:

- egrated 2-Gb/s single channel, full-duplex Fibre Channel protocol controller.
- 64-bit, 133-MHz PCI-X host bus interface.
- Integrated GigaBlaze™ 2-Gb/s serial link.
- Fusion MPT™ architecture.
- Auto-negotiation for legacy connect.
- Custom ARM RISC processor.
- Synchronous SRAM external memory interface.
- Full simultaneous target and initiator operations.
- PC2001 compliant.
- JTAG debug interface.
- 456 PBGA.

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8.27 Intersil™ (ISL6520) Single Synchronous Buck PW Modulation Controller

The ISL6520 makes simple work out of implementing a complete control and protection scheme for a DC-DC step-down converter. Designed to drive N-channel MOSFETs in a synchronous buck topology, the ISL6520 integrates the control, output adjustment, and monitoring and protection functions into a single 8-pin package.

The ISL6520 provides simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of +/- 1.5% over temperature and line voltage variations. A fixed frequency oscillator reduces design complexity, while balancing typical application cost and efficiency.

Part Number: **ISL6520CB**.

Additional Features:

- Operates from +5V Input.
- Drives N-Channel MOSFETs.
- Simple Single-Loop Control Design.
  - Voltage-Mode PWM Control.
- Fast Transient Response.
  - High-Bandwidth Error Amplifier.
  - Full 0% to 100% Duty Cycle.
- Loss less, Programmable Over-Current Protection.
  - Uses Upper MOSFETs rDS (on).
- Small Converter Size.
  - 300-KHz Fixed Frequency Oscillator.
- Internal Soft Start.
- 8 Ld SOIC or 16 Ld 4x4mm QFN.
- QFN Package.
  - Compliant to JEDEC PUB95 MO-220 QFN – Quad Flat No Leads – Package Outline.

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8.28 Serial Ports

Both serial ports can relocate to 480 different addresses with 13 IRQ options. By default, Port A appears at the front panel RJ-11C connector and Port B on the rear panel. Each serial port can be set to one of four different COM ports and can be enabled separately. When enabled, each port can be programmed to generate edge- or level-sensitive interrupts. When disabled, serial port interrupts are available to add-in boards.

8.29 Keyboard and Mouse

The Keyboard/Mouse controller is a PS/2 compatible device.

8.30 3-Volt Lithium Battery

The 3-Volt Lithium battery CR2032 manufactured by RENATA is the safest and most reliable Lithium battery system. The following features apply:

Additional Features:

- Operating temperature range: -20° C to +70° C.
- Nominal capacity (mAh): 235.
- Self-discharge: less than 1% per year at 25° C.
- Shelf Life: Up to 10 years at max 25° C.
- Stable voltage during shelf life.
- High reliability of operation, also regarding leakage resistance.
- Contains no heavy metals.

Note: If you need to replace the battery contact GMS Customer Service and give them the GMS Part Number 39/012A/W.

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8.31 Power Distribution

The power distribution block diagram for the V469 SBC is shown in Figure 7. Zoom to 150% for better clarity.

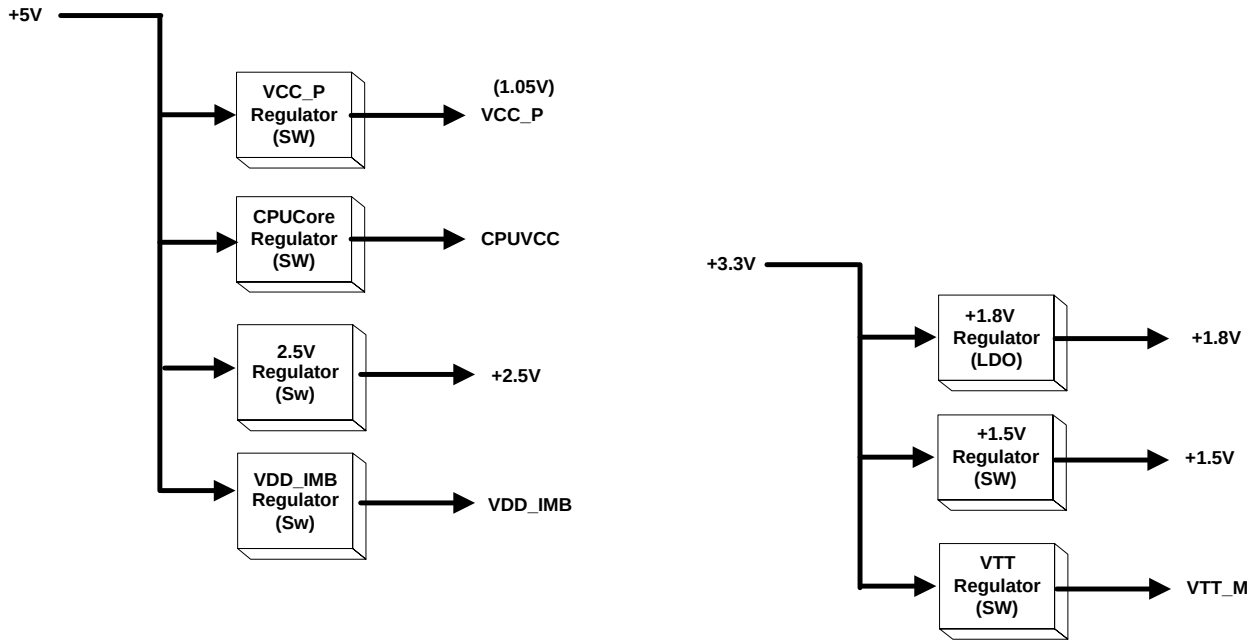


Figure 7. Power Distribution Block Diagram

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8.32 Heatsinks

The V469 has two passive heatsinks located on the board. Figure 8 is the processor heatsink (top and side view) and Figure 9 is the North Bridge (BGA) (top and side view).

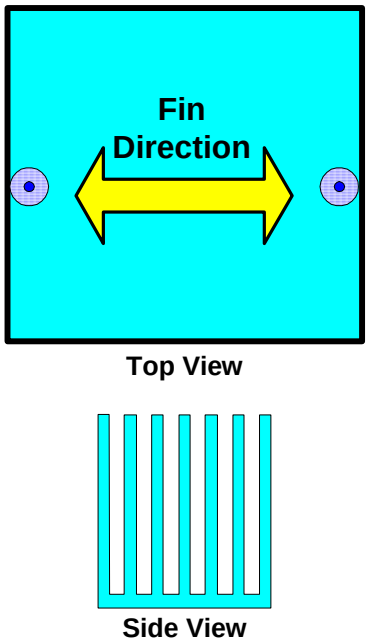


Figure 8. Passive Processor Heatsink Top/Side View

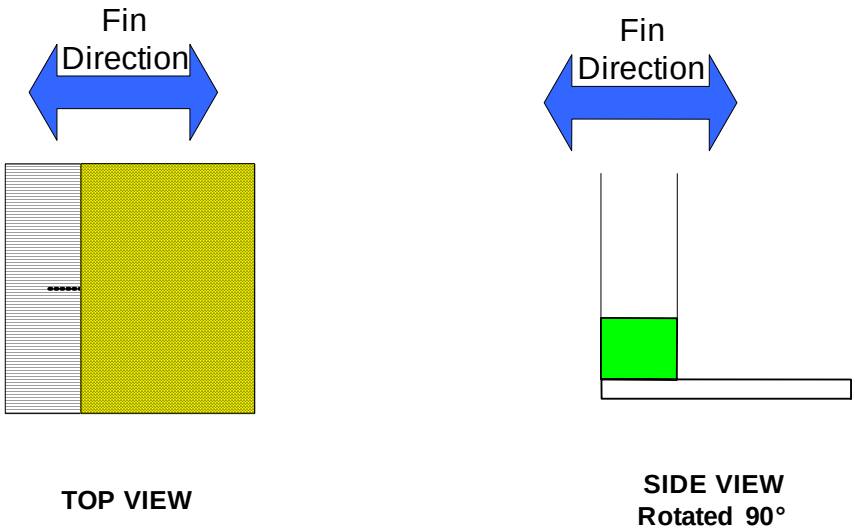


Figure 9. Passive North Bridge (BGA) Heatsink Top/Side View

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APPENDIX A

A.1 Front Panel

This section provides the V469 SBC Front Panel as shown in Figure 10. Zoom to 150% for clarity.

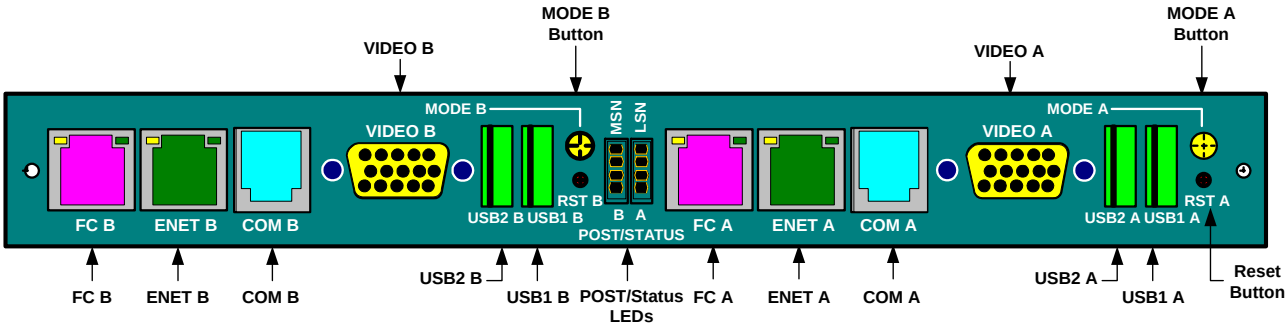


Figure 10. V469 SBC Front Panel

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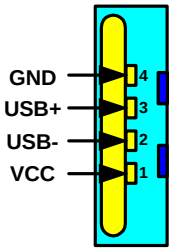
A.2 Connector Pin Assignments

This section provides the V469 System Board connector pin assignments. The tables that follow list the connector pin assignments. To read the pin assignments on the board, a number one (1) or a notch at the corner of the connector indicates pin one.

The following table lists the pin assignments for the **A-USB2 Connector J5.**

Pin #	Signal
1	AFPUSB2_PWR
2	AUSB20_D2-
3	AUSB20_D2+
4	AFPUSB2_GND
5	Chassis Ground
6	Chassis Ground
7	Chassis Ground

Table A.1. A-USB2 Connector J5 Pin Assignments



USB Connector

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The following table lists the pin assignments for the **A-SAM3 Connector J6.**

Pin #	Description	Pin #	Description
1	Ground	2	Ground
3	ABIMBD_R13	4	ABIMBCON_R
5	ABIMBD_R10	6	ABIMB
7	ABIMBD_R9	8	ABIMBD_R11
9	ABIMBD_R12	10	ABIMBD_R8
11	Ground	12	Ground
13	ABIMBD_R5	14	ABIMBCLK_R_P
15	ABIMBCLK_R_N	16	ABIMBD_R4
17	ABIMBD_R7	18	ABIMBD_R6
19	ABIMBD_R0	20	ABIMBD_R2
21	Ground	22	Ground
23	ABIMBD_3	24	ABIMBD_R1
25	ABIMBD_R14	26	ABIMBD_R15
27	Ground	28	+3.3 Volts
29	APS_PWRGD#	30	+3.3 Volts
31	APCIIRQ15#	32	+3.3 Volts
33	APCIIRQ14#	34	+3.3 Volts
35	APCIIRQ13#	36	Ground
37	APCIIRQ12#	38	APCICLK_IMBEXP
39	Ground	40	Ground
41	ABIMBD_T14	42	ABIMBD_T11
43	ABIMBD_T12	44	ABIMBD_T13
45	ABIMBPAR_T	46	ABIMBCLK_T_N
47	ABIMBCLK_T_P	48	ABIMBD_T7
49	Ground	50	Ground
51	ABIMBD_T1	52	ABIMBD_T8
53	ABIMBD_T0	54	ABIMBD_T2
55	ABIMBD_T6	56	ABIMBD_T9
57	ABIMBD_T5	58	ABIMBD_T3
59	Ground	60	Ground
61	ABIMBCON_T	62	ABIMBD_T15
63	ABIMBD_T4	64	ABIMBD_T10
65	Ground	66	No Connection
67	APCIRST#	68	No Connection
69	ARSB_SDA	70	+5 Volts
71	ARSB_SCL	72	+5 Volts
73	No Connection	74	+5 Volts
75	Ground	76	+5 Volts
77	Ground	78	Ground
79	Ground	80	Ground

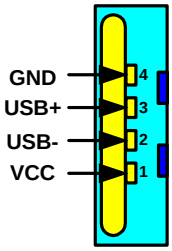
Table A.2. A-SAM-3 Expansion Bus Connector J6 Pin Assignments

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The following table lists the pin assignments for the **B-USB2 Connector J7.**

Pin #	Signal
1	BFPUSB2_PWR
2	BUSB20_D2-
3	BUSB20_D2+
4	BFPUSB2_GND
5	Chassis Ground
6	Chassis Ground
7	Chassis Ground

Table A.3. B-USB2 Connector J7 Pin Assignments



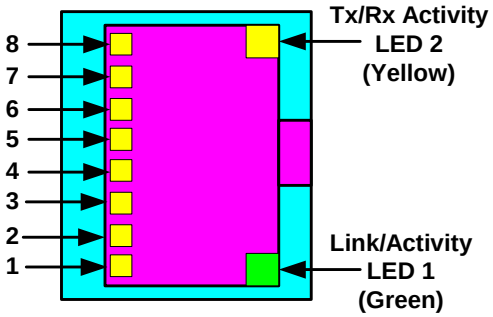
USB Connector

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The following table lists the pin assignments for the **A-ENET1 RJ-45 Connector J8.**

Pin #	Signal
1	AENET1_1
2	AENET1_2
3	AENET1_3
4	AENET1_4
5	AENET1_5
6	AENET1_6
7	AENET1_7
8	AENET1_8
9	AENET1_9
10	AENET1_10
D1	+3.3 Volts
D2	ALAN1_ACT#
D3	+3.3 Volts
D4	ALAN1_LINK#
S1	Shielded Ground
S2	Shielded Ground

Table A.4. A-ENET1 RJ-45 Connector J8 Pin Assignments



Ethernet RJ-45 Connector

Two LED's (LED1 - Green and LED2 Yellow) are integrated in each of the RJ-45 Connector. These LED's indicates the link status of the interface.

LED1 Green	Function
ON	Link
OFF	No Link

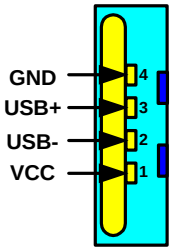
LED2 Yellow	Function
ON, Blink	Tx/Rx Activity
OFF	No Activity

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The following table lists the pin assignments for the **A-USB1 Connector J10.**

Pin #	Signal
1	AFPUSB1_PWR
2	AUSB20_D2-
3	AUSB20_D2+
4	AFPUSB1_GND
5	Chassis Ground
6	Chassis Ground
7	Chassis Ground

Table A.5. A-USB1 Connector J10 Pin Assignments



USB Connector

The following table lists the pin assignments for the **B-USB1 Connector J11.**

Pin #	Signal
1	AFPUSB1_PWR
2	AUSB20_D2-
3	AUSB20_D2+
4	AFPUSB1_GND
5	Chassis Ground
6	Chassis Ground
7	Chassis Ground

Table A.6. B-USB1 Connector J11 Pin Assignments

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The following table lists the pin assignments for the **Programming Header Connector J12.**

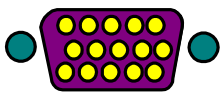
Pin #	Signal
1	BPLD_TCK
2	Ground
3	BPLD_TDO
4	+5 Volts
5	BPLD_TMS
6	No Connection
7	No Connection
8	No Connection
9	BPLD_TDI
10	Ground

Table A.7. Programming Header Connector J12 Pin Assignments

The following table lists the pin assignments for the **A-VGA Connector J13.**

Pin #	Signal
1	AVGA_Red
2	AVGA_Green
3	AVGA_Blue
4	AVGA_ID2
5	Ground
6	Ground
7	Ground
8	Ground
9	AVGA_PWR (+5 Volts)
10	Ground
11	AVGA_ID0
12	ADDC_DAT
13	AVGA_HSYNC
14	AVGA_VSYNC
15	ADDC_CLK

Table A.8. A-VGA Connector J13 Pin Assignments



Video Connector

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The following table lists the pin assignments for the **B-VGA Connector J14.**

Pin #	Signal
1	BVGA_Red
2	BVGA_Green
3	BVGA_Blue
4	BVGA_ID2
5	Ground
6	Ground
7	Ground
8	Ground
9	BVGA_PWR (+5 Volts)
10	Ground
11	BVGA_ID0
12	BDDC_DAT
13	BVGA_HSYNC
14	BVGA_VSYNC
15	BDDC_CLK

Table A.9. B-VGA Connector J14 Pin Assignments

The following table lists the pin assignments for the **A-COM1 RJ-45 Connector J15.**

Pin #	Signal
1	AFP_RTS0#
2	No Connection
3	AFP_TXD0
4	Ground
5	Ground
6	AFP_RXD0
7	No Connection (CTS)
8	AFP_CTS0#
9	S1 (Chassis Ground)
10	S2 (Chassis Ground)

Table A.10. A-COM1 RJ-45 Connector J15 Pin Assignments

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The following table lists the pin assignments for the **A-DDR Module Connector J17 part 1of 3.**

Pin #	Signal	Pin #	Signal
1	ASSTLREF_D1	2	ASSTLREF_D1
3	ABSD0_0	4	ABSD0_4
5	ABSD0_1	6	ABSD0_5
7	ABSD0_2	8	ABSD0_6
9	ABSD0_3	10	ABSD0_7
11	A-2.5 Volts	12	A-2.5 Volts
13	ABDQS0_0	14	ABDQS0_1
15	Ground	16	Ground
17	ABSD1_0	18	ABSD1_4
19	ABSD1_1	20	ABSD1_5
21	ABSD1_2	22	ABSD1_6
23	ABSD1_3	24	ABSD1_7
25	A-2.5 Volts	26	A-2.5 Volts
27	ABDQS1_0	28	ABDQS1_1
29	Ground	30	Ground
31	ABSD2_0	32	ABSD2_4
33	ABSD2_1	34	ABSD2_5
35	ABSD2_2	36	ABSD2_6
37	ABSD2_3	38	ABSD2_7
39	A-2.5 Volts	40	A-2.5 Volts
41	ABDQS2_0	42	ABDQS2_1
43	Ground	44	Ground
45	ABSD3_0	46	ABSD3_4
47	ABSD3_1	48	ABSD3_5
49	ABSD3_2	50	ABSD3_6
51	ABSD3_3	52	ABSD3_7
53	A-2.5 Volts	54	A-2.5 Volts
55	ABDQS3_0	56	ABDQS3_1
57	Ground	58	Ground
59	No Connection	60	No Connection
61	Ground	62	Ground
63	Ground	64	Ground

Table A.11. A-DDR Module Connector J17 Part 1 of 3 Pin Assignments

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The following table lists the pin assignments for the **A-DDR Module Connector J17 part 2of 3**.

Pin #	Signal	Pin #	Signal
61	ABSD8_0	62	ABSD8_4
63	ABSD8_1	64	ABSD8_5
65	ABSD8_2	66	ABSD8_6
67	ABSD8_3	68	ABSD8_7
69	A-2.5 Volts	70	A-2.5 Volts
71	ABDQS8_0	72	ABDQS8_1
73	Ground	74	Ground
75	ABMA0	76	ABMA4
77	ABMA1	78	ABMA5
79	ABMA2	80	ABMA6
81	ABMA3	82	ABMA7
83	A-2.5 Volts	84	A-2.5 Volts
85	ABMA8	86	ABMA12
87	ABMA9	88	ABMA13
89	ABMA10	90	ABMA14
91	ABMA11	92	No Connection
93	Ground	94	Ground
95	AB_CKE	96	AB_CKE
97	ABWE#	98	ABCS0#
99	ABRAS#	100	ABCS1#
101	ABCAS#	102	No Connection
103	A-2.5 Volts	104	A-2.5 Volts
105	ADCLK1	106	No Connection
107	ADCLK1#	108	No Connection
109	Ground	110	Ground
111	ACS2#	112	No Connection
113	ACS3#	114	No Connection
115	ACS4#	116	No Connection
117	ACS5#	118	No Connection
119	AMEMB_SCL	120	ADIMM_RST#
65	Ground	66	Ground
67	Ground	68	Ground

Table A.11. A-DDR Module Connector J17 Part 2 of 3 Pin Assignments

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The following table lists the pin assignments for the **A-DDR Module Connector J17 part 3of 3**.

Pin #	Signal	Pin #	Signal
121	AMEMB_SDA	122	AD3_SA1
123	AD3_SA2	124	AD3_SA0
125	ABSD4_0	126	ABSD4_4
127	ABSD4_1	128	ABSD4_5
129	ABSD4_2	130	ABSD4_6
131	ABSD4_3	132	ABSD4_7
133	A-2.5 Volts	134	A-2.5 Volts
135	ABDQS4_0	136	ABDQS4_1
137	Ground	138	Ground
139	ABSD5_0	140	ABSD5_4
141	ABSD5_1	142	ABSD5_5
143	ABSD5_2	144	ABSD5_6
145	ABSD5_3	146	ABSD5_7
147	A-2.5 Volts	148	A-2.5 Volts
149	ABDQS5_0	150	ABDQS5_1
151	Ground	152	Ground
153	ABSD6_0	154	ABSD6_4
155	ABSD6_1	156	ABSD6_5
157	ABSD6_2	158	ABSD6_6
159	ABSD6_3	160	ABSD6_7
161	A-2.5 Volts	162	A-2.5 Volts
163	ABDQS6_0	164	ABDQS6_1
165	Ground	166	Ground
167	ABSD7_0	168	ABSD7_4
169	ABSD7_1	170	ABSD7_5
171	ABSD7_2	172	ABSD7_6
173	ABSD7_3	174	ABSD7_7
175	A-2.5 Volts	176	A-2.5 Volts
177	ABDQS7_0	178	ABDQS7_1
179	Ground	180	Ground
69	Ground	G10	Ground
G11	Ground	G12	Ground

Table A.11. A-DDR Module Connector J17 Part 3 of 3 Pin Assignments

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The following table lists the pin assignments for the **A-DDR Module Connector J18 part 1of 3.**

Pin #	Signal	Pin #	Signal
1	ASSTLREF_D1	2	ASSTLREF_D1
3	AASD0_0	4	AASD0_4
5	AASD0_1	6	AASD0_5
7	AASD0_2	8	AASD0_6
9	AASD0_3	10	AASD0_7
11	A+2.5 Volts	12	A+2.5 Volts
13	AADQS0_0	14	AADQS0_1
15	Ground	16	Ground
17	AASD1_0	18	AASD1_4
19	AASD1_1	20	AASD1_5
21	AASD1_2	22	AASD1_6
23	AASD1_3	24	AASD1_7
25	A+2.5 Volts	26	A+2.5 Volts
27	AADQS1_0	28	AADQS1_1
29	Ground	30	Ground
31	AASD2_0	32	AASD2_4
33	AASD2_1	34	AASD2_5
35	AASD2_2	36	AASD2_6
37	AASD2_3	38	AASD2_7
39	A+2.5 Volts	40	A+2.5 Volts
41	AADQS2_0	42	AADQS2_1
43	Ground	44	Ground
45	AASD3_0	46	AASD3_4
47	AASD3_1	48	AASD3_5
49	AASD3_2	50	AASD3_6
51	AASD3_3	52	AASD3_7
53	A+2.5 Volts	54	A+2.5 Volts
55	AADQS3_0	56	AADQS3_1
57	Ground	58	Ground
59	No Connection	60	No Connection
61	Ground	62	Ground
63	Ground	64	Ground

Table A.12. A-DDR Module Connector J18 Part 1 of 3 Pin Assignments

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The following table lists the pin assignments for the **A-DDR Module Connector J18 part 2of 3**.

Pin #	Signal	Pin #	Signal
61	AASD8_0	62	AASD8_4
63	AASD8_1	64	AASD8_5
65	AASD8_2	66	AASD8_6
67	AASD8_3	68	AASD8_7
69	A+2.5 Volts	70	A+2.5 Volts
71	AADQS8_0	72	AADQS8_1
73	Ground	74	Ground
75	AAMA0	76	AAMA4
77	AAMA1	78	AAMA5
79	AAMA2	80	AAMA6
81	AAMA3	82	AAMA7
83	A+2.5 Volts	84	A+2.5 Volts
85	AAMA8	86	AAMA12
87	AAMA9	88	AAMA13
89	AAMA10	90	AAMA14
91	AAMA11	92	No Connection
93	Ground	94	Ground
95	AA_CKE	96	AA_CKE
97	AAWE#	98	AACS0#
99	AARAS#	100	AACS1#
101	AACAS#	102	No Connection
103	A+2.5 Volts	104	A+2.5 Volts
105	ADCLK3	106	No Connection
107	ADCLK3#	108	No Connection
109	Ground	110	Ground
111	No Connection	112	No Connection
113	No Connection	114	No Connection
115	No Connection	116	No Connection
117	No Connection	118	No Connection
119	AMEMA_SCL	120	ADIMM_RST#
65	Ground	66	Ground
67	Ground	68	Ground

Table A.12. A-DDR Module Connector J18 Part 2 of 3 Pin Assignments

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The following table lists the pin assignments for the **A-DDR Module Connector J18 part 3of 3**.

Pin #	Signal	Pin #	Signal
121	AMEMA_SDA	122	AD4_SA1
123	AD4_SA2	124	AD4_SA0
125	AASD4_0	126	AASD4_4
127	AASD4_1	128	AASD4_5
129	AASD4_2	130	AASD4_6
131	AASD4_3	132	AASD4_7
133	A+2.5 Volts	134	A+2.5 Volts
135	AADQS4_0	136	AADQS4_1
137	Ground	138	Ground
139	AASD5_0	140	AASD5_4
141	AASD5_1	142	AASD5_5
143	AASD5_2	144	AASD5_6
145	AASD5_3	146	AASD5_7
147	A+2.5 Volts	148	A+2.5 Volts
149	AADQS5_0	150	AADQS5_1
151	Ground	152	Ground
153	AASD6_0	154	AASD6_4
155	AASD6_1	156	AASD6_5
157	AASD6_2	158	AASD6_6
159	AASD6_3	160	AASD6_7
161	A+2.5 Volts	162	A+2.5 Volts
163	AADQS6_0	164	AADQS6_1
165	Ground	166	Ground
167	AASD7_0	168	AASD7_4
169	AASD7_1	170	AASD7_5
171	AASD7_2	172	AASD7_6
173	AASD7_3	174	AASD7_7
175	A+2.5 Volts	176	A+2.5 Volts
177	AADQS7_0	178	AADQS7_1
179	Ground	180	Ground
69	Ground	G10	Ground
G11	Ground	G12	Ground

Table A.12. A-DDR Module Connector J18 Part 3 of 3 Pin Assignments

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The following table lists the pin assignments for the **B-DDR Module Connector J19 part 1of 3.**

Pin #	Signal	Pin #	Signal
1	BSSTLREF_D1	2	BSSTLREF_D1
3	BBSD0_0	4	BBSD0_4
5	BBSD0_1	6	BBSD0_5
7	BBSD0_2	8	BBSD0_6
9	BBSD0_3	10	BBSD0_7
11	B+2.5 Volts	12	B+2.5 Volts
13	BBDQS0_0	14	BBDQS0_1
15	Ground	16	Ground
17	BBSD1_0	18	BBSD1_4
19	BBSD1_1	20	BBSD1_5
21	BBSD1_2	22	BBSD1_6
23	BBSD1_3	24	BBSD1_7
25	B+2.5 Volts	26	B+2.5 Volts
27	BBDQS1_0	28	BBDQS1_1
29	Ground	30	Ground
31	BBSD2_0	32	BBSD2_4
33	BBSD2_1	34	BBSD2_5
35	BBSD2_2	36	BBSD2_6
37	BBSD2_3	38	BBSD2_7
39	B+2.5 Volts	40	B+2.5 Volts
41	BBDQS2_0	42	BBDQS2_1
43	Ground	44	Ground
45	BBSD3_0	46	BBSD3_4
47	BBSD3_1	48	BBSD3_5
49	BBSD3_2	50	BBSD3_6
51	BBSD3_3	52	BBSD3_7
53	B+2.5 Volts	54	B+2.5 Volts
55	BBDQS3_0	56	BBDQS3_1
57	Ground	58	Ground
59	No Connection	60	No Connection
61	Ground	62	Ground
63	Ground	64	Ground

Table A.13. B-DDR Module Connector J19 Part 1 of 3 Pin Assignments

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The following table lists the pin assignments for the **B-DDR Module Connector J19 part 2of 3**.

Pin #	Signal	Pin #	Signal
61	BBSD8_0	62	BBSD8_4
63	BBSD8_1	64	BBSD8_5
65	BBSD8_2	66	BBSD8_6
67	BBSD8_3	68	BBSD8_7
69	B+2.5 Volts	70	B+2.5 Volts
71	BBDQS8_0	72	BBDQS8_1
73	Ground	74	Ground
75	BBMA0	76	BBMA4
77	BBMA1	78	BBMA5
79	BBMA2	80	BBMA6
81	BBMA3	82	BBMA7
83	B+2.5 Volts	84	B+2.5 Volts
85	BBMA8	86	BBMA12
87	BBMA9	88	BBMA13
89	BBMA10	90	BBMA14
91	BBMA11	92	No Connection
93	Ground	94	Ground
95	BB_CKE	96	BB_CKE
97	BBWE#	98	BBCS0#
99	BBRAS#	100	BBCS1#
101	BBCAS#	102	No Connection
103	B+2.5 Volts	104	B+2.5 Volts
105	BDCLK1	106	No Connection
107	BDCLK1#	108	No Connection
109	Ground	110	Ground
111	No Connection	112	No Connection
113	No Connection	114	No Connection
115	No Connection	116	No Connection
117	No Connection	118	No Connection
119	BMEMB_SCL	120	BDIMM_RST#
65	Ground	66	Ground
67	Ground	68	Ground

Table A.13. B-DDR Module Connector J19 Part 2 of 3 Pin Assignments

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The following table lists the pin assignments for the **B-DDR Module Connector J19 part 3of 3**.

Pin #	Signal	Pin #	Signal
121	BMEMB_SDA	122	BD3_SA1
123	BD3_SA2	124	BD3_SA0
125	BBSD4_0	126	BBSD4_4
127	BBSD4_1	128	BBSD4_5
129	BBSD4_2	130	BBSD4_6
131	BBSD4_3	132	BBSD4_7
133	B+2.5 Volts	134	B+2.5 Volts
135	BBDQS4_0	136	BBDQS4_1
137	Ground	138	Ground
139	BBSD5_0	140	BBSD5_4
141	BBSD5_1	142	BBSD5_5
143	BBSD5_2	144	BBSD5_6
145	BBSD5_3	146	BBSD5_7
147	B+2.5 Volts	148	B+2.5 Volts
149	BBDQS5_0	150	BBDQS5_1
151	Ground	152	Ground
153	BBSD6_0	154	BBSD6_4
155	BBSD6_1	156	BBSD6_5
157	BBSD6_2	158	BBSD6_6
159	BBSD6_3	160	BBSD6_7
161	B+2.5 Volts	162	B+2.5 Volts
163	BBDQS6_0	164	BBDQS6_1
165	Ground	166	Ground
167	BBSD7_0	168	BBSD7_4
169	BBSD7_1	170	BBSD7_5
171	BBSD7_2	172	BBSD7_6
173	BBSD7_3	174	BBSD7_7
175	B+2.5 Volts	176	B+2.5 Volts
177	BBDQS7_0	178	BBDQS7_1
179	Ground	180	Ground
69	Ground	G10	Ground
G11	Ground	G12	Ground

Table A.13. B-DDR Module Connector J19 Part 3 of 3 Pin Assignments

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The following table lists the pin assignments for the **B-DDR Module Connector J20 part 1of 3.**

Pin #	Signal	Pin #	Signal
1	BSSTLREF_D1	2	BSSTLREF_D1
3	BASD0_0	4	BASD0_4
5	BASD0_1	6	BASD0_5
7	BASD0_2	8	BASD0_6
9	BASD0_3	10	BASD0_7
11	B+2.5 Volts	12	B+2.5 Volts
13	BADQS0_0	14	BADQS0_1
15	Ground	16	Ground
17	BASD1_0	18	BASD1_4
19	BASD1_1	20	BASD1_5
21	BASD1_2	22	BASD1_6
23	BASD1_3	24	BASD1_7
25	B+2.5 Volts	26	B+2.5 Volts
27	BADQS1_0	28	BADQS1_1
29	Ground	30	Ground
31	BASD2_0	32	BASD2_4
33	BASD2_1	34	BASD2_5
35	BASD2_2	36	BASD2_6
37	BASD2_3	38	BASD2_7
39	B+2.5 Volts	40	B+2.5 Volts
41	BADQS2_0	42	BADQS2_1
43	Ground	44	Ground
45	BASD3_0	46	BASD3_4
47	BASD3_1	48	BASD3_5
49	BASD3_2	50	BASD3_6
51	BASD3_3	52	BASD3_7
53	B+2.5 Volts	54	B+2.5 Volts
55	BADQS3_0	56	BADQS3_1
57	Ground	58	Ground
59	No Connection	60	No Connection
61	Ground	62	Ground
63	Ground	64	Ground

Table A.14. B-DDR Module Connector J20 Part 1 of 3 Pin Assignments

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The following table lists the pin assignments for the **B-DDR Module Connector J20 part 2of 3**.

Pin #	Signal	Pin #	Signal
61	BASD8_0	62	BASD8_4
63	BASD8_1	64	BASD8_5
65	BASD8_2	66	BASD8_6
67	BASD8_3	68	BASD8_7
69	B+2.5 Volts	70	B+2.5 Volts
71	BADQS8_0	72	BADQS8_1
73	Ground	74	Ground
75	BAMA0	76	BAMA4
77	BAMA1	78	BAMA5
79	BAMA2	80	BAMA6
81	BAMA3	82	BAMA7
83	B+2.5 Volts	84	B+2.5 Volts
85	BAMA8	86	BAMA12
87	BAMA9	88	BAMA13
89	BAMA10	90	BAMA14
91	BAMA11	92	No Connection
93	Ground	94	Ground
95	BA_CKE	96	BA_CKE
97	BAWE#	98	BACS0#
99	BARAS#	100	BACS1#
101	BACAS#	102	No Connection
103	B+2.5 Volts	104	B+2.5 Volts
105	BDCLK3	106	No Connection
107	BDCLK3#	108	No Connection
109	Ground	110	Ground
111	No Connection	112	No Connection
113	No Connection	114	No Connection
115	No Connection	116	No Connection
117	No Connection	118	No Connection
119	BMEMA_SCL	120	BDIMM_RST#
65	Ground	66	Ground
67	Ground	68	Ground

Table A.14. B-DDR Module Connector J20 Part 2 of 3 Pin Assignments

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The following table lists the pin assignments for the **B-DDR Module Connector J20 part 3of 3**.

Pin #	Signal	Pin #	Signal
121	BMEMA_SDA	122	BD4_SA1
123	BD4_SA2	124	BD4_SA0
125	BASD4_0	126	BASD4_4
127	BASD4_1	128	BASD4_5
129	BASD4_2	130	BASD4_6
131	BASD4_3	132	BASD4_7
133	B+2.5 Volts	134	B+2.5 Volts
135	BADQS4_0	136	BADQS4_1
137	Ground	138	Ground
139	BASD5_0	140	BASD5_4
141	BASD5_1	142	BASD5_5
143	BASD5_2	144	BASD5_6
145	BASD5_3	146	BASD5_7
147	B+2.5 Volts	148	B+2.5 Volts
149	BADQS5_0	150	BADQS5_1
151	Ground	152	Ground
153	BASD6_0	154	BASD6_4
155	BASD6_1	156	BASD6_5
157	BASD6_2	158	BASD6_6
159	BASD6_3	160	BASD6_7
161	B+2.5 Volts	162	B+2.5 Volts
163	BADQS6_0	164	BADQS6_1
165	Ground	166	Ground
167	BASD7_0	168	BASD7_4
169	BASD7_1	170	BASD7_5
171	BASD7_2	172	BASD7_6
173	BASD7_3	174	BASD7_7
175	B+2.5 Volts	176	B+2.5 Volts
177	BADQS7_0	178	BADQS7_1
179	Ground	180	Ground
69	Ground	G10	Ground
G11	Ground	G12	Ground

Table A.14. B-DDR Module Connector J20 Part 3 of 3 Pin Assignments

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The following table lists the pin assignments for the **A-IDE Connector J22**.

Pin #	Signal	Pin #	Signal
1	+5 Volts	2	+5 Volts
3	AIDE_D0	4	AIDE_D1
5	AIDE_D2	6	AIDE_D3
7	AIDE_D4	8	AIDE_D5
9	AIDE_D6	10	AIDE_D7
11	Ground	12	Ground
13	AIDE_D8	14	AIDE_D9
15	AIDE_D10	16	AIDE_D11
17	AIDE_D12	18	AIDE_D13
19	AIDE_D14	20	AIDE_D15
21	+5 Volts	22	+5 Volts
23	AIDE_DREQ	24	AIDE_A0
25	AIDE_IOW#	26	AIDE_A1
27	AIDE_IOR#	28	AIDE_A2
29	Ground	30	Ground
31	AIDE_IORDY	32	AIDE_CS0#
33	AIDE_IRQ	34	AIDE_CS1#
35	AIDE_RST#	36	AIDE_DACK#
37	+3.3 Volts	38	+3.3 Volts
39	ALPC_AD0	40	ALPC_CLK_M
41	ALPC_AD1	42	ABRSTRDV#
43	ALPC_AD2	44	ALPC_DRQ#
45	Ground	46	Ground
47	ALPC_AD3	48	ALPC_FRAME#
49	AMIO_1	50	AMIO_3
51	AMIO_2	52	AMIO_4
53	+3.3 Volts	54	+3.3 Volts
55	AUSB20_D5-	56	AMIO_5
57	AUSB20_D5+	58	AMIO_6
59	Ground	60	Ground

Table A.15. A-IDE Connector J22 Pin Assignments

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The following table lists the pin assignments for the **B-COM1 RJ-45 Connector J24**.

Pin #	Signal
1	BFP_RTS0#
2	No Connection
3	AFP_TXD0
4	Ground
5	Ground
6	BFP_RXD0
7	No Connection (CTS)
8	BFP_CTS0#
9	S1 (Chassis Ground)
10	S2 (Chassis Ground)

Table A.16. B-COM1 RJ-45 Connector J24 Pin Assignments

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The following table lists the pin assignments for the **B-SAM-3 Connector J25**.

Pin #	Description	Pin #	Description
1	Ground	2	Ground
3	BIMBD_R13	4	BIMBCON_R
5	BIMBD_R10	6	BIMBPAR_R
7	BIMBD_R9	8	BIMBD_R11
9	BIMBD_R12	10	BIMBD_R8
11	Ground	12	Ground
13	BIMBD_R5	14	BIMBCLK_R_P
15	BBIMBCLK_R_N	16	BIMBD_R4
17	BIMBD_R7	18	BIMBD_R6
19	BIMBD_R0	20	BIMBD_R2
21	Ground	22	Ground
23	BIMBD_R3	24	BIMBD_R1
25	BIMBD_T15	26	BIMBD_T10
27	Ground	28	+3.3 Volts
29	PS_PWRGD#	30	+3.3 Volts
31	PCIIRQ15#	32	+3.3 Volts
33	PCIIRQ14#	34	+3.3 Volts
35	PCIIRQ13	36	Ground
37	PCIIRQ12#	38	PCICLK_IMBEXP
39	Ground	40	Ground
41	BIMBD_T14	42	BIMBD_T11
43	BIMBD_T12	44	BIMBD_T13
45	BIMPAR_T	46	BIMBCLK_T_N
47	BIMBCLK_T_P	48	BIMBD_T7
49	Ground	50	Ground
51	BIMBD_T1	52	BIMBD_T8
53	BIMBD_T0	54	BIMBD_T2
55	BIMBD_T6	56	BIMBD_T9
57	BIMBD_T5	58	BIMBD_T3
59	Ground	60	Ground
61	BIMBCON_T	62	BIMBD_R14
63	BIMBD_T4	64	BIMBD_R15
65	Ground	66	No Connection
67	PCIRST#	68	No Connection
69	RSB_SDA	70	+5 Volts
71	RSB_SCL	72	+5 Volts
73	No Connection	74	+5 Volts
75	Ground	76	+5 Volts
77	Ground	78	Ground
79	Ground	80	Ground

Table A.17. B-SAM-3 Expansion Bus Connector J25 Pin Assignments

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The following table lists the pin assignments for the **A-ENET2 RJ-45 Connector J26**.

Pin #	Signal
1	AENET2_1
2	AENET2_2
3	AENET2_3
4	AENET2_4
5	AENET2_5
6	AENET2_6
7	AENET2_7
8	AENET2_8
9	AENET2_9
10	AENET2_10
D1	+3.3 Volts
D2	ALAN2_ACT#
D3	+3.3 Volts
D4	ALAN2_LINK#
S1	Shielded Ground
S2	Shielded Ground

Table A.18. A-ENET2 RJ-45 Connector J26 Pin Assignments

The following table lists the pin assignments for the **B-ENET2 RJ-45 Connector J27**.

Pin #	Signal
1	BENET2_1
2	BENET2_2
3	BENET2_3
4	BENET2_4
5	BENET2_5
6	BENET2_6
7	BENET2_7
8	BENET2_8
9	BENET2_9
10	BENET2_10
D1	+3.3 Volts
D2	BLAN2_ACT#
D3	+3.3 Volts
D4	BLAN2_LINK#
S1	Shielded Ground
S2	Shielded Ground

Table A.19. B-ENET2 RJ-45 Connector J27 Pin Assignments

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The following table lists the pin assignments for the **B-IDE Connector J28**.

Pin #	Signal	Pin #	Signal
1	+5 Volts	2	+5 Volts
3	BIDE_D0	4	BIDE_D1
5	BIDE_D2	6	BIDE_D3
7	BIDE_D4	8	BIDE_D5
9	BIDE_D6	10	BIDE_D7
11	Ground	12	Ground
13	BIDE_D8	14	BIDE_D9
15	BIDE_D10	16	BIDE_D11
17	BIDE_D12	18	BIDE_D13
19	BIDE_D14	20	BIDE_D15
21	+5 Volts	22	+5 Volts
23	BIDE_DREQ	24	BIDE_A0
25	BIDE_IOW#	26	BIDE_A1
27	BIDE_IOR#	28	BIDE_A2
29	Ground	30	Ground
31	BIDE_IORDY	32	BIDE_CS0#
33	BIDE_IRQ	34	BIDE_CS1#
35	BIDE_RST#	36	BIDE_DACK#
37	+3.3 Volts	38	+3.3 Volts
39	BLPC_AD0	40	BLPC_CLK_M
41	BLPC_AD1	42	BBRSTRDV#
43	BLPC_AD2	44	BLPC_DRQ#
45	Ground	46	Ground
47	BLPC_AD3	48	BLPC_FRAME#
49	BMIO_1	50	BMIO_3
51	BMIO_2	52	BMIO_4
53	+3.3 Volts	54	+3.3 Volts
55	BUSB20_D5-	56	BMIO_5
57	BUSB20_D5+	58	BMIO_6
59	Ground	60	Ground

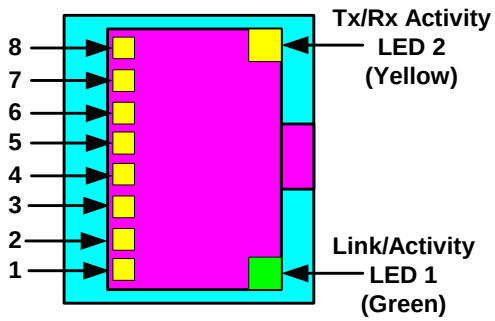
Table A.20. B-IDE Connector J28 Pin Assignments

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The following table lists the pin assignments for the **B-ENET1 RJ-45 Connector J29.**

Pin #	Signal
1	BENET1_1
2	BENET1_2
3	BENET1_3
4	BENET1_4
5	BENET1_5
6	BENET1_6
7	BENET1_7
8	BENET1_8
9	BENET1_9
10	BENET1_10
D1	+3.3 Volts
D2	BLAN1_ACT#
D3	+3.3 Volts
D4	BLAN1_LINK#
S1	Shielded Ground
S2	Shielded Ground

Table A.21. B-ENET1 RJ-45 Connector J29 Pin Assignments



Ethernet RJ-45 Connector

Two LED's (LED1 - Green and LED2 Yellow) are integrated in each of the RJ-45 Connector. These LED's indicates the link status of the interface.

LED1 Green	Function
ON	Link
OFF	No Link

LED2 Yellow	Function
ON, Blink	Tx/Rx Activity
OFF	No Activity

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The following table lists the pin assignments for the **VME P0 VITA 41.3 Connector J23.**

Pin #	Row A	Row B	Row C	Row D	Row E	Row F	Row G
1	A_MDI1+	A_MDI1-	Ground	A_MDI0+	A_MDI0-	Ground	NC
2	Ground	A_MDI3+	A_MDI3-	Ground	A_MDI2+	A_MDI2-	Ground
3	B_MDI1+	B_MDI1-	Ground	B_MDI0+	B_MDI0-	Ground	NC
4	Ground	B_MDI3+	B_MDI3-	Ground	B_MDI2+	B_MDI2-	Ground
5	Reserved	Reserved	Ground	Reserved	Reserved	Ground	Reserved
6	Ground	Reserved	Reserved	Ground	Reserved	Reserved	Ground
7	Reserved	Reserved	Ground	Reserved	Reserved	Ground	Reserved
8	Ground	Reserved	Reserved	Ground	Reserved	Reserved	Ground
9	Reserved	Reserved	Ground	Reserved	Reserved	Ground	Reserved
10	Ground	Reserved	Reserved	Ground	Reserved	Reserved	Ground
11	Reserved	Reserved	Ground	Reserved	Reserved	Ground	NC
12	Ground	NC	NC	Ground	NC	NC	Ground
13	NC	NC	Ground	NC	NC	Ground	NC
14	Ground	NC	NC	Ground	NC	NC	Ground
15	NC	NC	Ground	NC	NC	Ground	NC

Table A.22. VME P0 VITA 41.3 J23 Connector Pin Assignments

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The following table lists the pin assignments for the **VME P1 Connector.**

Pin #	Row Z	Row A	Row B	Row C	Row D
1	No Connection	No Connection	No Connection	No Connection	No Connection
2	Ground	No Connection	No Connection	No Connection	Ground
3	No Connection	No Connection	No Connection	No Connection	No Connection
4	Ground	No Connection	No Connection	No Connection	No Connection
5	No Connection	No Connection	No Connection	No Connection	No Connection
6	Ground	No Connection	No Connection	No Connection	No Connection
7	No Connection	No Connection	No Connection	No Connection	No Connection
8	Ground	No Connection	No Connection	No Connection	No Connection
9	No Connection	Ground	No Connection	Ground	VME_GAP#
10	Ground	No Connection	No Connection	No Connection	VME_GA0#
11	No Connection	Ground	No Connection	No Connection	VME_GA1#
12	Ground	No Connection	No Connection	No Connection	+3.3V
13	No Connection	No Connection	No Connection	No Connection	VME_GA2#
14	Ground	No Connection	No Connection	No Connection	+3.3V
15	No Connection	Ground	No Connection	No Connection	VME_GA3#
16	Ground	No Connection	No Connection	No Connection	+3.3V
17	No Connection	Ground	No Connection	No Connection	VME_GA4#
18	Ground	No Connection	No Connection	No Connection	+3.3V
19	No Connection	Ground	No Connection	No Connection	No Connection
20	Ground	No Connection	Ground	No Connection	+3.3V
21	No Connection	No Connection	No Connection	No Connection	No Connection
22	Ground	No Connection	No Connection	No Connection	+3.3V
23	No Connection	No Connection	Ground	No Connection	No Connection
24	Ground	No Connection	No Connection	No Connection	+3.3V
25	No Connection	No Connection	No Connection	No Connection	No Connection
26	Ground	No Connection	No Connection	No Connection	+3.3V
27	No Connection	No Connection	No Connection	No Connection	No Connection
28	Ground	No Connection	No Connection	No Connection	+3.3V
29	No Connection	No Connection	No Connection	No Connection	No Connection
30	Ground	No Connection	No Connection	No Connection	+3.3V
31	No Connection	-12 Volts	No Connection	+12 Volts	Ground
32	Ground	+5 Volts	+5 Volts	+5 Volts	No Connection

Table A.23. VME P1 Connector Pin Assignments

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The following table lists the pin assignments for the **VME P2 Connector.**

Pin #	Row Z	Row A	Row B	Row C	Row D
1	EXTBAT	BSIDE_D0	+5 Volts	BSIDE_D8	No Connection
2	Ground	BSIDE_D1	Ground	BSIDE_D9	No Connection
3	BMIO_1	BSIDE_D2	No Connection	BSIDE_D10	No Connection
4	Ground	BSIDE_D3	No Connection	BSIDE_D11	No Connection
5	BMIO_2	BSIDE_D4	No Connection	BSIDE_D12	No Connection
6	Ground	BSIDE_D5	No Connection	BSIDE_D13	No Connection
7	BMIO_3	BSIDE_D6	No Connection	BSIDE_D14	No Connection
8	Ground	BSIDE_D7	No Connection	BSIDE_D15	No Connection
9	BMIO_4	BSIDE_DRQ	No Connection	No Connection	BSIDE_IOR#
10	Ground	BSIDE_IORDY#	No Connection	BUSB20_PPON3	BSIDE_IOW#
11	BMIO_5	BSIDE_IRQ	No Connection	BUSB20_PPON4	BSIDE_CS1#
12	Ground	BTX_2	Ground	BUSB20_D3-	BSIDE_CS3#
13	BMIO_6	BRX2	+5 Volts	BUSB20_D3+	BSIDE_DACK#
14	Ground	BRTS2#	No Connection	BUSB20_D4-	BSIDE_A0
15	No Connection	BCTS2#	No Connection	BUSB20_D4+	BSIDE_A1
16	Ground	No Connection	No Connection	No Connection	BSIDE_A2
17	No Connection	ASDE_D0	No Connection	ASIDE_D8	No Connection
18	Ground	ASDE_D1	No Connection	ASIDE_D9	No Connection
19	No Connection	ASDE_D2	No Connection	ASIDE_D10	No Connection
20	Ground	ASIDE_D3	No Connection	ASIDE_D11	No Connection
21	AMIO_1	ASIDE_D4	No Connection	ASIDE_D12	No Connection
22	Ground	ASIDE_D5	Ground	ASIDE_D13	No Connection
23	AMIO_2	ASIDE_D6	No Connection	ASIDE_D14	ASIDE_IOR#
24	Ground	ASIDE_D7	No Connection	ASIDE_D15	ASIDE_IOW#
25	AMIO_3	ASIDE_DRQ	No Connection	No Connection	ASIDE_CS1#
26	Ground	ASIDE_IORDY#	No Connection	AUSB20_PPON3	ASIDE_CS3#
27	AMIO_4	ASIDE_IRQ	No Connection	AUSB20_PPON4	ASIDE_DACK#
28	Ground	ATX_2	No Connection	AUSB20_D3-	ASIDE_A0
29	AMIO_5	ARX2	No Connection	AUSB20_D3+	ASIDE_A1
30	Ground	ARTS2#	No Connection	AUSB20_D4-	ASIDE_A2
31	AMIO_6	ACTS2#	Ground	AUSB20_D4+	Ground
32	Ground	No Connection	+5 Volts	No Connection	VPC-3

Table A.24. VME P2 Connector Pin Assignments

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APPENDIX B

B.1 Rear Transition Module

The V469 SBC Rear Transition Module is shown in Figure 11.



Figure 11. Rear Transition Module

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The V469 SBC Rear Transition Module Block Diagram is shown in Figure 12.

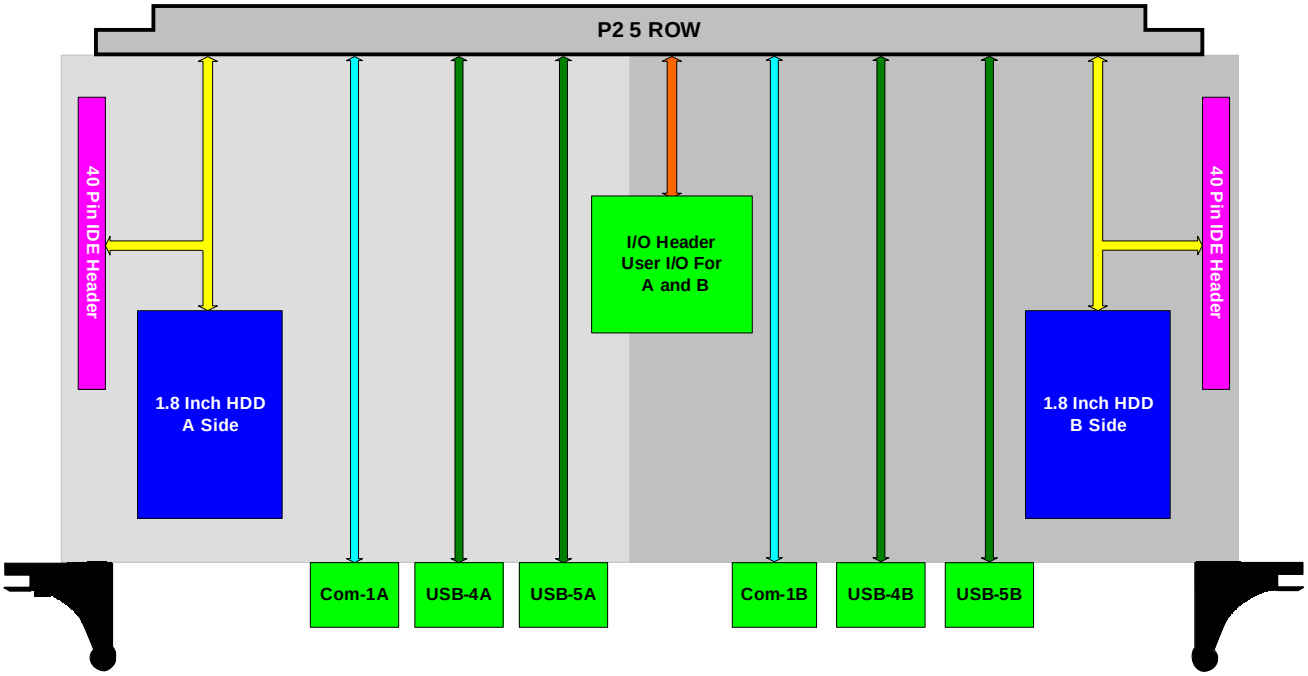


Figure 12. Rear Transition Module Block Diagram

The V469 SBC Rear Transition Module Front Panel is shown in Figure 13.

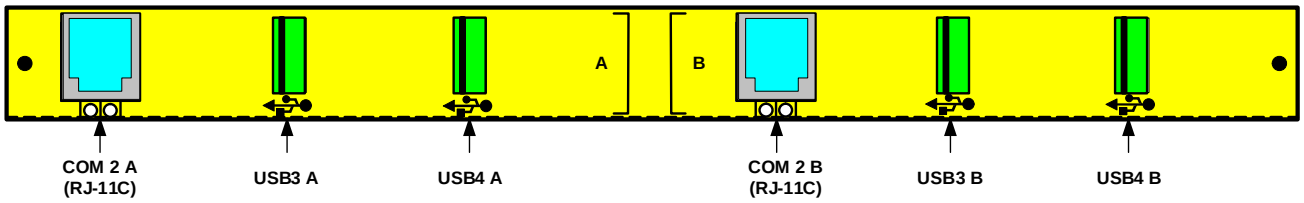


Figure 13. Rear Transition Module Front Panel

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B.2 Rear Transition Module Pin Assignments

This section provides the V469 SBC Rear Transition Module connector pin assignments. The tables that follow list the connector pin assignments. To read the pin assignments on the board, a number one (1) or a notch at the corner of the connector indicates pin one.

The following table lists the pin assignments for the **VME J2 Connector.**

Pin #	Row A	Row B	Row C	Row D	Row Z
1	BIDE_D0	+5 Volts	BSIDE_D8	No Connection	EXTBAT
2	BIDE_D1	Ground	BSIDE_D9	No Connection	Ground
3	BIDE_D2	No Connection	BSIDE_D10	No Connection	BMIO_1
4	BIDE_D3	No Connection	BSIDE_D11	No Connection	Ground
5	BIDE_D4	No Connection	BSIDE_D12	No Connection	BMIO_2
6	BIDE_D5	No Connection	BSIDE_D13	No Connection	Ground
7	BIDE_D6	No Connection	BSIDE_D14	No Connection	BMIO_3
8	BIDE_D7	No Connection	BSIDE_D15	No Connection	Ground
9	BIDE_DREQ	No Connection	No Connection	BSIDE_IOR#	BMIO_4
10	BIDE_IORDY	No Connection	BUSB20_PP0N3	BSIDE_IOW#	Ground
11	BIDE_IRQ	Ground	No Connection	BSIDE_CS1#	BMIO_5
12	BTX2	No Connection	BUSB20_D3-	BSIDE_CS3#	Ground
13	BRX2	No Connection	BUSB20_D3+	BSIDE_DACK#	BMIO_6
14	BRTS2#	No Connection	BUSB20_D4-	BSIDE_A0	Ground
15	BCTS2#	No Connection	BUSB20_D4+	BSIDE_A1	No Connection
16	No Connection	No Connection	No Connection	BSIDE_A2	Ground
17	ASIDE_D0	No Connection	ASIDE_D8	No Connection	No Connection
18	ASIDE_D1	No Connection	ASIDE_D9	No Connection	Ground
19	ASIDE_D2	No Connection	ASIDE_D10	No Connection	No Connection
20	ASIDE_D3	+5 Volts	ASIDE_D11	No Connection	Ground
21	ASIDE_D4	Ground	ASIDE_D12	No Connection	AMI0_1
22	ASIDE_D5	No Connection	ASIDE_D13	No Connection	Ground
23	ASIDE_D6	No Connection	ASIDE_D14	ASIDE_IOR#	AMI0_2
24	ASIDE_D7	No Connection	ASIDE_D15	ASIDE_IOW#	Ground
25	ASIDE_DREQ	No Connection	No Connection	ASIDE_CS1#	AMI0_3
26	ASIDE_IORDY	No Connection	AUSB20_PP0N3	ASIDE_CS3#	Ground
27	ASIDE_IRQ	No Connection	No Connection	ASIDE_DACK#	AMI0_4
28	ATX2	No Connection	AUSB20_D3-	ASIDE_A0	Ground
29	ARX2	No Connection	AUSB20_D3+	ASIDE_A1	AMI0_5
30	ARTS2#	No Connection	AUSB20_D4-	ASIDE_A2	Ground
31	ACTS2#	Ground	AUSB20_D4+	Ground	AMI0_6
32	No Connection	+5 Volts	No Connection	No Connection	Ground

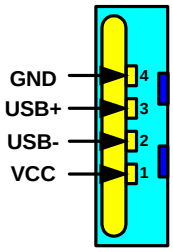
Table B.1. Rear Transition Module VME Connector J2 Pin Assignments

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The following table lists the pin assignments for the **B-USB4 Connector.**

Pin #	USB Signal
1	BUSB4_GND
2	BUSB20_D4+
3	BUSB20_D4-
4	BUSB4_PWR
5	CGND
6	CGND
7	CGND

Table B.2. Rear Transition Module B-USB4 Connector J3 Pin Assignments



USB Connector

The following table lists the pin assignments for the **B-USB3 Connector.**

Pin #	USB Signal
1	BUSB3_GND
2	BUSB20_D3+
3	BUSB20_D3-
4	BUSB3_PWR
5	CGND
6	CGND
7	CGND

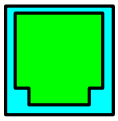
Table B.3. Rear Transition Module BUSB3 Connector J4 Pin Assignments

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The following table lists the pin assignments for the **B-COM2 (RJ-11C) Connector.**

Pin #	Signal
1	BRJ11_RTS2#
2	BRJ11_TXD2
3	Ground
4	Ground
5	BRJ11_RXD2
6	BRJ11_CTS2#
S1	Chassis Ground
S2	Chassis Ground

Table B.4. Rear Transition Module B-COM2 (RJ-11C) Connector J5 Pin Assignments

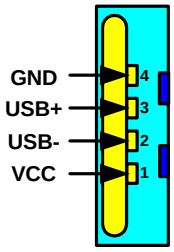


RJ-11C Connector

The following table lists the pin assignments for the **A-USB4 Connector.**

Pin #	USB Signal
1	AUSB4_GND
2	AUSB20_D4+
3	AUSB20_D4-
4	AUSB4_PWR
5	CGND
6	CGND
7	CGND

Table B.5. Rear Transition Module A-USB4 Connector J6 Pin Assignments



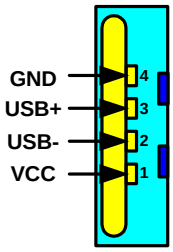
USB Connector

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The following table lists the pin assignments for the **A-USB3 Connector.**

Pin #	USB Signal
1	AUSB3_GND
2	AUSB20_D3+
3	AUSB20_D3-
4	AUSB3_PWR
5	CGND
6	CGND
7	CGND

Table B.6. Rear Transition Module A-USB3 Connector J7 Pin Assignments

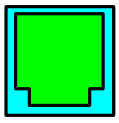


USB Connector

The following table lists the pin assignments for the **A-COM2 (RJ-11C) Connector.**

Pin #	Signal
1	ARJ11_RTS2#
2	ARJ11_TXD2
3	Ground
4	Ground
5	ARJ11_RXD2
6	ARJ11_CTS2#
S1	Chassis Ground
S2	Chassis Ground

Table B.7. Rear Transition Module A-COM2 (RJ-11C) Connector J8 Pin Assignments



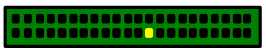
RJ-11C Connector

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The following table lists the pin assignments for the **B-IDE (44-Pin) Connector.**

Pin #	Signal	Pin #	Signal
A	B_IDE_PINA	B	B_IDE_PINB
C	B_IDE_PINC	D	B_IDE_PIND
E	No Connection	F	No Connection
1	B_IDE_RST#	2	Ground
3	B_IDE_D07	4	B_IDE_D08
5	B_IDE_D06	6	B_IDE_D09
7	B_IDE_D05	8	B_IDE_D10
9	B_IDE_D04	10	B_IDE_D11
11	B_IDE_D03	12	B_IDE_D12
13	B_IDE_D02	14	B_IDE_D13
15	B_IDE_D01	16	B_IDE_D14
17	B_IDE_D00	18	B_IDE_D15
19	Ground	20	No Connection (Key)
21	B_IDE_DREQ	22	Ground
23	B_IDE_DIOW#	24	Ground
25	B_IDE_DIOR#	26	Ground
27	B_IDE_IORDY	28	Ground
29	B_IDE_DACK#	30	Ground
31	B_IDE_IRQ	32	No Connection
33	B_IDE_DA1	34	BPDIAG#
35	B_IDE_DA0	36	B_IDE_DA2
37	B_IDE_CS0#	38	B_IDE_CS1#
39	B_IDE_LED#	40	Ground
41	BSIDEPWR_L	42	BSIDEPWR_M
43	Ground	44	No Connection

Table B.8. Rear Transition Module B-IDE Connector J9 Pin Assignments



IDE
(44-Pin)
Connector

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The following table lists the pin assignments for the **B-IDE (40-Pin) Connector.**

Pin #	Signal	Pin #	Signal
1	B_IDE_RST#	2	Ground
3	B_IDE_D07	4	B_IDE_D08
5	B_IDE_D06	6	B_IDE_D09
7	B_IDE_D05	8	B_IDE_D10
9	B_IDE_D04	10	B_IDE_D11
11	B_IDE_D03	12	B_IDE_D12
13	B_IDE_D02	14	B_IDE_D13
15	B_IDE_D01	16	B_IDE_D14
17	B_IDE_D00	18	B_IDE_D15
19	Ground	20	No Connection (Key)
21	B_IDE_DREQ	22	Ground
23	B_IDE_DIOW#	24	Ground
25	B_IDE_DIOR#	26	Ground
27	B_IDE_IORDY	28	Ground
29	B_IDE_DACK#	30	Ground
31	B_IDE_IRQ	32	No Connection
33	B_IDE_DA1	34	BPDIAG#
35	B_IDE_DA0	36	B_IDE_DA2
37	B_IDE_CS0#	38	B_IDE_CS1#
39	B_IDE_LED#	40	Ground

Table B.9. Rear Transition Module B-IDE Connector J10 Pin Assignments



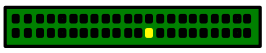
IDE
(40-Pin)
Connector

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The following table lists the pin assignments for the **A-IDE (44-Pin) Connector.**

Pin #	Signal	Pin #	Signal
A	A_IDE_PINA	B	A_IDE_PINB
C	A_IDE_PINC	D	A_IDE_PIND
E	No Connection	F	No Connection
1	A_IDE_RST#	2	Ground
3	A_IDE_D07	4	A_IDE_D08
5	A_IDE_D06	6	A_IDE_D09
7	A_IDE_D05	8	A_IDE_D10
9	A_IDE_D04	10	A_IDE_D11
11	A_IDE_D03	12	A_IDE_D12
13	A_IDE_D02	14	A_IDE_D13
15	A_IDE_D01	16	A_IDE_D14
17	A_IDE_D00	18	A_IDE_D15
19	Ground	20	No Connection (Key)
21	A_IDE_DREQ	22	Ground
23	A_IDE_DIOW#	24	Ground
25	A_IDE_DIOR#	26	Ground
27	A_IDE_IORDY	28	Ground
29	A_IDE_DACK#	30	Ground
31	A_IDE_IRQ	32	No Connection
33	A_IDE_DA1	34	APDIAG#
35	A_IDE_DA0	36	A_IDE_DA2
37	A_IDE_CS0#	38	A_IDE_CS1#
39	A_IDE_LED#	40	Ground
41	ASIDEPWR_L	42	ASIDEPWR_M
43	Ground	44	No Connection

Table B.10. Rear Transition Module A-IDE Connector J11 Pin Assignments



IDE
(44-Pin)
Connector

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The following table lists the pin assignments for the **A-IDE (40-Pin) Connector.**

Pin #	Signal	Pin #	Signal
1	A_IDE_RST#	2	Ground
3	A_IDE_D07	4	A_IDE_D08
5	A_IDE_D06	6	A_IDE_D09
7	A_IDE_D05	8	A_IDE_D10
9	A_IDE_D04	10	A_IDE_D11
11	A_IDE_D03	12	A_IDE_D12
13	A_IDE_D02	14	A_IDE_D13
15	A_IDE_D01	16	A_IDE_D14
17	A_IDE_D00	18	A_IDE_D15
19	Ground	20	No Connection (Key)
21	A_IDE_DREQ	22	Ground
23	A_IDE_DIOW#	24	Ground
25	A_IDE_DIOR#	26	Ground
27	A_IDE_IORDY	28	Ground
29	A_IDE_DACK#	30	Ground
31	A_IDE_IRQ	32	No Connection
33	A_IDE_DA1	34	APDIAG#
35	A_IDE_DA0	36	A_IDE_DA2
37	A_IDE_CS0#	38	A_IDE_CS1#
39	A_IDE_LED#	40	Ground

Table B.11. Rear Transition Module A-IDE Connector J12 Pin Assignments



IDE
(40-Pin)
Connector

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The following table lists the pin assignments for the **PIM Jn4 Mezzanine User I/O Connector.**

Pin #	Signal	Pin #	Signal
1	Ground	2	No Connection
3	BMI0_1	4	No Connection
5	Ground	6	No Connection
7	BMI0_2	8	No Connection
9	Ground	10	No Connection
11	BMI0_3	12	No Connection
13	Ground	14	No Connection
15	BMI0_4	16	No Connection
17	Ground	18	No Connection
19	BMI0_5	20	No Connection
21	Ground	22	No Connection
23	BMI0_6	24	No Connection
25	Ground	26	No Connection
27	No Connection	28	No Connection
29	Ground	30	No Connection
31	No Connection	32	No Connection
33	Ground	34	No Connection
35	No Connection	36	No Connection
37	Ground	38	No Connection
39	No Connection	40	No Connection
41	Ground	42	No Connection
43	AMI0_1	44	No Connection
45	Ground	46	No Connection
47	AMI0_2	48	No Connection
49	Ground	50	No Connection
51	AMI0_3	52	No Connection
53	Ground	54	No Connection
55	AMI0_4	56	No Connection
57	Ground	58	No Connection
59	AMI0_5	60	No Connection
61	Ground	62	No Connection
63	AMI0_6	64	No Connection

Table B.12. Rear Transition Module PIM Jn4 Mezzanine User I/O Connector J13 Pin Assignments

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APPENDIX C

C.1 Default Jumper Settings

This section provides information on the default jumper settings, and how to change them. A notched corner of the jumper socket represents pin one.

Default Jumper Descriptions			
Reference Designator	**Default Setting**	**Purpose/Description**	**Board Side**
W1		POST LED A Switch	**A**
W2		POST LED B Switch	**B**
W3	**IN**	BRST_SW: **IN = Enable**, OUT = Disabled	**B**
W4	**IN**	CPLD B Identify	**B**
W5	**IN**	ARST_SW: **IN = Enable**, OUT = Disabled	**A**
W6	**OUT**	CPLD A Identify	**A**
W7	**IN**	IMB-A Termination: **IN = Enable**, OUT Disabled	**A**
W8	**1-2**	Flash A Boot Protect: **1-2 = Normal**, 2-3 = Allow Boot Block Prog	**A**
W9	**IN**	IMB-B Termination: **IN = Enabled**, OUT = Disabled	**B**
W10	**1-2**	Flash B Boot Protect: **1-2 = Normal**, 2-3 = Allow Boot Block Prog	**B**
W11	**1-2**	CMOS Clear: **1-2 = Normal**, 2-3 = CMOS Clear	**A**
W12	**1-2**	CMOS Clear: **1-2 = Normal**, 2-3 = CMOS Clear	**B**

Note: Default configuration is indicated by **BOLD** type.

Table C.1. Default Jumper Settings

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APPENDIX D

D.1 POST/Status LEDs

The POST/STATUS LEDs are located in the center of the front panel for Side A and Side B as shown in Table D.1, D.2, and Figure 13.

Table D.1 lists the POST/Status LEDs Common Circuits for the V469 SBC A-Side.

Pin #	POST LEDS – Status A
1	POSTLED_7
2	POSTLED_6
3	POSTLED_5
4	POSTLED_4
5	+3.3 Volts
6	+3.3 Volts
7	APFLED_RED (User G/Y)
8	AUSERLED_T (Pass/Fail)

Table D.1. A-POST/Status LED Common Circuits

Table D.2 lists the POST/Status LEDs Common Circuits for the V469 SBC B-Side.

Pin #	POST LEDS – Status B
1	POSTLED_3
2	POSTLED_2
3	POSTLED_1
4	POSTLED_0
5	+3.3 Volts
6	+3.3 Volts
7	BPFLED_RED (User/G/Y)
8	BUSERLED_T (Pass/Fail)

Table D.2. B-POST/Status LED Common Circuits

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Figure 14 shows the POST/Status A and B LEDs.

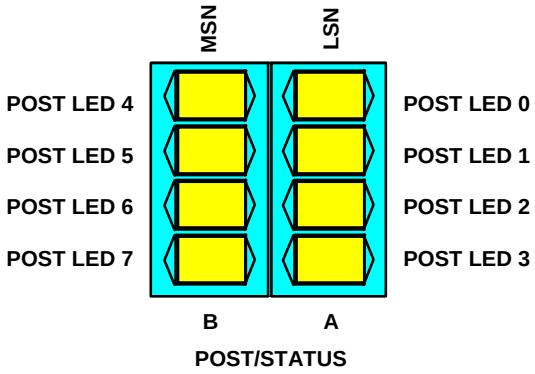


Figure 14. POST/STATUS A and B LEDs (on Front Panel)

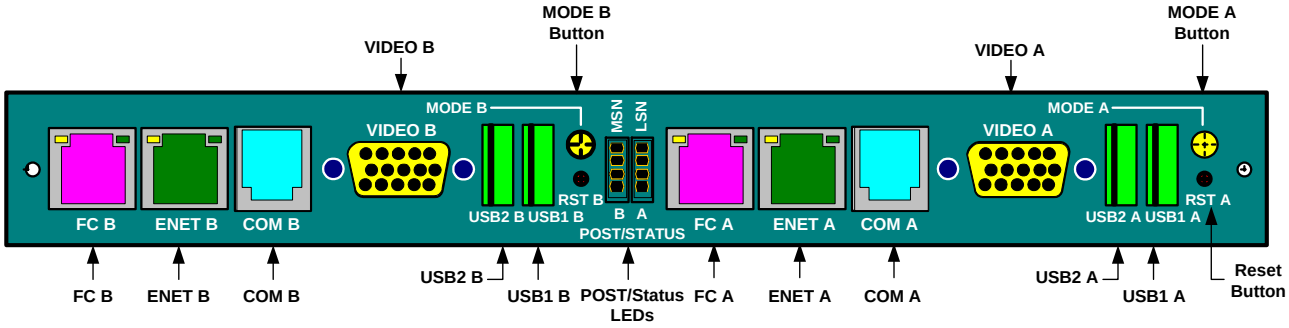
Note:
MSN = Most Significant Nibble.
LSN = Least Significant Nibble.

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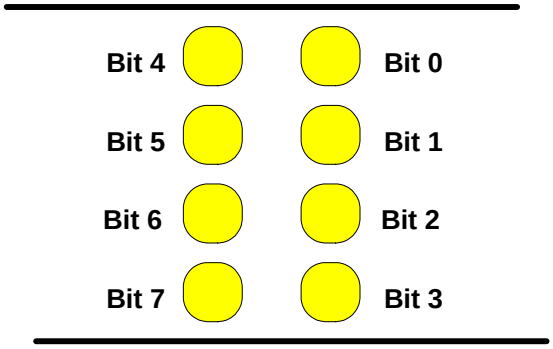
D.2 LED Description and Procedures

The following describes the operation and definition of the front panel LEDs on the V469 SBC.

The front panel is divided in two parts. The right has the peripheral connectors for CPU A, while the left has the connectors for CPU B. The LEDs are shared between the two CPUs. When POST display is enabled, the 8 LEDs display the POST codes for the CPU selected. During normal operation, the 4 right LEDs are the status for CPU A, while the 4 left LEDs are status for CPU B. See below for a detailed description.



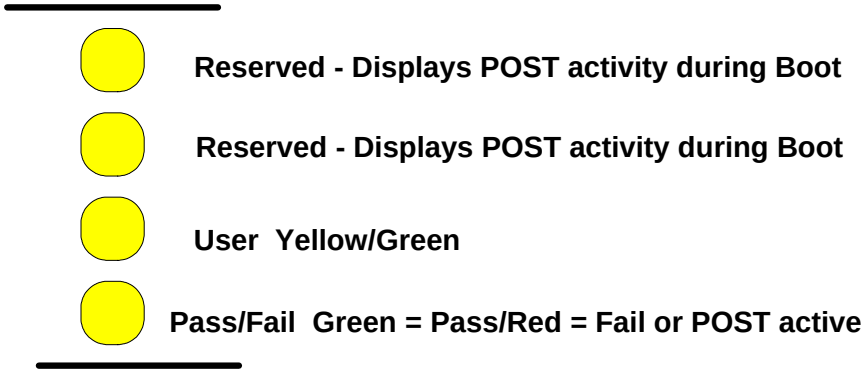
1. **POST** Display
   - Pres MODE A button during power on to display the POST codes for CPU A
   - Pres MODE B button during power on to display the POST codes for CPU B



Power Cycle is required to change the LEDs mode.

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2. **Status** Display (no MODE buttons pressed)
If neither MODE button is pressed, the LEDs default to the following status for each CPU.



The Pass fail LED will be initially Red and turn Green when POST successfully passes.

The User LED is controlled by I/O Port 78 bits 5 & 6. Port 78 must be read before setting any bits to keep the other bits in the same state. The following describes the user LED Port 78 settings.

Port 78 Bit 6	Port 78 Bit 5	User LED
0	0	Off (Default)
0	1	Green
1	0	Yellow
1	1	Off

The two top LEDs are reserved for future use. They will currently display POST activity to give a visual indication that POST is active for that CPU.

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D.3 Ethernet Default Configuration and Ethernet VITA41 Configuration

The Ethernet Default and Ethernet VITA41 Configurations are shown in Figure 15 and 16.

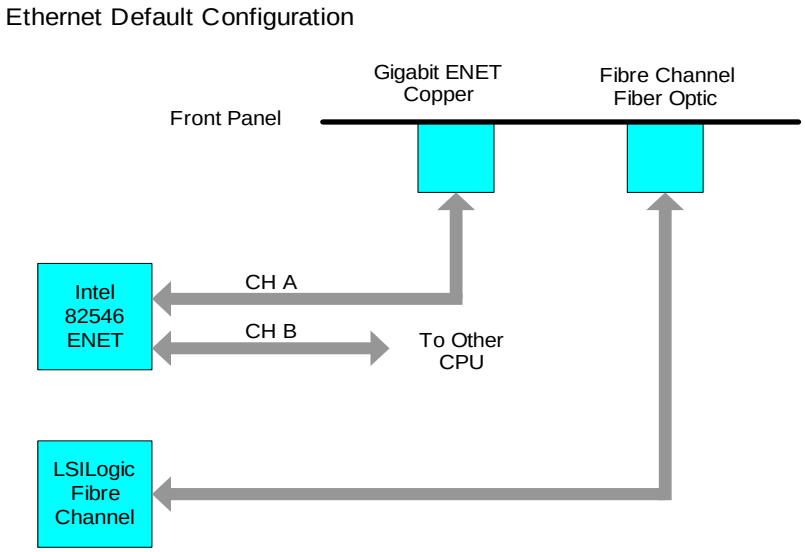


Figure 15. Ethernet Default Configuration

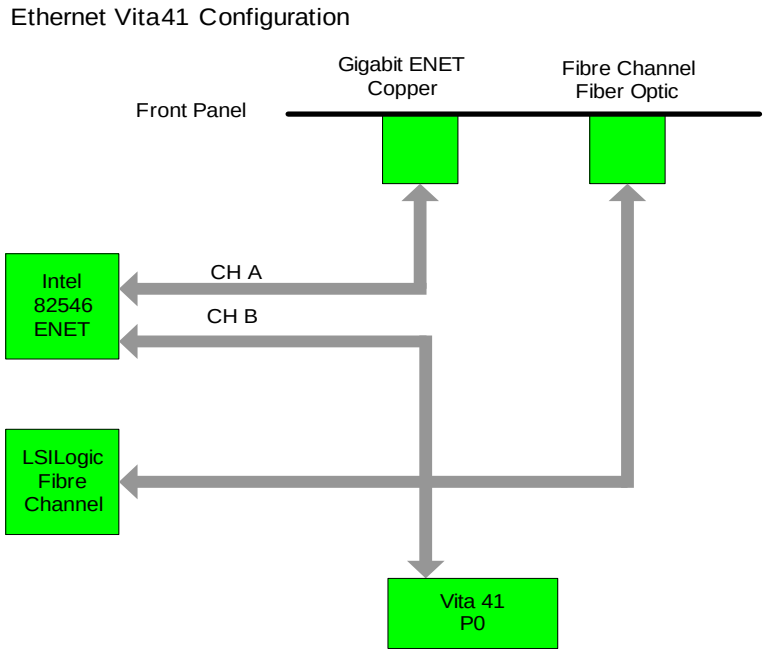


Figure 16. Ethernet VITA41 Configuration

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D.4. BIOS

The following tables will assist you in understanding the BIOS checkpoints generated by AMIBIOS.

D.4.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS.

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4-GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512-KB memory. Adjust policies and cache first 8-MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* table D.4 for more information.
D7	Restore CPUID value back into register. The Bootblock Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1-MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* table D.5 for more information.

Table D.3. BIOS Bootblock Initialization Code Checkpoints

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D.4.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS.

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
E9 or EA	Determine information about root directory of recovery media.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

Table D.4. Bootblock Recovery Code Checkpoints

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D.4.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS.

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, run-time data area. Also, initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags".
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock".
C0	Early CPU Init Start - - Disable Cache – Init Local APIC.
C1	Set up boot strap processor Information.
C2	Set up boot strap processor for POST.
C5	Enumerate and set up application processors.
C6	Re-enable cache for boot strap processor.
C7	Early CPU Init Exit.
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS module.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See *DIM Code Checkpoints* D.6 for further information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that has optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.

(Continued on next page)

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33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* D.6 for more information.
39	Initializes DMAC – 1 & DMAC – 2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU,…etc. successfully installed in the system and update the BDA, EBDA…etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initializes Int-13 and prepare for IPL detections.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed/requested.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported).
8E	Program the peripheral parameters. Enable/Disable NMI as selected.
90	Late POST initialization of system management interrupts.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of run-time image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the run-time language module. Disables the system configuration display if needed.
A4	Initialize run-time language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for INT 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

Table D.5. POST Code Checkpoints

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D.4.4 DIM Code Checkpoints

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different BUSes. The following table describes the main checkpoints where the DIM module is accessed.

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals; memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

Table D.6. DIM Code Checkpoints

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed.
'X' can be from 0 to 7.

- 0 = func#0, disable all devices on the BUS concerned.
- 1 = func#1, static devices initialization on the BUS concerned.
- 2 = func#2, output device initialization on the BUS concerned.
- 3 = func#3, input device initialization on the BUS concerned.
- 4 = func#4, IPL device initialization on the BUS concerned.
- 5 = func#5, general device initialization on the BUS concerned.
- 6 = func#6, error reporting for the BUS concerned.
- 7 = func#7, add-on ROM initialization for all BUSes.
- 8 = func#8, BBS ROM initialization for all BUSes.

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The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

- 0 = Generic DIM (Device Initialization Manager).
- 1 = On-board System devices.
- 2 = ISA devices.
- 3 = EISA devices.
- 4 = ISA PnP devices.
- 5 = PCI devices.

D.4.5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events.

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01,02,03,04,05	Entering sleep state S1, S2, S3, S4, and S5.
10,20,30,40,50	Waking from sleep state S1, S2, S3, S4, and S5.

Table D.7. ACPI Runtime Checkpoints

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APPENDIX E

E.1 Installing Operating Systems using Fibre Channel

Windows

Windows installation requires drivers to be installed when using devices like Fibre Channel Hard Drive.

1. Locate the Fibre Channel driver folder on the CD that comes with your SBC.
2. Open either Windows 2000 or XP folder and copy all the files and folders to a Floppy Disk.
3. Insert the disk into drive "A" that's connected to your SBC.
4. Power up the SBC.
5. Immediately as one boots to a Windows Installation Disk, the prompt to press is the F6 key to install the Third Party drivers, Press F6.
6. After pressing F6, Windows continues installing the needed software before asking for the driver.
7. Once the driver is read, Windows is able to access the Fibre Channel device.

REDHAT 9.0

REDHAT 9.0 does not require the driver; it is included in its install files.

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APPENDIX F

F.1 Making Hardware Upgrades or Changes – General Procedure

The general procedure for making hardware upgrades or changes to the board can be accomplished using the following procedures:

1. **Observe the safety and ESD precautions.** The V469 contains static sensitive electronic components. Industry standard precautions and procedures for ESD should be followed when handling the V469 or any of its components.
2. Turn off all connected peripherals, turn off system power, and disconnect the AC power cord.
3. Remove the V469 from the card cage by withdrawing the securing screws, and pressing the two card extractor levers outward until the board disconnects from the backplane connectors.
4. For changing a configuration setting, locate the configuration jumper to be changed on the System board or Rear Transition Module, and move the jumpers to pins specified for the desired setting. For all other changes, follow the installation/removal procedure provided with the item to be installed or removed.
5. Reinstall the V469 in the card cage (by pressing the board straight in until the levers snap into the latched position) and then tighten the securing screws.
6. Connect the power cord, and turn on the system for the change to take effect.

However, if something is wrong with your V469, refer to your warranty and contact the GMS Technical Support for assistance at **fae@gms4sbc.com,** or phone support at (909) 980-4863 from 8:00 A.M. to 5:00 P.M. Pacific Standard Time (PST).

Number	Date	Edited by	Hardware Upgrade or Change Description
1			
2			
3			

Table F.1. Hardware Upgrades or Changes

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APPENDIX G

G.1 Document – Revision History

Table G.1 is used to monitor and document all revisions of the V469 User Manual.

Revision	Date	Edited by	Changes
A	12/16/05	DO	User Manual
B	06/21/06	DO	User Manual
B	07/21/06	DO	User Manual
B	07/10/07	DO	User Manual

Table G.1. Document – Revision History

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