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High Performance Bus Interface Solutions

Rev: 092009

PMC-12AISS8AO4

12-Channel 12-Bit PMC Analog Input/Output Board

Eight Simultaneously-Sampled Wide-Range Inputs at 2.0 MSPS per Channel, Four Analog Outputs, and 16-Bit Digital I/O Port

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

The single-width PCI mezzanine card PMC-12AISS8AO4 provides 12-bit analog input and output capability for PMC applications. Eight analog input channels (Figure 1.1-1) are digitized simultaneously at rates up to 2,000,000 conversions per second per channel, with software-controlled voltage ranges of ±10V, ±1V or ±100mV. Digitized input data is buffered through a 64 K-sample FIFO.

Four 12-bit analog output channels provide software-selected output ranges of ±10V, ±5V or ±2.5V, and are accessed directly through dedicated control registers. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

The board is designed for minimum off-line maintenance. All functional parameters are under software control, thereby eliminating field-configuration jumpers. A selftest switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host.

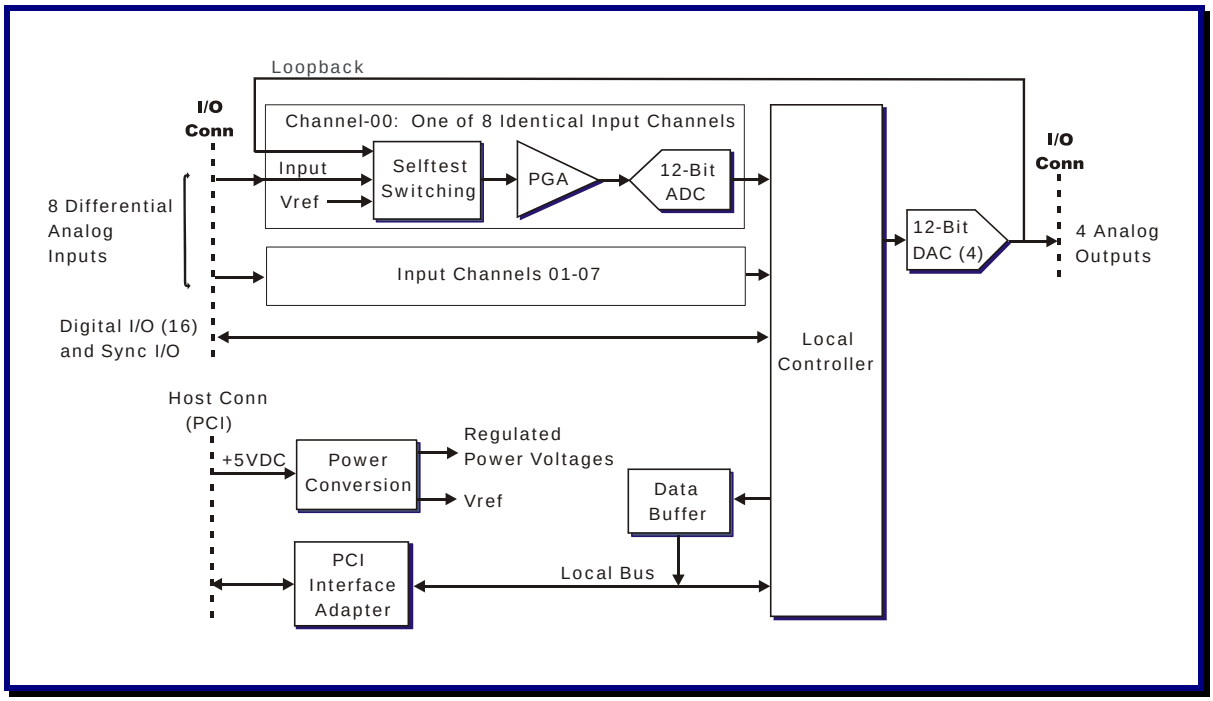


Figure 1.1-1. Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Electrical power is derived from +5VDC supplied by the PCI bus, and analog power voltages are generated internally. Universal signaling is supported, and all operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional convection cooling.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 PMC Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel (Figure 2.2-1). Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs are seated against the host board.

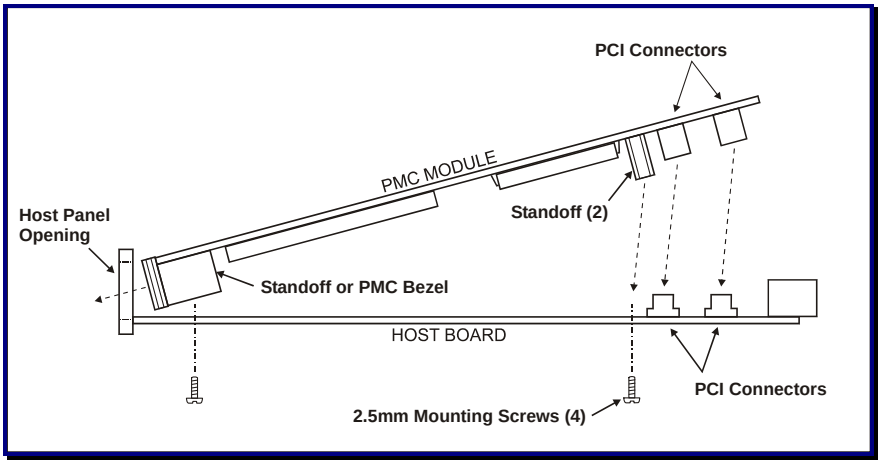


Figure 2.2-1: PMC Physical Installation

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-080-S-TG. The insulation displacement (IDC) Robinson Nugent connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-2. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connector Pin Functions

PIN	ROW-A SIGNAL
1	OUTPUT RTN
2	ANA OUT 00
3	OUTPUT RTN
4	ANA OUT 01
5	OUTPUT RTN
6	ANA OUT 02
7	OUTPUT RTN
8	ANA OUT 03
9	INPUT RTN
10	INPUT RTN
11	INP00 LO
12	INP00 HI
13	INPUT RTN
14	INPUT RTN
15	INP01 LO
16	INP01 HI
17	INPUT RTN
18	INPUT RTN
19	INP02 LO
20	INP02 HI
21	INPUT RTN
22	INPUT RTN
23	INP03 LO
24	INP03 HI
25	INPUT RTN
26	INPUT RTN
27	INP04 LO
28	INP04 HI
29	INPUT RTN
30	INPUT RTN
31	INP05 LO
32	INP05 HI
33	INPUT RTN
34	INPUT RTN
35	INP06 LO
36	INP06 HI
37	INPUT RTN
38	INPUT RTN
39	INP07 LO
40	INP07 HI

PIN	ROW-B SIGNAL
1	DIGITAL RTN
2	DIO 00
3	DIGITAL RTN
4	DIO 01
5	DIGITAL RTN
6	DIO 02
7	DIGITAL RTN
8	DIO 03
9	DIGITAL RTN
10	DIO 04
11	DIGITAL RTN
12	DIO 05
13	DIGITAL RTN
14	DIO 06
15	DIGITAL RTN
16	DIO 07
17	DIGITAL RTN
18	DIO 08
19	DIGITAL RTN
20	DIO 09
21	DIGITAL RTN
22	DIO 10
23	DIGITAL RTN
24	DIO 11
25	DIGITAL RTN
26	DIO 12
27	DIGITAL RTN
28	DIO 13
29	DIGITAL RTN
30	DIO 14
31	DIGITAL RTN
32	DIO 15
33	VTEST RTN
34	VTEST
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	INPUT TRIG I/O
39	DIGITAL RTN
40	INPUT CLK I/O

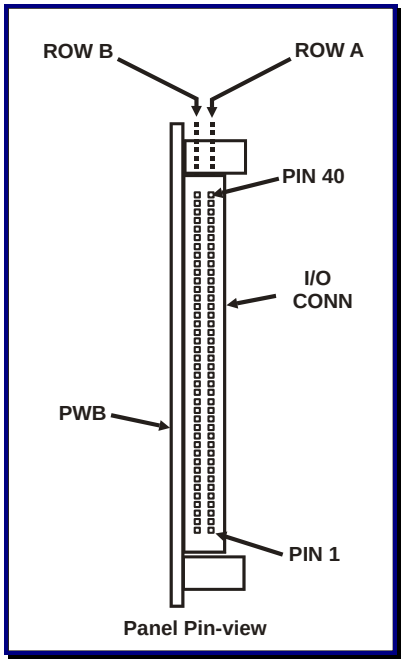


Figure 2.2-2. System I/O Connector

2.3 System Configuration

2.3.1 Analog Inputs

The eight analog input channels can be configured for either differential or single-ended operation. The hardware input configuration must be acknowledged by the control software.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

This operating mode also offers the highest rejection of the common mode noise that is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode, shown in Figure 2.3-1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point that ensures that the sum of the signal level **(Vsig)** and the common mode voltage **(Vcm)** remains within the range specified for the board. Ground current through the INPUT RTN line must be limited in order to avoid damage to the cable or the input board.

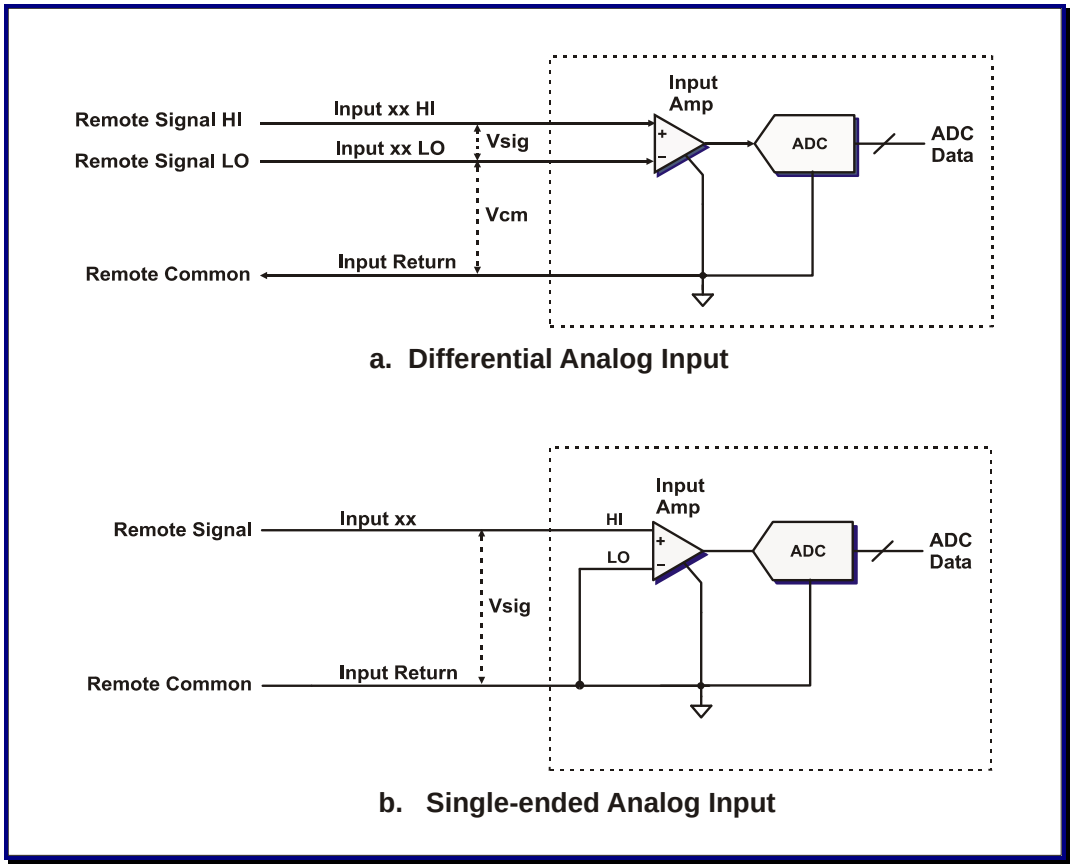


Figure 2.3-1. Analog Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1b) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. A single-ended configuration usually is more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or may generate potentially destructive ground current.

For applications in which multiple signal sources share a single ground point, the differential configuration is recommended, with all "LO" inputs connected together at the common remote return.

2.3.2 Analog Outputs

2.3.2.1 Output Configurations

The four analog output channels are single-ended and have a common signal return that is referred to in Table 2.2-1 as OUTPUT RTN. Single-ended outputs should drive only loads that have a high impedance to system ground. The best results are obtained when the loads are isolated also from each other.

Figure 2.3-2 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2.3-2a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads with a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

If the load return is connected to a remote system ground (Figure 2.3-2b), the potential difference **Vgnd** between the remote ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current Ignd developed in the return line is limited essentially only by **Rgnd**, and can damage the cable or the board if not controlled.

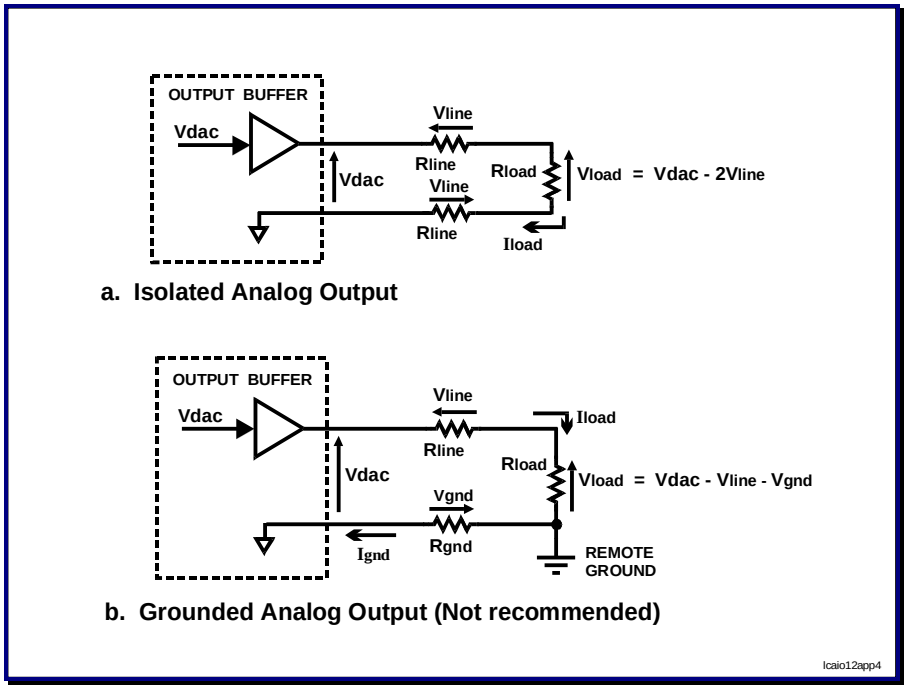


Figure 2.3-2. Output Configurations

2.3.2.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate or heavy loads. Figure 2.3-3 shows the effect of load current on the voltage drop in copper wire of various sizes. A 4.0 milliamp load for example, inserts a voltage drop of more than 0.25 millivolt *per foot* in #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors, especially in a 12-bit system, in which 1 LSB may represent

only 1.2 millivolts on a ±2.5 Volt range. High impedance loads generally do not produce significant DC errors.

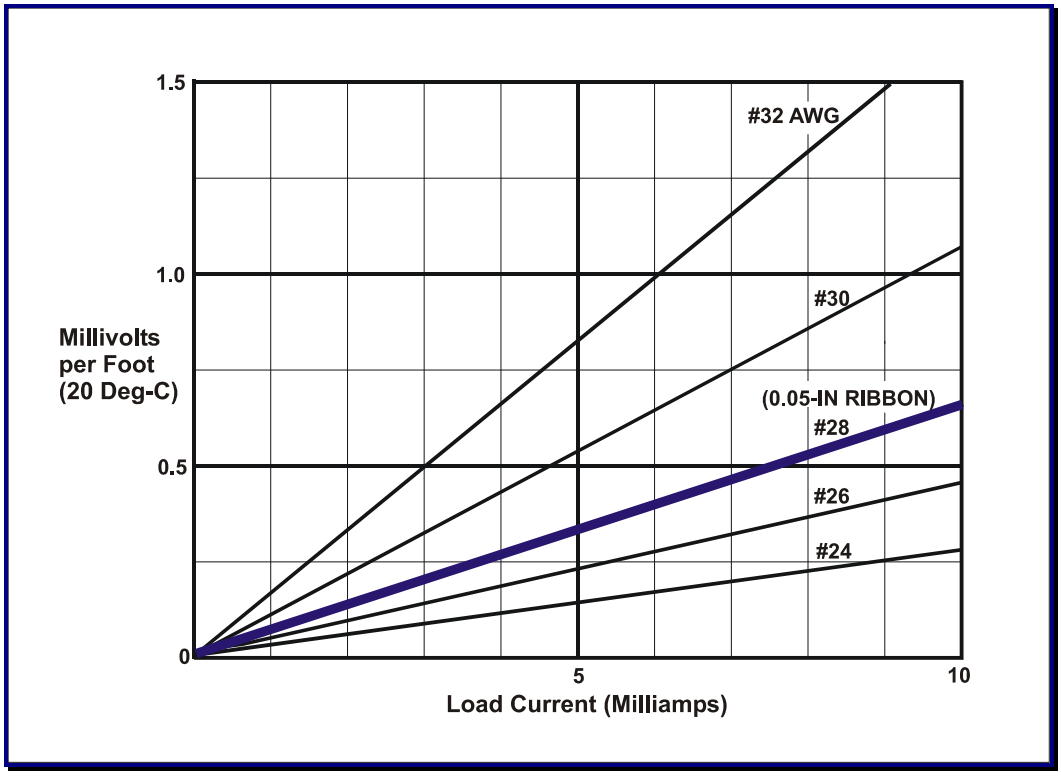


Figure 2.3-3. Line Loss Versus Load Current

2.3.3 External Sync I/O

The INPUT CLK I/O, INPUT TRIG I/O and OUTPUT CLK I/O pins in the system connector are bidirectional TTL synchronization signals that provide external control of analog input sampling and analog output clocking. Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

When a board is software-configured as an *Initiator*, these I/O signals are outputs that can be used to control multiple *Target* boards. Each clock or trigger event output consists of a 100 nanosecond TTL pulse, asserted LOW. Output loading in the Initiator configuration should be limited to 10 milliamps or less.

For Target boards, the I/O signals become inputs and can synchronize input and output operations to an Initiator board. All three inputs are asserted LOW, and are pulled up internally to +5V through approximately 33 KOhms.

2.3.4 Multiboard Synchronization

If multiple boards are to be synchronized together, the INPUT CLK I/O, INPUT TRIG I/O and OUTPUT CLK I/O pins from one board, the ***initiator***, are connected to the corresponding pins of as many as four ***target*** boards in the same backplane (Figure 2.3-4). The controlling software determines specific synchronization functions.

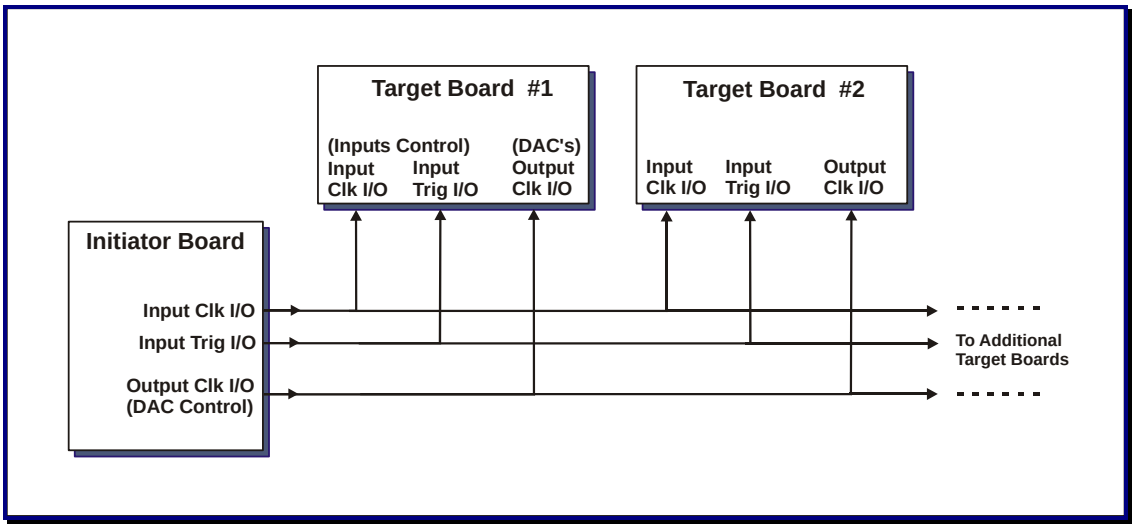


Figure 2.3-4. Multiboard Synchronization

2.4 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the internal voltage reference. The optimum verification interval will vary with upon the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog channels are software-calibrated to a single internal voltage reference by an embedded autocalibration utility. The procedure presented here describes the verification and adjustment of the reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to the system I/O connector.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the internal voltage reference. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1.

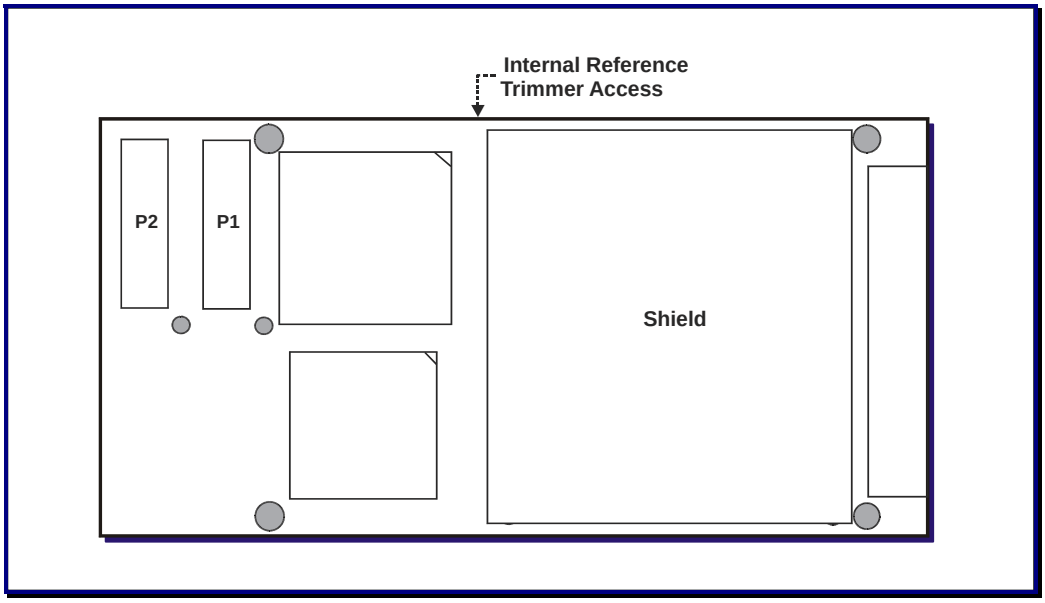


Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the PMC is installed on a host board, and that the host is installed in a system.

1. Connect the digital multimeter between the VTEST pin (+), and the VTEST RTN pin (-) in the System I/O connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is +9.9000 VDC ±0.0015 VDC. If the indication is not within this range, adjust the internal reference trimmer for an in-range digital multimeter indication.
4. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC-12AISS8AO4 board is compatible with the PCI Local Bus specification Revision 2.3, and supports auto configuration at the time of power-up. A PLX™ PCI-9080 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All data transfers are long-word D32. Several predefined interrupt conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer.

To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero), and maintenance registers should not be modified.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	ACCESS MODE [1]	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL	RW	2302 00A0h	Board Control Register (BCR)
0004	DIGITAL I/O PORT	RW	00XX 00XXh	16-Bit Digital I/O port data
0008	ANALOG OUTPUT CHAN 00	RW	0000 0800h	Output Channel 00 data
000C	ANALOG OUTPUT CHAN 01	RW	0000 0800h	Output Channel 01 data
0010	ANALOG OUTPUT CHAN 02	RW	0000 0800h	Output Channel 02 data
0014	ANALOG OUTPUT CHAN 03	RW	0000 0800h	Output Channel 03 data
0018	ANALOG INPUT DATA	RO	00XX XXXXh	Analog input buffer data
001C	RATE GENERATOR A	RW	0000 0140h	Rate-A generator divisor
0020	RATE GENERATOR B	RW	0000 3E80h	Rate-B generator divisor
0024	INPUT CONFIGURATION	RW	FF00 0400h	Analog inputs channel-mask and burst-size
0028	INPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the input buffer
002C	INPUT BUFFER THRESHOLD	RW	0000 FFFEh	Input buffer status flag threshold
0030	INTERRUPT CONTROL	RW	0000 0000h	Interrupt control/status register
0034	Board Configuration [2]	RO	000X XXXXh	Firmware revision and option straps
0038	Autocal Values [2]	RW	0000 XXXXh	Autocal value readback
003C	Auxiliary R/W Register [3]	RW	0000 0000h	Auxiliary register. No internal function.
0040-7F	(Reserved)	---	---	Inactive

Notes: 1. RW = Read/Write, RO = Read-Only.
2. Maintenance register; Shown for reference only.
3. Lower 16 bits (D00-D15) are active; upper 16 bits are all-zero.

3.2 Board Control Register (BCR)

Basic board functions such as initialization, autocalibration and input/output range selection are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset. PCI register configuration terminates with the PCI interrupts disabled (Section 3.11).

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked,
- Analog input and output ranges are ±10V,
- Analog data coding format is offset binary,
- External clock and trigger signals are in the initiator (output) mode,
- Analog Inputs:
  - Input channels are differential, and all are active,
  - Sample clocking is from the Rate-A generator; Bursting is disabled,
  - The Rate-A generator is adjusted to 100 kHz, and is disabled,
  - The analog input buffer is reset to empty; buffer threshold is FFFEh,
  - Burst block size is 1024 (0400h),
- Analog outputs are at midrange (zero), and the output clocking mode is 'immediate,'
- The Rate-B generator is adjusted to 2 kHz, and is disabled.
- The digital I/O port is configured as two input bytes.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2302 00A0h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION
D00-D02	RW	ANALOG INPUT MODE	0	Analog input mode: 0 => Differential system inputs 1 => Single-ended system inputs 2 => Zero selftest 3 => VREF selftest 4 => Output Channel 00 5 => Output Channel 01 6 => Output Channel 02 7 => Output Channel 03
D03	RW	Reserved	0	---
D04-D05	RW	INPUT RANGE A	2	Analog input Range-A; Channels 00, 01, 04, 05: 0 => ±100mV 1 => ±1V 2 => ±10V 3 => (Reserved)
D06-D07	RW	INPUT RANGE B	2	Analog input Range-B; Channels 02, 03, 06, 07: 0 => ±100mV 1 => ±1V 2 => ±10V 3 => (Reserved)
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.
D12	RW	ENABLE INPUT BUFFER	0	Enables the input buffer for accepting data.
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.
D14	RO	BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.
D15	RW	BUFFER OVERFLOW	0	Set HIGH if the buffer overflows. Stays HIGH until cleared from the bus or by a board reset.
D16-D17	RW	OUTPUT RANGE	2	Analog Output Voltage Range: 0 => ±2.5V 1 => ±5V 2 => ±10V 3 => (Reserved)
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.
D19	RW	SYNCHRONOUS OUTPUTS	0	When HIGH, the output of the Rate-B generator becomes the output clock. (Initiator mode only).
D20	RW	OUTPUT S/W CLOCK [2]	0	Updates all output channels simultaneously. Overrides existing output clocking source.
D21-D23	R/W	(Reserved)	0	---
D24	RW	INITIATOR	1	Configures the board as an initiator when HIGH, or as a target when LOW.
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator.
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator.
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D30	R/W	(Reserved)	0	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all registers to default values.

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

3.4 Analog Inputs

Each of eight analog input channels can be digitized with 12-bit resolution at rates from DC to 2 Megasamples per second. Data from any combination of inputs can be acquired in a 64 Ksample buffer, and a channel-tag is attached to each input sample. Three voltage ranges are available, and any two of these ranges can be used simultaneously on different channels. Each input channel contains a dedicated 12-Bit ADC.

All active inputs are sampled simultaneously, and the sample clock can be derived: (a) from an internal rate generator, (b) from an external hardware clock input, or (c) directly from the bus.

To illustrate the requirements for initiating analog input acquisition after a board reset, the following operations would start acquisition using the Rate-A generator:

a. Set the Rate-A generator to the required sample rate (paragraph 3.7)
b. Enable the input buffer and the Rate-A generator (paragraphs 3.4.5.1 and 3.7).

3.4.1 Input Modes

An input switching network routes either the system input signals or internal test signals through the input channels, and is controlled by the ANALOG INPUT MODE control field in the BCR. The system inputs are disconnected when internal signals are monitored, and have no effect on test results.

3.4.1.1 System Inputs

Of the eight possible input modes available through the ANALOG INPUT MODE field, two are dedicated to system inputs. In the differential configuration, the signal present between the HI and LO inputs in each channel is acquired. For a single-ended input, the input signal is measured between the HI input and the common return, and the LO input is ignored The selected system input configuration must agree with the system wiring configuration (Paragraph 2.3).

3.4.1.2 Test Modes

Internal analog nodes can be monitored to verify the functional integrity of the board. Since the selected input ranges apply in all input modes, including test modes, the input high-range of ±10V should be used for internal measurements. The following signals are present in *all input channels* when the indicated test modes are selected:

Zero Selftest: Midscale value, ideally equal to 0.000 VDC,

VREF Selftest: Internal voltage reference, ideally equal to +9.900 VDC,

Output Channels: Any of the four analog output channels.

3.4.2 Active Channel Selection

Input channels are designated as active by setting the corresponding ENABLE CHANNEL XX control bit HIGH in the Input Configuration register (Table 3.4-1), or as inactive by clearing the bit LOW. All active inputs are sampled simultaneously when a sample clock occurs. Inactive channels produce no data in the input buffer.

Table 3.4-1. Input Configuration Register

Offset: 0024h **Default: FF00 0400h**

BIT	MODE *	DESIGNATION	DEF	DESCRIPTION
D00-D15	RW	BURST BLOCK SIZE	0400h	Number of active channel sets acquired during a triggered burst.
D16-D23	RO	(Reserved)	0	Read back all-zero.
D24	RW	ENABLE INPUT 00	1	Analog input channel selection mask.
D25	RW	ENABLE INPUT 01	1	
D26	RW	ENABLE INPUT 02	1	
D27	RW	ENABLE INPUT 03	1	
D28	RW	ENABLE INPUT 04	1	
D29	RW	ENABLE INPUT 05	1	
D30	RW	ENABLE INPUT 06	1	
D31	RW	ENABLE INPUT 07	1	

* RW = Read/Write, RO = Read-Only.

3.4.3 Input Ranges

Input voltage ranges of ±10V, ±1V and ±100mV are assigned independently to two groups of input channels by the INPUT RANGE A and INPUT RANGE B control fields in the BCR:

Range A: Input channels 00, 01, 04, 05,

Range B: Input channels 02, 03, 06, 07.

Note: Voltage levels outside the selected ranges will produce saturation codes of plus or minus fullscale, but will not damage the inputs if they are within the range indicated in the product specification for overvoltage protection.

3.4.4 Sampling Modes

All active channels are sampled each time an input sample clock occurs. If the INITIATOR control bit is HIGH in the BCR, input sample clocks are supplied by either the Rate-A generator or by the INPUT S/W CLOCK control bit in the BCR. The INPUT S/W CLOCK control bit always produces an input clock, regardless of the state of the Rate-A generator or the INITIATOR control bit. In the ***Initiator*** mode, each sample clock produces a 100 nanosecond LOW output pulse at the bidirectional INPUT CLK I/O pin in the system I/O connector.

If the INITIATOR control bit is LOW, designating the board as a ***Target***, the INPUT CLK I/O pin becomes an input, and a sample clock is generated for each HIGH-to-LOW transition received at the pin. The Rate-A generator is ignored in the target clocking mode.

3.4.4.1 Continuous

During continuous sampling, all active input channels are sampled continuously as long as a clock source is present. Continuous sampling is selected when the ENABLE INPUT BURST control bit is LOW in the BCR.

3.4.4.2 Burst Sampling

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, an input trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired, and then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the BURST BLOCK SIZE control field in the Input Configuration register (Table 3.4-1). The value in this field is the number of samples acquired *for each active channe*l, and the total number of samples acquired equals this value *times* the number of active channels.

The END OF BURST status bit in the input buffer (Paragraph 3.4.5) is set HIGH for the last input value acquired in a burst. The INPUT BURST BUSY status flag in the BCR is HIGH during each triggered burst, and is LOW otherwise.

For an ***initiator***, a burst trigger is supplied by either the Rate-B generator or by the INPUT S/W TRIGGER control bit in the BCR. The INPUT S/W TRIGGER control bit always produces an burst trigger, regardless of the state of the Rate-B generator or the INITIATOR control bit. In the ***Initiator*** mode, each burst trigger produces a 100 nanosecond LOW output pulse at the bidirectional INPUT TRIG I/O pin in the system I/O connector. The INPUT S/W TRIGGER bit clears automatically.

If the INITIATOR control bit is LOW, the INPUT TRIG I/O pin becomes an input, and a trigger is generated for each HIGH-to-LOW transition received at the pin. The Rate-B generator is ignored in the target clocking mode.

3.4.5 Input Data Buffer

3.4.5.1 Organization

Analog input data accumulates in the input data FIFO buffer until extracted by the PCI bus. The buffer is 64 K-samples deep, and contains a 16-bit data field, a 4-bit tag field, and an END OF BURST status bit (Table 3.4-2). Analog input data is right-justified to the LSB, and occupies bit positions D00 through D11. The pad field is all-zero for offset binary coding, or extends the MSB value in two's complement coding.

The channel tag equals the channel number associated with each data value. Reserved bits are always returned as zeros. The END OF BURST (EOB) status bit identifies the last data value in an input burst.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant data bit (LSB)
D01-D10	DATA01 - DATA10	Data value intermediate data bits
D11	DATA11	Data value most significant data bit (MSB)
D12-D15	PAD FIELD	All-zero for offset binary coding. MSB extension for two's complement coding.
D16-D19	CHANNEL TAG	Channel number associated with data value.
D20	END OF BURST (EOB)	Identifies the last input value in a burst.
D21-D31	(Reserved)	Always zero.

In order for the input buffer to acquire input data, the ENABLE INPUT BUFFER control bit must be set HIGH in the BCR. The buffer can be cleared, or emptied, by writing a "one" to the CLEAR INPUT BUFFER control bit in the BCR. The CLEAR INPUT BUFFER bit clears automatically. An empty buffer returns an indeterminate value.

The BUFFER OVERFLOW status bit in the BCR is set HIGH if the buffer overflows, thereby indicating a potential data loss. The status bit remains HIGH until cleared, either directly from the bus, by the CLEAR INPUT BUFFER control bit, or by a board reset.

3.4.5.2 Buffer Size and Threshold Registers

The Input Buffer Size control register listed in Table 3.1-1 contains the current number of data values present in the input buffer. The Input Buffer Threshold register (Table 3.4-3) specifies the buffer size value above which the BUFFER THRESHOLD FLAG will be asserted HIGH. The threshold flag is duplicated in the Input Buffer Threshold register and the BCR.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0000 FFFEh**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION
D00-D15	RW	BUFFER THRESHOLD	FFFEh	Specifies the number of values in the input data buffer, above which the threshold flag is asserted HIGH.
D16	RO	BUFFER THRESHOLD FLAG [2]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D17-D19	RW	Reserved	0	---
D20-D31	RO	Reserved	0	---

Notes: 1. RO = Read-Only, RW = Read/Write. 2. Duplicated in the BCR.

3.5 Analog Outputs

Each of four analog output channels is controlled directly by one of the four ANALOG OUTPUT CHAN XX control registers listed in Table 3.1-1. The outputs are double-buffered, and can be clocked either independently or simultaneously. Output data is written to a 12-bit field that is right-justified in the data registers (Table 3.5-1).

Table 3.5-1. Analog Output Channel Data Register

Offset: 0008h - 0014h **Default: 0000 0800h**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant data bit
D01-D10	DATA01 - DATA10	Data value intermediate data bits
D11	DATA11	Data value most significant data bit
D12-D31	(Reserved)	Data in this field is ignored.

3.5.1 Output Ranges

An output voltage range of ±10V, ±5V or ±2.5V is assigned by the OUTPUT RANGE control field in the BCR. The default output range is ±10V.

3.5.2 Clocking Modes

3.5.2.1 Immediate

When the SIMULTANEOUS OUTPUTS control bit is LOW in the BCR, each analog output channel is updated immediately after the associated data register receives a new value.

NOTE: The analog outputs respond to new data in the ANALOG OUTPUT CHAN registers in the immediate mode, in the default condition directly after a board reset.

3.5.2.2 Simultaneous

When the SIMULTANEOUS OUTPUTS control bit is HIGH in the BCR, all analog outputs retain their existing values until an output clock occurs. An output clock updates all output channels simultaneously with the most recent data received by the data registers.

An output clock can be generated by:

- The OUTPUT S/W CLOCK control bit in the BCR,
- An external clock source, if the INITIATOR control bit is LOW, or
- The Rate-B generator, if the SYNCHRONOUS OUTPUTS and INITIATOR control bits are HIGH in the BCR.

If the INITIATOR control bit is HIGH in the BCR, output clocks are supplied by either the Rate-B generator or by the OUTPUT S/W CLOCK control bit in the BCR. The Rate-B generator produces an output clock only if the SYNCHRONOUS OUTPUTS and INITIATOR control bits both are HIGH in the BCR. The OUTPUT S/W CLOCK bit clears automatically.

The OUTPUT S/W CLOCK control bit always produces an output clock, regardless of the state of the Rate-B generator or the INITIATOR control bit. In the ***Initiator*** mode, each output clock produces a 100 nanosecond LOW output pulse at the bidirectional OUTPUT CLK I/O pin in the system I/O connector.

If the INITIATOR control bit is LOW, designating the board as a ***Target***, the OUTPUT CLK I/O pin becomes an input, and an output clock is generated for each HIGH-to-LOW transition received at the pin. The Rate-B generator is ignored in the target clocking mode.

3.6 Data Coding Formats

Analog input and output data is arranged as 12 active right-justified data bits in a 16-Bit data field, with the coding conventions shown in Figure 3.6-1. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR, and produces a sign extension through the 16th bit for negative values. Unless indicated otherwise, offset binary coding is assumed throughout this document.

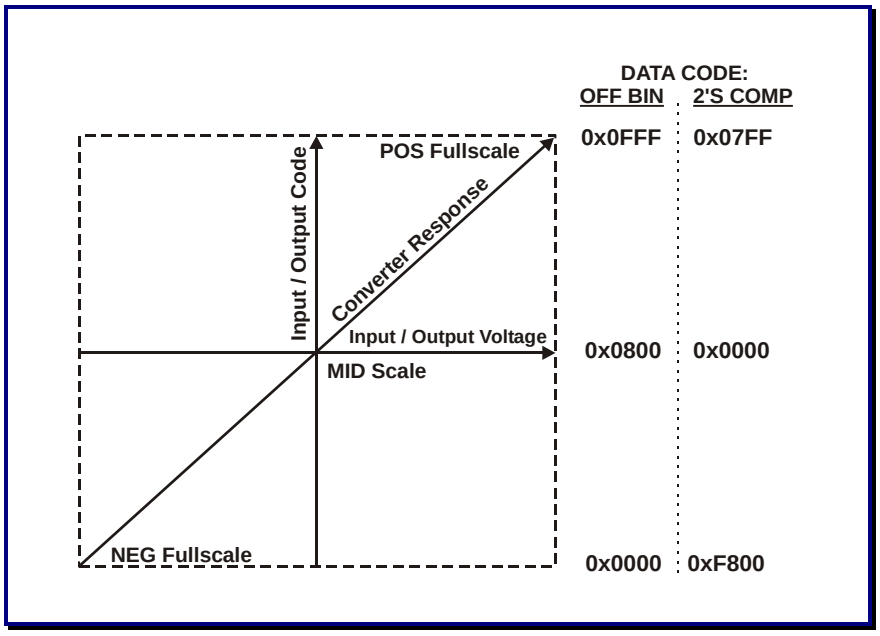


Figure 3.6-1. Analog Data Coding Formats; 12 Bit Data

3.7 Rate-A/B Generators

Two rate generators supply independent clock frequencies from 500 Hz to 2.000 MHz. The Rate-A Generator shown in Table 3.7-1 generates an internal sample clock for the analog inputs. The Rate-B generator output can be used as a trigger source for input burst acquisition, or as an analog output clock.

Each generator is enabled by the associated ENABLE RATE-A/B GENERATOR control bit in the BCR. The generators are nonfunctional when these bits are LOW.

Table 3.7-1. Rate Generator Registers

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 0140 (Rate-A), 0000 3E80h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	Ndiv	---	Rate generator frequency control
D16-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

The frequency **Fgen** (Table 3.7-2) of each generator is calculated as:

Fgen = Fclk / Ndiv,

where **Fclk** is the master clock frequency for the board, and **Ndiv** is the value written to the Rate-A/B Generator register. **Fgen** and **Fclk** are both expressed in the same frequency units. **Fclk** has a standard value of 32.000 MHz, but custom frequencies are available.

Table 3.7-2. Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (32 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
16	0010	2000
17	0011	1882
---	---	Fgen (Hz) = 32,000,000 / Ndiv

* ±0.015 percent.

3.8 Multiboard Synchronization

Analog input and output clocking and triggering can be synchronized among multiple boards by designating one of the boards as an ***initiator***, and the remaining boards as ***targets***. In order to implement this function, the boards must be connected together as described in Paragraph 2.3.4.

When multiple boards are configured as an initiator and multiple targets, the analog input clock, the analog input trigger, and the analog output clock generated in the initiator board are all duplicated in the target boards with delays of less than 130 nanoseconds.

All boards default to the initiator mode, with the INITIATOR control bit set HIGH in the BCR. To designate a board as a target, clear the INITIATOR control bit LOW.

NOTE: To avoid contention among boards that are wired in an initiator/target configuration, ensure that all target boards have been designated before initiating clocking operations.

3.9 Digital I/O Port

The 16-Bit bidirectional digital I/O port consists of two independent data bytes, as shown in Table 3.9-1. Data fields DIO BYTE 00 and DIO BYTE 01 represent the 16 digital I/O pins in the system I/O connector. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the Digital I/O Port register.

Each data byte is an *input field* from the system I/O connector if the corresponding BYTE XX OUTPUT control bit is LOW, or is an *output field* to the connector if the control bit is HIGH. Both byte fields default to inputs.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 00XX 00XXh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	RW	DIO BYTE 00	XXh	System connector pins DIO 00 through DIO 07.
D08	RW	BYTE 00 OUTPUT	0	Direction control for DIO BYTE 00. When LOW, DIO BYTE 00 is an input field. When HIGH, DIO BYTE 00 is an output field.
D09-D15	RO	(Reserved)	0h	Read back as all-zero.
D16-D23	RW	DIO BYTE 01	XXh	System connector pins DIO 08 through DIO 15.
D24	RW	BYTE 01 OUTPUT	0	Direction control for DIO BYTE 01. When LOW, DIO BYTE 01 is an input field. When HIGH, DIO BYTE 01 is an output field.
D25-D31	RO	(Reserved)	0h	Read back as all-zero.

3.10 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCIbus reset.,
- Analog outputs range change.

Note: Analog outputs are active during autocalibration, but do not produce voltage levels outside the selected output range. Analog input channels are calibrated on all input ranges, but to avoid overstressing analog output loads, the analog outputs are calibrated only on the selected output range. Control settings are not altered and external analog input signals are ignored.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of less than 3 seconds. Completion of the operation can be detected either by selecting the "Autocalibration completed" interrupt condition (paragraph 3.11) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.11 Interrupt Control

Specific events can be selected to produce an interrupt request on the single PCI interrupt line (INT-A). For the interrupt to be active however, it must first be enabled through the PCI adapter. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX^{TM} PCI-9080 reference manual.

3.11.1 Organization

Interrupt control fields in the Interrupt Control register (Table 3.11-1) are organized into a selection field and a response field. Each available interrupt event has both a selection control bit and a corresponding response status bit. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit, *or by clearing the associated selection bit*.

NOTE: The interrupt response status bits can *only* be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The local interrupt request (and the PCI INT-A request, if enabled) is asserted if any response bit in the interrupt control register is asserted. To clear the interrupt, all response bits must be cleared.

3.11.2 Event Detection

Interrupt event detection is edge-activated on a transition of the selected event from false to true. Once asserted, each response status bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

Table 3.11-1 Interrupt Control Register

Offset 0x0030 **Default 0x0000 0000**

SELECTION BIT [1]	INTERRUPT EVENT	RESPONSE BIT [2]
D00	Autocal completed	D16
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18
D03	Input Buffer Overflow	D19
D04	Analog Input Burst initiated	D20
D05	Analog Input Burst Completed	D21
D06	Analog Input Clock	D22
D07	Analog Output Clock	D23
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition	D24
D09	(Reserved)	D25
D10	(Reserved)	D26
D11	(Reserved)	D27
D12	(Reserved)	D28
D13	(Reserved)	D29
D14	(Reserved)	D30
D15	(Reserved)	D31

1. Interrupt event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. interrupt response. Asserted HIGH when a selected interrupt occurs. Remains HIGH until cleared LOW.

3.12 DMA Operation

2-Channel DMA transfers from the analog input buffer are supported with the board operating as bus master. Table 3.12-1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***exceeds the threshold value*** selected for the buffer.

The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The number of values read from the buffer equals the threshold value plus one,
(c) The buffer is cleared,
(d) The board is reset,
(e) Autocalibration is executed.

The first occurrence of any of these events terminates the DMA request.

Table 3.12-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

3.13 Board Configuration Register

The read-only board configuration register shown in Table 3.13-1 contains the existing firmware revision, as well as a status field that indicates the availability of optional hardware features.

Table 3.13-1. Board Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION	
D00-D11	Firmware Revision	
D12-D15	(Reserved status flags).	
D16	Low => 8 input channels.	High => 4 input channels.
D17	Low => 64K-sample input buffer.	High => 16K-sample input buffer.
D18	Low => No analog outputs.	High => 4 analog output channels.
D19-D31	(Reserved)	

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of eight single-ended analog input channels contains a selftest input switching network, a programmable-gain amplifier (PGA) and a 12-Bit ADC (Figure 4.1-1), and provides input ranges of ±10V, ±1V and ±100mV. A 64 Ksample FIFO buffer accumulates analog input data for subsequent retrieval through the PCI bus. Four 12-bit analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V, and are accessed directly through dedicated control registers. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller, and supports universal signaling. +5 VDC power from the PCI bus is converted into regulated power voltages for the internal analog networks.

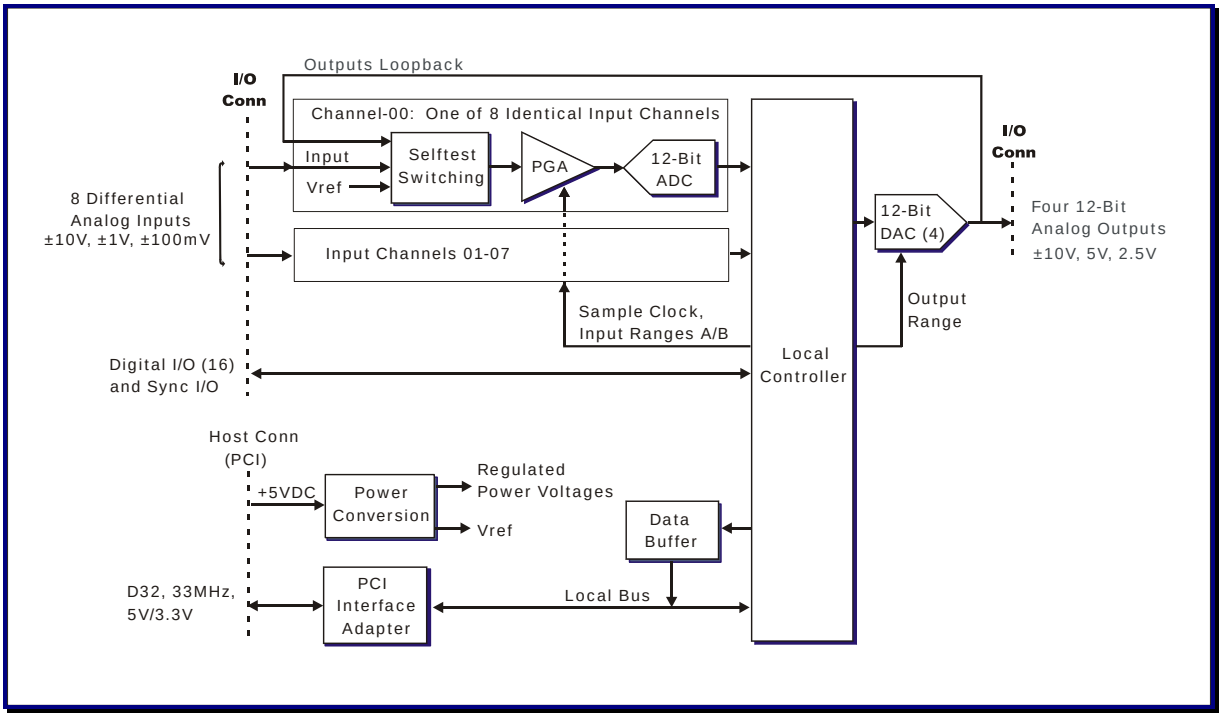


Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input and output channels, and can be configured to accept either differential or single-ended system inputs.

Analog input sampling and output clocking on multiple target boards can be synchronized to a single software-designated initiator board. An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, the 12-bit ADC's receive system analog input signals from the system I/O connector. For integrity testing and autocalibration operations, the internal voltage reference and the analog outputs can be routed through the selftest switches to the ADC's. A programmable-gain amplifier (PGA) in each channel provides the necessary scaling for software-controlled input ranging.

Parallel data from each ADC is multiplexed into a continuous data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies gain and offset correction values obtained during autocalibration. The corrected data is formatted, a channel tag is attached, and the final, processed and formatted data is loaded into analog input data buffer.

4.3 Input Data Buffer

A 64K-sample FIFO buffer accumulates analog input data for subsequent retrieval through the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by an adjustable threshold flag that can generate an interrupt request when the number of values in the buffer moves above or below a selected count.

4.4 Analog Outputs

Four independent 12-bit DAC's are controlled directly through dedicated control registers. Direct register control provides the minimum latency required in some servo applications. Wideband function generation, in general, is not supported.

When each control register receives a new value from the PCI bus, the data word is first corrected for gain and offset errors, and then is serialized for transfer to the associated output DAC. The outputs can operate independently, or can be synchronized to a single output clock.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input and output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample acquired during acquisition, and to each output value written to the DAC channels. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated supply voltages of ±5 VDC and ±15 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	ACCESS MODE [1]	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL	RW	2302 00A0h	Board Control Register (BCR)
0004	DIGITAL I/O PORT	RW	00XX 00XXh	16-Bit Digital I/O port data
0008	ANALOG OUTPUT CHAN 00	RW	0000 0800h	Output Channel 00 data
000C	ANALOG OUTPUT CHAN 01	RW	0000 0800h	Output Channel 01 data
0010	ANALOG OUTPUT CHAN 02	RW	0000 0800h	Output Channel 02 data
0014	ANALOG OUTPUT CHAN 03	RW	0000 0800h	Output Channel 03 data
0018	ANALOG INPUT DATA	RO	00XX XXXXh	Analog input buffer data
001C	RATE GENERATOR A	RW	0000 0140h	Rate-A generator divisor
0020	RATE GENERATOR B	RW	0000 3E80h	Rate-B generator divisor
0024	INPUT CONFIGURATION	RW	FF00 0400h	Analog inputs channel-mask and burst-size
0028	INPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the input buffer
002C	INPUT BUFFER THRESHOLD	RW	0000 FFFEh	Input buffer status flag threshold
0030	INTERRUPT CONTROL	RW	0000 0000h	Interrupt control/status register
0034	Board Configuration [2]	RO	000X XXXXh	Firmware revision and option straps
0038	Autocal Values [2]	RW	0000 XXXXh	Autocal value readback
003C	Auxiliary R/W Register [3]	RW	0000 0000h	Auxiliary register. No internal function.
0040-7F	(Reserved)	---	---	Inactive

Notes: 1. RW = Read/Write, RO = Read-Only.
2. Maintenance register; Shown for reference only.
3. Lower 16 bits (D00-D15) are active; upper 16 bits are all-zero.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2302 00A0h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION
D00-D02	RW	ANALOG INPUT MODE	0	Analog input mode: 0 => Differential system inputs 1 => Single-ended system inputs 2 => Zero selftest 3 => VREF selftest 4 => Output Channel 00 5 => Output Channel 01 6 => Output Channel 02 7 => Output Channel 03
D03	RW	Reserved	0	---
D04-D05	RW	INPUT RANGE A	2	Analog input Range-A; Channels 00, 01, 04, 05: 0 => ±100mV 1 => ±1V 2 => ±10V 3 => (Reserved)
D06-D07	RW	INPUT RANGE B	2	Analog input Range-B; Channels 02, 03, 06, 07: 0 => ±100mV 1 => ±1V 2 => ±10V 3 => (Reserved)
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.
D12	RW	ENABLE INPUT BUFFER	0	Enables the input buffer for accepting data.
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.
D14	RO	BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.
D15	RW	BUFFER OVERFLOW	0	Set HIGH if the buffer overflows. Stays HIGH until cleared from the bus or by a board reset.
D16-D17	RW	OUTPUT RANGE	2	Analog Output Voltage Range: 0 => ±2.5V 1 => ±5V 2 => ±10V 3 => (Reserved)
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.
D19	RW	SYNCHRONOUS OUTPUTS	0	When HIGH, the output of the Rate-B generator becomes the output clock. (Initiator mode only).
D20	RW	OUTPUT S/W CLOCK [2]	0	Updates all output channels simultaneously. Overrides existing output clocking source.
D21-D23	R/W	(Reserved)	0	---
D24	RW	INITIATOR	1	Configures the board as an initiator when HIGH, or as a target when LOW.
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator.
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator.
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D30	R/W	(Reserved)	0	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all registers to default values.

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Input Configuration Register

Offset: 0024h **Default: FF00 0400h**

BIT	MODE *	DESIGNATION	DEF	DESCRIPTION
D00-D15	RW	BURST BLOCK SIZE	0400h	Number of active channel sets acquired during a triggered burst.
D16-D23	RO	(Reserved)	0	Read back all-zero.
D24	RW	ENABLE INPUT 00	1	Analog input channel selection mask.
D25	RW	ENABLE INPUT 01	1	
D26	RW	ENABLE INPUT 02	1	
D27	RW	ENABLE INPUT 03	1	
D28	RW	ENABLE INPUT 04	1	
D29	RW	ENABLE INPUT 05	1	
D30	RW	ENABLE INPUT 06	1	
D31	RW	ENABLE INPUT 07	1	

* RW = Read/Write, RO = Read-Only.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant data bit (LSB)
D01-D10	DATA01 - DATA10	Data value intermediate data bits
D11	DATA11	Data value most significant data bit (MSB)
D12-D15	PAD FIELD	All-zero for offset binary coding. MSB extension for two's complement coding.
D16-D19	CHANNEL TAG	Channel number associated with data value.
D20	END OF BURST	Identifies the last input value in a burst.
D21-D31	(Reserved)	Always zero.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0000 FFFEh**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION
D00-D15	RW	BUFFER THRESHOLD	FFFEh	Specifies the number of values in the input data buffer, above which the threshold flag is asserted HIGH.
D16	RO	BUFFER THRESHOLD FLAG [2]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D17-D19	RW	Reserved	0	---
D20-D31	RO	Reserved	0	---

Notes: 1. RO = Read-Only, RW = Read/Write. 2. Duplicated in the BCR.

Table 3.5-1. Analog Output Channel Data Register

Offset: 0008h - 0014h **Default: 0000 0800h**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant data bit
D01-D10	DATA01 - DATA10	Data value intermediate data bits
D11	DATA11	Data value most significant data bit
D12-D31	(Reserved)	Data in this field is ignored.

Table 3.7-1. Rate Generator Registers

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 0140 (Rate-A), 0000 3E80h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	Ndiv	---	Rate generator frequency control
D16-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

Table 3.7-2. Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (32 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
16	0010	2000
17	0011	1882
---	---	Fgen (Hz) = 32,000,000 / Ndiv

* ±0.015 percent.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 00XX 00XXh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	RW	DIO BYTE 00	XXh	System connector pins DIO 00 through DIO 07.
D08	RW	BYTE 00 OUTPUT	0	Direction control for DIO BYTE 00. When LOW, DIO BYTE 00 is an input field. When HIGH, DIO BYTE 00 is an output field.
D09-D15	RO	(Reserved)	0h	Read back as all-zero.
D16-D23	RW	DIO BYTE 01	XXh	System connector pins DIO 08 through DIO 15.
D24	RW	BYTE 01 OUTPUT	0	Direction control for DIO BYTE 01. When LOW, DIO BYTE 01 is an input field. When HIGH, DIO BYTE 01 is an output field.
D25-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.11-1 Interrupt Control Register

Offset 0x0030 **Default 0x0000 0000**

SELECTION BIT [1]	INTERRUPT EVENT	RESPONSE BIT [2]
D00	Autocal completed	D16
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18
D03	Input Buffer Overflow	D19
D04	Analog Input Burst initiated	D20
D05	Analog Input Burst Completed	D21
D06	Analog Input Clock	D22
D07	Analog Output Clock	D23
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition	D24
D09	(Reserved)	D25
D10	(Reserved)	D26
D11	(Reserved)	D27
D12	(Reserved)	D28
D13	(Reserved)	D29
D14	(Reserved)	D30
D15	(Reserved)	D31

1. Interrupt event selection. Enables assertion of the corresponding response bit when the selected event occurs.

2. interrupt response. Asserted HIGH when a selected interrupt occurs. Remains HIGH until cleared LOW.

Table 3.12-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.13-1. Board Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION	
D00-D11	Firmware Revision	
D12-D15	(Reserved status flags).	
D16	Low => 8 input channels.	High => 4 input channels.
D17	Low => 64K-sample input buffer.	High => 16K-sample input buffer.
D18	Low => No analog outputs.	High => 4 analog output channels.
D19-D31	(Reserved)	

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09-04-2006:	Editorial corrections.
09-20-2009:	Added Section 3.13. Board Configuration Register.

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