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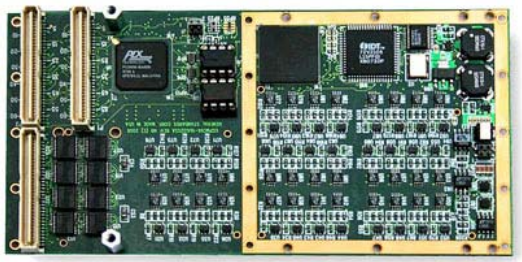
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CCPMC66-16AI32SSA

Conduction-Cooled, 32 Differential Channels; 16-Bit Simultaneous Sampling; PMC Analog Input Board

With 200 KSPS Sample Rate per Channel, 66 MHz PCI Support,
and Rear-Panel I/O



Features

- **32 Differential Analog Inputs with Dedicated 200KSPS 16-Bit ADC per Channel**
- **Compatible with Conduction-Cooled or Air-Cooled Hosts Without Faceplate**
- **Rear-Panel I/O Through P4**
- **Factory-Configurable as either 31 Differential Channels with 2 Ground Pins, or as 32 Channels Consisting of 25 Differential Channels and 7 Pseudo-Differential Channels with a Common Inverted Input and Sync and Clock I/O.**
- **Simultaneous Sampling of all Inputs; Minimum Data Skew**
- **Sampling Rates to 200 KSPS per Channel (6.4 MSPS Aggregate Rate)**
- **D32; 66MHz, 33MHz PCI Compatibility, with Universal 5V/3.3V Signaling**
- Increased Throughput Capacity with Local Data Packing
- Continuous, Burst and Single-Sample Clocking Modes
- Input Ranges: ±2.5V, ±1.25V, ±0.625V; Software-Selectable. An optional range set of ±10V, ±5V, ±2.5V is available.
- Hardware Sync I/O for Multiboard Operation
- 1 MByte FIFO Data Buffer; 512 K-Samples in packed-data mode.
- 2-Channel DMA Engine
- Sampling Controlled by Internal Rate Generator, by Software Trigger, or Externally
- On-Demand Internal Autocalibration of all Channels
- Single-width PMC Form Factor

Typical Applications

✓ High-Density Analog Inputs	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Analog Event Capture	✓ Biometric Signal Analysis	✓ Dynamic Test Systems

Rev: 121912

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Functional Description

The 16-Bit CCPMC66-16AI32SSA analog input board samples and digitizes up to 32 input channels simultaneously at rates up to 200,000 samples per second for each channel. Each input channel contains a dedicated 16-Bit sampling ADC, and the resulting 16-bit sampled data is available to the PCI bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing. Throughput capacity is further enhanced with 66MHz PCI support. All operational parameters are software configurable.

Inputs can be sampled in groups of 2, 4, 8, 16, or 31/32 channels; or any single channel can be sampled continuously. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as ±2.5V, ±1.25V or ±0.625V, with an optional maximum range of ±10V available.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host..

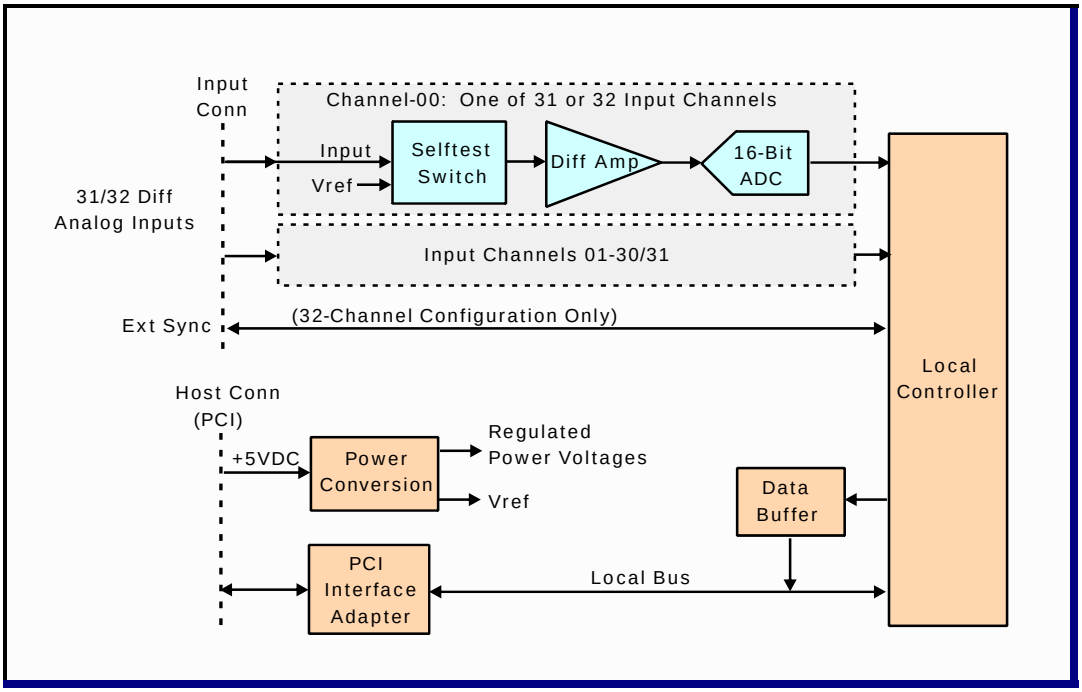


Figure 1. CCPMC66-16AI32SSA; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the rear panel through the 64-Pin PMC P4 connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and operation over the specified temperature range is achieved with either conduction or convection cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions.

Input Characteristics:

Configuration:	31 differential analog input channels with two ground pins, or 32 input channels configured as 20 differential pairs and 12 pseudo-differential inputs sharing a single inverted input.
Voltage Ranges:	Software configurable as ±2.5V, ±1.25V or ±0.625V fullscale. An optional range set of ±10V, ±5V, ±2.5V is available.
Input Impedance:	Low Range-set (±2.5V): 150KOhms typical, line-line. 75-150Kohms line-ground. High Range-set (±10V): 600KOhms typical, line-line. 300-370Kohms line-ground.
Bias Current:	28 ua maximum with inputs shorted to common ground.
Common Mode Rejection:	60dB typical, DC-50kHz
Min/Max Input Levels for rated performance:	Low Range-set (2.5V): LO input: -5V to +11V. HI input: -2.6V to +8.5V. High Range-set: (10V): LO input: -15V to +15V. HI input: -10V to +15V.
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise:	0.15 mVRMS; typical on all ranges. (0.60mVRMS on the optional ±10V range)
Overvoltage Protection:	±40 Volts with power removed; ±25V with power applied.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Maximum Sample Rate:	200 KSPS per channel
Input Bandwidth (-3dB):	DC to 250 kHz typical. Contact GSC Sales for lower cutoff frequencies.
Channels per Sample:	Lowest 2, 4, 8, 16, 31/32 channels; or any single channel.

DC Accuracy:
(Maximum composite error after autocalibration)

Range	Zero-Input	Fullscale
±10V	± 2.3mV	± 5.0mV
±5V	± 1.2mV	± 2.5mV
±2.5V	± 0.8mV	± 1.5mV
±1.25V	± 0.5mV	± 0.9mV
±0.625V	± 0.4mV	± 0.8mV

Integral Nonlinearity:	±0.008 percent of FSR, maximum
Differential Nonlinearity:	±0.004 percent of FSR, maximum

Analog Input Operating Modes and Controls

Input Data Buffer:	1 Megabyte in packed-data mode.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock. Continuous, Burst and Single-Sample Clocking Modes.
Rate Generator:	Programmable from 0.01-200,000 sample clocks per second. Divides the local master clock to the sample rate. (The standard master clock frequency is 40.000MHz. See ordering information for custom frequencies.)
External TTL Sync:	Bidirectional TTL lines; Zero to 200,000 sample clocks per second. Available through the I/O connector for the 32/16/8-Channel versions, or through a 6-pin connector located on the back of the board.
Input Data Format:	Nonpacked Mode: 16-Bit data word plus single-bit Channel-00 tag. Packed Mode: Lword sync code followed by packed channel data. Even-numbered channels occupy lower word (D00-15), odd channels occupy upper word (D16-31).
Data Format:	Selectable as offset binary or two's complement.

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PCI Compatibility:

Conforms to PCI Specification 2.3, with 66MHz/33MHz, D32 and universal signaling (5/3.3 Volt).
Single multifunction interrupt.
DMA transfers as bus master with two DMA channels.

Power Requirements

+5VDC ±0.2 VDC at 1.0 Amp maximum, 0.8 Amp typical.

Maximum Power Dissipation: Side-1: 4.0 Watts. Side 2: 1.0 Watt.

Physical Parameters

Mechanical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 143.75 mm (5.66 in)
Width: 74.0 mm (2.91 in)

Environmental Specifications

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +65 Degrees Celsius at thermal interface Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius at thermal interface Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Standard conduction cooling thermal interfaces.

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For extended-temperature operation, add the suffix "I" to the base model number.

For example, model number CCPMC66-16AI32SSAI-31-40M-0 describes an extended-temperature board with 31 input channels, a standard 40.0000MHz master clock frequency, a ±2.5V input range set, and no custom features.

Optional Parameter	Value	Specify Option As:
Number of Input Channels *	31 Channels **	A = 31
	32 Channels **	A = 32
Master Clock Frequency: (Standard frequency is 40.000MHz)	40.000 MHz	B = 40M
	(Specify custom frequency; 40-43 MHz)	B = (Custom frequency)M
Voltage Range	±2.5V, ±1.25V, ±0.625V Inputs	C=2.5V or Blank
	±10V, ±5V, ±2.5V Inputs	C=10V
Custom Feature	No custom features	D = 0 or blank

* Contact factory for fewer channels.
** See "Configuration" under Input Characteristics.

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Table 1. PMCP4 System I/O Connector

a. 31-Channel Configuration

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
63	INP00 HI	64	INP01 HI
61	INP00 LO	62	INP01 LO
59	INP02 HI	60	INP03 HI
57	INP02 LO	58	INP03 LO
55	INP04 HI	56	INP05 HI
53	INP04 LO	54	INP05 LO
51	INP06 HI	52	INP07 HI
49	INP06 LO	50	INP07 LO
47	INP08 HI	48	INP09 HI
45	INP08 LO	46	INP09 LO
43	INP10 HI	44	INP11 HI
41	INP10 LO	42	INP11 LO
39	INP12 HI	40	INP13 HI
37	INP12 LO	38	INP13 LO
35	INP14 HI	36	INP15 HI
33	INP14 LO	34	INP15 LO
31	INP16 HI	32	INP17 HI
29	INP16 LO	30	INP17 LO
27	INP18 HI	28	INP19 HI
25	INP18 LO	26	INP19 LO
23	INP20 HI	24	INP21 HI
21	INP20 LO	22	INP21 LO
19	INP22 HI	20	INP23 HI
17	INP22 LO	18	INP23 LO
15	INP24 HI	16	INP25 HI
13	INP24 LO	14	INP25 LO
11	INP26 HI	12	INP27 HI
9	INP26 LO	10	INP27 LO
7	INP28 HI	8	INP29 HI
5	INP28 LO	6	INP29 LO
3	INP30 HI	4	INPUT RTN
1	INP30 LO	2	INPUT RTN

b. 32-Channel Configuration

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
63	INP00 HI	64	INP01 HI
61	INP00 LO	62	INP01 LO
59	INP02 HI	60	INP03 HI
57	INP02 LO	58	INP03 LO
55	INP04 HI	56	INP05 HI
53	INP04 LO	54	INP05 LO
51	INP06 HI	52	INP07 HI
49	INP06 LO	50	INP07 LO
47	INP08 HI	48	INP09 HI
45	INP08 LO	46	INP09 LO
43	INP10 HI	44	INP11 HI
41	INP10 LO	42	INP11 LO
39	INP12 HI	40	INP13 HI
37	INP12 LO	38	INP13 LO
35	INP14 HI	36	INP15 HI
33	INP14 LO	34	INP15 LO
31	INP16 HI	32	INP17 HI
29	INP16 LO	30	INP17 LO
27	INP18 HI	28	INP19 HI
25	INP18 LO	26	INP19 LO
23	INP20 HI	24	INP21 HI
21	INP20 LO	22	INP21 LO
19	INP22 HI	20	INP23 HI
17	INP22 LO	18	INP23 LO
15	INP24 HI	16	INP25 HI
13	INP24 LO	14	INP25-31 LO *
11	INP26 HI	12	INP27 HI
9	INP25-31 LO *	10	INPUT RTN
7	INP28 HI	8	DIG RTN
5	INP29 HI	6	CLOCK I/O
3	INP30 HI	4	DIG RTN
1	INP31 HI	2	SYNC I/O

* Shared by Channels 25-31.

Table 2. P1 Sync-I/O Connector

PIN	SIGNAL
1	DIG RTN
2	AUX 00
3	DIG RTN
4	AUX 01
5	DIG RTN
6	Reserved. Ground or leave disconnected.

Recommended P1 mating cable connector is Molex# 51146-0600.

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