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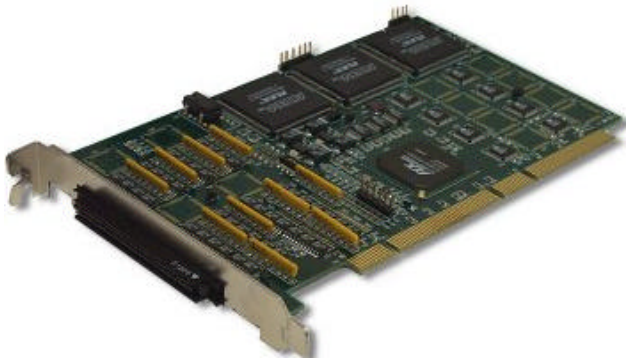
General Standards Corporation

High Performance Bus Interface Solutions

PCI64-HPDI32

High-speed 64 Bit Parallel Digital I/O PCI Board

80 to 400 Mbytes/s Cable I/O with PCI-DMA engine



Features Include:

- 80 Mbytes per second (max) input transfer rate via the front panel connector (RS422/485 differential I/O transceivers)
- 200 Mbytes per second input transfer rate via the front panel connector (LVDS transceivers)
- 264 Mbytes per second PCI transfer rate in burst mode.
- A single board can interface to a wide variety of external high-speed devices.
- "Deep FIFO buffers" (up to 512 Kbytes) allow data bursts to be transferred over the PCI bus independent of transfers over the cable.
- 64-Bit data transfers on the PCI bus.
- On-board cable controller, FIFOs, and DMA engine provide for continuous data transfer capability.
- Data input/output clock rate up to 50 MHz (LVDS, 20 MHz max RS422/485)
- Data input/output width of 32 bits
- 64-Bit, 66MHz PCI v2.2 compliant
- "Program-and-forget" DMA engine handles D64 transfers, also DMA Chaining
- Sample code and VxWorks driver available.
- Interrupts available upon DMA-completion, FIFO status, cable status, frame-valid and line-valid.
- External interrupt input line
- 7 bi-directional signals can be user defined and programmed by the factory to accommodate almost any handshaking protocol (Contact factory).

Applications Include:

- ✓ High speed data acquisition and control
- ✓ Point-to-Point PCI-to-PCI bus communication
- ✓ High-speed video data capture
- ✓ General Purpose Parallel DMA interface
- ✓ Development and research

General Standards Corporation
8302A Whitesburg Drive · Huntsville, AL 35802
Phone: (256)880-8787 or (800)653-9970
FAX: (256)880-8788
Email: sales@generalstandards.com

Overview:

The PCI64-HPDI32 board is a very high speed parallel digital input/output board. It provides for data I/O via the cable at 80 Mbytes per second (RS422/485 differential I/O) or 200 Mbytes per second (LVDS) and can transfer data indefinitely without host intervention. The board employs General Standards' high performance PCI-DMA (PLX) engine. The PCI-DMA is easily set up and operated by writing only a few programming instruction statements to the board. Once the link between the PCI64-HPDI32 board and the external customer device is established, the desired data transfers between the two devices are performed and are transparent to the user. The board employs differential (RS-422/485) or LVDS transceivers and the data path is 32 bits wide. The board will interface to a wide variety of digital I/O devices.

Functional Description:

The PCI64-HPDI32 board includes the PCI-DMA engine, FIFO memory, a 32-Bit cable input/output controller, and cable receivers (LVDS or RS-422/485). The DMA engine is capable of transferring data to host memory using D64 block transfers; while the FIFO memory provides continuous transmission of data without interrupting the DMA transfers or requiring intervention from the Host CPU.

After the DMA is initialized and started, the Host CPU will be free to proceed with other duties and will need to only respond to interrupts.

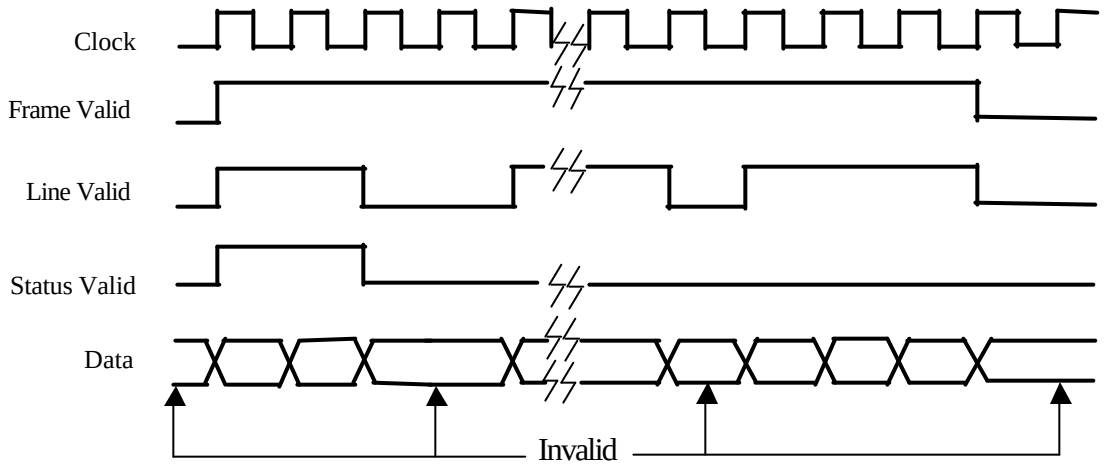
The board also includes interrupt generation for interface flexibility and end-of-transfer indication. Interrupts are also available to indicate FIFO status (Transmit and Receive FIFO almost-empty and almost-full), cable status, and frame and line valid for easy manipulation of the cable interface.

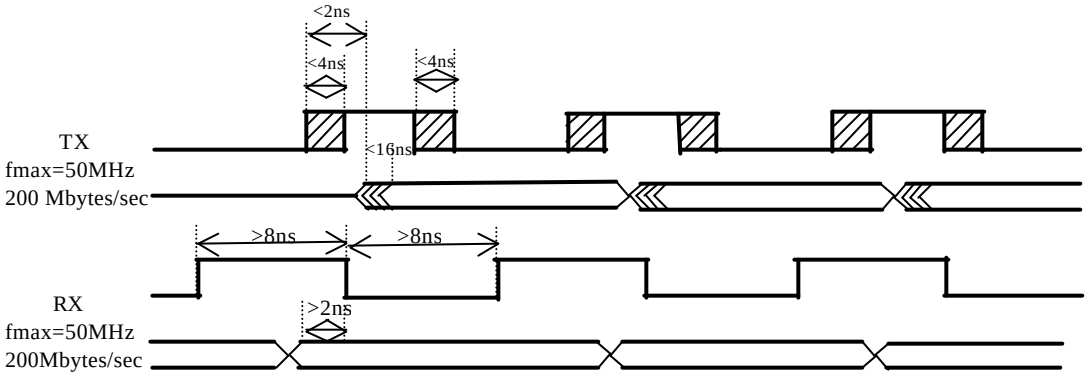
The PCI64-HPDI32 also offers 7 Bi-directional signals that can be customized to accommodate almost any handshaking protocol. General Standards routinely modifies the cable protocol to meet the customer's exact interface protocol.

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Cable Interface:

The cable interface provides for very high-speed reception of data (up to 200 Mbytes/sec). The cable interface provides for a data interface width of 32 bits. The data receivers are differential (RS-422/485) or LVDS. The PCI64-HPDI32 board offers five different cable transfer protocols that can be software defined to accommodate almost any handshake protocol desired. Handshake protocol #5 timing is shown in the following timing diagram.





Note: Data is transmitted on the rising edge of the Transmit clock and received on the negative edge of the receive clock.

High Performance Architecture:

The board is designed for the highest performance level using conventional (and moderately priced) components. The PCI-DMA engine is designed to require minimal intervention from the host; it provides for high-speed transfers between the FIFO and PCI memory using DMA instructions stored in RAM. Data is transferred from the cable to the FIFO using a high-speed dedicated I/O controller.

SPECIFICATIONS

DMA Transfer Rates

- Transfer Rate over cable (RS-422/485 Transceivers):
  80 Mbytes/sec at 20 MHz clock rate and 32-bit cable interface.
- Transfer Rate over cable (LVDS Transceivers):
  200 Mbytes/sec (max) at 50Mhz and 32 bit.
- PCI transfer rate from on-board FIFO to PCI:
  264 Mbytes/sec max
- Data transfers over the cable do not interrupt data transfers over PCI since data is decoupled using FIFO buffering.

DMA Start Latency (when started by cable input or by CPU)

Initialization and DMA start: less than 1 microsecond typ.

FIFO Memory

The FIFOs on the PCI64-HPDI32 are used for buffering the transmit or receive data. There is a total of eight FIFOs on the board; 1 set of 4 for transmit, and 1 set of 4 for receive. Each set consists of 32 bits of data and 4 status flags. The receive FIFOs are loaded by the cable receive control logic and read by either the CPU or the DMA.

The transmit FIFOs are loaded by either the CPU or the DMA and read by the cable transmit control logic. The 4 status flags that accompany the FIFOs are all active low (‘0’ being TRUE) and are as follows: Empty, Almost Empty, Almost Full, Full. The Almost Empty and the Almost Full status flags can be programmed by the software to become true at most desired levels.

Cable Interface Transceivers

RS-422/485 levels (contact factory for availability of TTL levels)

RS-422/485 transceivers provide ± 7.5 V of noise immunity and can withstand ± 25 V transients without damage. Optional on-board parallel termination. The parallel terminators provide the usual transmission line termination. In either case unused inputs can be left open; however, the logic level of unconnected inputs is indeterminate.

LVDS levels

Low Voltage Differential Signaling uses ±140-360mV Output Differential Voltage on a +1-1.65 Offset Voltage. The Receiver Input Threashold is ±100 mV. The low propagation delay of the transceivers allow the high data transmission rates. The transceivers are configured in Bi-Directional Half-Duplex Receiver with termination resistors. The Termination resistors can be removed for Multidrop Configurations.

PCI INTERFACE

❑ **Compatibility:** Conforms to 64-Bit 66MHz PCI Specification v2.2, with D64 read/write transactions.
Supports "plug-n-play" initialization.
Single multifunction interrupt.
Supports DMA transfers as bus master.

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MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

❑ Power Requirements

+5.0 VDC ±0.20 VDC at 4.5 Amps, maximum

❑ Physical Dimensions (Excluding panel bracket)

Height:	98 mm
Length:	175 mm
Width:	6.1 mm

❑ Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +55 degrees Celsius Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.

❑ Cooling Requirements

200 LFPM minimum air flow across component side of board;

ORDERING INFORMATION

Specify the basic product model number (PCI64-HPDI32-XXXK), where "X" is an option code as indicated below. For example, model number PCI64-HPDI32-256K describes a board with a total of 256Kbytes of FIFO buffering.

Other Examples Follow:

PCI64-HPDI32-64K with 8K x 32-bit FIFOs on each channel (both Tx & Rx, 64K byte total);
PCI64-HPDI32-256K with 32K x 32-bit FIFOs on each channel (both Tx & Rx, 256K byte total);
PCI64-HPDI32-512K with 64K x 32-bit FIFOs on each channel (both Tx & Rx, 512K byte total);
PCI64-HPDI32-1M with 128K x 32-bit FIFOs on each channel (both Tx & Rx, 1M byte total);

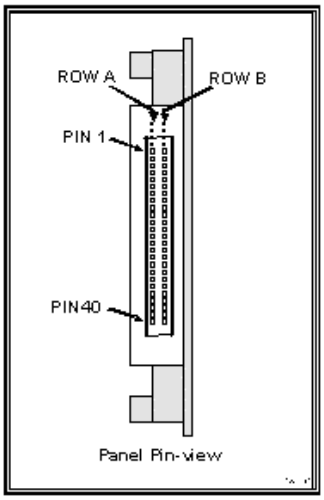
LVDS cable transceiver version:

PCI64-HPDI32-64K-LVDS with 8Kx32-bit FIFOs on each channel, (both Tx & Rx,64K bytes total);
PCI64-HPDI32-256K- LVDS with 32Kx32-bit FIFOs on each channel, (both Tx & Rx,256K byte total);
PCI64-HPDI32-512K- LVDS with 64Kx32-bit FIFOs on each channel, (both Tx & Rx,512K byte total);
PCI64-HPDI32-1M- LVDS with 128Kx32-bit FIFOs on each channel (both Tx & Rx, 1M byte total);

SYSTEM I/O CONNECTIONS

System Connector Pin Functions

Pin No.	Cable Signal Name	Pin No.	Cable Signal Name
1	CABLE CLK +	41	CABLE D12 +
2	CABLE CLK -	42	CABLE D12 -
3	CABLE COMMAND D0 +	43	CABLE D13 +
4	CABLE COMMAND D0 -	44	CABLE D13 -
5	CABLE COMMAND D1 +	45	CABLE D14 +
6	CABLE COMMAND D1 -	46	CABLE D14 -
7	CABLE COMMAND D2 +	47	CABLE D15 +
8	CABLE COMMAND D2 -	48	CABLE D15 -
9	CABLE COMMAND D3 +	49	CABLE D16 +
10	CABLE COMMAND D3 -	50	CABLE D16 -
11	CABLE COMMAND D4 +	51	CABLE D17 +
12	CABLE COMMAND D4 -	52	CABLE D17 -
13	CABLE COMMAND D5 +	53	CABLE D18 +
14	CABLE COMMAND D5 -	54	CABLE D18 -
15	CABLE COMMAND D6 +	55	CABLE D19 +
16	CABLE COMMAND D6 -	56	CABLE D19 -
17	CABLE D0 +	57	CABLE D20 +
18	CABLE D0 -	58	CABLE D20 -
19	CABLE D1 +	59	CABLE D21 +
20	CABLE D1 -	60	CABLE D21 -
21	CABLE D2 +	61	CABLE D22 +
22	CABLE D2 -	62	CABLE D22 +
23	CABLE D3 +	63	CABLE D23+
24	CABLE D3 -	64	CABLE D23 -
25	CABLE D4 +	65	CABLE D24 +
26	CABLE D4 -	66	CABLE D24 -
27	CABLE D5 +	67	CABLE D25 +
28	CABLE D5 -	68	CABLE D25 -
29	CABLE D6 +	69	CABLE D26 +
30	CABLE D6 -	70	CABLE D26 -
31	CABLE D7 +	71	CABLE D27 +
32	CABLE D7 -	72	CABLE D27 -
33	CABLE D8 +	73	CABLE D28 +
34	CABLE D8 -	74	CABLE D28 -
35	CABLE D9 +	75	CABLE D29 +
36	CABLE D9 -	76	CABLE D29 -
37	CABLE D10 +	77	CABLE D30 +



System Mating Connector:
Robinson Nugent # P50E-080-S-TG

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38	CABLE D10 -	78	CABLE D30 -
39	CABLE D11 +	79	CABLE D31 +
40	CABLE D11 -	80	CABLE D31 -

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