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PCI-HPDI32-PRINT

User Manual

Manual Revision: B

Preliminary

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PREFACE

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This user's manual provides information on the specifications, theory of operation, register level programming, installation of the board and information required for customized hardware/software development.

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RELATED PUBLICATIONS

The following manuals and specifications provide the necessary information for in depth understanding of the specialized parts used on this board.

EIA Standard for the RS-422A Interface (EIA order number EIA-RS-422A)

PCI Local Bus Specification Revision 2.1 June 1, 1995. Questions regarding the PCI specification be forwarded to:

PCI Special Interest Group
P.O. Box 14070
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PCI-HPDI32A-PRINT Documentation History

1) 03/20/2000: Converted PCI-HPDI32A Manual to PCI-HPDI32A-PRINT
2) 06/21/2000: Added documentation for Quadrature Transition Delay Register.
3) 11/17/2005: Firmware Revision 0x307+ added BCR bits D12 and D13 for FIFO almost values > 0xFFFF

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TABLE of CONTENTS

CHAPTER 1: INTRODUCTION....0

1.0 FUNCTIONAL DESCRIPTION....0
1.2 FIFOs....2

CHAPTER 2: REGISTERS....3

2.0 PCI-HPDI32A-PRINT REGISTER INFORMATION....3
2.1 PCI CONFIGURATION REGISTERS....3
Table 2.1-1: Register Mapping....3
2.2 PLX REGISTERS....4
Table 2.2-1: LOCAL CONFIGURATION REGISTERS....4
Table 2.2-2: RUN TIME REGISTERS....4
Table 2.2-3: DMA REGISTERS....5
Table 2.2-3: MESSAGING QUEUE REGISTERS....5
2.3 PCI CONFIGURATION REGISTER BIT MAPS....6
2.3.1 PCI Configuration ID Register (Offset 0x00)....6
2.3.2 PCI Command Register (Offset 0x04)....6
2.3.3 PCI Status Register (Offset 0x06)....6
2.3.4 PCI Revision ID Register (Offset 0x08)....6
2.3.5 PCI Class Code Register (Offset 0x09..0B)....6
2.3.6 PCI Cache Line Size Register (Offset 0x0C)....7
2.3.7 PCI Latency Timer Register (Offset 0x0D)....7
2.3.8 PCI Header Type Register (Offset 0x0E)....7
2.3.9 PCI Built-In Self Test (BIST) Register (PCI Offset 0x0F)....7
2.3.10 PCI Base Address Register for Memory Access to Runtime Registers (Offset 0x010)....7
2.3.11 PCI Base Address Register for I/O Access to Runtime Registers (Offset 0x14)....7
2.3.12 PCI Base Address Register for Memory Access to Local Address Space 0 (Offset 0x18)....7
2.3.13 PCI Base Address Register for Memory Access to Local Address Space 1 (Offset 0x1C)....8
2.3.14 PCI Base Address Register (Offset 0x20)....8
2.3.15 PCI Base Address Register (Offset 0x24)....8
2.3.16 PCI Cardbus CIS Pointer Register (Offset 0x28)....8
2.3.17 PCI Subsystem Vendor ID Register (Offset 0x2C)....8
2.3.18 PCI Subsystem ID Register (Offset 0x2E)....8
2.3.19 PCI Expansion ROM Base Register (Offset 0x30)....8
2.3.20 PCI Interrupt Line Register (Offset 0x3C)....8
2.3.21 PCI Interrupt Pin Register (Offset 0x3D)....8
2.3.22 PCI Min_Gnt Register (Offset 0x3E)....8
2.3.23 PCI Max_Lat Register (Offset 0x3F)....9
2.4 LOCAL CONFIGURATION REGISTERS....9
2.4.1 Local Address Space 0 Range Register for PCI to Local bus (PCI 0x00) (LOC 0x80)....9
2.4.2 Local Address Space 0 Local Base Address (Re-map) Register for PCI to Local Bus (PCI 0x04) (LOC 0x84) 9
2.4.3 Mode/Arbitration Register (PCI 0x08) (LOC 0x88)....9
2.4.4 Big/Little Endian Descriptor Register (PCI 0x0C) (LOC 0x8C)....9
2.4.5 Local Expansion ROM Range Register for PCI to Local Bus (PCI 0x10) (LOC 0x90)....10
2.4.6 Local Expansion ROM Local Base Address (Re-map) register for PCI to Local Bus and BREQo Control (PCI 0x14) (LOC 0x94)....10
2.4.7 Local Address Space 0/Expansion ROM Bus Region Descriptor Register (PCI 0x18) (LOC 0x98) 10
2.4.8 Local Range register for Direct Master to PCI (PCI 0x1C) (LOC 0x9C)....10
2.4.9 Local Bus Base Address register for Direct Master to PCI Memory (PCI 0x20) (LOC 0xA0)....11
2.4.10 Local Base Address for Direct Master to PCI IO/CFG Register (PCI 0x24) (LOC 0xA4)....11
2.4.11 PCI Base Address (Re-map) register for Direct Master to PCI Memory (PCI 0x28) (LOC 0xA8)...11

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2.4.12 PCI Configuration Address Register for Direct Master to PCI IO/CFG (PCI 0x2C) (LOC 0xAC) ..11
2.4.13 Local Address Space 1 Range Register for PCI to Local Bus (PCI 0xF0) (LOC 0x170).....11
2.4.14 Local Address Space 1 Local Base Address (Remap) Register (PCI 0xF4) (LOC 0x174) 11
2.4.15 Local Address Space 1 Bus Region Descriptor Register (PCI 0xF8) (LOC 0x178) 12
2.5 RUNTIME REGISTERS 12
2.5.1 Mailbox Register 0 (PCI 0x40) (LOC 0xC0).....12
2.5.2 Mailbox Register 1 (PCI 0x44) (LOC 0xC4).....12
2.5.3 Mailbox Register 2 (PCI 0x48) (LOC 0xC8).....12
2.5.4 Mailbox Register 3 (PCI 0x4C) (LOC 0xCC) 12
2.5.5 Mailbox Register 4 (PCI 0x50) (LOC 0xD0) 12
2.5.6 Mailbox Register 5 (PCI 0x54) (LOC 0xD4) 12
2.5.7 Mailbox Register 6 (PCI 0x58) (LOC 0xD8) 12
2.5.8 Mailbox Register 7 (PCI 0x5C) (LOC 0xDC) 12
2.5.9 PCI to Local Doorbell Register Description (PCI 0x60) (LOC 0xE0) 12
2.5.10 Local to PCI Doorbell Register Description (PCI 0x64) (LOC 0xE4).....13
2.5.11 Interrupt Control /Status (PCI 0x68) (LOC 0xE8) 13
2.5.12 Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI 0x6C) (LOC 0xEC).....13
2.5.13 PCI Permanent Configuration ID Register (PCI 0x70) (LOC 0xF0).....14
2.5.14 PCI Permanent Revision ID Register (PCI 0x74) (LOC 0xF4).....14
2.6 LOCAL DMA REGISTERS 14
2.6.1 DMA Channel 0 Mode Register (LOC 0x100).....14
2.6.2 DMA Channel 0 PCI Address Register (LOC 0x104) 14
2.6.3 DMA Channel 0 Local Address Register (LOC 0x108) 14
2.6.4 DMA Channel 0 Transfer Size (Bytes) Register (LOC 0x10C).....14
2.6.5 DMA Channel 0 Descriptor Pointer Register (LOC 0x110).....15
2.6.6 DMA Channel 1 Mode Register (LOC 0x114).....15
2.6.7 DMA Channel 1 PCI Data Address Register (LOC 0x118).....15
2.6.8 DMA Channel 1 Local Data Address Register (LOC 0x11C) 15
2.6.9 DMA Channel 1 Transfer Size (bytes) register (LOC 0x120) 15
2.6.10 DMA Channel 1 Descriptor Pointer Register (LOC 0x124).....15
2.6.11 DMA Command/Status Register (LOC 0x128).....15
2.6.12 DMA Channel 1 Command/Status Register 0 (LOC 0x128).....16
2.6.13 DMA Arbitration Register 1 (LOC 0x12C) same as Mode /Arbitration Register at address (LOC 0x88) 16
2.7 MESSAGING QUEUE REGISTERS 16
2.7.1 Outbound Post List FIFO Interrupt Status Register (PCI 0x30) (LOC 0xB0) 16
2.7.2 Outbound Post List FIFO Interrupt Status Register (PCI 0x34) (LOC 0xB4) 16
2.7.3 Inbound Queue Port Register (PCI 0x40) 16
2.7.4 Outbound Queue Port Register (PCI 0x44) 16
2.7.5 Messaging Queue Configuration Register (PCI 0xC0) (LOC 0x140).....17
2.7.6 Queue Base Address Register (PCI 0xC4) (LOC 0x144) 17
2.7.7 Inbound Free Head Pointer Register (PCI 0xC8) (LOC 0x148) 17
2.7.8 Inbound Free Head Tail Register (PCI 0xCC) (LOC 0x14C).....17
2.7.9 Inbound Post Head Pointer Register (PCI 0xD0) (LOC 0x150).....17
2.7.10 Inbound Post Tail Pointer Register (PCI 0xD4) (LOC 0x154).....17
2.7.11 Outbound Free Head Pointer Register (PCI 0xD8) (LOC 0x158).....17
2.7.12 Outbound Free Tail Pointer Register (PCI 0xDC) (LOC 0x15C) 17
2.7.13 Outbound Post Head Pointer Register (PCI 0xE0) (LOC 0x160) 17
2.7.14 Outbound Post Tail Pointer Register (PCI 0xE4) (LOC 0x164) 18
2.7.15 Queue Status/Control Register (PCI 0xE8) (LOC 0x168).....18
2.8 PCI CONFIGURATION REGISTER BIT DESCRIPTIONS 18
2.8.1 PCI Configuration ID Register (Offset 0x00) 18
2.8.2 PCI Command Register (Offset 0x04) 18
2.8.3 PCI Status Register (Offset 0x06).....19

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2.8.4 PCI Revision ID Register (Offset 0x08) 20
2.8.5 PCI Class Code Register (Offset 0x09 - 0B)....20
2.8.6 PCI Cache Line Size Register (Offset 0x0C)....20
2.8.7 PCI Latency Timer Register (Offset 0x0D) 20
2.8.8 PCI Header Type Register (Offset 0x0E) 20
2.8.9 PCI Built-In Self Test (BIST) Register (PCI Offset 0x0F)....20
2.8.10 PCI Base Address Register for Memory Access to Runtime Registers (Offset 0x010)....21
2.8.11 PCI Base Address Register for I/O Access to Runtime Registers (Offset 0x14) 21
2.8.12 PCI Base Address Register for Memory Access to Local Address Space 0 (Offset 0x18)....21
2.8.13 PCI Base Address Register for Memory Accesses to Local Address Space 1 (Offset 0x1C)....22
2.8.14 PCI Base Address Register (Offset 0x20) 22
2.8.15 PCI Base Address Register (Offset 0x24) 22
2.8.16 PCI Base Cardbus CIS Pointer Register (Offset 0x28) 22
2.8.17 PCI Subsystem Vendor ID Register (Offset 0x2C) 22
2.8.18 PCI Subsystem ID Register (Offset 0x2E) 22
2.8.19 PCI Expansion ROM Base Register (Offset 0x30)....22
2.8.20 PCI Interrupt Line Register (Offset 0x3C) 23
2.8.21 PCI Interrupt Pin Register (Offset 0x3D)....23
2.8.22 PCI Min_Gnt Register (Offset 0x3E) 23
2.8.23 PCI Max_Lat Register (Offset 0x3F) 23
2.9 LOCAL CONFIGURATION REGISTERS BIT DESCRIPTIONS....23
2.9.1 Local Address Space 0 Range Register for PCI to Local bus (PCI 0x00) (LOC 0x80)....23
2.9.2 Local Address Space 0 Local Base Address Register for PCI to Local Bus (PCI 0x04) (LOC 0x84)..24
2.9.3 Mode/Arbitration Register (PCI 0x08) (LOC 0x88)....24
2.9.4 Local Register (PCI 0x0C) (LOC 0x8C) 25
2.9.5 Local Expansion ROM Range Register for PCI to Local Bus (PCI 0x10) (LOC 0x90)....26
2.9.6 Local Expansion ROM Local Base Address (Re-map) register for PCI to Local Bus and BREQo Control (PCI 0x14) (LOC 0x94)....26
2.9.7 Local Bus Region Descriptor for PCI to Local Accesses Register (PCI 0x18) (LOC 0x98) 26
2.9.8 Local Range register for Direct Master to PCI (PCI 0x1C) (LOC 0x9C)....28
2.9.9 Local Bus Base Address register for Direct Master to PCI Memory (PCI 0x20) (LOC 0xA0) 28
2.9.10 Local Base Address for Direct Master to PCI IO/CFG Register (PCI 0x24) (LOC 0xA4) 28
2.9.11 PCI Base Address (Re-map) register for Direct Master to PCI (PCI 0x28) (LOC 0xA8)....28
2.9.12 PCI Configuration Address Register for Direct Master to PCI IO/CFG (PCI 0x2C) (LOC 0xAC) ..29
2.9.13 Local Address Space 1 Range Register for PCI to Local Bus (PCI 0xF0) (LOC 0x170)....29
2.9.14 Local Address Space 1 Local Base Address (Remap) Register (PCI 0xF4) (LOC 0x174) 30
2.9.15 Local Address Space 1 Bus Region Descriptor Register (PCI 0xF8) (LOC 0x178) 30
2.10 SHARED RUNTIME REGISTERS BIT DESCRIPTIONS....31
2.10.1 Mailbox Register 0 (PCI 0x40) (LOC 0xC0) 31
2.10.2 Mailbox Register 1 (PCI 0x44) (LOC 0xC4) 31
2.10.2 Mailbox Register 2 (PCI 0x48) (LOC 0xC8) 31
2.10.3 Mailbox Register 3 (PCI 0x4C) (LOC 0xCC)....31
2.10.4 Mailbox Register 4 (PCI 0x50) (LOC 0xD0)....31
2.10.5 Mailbox Register 5 (PCI 0x54) (LOC 0xD4)....31
2.10.6 Mailbox Register 6 (PCI 0x58) (LOC 0xD8)....31
2.10.7 Mailbox Register 7 (PCI 0x5C) (LOC 0xDC)....31
2.10.8 PCI to Local Doorbell Register Description (PCI 0x60) (LOC 0xE0)....31
2.10.9 Local to PCI Doorbell Register Description (PCI 0x64) (LOC 0xE4)....31
2.10.10 Interrupt Control /Status (PCI 0x68) (LOC 0xE8) 32
2.10.11 EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI 0x6C) (LOC 0xEC) 33
2.10.12 PCI Permanent Configuration ID Register (PCI 0x70) (LOC 0xF0)....34
2.10.13 PCI Permanent Revision ID Register (PCI 0x74) (LOC 0xF4)....34
2.11 LOCAL DMA REGISTERS 34
2.11.1 DMA Channel 0 Mode Register (LOC 0x100)....34

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2.11.2 DMA Channel 0 PCI Address Register (LOC 0x104) 35
2.11.3 DMA Channel 0 Local Address Register (LOC 0x108) 35
2.11.4 DMA Channel 0 Transfer Size (Bytes) Register (LOC 0x10C) 35
2.11.5 DMA Channel 0 Descriptor Pointer Register (LOC 0x110) 35
2.11.6 DMA Channel 1 Mode Register (LOC 0x114) 36
2.11.7 DMA Channel 1 PCI Data Address Register (LOC 0x118) 37
2.11.8 DMA Channel 1 Local Data Address Register (LOC 0x11C) 37
2.11.9 DMA Channel 1 Transfer Size (bytes) register (LOC 0x120) 37
2.11.10 DMA Channel 1 Descriptor Pointer Register (LOC 0x124) 37
2.11.11 DMA Command/Status Register (LOC 0x128) 37
2.11.12 DMA Command/Status Register (LOC 0x129) 38
2.11.13 DMA Arbitration Register 0 (LOC 0x12C). Same as Mode/Arbitration Register at address (LOC 0x88) 38
2.11.14 DMA Threshold Register 1 (LOC 0x130) 38
2.12 MESSAGING QUEUE REGISTERS 38
2.12.1 Outbound Post List FIFO Interrupt Status Register (PCI 0x30) (LOC 0xB0) 39
2.12.2 Outbound Post List FIFO Interrupt Status Register (PCI 0x34) (LOC 0xB4) 39
2.12.3 Inbound Queue Port Register (PCI 0x40) 39
2.12.4 Outbound Queue Port Register (PCI 0x44) 39
2.12.5 Messaging Queue Configuration Register (PCI 0xC0) (LOC 0x140) 39
2.12.6 Queue Base Address Register (PCI 0xC4) (LOC 0x144) 40
2.12.7 Inbound Free Head Pointer Register (PCI 0xC8) (LOC 0x148) 40
2.12.8 Inbound Free Head Tail Register (PCI 0xCC) (LOC 0x14C) 40
2.12.9 Inbound Post Head Pointer Register (PCI 0xD0) (LOC 0x150) 40
2.12.10 Inbound Post Tail Pointer Register (PCI 0xD4) (LOC 0x154) 40
2.12.11 Outbound Free Head Pointer Register (PCI 0xD8) (LOC 0x158) 40
2.12.12 Outbound Free Tail Pointer Register (PCI 0xDC) (LOC 0x15C) 41
2.12.13 Outbound Post Head Pointer Register (PCI 0xE0) (LOC 0x160) 41
2.12.14 Outbound Post Tail Pointer Register (PCI 0xE4) (LOC 0x164) 41
2.12.15 Queue Status/Control Register (PCI 0xE8) (LOC 0x168) 41
2.13 PCI-HPDI32A-PRINT LOCAL REGISTERS 43
2.14 PCI-HPDI32A-PRINT LOCAL REGISTERS, BIT MAP & BIT DESCRIPTIONS 43
2.14.1 FIRMWARE REVISION: (Offset 0x00) 44
2.14.2 BOARD CONTROL: (Offset 0x04) 44
2.14.3 BOARD STATUS: (Offset 0x08) 44
2.14.4 TX ALMOST: (Offset 0x0C) 45
2.14.5 TX FIFOs: (Offset 0x18) 45
2.14.6 HEAD SHIFT SIZE: (Offset 0x20) 45
2.14.7 INTERRUPT CONTROL: (Offset 0x30) 46
2.14.8 INTERRUPT STATUS: (Offset 0x34) 46
2.14.9 PRINTING CONTROL/STATUS: (Offset 0x40) 47
2.14.10 EDGE SELECTOR: (Offset 0x44) 48
2.14.11 HEAD DATA HOLDOFF: (Offset 0x48) 49
2.14.12 QUADRATURE TRANSISTION DELAY COUNT: (Offset 0x4C) 49
2.14.13 START POSITION: (Offset 0x50) 49
2.14.14 STOP POSITION: (Offset 0x54) 50
2.14.15 CURRENT POSITION: (Offset 0x58) 50
2.14.16 HEAD 0 FIRE DELAY: (Offset 0x80) 50
2.14.17 HEAD 0 FIRE WIDTH: (Offset 0x84) 50
2.14.18 HEAD 1 FIRE DELAY: (Offset 0x88) 50
2.14.19 HEAD 1 FIRE WIDTH: (Offset 0x8C) 50
2.14.20 HEAD 2 FIRE DELAY: (Offset 0x90) 51
2.14.21 HEAD 2 FIRE WIDTH: (Offset 0x94) 51
2.14.22 HEAD 3 FIRE DELAY: (Offset 0x98) 51
2.14.23 HEAD 3 FIRE WIDTH: (Offset 0x9C) 51

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2.14.24 HEAD 4 FIRE DELAY: (Offset 0xA0) 51
2.14.25 HEAD 4 FIRE WIDTH: (Offset 0xA4) 51
2.14.26 HEAD 5 FIRE DELAY: (Offset 0xA8) 51
2.14.27 HEAD 5 FIRE WIDTH: (Offset 0xAC) 51
2.14.28 HEAD 6 FIRE DELAY: (Offset 0xB0) 51
2.14.29 HEAD 6 FIRE WIDTH: (Offset 0xB4 51
2.14.30 HEAD 7 FIRE DELAY: (Offset 0xB8) 51
2.14.31 HEAD 7 FIRE WIDTH: (Offset 0xBC) 52

CHAPTER 3: PROGRAMMING 53

3.0 INITIALIZATION 53
3.1 RESETS 53
3.2 FIFOs 53
3.3 INTERRUPTS 53

CHAPTER 4: HARDWARE CONFIGURATION 55

4.0 THE ON-BOARD TRANSMIT CLOCK 55
Figure 4.0-1: Oscillator specification 55
4.1 EEPROM JUMPER (J1) 55
4.2 CABLE CONNECTOR 56
Table 4.2-1: Cable Pin-Out: 56

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CHAPTER 1: INTRODUCTION

1.0 FUNCTIONAL DESCRIPTION

The PCI_HPDI32A-PRINT Board is a PCI card designed to provide print control functions for eight individual print heads. These print functions include clocking data into each print head and a programmable fire pulse for each print head. The card will rely on external position/motion inputs (quadrature encoder A/B, Zfwd, Zrev) to determine when new data is loaded and the print heads are to be fired. The fire/load conditions, as well as the individual delay firing delays and widths, are fully programmable via software control.

The PCI-HPDI32A-PRINT Board utilizes the position/motion inputs (Zfwd, Zrev, A, B) to start printing and control the head firing pulses. Printing can start or stop upon transitions of Zfwd, Zrev, or at specific position counter locations. The position counter will track motion via changes in the Quadrature encoder inputs A and B, and may be reset to zero upon transitions of the Zfwd and/or Zrev inputs.

Upon startup, the user will load the FIFO on the printer interface board with print head data. Upon being enabled, the print control logic will transfers the first block of 16-bit words to the eight print heads (each print head gets two bits of each word). The print control logic then waits for a Z input signal and/or a certain position (relative to the Z transition) to start printing. Once printing has started, the heads are fired upon transitions of the quadrature inputs (A and B). Each time the heads are fired, a new block of data is transferred to the heads in preparation for the next firing. The data in the output FIFO is replenished by the DMA controller (as needed) until the end of the print buffer is reached. If the FIFO becomes empty, the loading of data into the print heads and the firing of the print heads will stall until more data is loaded into the FIFOs. Printing will continue until the programmed Z input signal or stop position is reached.

The firing of the heads is adjustable under software control. The firing pulse can be delayed and the firing pulse width can be adjusted so that the location and 'intensity' of the head/jet firing can be fine tuned under software control. Each head firing pulse each has a separate delay circuit and a separate pulse generator, thus allowing for software programmable delay and pulse width for each of the eight Head Fire Pulses. A hold off delay may also be programmed to delay clocking new data into the print heads following the completion of the print head firing. Since data is clocked into all eight print heads simultaneously, the hold off delay time starts when the last print head has completed it's firing pulse. All of the programmable delays may be set from 0ms to 1.024ms with a resolution of 0.25us.

One set of FIFOs on the PCI-HPDI32A-PRINT is used for buffering the transmit data. Each set consists of 16 bits of data and 4 status flags. The transmit FIFOs are loaded by either the CPU or the DMA and passed to the cable outputs by the print control logic. Since the output FIFO is only 16 bits wide, the user must ensure all CPU and DMA transfers are only 16 bits wide. The 4 status flags that accompany the FIFOs are all active low ('0' being TRUE) and are as follows: Empty, Almost Empty, Almost Full, Full. The Almost Empty and the Almost Full status flags can be programmed by the software to become true at most desired levels.

The signals to and from the cable are defined as differential RS485/422 signals. The signals output to the cable are 16 data bits, 8 print head clocks, and 8 head fire pulses. In addition, the 12MHz transmit clock is always output on the cable. The position/motion signals (A, B, Zfwd, Zrev) are defined as inputs on the cable. Presently, there are 3 unused signals on the cable, and these signals will be tristated. These signals may be enabled for factory testing via software, so the user should take care not drive these unused signals to eliminate any potential contention problems. Refer to cable pin-out Table 4.2-1.

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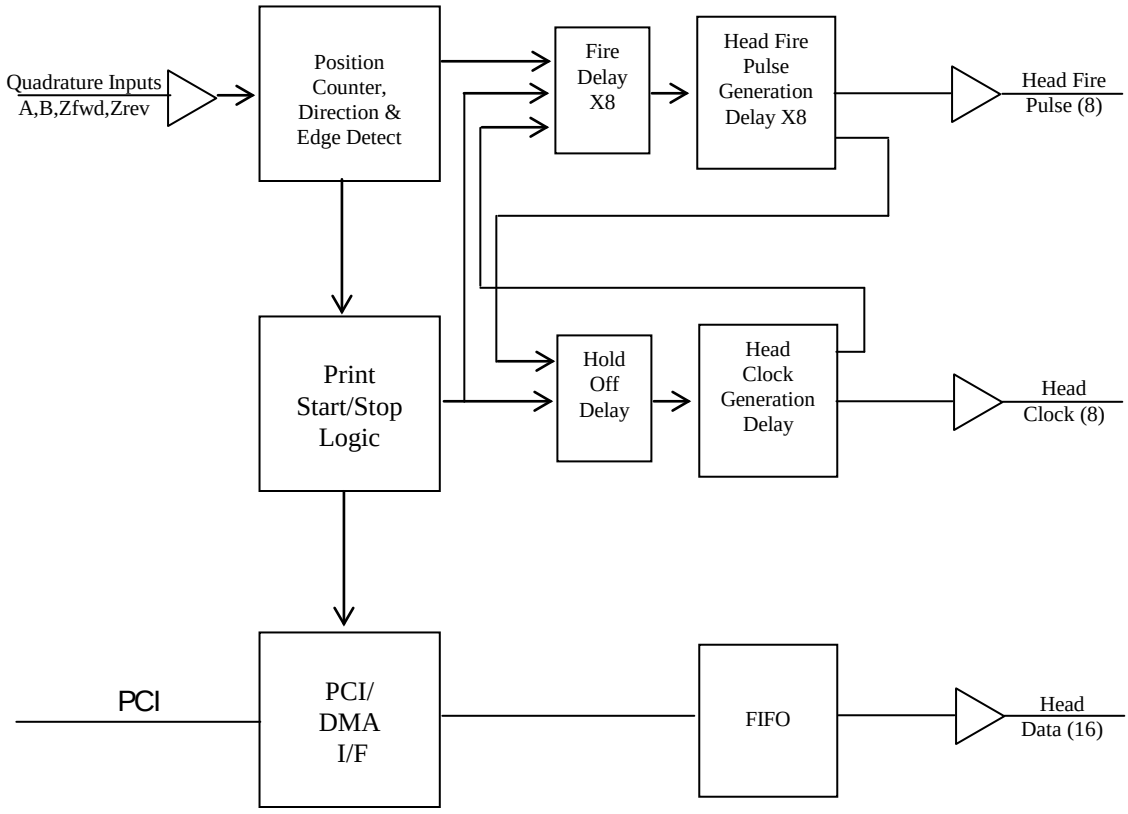


Figure 1.0-2: Block Diagram

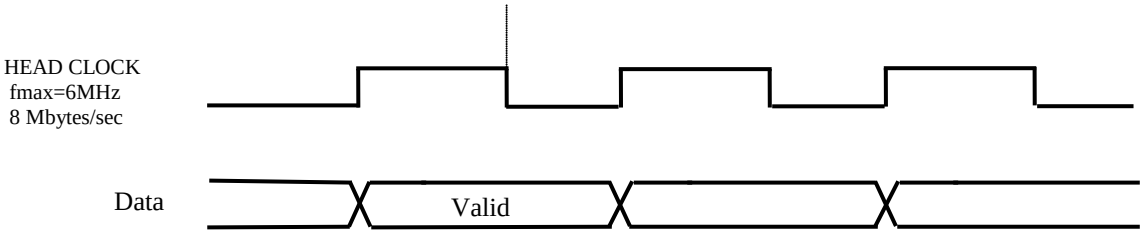
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1.1 CABLE INTERFACE

The cable interface consists of 32 bits of data, one clock, and 7 user definable bi-directional signals. All of which employ either differential I/O RS485/422 compatibility or differential pseudo ECL. Refer to cable pin-out Table 4.2-1.

1.2 FIFOS

The FIFOs on the PCI-HPDI32A-PRINT are used for buffering the transmit data. Although the board may be populated with up to eight FIFOs only two are used in this application. This set consists of 16 bits of data and 4 status flags. The transmit FIFOs are loaded by either the CPU or the DMA and read by the cable transmit control logic. The 4 status flags that accompany the FIFOs are all active low ('0' being TRUE) and are as follows: Empty, Almost Empty, Almost Full, Full. The Almost Empty and the Almost Full status flags are software programmable at almost any FIFO position.



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CHAPTER 2: REGISTERS

2.0 PCI-HPDI32A-PRINT REGISTER INFORMATION

The PCI-HPDI32A-PRINT Card complies with the **plug-n-play** concept. That is, at the time of power-up, an attempt will be made by the CPU to set up the board to meet the configuration requirements of the system. In doing this, the CPU will map the amount of I/O space requested by the PCI-HPDI32A-PRINT Card and return the configuration base address into the PCI Configuration Register (Offset 0x18) of this Board.

2.1 PCI CONFIGURATION REGISTERS

Table 2.1-1: Register Mapping

Local Side Offset Addr	Size	Access R	Access W	Register Name	Value after Reset	PCI CFG register address
0x00	D32	yes	Local Bus	Device ID/Vendor ID	0x9080/ 0x10B5 or 0x00000000	0x00
0x04	D32	yes	Bit Dep.	Status/Command	0x00010000	0x04
0x08	D32	yes	Local Bus	Class Code/Revision ID	0x(Current Rev#)068000	0x08
0x0C	D32	yes	Bit Dep.	BIST/Header Type/Latency Timer/Cache Line Size	0x00000000	0x0C
0x10	D32	yes	Bit Dep.	PCI Base Address for Memory Mapped Runtime Registers	0x00000000	0x10
0x14	D32	yes	Bit Dep.	PCI Base Address for 1 for I/O Mapped Configuration Registers	0x00000001	0x14
0x18	D32	yes	Bit Dep.	PCI Base Address 2 for Local Address Space 0	0x00000000	0x18
0x1C	D32	yes	no	PCI Base Address 3 for Local Address Space 1		0x1C
0x20	D32	yes	no	Unused Base Address		0x20
0x24	D32	yes	no	Unused Base Address		0x24
0x28	D32	yes	no	Cardbus CIS Pointer (Not Supported)		0x28
0x2C	D32	yes	no	Subsystem ID/Subsystem Vendor ID		0x2C
0x30	D32	yes	Bit Dep.	PCI Base Address to Local Expansion ROM	0x00000001	0x30
0x34	D32	yes	no	Reserved		0x34
0x38	D32	yes	no	Reserved		0x38
0x3C	D32	yes	Local Bus	Max_lat/Min_Gnt/Interrupt Pin/Interrupt Line	0x00010000	0x3C

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2.2 PLX REGISTERS

Table 2.2-1: LOCAL CONFIGURATION REGISTERS

Local Side Offset Addr	Size	Access R	Access W	Register Name	Value after Reset	PCI CFG register address
0x80	D32	yes	yes	Range for PCI to Local Address Space 0	0xFFF00000	0x00
0x84	D32	yes	yes	Local Base Address (Re-map) for PCI to Local Address Space 0	0x00000000	0x04
0x88	D32	yes	no	Mode Arbitration		0x08
0x8C	D32	yes	no	Big/Little Endian Descriptor		0x0C
0x90	D32	yes	yes	Range for PCI to Local Expansion ROM	0xFFF00000	0x10
0x94	D32	yes	Bit Dep.	Local Base Address (Re-map) for PCI to Local Expansion ROM and BREQo control	0x00000000	0x14
0x98	D32	yes	yes	Bus Region Descriptions for PCI Local Accesses	0x40030003 (Cx Mode)	0x18
0x9C	D32	yes	Bit Dep.	Range for Direct Master to PCI	0x00000000	0x1C
0xA0	D32	yes	Bit Dep.	Local Base Address for Direct Master to PCI Memory	0x00000000	0x20
0xA4	D32	yes	Bit Dep.	Local Base Address for Direct Master to PCI Memory IO/CFG	0x00000000	0x24
0xA8	D32	yes	Bit Dep.	PCI Base Address (Re-map) for Direct Master to PCI	0x00000000	0x28
0xAC	D32	yes	yes	PCI Configuration Address Register for Direct Master to PCI IO/CFG	0x00000000	0x2C
0xF0	D32	yes	yes	Range for PCI to Local Address Space 1	0x00000000	0x170
0xF4	D32	yes	yes	Local Base Address (Remap) for PCI to Local Address Space 1	0x00000000	0x174
0xF8	D32	yes	yes	Local Bus Region Descriptor (Space 1) for PCI to Local Accesses	0x00000000	0x178

Table 2.2-2: RUN TIME REGISTERS

Local Side Offset Addr	Size	Access R	Access W	Register Name	Value after reset	PCI CFG register address
0xC0	D32	yes	yes	Mailbox Register 0	0x00000000	0x40
0xC4	D32	yes	yes	Mailbox Register 1	0x00000000	0x44
0xC8	D32	yes	yes	Mailbox Register 2	0x00000000	0x48
0xCC	D32	yes	yes	Mailbox Register 3	0x00000000	0x4C
0xD0	D32	yes	yes	Mailbox Register 4	0x00000000	0x50
0xD4	D32	yes	yes	Mailbox Register 5	0x00000000	0x54
0xD8	D32	yes	yes	Mailbox Register 6	0x00000000	0x58
0xDC	D32	yes	yes	Mailbox Register 7	0x00000000	0x5C
0xE0	D32	yes	yes	PCI to Local Doorbell Register	0x00000000	0x60
0xE4	D32	yes	yes	Local to PCI Doorbell Register	0x00000000	0x64

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0xE8	D32	yes	Bit Dep.	Interrupt Control/Status	0x00000000	0x68
0xEC	D32	yes	Bit Dep.	EEPROM Control, PCI Command Codes, User I/O Control, Init Control	0x001767E	0x6C
0xF0	D32	yes	Bit Dep.	Device ID/Vendor ID	0x00	0x70
0xF4	D32	yes	Bit Dep.	Unused/Revision ID	0x00	0x74
0xC0	D32	yes	Bit Dep.	Mailbox Register 0 (1)	0x00	0x78
0xC4	D32	yes	Bit Dep.	Mailbox Register 1 (1)	0x00	0x7C

Table 2.2-3: DMA REGISTERS

Local Side Offset Addr	Size	Access R	Access W	Register Name	Value after Reset	PCI CFG register address
0x100	D32	yes	yes	DMA Ch 0 Mode	0x00000003 (Cx and Jx modes)	0x80
0x104	D32	yes	yes	DMA Ch 0 PCI Address	0x00000000	0x84
0x108	D32	yes	yes	DMA Ch 0 Local Address	0x00000000	0x88
0x10C	D32	yes	yes	DMA Ch 0 Transfer Byte Count	0x00000000	0x8C
0x110	D32	yes	yes	DMA Ch 0 Descriptor Pointer	0x00000000	0x90
0x114	D32	yes	yes	DMA Ch 1 Mode	0x00000003 (Cx and Jx modes)	0x94
0x118	D32	yes	yes	DMA Ch 1 PCI Address	0x00000000	0x98
0x11C	D32	yes	yes	DMA Ch 1 Local Address	0x00000000	0x9C
0x120	D32	yes	yes	DMA Ch 1 Transfer Byte Count	0x00000000	0xA0
0x124	D32	yes	yes	DMA Ch 1 Descriptor Pointer	0x00000000	0xA4
0x128	D32		Bit Dep.	Reserved/DMA Ch 1Command/Status Register/DMA Ch 0 Command/Status	0x00000010	0xA8
0x12C	D32	yes	Bit Dep.	Mode/ Arbitration Register	0x00000000	0xAC
0x130	D32	yes	Bit Dep.	DMA Threshold Register	0x00000000	0xB0

Table 2.2-3: MESSAGING QUEUE REGISTERS

Local Side Offset Addr	Size	Access R	Access W	Register Name	Value after reset	PCI CFG register address
0xB0	D32	yes	yes	Outbound Post Queue Interrupt Status	0x00000000	0x30
0xB4	D32	yes	yes	Outbound Post Queue Interrupt Mask	0x00000000	0x34
	D32	yes	yes	Inbound Queue Port	0x00000000	0x40
	D32	yes	yes	Outbound Queue Port	0x00000000	0x44
0x140	D32	yes	yes	Messaging Unit Configuration	0x00000000	0xC0

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0x144	D32	yes	yes	Queue Base Address	0x00000000	0xC4
0x148	D32	yes	yes	Inbound Free Head Pointer	0x00000000	0xC8
0x14C	D32	yes	yes	Inbound Free Trail Pointer	0x00000000	0xCC
0x150	D32	yes	yes	Inbound Post Head Pointer	0x00000000	0xD0
0x154	D32	yes	yes	Inbound Post Tail Pointer	0x00000000	0xD4
0x15C	D32	yes	yes	Outbound Free Head Pointer	0x00000000	0xDC
0x160	D32	yes	yes	Outbound Free Tail Pointer	0x00000000	0xE0
0x164	D32	yes	yes	Outbound Post Tail Pointer	0x00000000	0xE4
0x168	D32	yes	yes	Queue Status/Control Register	0x00000000	0xE8

2.3 PCI CONFIGURATION REGISTER BIT MAPS

2.3.1 PCI Configuration ID Register (Offset 0x00)

D0..15 Vendor ID
D16..31 Device ID

2.3.2 PCI Command Register (Offset 0x04)

D0 I/O Space
D1 Memory Space
D2 Master Enable
D3 Special Cycle
D4 Memory Write/Invalidate.
D5 VGA Palette Snoop. This bit is not supported.
D6 Parity Error Response
D7 Wait Cycle Control
D8 SERR# Enable
D9 Fast Back-to-Back Enable
D10..15 Reserved

2.3.3 PCI Status Register (Offset 0x06)

D0..5 Reserved
D6 User definable features
D7 Fast Back-to-Back Capable
D8 Master Data Parity Error Detected
D9..10 DEVSEL Timing
D11 Target Abort
D12 Received Target Abort
D13 Master Abort
D14 Signaled System Error
D15 Detected Parity Error

2.3.4 PCI Revision ID Register (Offset 0x08)

D0..7 Revision ID

2.3.5 PCI Class Code Register (Offset 0x09..0B)

D0..7 Special register level programming interface (0x00). No Interface defined.

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D8..15 Sub-class Encoding (0x80). Other bridge device.
D16..D23 Base Class Encoding other Bridge Device

2.3.6 PCI Cache Line Size Register (Offset 0x0C)

D0..7 System cache line size in units of 32-bit words.

2.3.7 PCI Latency Timer Register (Offset 0x0D)

D0..7 Latency Timer

2.3.8 PCI Header Type Register (Offset 0x0E)

D0..6 Configuration Layout Type
D7 Header Type

2.3.9 PCI Built-In Self Test (BIST) Register (PCI Offset 0x0F)

D0..3 0 means pass, non-zero means the device failed
D4..5 Reserved
D6 PCI writes a 1 to invoke BIST.
D7 Return 1 if device supports BIST, 0 if the device is not BIST compatible.

2.3.10 PCI Base Address Register for Memory Access to Runtime Registers (Offset 0x010)

D0 Memory space indicator
D1..2 Location of register:
00 - Locate anywhere in 32 bit memory address space
01 - Locate below 1 Mbyte memory address space
10 - Locate anywhere in 64 bit memory address space
11 – Reserved
Note: Hardcoded to 0.
D3 Prefectchable. Note: Hardcoded to 0.
D4..7 Memory Base Address. Note: Hardcoded to 0.
D8..31 Memory Base Address

2.3.11 PCI Base Address Register for I/O Access to Runtime Registers (Offset 0x14)

D0 Memory space indicator
D1 Reserved
D2..7 I/O Base Address. Note: Hardcoded to 0.
D8..31 I/O Base Address. Note: Hardcoded to 0.

2.3.12 PCI Base Address Register for Memory Access to Local Address Space 0 (Offset 0x18)

D0 Memory space indicator
D1..2 Location of register:

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00 - Locate anywhere in 32 bit memory address space
01 - Locate below 1 Mbyte memory address space
10 - Locate anywhere in 64 bit memory address space
11 - Reserved
D3 Prefetchable
D4..31 Memory Base Address

2.3.13 PCI Base Address Register for Memory Access to Local Address Space 1 (Offset 0x1C)

D0 Memory Space Indicator
D1..2 Reserved
D3 Prefetchable
D4..31 Memory Base Address

2.3.14 PCI Base Address Register (Offset 0x20)

D0..31 Reserved

2.3.15 PCI Base Address Register (Offset 0x24)

D0..31 Reserved

2.3.16 PCI Cardbus CIS Pointer Register (Offset 0x28)

D0..31 Reserved

2.3.17 PCI Subsystem Vendor ID Register (Offset 0x2C)

D0..15 Reserved

2.3.18 PCI Subsystem ID Register (Offset 0x2E)

D0..15 Reserved

2.3.19 PCI Expansion ROM Base Register (Offset 0x30)

D0 Address Decode Enable
D1..10 Reserved
D11..31 Expansion ROM Base Address (upper 21 bits)

2.3.20 PCI Interrupt Line Register (Offset 0x3C)

D0..7 Interrupt Line Routing Value

2.3.21 PCI Interrupt Pin Register (Offset 0x3D)

D0..7 Interrupt Pin register

2.3.22 PCI Min_Gnt Register (Offset 0x3E)

D0..7 Min_Gnt

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2.3.23 PCI Max_Lat Register (Offset 0x3F)

D0..7 Max_Lat

2.4 LOCAL CONFIGURATION REGISTERS

2.4.1 Local Address Space 0 Range Register for PCI to Local bus (PCI 0x00) (LOC 0x80)

D0 Memory space indicator
D1..2 If mapped into memory space, encoded as follows:
2/1 Meaning
00 locate anywhere in 32 bit PCI address space
01 locate below 1 Meg in PCI address space
10 locate anywhere in 64 bit PCI address space
11 Reserved
If mapped into I/O space,
bit 1 must be 0.
bit 2 is included with bits 3 through 31 to indicate decoding range.
D3 If mapped into memory space, a 1 indicates that reads are pre-fetchable.
If mapped into I/O space, bit is included with bits 2 through 31 to indicate decoding range.
D4..31 Specifies which PCI address bits will be used to decode a PCI access to local bus space 0.

2.4.2 Local Address Space 0 Local Base Address (Re-map) Register for PCI to Local Bus (PCI 0x04) (LOC 0x84)

D0 Space 0 Enable
D1 Reserved
D2..3 If local space is mapped into memory space, bits are not used.
If mapped into I/O space, bit is included with bits 4 through 31 for re-mapping.
D4..31 Re-map of PCI Address to Local Address Space 0 into a Local Address Space.

2.4.3 Mode/Arbitration Register (PCI 0x08) (LOC 0x88)

D0..7 Local bus Latency Timer
D8..15 Local bus Pause Timer
D16 Local bus Latency Timer Enable
D17 Local bus Pause Timer Enable
D18 Local bus BREQ Enable
D19..20 DMA Channel Priority
D21 Local bus direct slave give up bus mode
D22 Direct slave LLOCKo# Enable
D23 PCI Request Mode
D24 PCI Rev 2.1 Mode
D25 PCI Read No Write Mode
D26 PCI Read with Write Flush Mode
D27 Gate the Local Bus Latency Timer with BREQ
D28 PCI Read No Flush Mode
D29 Reads Device or Vendor ID
D30..31 Reserved

2.4.4 Big/Little Endian Descriptor Register (PCI 0x0C) (LOC 0x8C)

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D0 Configuration Register Big Endian Mode
D1 Direct Master Big Endian Mode
D2 Direct Slave Address Space 0 Big Endian Mode
D3 Direct Slave Address Expansion ROM 0 Big Endian Mode
D4 Big Endian Byte Lane Mode
D5 Direct Slave Address Space 1 Big Endian Mode
D6 DMA Channel 1 Big Endian Mode
D7 DMA Channel 0 Big Endian Mode
D8..31 Reserved

2.4.5 Local Expansion ROM Range Register for PCI to Local Bus (PCI 0x10) (LOC 0x90)

D0..10 Reserved
D11..31 Specifies which PCI address bits will be used to decode a PCI to local bus expansion ROM.

2.4.6 Local Expansion ROM Local Base Address (Re-map) register for PCI to Local Bus and BREQo Control (PCI 0x14) (LOC 0x94)

D0..3 Direct Slave BREQo Delay Clocks
D4 Local Bus BREQo Enable
D6..10 Reserved
D11..31 Re-map of PCI Expansion ROM space into a Local address space

2.4.7 Local Address Space 0/Expansion ROM Bus Region Descriptor Register (PCI 0x18) (LOC 0x98)

D0..1 Memory Space 0 Local Bus Width
D2..5 Memory Space 0 Internal Wait States (data to data)
D6 Memory Space 0 Input Enable
D7 Memory Space 0 Bterm Input Enable
D8 Memory Space 0 Prefetch Disable
D9 Expansion ROM Space Prefetch Disable
D10 Read Prefetch Count Enable
D11..14 Prefetch Counter
D15 Reserved
D16..17 Expansion ROM Space Local Bus Width
D18..21 Expansion ROM Space Internal Wait States
D22 Expansion ROM Space Ready Input Enable
D23 Expansion ROM Space Bterm Input Enable
D24 Memory Space 0 Burst Enable
D25 Extra Long Load from serial Enable
D26 Expansion ROM Space Burst Enable
D27 Direct Slave PCI write mode
D28..31 PCI Target Retry Delay Clocks

2.4.8 Local Range register for Direct Master to PCI (PCI 0x1C) (LOC 0x9C)

D0..15 Reserved
D16..31 Specifies which local address bits will be used to decode a Local to PCI bus access.

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2.4.9 Local Bus Base Address register for Direct Master to PCI Memory (PCI 0x20) (LOC 0xA0)

D0..15 Reserved
D16..31 Assigns a value to the bits which will be used to decode a Local to PCI memory access.

2.4.10 Local Base Address for Direct Master to PCI IO/CFG Register (PCI 0x24) (LOC 0xA4)

D0..15 Reserved
D16..31 Assigns a value to the bits which will be used to decode a Local PCI I/O or configuration access.

2.4.11 PCI Base Address (Re-map) register for Direct Master to PCI Memory (PCI 0x28) (LOC 0xA8)

D0 Direct Memory Access Enable
D1 Direct Master I/O Access Enable
D2 LLOCK# Input Enable
D3, 12 Direct Master Red Prefetch Size control
D4 Direct Master PCI read mode
D5..8, 10 Programmable Almost Full flag
D9 Write and Invalidate Mode
D11 Direct Master Prefetch Limit
D13 I/O Remap Select
D14..15 Direct Master Write Delay
D16..31 Re-map of Local to PCI space into a PCI address space

2.4.12 PCI Configuration Address Register for Direct Master to PCI IO/CFG (PCI 0x2C) (LOC 0xAC)

D0..1 Configuration Type. 00 = Type 0 01 = Type 1
D2..7 Register Number
D8..10 Function Number
D11..15 Device Number
D16..23 Bus Number
D24..30 Reserved
D31 Configuration Enable

2.4.13 Local Address Space 1 Range Register for PCI to Local Bus (PCI 0xF0) (LOC 0x170)

D0 Memory Space Indicator
D1..2 Encoded for Memory Space
D3 If mapped into memory space, a value of 1 indicates reads are prefetchable. If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.
D4..31 Specifies which PCI address bits to use for decoding a PCI access to local bus space 1.

2.4.14 Local Address Space 1 Local Base Address (Remap) Register (PCI 0xF4) (LOC 0x174)

D0 Space 1 Enable
D1 Reserved
D2..3 If local space 1 is mapped into memory space, bits are not used. If mapped I/O space, bit is included with bits [31:4] for remapping.
D4..31 Remap of PCI Address to Local Address space 1 into a Local Address Space.

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2.4.15 Local Address Space 1 Bus Region Descriptor Register (PCI 0xF8) (LOC 0x178)

D0..1 Memory Space 1 Local Bus Width
D2..5 Memory space 1 Internal Wait States
D6 Memory space 1 Ready Input Enable
D7 Memory space 1 BTERM# Input Enable
D8 Memory space 1 Burst Enable
D9 Memory space 1 Prefetch Disable
D10 Read Prefetch Count Enable
D11..14 Prefetch Counter
D15..31 Reserved

2.5 RUNTIME REGISTERS

2.5.1 Mailbox Register 0 (PCI 0x40) (LOC 0xC0)

D0..31 32 bit mailbox register

2.5.2 Mailbox Register 1 (PCI 0x44) (LOC 0xC4)

D0..31 32 bit mailbox register

2.5.3 Mailbox Register 2 (PCI 0x48) (LOC 0xC8)

D0..31 32 bit mailbox register

2.5.4 Mailbox Register 3 (PCI 0x4C) (LOC 0xCC)

D0..31 32 bit mailbox register

2.5.5 Mailbox Register 4 (PCI 0x50) (LOC 0xD0)

D0..31 32 bit mailbox register

2.5.6 Mailbox Register 5 (PCI 0x54) (LOC 0xD4)

D0..31 32 bit mailbox register

2.5.7 Mailbox Register 6 (PCI 0x58) (LOC 0xD8)

D0..31 32 bit mailbox register

2.5.8 Mailbox Register 7 (PCI 0x5C) (LOC 0xDC)

D0..31 32 bit mailbox register

2.5.9 PCI to Local Doorbell Register Description (PCI 0x60) (LOC 0xE0)

D0..31 Doorbell register

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2.5.10 Local to PCI Doorbell Register Description (PCI 0x64) (LOC 0xE4)

D0..31 Doorbell register

2.5.11 Interrupt Control /Status (PCI 0x68) (LOC 0xE8)

D0 Enable Local bus LSERR#
D1 Enable Local bus LSERR# when a PCI parity error occurs during a PCI9080 Master Transfer or a PCI9080 Slave access.
D2 Generate PCI Bus SERR#
D3 Mailbox Interrupt Enable
D4..7 Reserved
D8 PCI Interrupt Enable
D9 PCI doorbell interrupt enable
D10 PCI Abort interrupt enable
D11 PCI local interrupt enable
D12 Retry Abort Enable
D13 A value of 1 indicates that the PCI doorbell interrupt is active.
D14 A value of 1 indicates that the PCI abort interrupt is active.
D15 A value of 1 indicates that the PCI local interrupt input is active.
D16 Local interrupt output enable
D17 Local doorbell interrupt enable
D18 Local DMA channel 0 interrupt enable
D19 Local DMA channel 1 interrupt enable
D20 A value of 1 indicates that the Local doorbell interrupt is active.
D21 A value of 1 indicates that the DMA ch 0 interrupt is active.
D22 A value of 1 indicates that the DMA ch 1 interrupt is active.
D23 A value of 1 indicates that the BIST interrupt is active.
D24 A value of 0 indicates that a Direct Master was the bus master during a Master or Target abort.
D25 A value of 0 indicates that DMA CH 0 was the bus master during a Master or Target abort.
D26 A value of 0 indicates that DMA CH 1 was the bus master during a Master or Target abort.
D27 A value of 0 indicates that a Target Abort was generated by the PCI9080 after 256 consecutive Master retries to a Target.
D28 A value of 1 indicates PCI wrote data to the MailBox #0.
D29 A value of 1 indicates PCI wrote data to the MailBox #1.
D30 A value of 1 indicates PCI wrote data to the Mailbox #2.
D31 A value of 1 indicates PCI wrote data to the Mailbox #3.

2.5.12 Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI 0x6C) (LOC 0xEC)

D0..3 PCI Read Command Code for DMA
D4..7 PCI Write Command Code for DMA
D8..11 PCI Memory Read Command Code for Direct Master
D12..15 PCI Memory Write Command Code for Direct Master
D16 General Purpose Output
D17 General Purpose Input
D18..23 Reserved
D24 Serial EEPROM clock for Local or PCI bus reads or writes to Serial EEPROM.

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D25 Serial EEPROM chip select
D26 Write bit to serial EEPROM
D27 Read serial EEPROM data bit
D28 Serial EEPROM present
D29 Reload Configuration Registers
D30 PCI Adapter Software Reset
D31 Local Init Status, 1 = local init done.

2.5.13 PCI Permanent Configuration ID Register (PCI 0x70) (LOC 0xF0)

D0..15 Permanent Vendor ID
D16..31 Permanent Device ID

2.5.14 PCI Permanent Revision ID Register (PCI 0x74) (LOC 0xF4)

D0..7 Permanent Revision ID

2.6 LOCAL DMA REGISTERS

2.6.1 DMA Channel 0 Mode Register (LOC 0x100)

D0..1 Local Bus Width
D2..5 Internal Wait States (data to data)
D6 Ready Input Enable
D7 Bterm# Input Enable
D8 Local Burst Enable
D9 Chaining
D10 Done Interrupt Enable
D11 Local Addressing Mode
D12 Demand Mode
D13 Write and Invalidate Mode for DMA Transfers
D14 DMA EOT (End Of Transfer) Enable.
D15 DMA Stop Data Transfer Mode
D16 DMA Clear Count Mode
D17 DMA Channel 0 Interrupt Select
D18..31 Reserved

2.6.2 DMA Channel 0 PCI Address Register (LOC 0x104)

D0..31 PCI Address Register

2.6.3 DMA Channel 0 Local Address Register (LOC 0x108)

D0..31 Local Address Register

2.6.4 DMA Channel 0 Transfer Size (Bytes) Register (LOC 0x10C)

D0..22 DMA Transfer Size

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D23..31 Reserved

2.6.5 DMA Channel 0 Descriptor Pointer Register (LOC 0x110)

D0 Descriptor Location
D1 End of Chain
D2 Interrupt after Terminal Count
D3 Direction of transfer
D4..31 Next Descriptor Address

2.6.6 DMA Channel 1 Mode Register (LOC 0x114)

D0..1 Local Bus Width
D2..5 Internal Wait States (data to data).
D6 Ready Input Enable
D7 Bterm Input Enable
D8 Local Burst Enable
D9 Chaining
D10 Done Interrupt Enable
D11 Local Addressing Mode
D12 Demand Mode
D13 Write and Invalidate Mode for DMA Transfers
D14 DMA EOT (End of Transfer) Enable
D15 DMA Stop Data Transfer Mode
D16 DMA Clear Count Mode
D17 DMA Channel 1 Interrupt Select
D18..31 Reserved

2.6.7 DMA Channel 1 PCI Data Address Register (LOC 0x118)

D0..31 PCI Data Address Register

2.6.8 DMA Channel 1 Local Data Address Register (LOC 0x11C)

D0..31 Local Data Address Register

2.6.9 DMA Channel 1 Transfer Size (bytes) register (LOC 0x120)

D0..22 DMA Transfer Size (Bytes)
D23..31 Reserved

2.6.10 DMA Channel 1 Descriptor Pointer Register (LOC 0x124)

D0 Descriptor Location
D1 End of Chain
D2 Interrupt after Terminal Count
D3 Direction of transfer
D4..31 Next Descriptor Address

2.6.11 DMA Command/Status Register (LOC 0x128)

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D0 Channel 0 Enable
D1 Channel 0 Control
D2 Channel 0 Abort
D3 Clear Interrupt
D4 Channel 0 Done
D5..7 Reserved

2.6.12 DMA Channel 1 Command/Status Register 0 (LOC 0x128)

D0 Channel 1 Enable
D1 Channel 1 Start
D2 Channel 1 Abort
D3 Clear Interrupt
D4 Channel 1 Done
D5..7 Reserved

2.6.13 DMA Arbitration Register 1 (LOC 0x12C) same as Mode /Arbitration Register at address (LOC 0x88)

D0..3 DMA Channel 0 PCI to Local Almost Full (C0PLAF)
D4..7 DMA Channel 0 Local to PCI Almost Empty (C0LPAE)
D8..11 DMA Channel 0 Local to PCI Almost Full (C0LPAF)
D12..15 DMA Channel 0 PCI to Local Almost Empty (C0PLAE)
D16..19 DMA Channel 1 PCI to Local Almost Full (C1PLAF)
D20..23 DMA Channel 1 Local to PCI Almost Empty (C1LPAE)
D24..27 DMA Channel 1 PCI to Local Almost Full (C1LPAF)
D28..31 DMA Channel 1 PCI to Local Almost Empty (C1PLAE)

2.7 MESSAGING QUEUE REGISTERS

2.7.1 Outbound Post List FIFO Interrupt Status Register (PCI 0x30) (LOC 0xB0)

D0..2 Reserved
D3 Outbound Post List FIFO Interrupt.
D4..31 Reserved

2.7.2 Outbound Post List FIFO Interrupt Status Register (PCI 0x34) (LOC 0xB4)

D0..2 Reserved
D3 Outbound Post List FIFO Interrupt Mask.
D4..31 Reserved

2.7.3 Inbound Queue Port Register (PCI 0x40)

D0..31 Value written by PCI master is stored into the Inbound Post List FIFO.

2.7.4 Outbound Queue Port Register (PCI 0x44)

D0..31 Value written by PCI master is stored into the Outbound Free List FIFO.

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2.7.5 Messaging Queue Configuration Register (PCI 0xC0) (LOC 0x140)

D0 Queue Enable
D1..5 Circular FIFO Size
D6..31 Reserved

2.7.6 Queue Base Address Register (PCI 0xC4) (LOC 0x144)

D0..19 Reserved
D20..31 Queue Base Address

2.7.7 Inbound Free Head Pointer Register (PCI 0xC8) (LOC 0x148)

D0..1 Reserved
D2..19 Inbound Free Head Pointer
D20..31 Queue Base Address

2.7.8 Inbound Free Head Tail Register (PCI 0xCC) (LOC 0x14C)

D0..1 Reserved
D2..19 Inbound Free Tail Pointer
D20..31 Queue Base Address

2.7.9 Inbound Post Head Pointer Register (PCI 0xD0) (LOC 0x150)

D0..1 Reserved
D2..19 Inbound Post Head Pointer
D20..31 Queue Base Address

2.7.10 Inbound Post Tail Pointer Register (PCI 0xD4) (LOC 0x154)

D0..1 Reserved
D2..19 Inbound Post Tail Pointer
D20..31 Queue Base Address

2.7.11 Outbound Free Head Pointer Register (PCI 0xD8) (LOC 0x158)

D0..1 Reserved
D2..19 Outbound Free Head Pointer
D20..31 Queue Base Address

2.7.12 Outbound Free Tail Pointer Register (PCI 0xDC) (LOC 0x15C)

D0..1 Reserved
D2..19 Outbound Free Tail Pointer
D20..31 Queue Base Address

2.7.13 Outbound Post Head Pointer Register (PCI 0xE0) (LOC 0x160)

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D0..1 Reserved
D2..19 Outbound Post Head Pointer
D20..31 Queue Base Address

2.7.14 Outbound Post Tail Pointer Register (PCI 0xE4) (LOC 0x164)

D0..1 Reserved
D2..19 Outbound Post Tail Pointer
D20..31 Queue Base Address

2.7.15 Queue Status/Control Register (PCI 0xE8) (LOC 0x168)

D0 I(2)O Decode Enable
D1 Queue Local Space Select
D2 Outbound Post List FIFO Prefetch Enable
D3 Inbound Free List FIFO Prefetch Enable
D4 Inbound Post List FIFO Interrupt Mask
D5 Inbound Post List FIFO Interrupt
D6 Outbound Free List FIFO Overflow Interrupt Mask
D7 Outbound Free List FIFO Overflow Interrupt
D8..31 Unused

2.8 PCI CONFIGURATION REGISTER BIT DESCRIPTIONS

All registers may be written to or read from in byte, word, or Lword accesses.

2.8.1 PCI Configuration ID Register (Offset 0x00)

D0..15 Vendor ID- Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX (0x10B5) if no serial EEPROM is present and pin NB# (no local bus initialization) is asserted low.
D16..31 Device ID - Identifies the particular device. Defaults to the PLX part number for PCI interface chip (0x9080) if no serial EEPROM is present and pin NB#(no local bus initialization) is asserted low.

2.8.2 PCI Command Register (Offset 0x04)

D0 I/O Space
A value of 1 allows the device to respond to I/O space accesses.
A value of 0 disables the device from responding to I/O space accesses.
D1 Memory Space
A value of 1 allows the device to respond to memory space accesses.
A value of 0 disables the device from responding to memory space accesses.
D2 Master Enable. Controls a device's ability to act as a master on the PCI bus.
A value of 1 allows the device to behave as a bus master.
A value of 0 disables the device from generating bus master accesses.
This bit must be set for the PCI 9080 to perform Direct Master or DMA cycles.
D3 Special Cycle. (This bit is not supported.)
D4 Memory Write/Invalidate.
A value of 1 enables memory write/invalidate.

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A value of 0 disables memory write/invalidate.

D5 VGA Palette Snoop. (This bit is not supported.)

D6 Parity Error Response

A value of 0 indicates that a parity error is ignored and operation continues.
A value of 1 indicates that parity checking is enabled.

D7 Wait Cycle Control. Controls whether the device does address/data stepping.

A 0 value indicates the device never does stepping.
A value of 1 indicates that the device always does stepping.

Note: *Hardcoded to 0.*

D8 SERR# Enable

A value of 1 enables the SERR# driver.
A value of 0 disables the driver.

D9 Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus.

A value of 1 indicates that fast back-to-back transfers can occur to any agent on the bus.
A value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.

D10..15 Reserved

2.8.3 PCI Status Register (Offset 0x06)

D0..5 Reserved

D6 If high, supports User definable features. This bit can only be written from the local side. It is read-only from the PCI side.

D7 Fast Back-to-Back Capable.

When this bit is set to a 1, it indicates the adapter can accept fast back-to-back transactions.
A 0 indicates the adapter cannot.

D8 Master Data Parity Error Detected

This bit is set to a 1 when three conditions are met:
1. the PCI9080 asserted PERR# itself or observed PERR# asserted.
2. the PCI9080 was the bus master for the operation in which the error occurred.
3. the Parity Error Response bit in the Command Register is set.

Writing a 1 to this bit clears the bit to a 0.

D9..10 DEVSEL Timing. Indicates timing for DEVSEL# assertion.

A value of 01 indicates a medium decode.

Note: *Hardcode to 01.*

D11 Target Abort

When this bit is set to a 1, this bit indicates the PCI9080 has signaled a target abort.
Writing a 1 to this bit clears the bit (0).

D12 Received Target Abort

When set to a 1, this bit indicates the PCI9080 has signaled a target abort.
Writing a 1 to this bit clears the bit (0).

D13 Master Abort

When set to a 1, this bit indicates the PCI9080 has generated a master abort signal.
Writing a 1 to this bit clears the bit (0).

D14 Signal System Error

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When set to a 1, this bit indicates the PCI9080 has reported a system error on the SERR# signal.

Writing a 1 to this bit clears the bit (0).

D15 Detected Parity Error

When set to a 1, this bit indicates the PCI9080 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear). One of three conditions can cause this bit to be set:

1. the PCI9080 detected a parity error during a PCI address phase.
2. the PCI9080 detected a data parity error when it was the target of a write.
3. the PCI9080 detected a data parity error when performing a master read operation.

Writing a 1 to this bit clears the bit (0).

2.8.4 PCI Revision ID Register (Offset 0x08)

D0..7 Revision ID. The silicon revision of the PCI9080.

2.8.5 PCI Class Code Register (Offset 0x09 - 0B)

D0..7 Register level programming interface 0x00 = Queue Ports at 0x40 and 0x44.
0x01 = Queue Ports at 0x40 and 0x44, and Int Status and Int Mask at 0x30 and 0x34, respectively.

D8..15 Sub-class Code 0x80 = Other bridge device, 0x00 = I(2)O Device.

D16..D23 Base Class Code. 0x06 = Bridge Device, 0x0E = I(2)O controller.

2.8.6 PCI Cache Line Size Register (Offset 0x0C)

D0..7 System cache line size in units of 32-bit words.

2.8.7 PCI Latency Timer Register (Offset 0x0D)

D0..7 PCI Latency Timer. Units of PCI bus clocks, the amount of time the PCI9080, as a bus master, can burst data on the PCI bus.

2.8.8 PCI Header Type Register (Offset 0x0E)

D0..6 Configuration Layout Type. Specifies the layout of bits 0x10 through 0x3F in configuration space. Only one encoding 0 is defined. All other encodings are reserved.

D7 Header Type.

A 1 indicates multiple functions.

A 0 indicates a single function.

2.8.9 PCI Built-In Self Test (BIST) Register (PCI Offset 0x0F)

D0..3 A value of 0 means the device has passed its test.
Non-zero values mean the device failed.
Device specific failure codes can be encoded in the non-zero value.

D4..5 Reserved, Device returns 0.

D6 PCI writes a 1 to invoke BIST. Generates an interrupt to local bus. Local bus

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resets the bit when BIST is complete. Software should fail device if BIST is not complete after 2 seconds.
Refer to Runtime registers for interrupt control/status.

D7 Return 1 if device supports BIST.
Return 0 if the device is not BIST compatible.

2.8.10 PCI Base Address Register for Memory Access to Runtime Registers (Offset 0x010)

D0 Memory space indicator
A value of 0 indicates register maps into Memory space.
A value of 1 indicates the register maps into I/O space
Note: *Hardcoded to 0.*

D1..2 Location of register:
00 - Locate anywhere in 32 bit memory address space
01 - Locate below 1 Mbyte memory address space
10 - Locate anywhere in 64 bit memory address space
11 – Reserved
Note: *Hardcoded to 0.*

D3 Prefectchable.
A value of 1 indicates there are no side effects on reads. This bit has no effect on the operation of thPCI 9080.
Note: *Hardcoded to 0.*

D4..7 Memory Base Address.
Memory base address for access to Local, Runtime and DMA registers. (default is 256 bytes.)
Note: *Hardcoded to 0.*

D8..31 Memory Base Address.
Memory base address for access to Local, Runtime, and DMA registers.

2.8.11 PCI Base Address Register for I/O Access to Runtime Registers (Offset 0x14)

D0 Memory space indicator
A value of 0 indicates register maps into Memory space.
A value of 1 indicates the register maps into I/O space.
Note: *Hardcoded to 1.*

D1 Reserved

D2..7 I/O Base Address.
Base Address for I/O access to runtime registers. (Minimum Block Size = 128 bytes.)
Note: *Hardcoded to 0.*

D8..31 I/O Base Address.
Base Address for I/O access to Local, Runtime, and DMA Registers.

2.8.12 PCI Base Address Register for Memory Access to Local Address Space 0 (Offset 0x18)

D0 Memory space indicator
A value of 0 indicates register maps into Memory space.
A value of 1 indicates the register maps into I/O space.
(Specified in Local Address Space 0 Range Register, LOC 0x80.)

D1..2 Location of register (if memory space). Location values:
00 - Locate anywhere in 32 bit memory address space
01 - Locate below 1 Mbyte memory address space
10 - Locate anywhere in 64 bit memory address space
11 - Reserved
(Specified in Local Address Space 0 Range Register, LOC 0x80.)

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D3 Prefetchable (if memory space)

A value of 1 indicates there are no side effects on reads.

This bit reflects the value of bit 3 in the LASORR register and provides only status to the system. This bit has no effect on the operation of the PCI 9080. Prefetching features of this address space are controlled by the associated Bus Region Descriptor Register. (Specified in LASORR register.)

If I/O Space, bit 3 is included in the base address.

D4..31 Memory Base Address

Memory base address for access to Local Address Space 0.

2.8.13 PCI Base Address Register for Memory Accesses to Local Address Space 1 (Offset 0x1C)

D0 Memory Space Indicator

A value of 0 indicates register maps into memory space.

A value of 1 indicates register maps into I/O space.

(Specified in LAS1RR register)

D1..2 Location of Register. Location values:

00 - Locate anywhere in 32 bit memory address space

01 - Locate below 1 Mbyte memory address space

10 - Locate anywhere in 64 bit memory address space

11 - Reserved

(Specified in LAS1RR register)

If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.

2.8.14 PCI Base Address Register (Offset 0x20)

D0..31 Reserved

2.8.15 PCI Base Address Register (Offset 0x24)

D0..31 Reserved

2.8.16 PCI Base Cardbus CIS Pointer Register (Offset 0x28)

D0..31 Cardbus Information Structure Pointer for PCMCIA. (Not supported.)

2.8.17 PCI Subsystem Vendor ID Register (Offset 0x2C)

D0..31 Subsystem Vendor ID (unique add-in board Vendor ID).

2.8.18 PCI Subsystem ID Register (Offset 0x2E)

D0..31 Subsystem ID (unique add-in board Device D).

2.8.19 PCI Expansion ROM Base Register (Offset 0x30)

D0 Address Decode Enable

A value of 1 indicates the device accepts accesses to the expansion ROM address.

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A value of 0 indicates the device does not accept accesses to expansion ROM space.
Should be set to 1 by PCI host if expansion ROM is present.

D1..10 Reserved

D11..31 Expansion ROM Base Address (upper 21bits)

2.8.20 PCI Interrupt Line Register (Offset 0x3C)

D0..7 Interrupt Line Routing Value.
Indicates which input of the system interrupt controller(s) to which the interrupt line of the device is connected.

2.8.21 PCI Interrupt Pin Register (Offset 0x3D)

D0..7 Interrupt Pin register. Indicates which interrupt pin the device uses.
The following values are decoded:

0=No Interrupt Pin
1=INTA#
2=INTB#
3=INTC#
4=INTD#

Note: *PCI 9080 supports only one PCI interrupt pin (INTA#).*

2.8.22 PCI Min_Gnt Register (Offset 0x3E)

D0..7 Min_Gnt.
Used to specify how long a burst period the device needs assuming a clock rate of 33 MHz. Value is multiple of ¼ use increments.

2.8.23 PCI Max_Lat Register (Offset 0x3F)

D0..7 Max_Lat.
Specifies how often the device must gain access to the PCI bus. Value is multiple of ¼ use increments.

2.9 LOCAL CONFIGURATION REGISTERS BIT DESCRIPTIONS

2.9.1 Local Address Space 0 Range Register for PCI to Local bus (PCI 0x00) (LOC 0x80)

D0 Memory space indicator
A value of 0 indicates Local address space 0 maps into PCI memory space.
A value of 1 indicates address space 0 maps into PCI I/O space.

D1..2 If mapped into memory space, encoded as follows (D1 being the LSB):
Meaning

00-locate anywhere in 32 bit PCI address space
01-locate below 1 Meg in PCI address space
10-locate anywhere in 64 bit PCI address space
11-reserved

If mapped into I/O space, bit 1 must be a 0.
Bit 2 is included with bits 3 through 31 to indicate decoding range.

D3 If mapped into memory space, a value of 1 indicates that reads are pre-fetchable (bit has no effect on the PCI9080, but it is used for system status). If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.

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If mapped into I/O space, bit is included with bits 2 through 31 to indicate decoding range.

D4..31 Specifies which PCI address bits to use for decoding a PCI access to local bus space 0. Each bit corresponds to a PCI address bit. Bit 31 corresponds to Address bit 31. Write a value of 1 to all others (used in conjunction with PCI Configuration register 0x18). Default is 1 Meg.

2.9.2 Local Address Space 0 Local Base Address (Re-map) Register for PCI to Local Bus (PCI 0x04) (LOC 0x84)

D0 Space 0 Enable

A 1 value enables decoding of PCI addresses for Direct Slave access to local space 0.

A value of 0 disables Decode.

If this bit is set to 0, the PCI BIOS may not allocate (assign) the base address for Space 0.
Note: *Must be set to 1 for any Direct Slave access to Space 0.*

D1 Reserved

D2..3 If local space 0 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits 4 through 31 for re-mapping.

D4..31 Re-map of PCI Address to Local Address Space 0 into a Local Address Space.
The bits in this register re-map (replace) the PCI Address bits used in decode as the Local Address bits.
Note: *Remap Address value must be multiple of Range (not the Range register)*

2.9.3 Mode/Arbitration Register (PCI 0x08) (LOC 0x88)

D0..7 Local bus Latency Timer
Number of local bus clock cycles before negating HOLD and releasing the local bus. This timer is also used with bit 27 to delay BREQ input to give up the local bus only when this timer expires.

D8..15 Local bus Pause Timer
Number of local bus clock cycles before reasserting HOLD after releasing the local bus.
Note: *Applicable only to DMA operation.*

D16 Local bus Latency Timer Enable

A value of 1 enables latency timer.

D17 Local bus Pause Timer Enable

A value of 1 enables pause timer.

D18 Local bus BREQ Enable

A value of 1 enables local bus BREQ input. When the BREQ input is active, PCI 9080 negates HOLD and releases the local bus.

D19..20 DMA Channel Priority

A value of 00 indicates a rotational priority scheme.
A value of 01 indicates Channel 0 has priority.
A value of 10 indicates Channel 1 has priority.
A value of 11 is reserved.

D21 Local bus direct slave give up bus mode

When set to 1, PCI 9080 negates HOLD and releases the local bus when the Direct Slave write FIFO becomes empty during a Direct Slave write or when the Direct Slave read FIFO becomes full during a Direct Slave read.

D22 Direct slave LLOCKo# Enable

A value of 1 enables PCI Direct Slave locked sequences.

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A value of 0 disables Direct Slave locked sequences.

D23 PCI Request Mode

A value of 1 causes PCI9080 to negate REQ when it asserts FRAME during a master cycle.

A value of 0 causes PCI 9080 to leave REQ asserted for the entire bus master cycle.

D24 PCI Rev 2.1 Mode

When set to 1, PCI 9080 operates in Delayed Transaction mode for Direct Slave Reads. PCI 9080 issues a RETRY and prefetches the read data.

D25 PCI Read No Write Mode

A value of 1 forces a retry on writes if read is pending.

A value of 0 allows writes to occur while read is pending.

D26 PCI Read with Write Flush Mode

A value of 1 submits a request to flush a pending read cycle if a write cycle is detected.

A value of 0 submits a request to not effect pending reads when a write cycle occurs. (PCI v2.1 compatible)

D27 Gate the Local Bus Latency Timer with BREQ

If this bit is set to 0, PCI 9080 gives up the local bus during Direct Slave or DMA transfer after the current cycle (if enabled and BREQ is sampled).

If this bit is set to 1, PCI 9080 gives up the local bus only (if BREQ is sampled) and the Local Bus Latency Timer is enabled and expires during Direct Slave or DMA transfer.

D28 PCI Read No Flush Mode

A value of 1 submits request to not flush the read FIFO if PCI read cycle completes (Read Ahead mode).

A value of 0 submits request to flush read FIFO if PCI read cycle completes.

D29 Reads Device or Vendor ID

If set to 0, reads from the PCI Configuration Register address 0x00 and returns the Device ID and Vendor ID.

If set to 1, reads from the PCI Configuration Register address 0x00 and returns the Subsystem and Subsystem Vendor ID.

D30..31 Reserved

2.9.4 Local Register (PCI 0x0C) (LOC 0x8C)

D0 Configuration Register Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for local accesses to the configuration registers.

A value of 0 specifies Little Endian ordering. Big Endian mode can be specified for configuration register accesses by asserting the BIGEND# pin during the address phase of the access.

D1 Direct Master Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for Direct Master accesses.

A value of 0 specifies Little Endian ordering. Big BIGEND# input pin during the address phase of the access.

D2 Direct Slave Address Space 0 Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address space 0.

A value of 0 specifies Little Endian ordering.

D3 Direct Slave Address Expansion ROM 0 Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Expansion ROM.

A value of 0 specifies Little Endian ordering.

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D4 Big Endian Byte Lane Mode

A vlaue of 1 specifies that in Big Endian mode, use byte lanes 31:16 for a bit local bus and byte lanes 31:24 for an 8 bit local bus.

A value of 0 specifies that in Big Endian mode, byte lanes 15:0 be used for a 16 bit local bus byte lanes 7:0 for an 8 bit local bus.

D5 Direct Slave Address Space 1 Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to loal Address Space 1.

A value of 0 specifies Little Endian ordering.

D6 DMA Channel 1 Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for DMA Channel 1 accesses to the local Address Space.

A value of 0 specifies Little Endian ordering.

D7 DMA Channel 0 Big Endian Mode

A value of 1 specifies use of Big Endian data ordering for DMA Channel 0 accesses to the local Address Space.

A value of 0 specifies Little Endian ordering.

D8..31 Reserved

2.9.5 Local Expansion ROM Range Register for PCI to Local Bus (PCI 0x10) (LOC 0x90)

D0..10 Reserved

D11..31 Specifies which PCI address bits will be used for decoding a PCI to local bus expansion ROM. Each of the bits corresponds to an Address bit. Bit 31 corresponds to Address bit 31. Write a value of 1 to all bits to be included in decode and a 0 to all others (Used in conjunction with PCI Configuration register 0x30). Default is 64 Kbytes.

2.9.6 Local Expansion ROM Local Base Address (Re-map) register for PCI to Local Bus and BREQo Control (PCI 0x14) (LOC 0x94)

D0..3 Direct Slave BREQo (Backoff Requests Out) Delay Clocks. Number of local bus clocks in which a Direct Slave HOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (HOLDA) before asserting BREQo. Once asserted, BREQo remains asserted until the PCI900 receives HOLDA (LSB = 8 or 64 clocks)

D4 Local Bus BREQo Enable

A 1 value enables the PCI9080 to assert the BREQo output.

D6..10 Reserved

D11..31 Re-map of PCI Expansion ROM space into a Local address space. The bits in this register re-map (replace) the PCI address bits used in decode as the Local address bits.

2.9.7 Local Bus Region Descriptor for PCI to Local Accesses Register (PCI 0x18) (LOC 0x98)

D0..1 Memory Space 0 Local Bus Width

A value of 00 indicates a bus width of 8 bits

A value of 01 indicates a bus width of 16 bits

A value of 10 or 11 indicates a bus width of 32 bits

The bus width is forced to 16 bits for the Sx mode.

D2..5 Memory Space 0 Internal Wait States (data to data; 0-15 wait states).

D6 Memory Space 0 Ready Input Enable

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A 1 value enables Ready input.
A value of 0 disables the Ready input.

D7 Memory Space 0 BTERM# Input Enable
A 1 value enables BTERM# input.
A value of 0 disables the BTERM# input.

D8 Memory Space 0 Prefetch Disable
If mapped into memory space,
A 0 enables read pre-fetching.
A value of 1 disables prefetching.
If prefetching is disabled, the PCI9080 will disconnect after each memory read.

D9 Expansion ROM Space Prefetch Disable.
A 0 enables read prefetching.
A 1 disables prefetching
If prefetching is disabled, the PCI9080 will disconnect after each memory read.

D10 Read Prefetch Count Enable.
When set to a 1 and memory prefetching is enabled, PCI 9080 prefetches up to the number of Lwords specified in the prefetch count.
When set to 0, PCI 9080 ignores the count and continues prefetching until terminated by the PCI bus.

D11..14 Prefetch Counter
Number of Lwords to prefetch during memory read cycles (0-15).
A count of zero selects a prefetch of 16 Lwords.

D15 Reserved

D16..17 Expansion ROM Space Local Bus Width.
A value of 00 indicates a bus width of 8 bits
A value of 01 indicates a bus width of 16 bits
A value of 10 or 11 indicates a bus width of 32 bits.

D21..18 Expansion ROM Space Internal Wait States (data to data; 0-15 wait states).

D22 Expansion ROM Space Ready Input Enable
A 1 value enables Ready input.
A value of 0 disables the Ready input.

D23 Expansion ROM Space BTERM# Input Enable
A 1 value enables BTERM# input.
A value of 0 disables the BTERM# input.
If this bit is set to 1, PCI 9080 bursts four Lword maximum at a time.

D24 Memory Space 0 Burst Enable
A 1 value enables bursting.
A value of 0 disables bursting.
If burst is disabled, the local bus performs continuous single cycles for burst PCI read/write cycles.

D25 Extra Long serial EEPROM.
A value of 1 loads the Subsystem ID and Local Address Space 1 registers.
A value of 0 indicates not to load them.

D26 Expansion ROM Space Burst Enable
A 1 value enables bursting.
A value of 0 disables bursting.
If burst is disabled, the local bus performs continuous single cycles for burst PCI read/write cycles.

D27 Direct Slave PCI write mode
A 0 indicates that the PCI9080 should disconnect when the Direct Slave write FIFO is full.
A 1 indicates that the PCI9080 should de-assert TRDY when the write FIFO is full.

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D28..31 PCI Target Retry Delay Clocks. Contains the value (multiplied by 8) of the # of PCI bus clocks after receiving a PCI-Local read or write access and not successfully completing a transfer. Only pertains to Direct Slave writes when bit 27 is set to 1.

2.9.8 Local Range register for Direct Master to PCI (PCI 0x1C) (LOC 0x9C)

D0..15 Reserved (64 KB increments)

D16..31 Specifies which local address bits to use for decoding a Local to PCI bus access. Each of the bits corresponds to an address bit. Bit 31 corresponds to Address bit 31.
A value of 1 should be written to all bits that should be included in decode and a 0 to all others. This range is used for Direct Master memory, I/O, or configuration accesses.

2.9.9 Local Bus Base Address register for Direct Master to PCI Memory (PCI 0x20) (LOC 0xA0)

D0..15 Reserved

D16..31 Assigns a value to the bits which will be used to decode a Local to PCI memory access.

2.9.10 Local Base Address for Direct Master to PCI IO/CFG Register (PCI 0x24) (LOC 0xA4)

D0..15 Reserved

D16..31 Assigns a value to the bits to be used for decoding a Local to PCI I/O or configuration access.
This base address is used for Direct Master I/O and configuration accesses.

2.9.11 PCI Base Address (Re-map) register for Direct Master to PCI (PCI 0x28) (LOC 0xA8)

D0 Direct Memory Access Enable
A value of 1 enables decode of Direct Master Memory accesses.
A value of 0 disables decode of Direct Master Memory accesses.

D1 Direct Master I/O Access Enable
A value of 1enables decode of Direct Master I/O accesses.
A value of 0 disables decode of Direct Master I/O accesses.

D2 LOCK# Input Enable
A 1 value enables LOCK# input.
A value of 0 disables the LOCK# input.

D3 Direct Master Red Prefetch Size control
00=PCI 9080 continues to prefetch read data from the PCI bus until Direct Master access is finished. This may result in an additional four unneeded Lwords being prefetched from the PCI bus.
01= Prefetch up to four Lwords from the PCI bus
10= Prefetch up to eight Lwords from the PCI bus
11= Prefetch up to 16 Lwords from the PCI bus
If PCI memory prefetch is not wanted, performs a Direct Master single cycle.
The direct master burst reads must not exceed the programmed limit.

D4 Direct Master PCI read mode
A value of 0 indicates that the PCI9080 should release the PCI bus when the read FIFO becomes full.
A value of 1 indicates that the PCI9080 should keep the PCI bus and de-assert IRDY when the read FIFO becomes full.

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D5..8,10 Programmable Almost Full flag.
When the number of entries in the 32 word direct master write FIFO exceed this value, the output pin DMPAF# is asserted low

D9 Write and Invalidate Mode.
When set to 1, PCI 9080 waits for 8 or 16 Lwords to be written from the local bus before starting PCI accesses.
When set , all local Direct Master to PCI write accesses must be 8 or 16 Lwords bursts.
Use in conjunction with (PCI 0x04)

D10 Direct Master Prefetch Limit.
If set to 1, don't prefetch past 4K (4098 bytes) boundaries.

D13 I/O Remap Select.
When set to1, forces PCI address bits [31:16] to all zeros.
When set to 0, uses bits [31:16] of this register as PCI address bits [31:16].

D14..15 Direct Master Write Delay.
This register is used to delay the PCI bus request after direct master burst write cycle has started. Values:
00=No delay; start the cycle immediately
01=Delay 4 PCI clocks
10=Delay 8 PCI clocks
11=Delay 16 PCI clocks

D16..31 Re-map of Local to PCI space into a PCI address space.
The bits in this register re-map (replace) the Local address bits used in decode as the PCI address bits. This PCI Remap address is used for Direct Master memory and I/O accesses.

2.9.12 PCI Configuration Address Register for Direct Master to PCI IO/CFG (PCI 0x2C) (LOC 0xAC)

D0..1 Configuration Type (00=Type 0, 01=Type 1)

D2..7 Register Number.
If different register read/write is needed, this register value must be programmed and a new PCI configuration cycle must be generated.

D8..10 Function Number

D11..15 Device Number

D16..23 Bus Number

D24..30 Reserved

D31 Configuration Enable.
A value of 1 allows Local to PCI I/O accesses to be converted to a PCI configuration cycle. The parameters in this table are used to generate the PCI configuration address.

2.9.13 Local Address Space 1 Range Register for PCI to Local Bus (PCI 0xF0) (LOC 0x170)

D0 Memory Space Indicator
A value of 0 indicates Local Address Space 1 maps into PCI memory space.
A value of 1 indicates Local Address Space 1 maps into PCI I/O space.

D1..2 Encoded for Memory Space
If mapped into memory space, encoding is as follows:
00-Locate anywhere in 32 bit PCI address space
01-Locate below 1 MB in PCI address space
10-Locate anywhere in 64 bit PCI address space
11-Reserved

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If mapped into I/O space, bit 1 must be set to 0.
Bit 2 is included with bits [31:3] to indicate decoding range.

D3 If mapped into memory space, a value of 1 indicates reads are prefetchable (bit has no effect on the operation of the PCI 9080, but is for system status). If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.

D4..31 Specifies which PCI address bits to use for decoding a PCI access to local bus space 1. Each of the bits corresponds to a PCI address bit. Bit 31 corresponds to Address bit 31. Write a value of 1 to all bits that must be included in decode and a 0 to all others (Used in conjunction with PCI Configuration Register). Default is 1 MB.

2.9.14 Local Address Space 1 Local Base Address (Remap) Register (PCI 0xF4) (LOC 0x174)

D0 Space 1 Enable

A value of 1 enables decoding of PCI addresses for Direct Slave access to local space 1.

A value of 0 disables decoding.

If this bit is set to 0, the PCI BIOS may not allocate (assign) the base address for Space 1.
Note: *Must be set to 1 for any Direct Slave access to Space 1.*

D1 Reserved

D2..3 If local space 1 is mapped into memory space, bits are not used. If mapped I/O space, bit is included with bits [31:4] for remapping.

D4..31 Remap of PCI Address to Local Address space 1 into a Local Address Space.
The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

2.9.15 Local Address Space 1 Bus Region Descriptor Register (PCI 0xF8) (LOC 0x178)

D0..1 Memory Space 1 Local Bus Width

A value of 00 indicates bus width of 8 bits
A value of 01 indicates bus width of 16 bits
A value of 10 indicates bus width of 32 bits

D2..5 Memory space 1 Internal Wait States (data to data; 0-15 wait states).

D6 Memory space 1 Ready Input Enable

A value of 1 enables BTERM# input.
A value of 0 disables Ready input.

D7 Memory space 1 BTERM# Input Enable

A value of 1 enables BTERM# input.
A value of 0 disables BTERM# input.

If this bit is set to 0, PCI 9080 bursts four Lword maximum at a time.

D8 Memory space 1 Burst Enable

A value of 1 enables bursting.
A value of 0 disables bursting.

If burst is disabled, the local bus performs continuous single cycle for burst PCI read/write cycles.

D9 Memory space 1 Prefetch Disable
If mapped into memory space

A value of 0 enables read prefetching.
A value of 1 disables read prefetching.

If prefetching is disabled, PCI 9080 disconnects after each memory read.

D10 Read Prefetch Count Enable

When set to 1 and memory prefetching is enabled, PCI 9080 prefetches up to the number of Lwords specified in the prefetch count.
When set to 0, PCI 9080 ignores the count and continues prefetching until terminated by the PCI bus.

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D11..14 Prefetch Counter
Number of Lwords to prefetch during memory read cycles (0-15).
D15..31 Reserved

2.10 SHARED RUNTIME REGISTERS BIT DESCRIPTIONS

2.10.1 Mailbox Register 0 (PCI 0x40) (LOC 0xC0)

D0..31 32 bit mailbox register

2.10.2 Mailbox Register 1 (PCI 0x44) (LOC 0xC4)

D0..31 32 bit mailbox register

2.10.2 Mailbox Register 2 (PCI 0x48) (LOC 0xC8)

D0..31 32 bit mailbox register

2.10.3 Mailbox Register 3 (PCI 0x4C) (LOC 0xCC)

D0..31 32 bit mailbox register

2.10.4 Mailbox Register 4 (PCI 0x50) (LOC 0xD0)

D0..31 32 bit mailbox register

2.10.5 Mailbox Register 5 (PCI 0x54) (LOC 0xD4)

D0..31 32 bit mailbox register

2.10.6 Mailbox Register 6 (PCI 0x58) (LOC 0xD8)

D0..31 32 bit mailbox register

2.10.7 Mailbox Register 7 (PCI 0x5C) (LOC 0xDC)

D0..31 32 bit mailbox register

2.10.8 PCI to Local Doorbell Register Description (PCI 0x60) (LOC 0xE0)

D0..31 Doorbell register.
A PCI master can write to this register and it will generate a local interrupt to the local processor. The local processor can then read this register to determine which doorbell bit was asserted. The PCI master sets a doorbell by writing a 1 to a particular bit. The local processor can clear a doorbell bit by writing a 1 to that bit position.

2.10.9 Local to PCI Doorbell Register Description (PCI 0x64) (LOC 0xE4)

D0..31 Doorbell register.
The local processor can write to this register and it will generate a PCI interrupt. A PCI master can then read this register to determine which doorbell bit was asserted. The local

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processor sets a doorbell by writing a 1 to a particular bit. The PCI master can clear a doorbell bit by writing a 1 to that bit position.

2.10.10 Interrupt Control /Status (PCI 0x68) (LOC 0xE8)

D0 Enable Local Bus LSERR#.
A value of 1 enables PCI 9080 to assert LSERR# interrupt output when PCI bus Target Abort or Master Abort status bit is set in the PCI Status configuration register.

D1 Enable Local Bus SERR# when PCI parity error occurs during PCI 9080 Master Transfer or PCI 9080 Slave access or Outbound Free List FIFO Overflow Init.

D2 Generate PCI Bus SERR#.
When this bit is set to 0, writing a 1 generates a PCI bus SERR#.

D3 Mailbox Interrupt Enable.
A value of 1 enables a Local Interrupt to be generated when the PCI bus writes to Mailbox register 0-3.
To clear the Local Interrupt, the Local master must read the Mailbox. Used in conjunction with Local interrupt enable.

D4..7 Reserved

D8 PCI Interrupt Enable.
A value of 1 enables PCI interrupts.

D9 PCI Doorbell Interrupt Enable.
A value of 1 enables doorbell interrupts. Used in conjunction with PCI interrupt enable. Clearing the doorbell interrupt bits that caused the interrupt also clears the interrupt.

D10 PCI Abort Interrupt Enable
A value of 1 enables a master abort or master detect of a target abort to generate a PCI interrupt. Used in conjunction with PCI interrupt enable. Clearing the abort status bits also clears the PCI interrupt.

D11 PCI Local Interrupt Enable.
A value of 1 enables a local interrupt input to generate a PCI interrupt. Use in conjunction with PCI Interrupt enable. Clearing the local bus cause of the interrupt also clears the interrupt.

D12 Retry Abort Enable.
A value of 1 enables PCI 9080 to treat 256 Master consecutive retries to a Target as a target abort.
A value of 0 enables PCI 9080 to attempt Master Retries indefinitely.
Note: *for diagnostic purposes only*.

D13 Value of 1 indicates PCI doorbell interrupt is active.

D14 Value of 1 indicates PCI abort interrupt is active.

D15 Value of 1 indicates local interrupt is active (LINTi#).

D16 Local Interrupt Output Enable.
A value of 1 enables local interrupt output.

D17 Local Doorbell Interrupt Enable.
A value of 1 enables doorbell interrupts. Used in conjunction with Local interrupt enable. Clearing the local doorbell interrupt bits that caused the interrupt also clears the interrupt.

D18 Local DMA Channel 0 Interrupt Enable.
A value of 1 enables DMA Channel 0 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits also clears the interrupt.

D19 Local DMA Channel 1 Interrupt Enable.
A value of 1 enables DMA Channel 1 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits also clears the interrupt.

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D20 Value of 1 indicates local doorbell interrupt is active.
D21 Value of 1 indicates DMA Ch 0 interrupt is active.
D22 Value of 1 indicates DMA Ch 1 interrupt is active.
D23 Value of 1 indicates BIST interrupt is active.
BIST (Built-In Self Test) interrupt is generated by writing 1 to bit 6 of the PCI Configuration BIST register. Clearing bit 6 clears the interrupt. Refer to the BIST Register for a description of self test.
D24 Value of 0 indicates a Direct master was the bus master during a master or Target abort. (Not valid until abort occurs.)
D25 Value of 0 indicates a DMA CH 0 was the bus master during a master or Target abort. (Not valid until abort occurs.)
D26 Value of 0 indicates a DMA CH 1 was the bus master during a master or Target abort. (Not valid until abort occurs.)
D27 Value of 0 indicates a Target Abort was generated by the PCI 9080 after 256 consecutive Master retries to a Target. (Not valid until abort occurs.)
D28 Value of 1 indicates PCI wrote data to the Mailbox #0. Enabled only if MBOXINTENB is enabled (bit 3 high).
D29 Value of 1 indicates PCI wrote data to the Mailbox #1. Enabled only if MBOXINTENB is enabled (bit 3 high).
D30 Value of 1 indicates PCI wrote data to the Mailbox #2. Enabled only if MBOXINTENB is enabled (bit 3 high).
D31 Value of 1 indicates PCI wrote data to the Mailbox #3. Enabled only if MBOXINTENB is enabled (bit 3 high).

2.10.11 EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI 0x6C) (LOC 0xEC)

D0..3 PCI Read Command Code for DMA
This PCI command is sent out during DMA read cycles.
D4..7 PCI Write Command Code for DMA
This PCI command is sent out during DMA write cycles.
D8..11 PCI Memory Read Command Code for Direct Master
This PCI command is sent out during Direct Master read cycles.
D12..15 PCI Memory Write Command Code for Direct Master
This PCI command is sent out during Direct Master write cycles.
D16 General Purpose Output
A value of 1 will cause the USERO output to go high.
A value of 0 will cause the output to go low.
D17 General Purpose Input
A value of 1 indicates that USERI input pin is high.
A value of 0 indicates that USERI pin is low.
D18..23 Reserved
D24 Serial EEPROM clock for Local or PCI bus reads or writes to serial EEPROM. Toggling this bit generates a serial EEPROM clock. (Refer to the manufacturer's data sheet for the particular EEPROM being used.)
D25 Serial EEPROM chip select. For Local or PCI bus reads or writes to serial EEPROM Setting this bit to a 1 provides the EEPROM chip select.
D26 Write bit to serial EEPROM. For writes, this output bit is the input to the serial EEPROM. It is clocked into the serial EEPROM by the serial EEPROM clock.
D27 Read serial EEPROM data bit. For reads, this input bit is the output of the serial EEPROM. It is clocked out of the serial EEPROM by the serial EEPROM clock.
D28 Serial EEPROM present
A 1 in this bit indicates that an EEPROM is present.
D29 Reload Configuration Registers

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When this bit is 0, writing a 1 causes the PCI9080 to reload the local configuration registers from the serial EEPROM.

D30 PCI Adapter Software Reset
A value of 1 written to this bit will hold the local bus logic in the PCI9080 reset and LRESETO# asserted. The contents of the PCI configuration registers and Shared Run Time registers will not be reset. Software Reset can only be cleared from the PCI bus. (Local bus remains reset until this bit is cleared.)

D31 Local Init Status.
Value of 1indicates local init done. Responses to PCI accesses will be RETRYs until this bit is set. While Input NB# is asserted low this bit will be forced to 1.

2.10.12 PCI Permanent Configuration ID Register (PCI 0x70) (LOC 0xF0)

D0..15 Permanent Vendor ID. Identifies device manufacturer.
Note: *Hardcoded to the PCI SIG issued vendor ID of PLX (10B5).*

D16..31 Permanent Device ID. Identifies the particular device.
Note: *Hardcoded to the PLX part number for PCI interface chip PCI 9080.*

2.10.13 PCI Permanent Revision ID Register (PCI 0x74) (LOC 0xF4)

D0..15 Permanent Revision ID.
Note: *Hardcoded to the silicon revision of the PCI 9080.*

2.11 LOCAL DMA REGISTERS

2.11.1 DMA Channel 0 Mode Register (LOC 0x100)

D0..1 Local DMA Bus Width
A value of 00 indicates a DMA bus width of 8 bits.
A value of 01 indicates DMA bus width of 16 bits.
A value of 10 or 11 indicates a DMA bus width of 32 bits.

D2..5 Internal Wait States (data to data)

D6 Ready Input Enable
A value of 1 enables Ready input.
A value of 0 disables the Ready input.

D7 Bterm Input Enable
A value of 1 enables Bterm input.
A value of 0 disables Bterm input.

D8 Local Burst Enable
A value of 1 enables bursting.
A value of 0 disables bursting.

D9 Chaining
A 1 value indicates non-chaining mode is enabled.
For chaining mode, the DMA source address, destination address and byte count are loaded from memory in PCI or Local Address Spaces.
A 0 value indicates non-chaining mode is enabled.

D10 Done Interrupt Enable
A 1 value enables interrupt when done.
A 0 value disables interrupt when done.
If DMA clear count mode is enabled, the interrupt won't occur until the byte count is cleared.

D11 Local Addressing Mode
A 1 value indicates local addresses LA [31:2] to be held constant.

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A 0 value indicates local address is incremented.

D12 Demand Mode
A value of 1 causes the DMA controller to operate in demand mode.
In demand mode the DMA controller transfers data when it's DREQ# input is asserted. It asserts DACK# to indicate that the current local bus transfer is in response to the DREQ# input. The DMA controller transfers Lwords (32bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.

D13 Write and Invalidate mode for DMA transfers.
When set to 1, PCI 9080 performs Write and Invalidate cycles to the PCI bus. PCI 9080 supports Write and Invalidate sizes of 8 or 16 Lwords. The size is specified in the PCI Cache Line Size Register. If a size other than 8 or 16 is specified, PCI 9080 performs write transfers rather than Write and Invalidate transfers. Transfers must start and end at the Cache Line Boundaries.

D14 DMA EOT (End Of Transfer) Enable.
Value of 1 enables EOT# input pin.
Value of 0 disables EOT# input pin.

D15 DMA Stop Data Transfer Mode
Value of 0 sends a BLAST to terminate DMA transfer.
Value of 1 indicates an EOT asserted or DREQ# negated during demand mode DMA terminates the DMA transfer.

D16 DMA Clear Count Mode.
When set to 1, the byte count in each chaining descriptor, if it is in local memory, is cleared when the corresponding DMA transfer is complete.
Note: *If chaining descriptor is in PCI memory, the count is not cleared.*

D17 DMA Channel 0 Interrupt Select
Value of 1 routes the DMA Channel 0 interrupt to the PCI interrupt.
Value of 0 routes the DMA Channel 0 interrupt to the local bus interrupt.

D18..31 Reserved

2.11.2 DMA Channel 0 PCI Address Register (LOC 0x104)

D0..31 PCI Address Register. This indicates where in the PCI memory space the DMA transfers (reads or writes) will start from.

2.11.3 DMA Channel 0 Local Address Register (LOC 0x108)

D0..31 Local Address Register. This indicates where in the local memory space the DMA transfers (reads or writes) will start from.

2.11.4 DMA Channel 0 Transfer Size (Bytes) Register (LOC 0x10C)

D0..22 DMA Transfer Size (Bytes). Indicates number of bytes to be transferred during DMA operation.

D23..31 Reserved

2.11.5 DMA Channel 0 Descriptor Pointer Register (LOC 0x110)

D0 Descriptor Location.
Value of 1 indicates PCI address space.
Value of 0 indicates Local Address Space.

D1 End of Chain

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A 1 value indicates end of chain.
A 0 value indicates not end of chain descriptor. (Same as Nonchaining Mode)

D2 Interrupt after Terminal Count
A 1 value causes an interrupt to be generated after the terminal count for this descriptor is reached.
A 0 value disables interrupts from being generated.

D3 Direction of transfer
A 1 value indicates transfers from local bus to PCI bus.
A 0 value indicates transfers from PCI to local bus.

D4..31 Next Descriptor Address. Quad word aligned (Bit[3:0] = 0000).

2.11.6 DMA Channel 1 Mode Register (LOC 0x114)

D0..1 Local Bus Width
A value of 00 indicates a bus width of 8 bits.
A value of 01 indicates bus width of 16 bits.
A value of 10 or 11 indicates a DMA bus width of 32 bits.
The bus width is forced to 16 bits for the Sx mode

D2..5 Internal Wait States (data to data).

D6 Ready Input Enable
A 1 value enables Ready input.
A value of 0 disables the Ready input.

D7 Bterm Input Enable
A 1 value enables Bterm input.
A value of 0 disables the Bterm input.
If this bit is set to 0, PCI 9080 bursts four Lword maximum at a time.

D8 Local Burst Enable
A 1 value enables Local bursting input.
A value of 0 disables Local bursting.
If burst is disabled, the local bus performs continuous single cycles for burst PCI read/write cycles.

D9 Chaining
A 1 value indicates chaining mode enabled. For chaining mode, the DMA source address, destination address and byte count are loaded from memory in PCI or Local address spaces.
A value indicates non-chaining mode.

D10 Done Interrupt Enable
A 1 value enables interrupt when done.
A 0 value disables the interrupt when done.
If DMA Clear Count Mode is enabled, the interrupt won't occur until the byte count is cleared.

D11 Local Addressing Mode
A 1 value indicates local addresses LA[31:2] to be held constant.
A 0 value indicates local addresses is incremented.

D12 Demand Mode
A value of 1 causes the DMA controller to operate in demand mode. In demand mode the DMA controller transfers data when its DREQ# input is asserted. It asserts DACK# to indicate that the current local bus transfer is in response to the

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DREQ# input. The DMA controller transfers Lwords (32bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.

D13..31 Reserved

2.11.7 DMA Channel 1 PCI Data Address Register (LOC 0x118)

D0..31 PCI Data Address Register. This indicates where in the PCI memory space the DMA transfers (reads or writes) will start from.

2.11.8 DMA Channel 1 Local Data Address Register (LOC 0x11C)

D0..31 Local data Address Register. This indicates where in the local memory space the DMA transfers (reads or writes) will start from.

2.11.9 DMA Channel 1 Transfer Size (bytes) register (LOC 0x120)

D0..22 DMA Transfer Size (Bytes). Indicates number of bytes to be transferred during DMA operation.

D23..31 Reserved

2.11.10 DMA Channel 1 Descriptor Pointer Register (LOC 0x124)

D0 Descriptor Location.
A 1 value indicates PCI address space.
A 0 value indicates Local address space.

D1 End of Chain
A 1 value indicates end of chain.
A 0 value indicates not end of chain descriptor. (Same as Nonchaining Mode)

D2 Interrupt after Terminal Count
A 1 value causes an interrupt to be generated after the terminal count for this descriptor is reached.
A 0 value disables interrupts from being generated.

D3 Direction of transfer
A 1 value indicates transfers from local bus to PCI bus.
A 0 value indicates transfers from PCI bus to local bus.

D4..31 Next Descriptor Address. Quad word aligned (bits [3:0] =0000).

2.11.11 DMA Command/Status Register (LOC 0x128)

D0 Channel 0 Enable
A 1 value enables the channel to transfer data.
A 0 value disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (Pause).

D1 Channel 0 Start
Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled.

D2 Channel 0 Abort
Writing a 1 to this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. The channel complete bit is set when the abort has completed.

D3 Clear Interrupt.
Writing a 1 to this bit clears channel 0 interrupts.

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D4 Channel 0 Done
A 1 value indicates this channels transfer is complete.
A 0 value indicates the channel transfer is not complete.

D5..7 User Defined

2.11.12 DMA Command/Status Register (LOC 0x129)

D0 Channel 1 Enable
A 1 value enables the channel to transfer data.
A 0 value disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (Pause).

D1 Channel 1 Start
Writing a 1 to this bit causes the channel to start transferring data if the channel is enabled.

D2 Channel 1 Abort
Writing a 1 to this bit causes the channel to abort the current transfer. The channel enable bit must be cleared. The channel complete bit is set when the abort has completed.

D3 Clear Interrupt.
Writing a 1 to this bit clears channel 1 interrupts.

D4 Channel 1 Done
A 1 value indicates this channel's transfer is complete.
A 0 value indicates the channel transfer is not complete.

D5..7 Reserved

2.11.13 DMA Arbitration Register 0 (LOC 0x12C). Same as Mode/Arbitration Register at address (LOC 0x88)

2.11.14 DMA Threshold Register 1 (LOC 0x130)

D0..3 DMA Channel 0 PCI to Local Almost Full (C0PLAF):
# of Full Entries (minus 1) in FIFO before Requesting Local Bus for Writes.
(C0PLAF+1) + (C0PLAE+1) should be <= FIFO Depth of 16

D4..7 DMA Channel 0 Local to PCI Almost Empty (C0LPAE):
# of Empty Entries (minus 1) in FIFO before Requesting Local Bus for Reads.
(C0LPAF+1) + (C0LPAE+1) should be <= FIFO Depth of 16

D8..11 DMA Channel 0 Local to PCI Almost Full (C0LPAF):
# of Full Entries (minus 1) in FIFO before requesting PCI bus for Writes.

D12..15 DMA Channel 0 PCI to Local Almost Empty (C0PLAE):
# of Empty Entries (minus 1) in FIFO before Requesting PCI Bus for Reads.

D16..19 DMA Channel 1 PCI to Local Almost Full (C0PLAF):
# of Full Entries (minus 1) in FIFO before Requesting Local Bus for Writes.
(C0PLAF+1) + (C0PLAE+1) should be <= FIFO Depth of 16

D20..23 DMA Channel 1 Local to PCI Almost Empty (C0LPAE):
# of Empty Entries (minus 1) in FIFO before Requesting Local Bus for Reads.
(C0LPAF+1) + (C0LPAE+1) should be <= FIFO Depth of 16

D24..27 DMA Channel 1 Local to PCI Almost Full (C0LPAF):
# of Full Entries (minus 1) in FIFO before requesting PCI bus for Writes.

D28..31 DMA Channel 1 PCI to Local Almost Empty (C0PLAE):
# of Empty Entries (minus 1) in FIFO before Requesting PCI Bus for Reads.

2.12 MESSAGING QUEUE REGISTERS

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2.12.1 Outbound Post List FIFO Interrupt Status Register (PCI 0x30) (LOC 0xB0)

D0..2 Reserved
D3 Outbound Post List FIFO Interrupt.
This bit is set when the Outbound Post List FIFO is not empty. This bit is not affected by the interrupt mask bit.
D4..31 Reserved

2.12.2 Outbound Post List FIFO Interrupt Status Register (PCI 0x34) (LOC 0xB4)

D0..2 Reserved
D3 Outbound Post List FIFO Interrupt Mask.
Interrupt is masked when this bit is set.
D4..31 Reserved

2.12.3 Inbound Queue Port Register (PCI 0x40)

D0..31 Value written by PCI master is stored into the Inbound Post List FIFO, which is located in local memory at the address pointed to by the Queue Base Address + FIFO Size + Inbound Post Head Pointer. From the time of the PCI write until the local memory write and update of the Inbound Post Queue Head Pointer, further accesses to this register result in a retry. A local interrupt is generated when the Inbound Post List FIFO is not empty.

When the port is read by the PCI master, the value is read from the Inbound Free List FIFO, which is located in local memory at the address pointed the by The Queue Base Address + Inbound Free Tail Pointer. If FIFO is empty, a value of FFFFFFFh is returned..

2.12.4 Outbound Queue Port Register (PCI 0x44)

D0..31 Value written by PCI master is stored into the Outbound Free List FIFO, which is located in local memory at the address pointed to by the Queue Base Address + (3*FIFO Size) + Outbound Free Head Pointer. From the time of the PCI write until the local memory write and update of the Outbound Free Head Pointer, further accesses to this register result in a retry. If FIFO fills up, a local LSERR interrupt is generated.

When the port I s read by the PCI master, the value is read from the Outbound Post List FIFO, which is located in local memory at the address pointed to by the Queue Base address + (2*FIFO Size) + Outbound Trail Pointer. If FIFO is empty, a value of FFFFFFFh is returned. A PCI interrupt is generated if Outbound Post List FIFO is not empty.

2.12.5 Messaging Queue Configuration Register (PCI 0xC0) (LOC 0x140)

D0 Queue Enable
Value of 1 allows accesses to the Inbound and Outbound Queue ports. If cleared to 0, writes are accepted but ignored and reads return FFFFFFFF. All pointer initialization and frame allocation should be completed before enabling this bit.
D1..5 Circular FIFO Size
Defines the size of one of the circular FIFOs. Each of the four FIFOs are the same size. Each FIFO entry is one 32 bit word.
FIFO Size Encoding

Max entries	FIFO	Total FIFO

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5:1	per FIFO	Size	Memory
00001	4K entries	16 KB	64 KB
00010	8K entries	32 KB	128 KB
00100	16K entries	64 KB	256 KB
01000	32K entries	128 KB	512 KB
10000	64K entries	256 KB	1 MB

D6..31 Reserved

2.12.6 Queue Base Address Register (PCI 0xC4) (LOC 0x144)

D0..19 Reserved
D20..31 Queue Base Address
Local Memory base address of the Inbound and Outbound Queues (four contiguous and equal size FIFOs). Queue base address must be aligned on a 1 MB boundary.

2.12.7 Inbound Free Head Pointer Register (PCI 0xC8) (LOC 0x148)

D0..1 Reserved
D2..19 Inbound Free Head Pointer
Local memory Offset for Inbound Free List FIFO. This register is initialized as (0*FIFO Size) and maintained by the local CPU software.
D20..31 Queue Base Address

2.12.8 Inbound Free Head Tail Register (PCI 0xCC) (LOC 0x14C)

D0..1 Reserved
D2..19 Inbound Free Tail Pointer
Local Memory Offset for Inbound Free List FIFO. This register is initialized as (0*FIFO Size) by the local CPU software. It is maintained by the MU hardware and is incremented modulo the FIFO size.
D20..31 Queue Base Address

2.12.9 Inbound Post Head Pointer Register (PCI 0xD0) (LOC 0x150)

D0..1 Reserved
D2..19 Inbound Post Head Pointer
Local Memory Offset for Inbound Post List FIFO. This register is initialized as (1*FIFO Size) by the local CPU software. It is maintained by the MU hardware and is incremented modulo the FIFO size.
D20..31 Queue Base Address

2.12.10 Inbound Post Tail Pointer Register (PCI 0xD4) (LOC 0x154)

D0..1 Reserved
D2..19 Inbound Post Tail Pointer
Local Memory Offset for Inbound Post List FIFO. This register is initialized as (1*FIFO Size) by the local CPU software.
D20..31 Queue Base Address

2.12.11 Outbound Free Head Pointer Register (PCI 0xD8) (LOC 0x158)

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D0..1 Reserved
D2..19 Outbound Free Head Pointer
Local Memory Offset for Outbound Free List FIFO. This register is initialized as (3*FIFO Size) by the local CPU software. It is maintained by the MU hardware and is incremented modulo the FIFO size.
D20..31 Queue Base Address

2.12.12 Outbound Free Tail Pointer Register (PCI 0xDC) (LOC 0x15C)

D0..1 Reserved
D2..19 Outbound Free Tail Pointer
Local Memory Offset for Outbound Free List FIFO. This register is initialized as (3*FIFO Size) by the local CPU software.
D20..31 Queue Base Address

2.12.13 Outbound Post Head Pointer Register (PCI 0xE0) (LOC 0x160)

D0..1 Reserved
D2..19 Outbound Post Head Pointer
Local Memory Offset for Outbound Post List FIFO. This register is initialized as (2*FIFO Size) by the local CPU software.
D20..31 Queue Base Address

2.12.14 Outbound Post Tail Pointer Register (PCI 0xE4) (LOC 0x164)

D0..1 Reserved
D2..19 Outbound Post Tail Pointer
Local Memory Offset for Outbound Post List FIFO. This register is initialized as (2*FIFO Size) and maintained by the MU hardware and is incremented modulo the FIFO size.
D20..31 Queue Base Address

2.12.15 Queue Status/Control Register (PCI 0xE8) (LOC 0x168)

D0 I(2)O Decode Enable
When this bit is set, Mailbox registers 0 and 1 are replaced by the Inbound and Outbound Queue Port Registers and redefines Space 1 as PCI Base Address 0 to be accessed by PCIBAR0. Former Space 1 registers F0, F4, and F8 should be programmed to configure their shared I(2)O memory space, defined as PCI Base Address 0.
D1 Queue Local Space Select
When this bit is set to 0, use Local Address Space 0 bus region descriptor for queue accesses.
When this bit is set to 1, use Local Address Space 1 bus region descriptor for queue accesses.
D2 Outbound Post List FIFO Prefetch Enable
When this bit is set, prefetching occurs from the Outbound Post List FIFO if not empty.
D3 Inbound Free List FIFO Prefetch Enable

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When this bit is set, prefetching occurs from the Inbound Free List FIFO if not empty.

D4 Inbound Post List FIFO Interrupt Mask
When this bit is set, interrupt is masked.

D5 Inbound Post List FIFO Interrupt
This bit is set when the Inbound Post List FIFO if not empty. This bit is not affected by the Interrupt Mask bit.

D6 Outbound Free List FIFO Overflow Interrupt Mask
When this bit is set, interrupt is masked.

D7 Outbound Free List FIFO Overflow Interrupt
This bit is set when the Outbound Free List FIFO becomes full. A local SERR (NMI) interrupt is generated if enabled in the Interrupt Control/Status Register. Writing 1 clears the interrupt.

D8..31 Unused

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2.13 PCI-HPDI32A-PRINT LOCAL REGISTERS

Table 2.13-1 Register Map

Offset Address	Size	Access*	Register Name	Value after Reset
0x00	D32	RO	Firmware Revision	0xXXXXXXXX
0x04	D32	RW	Board Control	0x00000000
0x08	D32	RO	Board Status	0xXXXXXCXX
0x0C	D32	RW	Tx Programmable Almost	0x00000000
0x10	N/A	N/A	Reserved	N/A
0x14	N/A	N/A	Reserved	N/A
0x18	D32	RW	Tx FIFOs	EMPTY
0x1C	N/A	N/A	Reserved	N/A
0x20	D32	RW	Head Shift Size	0x00000080
0x24	N/A	N/A	Reserved	N/A
0x28	N/A	N/A	Reserved	N/A
0x2C	N/A	N/A	Reserved	N/A
0x30	D32	RW	Interrupt Control	0x00000000
0x34	D32	RC	Interrupt Status	0xXXXXX3XX
0x40	D32	RW	Printing Control/Status	0x00000000
0x44	D32	RW	Edge Selector	0x00000000
0x48	D32	RW	Head Data Holdoff	0x00000000
0x4C	D32	RW	Quadrature Transition Delay Count	0x00000000
0x50	D32	RW	Start Position	0x00000000
0x54	D32	RW	Stop Position	0x00000000
0x58	D32	RO	Current Position	0x00000000
0x5C-0x7C	D32	N/A	Reserved	N/A
0x80	D32	RW	Head 0 Fire Delay	0x00000000
0x84	D32	RW	Head 0 Fire Width	0x00000000
0x88	D32	RW	Head 1 Fire Delay	0x00000000
0x8C	D32	RW	Head 1 Fire Width	0x00000000
0x90	D32	RW	Head 2 Fire Delay	0x00000000
0x94	D32	RW	Head 2 Fire Width	0x00000000
0x98	D32	RW	Head 3 Fire Delay	0x00000000
0x9C	D32	RW	Head 3 Fire Width	0x00000000
0xA0	D32	RW	Head 4 Fire Delay	0x00000000
0xA4	D32	RW	Head 4 Fire Width	0x00000000
0xA8	D32	RW	Head 5 Fire Delay	0x00000000
0xAC	D32	RW	Head 5 Fire Width	0x00000000
0xB0	D32	RW	Head 6 Fire Delay	0x00000000
0xB4	D32	RW	Head 6 Fire Width	0x00000000
0xB8	D32	RW	Head 7 Fire Delay	0x00000000
0xBC	D32	RW	Head 7 Fire Width	0x00000000
0xC0..0xFC	D32		Reserved	N/A

* RO - read only
RW - read/write capability
RC - read clear (a write clears the specified bits)

2.14 PCI-HPDI32A-PRINT LOCAL REGISTERS, BIT MAP & BIT DESCRIPTIONS

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Note: All bits labeled “Reserved” are unused in this implementation. To avoid unpredictable results a “0” should be written to these bits. The value of these “Reserved” bits is indeterminate when read.

2.14.1 FIRMWARE REVISION: (Offset 0x00)

This Register is used to determine the version of firmware that is programmed into the board. If the logic is changed to accommodate a modification for any reason then the value in this register is incremented.

Revision 0: Original version after debug and final release.

2.14.2 BOARD CONTROL: (Offset 0x04)

The Board Control Register is strictly under software control and provides the following functions:

D0 Board Reset
Writing a *1* to this bit will generate a self-timed pulse that
is used to reset the on-board logic and the FIFOs.
There is no need for the software to clear this bit, the bit will clear itself.

D1 Tx FIFO Reset
Writing a *1* to this bit will generate a self-timed pulse that will be
used to reset the Tx FIFOs. Setting This bit will also program the FIFO Almost Empty and the Almost Full Flags.
There is no need for the software to clear this bit, the bit will clear itself.

D2..3 Reserved

D4 Enable Tx
Writing a *1* to this bit will enable the transmit signals on the cable.
Writing a 0 to this bit will tristate the transmit signals on the cable.

D5..7 Reserved

D8 Start Tx
Writing a *1* to this bit will enable the logic.
Writing a 0 to this bit will disable the logic.

D9..11 Reserved

D12 FIFO almost empty bit D16 (for FIFO almost full values > 0xFFFF)

D13 FIFO almost full bit D16 (for FIFO almost full values > 0xFFFF)

D14..31 Reserved

2.14.3 BOARD STATUS: (Offset 0x08)

The Board Status Register is used to return information to the software about the most current status of the board, at the time of the reading. Listed below is the information that this register contains:

D0..1 Reserved

D2 Encoder A Input from cable

D3 Encoder B Input from cable

D4 Zfwd Input from cable

D5 Zrev Input from cable

D6..7 Reserved

D8 Tx FIFO Empty L
1 will indicate the Tx FIFO is not empty.
0 will indicate the Tx FIFO is empty.

D9 Tx FIFO Almost Empty L

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1 will indicate the Tx FIFO is not almost empty.
0 will indicate the Tx FIFO is almost empty.

D10 Tx FIFO Almost Full L
1 will indicate the Tx FIFO is not almost full.
0 will indicate the Tx FIFO is almost full.
D11 Tx FIFO Full L
1 will indicate the Tx FIFO is not full.
0 will indicate the Tx FIFO is full.
D12..31 Reserved

2.14.4 TX ALMOST: (Offset 0x0C)

D0..31 This register is used to program the Almost flags of the Tx FIFOs. These values will be programmed following a Tx FIFO reset from the Board Control Register.

Data 0..15 High byte, Almost Empty
This value represents the number of words remaining in the FIFO when the Almost Empty Flag is asserted.
Data 16..31 High byte, Almost Full
This value represents the number of empty words remaining in the FIFO when the Almost Full Flag is asserted.

For values larger than 0xFFFF, please use the bits D12..D13 in the Board Control Register as the D16 bits of these values (see section 2.14.2 BOARD CONTROL).
For Example: BCR D12 = 1
TX ALMOST D0..15 = 0x0000
FIFO almost empty value will be 0x10000.

BCR D13 = 1
TX ALMOST D16..31 = 0x0000
FIFO almost full value will be 0x10000.

2.14.5 TX FIFOs: (Offset 0x18)

Two 32Kbyte FIFOs are used for buffering print head data. This gives the software a means of buffering the data before it is transmitted to the cable. The FIFOs are also used by the DMA for the same purpose. This eliminates unnecessary PCI bus arbitration which provides for faster and more efficient bus cycles for transfers; hence, a faster and more efficient system. The user will need to ensure that all DMA transfers to the FIFOs are set to use a 16-bit wide local bus transfer.

D0..15 TX FIFO DATA
D16..32 Reserved

2.14.6 HEAD SHIFT SIZE: (Offset 0x20)

This determines the number of 16 bit words to be clocked to the print heads before the print heads are fired. This value may vary from 0 to 511, and is reset to 128.
Note: Loading this register with 0x00000000 may cause unpredictable results.

D0..7 Head Shift Size
D8..31 Reserved

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2.14.7 INTERRUPT CONTROL: (Offset 0x30)

The Interrupt Control Register provides the software with a means of selecting what conditions will be allowed to generate an interrupt.

D0..7 Reserved
D8 Enable on Tx Interrupt on FIFO Empty
1 will allow an interrupt on Tx FIFO Empty.
0 will disallow an interrupt on Tx FIFO Empty.
D9 Enable on Tx Interrupt on FIFO Almost Empty
1 will allow an interrupt on Tx FIFO Almost Empty.
0 will disallow an interrupt on Tx FIFO Almost Empty.
D10 Enable on Tx Interrupt on FIFO Almost Full
1 will allow an interrupt on Tx FIFO Almost Full.
0 will disallow an interrupt on Tx FIFO Almost Full.
D11 Enable on Tx Interrupt on FIFO Full
1 will allow an interrupt on Tx FIFO Full.
0 will disallow an interrupt on Tx FIFO Full.
D12 ..31 Reserved

2.14.8 INTERRUPT STATUS: (Offset 0x34)

The Interrupt Status Register serves as a dual-purpose register. Each bit in this register operates independently of each other. If an interrupt condition is enabled in the Interrupt Control Register, the appropriate bit in the Interrupt Status Register will indicate if an interrupt has occurred or not. When an interrupt occurs the status bit will latch the interrupt condition until software resets it by writing a "1" to the appropriate bit. If an interrupt is not enabled in the Interrupt Control Register, then the appropriate bit in the Interrupt Status Register will indicate whether or not the condition currently exists for an interrupt request. In this case, the interrupt condition is not latched and does not need to be cleared by software.

The Printhead IRQ bit in this register is a status bit only. It does not have a corresponding bit in the Interrupt Control Register, and is not latched. Enabling and clearing of the Printhead IRQ is handled in the Printing/Control Register.

D0 Printhead IRQ from Printing Control/Status Register
If this bit is enabled as an interrupt
a *1* will indicate that an interrupt from the PCSR has occurred.
a 0 will indicate that an interrupt from the PCSR has not occurred.
D1..7 Reserved
D8 Tx FIFO Empty
If this bit is enabled as an interrupt
a *1* will indicate that an interrupt on the Tx FIFO empty has occurred.
a *0* will indicate that an interrupt on the Tx FIFO empty has not occurred.
If this bit is not enabled as an interrupt
a *1* will indicate that the Tx FIFO is currently empty
a *0* will indicate that the Tx FIFO is not currently empty.
D9 Tx FIFO Almost Empty

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If this bit is enabled as an interrupt
a *1* will indicate that an interrupt on the Tx FIFO AE has occurred.
a *0* will indicate that an interrupt on the Tx FIFO AE has not occurred.
If this bit is not enabled as an interrupt
a *1* will indicate that the Tx FIFO is currently almost empty.
a *0* will indicate that the Tx FIFO is not currently almost empty.

D10 Tx FIFO Almost Full
If this bit is enabled as an interrupt
a *1* will indicate that an interrupt on the Tx FIFO almost full has occurred.
a *0* will indicate that an interrupt on the Tx FIFO almost full has not occurred.
If this bit is not enabled as an interrupt
a *1* will indicate that the Tx FIFO is currently almost full.
a *0* will indicate that the Tx FIFO is not currently almost full.

D11 Tx FIFO Full
If this bit is enabled as an interrupt
a *1* will indicate that an interrupt on the Tx FIFO full has occurred.
a *0* will indicate that an interrupt on the Tx FIFO full has not occurred.
If this bit is not enabled as an interrupt
a *1* will indicate that the Tx FIFO is currently full.
a *0* will indicate that the Tx FIFO is not currently full.

D12..31 Reserved

2.14.9 PRINTING CONTROL/STATUS: (Offset 0x40)

CONTROL

D0 Quadrature Encoder Error IRQ Enable
Writing a 1 to this bit will enable IRQ on Quadrature Encoder Error.

D1 Zfwd Reached IRQ Enable
Writing a 1 to this bit will enable IRQ if Zfwd is detected.

D2 Zrev Reached IRQ Enable
Writing a 1 to this bit will enable IRQ if Zrev is detected.

D3 Stop Reached IRQ Enable
Writing a 1 to this bit will enable IRQ if current position is equal to the Stop Position Register.

D4..5 Filter Strength
Filter strength defines the number of 12Mhz clocks an input must be stable before it is recognized by the Print Control Logic. This filter value applies to the A,B, and Z inputs.
Note: The following table concerns bits D4 and D5
00= 2 Clocks
01= 3 Clocks
10= 4 Clocks
11= 5 Clocks

D6..8 Reserved

D9 Drive Test Point on Cable
Writing a 1 to this bit will output test signals on unused cable command pins on the cable. This signal is intended for factory test and should not be set by the user.

D10 Reserved

D11 Internal Test Inputs Enabled
Writing a 1 to this bit can drive test A, B, Z inputs from bits 12-15 of this register instead of the actual cable inputs. This signal is intended for factory test and should not be set by the user.

D12 Zfwd Test

D13 Zrev Test

D14 A Test

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D15 B Test

STATUS

D16 Quadrature Encoder Error has been detected

Quadrature Encoder Error is defined as both A and B inputs changing simultaneously.

D17 Zfwd has been detected
D18 Zrev has been detected
D19 Stop Position has been reached
D20 Filtered Zfwd input
D21 Filtered Zrev input
D22 Filtered A input
D23 Filtered B input
D24..31 Reserved

2.14.10 EDGE SELECTOR: (Offset 0x44)

D0..4 define the condition to clear the position counter. A 1 will enable each condition. Multiple conditions may be selected to reset the counter.

D0 Clears Position Counter if Zfwd Rises
D1 Clears Position Counter if Zfwd Falls
D2 Clears Position Counter if Zrev Rises
D3 Clears Position Counter if Zrev Falls

D4..8 define the conditions to start printing. A 1 will enable each start print condition. Multiple conditions may be selected to start printing, but printing will start when the first condition is met. A “start print” is defined as enabling the heads to fire. The first block of data will be clocked into the print heads regardless of the start print condition.

D4 Start Print when Zfwd Rises
D5 Start Print when Zfwd Falls
D6 Start Print when Zrev Rises
D7 Start Print when Zrev Falls
D8 Start Print at Start Location

D9..13 define the conditions to start printing. A 1 will enable each start print condition. Multiple conditions may be selected to stop printing, but printing will start when the first condition is met. A “stop print” is defined as disabling the heads from firing.

D9 Stop Print when Zfwd Rises
D10 Stop Print when Zfwd Falls
D11 Stop Print when Zrev Rises
D12 Stop Print when Zrev Falls
D13 Stop Print at Stop Location

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D14..17 define the conditions to fire the print heads. A 1 will enable each head fire condition. Multiple conditions may be defined to fire the print heads. The print heads will only fire if new data has been loaded into the print heads, prior to the defined firing condition.

D14 Fire heads if A Rises
D15 Fire heads if A Falls
D16 Fire heads if B Rises
D17 Fire heads if B Falls
D18 Disable Start At Start Location if Direction is Reverse
Writing a 1 will disable a start print condition at Start Location (bit 8) if the quadrature encoder direction is reversed.
D19 Disable Start At Start Location if Direction is Forward
Writing a 1 will disable a start print condition at Start Location (bit 8) if the quadrature encoder direction is forward.
D20 Disable Start by Zfwd if Direction is Reversed
Writing a 1 will disable a start print condition at Zfwd Edge (D4&D5) if the quadrature encoder direction is reversed.
D21 Disable Start by Zrev if Direction is Forward
Writing a 1 will disable a start print condition at Zrev Edge (D6&D7) if the quadrature encoder direction is forward.
D22..31 Reserved

2.14.11 HEAD DATA HOLDOFF: (Offset 0x48)

This register defines the time delay after all heads have completed firing until new data is clocked into the heads. The delay has a resolution of 0.25ns, providing a delay range from 0 to 1.024ms.

D0..11 Head Data Hold Off
D12..31 Reserved

2.14.12 QUADRATURE TRANSISTION DELAY COUNT: (Offset 0x4C)

This register adds a head firing delay based on the number of quadrature transitions. The Quadrature Transition Delay Register defines the head fire condition such that the heads will fire on the Nth edge selector transition. The edge select firing condition is defined in bits D17-D14 of the Edge Select Register (offset 0x44).

For example:
If Edge Select Register D17..D14 = '0001' (Fire heads on Quadrature Input A rising), and Quadrature Transition Delay Register = 0x00000008, then the heads will fire on every 8th rising edge transition of the quadrature input A.

The head fire delay will still apply to define the time from the transition to the head fire signal. If this register is a '0x00000000' or '0x00000001', the print heads will fire on every detected edge select condition.

D0.. 11 Quadrature Transition Delay Count
D12..31 Reserved

2.14.13 START POSITION: (Offset 0x50)

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This register provides a relative position, which may be used to start printing.

D0..19 Start Position
D20..31 Reserved

2.14.14 STOP POSITION: (Offset 0x54)

This register provides a relative position, which may be used to stop printing.

D0..19 Stop Position
D20..31 Reserved

2.14.15 CURRENT POSITION: (Offset 0x58)

This register provides the current quadrature position used to start and/or stop printing. The position counter is reset by the condition set in the Edge Selector Register. The quadrature position will increment or decrement based on a change in the encoder A and B inputs.

D0..19 Current Position
D20..31 Reserved

2.14.16 HEAD 0 FIRE DELAY: (Offset 0x80)

Note: The following applies to all Head Fire Delay Registers:

These registers determine the delay between the head firing condition (as defined in the Edge Selector Register) and the assertion of the head fire signal. This delay has a resolution of 0.25µs, which will provide a delay between 0 and 1.024µs.

D0..11 Head 0 Fire Delay
D12..31 Reserved

2.14.17 HEAD 0 FIRE WIDTH: (Offset 0x84)

Note: The following applies to all Head Fire Width Registers:

These registers determine the amount of time the head fire signal is asserted. This timer has a resolution of 0.25µs, which will provide a firing width between 0.25µs and 1.024µs. If this register is set to a zero, a minimum firing width of 0.25µs will still be seen.

D0..11 Head 0 Fire Width
D12..31 Reserved

2.14.18 HEAD 1 FIRE DELAY: (Offset 0x88)

D0..11 Head 1Fire Delay
D12..31 Reserved

2.14.19 HEAD 1 FIRE WIDTH: (Offset 0x8C)

D0..11 Head 1 Fire Width
D12..31 Reserved

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2.14.20 HEAD 2 FIRE DELAY: (Offset 0x90)

D0..11 Head 2 Fire Delay
D12..31 Reserved

2.14.21 HEAD 2 FIRE WIDTH: (Offset 0x94)

D0..11 Head 2 Fire Width
D12..31 Reserved

2.14.22 HEAD 3 FIRE DELAY: (Offset 0x98)

D0..11 Head 3 Fire Delay
D12..31 Reserved

2.14.23 HEAD 3 FIRE WIDTH: (Offset 0x9C)

D0..11 Head 3 Fire Width
D12..31 Reserved

2.14.24 HEAD 4 FIRE DELAY: (Offset 0xA0)

D0..11 Head 4 Fire Delay
D12..31 Reserved

2.14.25 HEAD 4 FIRE WIDTH: (Offset 0xA4)

D0..11 Head 4 Fire Width
D12..31 Reserved

2.14.26 HEAD 5 FIRE DELAY: (Offset 0xA8)

D0..11 Head 5 Fire Delay
D12..31 Reserved

2.14.27 HEAD 5 FIRE WIDTH: (Offset 0xAC)

D0..11 Head 5 Fire Width
D12..31 Reserved

2.14.28 HEAD 6 FIRE DELAY: (Offset 0xB0)

D0..11 Head 6 Fire Delay
D12..31 Reserved

2.14.29 HEAD 6 FIRE WIDTH: (Offset 0xB4

D0..11 Head 6 Fire Width
D12..31 Reserved

2.14.30 HEAD 7 FIRE DELAY: (Offset 0xB8)

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D0..11 Head 7 Fire Delay
D12..31 Reserved

2.14.31 HEAD 7 FIRE WIDTH: (Offset 0xBC)

D0..11 Head 7 Fire Width
D12..31 Reserved

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CHAPTER 3: PROGRAMMING

3.0 INITIALIZATION

Initializing the PCI-HPDI32A-PRINT Card will generally need to be done only once by the software, unless the mode needs to change. The software is responsible for tracking any changes; for making all changes necessary to meet the needs of the application; and for making all the adjustments when requirements change. Most of the configuration status can be determined by reading the Board Control Register. Upon system reset, and also after a board reset is performed, the board will be in a state where the following initialization will apply:

a. all cable transceivers will be turned off;
b. all interrupts will be disabled;
c. the FIFOs will be empty;
d. all RW registers will be set to 0 (Board Control Register bits are set to 0 on system reset)

3.1 RESETS

There are two (2) bits on this board that are used as resets to the local side. Both bits are located in the Board Control Register. These bits perform a reset when the software writes a 1 to them. After writing a 1, the software does not need to return to clear the bits, the bits operate as a self-timed pulse that will return to 0 after they have been asserted long enough to perform the reset(s). For further details on the resets refer to the PCI-HPDI32A-PRINT Register Map, See Table 2.1-1.

D0: Board Reset will reset the local logic, clear the FIFOs, and place the appropriate registers into a known state.
D1: Tx FIFO Reset will reset the Tx FIFOs.

The FIFOs are reset by either a hardware system reset of the board, a software FIFO reset (Board Control Register bit 1), or a software board reset (Board Control Register bit 0).

3.2 FIFOS

The FIFOs flags are used to indicate the current fill level of the FIFO. There are four flags for Tx. These flags are labeled and defined as follows:

Empty:
Almost Empty:
Almost Full:
Full:

There are 0 true signals. The almost registers are used for programming the FIFOs, states are:

Empty – 0
Almost Empty – 0 –
Almost Full – depth –1
Full – depth

Use bit 1 of the BCR (a board reset) will not program the FIFOs. Bit 2 in the BCR will cause the Almost Empty /Almost Full Flags to program

3.3 INTERRUPTS

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In order for this board to generate interrupts to the PCI bus, Bits 8, 11, and 16 of the PLX Interrupt Control/Status Register must be set to a 1. These bits must be set to a 1 in order for the interrupts to occur.

The next step in initializing the interrupt, is to specify which interrupts are to be allowed. The board allows the software to enable some interrupts and leave others disabled. This is accomplished by writing a 1 to the appropriate bits in the Interrupt Control Register (ICR) and the Print Control/Status Register. For example, to enable the interrupt for FIFO Almost Empty, the software will need to write a 1 to bit 13 of the ICR. This bit will not need to be changed again until the need to disable this specific interrupt. This enable can be a one-time process, which will allow many interrupts to occur.

Multiple interrupts from the same source are prevented via the Interrupt Status Register (ISR). Writing to the ISR is the method by which the software acknowledges to the board that it has received the previous interrupt request and signals to the board that it may now generate any other interrupts that may occur. This register will need some attention from the software after each interrupt has occurred. Following the previous example, when this interrupt has occurred, the software will find that bit 13 of the ISR is now a 1, indicating that a FIFO Almost Empty interrupt has occurred. This bit will remain a 1 and will not allow any additional interrupts to be generated until the software performs a write to this register. To re-enable the FIFO Almost Empty interrupt, the software must write a 1 to bit 13. This will clear the occurrence of the interrupt.

The enabling, latching, and clearing of the FIFO Almost Empty status bit will not effect the other bits of the register. This means that if the software receives the interrupt for FIFO Almost Empty (the only interrupt currently enabled) the software may very well find that the FIFO is now Empty, (indicated by bit 12 being a 1). Since this bit is not enabled as an interrupt, it is acting as a status bit. If it is enabled now, it will immediately generate an interrupt.

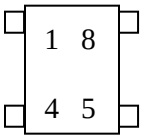
There are two potential sources for interrupts on the PCI-HPDI32-PRINT Board. The transmit FIFO flags are controlled through the ICR and ISR registers. The Print Control interrupts are controlled through the Print Control/Status Register. In addition, the Print Control Interrupt is also a status bit in the ISR. In this way, software should be able to determine the IRQ source by checking the ISR. If a transmit FIFO flag is the source, the interrupt will be cleared via the ISR. If the Print Control Interrupt is the source, the software must check the PCSR to determine the true cause. The Interrupt will be cleared by software through the PCSR.

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CHAPTER 4: HARDWARE CONFIGURATION

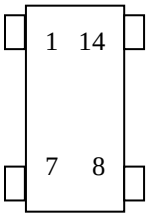
4.0 THE ON-BOARD TRANSMIT CLOCK

The on-board oscillator, U70, is used as the transmit clock for the synchronizing the transmit logic. The oscillator is factory installed at 12MHz. Using the 12MHz oscillator gives the transfer rate of 96Mbytes/sec. This oscillator can be changed in the field by the end user. Since the clock controls all the print head timing delays, changing this value will scale all the print head timing delays appropriately.



Pin	Name
1	NC
4	GND
5	OUT
8	VDD

8 pin oscillator pin-out



Pin	Name
1	NC
7	GND
8	OUT
14	VDD

14 pin oscillator pin-out

Figure 4.0-1: Oscillator specification

4.1 EEPROM JUMPER (J1)

The EEPROM jumper (J1) is a 1x2 header. This jumper is for manufacturer uses only. It should not be necessary for any users of the PCI-HPDI32A-PRINT to perform any operations involving this jumper; this section is an only explanation of its purpose.

This jumper connects the PNP EEPROM to the PCI chip set, called the PCI9080, from PLX Technologies. When this board is first assembled, the contents of the PNP EEPROM is considered, by General Standards Corporation, to be unknown. On power up or reset, this EEPROM is used to configure the boards PCI interface so that it may operate properly with plug-n-play systems. If this EEPROM is not programmed with the correct data, then the system could easily be frozen, rendering it inoperable. This jumper is used to disconnect the EEPROM from the PCI chip set; therefore forcing the PCI chip set into believing that the EEPROM is not present or has been erased. This will force the PCI chip set into a default state that will allow the system to complete the power up or reset cycle. After the system is running, the jumper may now be installed and the EEPROM programmed with the correct values. This cycle, involving the PNP EEPROM and the jumper J1, should only need to be performed one time. This is all done during the testing of each board. Once the PNP EEPROM has been programmed with the correct values, J1 should never need to be removed. If the jumper shunt for J1 is removed, the board can be expected to operate incorrectly.

Summary of Jumper Shunt for J1:

This jumper must **not** be installed on first power up, but must be permanently installed before programming the PNP EEPROM. The removal of the jumper will prevent the EEPROM from programming the PLX upon power up or reset, thus, causing the PLX to go into a default configuration. When the PLX is in its default configuration, the performance of the board is to be considered unknown and untested by General Standards Corporation.

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4.2 CABLE CONNECTOR

The 80-pin user connector (reference designator: P1) is manufactured by Robinson Nugent, the part number is P50E-080-P1-SR1-TG. The part number for the mate is P50E-080-S-TG, (50 mil. cabling is suggested for twisted pair), or P25E-080S-TG (25 mil. cabling may be used for multi-drop capability, but with loss of twisted pair).

Table 4.2-1: Cable Pin-Out:

Pin No.	Cable Signal Name
1	TX CLOCK+
2	TX CLOCK-
3	RESERVED
4	RESERVED
5	RESERVED
6	RESERVED
7	QUADRATURE A INPUT+
8	QUADRATURE A INPUT-
9	QUADRATURE B INPUT+
10	QUADRATURE B INPUT-
11	ZFWD INPUT+
12	ZFWD INPUT-
13	ZREV INPUT+
14	ZREV INPUT-
15	RESERVED
16	RESERVED
17	HEAD0 D0+
18	HEAD0 D0 -
19	HEAD0 D1+
20	HEAD0 D1 -
21	HEAD0 CLOCK+
22	HEAD0 CLOCK-
23	HEAD0 FIRE+
24	HEAD0 FIRE-
25	HEAD1 D0+
26	HEAD1 D0 -
27	HEAD1 D1+
28	HEAD1 D1 -
29	HEAD1 CLOCK+
30	HEAD1 CLOCK-
31	HEAD1 FIRE+
32	HEAD1 FIRE-
33	HEAD2 D0+
34	HEAD2 D0 -
35	HEAD2 D1+
36	HEAD2 D1 -
37	HEAD2 CLOCK+
38	HEAD2 CLOCK-
39	HEAD2 FIRE+
40	HEAD2 FIRE-

Pin No.	Cable Signal Name
41	HEAD3 D0+
42	HEAD3 D0 -
43	HEAD3 D1+
44	HEAD3 D1 -
45	HEAD3 CLOCK+
46	HEAD3 CLOCK-
47	HEAD3 FIRE+
48	HEAD3 FIRE-
49	HEAD4 D0+
50	HEAD4 D0 -
51	HEAD4 D1+
52	HEAD4 D1 -
53	HEAD4 CLOCK+
54	HEAD4 CLOCK-
55	HEAD4 FIRE+
56	HEAD4 FIRE-
57	HEAD5 D0+
58	HEAD5 D0 -
59	HEAD5 D1+
60	HEAD5 D1 -
61	HEAD5 CLOCK+
62	HEAD5 CLOCK-
63	HEAD5 FIRE+
64	HEAD5 FIRE-
65	HEAD6 D0+
66	HEAD6 D0 -
67	HEAD6 D1+
68	HEAD6 D1 -
69	HEAD6 CLOCK+
70	HEAD6 CLOCK-
71	HEAD6 FIRE+
72	HEAD6 FIRE-
73	HEAD7 D0+
74	HEAD7 D0 -
75	HEAD7 D1+
76	HEAD7 D1 -
77	HEAD7 CLOCK+
78	HEAD7 CLOCK-
79	HEAD7 FIRE+
80	HEAD7 FIRE-

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