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PCI-SIO4

User Manual

General Standards Corporation
8302A Whitesburg Drive
Huntsville, AL 35802
Phone: (256) 880-8787
Fax: (256) 880-8788
URL: www.generalstandards.com
E-mail: techsupport@generalstandards.com/

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PREFACE

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8302A Whitesburg Drive
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Telephone: (256) 880-8787
Fax: (256) 880-8788
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This user's manual provides information on the, register level programming, of the PCI-SIO4 board.

Information required for customized software development.

This manual assumes that the user is familiar with the PCI bus interface specification. In an effort to avoid redundancy, this manual relies on data books, other manuals, and specifications as indicated in the related publication section.

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RELATED PUBLICATIONS

EIA Standard for the RS-422A Interface (EIA order number EIA-RS-422A)

Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC

Sponsored by the
Bus Architecture Standards Committee
of the IEEE Computer Society

P1386.1/Draft 2.0
April 4,1995
Sponsor Ballot Draft

For questions or comments regarding this draft, please contact either the chair or draft editor of this proposed standard:

Wayne Fisher
PMC Chair
2001 Logic Drive
San Jose, CA 95124-3456 USA
Ph: 408-369-6250
Fax: 408-371-3382
Em: wfisher@fci.com

Dave Moore
PMC Draft Editor
Digital Equipment Corporation
146 Main Street MLO11-4/U32
Maynard, MA 01754-2571 USA
Ph: 408-493-2257
Fax: 408-493-0652
E-mail: moore@eng.pko.dec.com

PCI Local Bus Specification Revision 2.1 June 1, 1995. Questions regarding the PCI specification should be forwarded to:

PCI Special Interest Group

P.O. Box 14070

Portland, OR 97214
(800) 433- 5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

Zilog User's Manual and Product Specifications Databook for the Z16C30 USC requests should be forwarded to:

ZILOG, Inc.
210 East Hacienda Ave.
Campbell, CA 95008-6600
(408) 370-8000

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CHAPTER 1: INTRODUCTION

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1.0 INTRODUCTION

The PCI-SI04 interface card is capable of transmitting and receiving serial data, generating interrupts, and also provides loop-back testing.

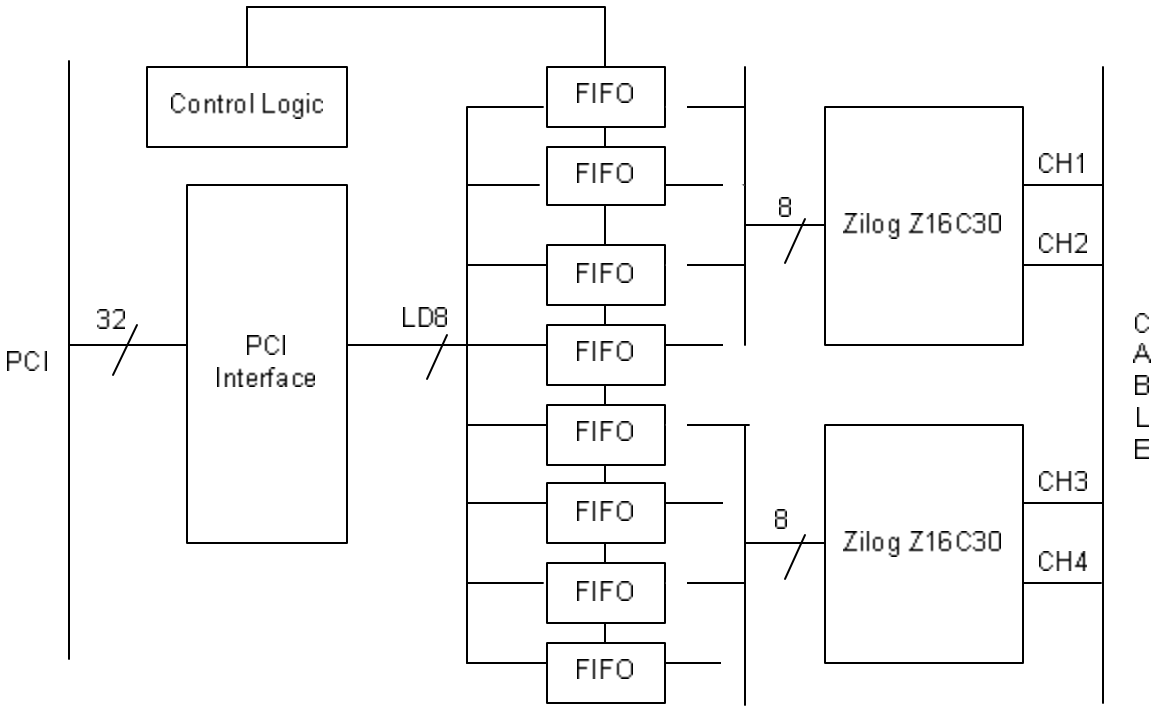
This card provides the following specific functionalities:

- PCI Bus Interface
- Interrupt functionality
- FIFOs are provided for data transmit and for data receive to increase the size of the receive buffers.
- User interface signals connections are provided via connectors on the front panel.

1.1 FUNCTIONAL DESCRIPTION

As shown in the functional block diagram (see Figure 1.1-1), this board includes the following:

- PCI Bus Slave Interface
- RS 485/422 Differential Cable Transceivers
- 2 Universal Serial Controllers (USC), The (Zilog ZI6C30s)
- Transmit FIFO Buffers
- Receive FIFO Buffers



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1.2 BOARD CONTROL REGISTER

The board control register will provide configuration for the PCI/DMA request priorities.

1.3 BOARD STATUS REGISTER

The board status register will provide status of the board (for future expansion).

1.4 SYNC WORD SELECTION REGISTERS

The sync word selection registers are used to provide an interrupt upon the reception of a particular character on a particular channel. The character is software programmable.

1.5 DATA RECEPTION

Data is received into the Zilog Z16C30. After the data is received, the software may retrieve the data from the Z16C30 or have the data buffered into the main Rx FIFOs and retrieved by the software at a later time, depending on how the Z16C30 has been initialized.

1.6 DATA TRANSMISSION

Data is placed into the Zilog Z16C30 or buffered into the main Tx FIFOs, depending on how the Z16C30 has been initialized. The Zilog can transmit and receive in any of several serial protocols:

- Asynchronous
- External Sync
- Isochronous
- Asynchronous with Code Violations
- Monosynchronous
- Bisynchronous
- HDLC
- SDLC
- Plus many more

1.7 ERROR DETECTION

By utilizing the features of the Z16C30, various forms of error detection are built into the board. The following are some of the methods of error detection available:

- Parity error detection
- CRC error detection
- Rx overrun
- Tx underrun

1.8 INTERRUPTS

Interrupts will be provided for the following conditions:

- DMA Complete
- Sync word detected

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- Tx FIFO almost empty
- Rx FIFO almost full
- Exited Hunt
- IdleRcvd
- Break/Abort
- RxBound
- Abort/ParityError
- RxOverrun
- Plus many others

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CHAPTER 2: LOCAL SPACE REGISTERS

2.0 REGISTER MAP

Table 2.0-1: PCI-SIO4 Register Address Map

Offset Address	Size	Access*	Register Name	Value after Programming
0x00	D32	RW	Firmware Revision	0xFFFF0001
0x04	D32	RW	Board Control	0xXXXX0000
0x08	Reserved			
0x0C	D32	RW	Clock Control	0xXXXX0000
0x10	D32	RW	Channel 1 Tx Almost	0xXXXXXXXX
0x14	D32	RW	Channel 1 Rx Almost	0xXXXXXXXX
0x18	D32	RW	Channel 1 FIFO	Empty
0x1C	D32	RW	Channel 1 Control/Status	0xXXXXCCXX
0x20	D32	RW	Channel 2 Tx Almost	0xXXXXXXXX
0x24	D32	RW	Channel 2 Rx Almost	0xXXXXXXXX
0x28	D32	RW	Channel 2 FIFO	Empty
0x2C	D32	RW	Channel 2 Control/Status	0xXXXXCCXX
0x30	D32	RW	Channel 3 Tx Almost	0xXXXXXXXX
0x34	D32	RW	Channel 3 Rx Almost	0xXXXXXXXX
0x38	D32	RW	Channel 3 FIFO	Empty
0x3C	D32	RW	Channel 3 Control/Status	0xXXXXCCXX
0x40	D32	RW	Channel 4 Tx Almost	0xXXXXXXXX
0x44	D32	RW	Channel 4 Rx Almost	0xXXXXXXXX
0x48	D32	RW	Channel 4 FIFO	Empty
0x4C	D32	RW	Channel 4 Control/Status	0xXXXXCCXX
0x50	D32	RW	Channel 1 Sync Detected	0xXXXXXX00
0x54	D32	RW	Channel 2 Sync Detected	0xXXXXXX00
0x58	D32	RW	Channel 3 Sync Detected	0xXXXXXX00
0x5C	D32	RW	Channel 4 Sync Detected	0xXXXXXX00
0x60	D32	RW	Interrupt Control	0x00000000
0x64	D32	RW	Interrupt Status	0x00000000
0x100	D8	see Zilog Reference Data Book	Channel 1 USC	see Zilog Reference Data Book
0x200	D8		Channel 2 USC	
0x300	D8		Channel 3 USC	
0x400	D8		Channel 4 USC	

* RO = read only, WO = write only, RW = read/write capability, BD = Bit Dependent

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2.1 BIT MAP FOR LOCAL SPACE REGISTERS

When writing to the registers all reserved bits should be set to **0** for future compatibility. Also, the value read from a reserved bit will be indeterminate.

2.1.0 FIRMWARE REVISION: (LOC 0X00)

D0..31 0x00000000 Original Revision

2.1.1 BOARD CONTROL: (LOC 0X04)

D2: 0 DEMAND MODE DMA CHANNEL 0 REQUEST ENCODER

2 1 0

0 0 0 Request DMA on Serial Channel 1 Rx FIFO Almost Full - Hold until Serial Channel 1 Rx FIFO Almost Empty

1 0 0 Request DMA on Serial Channel 1 Tx FIFO Almost Empty - Hold until Serial Channel 1 Tx FIFO Almost Full

0 1 0 Request DMA on Serial Channel 2 Rx FIFO Almost Full - Hold until Serial Channel 2 Rx FIFO Almost Empty

1 1 0 Request DMA on Serial Channel 2 Tx FIFO Almost Empty - Hold until Serial Channel 2 Tx FIFO Almost Full

0 0 1 Request DMA on Serial Channel 3 Rx FIFO Almost Full - Hold until Serial Channel 3 Rx FIFO Almost Empty

1 0 1 Request DMA on Serial Channel 3 Tx FIFO Almost Empty - Hold until Serial Channel 3 Rx FIFO Almost Empty

0 1 1 Request DMA on Serial Channel 4 Rx FIFO Almost Full - Hold until Serial Channel 4 Rx FIFO Almost Empty

1 1 1 Request DMA on Serial Channel 4 Tx FIFO Almost Empty - Hold until Serial Channel 4 Rx FIFO Almost Empty

D3 Reserved

D4:6 Demand Mode DMA Channel Request Encoder

6 5 4

0 0 0 Request DMA on Serial Channel 1 Rx FIFO Almost Full - Hold until Serial Channel 1 Rx FIFO Almost Empty

1 0 0 Request DMA on Serial Channel 1 Tx FIFO Almost Empty - Hold until Serial Channel 1 Tx FIFO Almost Full

0 1 0 Request DMA on Serial Channel 2 Rx FIFO Almost Full - Hold until Serial Channel 2 Rx FIFO Almost Empty

1 1 0 Request DMA on Serial Channel 2 Tx FIFO Almost Empty - Hold until Serial Channel 2 Tx FIFO Almost Full

0 0 1 Request DMA on Serial Channel 3 Rx FIFO Almost Full - Hold until Serial Channel 3 Rx FIFO Almost Empty

1 0 1 Request DMA on Serial Channel 3 Tx FIFO Almost Empty - Hold until Serial Channel 3 Rx FIFO Almost Empty

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0 1 1 Request DMA on Serial Channel 4 Rx FIFO Almost Full - Hold until Serial Channel 4 Rx FIFO Almost Empty

1 1 1 Request DMA on Serial Channel 4 Tx FIFO Almost Empty - Hold until Serial Channel 4 Rx FIFO Almost Empty Serial Channel

D31:7 Reserved

2.1.2 CLOCK CONTROL: (LOC 0X0C)

D0..15 Clock Controls for all 4 channels

D0 Channel 1 Enable Drive Upper Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 1 Tx Clk on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D1 Channel 1 Enable Drive Lower Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 1 Tx Clk on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D2 Channel 1 Enable Receive Upper Clk
Writing a '1' to this bit will turn on the receiver for the Channel 1 Rx clock on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D3 Channel 1 Enable Receive Lower Clk
Writing a '1' to this bit will turn on the receiver for the Channel 1 Rx clock on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D4 Channel 2 Enable Drive Upper Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 2 Tx Clk on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D5 Channel 2 Enable Drive Lower Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 2 Tx Clk on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D6 Channel 2 Enable Receive Upper Clk
Writing a '1' to this bit will turn on the receiver for the Channel 2 Rx clock on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D7 Channel 2 Enable Receive Lower Clk
Writing a '1' to this bit will turn on the receiver for the Channel 2 Rx clock on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D8 Channel 3 Enable Drive Upper Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 3 Tx Clk on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D9 Channel 3 Enable Drive Lower Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 3 Tx Clk on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

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D10 Channel 3 Enable Receive Upper Clk
Writing a '1' to this bit will turn on the receiver for the Channel 3 Rx clock on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D11 Channel 3 Enable Receive Lower Clk
Writing a '1' to this bit will turn on the receiver for the Channel 3 Rx clock on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D12 Channel 4 Enable Drive Upper Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 4 Tx Clk on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D13 Channel 4 Enable Drive Lower Clk
Writing a '1' to this bit will turn on the transmitter for the Channel 4 Tx Clk on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a driven state.

D14 Channel 4 Enable Receive Upper Clk
Writing a '1' to this bit will turn on the receiver for the Channel 4 Rx clock on the upper portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

D15 Channel 4 Enable Receive Lower Clk
Writing a '1' to this bit will turn on the receiver for the Channel 4 Rx clock on the lower portion of the cable. This will cause this signal on the cable to go from a tri-state condition to a loaded condition.

2.1.4 CHANNEL 1 TX ALMOST: (LOC 0X10)

D0..31 Channel 1 Tx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.

D0..15 Used for the Almost Empty Flag

D16..31 Used for the Almost Full Flag

2.1.5 CHANNEL 1 RX ALMOST: (LOC 0X14)

D0..31 Channel 1 Rx Almost Data
The data in this register is used for programming the Almost Flags of the Rx FIFOs for this channel.

D0..15 Used for the Almost Empty Flag

D16..31 Used for the Almost Full Flag

2.1.6 CHANNEL 1 FIFO: (LOC 0X18)

D0..7 Channel 1 FIFO Data
The FIFOs are setup in a way that the Rx FIFO and the Tx FIFO are located at the same address. A write to this address will be directed toward the Tx FIFO, and a read from this address will be directed toward the Rx FIFO.

D8..31 Reserved

2.1.7 CHANNEL 1 CONTROL/STATUS: (LOC 0X1C)

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D0 Reset Channel 1 Tx FIFO (Pulsed)

Writing a '1' to this bit will cause the channel 1 Tx FIFOs to be reset. If the channel 1 Tx Almost register is not a value of 0x00000000 then this will also cause the channel 1 Tx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

D1 Reset Channel 1 Rx FIFO (Pulsed)

Writing a '1' to this bit will cause the channel 1 Rx FIFOs to be reset. If the channel 1 Rx Almost register is not a value of 0x00000000 then this will also cause the channel 1 Rx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself..

D2 Enable the Channel 1 Transmitters for the Upper portion of the cable (will drive the cable)

Writing a '1' to this bit will turn on the transmitters for the Channel 1 upper portion of the cable. The signals that are turned on are the Channel 1 TxD and Channel 1 CTS on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D3 Enable the Channel 1 Transmitters for the Lower portion of the cable (will drive the Cable)

Writing a '1' to this bit will turn on the transmitters for the Channel 1 lower portion of the cable. The signals that are turned on are the Channel 1 TxD and Channel 1 CTS on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D4 Enable the Channel 1 Receivers for the Upper portion of the cable (will load the cable)

Writing a '1' to this bit will turn on the receivers for the Channel 1 upper portion of the cable. The signals that are turned on are the Channel 1 RxD and Channel 1 DCD on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D5 Enable the Channel 1 Receivers for the Lower portion of the cable (will load the cable)

Writing a '1' to this bit will turn on the receivers for the Channel 1 lower portion of the cable. The signals that are turned on are the Channel 1 RxD and Channel 1 DCD on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D6 Reserved

D7 Reset Zilog for Channel 1-2 (Pulsed)

Writing a '1' to this bit will cause the channel 1-2 Zilog Z16C30 USC to be reset. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

Note: After power up and after any reset to this component, the next access to channel 1 or channel 2 USC must be a write of 0x00 to offset 0x00 of channel 1 USC.

D8 Channel 1 Tx FIFO Empty (TRUE == 0)

D9 Channel 1 Tx FIFO Almost Empty (TRUE == 0)

D10 Channel 1 Tx FIFO Almost Full (TRUE == 0)

D11 Channel 1 Tx FIFO Full (TRUE == 0)

D12 Channel 1 Rx FIFO Empty (TRUE == 0)

D13 Channel 1 Rx FIFO Almost Empty (TRUE == 0)

D14 Channel 1 Rx FIFO Almost Full (TRUE == 0)

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D15 Channel 1 Rx FIFO Full (TRUE == 0)

The FIFO status flags are active low indicators of the current FIFO status. These flags are continuously being updated every 33ns. A value of '0' indicates that the current status is true and a value of '1' indicates that it is not true. There are only 5 valid combinations for each nibble (D8..D11 or D12..D15). These combinations are as follows:

0xC	**1100**	Almost Empty and Empty
0xD	**1101**	Almost Empty but not Empty
0xF	**1111**	In between Almost Empty and Almost Full
0xB	**1011**	Almost Full but not full
0x3	**0011**	Almost Full and Full

2.1.8 CHANNEL 2 TX ALMOST: (LOC 0X20)

D7..0 Channel 2 Tx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.
D0..15 Used for the Almost Empty Flag
D16..31 Used for the Almost Full Flag

2.1.9 CHANNEL 2 RX ALMOST: (LOC 0X24)

D0..7 Channel 2 Rx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.
D0..15 Used for the Almost Empty Flag
D16..31 Used for the Almost Full Flag

2.1.10 CHANNEL 2 FIFO: (LOC 0X28)

D0..7 Channel 2 FIFO Data
The FIFOs are setup in a way that the Rx FIFO and the Tx FIFO are located at the same address. A write to this address will be directed toward the Tx FIFO, and a read from this address will be directed toward the Rx FIFO.

2.1.11 CHANNEL 2 CONTROL/STATUS: (LOC 0X2C)

D0 Reset Channel 2 Tx FIFO (Pulsed)
Writing a '1' to this bit will cause the channel 2 Tx FIFOs to be reset. If the channel 2 Tx Almost register is not a value of 0x00000000 then this will also cause the channel 2 Tx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.
D1 Reset Channel 2 Rx FIFO (Pulsed)
Writing a '1' to this bit will cause the channel 2 Rx FIFOs to be reset. If the channel 2 Rx Almost register is not a value of 0x00000000 then this will also cause the channel 2 Rx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before

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accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

D2 Enable the Channel 2 Transmitters for the Upper portion of the cable (will drive the cable)

Writing a '1' to this bit will turn on the transmitters for the Channel 2 upper portion of the cable. The signals that are turned on are the Channel 2 TxD and Channel 2 CTS on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D3 Enable the Channel 2 Transmitters for the Lower portion of the cable (will drive the Cable)

Writing a '1' to this bit will turn on the transmitters for the Channel 2 lower portion of the cable. The signals that are turned on are the Channel 2 TxD and Channel 2 CTS on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D4 Enable the Channel 2 Receivers for the Upper portion of the cable (will load the cable)

Writing a '1' to this bit will turn on the receivers for the Channel 2 upper portion of the cable. The signals that are turned on are the Channel 2 RxD and Channel 2 DCD on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D5 Enable the Channel 2 Receivers for the Lower portion of the cable (will load the cable)

Writing a '1' to this bit will turn on the receivers for the Channel 2 lower portion of the cable. The signals that are turned on are the Channel 2 RxD and Channel 2 DCD on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D6 Reserved

D7 Reset Zilog for Channel 1-2 (Pulsed)

Writing a '1' to this bit will cause the channel 1-2 Zilog Z16C30 USC to be reset. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself. Note, that after power up and after any reset to this component, the next access to channel 1 or channel 2 USC must be a write of 0x00 to offset 0x00 of channel 1 USC.

D8	Channel 2 Tx FIFO Empty	(TRUE == 0)
D9	Channel 2 Tx FIFO Almost Empty	(TRUE == 0)
D10	Channel 2 Tx FIFO Almost Full	(TRUE == 0)
D11	Channel 2 Tx FIFO Full	(TRUE == 0)
D12	Channel 2 Rx FIFO Empty	(TRUE == 0)
D13	Channel 2 Rx FIFO Almost Empty	(TRUE == 0)
D14	Channel 2 Rx FIFO Almost Full	(TRUE == 0)
D15	Channel 2 Rx FIFO Full	(TRUE == 0)

The FIFO status flags are active low indicators of the current FIFO status. These flags are continuously being updated every 33ns. A value of '0' indicates that the current status is true and a value of '1' indicates that it is not true. There are only 5 valid combinations for each nibble (D8..D11 or D12..D15). These combinations are as follows:

0xC	**1100**	Almost Empty and Empty
0xD	**1101**	Almost Empty but not Empty
0xF	**1111**	In between Almost Empty and Almost Full
0xB	**1011**	Almost Full but not full
0x3	**0011**	Almost Full and Full

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2.1.12 CHANNEL 3 TX ALMOST: (LOC 0X30)

D0..31 Channel 3 Tx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.
D0..15 Used for the Almost Empty Flag
D16..31 Used for the Almost Full Flag

2.1.13 CHANNEL 3 RX ALMOST: (LOC 0X34)

D0..31 Channel 3 Rx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.
D0..15 Used for the Almost Empty Flag
D16..31 Used for the Almost Full Flag

2.1.14 CHANNEL 3 ALMOST: (LOC 0X38)

D0..7 Channel 3 FIFO Data
The FIFOs are setup in a way that the Rx FIFO and the Tx FIFO are located at the same address. A write to this address will be directed toward the Tx FIFO, and a read from this address will be directed toward the Rx FIFO.

2.1.15 CHANNEL 3 CONTROL/STATUS: (LOC 0X3C)

D0 Reset Channel 3 Tx FIFO (Pulsed)
Writing a '1' to this bit will cause the channel 3 Tx FIFOs to be reset. If the channel 3 Tx Almost register is not a value of 0x00000000 then this will also cause the channel 3 Tx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

D1 Reset Channel 3 Rx FIFO (Pulsed)
Writing a '1' to this bit will cause the channel 3 Rx FIFOs to be reset. If the channel 3 Rx Almost register is not a value of 0x00000000 then this will also cause the channel 3 Rx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

D2 Enable the Channel 3 Transmitters for the Upper portion of the cable (will drive the cable)
Writing a '1' to this bit will turn on the transmitters for the Channel 3 upper portion of the cable. The signals that are turned on are the Channel 3 TxD and Channel 3 CTS on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D3 Enable the Channel 3 Transmitters for the Lower portion of the cable (will drive the Cable)
Writing a '1' to this bit will turn on the transmitters for the Channel 3 lower portion of the cable. The signals that are turned on are the Channel 3 TxD and

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Channel 3 CTS on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D4 Enable the Channel 3 Receivers for the Upper portion of the cable (will load the cable)
Writing a '1' to this bit will turn on the receivers for the Channel 3 upper portion of the cable. The signals that are turned on are the Channel 3 RxD and Channel 3 DCD on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D5 Enable the Channel 3 Receivers for the Lower portion of the cable (will load the cable)
Writing a '1' to this bit will turn on the receivers for the Channel 3 lower portion of the cable. The signals that are turned on are the Channel 3 RxD and Channel 3 DCD on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D6 Reserved

D7 Reset Zilog for Channel 3-4 (Pulsed)
Writing a '1' to this bit will cause the channel 3-4 Zilog Z16C30 USC to be reset. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself. Note, that after power up and after any reset to this component, the next access to channel 3 or channel 4 USC must be a write of 0x00 to offset 0x00 of channel 3 USC.

D8	Channel 3 Tx FIFO Empty	(TRUE == 0)
D9	Channel 3 Tx FIFO Almost Empty	(TRUE == 0)
D10	Channel 3 Tx FIFO Almost Full	(TRUE == 0)
D11	Channel 3 Tx FIFO Full	(TRUE == 0)
D12	Channel 3 Rx FIFO Empty	(TRUE == 0)
D13	Channel 3 Rx FIFO Almost Empty	(TRUE == 0)
D14	Channel 3 Rx FIFO Almost Full	(TRUE == 0)
D15	Channel 3 Rx FIFO Full	(TRUE == 0)

The FIFO status flags are active low indicators of the current FIFO status. These flags are continuously being updated every 33ns. A value of '0' indicates that the current status is true and a value of '1' indicates that it is not true. There are only 5 valid combinations for each nibble (D8..D11 or D12..D15). These combinations are as follows:

0xC	**1100**	Almost Empty and Empty
0xD	**1101**	Almost Empty but not Empty
0xF	**1111**	In between Almost Empty and Almost Full
0xB	**1011**	Almost Full but not full
0x3	**0011**	Almost Full and Full

2.1.16 CHANNEL 4 TX ALMOST: (LOC 0X40)

D0..31 Channel 4 Tx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.

D0..15 is used for the Almost Empty Flag

D16..31 is used for the Almost Full Flag

2.1.17 CHANNEL 4 RX ALMOST: (LOC 0X44)

D0..31 Channel 4 Rx Almost Data
The data in this register is used for programming the Almost Flags of the Tx FIFOs for this channel.

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D0..15 is used for the Almost Empty Flag
D16..31 is used for the Almost Full Flag

2.1.18 CHANNEL 4 FIFO: (LOC 0X48)

D0..7 Channel 4 FIFO Data

The FIFOs are set in a way that the Rx FIFO and the Tx FIFO are located at the same address.

A write to this address will be directed toward the Tx FIFO, and a read from this address will be directed toward the Rx FIFO.

2.1.19 CHANNEL 4 CONTROL/STATUS: (LOC 0X4C)

D0 Reset Channel 4 Tx FIFO (Pulsed)

Writing a '1' to this bit will cause the channel 4 Tx FIFOs to be reset. If the channel 4 Tx Almost register is not a value of 0x00000000 then this will also cause the channel 4 Tx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

D1 Reset Channel 4 Rx FIFO (Pulsed)

Writing a '1' to this bit will cause the channel 4 Rx FIFOs to be reset. If the channel 4 Rx Almost register is not a value of 0x00000000 then this will also cause the channel 4 Rx FIFOs almost flags to be programmed. After setting this bit to a '1', it is the software's responsibility to delay approximately 10ms before accessing the local side of the board again. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

D2 Enable the Channel 4 Transmitters for the Upper portion of the cable (will drive the cable)

Writing a '1' to this bit will turn on the transmitters for the Channel 4 upper portion of the cable. The signals that are turned on are the Channel 4 TxD and Channel 4 CTS on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D3 Enable the Channel 4 Transmitters for the Lower portion of the cable (will drive the Cable)

Writing a '1' to this bit will turn on the transmitters for the Channel 4 lower portion of the cable. The signals that are turned on are the Channel 4 TxD and Channel 4 CTS on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a driven state.

D4 Enable the Channel 4 Receivers for the Upper portion of the cable (will load the cable)

Writing a '1' to this bit will turn on the receivers for the Channel 4 upper portion of the cable. The signals that are turned on are the Channel 4 RxD and Channel 4 DCD on the upper portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D5 Enable the Channel 4 Receivers for the Lower portion of the cable (will load the cable)

Writing a '1' to this bit will turn on the receivers for the Channel 4 lower portion of the cable. The signals that are turned on are the Channel 4 RxD and Channel 4 DCD on the lower portion of the cable. This will cause these signals on the cable to go from a tri-state condition to a loaded condition.

D6 Reserved

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D7 Reset Zilog for Channel 3-4 (Pulsed)

Writing a '1' to this bit will cause the channel 3-4 Zilog Z16C30 USC to be reset. This bit is a self-timed pulse; therefore, it is not necessary for software to return to clear this bit, it will clear itself.

Note: After power up and after any reset to this component, the next access to channel 3 or channel 4 USC must be a write of 0x00 to offset 0x00 of channel 3 USC.

D8	Channel 4 Tx FIFO Empty	(TRUE == 0)
D9	Channel 4 Tx FIFO Almost Empty	(TRUE == 0)
D10	Channel 4 Tx FIFO Almost Full	(TRUE == 0)
D11	Channel 4 Tx FIFO Full	(TRUE == 0)
D12	Channel 4 Rx FIFO Empty	(TRUE == 0)
D13	Channel 4 Rx FIFO Almost Empty	(TRUE == 0)
D14	Channel 4 Rx FIFO Almost Full	(TRUE == 0)
D15	Channel 4 Rx FIFO Full	(TRUE == 0)

The FIFO status flags are active low indicators of the current FIFO status. These flags are continuously being updated every 33ns. A value of '0' indicates that the current status is true and a value of '1' indicates that it is not true. There are only 5 valid combinations for each nibble (D8..D11 or D12..D15). These combinations are as follows:

0xC	**1100**	Almost Empty and Empty
0xD	**1101**	Almost Empty but not Empty
0xF	**1111**	In between Almost Empty and Almost Full
0xB	**1011**	Almost Full but not full
0x3	**0011**	Almost Full and Full

2.1.20 CHANNEL 1 SYNC DETECT: (LOC 0X50)

D0..7 Channel 1 Sync Detected Data

The data in this register is used to watch the Rx data as it is being loaded into the main Rx FIFO. If the data being loaded into the FIFO for this channel matches this data, then an interrupt request will be generated to the interrupt logic. An actual interrupt to the host will only occur if this interrupt source is enable in the interrupt control register.

2.1.21 CHANNEL 2 SYNC DETECT: (LOC 0X54)

D0..7 Channel 2 Sync Detected Data

The data in this register is used to watch the Rx data as it is being loaded into the main Rx FIFO. If the data being loaded into the FIFO for this channel matches this data, then an interrupt request will be generated to the interrupt logic. An actual interrupt to the host will only occur if this interrupt source is enable in the interrupt control register.

2.1.22 CHANNEL 3 SYNC DETECT: (LOC 0X58)

D0..7 Channel 3 Sync Detected Data

The data in this register is used to watch the Rx data as it is being loaded into the main Rx FIFO. If the data being loaded into the FIFO for this channel matches this data, then an interrupt request will be generated to the interrupt logic. An

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actual interrupt to the host will only occur if this interrupt source is enable in the interrupt control register.

2.1.23 CHANNEL 4 SYNC DETECT: (LOC 0X5C)

D0..7 Channel 4 Sync Detected Data

The data in this register is used to watch the Rx data as it is being loaded into the main Rx FIFO. If the data being loaded into the FIFO for this channel matches this data, then an interrupt request will be generated to the interrupt logic. An actual interrupt to the host will only occur if this interrupt source is enable in the interrupt control register.

2.1.24 INTERRUPT CONTROL: (LOC 0X60)

D0 Enable Channel 1 Interrupt on Sync Detected
D1 Enable Channel 1 Interrupt on Tx FIFO Almost Empty
D2 Enable Channel 1 Interrupt on Rx FIFO Almost Full
D3 Enable Channel 1 Interrupt on USC Request Interrupt
D4 Enable Channel 2 Interrupt on Sync Detected
D5 Enable Channel 2 Interrupt on Tx FIFO Almost Empty
D6 Enable Channel 2 Interrupt on Rx FIFO Almost Full
D7 Enable Channel 2 Interrupt on USC Request
D8 Enable Channel 3 Interrupt on Sync Detected
D9 Enable Channel 3 Interrupt on Tx FIFO Almost Empty
D10 Enable Channel 3 Interrupt on Rx FIFO Almost Full
D11 Enable Channel 3 Interrupt on USC Request Interrupt
D12 Enable Channel 4 Interrupt on Sync Detected
D13 Enable Channel 4 Interrupt on Tx FIFO Almost Empty
D14 Enable Channel 4 Interrupt on Rx FIFO Almost Full
D15 Enable Channel 4 Interrupt on USC Request Interrupt

Note: A '1' in any of these positions will enable the corresponding interrupt source to perform a PCI interrupt. A '0' in any of these positions will disable the corresponding interrupt source from performing a PCI interrupt.

2.1.25 INTERRUPT STATUS: (LOC 0X64)

D0 Status on Channel 1 Interrupt for Sync Detected
D1 Status on Channel 1 Interrupt for Tx FIFO Almost Empty
D2 Status on Channel 1 Interrupt for Rx FIFO Almost Full
D3 Status on Channel 1 Interrupt for USC Request Interrupt
D4 Status on Channel 2 Interrupt for Sync Detected
D5 Status on Channel 2 Interrupt for Tx FIFO Almost Empty
D6 Status on Channel 2 Interrupt for Rx FIFO Almost Full
D7 Status on Channel 2 Interrupt for USC Request
D8 Status on Channel 3 Interrupt for Sync Detected
D9 Status on Channel 3 Interrupt for Tx FIFO Almost Empty
D10 Status on Channel 3 Interrupt for Rx FIFO Almost Full
D11 Status on Channel 3 Interrupt for USC Request Interrupt
D12 Status on Channel 4 Interrupt for Sync Detected
D13 Status on Channel 4 Interrupt for Tx FIFO Almost Empty
D14 Status on Channel 4 Interrupt for Rx FIFO Almost Full

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D15 Status on Channel 4 Interrupt for USC Request Interrupt

Note: A '1', in any of these positions, will indicate that the corresponding source has either performed a PCI interrupt or that the source for the interrupt is currently active; thus, could perform a PCI interrupt if enabled in the interrupt control register. Whether or not the interrupt was performed depends on the interrupt control register.
If the corresponding bit in the interrupt control register is a '0', then the source has not performed a PCI interrupt and is only indicating the current status of that source.
If the corresponding bit in the interrupt control register is a '1', then the source has performed a PCI interrupt and has latched itself. Writing a '1' to the respective bit in the interrupt status register clears the interrupt status bit. A second interrupt will not occur until after that status bit has been cleared. The interrupts are not queued; hence, each potential interrupt should be observed when identifying the source and clearing the status register. Failure to do so could prevent any other interrupts from occurring.

2.2 USC REGISTERS

2.2.1 CHANNEL 1 USC: (LOC 0X100 TO 0X17E)

D0..7 Channel 1 USC Data (Zilog Data Bus, See Serial Controller Registers)

2.2.2 CHANNEL 2 USC: (LOC 0X200 TO 0X27E)

D0..7 Channel 2 USC Data (Zilog Data Bus, See Serial Controller Registers)

2.2.3 CHANNEL 3 USC: (LOC 0X300 0X37E)

D0..7 Channel 3 USC Data (Zilog Data Bus, See Serial Controller Registers)

2.2.4 CHANNEL 4 USC: (LOC 0X400 TO 0X47E)

D0..7 Channel 4 USC Data (Zilog Data Bus, See Serial Controller Registers)

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2.3 SERIAL CONTROLLER REGISTERS

IMPORTANT: Write to Loc 0x100 and Loc 0x300 after every reset to confirm the USC address system. Contact your local Zilog Representative for Data books and User manuals in reference to the Z16C30, USC Universal Serial Controller, for a more detailed description of the following registers. It is the advice of the design engineer of this product that both books should be obtained by any persons desiring to design using this product. See Related Publications section of this document for address of Zilog.

Note: In the following register addresses 'n' stands for Channel Number.

2.3.1 CHANNEL COMMAND/ADDRESS REGISTER (CCAR)

(Same format for Channels 0..3 USC Control Registers)

2.3.1.1 Low: (LOC 0xn00)

D0	WO	Upper/Lower Byte Select
D1..D5	WO	Address 4..0
D6	WO	Byte/Word Access
D7	WO	DMA Continue

The contents of this register should always be set to 0x00 for this product.

2.3.1.2 High: (LOC: 0xn01)

D0..D1 WO Mode Control (encoded as follows):

D9 D8
0 0 Normal Operation
0 1 Auto Echo
1 0 External Local Loop-back
1 1 Internal Local Loop-back

D2 Channel Reset

D3..7 WO Channel Command (encoded as follows, D11 as the LSB):

00000 Null Command
00001 Reserved
00010 Reset Highest IUS
00011 Trigger Channel Load DMA
00101 Trigger Rx DMA
00110 Trigger Tx DMA
00111 Trigger Rx & Tx DMA
00100 Reserved
00100 Rx FIFO Purge
00101 Tx FIFO Purge
01011 Rx & Tx FIFO Purge
01100 Reserved
01101 Load Rx Character Count
01110 Load Tx Character Count
01111 Reserved

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10000 Load TC0
10001 Load TC1
10010 Load TC0 & TC1
10011 Select Serial Data LSB First*
10100 Select Serial Data MSB First
10101 Select Straight Memory Data*
10110 Select Swapped Memory Data
10111 Reserved
11000 Rx Purge
11001 Reserved
11010 Reserved
11011 Reserved
11100 Reserved
11101 Reserved
11110 Reserved
11111 Reserved

*Selected upon reset

2.3.2 CHANNEL MODE REGISTER (CMR)

2.3.2.1 Low: (LOC 0xn02)

D0..D3 WO Receiver Mode (encoded as follows):

0000 Asynchronous
0001 External Synchronous
0010 Isochronous
0011 Asynchronous with CV
0100 Monosync
0101 Bisync
0110 HDLC
0111 Transparent Bisync
1000 NBIP
1001 802.3
1010 Reserved
1011 Reserved
1100 Reserved
1101 Reserved
1110 Reserved
1111 Reserved

D4..D7 Rx Submode 3..0

2.3.2.2 High: (LOC 0xn03)

D0..3 Transmitter Mode (encoded as follows):

0000 Asynchronous
0001 Reserved
0010 Isochronous
0011 Asynchronous with CV

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0100 Monosync
0101 Bisync
0110 HDLC
0111 Transparent Bisync
1000 NBIP
1001 802.3
1010 Reserved
1011 Reserved
1100 Slaved Monosync
1101 Reserved
1110 HDLC Loop
1111 Reserved

D4..7 Tx Submode 3..0

2.3.3 CHANNEL COMMAND/STATUS REGISTER (CCSR)

2.3.3.1 Low: (LOC 0xn04)

D0 RO RxACK
D1 RO TxACK
D2..4 HDLC Tx Last Character Length (encoded as follows):

000 8 bits
001 1 bit
010 2 bits
011 3 bits
100 4 bits
101 5 bits
110 6 bits
111 7 bits

D5 Reserved
D6 RO Loop Sending
D7 RO On Loop

2.3.3.2 High: (LOC 0xn05)

D0..1 DPLL Adjust/Sync Edge (encoded as follows):

00 Both Edges
01 Rising Edge Only
10 Falling Edge Only
11 Adjust/Sync Inhibit

D2 RW Clocks Missed Latched/Unlatch
D3 RW Clocks Missed Latched/Unlatch
D4 RW DPLL in Sync/Quick Sync
D5 WO RCC FIFO Clear
D6 RO RCC FIFO Valid
D7 RO RCC FIFO Overflow

2.3.4 CHANNEL CONTROL REGISTER (CCR)

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2.3.4.1 Low: (LOC 0xn06)

D0..4 Reserved
D5 Wait for Rx DMA Trigger
D6..7 Rx Status Block Transfer (encoded as follows, D6 being the LSB):
- 00 No Status Block
- 01 One word Status Block
- 10 Two word Status Block
- 11 Reserved

2.3.4.2 High: (LOC 0xn07)

D0..1 Tx Preamble Pattern (encoded as follows):
- 00 All Zeros
- 01 All Ones
- 10 Alternating 1 & 0
- 11 Alternating 0 & 1

D2..3 Tx Preamble Length (encoded as follows):
- 00 8 bits
- 01 16 bits
- 10 32 bits
- 11 64 bits

D4 Tx Flag Preamble
D6..7 Tx Status Block Transfer (encoded as follows):
- 00 No Status Block
- 01 One word Status Block
- 10 Two word Status Block
- 11 Reserved

2.3.5 PRIMARY RESERVED REGISTER (RESERVED)

2.3.5.1 Low: (LOC 0xn08)

D0..D7 RW Reserved

2.3.5.2 High: (LOC 0xn09)

D0..D7 RW Reserved

2.3.6 SECONDARY RESERVED REGISTER (RESERVED)

2.3.6.1 Low: (LOC 0xnA)

D0..D7 RW Reserved

2.3.6.2 High: (LOC 0xnB)

D0..D7 RW Reserved

2.3.7 TEST MODE DATA REGISTER (TMDR)

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2.3.7.1 Low: (LOC: 0xnC)

D0..D7 RW Test Data 7..0

2.3.7.2 High: (LOC 0xn1A)

D0..D7 RW Test Data 7..0

2.3.8 TEST MODE CONTROL REGISTER (TMCR)

2.3.8.1 Low: (LOC 0xnE)

D0..4 Test Register Address (encoded as follows):

00000	Null Address
00001	High Byte of Shifters
00010	CRC Byte 0
00011	CRC Byte 1
00100	Rx FIFO (Write)
00101	Clock Multiplexer Outputs
00110	CTR0 and CTR1 Counters
00111	Clock Multiplexer Inputs
01000	DPLL State
01001	Low Byte of Shifters
01010	CRC Byte 2
01011	CRC Byte 3
01100	Tx FIFO (Read)
01101	Reserved
01110	I/O and Device Status Latches
01111	Internal Daisy Chain
10000	Reserved
10001	Reserved
10010	Reserved
10011	Reserved
10100	Reserved
10101	Reserved
10110	Reserved
10111	Reserved
11000	4044H
11001	4044H
11010	4044H
11011	4044H
11100	4044H
11101	4044H
11110	4044H
11111	4044H

D5..7 RW Reserved

2.3.8.2 High: (LOC 0xn0F)

D0..7 RW Reserved

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2.3.9 CLOCK MODE CONTROL REGISTER (CMCR)

2.3.9.1 Low: (LOC 0xn10)

D0..2 RW Receive Clock Source (encoded as follows):

000 Disabled
001 /RxC Pin
010 /TxC Pin
011 DPLL Output
100 BRG0 Output
101 BRG1 Output
110 CTR0 Output
111 CTR1 Output

D3..5 RW Transmit Clock Source (encoded as follows):

000 Disabled
001 /RxC Pin
010 /TxC Pin
011 DPLL Output
100 BRG0 Output
101 BRG1 Output
110 CTR0 Output
111 CTR1 Output

D6..7 RW DPLL Clock Source (encoded as follows):

00 BRG0 Output
01 BRG1 Output
10 /RxC Pin
11 /TxC Pin

2.3.9.2 High: (LOC 0xn11)

D0..1 BRG0 Clock Source (encoded as follows):
00 CTR0 Output
01 CTR1 Output
10 /RxC Pin
11 /TxC Pin

D2..3 BRG1 Clock Source (encoded as follows):
00 CTR0 Output
01 CTR1 Output
10 /RxC Pin
11 /TxC Pin

D4..5 CRT0 Clock Source (encoded as follows):
00 BRG0 Output
01 BRG1 Output
10 /RxC Pin

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11 /TxC Pin

D6..7 CTR1 Clock Source (encoded as follows):
00 Disabled
01 Disabled
10 /RxC Pin
11 /TxC Pin

2.3.10 HARDWARE CONFIGURATION REGISTER (HCR)

2.3.10.1 Low: (LOC 0xn12)

D1 RW BRG0 Enable
D0 RW BRG0 Single Cycle/Continuous
D2..3 Rx ACK Pin Control (encoded as follows):
00 3 - State Output
01 Rx Acknowledge Input
10 Output 0
11 Output 1
D5 RW BRG1 Enable
D4 RW BRG1 Single Cycle/Continuous
D6..7 Tx ACK Pin Control (encoded as follows):
00 3 - State Output
01 Tx Acknowledge Input
10 Output 0
11 Output 1

2.3.10.2 High: (LOC 0xn13)

D0..D1 DPLL Mode (encoded as follows):
00 Disabled
01 NRZ/NRZI
10 Biphase-Mark/Space
11 Biphase-Level
D2..D3 DPLL Clock Rate (encoded as follows):
00 32x Clock Mode
01 16x Clock Mode
10 8x Clock Mode
11 Reserved
D4 RW Accept Code Violations
D5 RW CTR1 Rate Match DPLL/CTR0
D6..7 CTR0 Clock Rate (encoded as follows):
00 32x Clock Mode
01 16x Clock Mode
10 8x Clock Mode
11 4x Clock Mode

2.3.11 INTERRUPT VECTOR REGISTER (IVR)

2.3.11.1 Low: (LOC 0xn14)

D1..3 RW IV 7..0

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2.3.11.2 High: (LOC 0xn2A)

D4..7	RO	Modified Vector (encoded as follows):
	000	None
	001	Device Status
	010	I/O Status
	011	Transmit Data
	100	Transmit Status
	101	Receive Data
	110	Receive Status
	111	Not Used
D12..15	RO	IV 7..4

2.3.12 I/O CONTROL REGISTER (IOCR)

2.3.12.1 Low: (LOC 0xn16)

D0..2	RxC Pin Control (encoded as follows):	
	000	Input Pin
	001	Rx Clock Output
	010	Rx Byte Clock Output
	011	SYNC Output
	100	BRG0 Output
	101	BRG1 Output
	110	CTR0 Output
	111	DPLL Rx Output
D3..D5	TxC Pin Control (encoded as follows):	
	000	Input Pin
	001	Tx Clock Output
	010	Tx Byte Clock Output
	011	Tx Complete Output
	100	BRG0 Output
	101	BRG1 Output
	110	CTR1 Output
	111	DPLL Tx Output
D6..7	TxD Pin Control (encoded as follows):	
	00	Tx Data Output
	01	3-State Output
	10	Output 0
	11	Output 1

2.3.12.2 High: (LOC 0xn17)

D0..D1	RxREQ Pin Control (encoded as follows):	
	00	Input pin
	01	Rx DMA Request Output
	10	Output 0
	11	Output 1
D2..D3	TxREQ Pin Control (encoded as follows):	
	00	Input pin

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	01	Tx DMA Request Output
	10	Output 0
	11	Output 1
D4..5	DCD Pin Control (encoded as follows):	
	00	/DCD Input
	01	/DCD//SYNC Input
	10	Output 0
	11	Output 1
D6..7	CTS Pin Control (encoded as follows):	
	00	/CTS Input
	01	/CTS Input
	10	Output 0
	11	Output 1

2.3.13 INTERRUPT CONTROL REGISTER (ICR)

2.3.13.1 Low: (LOC 0xn18)

D0	RW	Device Status IE
D1	RW	I/O Status IE
D2	RW	Transmit Data IE
D3	RW	Transmit Status IE
D4	RW	Receive Data IE
D5	RW	Receive Status IE
D6..7	IE Command (encoded as follows):	
	00	Null Command
	01	Null Command
	10	Reset IE
	11	Set IE

2.3.13.2 High: (LOC 0xn19)

D0	RW	Reserved
D1..3		VIS Level (encoded as follows):
	000	All
	001	All
	010	I/O Status and Above
	011	Transmit Data and Above
	100	Transmit Status and Above
	101	Receive Data and Above
	110	Receive Status Only
	111	None
D4	RW	MIE
D5	RW	DLC
D6	RW	NV
D7	RW	VIS

2.3.14 DAISY-CHAIN CONTROL REGISTER (DCCR)

2.3.14.1 Low: (LOC: 0xn1A)

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D0	RW	Device Status INTERRUPT PENDING
D1	RW	I/O Status INTERRUPT PENDING
D2	RW	Transmit Data INTERRUPT PENDING
D3	RW	Transmit Status INTERRUPT PENDING
D4	RW	Receive Data INTERRUPT PENDING
D5	RW	Receive Status INTERRUPT PENDING
D6..7	INTERRUPT PENDING Command (encoded as follows):	
	00	Null Command
	01	Reset INTERRUPT PENDING and IUS
	10	Reset INTERRUPT PENDING
	11	Set INTERRUPT PENDING

2.3.14.2 High RW: (LOC 0xn1B)

D0	RW	Device Status IUS
D1	RW	I/O Status IUS
D2	RW	Transmit Data IUS
D3	RW	Transmit Status IUS
D4	RW	Receive Data IUS
D5	RW	Receive Status IUS
D6..7	IUS Command (encoded as follows):	
	00	Null Command
	01	Null Command
	10	Reset IUS
	11	Set IUS

2.3.15 MISCELLANEOUS INTERRUPT STATUS REGISTER (MISR)

2.3.15.1 Low: (LOC 0xn1C)

D0	RW	BRG0 ZC Latched/Unlatch
D1	RW	BRG1 ZC Latched/Unlatch
D2	RW	DPLL SYNC Latched/Unlatch
D3	RW	RCC Overflow Latched/Unlatch
D4	RO	/CTS
D5	RW	/CTS Latched/Unlatch
D6	RO	/DCD
D7	RW	/DCD Latched/Unlatch

2.3.15.2 High: (LOC 0xn1D)

D0	RO	TxREQ
D1	RW	/TxREQ Latched/Unlatch
D2	RO	/RxREQ
D3	RW	/RxREQ Latched/Unlatch
D4	RO	/TxC
D5	RW	/TxC Latched/Unlatch
D6	RO	/RxC
D7	RW	/RxC Latched/Unlatch

2.3.16 STATUS INTERRUPT CONTROL REGISTER (SICR)

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2.3.16.1 Low: (LOC 0xn1E)

D0	RW	BRG0 ZC INTERRUPT ENABLE
D1	RW	BRG1 ZC INTERRUPT ENABLE
D2	RW	DPLL SYNC INTERRUPT ENABLE
D3	RW	RCC Overflow INTERRUPT ENABLE
D4..5	RW	/CTS Interrupts (encoded as follows, D4 being the LSB):
	00	Disabled
	01	Rising Edge Only
	10	Falling Edge Only
	11	Both Edges
D6..7	RW	/DCD Interrupts (encoded as follows, D6 being the LSB):
	00	Disabled
	01	Rising Edge Only
	10	Falling Edge Only
	11	Both Edges

2.3.16.2 High: (LOC 0xn1F)

D0..1	RW	/TxREQ Interrupts (encoded as follows):
	00	Disabled
	01	Rising Edge Only
	10	Falling Edge Only
	11	Both Edges
D3..2	RW	/RxREQ Interrupts (encoded as follows):
	00	Disabled
	01	Rising Edge Only
	10	Falling Edge Only
	11	Both Edges
D4..5	RW	TxC Interrupts (encoded as follows, D12 being the LSB):
	00	Disabled
	01	Rising Edge Only
	10	Falling Edge Only
	11	Both Edges
D6..7	RW	RxC Interrupts (encoded as follows, D14 being the LSB):
	00	Disabled
	01	Rising Edge Only
	10	Falling Edge Only
	11	Both Edges

2.3.17 TX/RX DATA REGISTER (RDR/TDR)

2.3.17.1 Low: (LOC 0xn20)

D0..7	RW	Tx/Rx D7..0

2.3.17.2 High: (LOC 0xn21)

D0..7	RW	Tx/Rx D7..0

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2.3.18 RECEIVER MODE REGISTER (RMR)

2.3.18.1 Low: (LOC 0xn22)

D0..1 Rx Enable (encoded as follows):
- 00 Disable Immediately
- 01 Disable After Reception
- 10 Enable Without Auto-Enables
- 11 Enable With Auto-Enables

D2..4 Rx Character Length (encoded as follows):
- 000 8 Bits
- 001 1 Bits
- 010 2 Bits
- 011 3 Bits
- 100 4 Bits
- 101 5 Bits
- 110 6 Bits
- 111 7 Bits

D5 RW Rx Parity Enable

D6..7 Rx Parity Sense (encoded as follows):
- 00 Even
- 01 Odd
- 10 Space
- 11 Mark

2.3.18.2 High: (LOC 0xn23)

D0 RW Queue Abort

D1 RW Rx CRC Enable

D2 RW Rx CRC Preset Value

D3..4 Rx CRC Polynomial (encoded as follows):
- 00 CRC-CCITT
- 01 CRC-16
- 10 CRC-32
- 11 Reserved

D5..7 Rx Data Decoding (encoded as follows):
- 000 NRZ
- 001 NRZB
- 010 NRZI-Mark
- 011 NRZI-Space
- 100 Biphase-Mark
- 101 Biphase-Space
- 110 Biphase-Level
- 111 Diff. Biphase-Level

2.3.19 RECEIVE COMMAND STATUS REGISTER (RCSR)

2.3.19.1 Low: (LOC 0xn24)

D0 RO Rx Character Available

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D1	RW	Rx Overrun
D2	RW	Parity Error/Frame Abort
D3	RO	CRC/Framing Error
D4	RW	Rx CV/EOT/EOF
D5	RW	Rx Break Abort
D6	RW	Rx Idle
D7	RW	Exited Hunt

2.3.19.2 High: (LOC 0xn25)

D0	RO	Short Frame/CV Polarity
D1	RO	Residue Code 0
D2	RO	Residue code 1
D3	RO	Residue Code 2
D4..7	WO	Receive Command (encoded as follows, D12 being the LSB):
	0000	Null command
	0001	Reserved
	0010	Preset CRC
	0011	Enter Hunt Mode
	0100	Reserved
	0101	Select FIFO Status
	0110	Select FIFO Interrupt Level
	0111	Select FIFO Request Level
	1000	Reserved
	1001	Reserved
	1010	Reserved
	1011	Reserved
	1100	Reserved
	1101	Reserved
	1110	Reserved
	1111	Reserved
D6	RO	First Byte in Error
D7	RO	Second Byte in Error

2.3.20 RECEIVE INTERRUPT CONTROL REGISTER (RICR)

2.3.20.1 Low: (LOC 0xn26)

D0	RW	TC0R Read Count/TC
D1	RW	Rx Overrun INTERRUPT ARMED
D2	RW	Parity Error/Frame Abort INTERRUPT ARMED
D3	RW	Status on Words
D4	RW	Rx CV/EOT/EOF INTERRUPT ARMED
D5	RW	Rx Break/Abort INTERRUPT ARMED
D6	RW	Rx Idle INTERRUPT ARMED
D7	RW	Exited Hunt INTERRUPT ARMED

2.3.20.2 High: (LOC 0xn27)

D0..7	RW	Rx FIFO Control and Status (Fill/Interrupt/DMA Level)

2.3.21 RECEIVE SYNC REGISTER (RSR)

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2.3.21.1 Low: (LOC 0xn28)

D0..7 RW RSYN 0..7

2.3.21.2 High: (LOC 0xn29)

D0..7 RW RSYN 15..8

2.3.22 RECEIVE COUNT LIMIT REGISTER (RCLR)

2.3.22.1 Low: (LOC 0xn2A)

D0..7 RW RCL 7..0

2.3.22.2 High: (LOC 0xn2B)

D0..7 RW RCL 15..8

2.3.23 RECEIVE CHARACTER COUNT REGISTER (RCCR)

2.3.23.1 Low: (LOC 0xn2C)

D0..7 RO RCC 7..0

2.3.23.2 High: (LOC 0xn2D)

D0..7 RO RCC 15..8

2.3.24 TIME CONSTANT 0 REGISTER (TC0R)

2.3.24.1 Low: (LOC 0xn2E)

D0..7 RW TC0 7..0

2.3.24.2 High: (LOC 0xn2F)

D0..7 RW TC0 15..8

2.3.25 TRANSMIT MODE REGISTER (TMR)

2.3.25.1 Low: (LOC 0xn32)

D0..1 Tx Enable (encoded as follows, D0 being the LSB):
- 00 Disable Immediately
- 01 Disable After Transmission
- 10 Enable Without Auto-Enables
- 11 Enable With Auto-Enables

D2..4 Tx Character Length (encoded as follows):
- 000 8 Bits

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001 1 Bit
010 2 Bits
011 3 Bits
100 4 Bits
101 5 Bits
110 6 Bits
111 7 Bits

D5 RW Tx Parity Enable

D6..7 Tx Parity Sense (encoded as follows):
00 Even
01 Odd
10 Space
11 Mark

2.3.25.2 High: (LOC 0xn33)

D0 RW Tx CRC EOF/EOM

D1 RW Tx CRC Enable

D2 RW Tx CRC on Preset Value

D3..4 Polynomial Tx CRC (encoded as follows):
00 CRC-CCITT
01 CRC-16
10 CRC-32
11 Reserved

D5..7 Tx Data Encoding (encoded as follows):
000 NRZ
001 NRZB
010 NRZI-Mark
011 NRZI-Space
100 Biphase-Mark
101 Biphase-Space
110 Biphase-Level
111 Diff. Biphase-Level

2.3.26 TRANSMIT COMMAND/STATUS REGISTER (TCSR)

2.3.26.1 Low: (LOC 0xn34)

D0 RO Tx Buffer Empty

D1 RW Tx Underrun

D2 RO All Sent

D3 RW Tx CRC Sent

D4 RW Tx EOF/EOT Sent

D5 RW Tx Abort Sent

D6 RW Tx Idle Sent

D7 RW Tx Preamble Sent

2.3.26.2 High: (LOC 0xn35)

D0..2 Tx Idle Line Condition
000 SYNC/Flag/Normal
001 Alternating 1 & 0

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	010	All Zeros
	011	All Ones
	100	Reserved
	101	Alternating Mark & Space
	110	Space
	111	Mark
D3	RW	TxWait on Underrun
D4..7	WO	Transmit Command
	0000	Null Command
	0001	Reserved
	0010	Preset CRC
	0011	Reserved
	0100	Reserved
	0101	Select FIFO Status
	1110	Select FIFO Interrupt Level
	0111	Select FIFO Request Level
	1000	Send Frame/Message
	1001	Send Abort
	1010	Reserved
	1011	Reserved
	1100	Reset DLE Inhibit
	1101	Set DLE Inhibit
	1110	Reset EOF/EOM
	1111	Set EOF/EOM

2.3.27 TRANSMIT INTERRUPT CONTROL REGISTER (TICR)

2.3.27.1 Low: (LOC 0xn36)

D0	RW	TC1R Read Count/TC
D1	RW	Tx Overrun INTERRUPT ARMED
D2	RW	Wait for Send Command
D3	RW	Tx CRC Sent INTERRUPT ARMED
D4	RW	Tx EOF/EOT Sent INTERRUPT ARMED
D5	RW	Tx Abort Sent INTERRUPT ARMED
D6	RW	Tx Idle Sent INTERRUPT ARMED
D7	RW	Tx Preamble Sent INTERRUPT ARMED

2.3.27.2 High: (LOC 0xn37)

D0..7	RW	Tx FIFO Control and Status (Fill/Interrupt/DMA Level)

2.3.28 TRANSMIT SYNC REGISTER (TSR)

2.3.28.1 Low: (LOC 0xn38)

D0..7	RW	TSYN 7..0

2.3.28.2 High: (LOC 0xn39)

D0..7	RW	TSYN 15..8

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2.3.29 TRANSMIT COUNT LIMIT REGISTER (TCLR)

2.3.29.1 Low: (LOC 0xn3A)

D0..7 RW TCL 7..0

2.3.29.2 High: (LOC 0xn3B)

D0..7 RW TCL 15..8

2.3.30 TRANSMIT CHARACTER COUNT REGISTER (TCCR)

2.3.30.1 Low: (LOC 0xn3C)

D0..7 RO TCC 7..0

2.3.30.2 High: (LOC 0xn3D)

D0..7 RO TCC 15..8

2.3.31 TIME CONSTANT 1 REGISTER (TC1R)

2.3.31.1 Low: (LOC 0xn3E)

D0..7 RW TC1 7..0

2.3.31.2 High: (LOC 0xn3F)

D7..0 RW TC1 15..8

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CHAPTER 3: PCI INTERFACE

3.0 PCI INTERFACE REGISTERS

A PCI9080 I/O Accelerator from PLX Technology handles the PCI Interface. The PCI interface is compliant with the 5V, 33MHz PCI Specification 2.1. The PCI9080 provides dual DMA controllers for fast data transfers to and from the on-board FIFOs. Fast DMA burst accesses provide for a maximum burst throughput of 132MB/s to the PCI interface. To reduce CPU overhead during DMA transfers, the controller also implements Chained (Scatter/Gather) DMA, as well as Demand Mode DMA.

Since many features of the PCI9080 are not utilized in this design, it is beyond the scope of this document to duplicate the PCI9080 User's Manual. Only those features, which will clarify areas specific to the PCI/PMC-HPDI32, are detailed here. Please refer to the PCI9080 User's Manual (See Related Publications) for more detailed information. Note that the BIOS configuration and software driver will handle most of the PCI9080 interface. Unless the user is writing a device driver, the details of the PCI interface (Chapter 2) may be skipped.

3.1 PCI CONFIGURATION REGISTERS

The PCI device configuration for the PCI/PMC-HPDI32 is fully PCI 2.1 compliant. Table 3.1-1 contains a list of the PCI configuration registers present in the PCI9080. An on-board configuration serial EEPROM initializes many of these registers.

Table 3.1-1: PCI Configuration Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x00	0x00	Local	Device ID/Vendor ID	0x908010B5
0x04	0x04	Y	Status/Command	0x02800017
0x08	0x08	Local	Class Code/Revision ID	0x0680003
0x0C	0x0C	Y[15:0], Local	BIST (Unused)/Header Type/Latency Timer/Cache Line Size	0x00002008
0x10	0x10	Y	PCI Base Addr 0 for Memory Mapped Local/Runtime/DMA Registers (PCIBAR0)	0x00000000
0x14	0x14	Y	PCI Base Addr 1 for I/O Mapped Local/Runtime/DMA Registers (PCIBAR1)	0x00000001
0x18	0x18	Y	PCI Base Addr 2 for Local Addr Space 0 (PCIBAR2)	0x00000000
0x1C	0x1C	Y	PCI Base Addr 3 for Local Addr Space 1 (PCIBAR3) (Unused)	0x00000000
0x2C	0x2C	Local	Subsystem ID/Subsystem Vendor ID	0x90802400
0x30	0x30	Y	PCI Base Address to Local Expansion ROM (Unused)	0x00000000
0x3C	0x3C	Y[7:0], Local	Max_Lat/Min_Gnt/Interrupt Pin/Interrupt Line	0x00000100

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Note: The Local Base Address for the PCI Configuration registers in Local Address Space is 0xC0000000. However, there should be no need for the user to access the PCI Configuration registers through Local Address Space.

3.1.1 PCI CONFIGURATION ID REGISTER: (OFFSET 0X00, RESET 0X908010B5)

D15:0 VENDOR ID –– 0X10B5 = PLX TECHNOLOGY
D31:16 DEVICE ID –– 0X9080 = PCI9080

3.1.2 PCI

D0 I/O SPACE
A '1' allows the device to respond to I/O space accesses.
D1 Memory Space
A '1' allows the device to respond to memory space accesses.
D2 PCI Master Enable.
A '1' allows the device to behave as a PCI bus master.
Note: This bit must be set for the PCI 9080 to perform DMA cycles.
D3 Special Cycle. (*Not Supported*.)
D4 Memory Write/Invalidate.
A '1' enables memory write/invalidate.
D5 VGA Palette Snoop. (*Not Supported*.)
D6 Parity Error Response
A '0' indicates that a parity error is ignored and operation continues.
A '1' indicates that parity checking is enabled.
D7 Wait Cycle Control. Controls whether the device does address/data stepping.
A '0' indicates the device never does address/data stepping.
Note: Hardcoded to 0.
D8 SERR# Enable
A '1' allows the device to drive the SERR# line.
D9 Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus.
A '1' indicates fast back-to-back transfers can occur to any agent on the bus.
A '0' indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.
D15:10 Reserved

3.1.3 PCI STATUS REGISTER: (OFFSET 0X06, RESET 0X0280)

D5:0 Reserved
D6 User Definable Features Supported
A '1' indicates UDF are supported.
Note: User Definable Features are Not Implemented.
D7 Fast Back-to-Back Capable.
A '1' indicates the adapter can accept fast back-to-back transactions.
D8 Master Data Parity Error Detected
A '1 indicates the following three conditions are met:
1. PCI9080 asserted PERR# itself or observed PERR# asserted.
2. PCI9080 was bus master for the operation in which the error occurred.
3. Parity Error Response bit in the Command Register is set.

Writing a '1' to this bit clears the bit.
D10:9 DEVSEL Timing. Indicates timing for DEVSEL# assertion.
A value of '01' indicates a medium decode.

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Note: Hardcode to 01.

D11 Target Abort
A '1' indicates the PCI9080 has signaled a target abort.
Writing a '1' to this bit clears the bit.

D12 Received Target Abort
A '1' indicates the PCI9080 has received a target abort.
Writing a '1' to this bit clears the bit.

D13 Master Abort
A '1' indicates the PCI9080 has generated a master abort signal.
Writing a '1' to this bit clears the bit.

D14 Signal System Error
A '1' indicates the PCI9080 has reported a system error on the SERR# signal.
Writing a '1' to this bit clears the bit.

D15 Detected Parity Error
A '1' indicates the PCI9080 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear).
One of three conditions can cause this bit to be set:

1. PCI9080 detected a parity error during a PCI address phase.
2. PCI9080 detected a data parity error when it was the target of a write.
3. PCI9080 detected a data parity error when performing a master read.

Writing a '1' to this bit clears the bit.

3.1.4 PCI REVISION ID REGISTER : (OFFSET 0X08)

D7:0 Revision ID - The silicon revision of the PCI9080.

3.1.5 PCI CLASS CODE REGISTER: (OFFSET 0X09-0B, RESET=0X068000)

D7:0 Register level programming interface
0x00 = Queue Ports at 0x40 and 0x44.
0x01 = Queue Ports at 0x40 and 0x44, Int Status and Int Mask at 0x30 and 0x34

D15:8 Sub-class Code - 0x80 = Other bridge device.

D23:16 Base Class Code. - 0x06 = Bridge Device

3.1.6 PCI CACHE LINE SIZE REGISTER: (OFFSET 0X0C, RESET 0X00)

D7:0 System cache line size in units of 32-bit words.

3.1.7 PCI LATENCY TIMER REGISTER : (OFFSET 0X0D, RESET 0X00)

D7:0 PCI Latency Timer. Units of PCI bus clocks, the amount of time the PCI9080, as a bus master, can burst data on the PCI bus.

3.1.8 PCI HEADER TYPE REGISTER: (OFFSET 0X0E, RESET 0X00)

D6:0 Configuration Layout Type = 0

D7 Header Type = 0.

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3.1.9 PCI BASE ADDRESS REGISTER FOR MEMORY ACCESS TO LOCAL/RUNTIME/DMA REGISTERS :

(OFFSET 0X010, RESET 0X00000000)

D0	Memory Space Indicator A '0' indicates register maps into Memory space. **Note: Hardcoded to 0.**
D2:1	Location of Register: 00 - Locate anywhere in 32-bit memory address space **Note: Hardcoded to 0.**
D3	Prefetchable. **Note: Hardcoded to 0.**
D7:4	Memory Base Address. Default Size = 256 bytes. **Note: Hardcoded to 0.**
D31:8	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers.

Note: PCIBAR0 is Memory Mapped Base Address of PCI9080 Registers.

3.1.10 PCI BASE ADDRESS REGISTER FOR I/O ACCESS TO LOCAL/RUNTIME/DMA REGISTERS : (OFFSET 0X14, RESET 0X00000001)

D0	Memory Space Indicator A '1' indicates the register maps into I/O space. **Note: Hardcoded to 1.**
D1	Reserved
D7:2	I/O Base Address. Default Size = 256 bytes. **Note: Hardcoded to 0.**
D31:8	I/O Base Address. Base Address for I/O access to Local, Runtime, and DMA Registers.

Note: PCIBAR1 is I/O Mapped Base Address of PCI9080 Registers.

3.1.11 PCI BASE ADDRESS REGISTER FOR MEMORY ACCESS TO LOCAL ADDRESS SPACE 0: (OFFSET 0X18, RESET 0X00000000)

D0	Memory Space Indicator A '0' indicates register maps into Memory space. (Specified in Local Address Space 0 Range Register - LAS0RR.)
D2:1	Location of register (if memory space). Location values: 00 - Locate anywhere in 32-bit memory address space (Specified in Local Address Space 0 Range Register - LAS0RR.)
D3	Prefetchable A '0' indicates reads are not prefetchable. (Specified in Local Address Space 0 Range Register - LAS0RR
D31:4	Memory Base Address Memory base address for access to Local Address Space 0.

3.1.12 PCI SUBSYSTEM DEVICE/VENDOR ID REGISTER: (OFFSET 0X2C, RESET 0X908010B5)

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D15:0 Subsystem Vendor ID – 0x10B5 = PLX Technology
D31:16 Subsystem Device ID – 0x2400 = General Standards Corporation HPDI32).

3.1.13 PCI INTERRUPT LINE REGISTER: (OFFSET 0X3C, RESET 0X00)

D7:0 Interrupt Line Routing Value
Indicates which input of the system interrupt controller(s) to which the interrupt line of the device is connected.

3.1.14 PCI INTERRUPT PIN REGISTER : (OFFSET 0X3D, RESET 0X01)

D7:0 Interrupt Pin register. Indicates which interrupt pin the device uses.
01=INTA#

Note: PCI 9080 supports only one PCI interrupt pin (INTA#).

3.1.15 PCI MIN_GNT REGISTER : (OFFSET 0X3E, RESET 0X00)

D7:0 Minimum Grant
Specifies the minimum burst period the device needs assuming a clock rate of 33 MHz. Value is in 250 nsec increments. A '0' indicates no stringent requirement.

3.1.16 PCI MAX_LAT REGISTER : (OFFSET 0X3F, RESET 0X00)

D7:0 Maximum Latency
Specifies the maximum burst period the device needs assuming a clock rate of 33 MHz. Value is in 250 nsec increments. A '0' indicates no stringent requirement.

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3.2 LOCAL CONFIGURATION REGISTERS

The Local Configuration registers give information on the Local side implementation. Since Local Expansion ROM, Local Address Space 1, and Direct Master accesses are not implemented on the PCI/PMC-HPDI32, the descriptions of these registers have been omitted. Most of the Local Configuration Registers are preloaded from the configuration Serial EEPROM at system reset.

Table 3.2-1: Local Configuration Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x00	0x80	Y	Range for PCI to Local Address Space 0	0xFFFFF000
0x04	0x84	Y	Local Base Address (Remap) for PCI to Local Address Space 0 (Unused)	0x00000000
0x08	0x88	Y	Mode/Arbitration Register	0x00000000
0x0C	0x8C	Y	Big/Little Endian Descriptor	0x00000000
0x10	0x90	Y	Range for PCI to Local Expansion ROM (Unused)	0x00000000
0x14	0x94	Y	Local Base Address (Re-map) for PCI to Local Expansion ROM and BREQo control (Unused)	0x00000000
0x18	0x98	Y	Local Bus Region Descriptions for PCI Local Accesses	0x00000000
0x1C	0x9C	Y	Range for Direct Master to PCI (Unused)	0x00000000
0x20	0xA0	Y	Local Base Address for Direct Master to PCI Memory (Unused)	0x00000000
0x24	0xA4	Y	Local Base Address for Direct Master to PCI Memory IO/CFG (Unused)	0x00000000
0x28	0xA8	Y	PCI Base Address (Re-map) for Direct Master to PCI (Unused)	0x00000000
0x2C	0xAC	Y	PCI Configuration Address Register for Direct Master to PCI IO/CFG (Unused)	0x00000000
0xF0	0x170	Y	Range for PCI to Local Address Space 1 (Unused)	0x00000000
0xF4	0x174	Y	Local Base Address (Remap) for PCI to Local Address Space 1 (Unused)	0x00000000
0xF8	0x178	Y	Local Bus Region Descriptor (Space 1) for PCI to Local Accesses (Unused)	0x00000000

3.2.1 LOCAL ADDRESS SPACE 0 RANGE REGISTER FOR PCI TO LOCAL BUS : (PCI 0X00, RESET 0XFFFFF000)

D0 Memory Space Indicator
A '0' indicates register maps into Memory space.

D2:1 Location of register (if memory space). Location values:
00 - Locate anywhere in 32-bit memory address space

D3 Prefetchable
A '0' indicates reads are not prefetchable.

D31:4 Specifies which PCI address bits will be used to decode a PCI access to Local Address Space 0. A '1' indicates bit is included in address decode.

Local Address Space 0 value 0xFFFFF000 maps a 4kbyte range.
Since entire Local Address Space can be mapped into 4kb range, the remap register is not used.

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3.2.2 MODE/ARBITRATION REGISTER : (PCI 0X08)

D7:0	Local bus Latency Timer (Unused)
D8:15	Local bus Pause Timer (Unused)
D16	Local bus Latency Timer Enable (Unused)
D17	Local bus Pause Timer Enable (Unused)
D18	Local bus BREQ Enable (Unused)
D20:19	DMA Channel Priority 00 = Rotational priority 01 = Channel 2 priority 10 = Channel 1 priority 11 = Reserved
D21	Local bus direct slave give up bus mode A value of 1 indicates local bus will be released when PCI9080 write FIFO empty or read FIFO full.
D22	Direct slave LLOCKo# Enable (Unused)
D23	PCI Request Mode
D24	PCI Rev 2.1 Mode
D25	PCI Read No Write Mode
D26	PCI Read with Write Flush Mode
D27	Gate the Local Bus Latency Timer with BREQ (Unused)
D28	PCI Read No Flush Mode
D29	Reads Device/Vendor ID or SubDevice/SubVendor ID
D31:30	Reserved

3.2.3 BIG/LITTLE ENDIAN DESCRIPTOR REGISTER : (PCI 0X0C)

Since local bus is little endian, all bits should be left zero.

3.2.4 LOCAL ADDRESS SPACE 0/EXPANSION ROM BUS REGION DESCRIPTOR REGISTER (PCI 0X18, RESET 0X40030143)

D1:0	Memory Space 0 Local Bus Width 11 indicates 32-bit local bus
D5:2	Memory Space 0 Internal Wait States A '0' indicates no wait states required
D6	Memory Space 0 Ready Input Enable A '1' indicates Local Ready input enabled.
D7	Memory Space 0 Bterm Input Enable (Unused)
D8	Memory Space 0 Prefetch Disable (Unused)
D9	Expansion ROM Space Prefetch Disable (Unused)
D10	Read Prefetch Count Enable (Unused)
D14:11	Prefetch Counter (Unused)
D15	Reserved
D17:16	Expansion ROM Space Local Bus Width (Unused)
D21:18	Expansion ROM Space Internal Wait States (Unused)
D22	Expansion ROM Space Ready Input Enable (Unused)
D23	Expansion ROM Space Bterm Input Enable (Unused)
D24	Memory Space 0 Burst Enable
D25	Extra Long Load from Serial Enable
D26	Expansion ROM Space Burst Enable (Unused)

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D27 Direct Slave PCI Write Mode
D28:31 PCI Target Retry Delay Clocks

3.3 RUNTIME REGISTERS

The Runtime registers consist of mailbox registers, doorbell registers, and a general-purpose control register. The mailbox and doorbell registers serve no purpose on the PCI/PMC-HPDI32.

Table 3.3-1: Runtime Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x40	0xC0	Y	Mailbox Register 0 (Unused)	0x00000000
0x44	0xC4	Y	Mailbox Register 1 (Unused)	0x00000000
0x48	0xC8	Y	Mailbox Register 2 (Unused)	0x00000000
0x4C	0xCC	Y	Mailbox Register 3 (Unused)	0x00000000
0x50	0xD0	Y	Mailbox Register 4 (Unused)	0x00000000
0x54	0xD4	Y	Mailbox Register 5 (Unused)	0x00000000
0x58	0xD8	Y	Mailbox Register 6 (Unused)	0x00000000
0x5C	0xDC	Y	Mailbox Register 7 (Unused)	0x00000000
0x60	0xE0	Y	PCI to Local Doorbell Register (Unused)	0x00000000
0x64	0xE4	Y	Local to PCI Doorbell Register (Unused)	0x00000000
0x68	0xE8	Y	Interrupt Control/Status	0x00000000
0x6C	0xEC	Y	General Purpose Control	0x00000000
0x70	0xF0	N	Permanent Device ID/ Permanent Vendor ID	0x10B59080
0x74	0xF4	N	Permanent Revision ID	0x0000000X
0x78	0xC0	Y	Mailbox Register 0 (Unused)	0x00000000
0x7C	0xC4	Y	Mailbox Register 1 (Unused)	0x00000000

3.3.1 INTERRUPT CONTROL /STATUS : (PCI 0X68, RESET 0X00000000)

D0 Enable Local bus LSERR# (Unused)
D1 Enable Local bus LSERR# on a PCI parity error (Unused)
D2 Generate PCI Bus SERR#
D3 Mailbox Interrupt Enable (Unused)
D7:4 Reserved
D8 PCI Interrupt Enable
D9 PCI Doorbell Interrupt Enable (Unused)
D10 PCI Abort Interrupt Enable
D11 PCI Local Interrupt Enable
Local Interrupt must be enabled for USC/FIFO interrupts.
D12 Retry Abort Enable (Unused)
D13 PCI Doorbell Interrupt Status.
D14 PCI Abort Interrupt Status
D15 PCI Local Interrupt Status
D16 Local Interrupt Output Enable
D17 Local Doorbell Interrupt Enable (Unused)

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D18 Local DMA Channel 0 Interrupt Enable
D19 Local DMA Channel 1 Interrupt Enable
D20 Local Doorbell Interrupt Status
D21 DMA Channel 0 Interrupt Status
D22 DMA Channel 1 Interrupt Status
D23 BIST Interrupt Status
D24 A '0' indicates a Direct Master was bus master during a Master or Target abort.
D25 A '0' indicates that DMA CH0 was bus master during a Master or Target abort.
D26 A '0' indicates that DMA CH1 was bus master during a Master or Target abort.
D27 A '0' indicates that a Target Abort was generated by the PCI9080 after 256 consecutive Master retries to a Target.
D31:28 PCI Mailbox 3:0 Write Status

3.3.2 SERIAL EEPROM CONTROL, PCI COMMAND CODES, USER I/O CONTROL, INIT CONTROL REGISTER: (PCI 0X6C, RESET 0X0X001767E)

D3:0 PCI Read Command Code for DMA
D7:4 PCI Write Command Code for DMA
D11:8 PCI Memory Read Command Code for Direct Master (Unused)
D15:12 PCI Memory Write Command Code for Direct Master (Unused)
D16 General Purpose Output (Unused)
D17 General Purpose Input (Unused)
D23:18 Reserved
D24 Serial EEPROM clock for Local or PCI bus reads or writes to Serial EEPROM.
D25 Serial EEPROM chip select
D26 Write bit to serial EEPROM
D27 Read serial EEPROM data bit
D28 Serial EEPROM present
D29 Reload Configuration Registers
D30 PCI Adapter Software Reset
D31 Local Init Status
A '1' indicates Local initialization done.

3.3.3 PCI PERMANENT CONFIGURATION ID REGISTER : (PCI 0X70, RESET 0X10B59080)

D15:0 Permanent Vendor ID (0x10B5)
D31:16 Permanent Device ID (0x9080)

3.3.4 PCI PERMANENT REVISION ID REGISTER: (PCI 0X74)

D7:0 Permanent Revision ID

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3.4 LOCAL DMA REGISTERS

The Local DMA registers are used to setup the DMA transfers to and from the on-board FIFOs. Since the PCI/PMC-HPDI32 is half-duplex (data is only transferred in one direction at a time), only DMA Channel 0 is used.

Table 3.4-1: DMA Registers

PCI CFG Addr	Local Offset Addr	PCI/Local Writable	Register Name	Value after Reset
0x80	0x100	Y	DMA Channel 0 Mode Register	0x00000003
0x84	0x104	Y	DMA Channel 0 PCI Address Register	0x00000000
0x88	0x108	Y	DMA Channel 0 Local Address Register	0x00000000
0x8C	0x10C	Y	DMA Channel 0 Transfer Byte Count Register	0x00000000
0x90	0x110	Y	DMA Channel 0 Descriptor Pointer Register	0x00000000
0x94	0x114	Y	DMA Channel 1 Mode Register (Unused)	0x00000003
0x98	0x118	Y	DMA Channel 1 PCI Address Register (Unused)	0x00000000
0x9C	0x11C	Y	DMA Channel 1 Local Address Register (Unused)	0x00000000
0xA0	0x120	Y	DMA Channel 1 Transfer Byte Count Register (Unused)	0x00000000
0xA4	0x124	Y	DMA Channel 1 Descriptor Pointer Register (Unused)	0x00000000
0xA8	0x128	Y	DMA Channel 1Command/Status Register DMA Channel 0 Command/Status Register	0x00000010
0xAC	0x12C	Y	DMA Mode/ Arbitration Register	0x00000000
0xB0	0x130	Y	DMA Threshold Register	0x00000000

3.4.1 DMA CHANNEL 0 MODE REGISTER : (PCI 0X80)

D1:0 Local Bus Width
00 = 8 bit DMA transfer width
01 = 16 bit DMA transfer width
10/11 = 32 bit DMA transfer width

D5:2 Internal Wait States (Unused)

D6 Ready Input Enable
Note: This bit should always be set to '1' (Ready Input Enabled).

D7 Bterm# Input Enable (Unused)
Note: This bit should always be set to '0' (BTERM# Disabled).

D8 Local Burst Enable
Note: If Burst enabled, the user must ensure FIFO will not become empty (read) or full (write) during the burst access. For Demand Mode DMA, this means the Almost Empty/Almost Full flags should be set to a value of at least 8.

D9 Chaining Enable
A '1' indicates chaining mode is enabled.
For chaining mode, the DMA source address, destination address and byte count are loaded from memory in PCI Space.

D10 Done Interrupt Enable
A '1' enables interrupt when DMA done.
Note: If DMA clear count mode is enabled, the interrupt won't occur until the byte count is cleared.

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D11 Local Addressing Mode
A '1' indicates local addresses LA [31:2] to be held constant.
Note: This bit should always be set to '1' (no address increment).

D12 Demand Mode Enable
A '1' causes the DMA controller to operate in Demand Mode.
In Demand Mode, the DMA controller transfers data when its DREQ# input is asserted. The DMA controller transfers Lwords (32bits) of data. This may result in multiple transfers for an 8 or 16 bit bus.

D13 Write and Invalidate Mode for DMA Transfers
When set to 1, PCI 9080 performs Write and Invalidate cycles to the PCI bus. PCI 9080 supports Write and Invalidate sizes of 8 or 16 Lwords. The size is specified in the PCI Cache Line Size Register. If a size other than 8 or 16 is specified, PCI 9080 performs write transfers rather than Write and Invalidate transfers. Transfers must start and end at the Cache Line Boundaries.

D14 DMA EOT (End of Transfer) Enable (Unused)

D15 DMA Stop Data Transfer Mode
A'0' sends a BLAST to terminate DMA transfer
Note: This bit should always be set to '0'.

D16 DMA Clear Count Mode (Unused)

D17 DMA Channel 0 Interrupt Select
A '1' routes the DMA Channel 0 interrupt to the PCI interrupt.
Note: This bit should always be set to '1'.

D31:18 Reserved

3.4.2 DMA CHANNEL 0 PCI ADDRESS REGISTER : (PCI 0X84)

D31:0 PCI Address Register

3.4.3 DMA CHANNEL 0 LOCAL ADDRESS REGISTER : (PCI 0X88)

D31:0 Local Address Register
Note: Should be set to Local FIFO offset 0x18.

3.4.4 DMA CHANNEL 0 TRANSFER SIZE (BYTES) REGISTER: (PCI 0X8C)

D22:0 DMA Transfer Size

D31:23 Reserved

3.4.5 DMA CHANNEL 0 DESCRIPTOR POINTER REGISTER : (PCI 0X90)

D0 Descriptor Location
A '1' indicates PCI address space.
Note: This bit should always be set to '1' if Chained DMA enabled.

D1 End of Chain

D2 Interrupt after Terminal Count

D3 Direction of transfer
A '1' indicates transfers from local bus to PCI bus (Read Receive FIFO)
A '0' indicates transfers from local bus to PCI bus (Write Transmit FIFO)

D31:4 Next Descriptor Address

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3.4.6 DMA CHANNEL 0 COMMAND/STATUS REGISTER : (PCI 0XA8)

D0	Channel 0 Enable
D1	Channel 0 Control
D2	Channel 0 Abort
D3	Clear Interrupt
D4	Channel 0 Done
D7:5	Reserved

3.4.7 DMA ARBITRATION REGISTER : (PCI 0XAC)

Same as Mode /Arbitration Register (MARBR) (PCI 0x08 – See Section 2.2.2)

3.4.8 DMA THRESHOLD REGISTER: (PCI 0XB0)

D3:0	DMA Channel 0 PCI to Local Almost Full (C0PLAF)
D7:4	DMA Channel 0 Local to PCI Almost Empty (C0LPAE)
D11:8	DMA Channel 0 Local to PCI Almost Full (C0LPAF)
D15:12	DMA Channel 0 PCI to Local Almost Empty (C0PLAE)
D19:16	DMA Channel 1 PCI to Local Almost Full (C1PLAF) (Unused)
D23:20	DMA Channel 1 Local to PCI Almost Empty (C1LPAE) (Unused)
D27:24	DMA Channel 1 PCI to Local Almost Full (C1LPAF) (Unused)
D31:28	DMA Channel 1 PCI to Local Almost Empty (C1PLAE) (Unused)

3.5 MESSAGING QUEUE REGISTERS

Messaging queue registers are not used on the PCI/PMC-HPDI32.

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CHAPTER 4: PROGRAMMING

4.0 INTRODUCTION

This section was written for the user who is attempting to write his/her own device driver or would just like a better understanding of how the SIO4 family of cards operates. Some of the operations listed in this section may be performed by or differently from the same operation when using a General Standards provided device driver. Please see the device driver documentation for specific differences.

4.1 RESETS

Each serial communication channel of the SIO4 provides three reset sources: a transmit FIFO buffer reset, a receive FIFO buffer reset and a Zilog Z16C30 reset. Please note that performing a FIFO buffer reset while data is present in that FIFO will cause the data to be lost. Also note: since each Zilog Z16C30 chip contains two serial channels, performing a Zilog reset to either channel will reset the entire chip. For instance, performing a Zilog reset on either channel 1 or channel 2 will reset the entire Zilog chip, clearing all registers for both channel 1 and channel 2. Likewise, performing a Zilog reset of either channel 3 or channel 4 will reset the second Zilog chip and clear all the registers for channel 3 and channel 4.

4.2 FIFO ALMOST FLAGS

The FIFO buffer chips utilized on the SIO4 provide a means by which the user can determine the approximate amount of data in the FIFO. This mechanism is called FIFO almost full and FIFO almost empty flags, and these are programmable by the user. Each serial communication channel provides two 32 bit registers for setting these values: a TX FIFO Almost Register, and an RX FIFO Almost Register. Each of these registers if further broken up into two 16 bit portions, where the value in the upper 16 bits (D16 - D31) is used to program the almost full FIFO flag, and the value in the lower 16 bits (D0 - D15) is used to program the FIFO almost empty flag. The almost flags current status may be read from the respective channel's Control/Status register. These FIFO status bits are updated every 33 nanoseconds.

Each value in the corresponding portion of the almost register represents the number of bytes from each respective "end" of the FIFO. Meaning, a value of 0x00100010 in the FIFO almost register means that the FIFO almost flags will be programmed to trigger at a point 0x10 bytes from each "end" of the FIFO. This means that the almost empty flag will be asserted when the FIFO has (0x10 + 1) bytes in it, whereas the almost full flag will be asserted when the FIFO has (Total FIFO size in bytes – 0x10) bytes in it. For the standard 32Kbyte FIFO, an almost full value of 0x10 will cause the almost full flag to be asserted when the FIFO has 32752 bytes of data (32768 – 16 or 0x8000 – 0x10).

The values placed in the FIFO almost registers are programmed to the FIFO chips whenever a FIFO reset is performed; the proper steps to program these values are:

- Program the respective FIFO almost register(s)
- Perform a FIFO reset of the respective FIFO
- The value in the almost register is now programmed into the FIFO chips

Please note: if the FIFO almost registers are left at a value of 0x0 during a FIFO reset, the almost flags will be set to the FIFO chip manufacturer default of 7 bytes from empty and 7 bytes from full.

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4.3 PCI DMA

The PCI DMA functionality allows data to be transferred to/from host memory from/to the SIO4's onboard FIFO buffers with the least amount of CPU overhead. The PLX Technology PCI9080 interface chip used on the SIO4 cards handles all PCI DMA functions.

Due to the lack of interrupt sources needed by some device drivers, demand mode DMA transfers are not fully supported by the SIO4 at this time.

4.4 ZILOG Z16C30 DMA

While not a "true" DMA in the technical sense, the Zilog DMA function does provide a means for data transfer, mostly transparent to the user, to/from the Z16C30 serial controller chips from/to the SIO4's onboard FIFO buffers.

While in transmit mode, the Zilog DMA provides a mechanism by which each byte transferred to the SIO4's onboard transmit FIFO buffer, will automatically be read out by the Z16C30 chip and sent out to the cable. This operation will continue as long as the transmit FIFO buffer has data in it.

While in receive mode, the Zilog DMA provides a mechanism by which each byte read from the cable by the Z16C30 chip, will be automatically transferred to the SIO4's onboard receive FIFO buffer. This operation will continue as long as the receive FIFO buffer is not full.

4.5 INTERRUPTS

The SIO4 is capable of generating a number of interrupts to the host CPU, which may be utilized by the application code or device driver to perform various operations. Interrupt sources may include, but are not limited to, receive FIFO buffer almost empty, sync word detection, and Zilog Z16C30 serial controller chip interrupts.

4.6 Upper/Lower Connector Naming Convention

Since all the cable transceivers are bidirectional, the serial Data and Clock signals can be transmitted or received on two separate IO connector pins. The naming convention "Upper" and "Lower" is used in order to differentiate between these two pins with identical function. Typically, one pin is used for receive data, and the other pin is used for transmit. Separate controls for the transmitter/receiver enables allow the user flexibility to monitor the transmit line or perform a standalone loop back test. This also allows two SIO4 boards to be connected directly or two channels to be connected directly using standard cabling options by simply configuring the transmitter and receiver pins correctly.

Figure 5.4-2 shows the overall operation for the Upper/Lower Clock and Data signals. The clock enables are controlled from the GSC Clock Control Register (Section 2.1.2) and the data signals are enabled in the GSC Channel Control/Status Registers (starting at Section 2.1.5). Even though the clock and data lines have separate enables, they will typically be set the same. For example, if you want to transmit on the Channel 1 Upper signals and receive on the Channel 1 Lower signals, the Upper Tx Clock and Upper Tx Data will be enabled for transmit; and the Lower Rx Clock and Lower Rx Data should be enabled for receive.

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CHAPTER 5: HARDWARE CONFIGURATION

5.0 THE ON-BOARD MASTER & TRANSMIT/RECEIVE CLOCKS

The oscillator, U3, is used for generating the on-board clock. It is factory installed at 20 MHz.

The oscillator, U1, is used for generating a transmit/receive clock. It is factory installed at 20 MHz and may be changed to accommodate different baud rates. Any standard 8 or 14 pin dip oscillator will fit into the socket of U1.

5.1 EEPROM JUMPER (J12)

The jumper (J12) is a 2x3 header. These jumpers are used for manufacturer uses only. It should not be necessary for any users of the PCI-SIO4 to perform any operations involving these jumpers.

5.2 CABLE INTERFACE CONNECTIONS

There is a 68-pin DSUB (user I/O interface) connector (PLUG) mounted/soldered to the front edge of the board (Ref. Des.: PA2, for row A & PB2, for row B). The part number is P50E-068PI-SRI-TG, manufacturer, Robinsen Nugent. The mating part number is P50E68-S-TG. This cable is used for all 4 channels. See Table 4.2-1 below for pin-out.

Table 5-2.1: User Cable Pin-Out

PA2, Row A, Signal Names:	Pin #	PB2, Row B, Signal Names:	Pin #
Channel 1 Lwr Cable TXD/RXD +	1	Channel 3 Lwr Cable TXD/RXD +	35
Channel 1 Lwr Cable TXD/RXD -	2	Channel 3 Lwr Cable TXD/RXD -	36
Channel 1 Lwr Cable CTS/DCD +	3	Channel 3 Lwr Cable CTS/DCD +	37
Channel 1 Lwr Cable CTS/DCD -	4	Channel 3 Lwr Cable CTS/DCD -	38
Channel 1 Lwr Cable TX/RX Clk +	5	Channel 3 Lwr Cable TX/RX Clk +	39
Channel 1 Lwr Cable TX/RX Clk -	6	Channel 3 Lwr Cable TX/RX Clk -	40
Channel 1 Upr Cable TXD/RXD +	7	Channel 3 Upr Cable TXD/RXD +	41
Channel 1 Upr Cable TXD/RXD -	8	Channel 3 Upr Cable TXD/RXD -	42
Channel 1 Upr Cable CTS/DCD +	9	Channel 3 Upr Cable CTS/DCD +	43

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Channel 1 Upr Cable CTS/DCD -	10	Channel 3 Upr Cable CTS/DCD -	44
Channel 1 Upr Cable TX/RX Clk +	11	Channel 3 Upr Cable TX/RX Clk +	45
Channel 1 Upr Cable TX/RX Clk -	12	Channel 3 Upr Cable TX/RX Clk -	46
Channel 2 Lwr Cable TXD/RXD +	13	Channel 4 Lwr Cable TXD/RXD +	47
Channel 2 Lwr Cable TXD/RXD -	14	Channel 4 Lwr Cable TXD/RXD -	48
Channel 2 Lwr Cable CTS/DCD +	15	Channel 4 Lwr Cable CTS/DCD +	49
Channel 2 Lwr Cable CTS/DCD -	16	Channel 4 Lwr Cable CTS/DCD -	50
Channel 2 Lwr Cable TX/RX Clk +	17	Channel 4 Lwr Cable TX/RX Clk +	51
Channel 2 Lwr Cable TX/RX Clk -	18	Channel 4 Lwr Cable TX/RX Clk -	52
Channel 2 Upr Cable TXD/RXD +	19	Channel 4 Upr Cable TXD/RXD +	53
Channel 2 Upr Cable TXD/RXD -	20	Channel 4 Upr Cable TXD/RXD -	54
Channel 2 Upr Cable CTS/DCD +	21	Channel 4 Upr Cable CTS/DCD +	55
Channel 2 Upr Cable CTS/DCD -	22	Channel 4 Upr Cable CTS/DCD -	56
Channel 2 Upr Cable TX/RX Clk +	23	Channel 4 Upr Cable TX/RX Clk +	57
Channel 2 Upr Cable TX/RX Clk -	24	Channel 4 Upr Cable TX/RX Clk -	58
No connect	25	No connect	59
No connect	26	No connect	60
No connect	27	No connect	61
No connect	28	No connect	62
No connect	29	No connect	63

5.3 BOARD LAYOUT

The following figure is a drawing of the physical components of the PCI-SIO4:

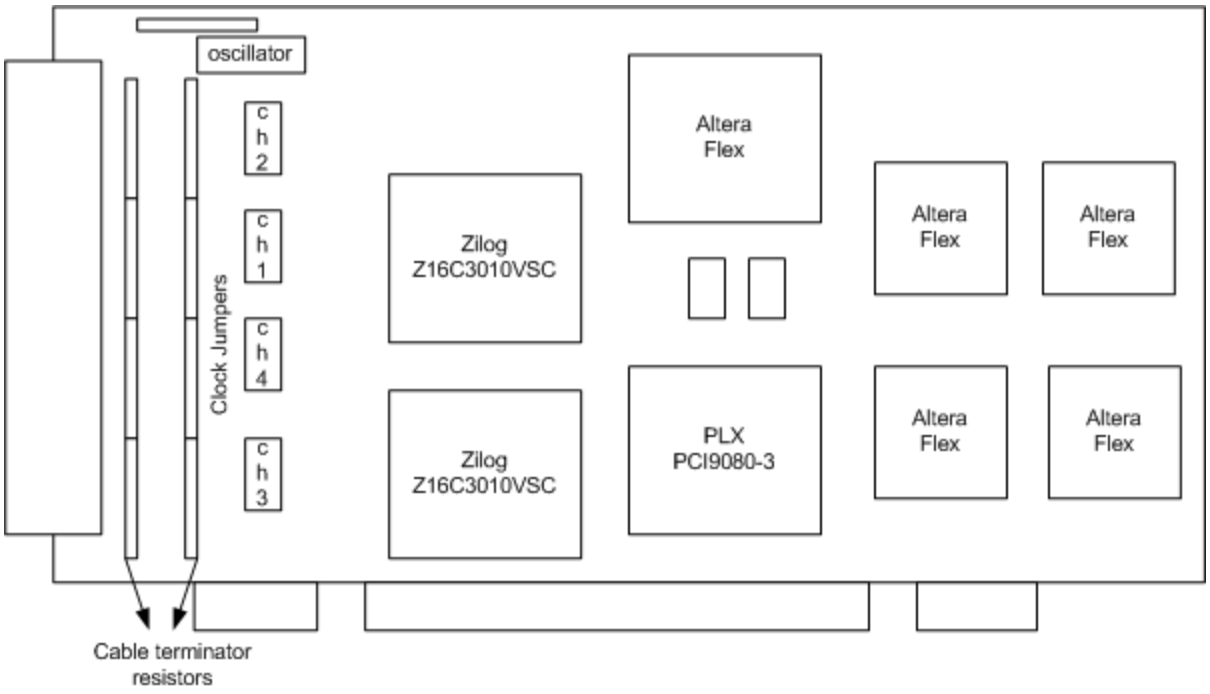


FIGURE 5.4-1: Board Layout

5.4 THE ZILOG CLOCK SELECT JUMPERS (J3, J4, J7, & J8)

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The purpose of these jumpers is to select where the Zilog clock comes from or goes to. If the Zilog clock uses the on-board transmit/receive clock, or the cable clock, then the jumpers should be installed. If the Zilog is going to generate an output clock to the cable, then some of the jumpers should not be installed. The Zilog Clock Select Jumpers are 2x8, the pin-out is shown below, there are individual jumpers for each channel, see Figure 4.3-1 below for a graphical description of how Channels 1 & 2 are configured.

Note: Channels 3 & 4 are implemented in the same manner, substituting the following parts; Jumpers J4 for Channel 3 and J7 for Channel 4:

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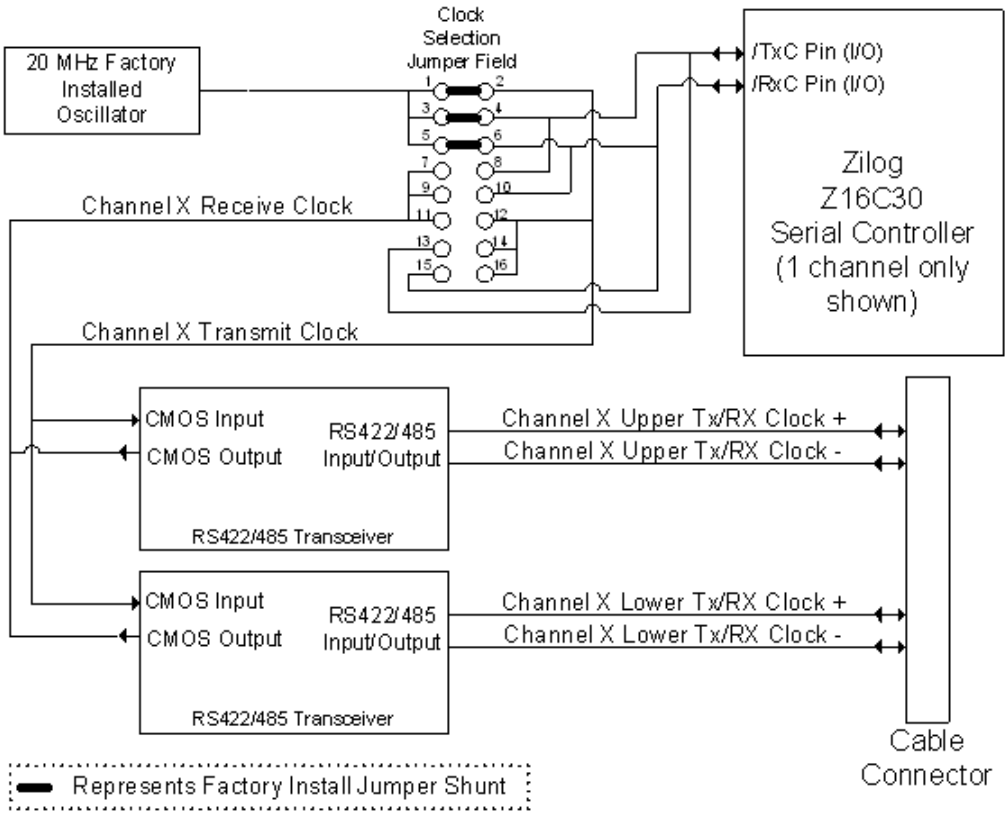


Figure 5.4-2 Clock Jumpers/Routing

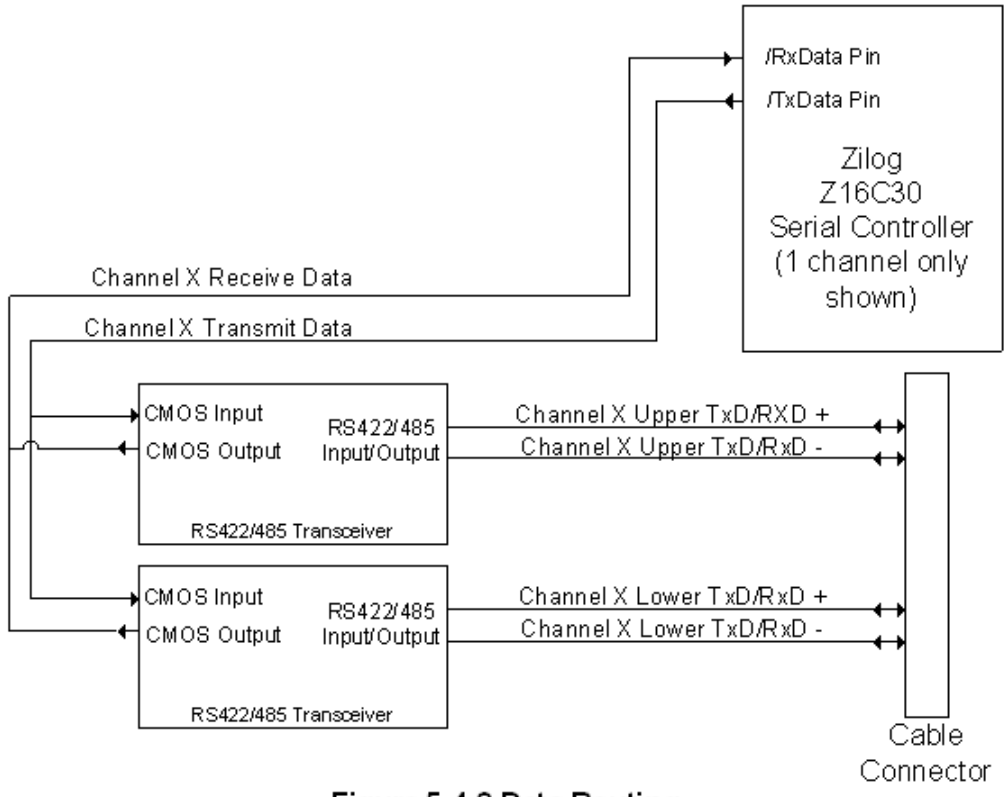


Figure 5.4-2 Data Routing

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8302A Whitesburg Drive Huntsville, AL 35802, Phone: (256) 880-8787

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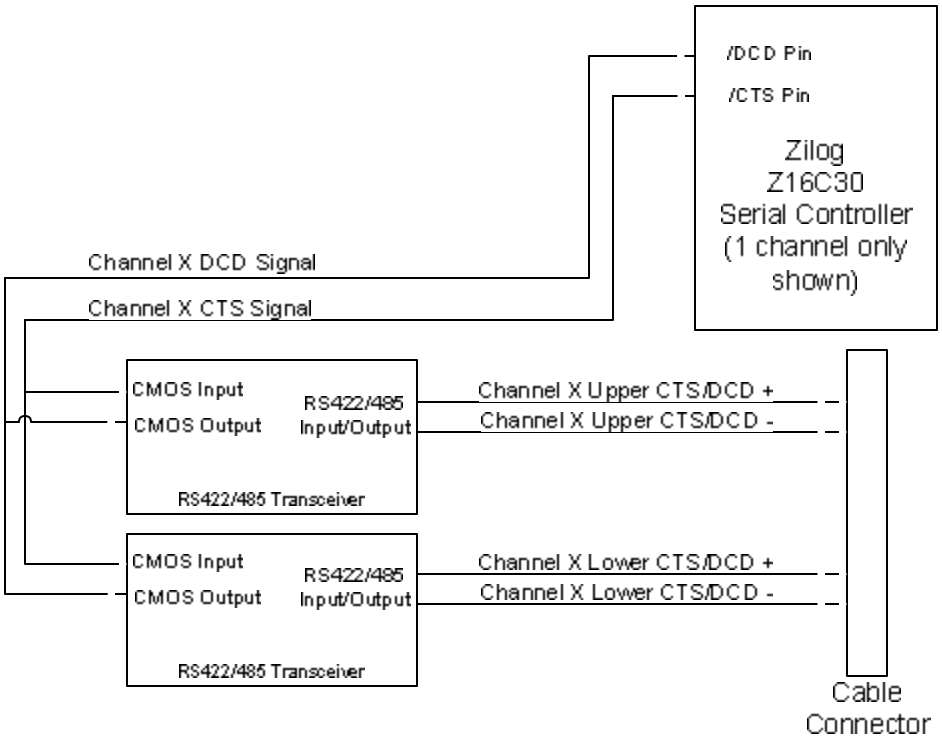


Figure 5.4-4 SIO4 CTS/DCD Routing

The "direction" of the CTS/DCD transceivers follows the data transceivers. I.e., if channel X data is configured to transmit on the "upper" portion of the cable, the CTS/DCD signal on the upper portion of the cable will also be configured as an output.
One work-around to enable receiving CTS/DCD signals while data is configured as an output, would be to wire a cable such that the CTS/DCD lines are connected to the "lower" cable portion, thus data would be transmitted on the upper cable portion, but the SIO4 can receive the CTS/DCD signal.

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CHAPTER 6: ORDERING OPTIONS

6.0 ORDERING INFORMATION

Since the SIO4 is designed to fit a variety of high-speed serial interface needs, there are several options that must be specified when ordering the SIO4 board. Please consult our sales department with your application requirements to decide on the correct ordering options.

6.0.1 CABLE INTERFACE

RS485/422 INTERFACE

The RS485/RS422 interface provides for clock speeds up to 26MHz. This is the standard interface option.

RS232 INTERFACE

The RS232 interface provides for clock speeds up to 1MHz. This is the standard interface option.

6.0.2 FIFO SIZE

The SIO4 can accept FIFOs with depths ranging from 512 bytes to 32k bytes. Larger FIFO depth is important for faster interfaces to reduce the risk of software overhead. Standard configuration of the SIO4 contains 32k byte deep FIFOs.

6.0.2 INTERFACE CABLE

General Standards Corporation can provide an interface cable for the SIO4 board. This cable is twisted pair for increased noise immunity. Several standard cable lengths are offered, or the cable length can be custom ordered to the user's needs. Versions of the cable are available with connectors on both ends, or the cable may be ordered with a single connector to allow the user to adapt the other end for a specific application. Please consult factory for more information on cabling options and pricing.

6.1 CUSTOM APPLICATIONS

Although the SIO4 board provides extensive flexibility to accommodate most user applications, custom interfaces exist, which may not exactly conform to the SIO4 interface standard. General Standards Corporation has worked with many customers to provide customized versions based on the HPDI32 board. Please consult our sales department with your specifications to inquire about a custom application.

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