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Find the *General Standards PMC-16AO12-10201* at our website: *Click HERE*

General Standards Corporation

High Performance Bus Interface Solutions

16AO12

12-Channel 16-Bit High-Speed Analog Output PMC

With 400,000 Samples per Second per Channel, and Simultaneous Clocking

Available in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC-16AO12:	**PMC**, Single-width
PCI-16AO12:	**PCI**, short length
cPCI-16AO12:	**cPCI,** 3U
PC104P-16AO12:	**PC104-*Plus***
PCIe-16AO12:	**PCI Express**
PCIe104-16AO12:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details.
Call for availability of other form factors, such as XMC, CCPMC, etc.

Features Include:

- 12 Precision High-Speed Analog Output Channels;
- 16-Bit Resolution; D/A Converter per Channel
- Data Rates to 400K Samples per Second per Channel; 4.8 MSPS Aggregate Rate
- Output Ranges of ±10V, ±5V or ±2.5V
- Output Clocking Mode Selectable as Simultaneous or Sequential
- Output Data Buffer Size Factory-Configured for 32K, 64K or 128K Channel Samples
- Analog Output FIFO Buffer Software-Configurable as Open or Circular
- Continuous and Burst (One-Shot) Output Modes Support Seamless Waveform Sequencing
- Data Rate Controlled by Adjustable Internal Clock, or by Externally Supplied Clock
- Supports Multiboard Synchronization
- Optional Differential Clock I/O Available for Synchronizing Sigma-Delta A/D Boards
- Internal Autocalibration of all Channels
- Remote Ground Sensing
- High Accuracy; 0.017% FSR max error on ±10V Range, INL = 0.007%
- Fast Settling; 5 us to 0.1%; 8 us to 0.01%;with No-filter Option
- VxWorks™ and NT Drivers™ can be provided.

Applications Include:

- ✓ Precision Voltage Source
- ✓ Industrial Robotics
- ✓ Acoustic Research
- ✓ Process Monitoring
- ✓ Waveform Synthesis
- ✓ Audio Synthesis

REV: 112712

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Overview:

The PMC-16AO-12 board contains twelve 16-bit D/A converters (DAC's), and all supporting functions necessary for adding precision high-speed analog output capability to a PCI host. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. Unique FIFO buffer controls support the seamless sequencing of successive waveforms. In less demanding applications, the outputs can be updated individually. An optional clock output for synchronizing Sigma-Delta ADC boards is available.

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller (Figure 1). Twelve analog output channels are controlled through an analog output FIFO buffer, and can be updated either simultaneously or sequentially. The output sample rate can be controlled by an internal rate generator, or by an external clock. The local controller manages all input/output configuration and data manipulation functions, including auto calibration. Analog output levels are initialized to zero (midrange). Multiboard synchronization is supported.

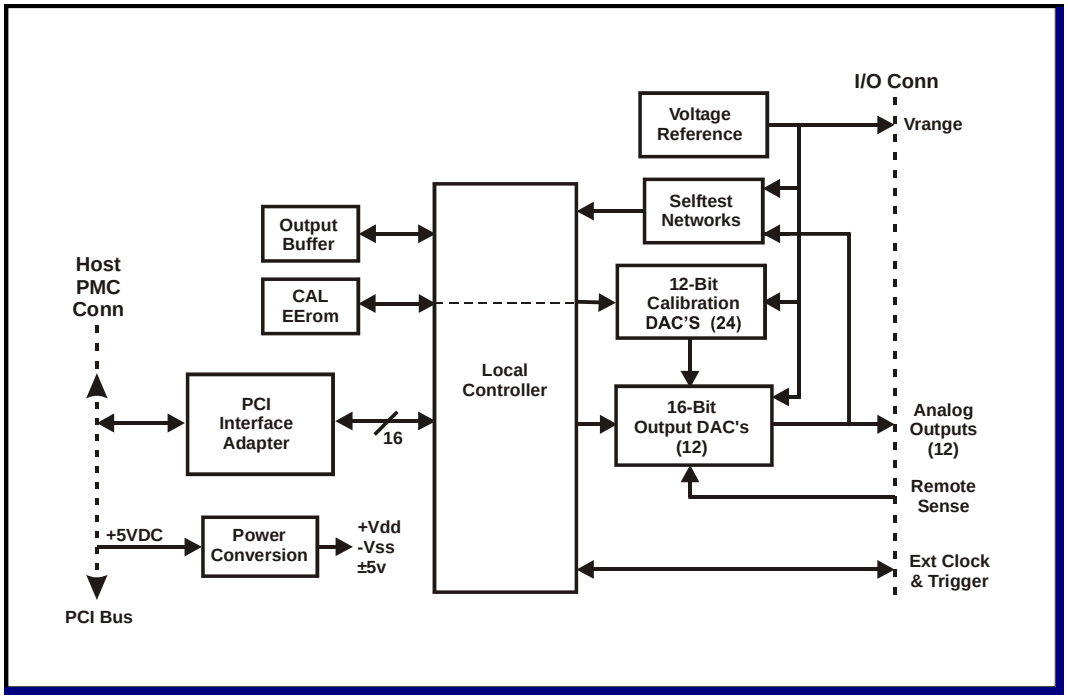


Figure 1. PMC-16AO-12 Board; Functional Organization

The board is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All analog input and output system connections are made through a single 50-pin, dual-ribbon front-access I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

Selftest networks permit all channels to be calibrated automatically to a single internal voltage reference. Offset and gain trimming of the output channels is performed by calibration DAC's that are loaded with channel correction values during initialization. The correction values are determined during auto calibration, and are stored in nonvolatile EEprom for subsequent transfer to the calibration DAC's. Either auto calibration or initialization can be invoked at any time by asserting a single control bit in the board control register.

Electrical Specifications

(At +25 ^{O}C, with specified operating voltages)

Analog Output Channels

Output Characteristics:

Configuration:	Twelve single-ended analog output channels, with dedicated 16-Bit DAC per channel; Optional 4-channel and 8-Channel configurations available.
Voltage Ranges:	Factory configured as ±10 Volts, ±5 Volts or ±2.5 Volts
Output Resistance:	1.0 Ohm maximum
Output protection:	Withstands sustained short-circuiting to ground without damage
Load Current:	±5 ma maximum; ±2 ma recommended for minimum crosstalk and line loss
Load Capacitance:	Stable with zero to 2000 pF shunt capacitance
Settling Time (Typical):	No Filter : 7 us to 0.1%, 9 us to 0.01% 100 kHz Filter: 14 us to 0.1%, 18 us to 0.01% 10 kHz Filter: 100 us to 0.1%, 140 us to 0.01%
Noise:	No Filter: 1.3 mVRMS, 10Hz-10MHz 10 kHz Filter: 0.4 mVRMS, 10Hz-10MHz
Glitch Impulse:	±2.5V Range: 3 nV-Sec max. ±5V Range: 5 nV-Sec ±10V Range: 8 nV-Sec
Remote Sensing:	Single input pin compensates for ground potential at load. Maximum range ±1.0 Volt. Correction ±1 percent. Enabled or disabled by control software.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Clocking Rate:	Internal Rate Clock: 460 to 400,000 samples per second per channel External Rate Clock: 0 to 400,000 samples per second per channel

DC Accuracy:
(Max error, no-load)

Range	Midscale Accuracy	±Fullscale Accuracy
±10V	±2.4mv	±3.3mv
±5V	±1.7mv	±2.2mv
±2.5V	±1.4mv	±1.6mv

Bandwidth: (Single-pole lowpass)	10 kHz, 100 kHz and No-Filter (300 kHz) options, Typical at -3dB.
Crosstalk Rejection:	80 dB minimum, DC-10 kHz
Integral Nonlinearity:	±0.007 percent of FSR, maximum
Differential Nonlinearity:	±0.003 percent of FSR, maximum

Operating Modes and Control

DAC Clocking Source: Internal rate generator, external hardware input, or software clock.

Multiboard Clocking Configurations: To support the simultaneous clocking of DAC outputs on multiple boards, the 16AO12 can be software-designated as either a clock initiator or a clock target. Initiators provide an output clock for target boards, each of which retransmits the clock signal to subsequent boards connected in a daisy-chain configuration.

TTL I/O Synchronization:
(Option: "TTL I/O")

An initiator transmits its DAC output clock through the TTL Clock Out pin. A target board receives its DAC clock through the TTL Clock I/O pin, and retransmits the clock through the Clock Output pin.

Differential I/O Synchronization:

For systems requiring 16AO12 boards to be synchronized with GSC's sigma-delta analog input boards which use high-frequency reference signals for multiboard synchronization, the 16AO12 can be configured with differential LVDS clock I/O and a 16MHz to 32MHz adjustable high frequency rate generator. Adjustment resolution of the rate generator is 0.2-percent or less.

Sigma-Delta Board(s) Synchronized to a 16AO12:
(Option: "Differential Sync I/O without Clock I/O termination")

The 16AO12 transmits a high-frequency reference signal through the Clock I/O port (software-configured as an output), and divides the reference internally to its DAC clocking frequency. The sigma-delta board divides the reference down to its input sample clock frequency, and can retransmit the reference to multiple sigma-delta target boards. 16AO12 Clock I/O termination is omitted to reduce LVDS transmitter loading.

Sigma-Delta and 16AO12 Boards Synchronized to a single 16AO12:
(Initiator Option: "Differential Sync I/O without Clock I/O termination")
(Target Option: "Differential Sync I/O with Clock I/O termination")

A 16AO12 initiator transmits a high-frequency reference signal through the Clock I/O port (software-configured as an output) for sigma-delta targets, and divides the same reference internally to its DAC clocking frequency. The DAC clock is also transmitted through the Clock Output port to 16AO12 targets.

Multiple 16AO12 Boards Synchronized to a Sigma-Delta board:
(Option: "Differential Ext Rate Gen I/O")

A 16AO12 receives the high frequency reference signal from a sigma-delta board through the Clock I/O port, which is software-configured as an input. The reference is divided down to the 16AO12 DAC clocking frequency, and is transmitted to subsequent 16AO12 target boards through the Clock Output port. (This option is also available in a TTL configuration, which limits the interboard cable length to several inches).

16AO12 Boards Synchronized to a Single 16AO12:

Same as "TTL I/O synchronization," with the single-ended TTL signals replaced by differential LVDS signals.

Operating Modes and Control (Continued)

Burst Trigger:	Software control bit, or external TTL trigger input (Same as clock I/O option). Burst triggering also can be obtained from an external source.
Update Mode:	Simultaneous or channel-sequential output updating
Active Buffer Size:	From 4 output values to 32K, 64K, or 128K-values, in 2:1 steps.
Buffer Mode:	Selected as Circular for periodic waveforms, or as Open for one-shot functions
Data Format:	Software selected as offset binary or Two's complement

PCI Compatibility

Conforms to PCI Specification 2.3, with 33 MHz D32 read/write transactions.
Multifunction interrupt.
Supports DMA transfers as bus master.

Power, Mechanical and Environmental Specifications

Power Requirements:

+5VDC ±0.2 VDC at 1.3 Amps maximum, 1.0 Amp typical. Outputs fully loaded.

Maximum Power Dissipation:	Side-1: 5.2 Watts max; 4.1 Watts typical Side-2: 1.3 Watts max; 0.9 Watt typical.

Mechanical Characteristics: (PMC Form Factor)

Height:	13.5 mm (0.53 in)
Depth:	149.0 mm (5.87 in)
Width:	74.0 mm (2.91 in)
Shield:	Side 1 is protected by an EMI shield.

Environmental Requirements:

Ambient Temperature Range:	Operating: 0 to +65 degrees Celsius inlet air Storage: -40 to +85 degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling.

Ordering Information

Specify the basic product model number (PMC-16AO-12), followed by an option suffix "-ABCDE", as indicated below. For example, model number PMC-16AO-12-10201 describes a board with a ±5 Volt output range, no output filter, 12 output channels, a 32K-Sample buffer, and non-differential sync I/O.

Basic Model Number	Form Factor
PMC-16AO12	PMC (Native)
PCI-16AO12[1]	PCI, short length
cPCI-16AO12[1]	cPCI, 3U
PCIe-16AO12[1]	cPCI, 3U
PC104P-16AO12	PC104-*Plus* (Native)
PCIe104-16AO12[1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Output Range:	±2.5 Volts	A = 0
	±5 Volts	A = 1
	±10 Volts	A = 2
Output Lowpass Filter:	No output Filter	B = 0
	10 kHz Output Filter	B = 1
	100 kHz Output Filter	B = 2
Number of Output Channels:	4 Channels	C = 0
	8 Channels	C = 1
	12 Channels	C = 2
Output Buffer Size:	32K Samples	D = 0
	64K Samples	D = 1
	128K Samples *	D = 2
Sync I/O Configuration	TTL (non differential) I/O	E = 1
	Differential LVDS I/O, with Clock I/O termination	E = 2
	Differential LVDS I/O, without Clock I/O termination	E = 3
	Differential LVDS Ext Rate Gen I/O	E = 4
	TTL Ext Rate Gen I/O	E = 5

* Contact factory for availability.

System I/O Connections

Table 1. System Connector Pin Functions

P5A		P5B	
PIN	SIGNAL	PIN	SIGNAL
1	OUTPUT RETURN	1	OUTPUT RETURN
2	OUTPUT CHANNEL 00	2	REMOTE GROUND SENSE
3	OUTPUT RETURN	3	OUTPUT RETURN
4	OUTPUT CHANNEL 01	4	OUTPUT RETURN
5	OUTPUT RETURN	5	VRANGE RETURN
6	OUTPUT CHANNEL 02	6	VRANGE OUTPUT
7	OUTPUT RETURN	7	VRANGE RETURN
8	OUTPUT CHANNEL 03	8	OUTPUT RETURN
9	OUTPUT RETURN	9	OUTPUT RETURN
10	OUTPUT CHANNEL 04	10	OUTPUT RETURN
11	OUTPUT RETURN	11	OUTPUT RETURN
12	OUTPUT CHANNEL 05	12	OUTPUT RETURN
13	OUTPUT RETURN	13	OUTPUT RETURN
14	OUTPUT CHANNEL 06	14	OUTPUT RETURN
15	OUTPUT RETURN	15	OUTPUT RETURN
16	OUTPUT CHANNEL 07	16	OUTPUT RETURN
17	OUTPUT RETURN	17	DIGITAL RETURN
18	OUTPUT CHANNEL 08	18	TRIG INPUT *
19	OUTPUT RETURN	19	TRIG INPUT RETURN *
20	OUTPUT CHANNEL 09	20	TRIG OUTPUT *
21	OUTPUT RETURN	21	TRIG OUTPUT RETURN *
22	OUTPUT CHANNEL 10	22	CLOCK I/O **
23	OUTPUT RETURN	23	CLOCK I/O RETURN **
24	OUTPUT CHANNEL 11	24	CLOCK OUTPUT *
25	OUTPUT RETURN	25	CLOCK OUTPUT RETURN *

* Available optionally as LVDS differential pairs (Differential Sync I/O option).

** Differential pair in the Differential Sync I/O configuration; selectable as either an input or an output clock signal.

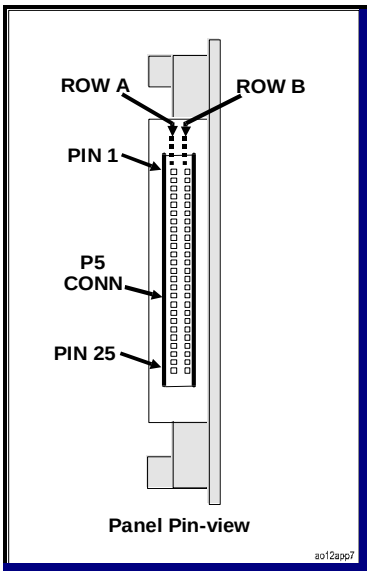


Figure 2. System Input/Output Connector

System Mating Connector:
Standard 50-pin 0.050"
Dual-ribbon socket connector;
3M# P50E-050S-EA.

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